Chapter 7
ITRS 2028—International Roadmap of Semiconductors

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Abstract In CHIPS 2020, we based our discussion on the 2009 edition of the ITRS, looking forward to 2024. Its 5-year predictions for 2014 have been surpassed by the product introduction of 16 nm Flash (prediction: 20 nm), and the predictions have been reached for processors in 2014 with 24 nm. The 2013 edition has pushed back some of the 2024 data. For comparison, the 2013–2014 reality shows very clearly, that functional chip products are settling at 14 nm for SRAM and Flash, 20 nm for DRAM, and 24 nm for processors. The aggressive data in the ITRS, 5 nm in 2028, are hard to support, with less than one doping atom in the transistor channel and no large-scale lithography in sight for <7 nm.

7.1 General Observations

The International Technology Roadmap of Semiconductors (ITRS) continues its aggressive "one-dimensional" nanometer strategy with

(a) defining nanometer "nodes" out to 1.x nm that no longer have any correlation with either transistor channel-lengths or gate half-pitch, respectively first-metal half-pitch (Table 7.1),
(b) postulating min. metal half-pitch scaling progress (Table 7.1) with math formulas that have no correlation with scientific/technical publications,
(c) using standard lists of challenges in reaching the scaling projections.

The relevance of such a nanometer roadmap becomes increasingly limited. As the 2013 report observed in its introduction, in hindsight, all long-term projections beyond 5 years (and certainly the 15-year time span of the bi-annual editions of the roadmap) had to be reduced again and again, as is particularly evident in the projections for the maximum clock frequency as shown in Fig. 7.1 [3].

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Table 7.1 Master plan of critical parameters, 2013 edition

Year	2015	2020	2025	2028
Node (nm)	10	4	1.8	?
Logic 1/2 pitch (nm)	32	20	10	7
2D Flash 1/2 pitch (nm)	15	10	8	8
DRAM 1/2 pitch (nm)	24	15.5	10	7.7
FinFET 1/2 pitch (nm)	24	13.5	7.5	5.3
Fin width (nm)	7.2	6.3	5.4	5.0
6T SRAM cell area (nm^2)	6×10^4	2×10^4	6×10^3	3×10^3
NAND flash (b/chip)	128/256 Gb	512 Gb/1T	2T/4T	4T/8T
Flash layers	16–32	40–76	96–192	192–384
DRAM (Gb/chip)	8	24	32	32
Wafer diameter (mm)	300	450	450	450
VDD (V)	0.83	0.75	0.68	0.64
CV/I (ps)	0.65	0.5	0.4	0.3

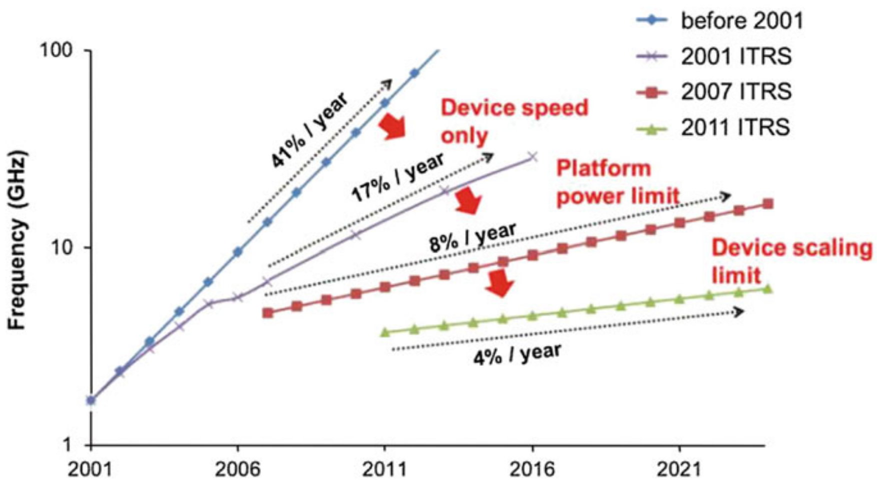

Fig. 7.1 Corrections of the Roadmap for max. clock frequency between 2001 and 2013 from 41 %/year to 4 %/year [3] *Source* Sematech

Projecting clock frequencies >10 GHz in 2000 had limited value, when it was already evident [1] that the limit would be <5 GHz because of limits on operating voltage, max. currents, over-estimated because of simplistic models, and because of RC delays of interconnects. Bandwidths- and density-estimates in the 2009 road-map received a review in [2], and reality obviously was included in the state-of-the-art starting data of the 2013 edition.

7.2 ORTC—Overall Roadmap Technology Characteristics

The important ORTC forecast table shows new labels and new characteristics, which have become critical in the assessment of progress. Table 7.1 is a condensed adaptation and interpolation regarding the 2020 column. As to the critical items:

The simplistic node-naming has been maintained, although it no longer has any correlation with the minimum features or channel-lengths of transistors on any chip at that node. Therefore, any one of these node names is identified in the four following lines by its 1/2 pitch, (line + space)/2, for M1 in logic, rows of NAND transistors in 2D Flash memory, rows of transistors in DRAM, and minimally spaced fins of FinFET's, respectively. The pace of scaling on paper has been slowed to 70 % in 4 years or 50 % in 8 years, respectively. Final limits are stated in the 2013 report for 2D NAND Flash at 12 nm and for DRAM at 14 nm, presumably, channel length, but contrasting with the values in the table, anyway. To judge the relevance of the data in the table, we should have in mind that

- **In a Si cube of $(10\ \text{nm})^3$, a doping level of $10^{18}/\text{cm}^3$ means just 1 active p- or n-type atom.**

Since the transistor characteristics are determined by these dopant-atom numbers N within a channel and since their standard deviation is $(N)^{1/2}$, any such numbers N < 10 to 50 make such transistors useless for large-scale integration. This observation is one reason why any of the scaled data, at least beyond 2020, have a limited relevance.

7.3 System Drivers

The System-Drivers Summary in the 2013 ITRS report is governed by the

- Design-Capability Gap:

Although dimensional scaling advanced, at least until 2013, this progress could not be designed into an equivalent progress in transistor density. This statement does not even consider the additional negative effect of scaling on transistor variability.

The design-capability gap is widened further by the handicapped scaling of all Metal pitches due to resistance, granularity, crosstalk and manufacturing problems. 3D integration is mentioned as a relief, however, only in the manner of the vertical poly-Si NAND flash, and not in the sustainable, monolithic 3D strategy, as presented in Chap. 3 in this book.

Admitting that geometry scaling effectively does not offer any density, cost or performance advantages, the report generated the DES = "Design Equivalent Scaling" as the expected performance improvements "per node" by

- Error-correcting codes,
- Lithographic-patterning-related design rules,
- Adaptive voltage and frequency scaling,
- Clock gating,

in other words, "engineering cleverness", advocated by Gordon Moore as early as 1975 to maintain the Roadmap.

7.4 PIDS—Process Integration, Devices and Structures

This part states the challenges for

- Logic
- DRAM
- Non-volatile Memory.

Its tables of difficult challenges are organized in near-term, 2014–2020, and long-term, 2021–2028.

Immanent scaling limits are quoted everywhere, and the leading hit-words for progress are:

- Multi-gate transistors,
- Gate insulators with a high dielectric constant,
- III–V materials for transistor channels,
- Vertical transistor stacks for NAND Flash NV memory.

The new no. 1 issue is the reliability of devices and circuits, which suffer from variability, ageing, and breakdown related to further reduction of the volume of devices and their interconnects.

7.5 ERD—Emerging Research Devices

The challenges listed in this chapter are the same as in the other chapters like PIDS and SD. No emerging devices are mentioned other than the hit-words in PIDS (see Sect. 7.4). The alternative demand for memories is the replacement of SRAM and Flash by 2018 without any suggestions. No short-term incorporation of III–V channels is envisioned.

7.6 Interconnects

The goal for interconnects on-chip is Tb's per second at the energy level of fJ/b. However, it is stated that no tangible progress has been made between 2009 and 2013 due to basic material limitations, both regarding the metal layers as well as the isolation layers. Therefore, as detailed in Chap. 5, the energy levelled off at ~1 pJ/b. No solutions were found with relative dielectric constants <2. A partial remedy was introduced with air gaps in NAND Flash. The potential of 3D integration is quoted regarding through-silicon vias, but there are no indications of the potential of monolithic 3D integration (see Chap. 3) or of directed self-assembly (DSA) as techniques to fundamentally shorten the interconnects.

7.7 RF-AMS: Radio-Frequency and Analog-Mixed-Signal Technologies

The continuing progress of THz transistors leads to optimistic projections for frequency limits.

Figure 7.2 and high-frequency power-amplification capabilities. The sustained performance level of Silicon-Germanium transistors is proof of the unique significance of this central part of the periodic table (Fig. 7.3).

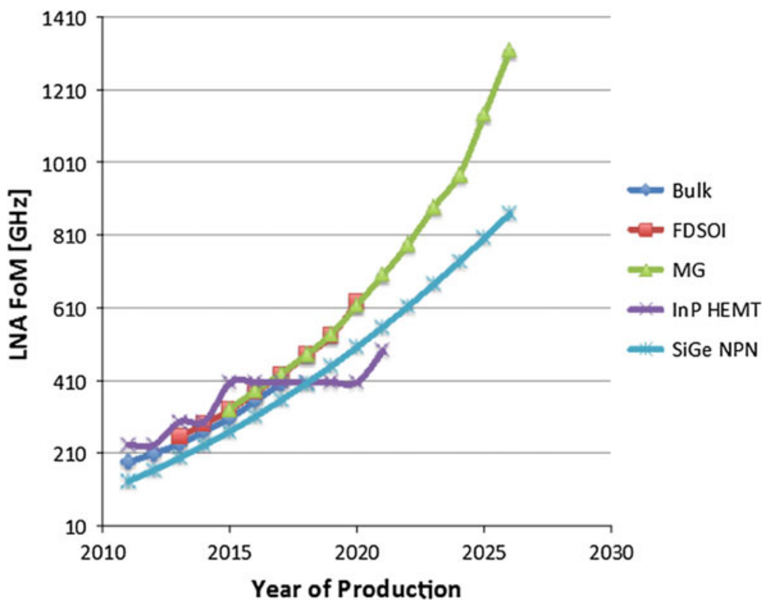

Fig. 7.2 Unity-gain frequency figure-of-merit of THz transistors [3]

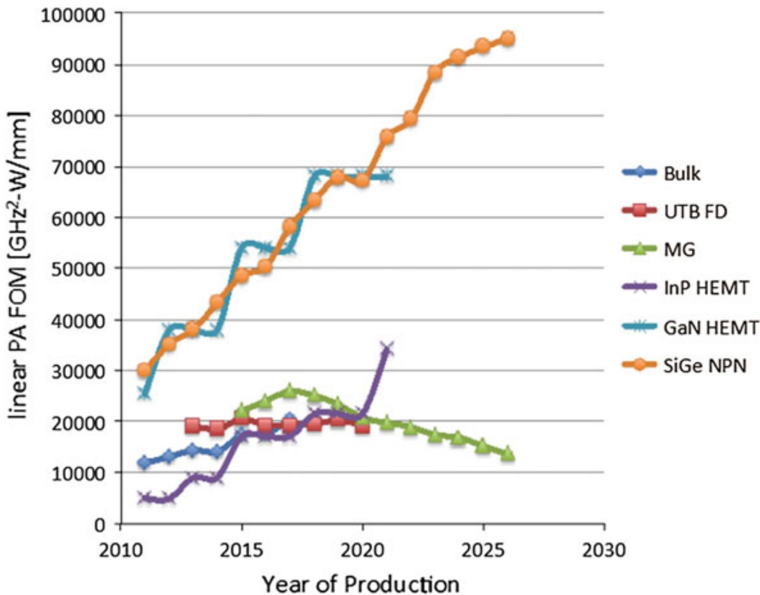

Fig. 7.3 Power-amplification figure-of-merit of RF transistors [3]

7.8 Conclusion

The ITRS has been under pressure at least since 2010 because of its "one-dimensional" exponential-growth philosophy. It had and has no energy- and no monolithic-3D-strategy. The advent of 3D chip stacks for DRAM and Flash memory since 2006 came as a surprise to save Moore's law in the face of the continuous down-ward corrections of progress on the ITRS. Nevertheless, the ITRS has had the unique effect of focusing development resources in the semiconductor industry.

It could continue to play this role, if future editions of the ITRS would concentrate on a holistic strategy for monolithic and heterogeneous 3D integration with energy efficiency of nanoelectronics as milestones.

References

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