Chapter 4
Analog-Digital Interfaces—Review and Current Trends

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Abstract By updating the figure-of-merit plots presented in CHIPS 2020 using new survey data collected over the years 2011–2015, this chapter discusses asymptotes and extracts recent improvement rates in the area of low-power, high-performance A/D conversion. Moreover, five years after the writing of CHIPS 2020, the developments in current architectures will be re-iterated, and the emerging concept of analog-to-information conversion will be discussed.

4.1 Introduction

Five years after our survey on analog-to-digital converters (ADCs) in *CHIPS 2020—A Guide to the Future of Nanoelectronics* [1], innovation and progress in data converter design is alive and well. In 2010, we had predicted that the future will bring further improvements in power efficiency, fueled by a combination of technology scaling, minimalistic design and digital assist. The purpose of this chapter is to provide a reality check, quantify recent progress and document the state-of-the-art.

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4.2 General ADC Performance Trends

In order to illustrate the progress made over the past five years, we consider the conversion energy and conversion bandwidth plots that were introduced in [1]. As before, the data used for the plots shown in Fig. 4.1 is taken from the online survey data of [2], now extended up to the most recent data set from the 2015 International Solid-State Circuit Conference (ISSCC). From the points added between 2010 and 2015 (marked in gray), one can immediately see that there has been significant progress.

As far as the conversion energy (power divided by Nyquist sampling frequency) in Fig. 4.1a is concerned, we can summarize the key observations as follows. First, there are now 15 designs that reported a Walden figure-of-merit (FOM_W) [3] of less than 10 fJ/conversion-step. In 2010, there was only one such design. Second, while we see improvements across the board, the successive approximation register (SAR) architecture stands out and now clearly dominates the low-energy design space. We will return to this point in Sect. 4.3. Third, and most importantly, we observe that the leading-edge designs for a signal-to-noise and distortion ratio (SNDR) beyond 50 dB align well with a slope of 4× per 6 dB (1 bit). As discussed in [1], this slope corresponds to the "thermal slope," i.e., the trade-off for circuits that are limited by thermal noise. The important conclusion to draw from this is that we have pushed our designs closer to thermal limits, indicating a higher degree of optimization away from technology-imposed limits.

The fact that most leading-edge designs (with SNDR > 50 dB) now follow the thermal slope has led to the widespread adoption of a figure-of-merit that takes this trade-off into account. Recall from [1] that the Walden FOM assumes a slope of 2× per 6 dB, which no longer fits the leading edge (see Fig. 4.1a). The so-called Schreier FOM_S was first defined in [4] and is based on a 4x per 6 dB slope in the trade-off between energy and dynamic range (DR). For our discussion below, we will utilize a modified version of this FOM that includes distortion [5], i.e., DR is replaced by SNDR:

$$FOM_S = SNDR(\text{dB}) + 10\log\left(\frac{f_{snyq}/2}{P}\right) \tag{4.1}$$

Here, P stands for ADC power consumption and f_{snyq} is the Nyquist output sample rate of the ADC (twice the conversion bandwidth). The bold dashed line in Fig. 4.1a corresponds to FOM_S = 175 dB, which can be viewed as the state of the art. It is also worth noting that the data we use for SNDR are based on an input frequency near Nyquist to enable a fair comparison (see [2] for a discussion on this subject).

As far as the conversion bandwidth[1] plot in Fig. 4.1b is concerned, we observe that the improvements are significant, but not as pronounced as for conversion

[1]We define the conversion bandwidth as the highest input frequency for which the plotted SNDR was measured. This frequency is typically $f_s/2$ with exceptions noted in the fin_hf column of [2].

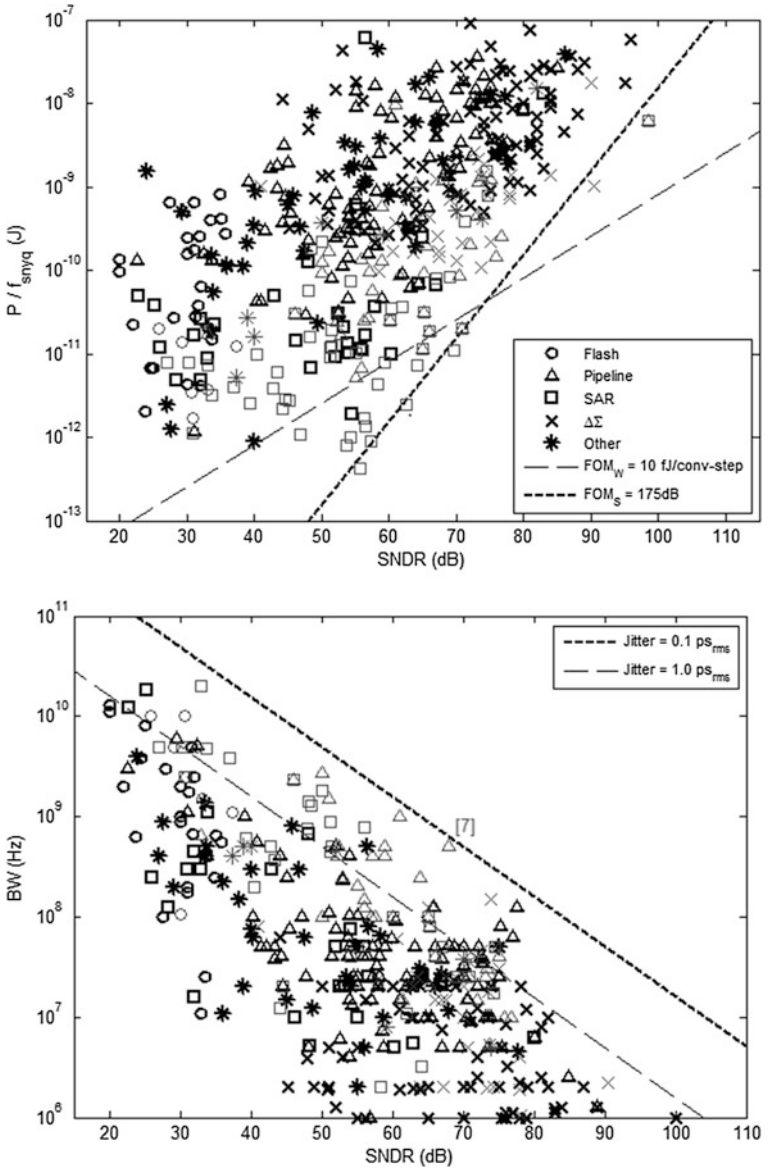

Fig. 4.1 ADC performance data (ISSCC 1997–2015 and VLSI circuit symposium 1997–2014). The *gray markers* indicate data reported after 2010. Conversion energy (**a**) and conversion bandwidth (**b**) versus SNDR

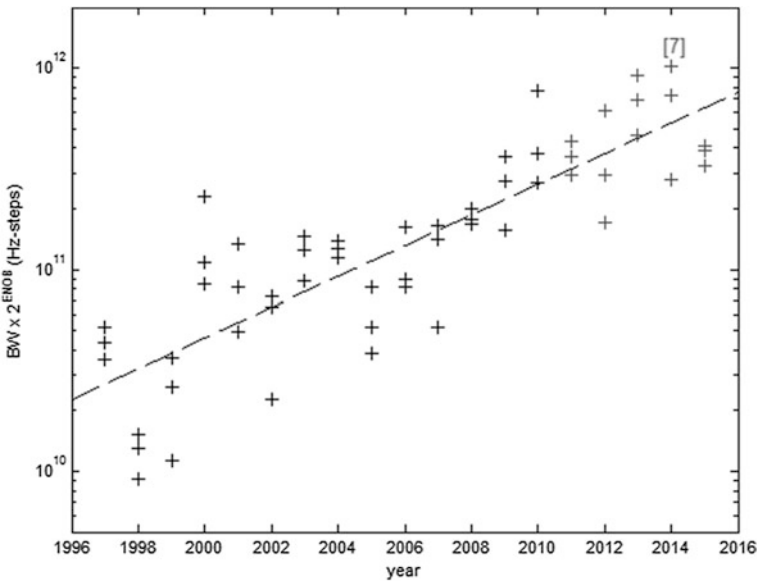

Fig. 4.2 Fit to speed-resolution product of the top 3 designs in each year. The fit line has a slope of 2×/4 years

energy. The reason for this is that the speed-resolution product is limited by our ability to make a low-jitter clock, and it is generally difficult to achieve a standard deviation better than 50 fs_{rms} [6]. The data point with the best combination of bandwidth and SNDR is [7], located at an equivalent aperture jitter of 127 fs. Note that since this converter suffers from other nonidealities, the actual clock jitter in this design must be significantly better.

To look into the conversion bandwidth trends more closely, we re-plot the speed-resolution chart (Fig. 4.2b) in [1] as shown in Fig. 4.2. From here we see that only two designs reported after 2010 surpass the speed-resolution product of [8] (which is the peak point for 2010). The overall progress slope for the speed-resolution product indicates a doubling every 4.0 years (was 3.6 years until 2010 [1]). Finally, we note that many other SAR-based designs have now managed to pass the line for 1 ps_{rms}. However, pipelined ADCs (like [7]) still dominate the performance in the 60–80 dB range, mostly driven by the needs for wireless base stations [9].

Given that (1) has emerged as a figure-of-merit that not only accounts for the fundamental thermal noise trade-off, but also does a good job at fitting the recent leading edge, it makes sense to use FOM_S for quantifying conversion-efficiency trends and efficiency-speed tradeoffs. In absence of an acceptable figure-of-merit, our previous analysis [1] used 3D fitting to extract the progress rate in conversion efficiency. Using FOM_S, we can now look at the data in two dimensions, which allows us, among other things, to plot efficiency versus speed.

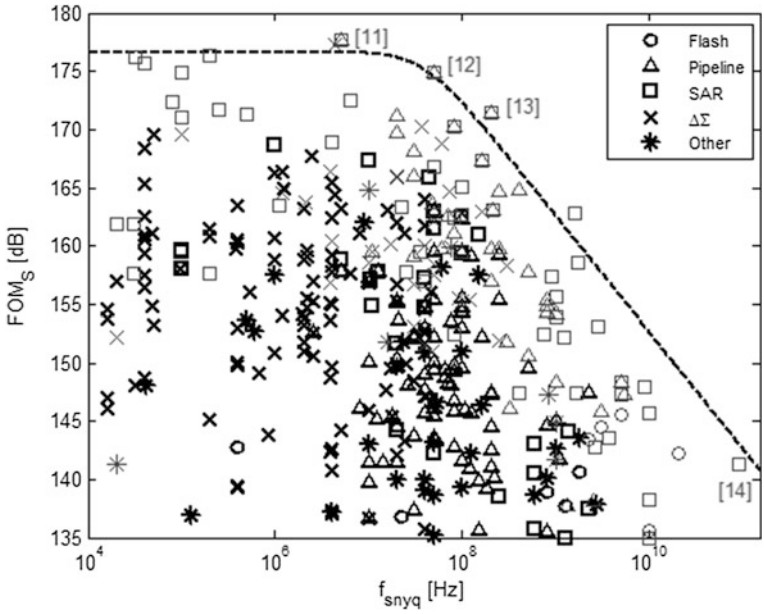

Fig. 4.3 FOM_S versus Nyquist sampling rate. The *gray markers* indicate data reported after 2010

From the plot in Fig. 4.3, we make the following observations. First, note that as expected, the achieved FOM_S is highest for low conversion rates. At frequencies between 10 and 100 MHz, the efficiency begins to deteriorate and rolls off with a slope of approximately −10 dB per decade. As discussed in [10], this indicates that power dissipation scales with the square of speed in this regime. Also notice from the plot that the pipelined SAR designs [11–13] set the peak performance near the corner. The time-interleaved SAR design of [14] marks the rightmost point in this chart and, interestingly, lies almost exactly on the −10 dB/decade roll-off of the drawn envelope. The envelope is constructed by taking the average of the top five data points to define the horizontal asymptote, and the average of the top five designs along a −10 dB roll-off to define the location of that asymptote.

As we can see from Fig. 4.3, the contributions of the past five years have pushed the asymptotes up and to the right. It is interesting to quantify the rate at which this movement occurs. This is done for the location of the low-frequency (LF) asymptote in Fig. 4.4. We observe that the improvements have followed a steady pace with minor variations from year to year (likely due to the finite sample size of the data). Interestingly, the overall progress rate comes out almost exactly to 1 dB per year (or doubling of power efficiency every 3 years). In this context, it is interesting to re-visit the fundamental-limit discussion presented in [1]. There, we noted that a useful bound on conversion energy is given by [15, 16]:

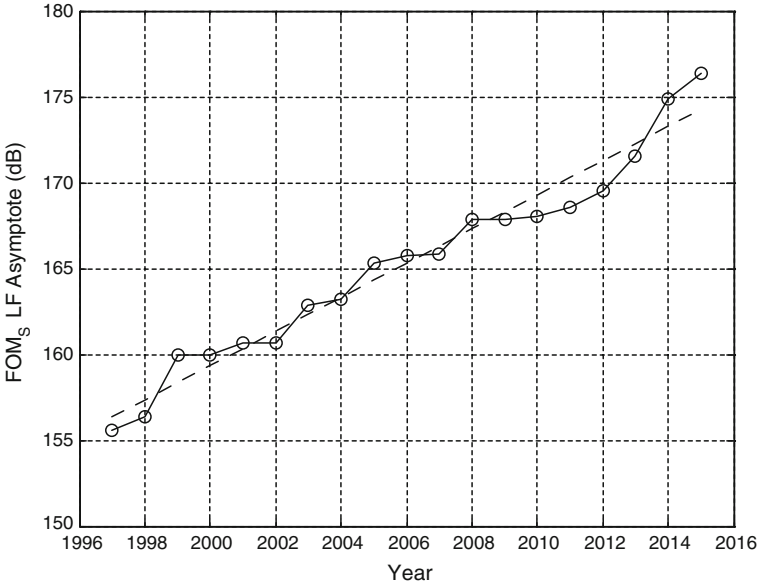

Fig. 4.4 FOM$_S$ trend (low-frequency asymptote)

$$\left(\frac{P}{f_{snyq}}\right)_{min} = 8\ \text{kT} \times SNR \tag{4.2}$$

Approximating SNDR ≅ SNR and inserting into (4.1) gives (assuming room temperature):

$$FOM_{S,max} = SNR(\text{dB}) + 10\ \log\left(\frac{1}{16\ \text{kT} \times SNR}\right) = -10\ \log(16\ \text{kT}) = 192\ \text{dB} \tag{4.3}$$

Since this bound includes only the energy to drive a sampler using an ideal (class-B) amplifier, it is clear that we will likely never reach this number. A more practical limit may be 186 dB, which would be reached in about ten years, assuming that we can maintain the 1 dB per year progress rate.

To extract the rate, at which the high-frequency asymptote of Fig. 4.3 moves to the right, we use FOM$_S$ = 150 dB as an arbitrary reference point and measure (for each year) up to which frequency this level of efficiency is maintained. This yields the plot of Fig. 4.5, from which we observe doubling every 1.8 years, or 10× every 5.9 years (1.7 dB per year). These numbers quantify the rate of power-efficiency improvement for high-speed designs. Since the low- and high-frequency asymptotes shift at different rates, the corner shifts to the right over time. While it was located at about 1.4 MHz in 1997, the corner now occurs at about 42 MHz.

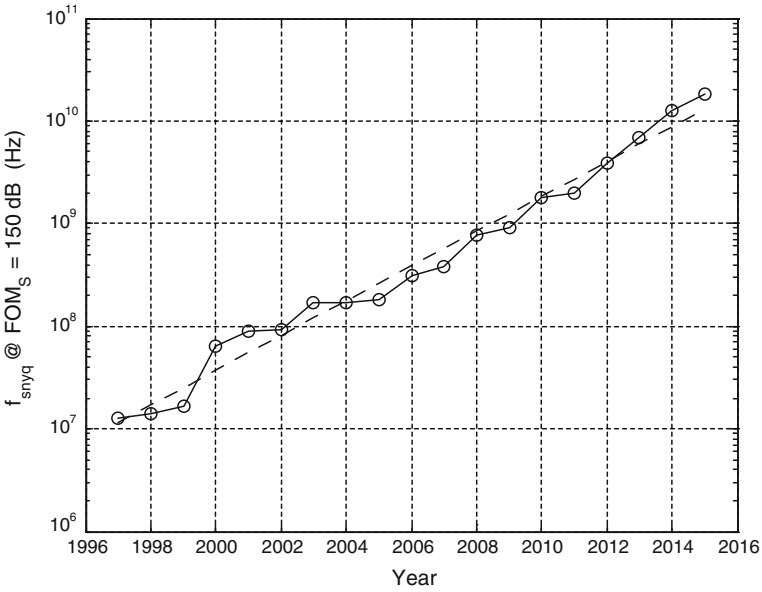

Fig. 4.5 FOM_S trend (high-frequency asymptote)

4.3 Trends in Nyquist A/D Converters

An interesting consequence of the relentless optimization and improvements seen above is the increasing competition among ADC architectures. While it was relatively straightforward to make architectural decisions in the past, today's ADC designer is confronted with an overlapping design space offering multiple solutions that are difficult to differentiate in their suitability. For example, the design space for pipelined ADCs has been encroached by time-interleaved SAR converters. Similarly, wideband delta-sigma converters such as [17] now offer bandwidths that were previously only achievable with Nyquist converters (see also Sect. 4.4).

Figure 4.6 gives an indication on architectural trends. As we had already noted in [1], the SAR architecture continues to be actively researched and conforms with the general trend toward "minimalistic," opamp-less Nyquist ADC architectures. In order to extract high-speed from the SAR topology, time interleaving is typically needed. This explains in part an up-tick in the number of reported designs that use time interleaving, illustrated in Fig. 4.7. More generally, this trend is of course also supported by the increasing integration density available in silicon, which has also enabled multi-core microprocessors.

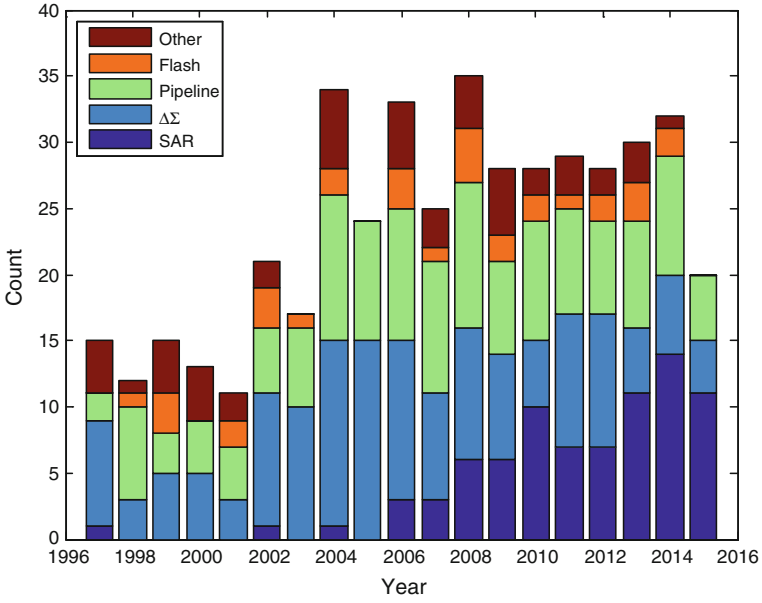

Fig. 4.6 Architectures of published ADCs (ISSCC 1997–2015 and VLSI circuit symposium 1997–2014)

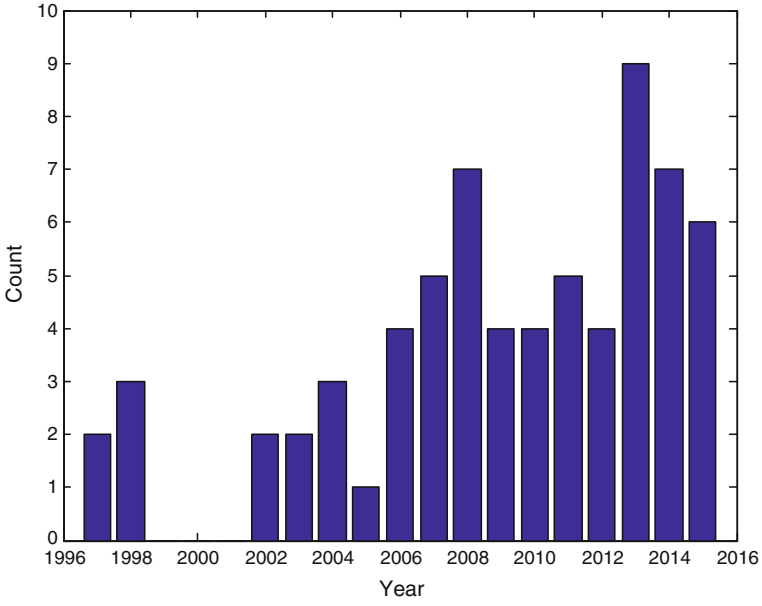

Fig. 4.7 Number of reported time-interleaved ADCs (ISSCC 1997–2015 and VLSI circuit symposium 1997–2014)

4.3.1 SAR ADCs

The SAR ADCs published in recent years show great versatility and range from ultra-low power to ultra-high speed designs (using time interleaving). To see this, contrast the 10-bit 200 kS/s converter of [18] with the 8-bit 90 GS/s part of [14]; both use a very similar circuitry in their converter core. Somewhere in between, we see 10-bit 2.6 GS/s time-interleaved SAR ADCs that can digitize the entire cable TV spectrum [19], as well as highly efficient 100 MS/s, 11-ENOB converters [20] that meet the demands of typical wireless receivers. While much of the progress in SAR converters is enabled by technology scaling, there have been a number of important circuit and architecture innovations as well. These include the combination of SAR conversion with pipelining [21] and the use of dynamic residue amplification in such hybrid topologies [20]. Other recent advancements include the judicious use of redundancy and DAC replica timing [22], majority voting for noise reduction [23], as well as integrated buffering to ease the input drive requirements [24].

4.3.2 Pipelined ADCs

Challenged by the impressive energy efficiency and scaling robustness of SAR converters, the designers of pipelined ADCs have continued their search for "opamp-less" residue amplification techniques. We have seen intriguing innovations in fully-dynamic amplification [25], ring-amplifier-based amplification [26, 27], comparator-based amplification [28], as well as bucket-brigade processing [29]. These and other approaches have helped in keeping the power dissipation of pipelined ADCs competitive for low to moderate sampling rates. Architecturally, the work of [30] reported an intriguing modification to the typical pipeline by splitting the amplifier into a coarse and fine path. This change extends the available settling time in each stage and may prove to be a valuable concept going forward. In the context of high-speed conversion for wireless infrastructure, pipelined ADCs are still the only topology that can meet the stringent application requirements. With proper calibration, we have seen that the pipelined architecture can be pushed to 1 GS/s at 14 bits [7]; a performance level that is hard (if not impossible) to reach with any other topology.

4.3.3 Flash ADCs

Flash ADCs have regained some interest due to the imminent shift from PAM2 to PAM4 signaling in high-speed data links. The time-interleaved flash design of [31] operates at 10.3 GS/s and thereby enables a multi-standard transceiver. As shown in the 32-nm SOI design of [32], the speed can even be extended to 20 GS/s while

maintaining outstanding power efficiency. Key to maintaining high efficiency in flash ADCs is to identify a proper offset calibration/mitigation scheme and to minimize the circuit complexity as much as possible. In that vein, the design of [33] introduced a technique that generates extra decision levels using dynamic interpolation at the comparators' regenerative nodes. These and other innovations are strongly linked to the unprecedented speed and integration density that is now at the disposal of the designers. In terms of concept innovation, the approach described in [34] points toward an intriguing new direction. Instead of designing flash ADCs with near perfect thresholds, this work proposes to adaptively control the decision levels to minimize the system's bit error rate, which is the ultimate specification of interest. Broadly speaking, this approach also falls into the categories of digitally assisted and analog-to-information conversion, discussed in more detail in Sect. 4.5.

4.3.4 Digitally Assisted Design

At the front of digitally assisted design, we have seen a variety of ideas applied to all of the above architectures. Perhaps the most complex and sophisticated scheme was implemented in the time-interleaved pipeline ADC of [35], which leverages two million logic gates to reach the unprecedented performance level of 14 bits at 2.5 GS/s. The digital logic is used to correct a variety of analog imperfections including dynamic sampling nonlinearity and signal-dependent self-heating. Similarly, digital equalization concepts are used in [36] to alleviate the residue-amplifier speed requirements and achieve 5.4 GS/s with only two interleaved slices. In the context of background calibration for pipelined ADCs, another noteworthy development was the introduction of algorithms with short convergence times [37]. Another area where digital assist has been pushed to new levels is in the correction of time interleaving artifacts. The time-interleaved SAR converter of [38] uses fully digital compensation of timing skew, which was previously thought to be prohibitively complex. In flash ADC design, digital assist was shown to be effective in reducing the comparator offset trim range by employing a fault-tolerant encoder [31], leading to significant savings in complexity and power. Another area, where digital assisted techniques have found their use, is in emerging topologies, such as VCO-based Nyquist converters [39, 40]. Here, digital calibration is not only an add-on, but needed to make these approaches practical.

4.4 Trends in Delta-Sigma A/D Converters

Delta-Sigma ADCs continued to follow an exploratory focus in both industrial and academic research activities. As a result, numerous findings, answers to previously open questions, and advances over the state-of-the-art were presented at conferences and published in journals. This trend continues to-date.

In the following, we provide an overview and summary of these advancements. Moreover, we reflect on them with regard to the predictions made on the development of Delta-Sigma ADCs back in 2010. Finally, based on recent and actual trends in the design of Delta-Sigma ADCs, we make predictions on future trends. By doing so, the most recent version of the survey provided in [2], extended by Delta-Sigma ADCs published in *IEEE Journal of Solid-State Circuits* from 2010 to 2015, serves as a data base. A detailed survey on Delta-Sigma ADCs covering further conferences and journals can be found in [41].

In accordance with [1], we consider in the following the major sub-blocks of a Delta-Sigma ADC, i.e., the loop filter, the quantizer, and the DAC, in order to present advancements and to discuss trends. Moreover, we stick to the $\mathrm{FOM_W}$ in this subchapter in order to facilitate a comparison with our results presented in [1].

4.4.1 Loop Filter

As outlined in [1], the loop filter of a Delta-Sigma ADC is categorized based on several criteria. Amongst others, the time domain it was designed for, i.e., continuous-time (CT) or discrete-time (DT). In 2010, it was observed that Delta-Sigma ADCs using a CT loop filter seemed to become the vehicle for high-speed implementations, a trend that was predicted to continue. Considering Fig. 4.8, which is an update of Fig. 4.13 in [1] with CT and DT designs published later than 2010, this prediction proved to be true over the past five years: all high-speed implementations with bandwidths larger than 20 MHz were implemented using a CT loop filter. Almost all have achieved SNDRs and FOMs comparable to those of the latest DT implementations while the lowest and thus the best CT FOM for a bandwidth larger than 20 MHz outperforms the lowest DT one by a factor of six. In general, a trend to lower FOMs is clearly visible. However, the minimum CT FOM improved only slightly from 40 to 30 fJ/conversion-step over the past five years.

Considering recent designs for frequency bands up to 20 MHz, CT loop filters were mostly used for the implementations as well. Overall, in comparison with DT Delta-Sigma modulators, nearly twice the number of CT implementations was published from January 2011 to March 2015. An overview of the quantitative distribution of the published architectures is given in Fig. 4.9. As can be seen, a switched-capacitor technique and thus DT circuitry were preferably used only for the implementation of MASH modulators. The better matching between the analog loop filter and the digital cancellation filters may account for this preference. On the other hand, this argumentation implies that, contrary to the prediction made in [1], less research was performed on digitally assisted circuits in order to overcome matching issues in CT multi-stage noise-shaping (MASH) architectures.

Interestingly, only one sturdy multi-stage noise-shaping (SMASH) modulator was among the recent MASH implementations [42]. This fact may be due to the guess ventured in [1], i.e., any SMASH modulator exhibits a feedback loop whose

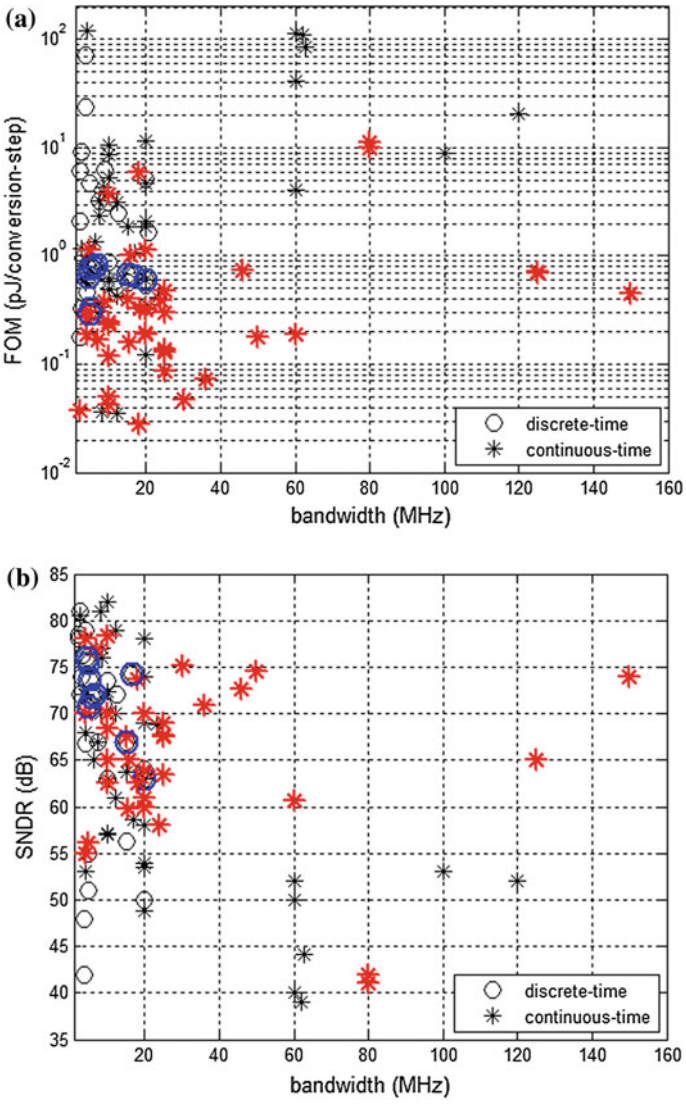

Fig. 4.8 Comparison of FOM and SNDR between DT and CT Delta-Sigma modulators exhibiting a bandwidth larger than 2 MHz. DT and CT designs published later than 2010 are highlighted in *blue* and *red*, respectively. FOM (**a**) and SNDR (**b**) versus bandwidth

order is equal to the sum of the orders of the single-stage modulators used in the cascade. Consequently, they face the stability issues of their equivalent single-stage modulator while requiring at least one additional quantizer for the implementation.

Another criterion for categorizing Delta-Sigma ADCs is based on the architecture of the loop filter, i.e., CIFB, CRFB, CIFF, CRFF, or any mixture of them [4]. In 2010, it was predicted that the CIFF architecture will become the preferred

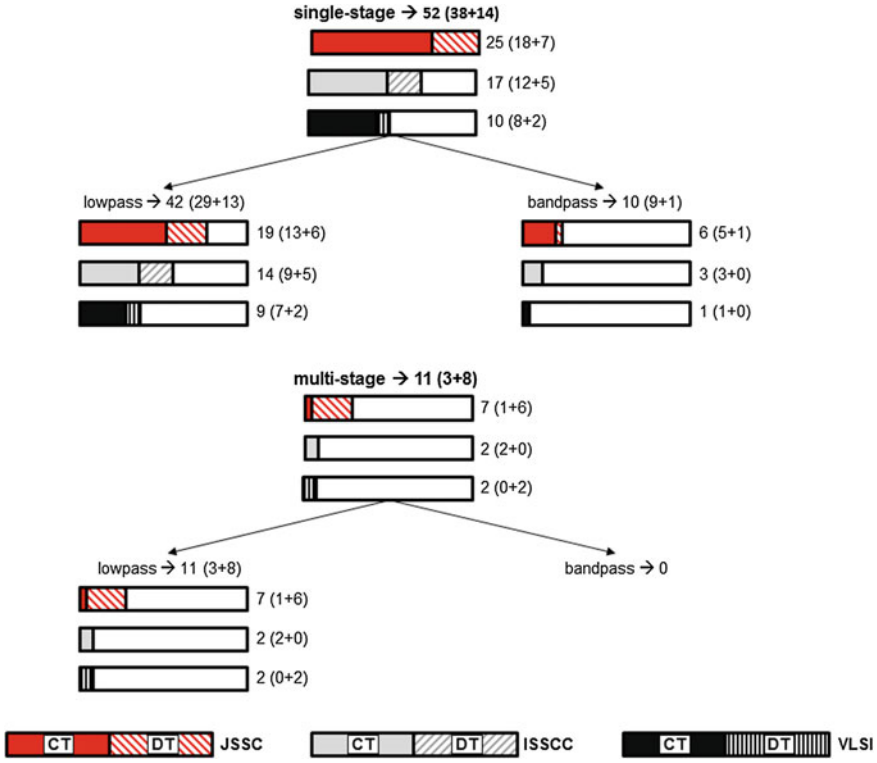

Fig. 4.9 Overview on delta-sigma modulators published between January 2011 and March 2015

architecture for implementations in the latest technology nodes. Despite the peaking of the STF and less anti-aliasing filtering, the signal swings inside a CIFF filter are much lower for input signals close to full scale in comparison to a CIFB filter; a characteristic that makes them very attractive for implementations using low supply voltages. Indeed, all recent designs with supply voltages around 0.5 V used a CIFF loop filter [43–45].

In general, all types of loop filters still enjoy great popularity today, even for supply voltages as low as 1 V. When it comes to the implementation of Delta-Sigma ADCs for telecommunication applications, e.g., wireless receivers, CIFB and CRFB represent the first choice. Not only do they provide better anti-aliasing filtering, but also a flat STF, which is considered a key characteristic with respect to blockers and interferers. However, in 2004, it was proposed to embed a first-order low-pass filter within a fourth-order CIFF loop filter of a Delta-Sigma ADC in order to reduce the peaking of the STF [46]. Both the robustness against interferers and blockers and the anti-aliasing filtering were thus improved. This approach was further pursued recently. In [47], a second-order Butterworth low-pass filter was embedded within a fourth-order CIFF loop filter. In comparison to an implementation with an explicit up-front filter, 25 % less power

consumption and 20 % less area were thus achieved. In another approach [48], a second-order CIFB Delta-Sigma ADC was merged with a third-order Chebyshev channel-select filter. As a result, the order of noise-shaping increased from two to five while the low-frequency STF was determined by the Chebyshev channel-select filter. Further research on both approaches may pave the way for CIFF loop filters to become the dominant architecture in the near future, even in telecommunication systems.

Finally, the lower FOMs seen in Fig. 4.9 are in part due to advancements in the implementation of the loop filter, i.e., minimalistic and digitally assisted architectures. Using inverter-based opamps, minimalistic loop filters for Delta-Sigma modulators started to emerge in 2007 [49–52]. Further approaches were presented recently, which allow for implementing second- and third-order loop filters using only a single amplifier [53–58]. These concepts, amongst others, were applied to achieve FOMs of 50 fJ/conversion-step and 41 fJ/conversion-step in a bandwidth of 10 MHz [55, 57].

In [57], another path-breaking technique was presented, which may shape the future of loop filters: integrator loss compensation. Considering an active RC integrator, this technique virtually boosts the DC gain of the amplifier by inserting a negative replica of the resistor R from the input of the amplifier to ground. Implementing high DC-gain amplifiers by means of cascading low DC-gain stages thus becomes obsolete. At present, cascading represents a very popular yet power consuming approach to tackling the reduced intrinsic gain per transistor and the low supply voltages of modern technology nodes that limit the number of stacked transistors and thus the efficiency of cascoding.

4.4.2 Quantizer

In [1], two concepts for the implementation of a multi-bit quantizer were considered that comply with the benefits of scaled CMOS technologies for digital applications: the VCO-based quantizer and the time-encoding quantizer. It was predicted that they may become favorite architectures for the implementation of a multi-bit quantizer in the near future, thus replacing power consuming multi-bit flash ADCs. In the following, the developments and advancements of these quantizers are summarized and analyzed.

4.4.2.1 Voltage-Controlled Oscillator-Based Quantizer

Voltage-controlled oscillator-based quantizers highly comply with technology scaling since they consist of digital circuit blocks, e.g., flip-flops and standard logic cells, which provide signal levels equal to the supply voltage. Sampling the phase instead of the frequency, they provide first-order noise shaping to the quantization error by embedding a digital differentiator in order to reconvert the phase to frequency. Without feedback, a VCO-based quantizer thus achieves first-order noise

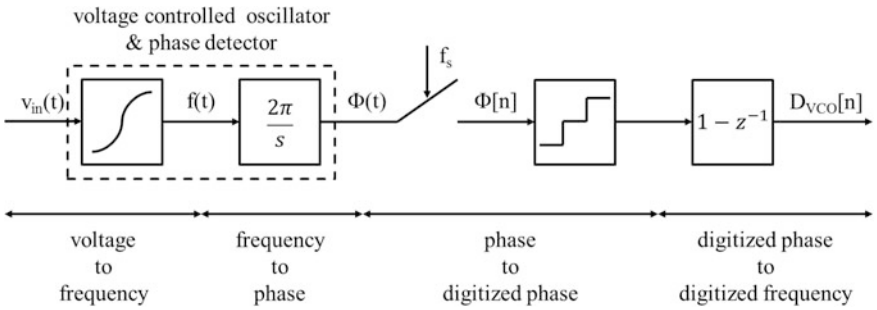

Fig. 4.10 Block diagram of a VCO-based quantizer

shaping by cascading a VCO, a phase detector and a digital differentiator as illustrated in Fig. 4.10. In spite of this fundamental distinction to a Delta-Sigma modulator, where feedback is applied in order to achieve noise shaping, they are often called a first-order Delta-Sigma modulator. Strictly speaking, they belong to the class of noise-shaping ADCs while not representing a Delta-Sigma modulator.

The intrinsic resolution of a VCO-based quantizer is determined by distortion due the non-linear voltage-to-frequency characteristic and phase noise, which are not subject to the intrinsic noise shaping. Thus, a pseudo-differential architecture is used quite frequently in order to reduce even-order harmonics and to improve the SNDR by 3 dB since the signal power quadruples while the noise power doubles. Further means were developed over the past five years in order to reduce the impact of these non-idealities on the resolution of a VCO-based quantizer, e.g., digital background or foreground calibration techniques. While these concepts were developed for improving the performance of stand-alone VCO-based quantizers, other approaches pursued embedding a VCO based quantizer in a Delta-Sigma modulator or using it as a later stage in MASH architectures. Embedding a VCO based quantizer in a Delta-Sigma modulator as performed in [59, 60] or [61] provides two advantages. First, using an N-th order loop filter, an (N + 1)-order noise shaping of the quantization error is achieved since one order is provided by the VCO. Second, distortion and phase noise of the VCO are suppressed by the N-th order loop filter, if referred to the input of the modulator. Using a VCO-based quantizer as a later stage of a MASH architecture as proposed in [62] results in less signal swing at the input of the VCO since later stages in a cascade only have to process the quantization error of the previous stage. Thus, the almost linear range of the non-linear voltage-to-frequency transfer characteristic is used whereby less distortion is induced.

A summary of recent architectures and achieved performances, including [59, 60] which already were considered in [1], is given in Table 4.1, sorted by their publication date. In particular, the advancements achieved in [61] in comparison with [59, 60] should be highlighted: Using a two-step quantizer consisting of a 4-bit flash and a 4-bit VCO, the design achieved an SNR which approximately equals the SNR of an ideal and thus unscaled 2nd-order Delta-Sigma ADC with an 8-bit quantizer. An 8-bit flash ADC, however, is considered to be hardly feasible using a

Table 4.1 Survey on and comparison of recent VCO-based ADCs

	Straayer [59] JSSC 04/2008	Park [60] JSSC 12/2009	Daniels [63] VLSI 2010	Taylor [64] JSSC 12/2010	Asl [62] CICC 2011	Rao [65] VLSI 2011	Reddy [61] JSSC 12/2012	Taylor [66] JSSC 04/2013	Rao [67] JSSC 04/2014
ADC architecture	2nd-order DSMw. VCO quantizer → 3rd-order noise shaping	3rd-order DSMw. VCO quantizer → 4th-order noise shaping	Pseudo differential VCO	Pseudo differential VCO	MASH 1st: lst-order DSM 2nd: VCO ADC → 2nd-order noise shaping	Pseudo differential VCO	lst-order DSMw. 2-step quantizer (4bflash—VCO)	Configurable pseudo differential VCO	pseudo differential VCO
Resolution of VCO (bits)	5	4	4	4	3	4	4	4	4
Calibration	N/A	N/A	Foreground	Background	N/A	Two-level modulation	N/A	Background	Background
Technology (nm)	130	130	65	65	130	90	90	65	90
Supply voltage (V)	1.2	1.5	N/A	2.5 (V/l conv.) 1.2	1.3	N/A	1.4(A) 1.0(D)	0.9–1.2	1.2(A) 1.0 (D)
SNR(dB)	86	81.2	N/A	70	77.3	N/A	83	70–76	75.4
SNDR(dB)	72	78.1	64	69	77	59.1	78.3	69–75	73–74.7
SFDR(dB)	N/A	N/A	79	N/A	91.6	71	78.3	77–83	N/A
Bandwidth (MHz)	10	20	30	18	4	8	10	5.08–37.5	5
Sampling frequency (MHz)	950	900	300	1152	100 (DSM) 1200 (VCO)	640	600	1300–2400	640
Power (mW)	40	87	11.4	17	6.1(A) 7.7(D)	4.3	6.5(A) 9.5(D)	11.5–39	4.1
Area (mm^2)	0.42	0.45	0.02	0.07	0.7	0.1	0.36	0.075	0.16
FOM (fl/cornv.-step)	500	330	150	159	296	366	120	123–305	92–112

supply voltage of 1.4 V since the LSB becomes as small as 5.5 mV. Future research may focus on merging a minimalistic higher-order loop filter and a VCO-based quantizer in order to design a very power and area efficient Delta-Sigma modulator while suppressing distortion of the VCO by the loop filter.

4.4.2.2 Time-Encoding Quantizer

Time-encoding quantizers use a single-bit PWM quantizer whose power of the quantization noise is mostly located at a defined limit cycle outside the signal band. By means of a sinc-decimation filter whose zeros are placed accordingly, this quantization noise is removed [68]. The residual power of the quantization noise within the signal band thus resembles the power of the quantization noise of a multi-bit quantizer although a single-bit quantizer is used. Obviously, the advantage of this approach is its compatibility with scaled CMOS technologies for digital applications, since only a single comparator is needed.

Recently, advancements were achieved in the generation of the limit cycle. Applying describing-function theory, it was shown in [69] that a stable limit cycle with well controlled amplitude and frequency can be generated using a flip-flop instead of an inverter based programmable delay-line in the feedback loop of the time-encoding quantizer. Moreover, an FIR DAC was used in the feedback loop of the Delta-Sigma modulator in order to suppress the limit cycle in the loop, thus reducing the slewing requirement of the first opamp. In [70], the active integrator in the feedback loop of the time-encoding quantizer was replaced by a passive low-pass filter and an amplifying DAC in order to lower the power consumption to 7mW and the area to 0.08 mm^2. Using a 65 nm technology, an SNDR of 61 dB was achieved in a bandwidth of 20 MHz which results in a FOM of 191 fJ/conversion-step.

Another concept for implementing a time-encoding quantizer was presented in [71] which consist of a comparator-based PWM modulator followed by a time-to-digital converter. The publication represents an extended version of [72], which achieved an SNDR of 60 dB in a bandwidth of 20 MHz for a power consumption of 10.5 mW using a 65 nm technology. Similar results were presented almost two and a half year later in [70] while the FOM and the area were improved by 40 and 50 %, respectively; a quite noticeable advancement.

In all considered designs, multi-stage opamp-based loop filters were applied. As for VCO-based Delta-Sigma ADCs, merging the concept of time-encoding quantizer and minimalistic/digitally assisted loop filter may be the next step toward reducing the power consumption and area of these low-voltage compliant ADCs.

4.4.3 DAC

In 2003, it was proposed to use a single-bit quantizer with a multi-tap finite impulse response (FIR) DAC in the feedback path of the Delta-Sigma modulator [73]. Since

only a single comparator is needed for the implementation of the quantizer, a power-and area-efficient design thus becomes feasible while the feedback signal resembles the signal of a multi-bit DAC. Consequently, a design using an FIR DAC is nearly as robust against clock jitter as its equivalent multi-bit implementation [74]. Moreover, as in the multi-bit case, the dynamic range of the Delta-Sigma modulator increases since the multi-bit feedback signal contains less power compared to the single-bit case. Finally, since the amplitude of a multi-bit signal better matches the amplitude of the input signal, the signal to be processed by the loop filter, in particular by the first integrator, becomes smaller. As a result, less opamp-related distortions are induced.

The approach has received attention recently in order to replace a multi-bit flash quantizer, since its power consumption determines the overall power consumption of today's Delta-Sigma ADCs to a great extent [69, 75–77]. In [77], it was shown that such a design is more power efficient than an equivalent design using a 4-bit quantizer although a higher sampling frequency must be applied in order to achieve the same resolution. Achieving an SNDR of 70.9 dB in a bandwidth of 36 MHz for a power consumption of 15 mW, the FOM equal to 73 fJ/conversion-step is among the lowest FOMs reported to date for Delta-Sigma ADCs.

4.4.4 Conclusion on Delta-Sigma A/D Converters

Concluding our overview on and summary of advancements of Delta-Sigma modulators: Many innovative cooks all over the world rely on the cooking recipe *Delta-Sigma ADC,* which dictates a loop filter, a quantizer and feedback. By trying ever new ingredients, they are competing with each other for being the first serving the meal with the ultimate taste according to this particular recipe. Naturally, tastes differ, which is why selections of the best recipes are provided as a subchapter in one of the many cookery books entitled *Oversampled Analog-to-Digital Converters* or the like. However, the time may be ripe for focusing on and writing a fundamentally different and thus never before seen cookery book. This book may be entitled *Analog-to-Information Converters*. A glimpse on its first pages and thus what it will be about one day is provided next.

4.5 Analog-to-Information Converters

The term "analog-to-information" was first coined in 2008 [78], and it was discussed in the context of a specific technique called compressed sensing (CS) [79, 80]. From CS theory, it follows that one can recover certain signals (which are "sparse" in some domain), using much fewer samples than required per the Shannon-Nyquist sampling theorem. In recent years, this theory has been translated down to practical realizations, and we are seeing the first few hardware demos

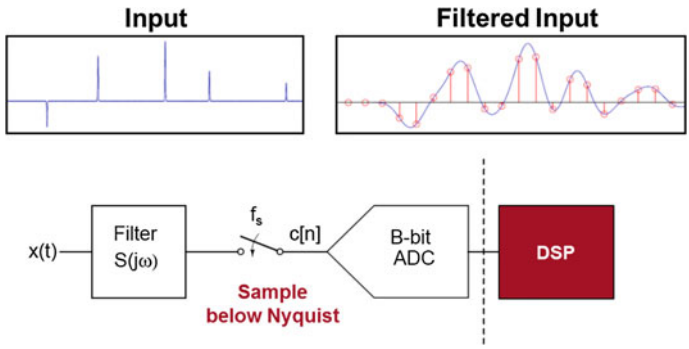

Fig. 4.11 FRI sampling of a pulse train signal

ranging from bio interfaces [81] to CMOS imagers [82] and radios [83]. Due to the requirement of "sparsity," CS is not suitable for arbitrary signals and one must carefully consider the impact of circuit impairments in practical realizations [84].

In the meantime, similar concepts that target sub-Nyquist signal acquisition have emerged. These include Xampling, which uses aliasing in conjunction with CS-like reconstruction in the digital domain [85]. Another approach is finite rate of innovation (FRI) sampling [86, 87], which models a signal in terms of its number of degrees of freedom per unit of time (corresponding to the rate of innovation). This idea is illustrated in Fig. 4.11 using a pulse-train input, which could be viewed as a basic model of an ultrasound or radar signal. The shown waveform has 5 pulses that can be described by 5 arrival times and 5 amplitudes. So, according to FRI theory, there are 10 degrees of freedom and 10 samples should suffice to reconstruct this signal in the digital domain. However, if we take the typical approach of uniform sampling, a very high sampling rate is needed to preserve the information according to Shannon-Nyquist. Namely, the sampling rate must be twice as high as the highest input frequency, which is very large due to the narrow pulses. The solution offered within the FRI framework is to pre-filter the signal before sampling and sample the signal at a rate commensurate with the low-bandwidth content of the smoothed signal ("filtered output" in Fig. 4.11). Xampling and FRI approaches are currently being taken toward practical hardware realizations and promise to offer significant benefits in various applications. In imaging and video, compressed sensing and FRI sampling are particularly powerful directions and receive further treatment in Chaps. 12 and 14.

Another class of analog-to-information interfaces is emerging in the context of feature extraction and classification of patterns that are buried in analog waveforms. Building on similar ideas that have already been explored in the imaging community [88, 89], it is conceivable that new forms of specialized "feature-extraction" A/D converters will emerge. A very recent example is a 6 μW acoustic sensor front-end, featuring analog feature extraction and mixed-signal embedded classification [90]. Such interfaces will undoubtedly gain in popularity as we steer toward the "internet of everything," in which massive amounts of sensor data will force us to feature-extract, classify and interpret signals as close as possible to the sensor itself.

4.6 Conclusions

From Fig. 4.4, it was observed that the overall progress rate of the low-frequency FOM_S asymptote is approximately 1 dB per year. Based on this rate, the practical limit $FOM_{S,max}$ = 186 dB according to (1) will be reached in ten years, i.e., in 2025. At the same time, the high-frequency asymptote at the (arbitrary) reference level FOM_S = 150 dB in Fig. 4.3 would increase from 20 GHz to 1.28 THz, i.e., by about a factor 2^6 based on the progress rate of ×2 every 1.8 years (see Fig. 4.5). Thus, the intersection point of the two asymptotes will increase from 42 to about 320 MHz.

Accounting for a safety margin as large as three, this trend implies that by 2025, ADCs for Nyquist sampling rates up to 100 MHz cannot be further optimized in terms of FOM_S. Despite some inherent uncertainty in these numbers, this result poses several questions the ADC community must face and deal with in the near future. Will the optimization of conventional ADCs indeed run out of steam, or will new applications emerge that fuel new demand for higher bandwidths, thus keeping the wheels of optimization turning? Will we stick to a general FOM or define application-specific FOMs, which will then provide opportunities for application-specific optimization? Will we overcome the limitation of clock jitter by means of new approaches or architectures that avoid clock-driven sampling? How will the designers of analog-to-information converters respond to the challenges?

In summary, we conclude that the development and progress of ADCs in recent years was mostly driven by the optimization of figures of merit, and remarkable improvements have been recorded over time. However, in the near future, this trend will have to come to a halt, since we are approaching practical limits that are difficult, if not impossible, to surpass. As in the case of the MOS transistor, the broad question on "What's next?" is looming on the horizon of data converter research.

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