Chapter 18: MOS Field-Effect Transistor (MOSFET)

Overview

Prerequisites:
- Knowledge of basic circuit analysis
- Exposure to theory of the pn-junction (optional)
- Exposure to BJT circuit analysis and amplifiers (Chapter 17, optional)

Objectives of Section 18.1:
- Learn physical composition of the field-effect transistor, four- and three-terminal configurations
- Understand principle of operation of the MOSFET
- Realize the origin and understand the value of MOSFET threshold voltage
- Be able to estimate threshold voltage based on MOSFET's physical composition

Objectives of Section 18.2:
- Learn MOSFET test circuits
- Become familiar with the dynamics of channel inversion and quantify the underlying mechanism
- Derive MOSFET equations (large-signal model) for three regions of operation from first principles
- Pay special attention to large-signal MOSFET model in saturation
- Become familiar with *v-i* dependencies for the NMOS and PMOS transistors

Objectives of Section 18.3:
- Learn the resistor-switch model of the MOSFET for switching applications
- Apply the resistor-switch model of the MOSFET to logic gates
- Understand the value of the triode and cutoff regions for switching applications
- Become fluent with the method of assumed states for MOSFET DC circuit analysis
- Use the load-line method, either graphically or analytically
- Solve in basic MOSFET DC bias circuits

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Objectives of Section 18.4:

- Learn circuit topology of the common-source MOSFET amplifier
- Analyze and characterize the voltage transfer characteristic of the common-source amplifier
- Understand the value of the saturation region for amplifier applications
- Be able to properly select the quiescent (bias) point
- Formulate the small-signal MOSFET model and solve in the common-source amplifier circuit

Application Examples:

- Output resistance of digital logic gates
- Basic MOSFET switching actuator

Keywords:

Field-effect transistor (FET), Metal-oxide semiconductor FET (MOSFET), Enhancement-mode MOSFET, E-MOSFET, Depletion-mode MOSFET, n-channel MOSFET, p-channel MOSFET, NMOS transistor, PMOS transistor, MOSFET drain terminal, MOSFET source terminal, MOSFET gate terminal, MOSFET body terminal, MOSFET substrate terminal, Four-terminal MOSFET, Three-terminal MOSFET, MOSFET channel, MOSFET threshold voltage, MOS capacitor, Ideal MOS capacitor model, Surface space-charge region of MOS capacitor, Surface voltage of MOS capacitor, Surface potential of MOS capacitor, One-sided pn-junction approximation, Strong inversion in MOS capacitor, Inversion layer of MOS capacitor, Flat-band voltage, Work function difference, Junction FET (JFET), Metal–semiconductor FET (MESFET), Triode region of a MOSFET, Saturation region of a MOSFET, Cutoff region of a MOSFET, Process transconductance parameter, MOSFET transconductance parameter, MOSFET lumped process parameter, MOSFET turn-on resistance, Channel pinch-off, Saturation current, Saturation velocity, Velocity saturation region, Early effect, Channel modulation effect, Transconductance curve, Large-signal MOSFET model in saturation, MOSFET parameter extraction, MOSFET on-state resistance, MOSFET resistor-switch model, CMOS logic gates, CMOS NOT gate (inverter), CMOS NAND gate, CMOS NOR gate, Gate output resistance, Method of assumed states, Gate-bias (fixed-gate) MOSFET circuit, Diode-connected MOSFET circuit, Load-line analysis, Load line, Basic MOSFET actuator device, Common-source MOSFET amplifier, Voltage transfer characteristic, Quiescent point of NMOS amplifier, Small-signal MOSFET model, Open-circuit small-signal voltage gain, Small-signal MOSFET transconductance, Small-signal ground

Section 18.1 Principle of Operation and Threshold Voltage

In this chapter we study the *field-effect transistor* (FET). The most important member of the FET family is the *metal-oxide-semiconductor FET* or MOSFET. Similar to the npn and pnp BJT transistors, MOSFETs are subdivided into n-channel MOSFETs and p-channel MOSFETs, also known as NMOS and PMOS transistors. The abbreviation CMOS, or complementary MOS, implies an integrated circuit which incorporates *both* of these types of transistors on the same substrate. It is the CMOS transistor that allows high-density chip integration as part of microelectronic analog and digital circuits. MOSFETs are used in both logic gates and in memory cells. Discrete power MOSFETs are also deployed in many power engineering applications. We will concentrate on the *enhancement-mode MOSFET* (or E-MOSFET), which relies on a positive gate-to-source threshold voltage. Other MOSFET types (*depletion-mode MOSFET*) may have either negative or near-zero threshold voltages.

18.1.1 Physical Structure: Terminal Voltages and Currents

An *enhancement-mode n-channel MOSFET* (*NMOS transistor*) is a *four-terminal* semiconductor device. The NMOS transistor shown in Fig. 18.1 consists of a p-doped substrate (the Si wafer) into which two n (or rather heavily doped n+) regions, the *source* and the *drain*, are formed through ion implantation. The *gate* electrode (source of the control voltage) used to be a metal film, but nowadays it is a heavily doped polysilicon. The gate length L, also known as *channel length*, can be as small as 30 nm. The gate isolation, necessary to form a capacitor, is a SiO_2 dielectric. It is formed directly from the Si substrate by thermal oxidation of Si. There are four metal electrodes corresponding to four transistor terminals: the *gate terminal* (G), the *source terminal* (S), the *drain terminal* (D), and the *body* (or *substrate*) *terminal* (B). The basic geometrical device parameters are the channel length, L, in horizontal direction, and the channel width, W, in vertical direction in Fig. 18.1. The channel length is the distance between the two pn+−junctions; the channel width characterizes the region of electron carrier flow between the drain and the source. Typical substrate acceptor concentrations (p-doping) are in the range of $N_A = 10^{16} - 10^{17}$ cm^{-3}. The doping of the two n+ domains (donor doping) is large. For example, $N_D \approx 10^{19}$ cm^{-3} for a power MOSFET.

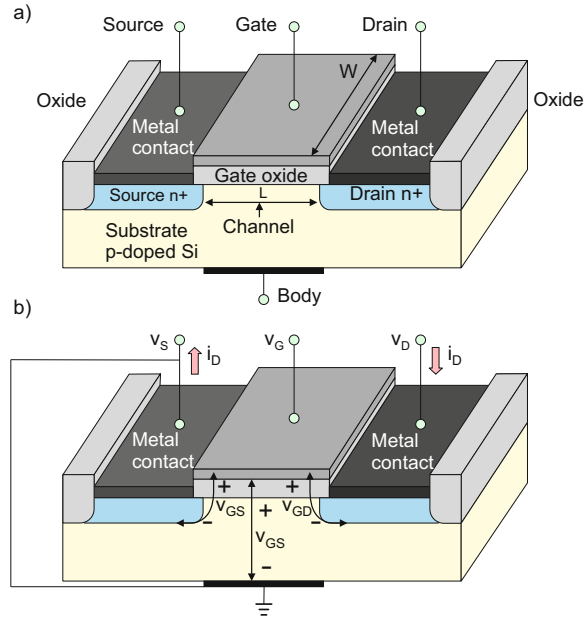


Fig. 18.1. Semiconductor composition of the NMOS transistor—*lateral or planar channel design*. The *vertical channel design* typical for power MOSFETs implies rotation by 90 degrees.

The circuit symbol for the four-terminal NMOS transistor is shown in Fig. 18.2a. The device is strictly *symmetrical*, which means that we can interchange the drain and the source; this is in contrast to the BJT. The arrow denotes the pn-junction polarity (from p to n) similar to the diode arrow. The four-terminal NMOS transistor is widely used in *integrated circuits. In discrete circuit*s, which employ *discrete transistor components*, the body terminal is tied to the source terminal as shown in Fig. 18.1b. Therefore, the NMOS transistor becomes the *three-terminal MOSFET device* (gate, drain, and source), similar to the BJT. However, it is no longer symmetrical. Figure 18.2b shows the corresponding circuit symbol. You encounter this symbol in the majority of manufacturer datasheets and electronic simulation packages. Simplified symbols are widely used; see Fig. 18.2c.

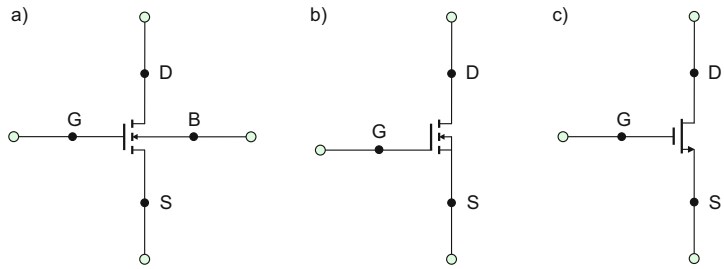


Fig. 18.2. Circuit symbols of (**a**) a four-terminal NMOS transistor, (**b**) a three-terminal asymmetric NMOS transistor with the body tied to the source, and (**c**) the same device but simplified.

We are going to study only the three-terminal configuration and use the symbol shown in Fig. 18.2b. Figure 18.3a shows transistor terminal voltages for the three-terminal device:

- *Gate-source voltage* v_{GS}
- *Drain-source voltage* v_{DS}
- *Gate-drain voltage* v_{GD}

Only two voltages are independent since KVL relates all three voltages to each other. The voltages v_{GS} and v_{DS} are chosen as independent variables. Then,

$$v_{GD} = v_{GS} - v_{DS} \tag{18.1}$$

The principal difference from the BJT is that the *control terminal of the transistor*, the gate, is electrically insulated. There is no current flowing into or out of the gate. Therefore, the transistor current is the only drain current, i_D, which flows from the drain to the source in Fig. 18.3b.

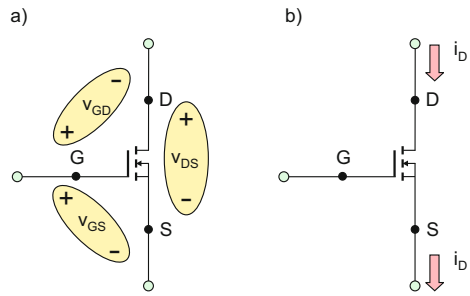


Fig. 18.3. Terminal voltages and currents for the NMOS transistor.

Exercise 18.1: A NMOS transistor has the gate-source voltage of 2 V and drain-source voltage of 0.3 V. What is the gate-drain voltage?

Answer: 1.7 V.

18.1.2 Simplified Principle of Operation

We consider the simplified transistor circuit shown in Fig. 18.4. Both the source and the substrate are grounded. When $v_{GS} = 0$, the path between the drain and the source includes two oppositely directed pn-junction diodes; see Fig. 18.4a. Therefore, there will be no current between the drain and the source for *any* possible value of drain-source voltage v_{DS} since one of the diodes will always be off. Now let us assume a positive control voltage v_{GS} is applied to the gate control terminal and $v_{DS} = 0$ for simplicity. A capacitor will form between the gate and all remaining (grounded) terminals; the initial electric field is shown

in Fig. 18.4b by dashed lines. This electric field *attracts* more negative electron carriers to the *channel* between the drain and the source and repels the positive carrier (holes) from the channel until the initial electric field will be essentially neutralized in the bulk of the substrate. The dependence of the electron concentration in the channel on υ_{GS} is exponential, i.e., very sharp. When υ_{GS} reaches a certain threshold value V_{Th} or exceeds it, the *MOSFET channel* appears (a thin subsurface domain just below the oxide) that has enough electron carriers to form a conducting "wire" between the drain and source as in Fig. 18.4b. The transistor switch becomes closed and transistor conducts the current i_D from the drain to the source given *any* (even small) positive voltage $\upsilon_{DS} > 0$. One may think of the boundary of the n+ region in Fig. 18.4b as a "rubber band" that is pushed away from the gate by the positive gate voltage. The value V_{Th} is the *intrinsic threshold voltage* (or simply *threshold voltage*) of the NMOS transistor. V_{Th} depends on transistor geometry and its doping concentrations. For the NMOS transistor, the threshold voltage is often denoted by V_{Tn} and for the PMOS transistor by V_{Tp}. In the following text, we will attempt to keep the generic notation V_{Th} for both transistor types.

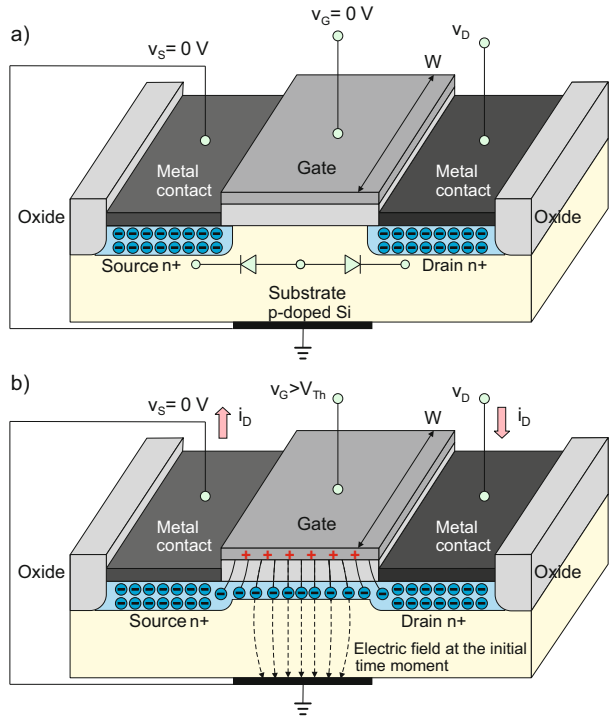


Fig. 18.4. Simplified NMOS configuration and creating a channel for current flow.

18.1.3 NMOS Capacitor

The phenomenon described above is known as *channel inversion* (from p- to n-type) of the NMOS transistor. The inversion can be quantified analytically since we deal with a

homogeneous p-type material in the bulk of the channel, as you can see in Fig. 18.4b. The central region of the NMOS transistor in Fig. 18.4 thus forms a *MOS capacitor* that consists of the gate, insulator, and the p-body. We will apply the semiconductor analysis to the MOS capacitor and use its one-dimensional electrostatic model which is shown in Fig. 18.5a (in fact it is turned 90° counterclockwise with respect to Fig. 18.4).

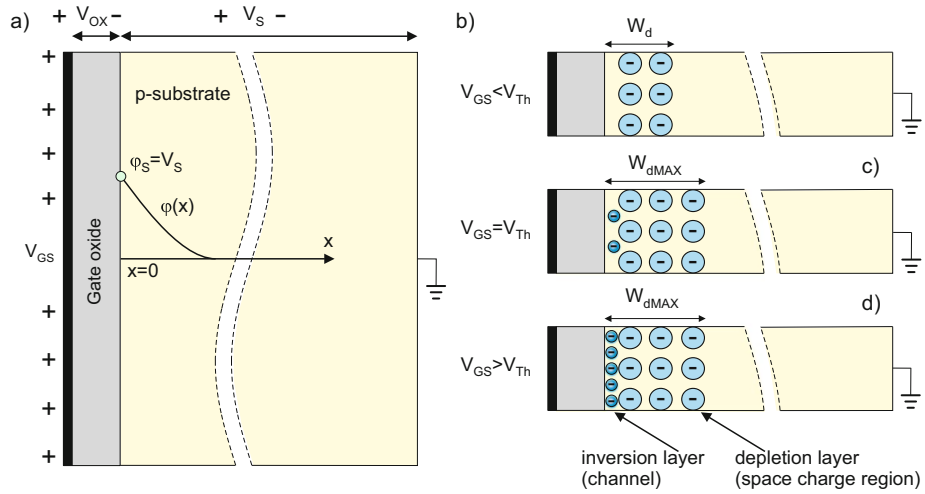


Fig. 18.5. (**a**) Central region of the MOSFET under an applied voltage v_{GS}: the MOS capacitor. (**b**) to (**d**) Formation of the depletion and inversion layers in the substrate. The entire region close to the semiconductor surface is called the *surface space-charge region*.

The *ideal MOS capacitor model* will be considered first. By KVL, the voltage $v_{GS} > 0$ is the sum of two positive components shown in Fig. 18.5a:

$$v_{GS} = V_S + V_{OX} \tag{18.2}$$

The first component V_S is the voltage across the semiconductor substrate, which is also called the *surface voltage* or the *surface potential* $\varphi_S = V_S$ (given zero potential at the body terminal). The second component V_{OX} is the *voltage across the oxide layer*. We will express it in terms of the surface potential $\varphi_S = V_S$ first. Then, φ_S itself will be quantified at the onset of *strong inversion*. Substitution of those two values in Eq. (18.2) will give us the desired threshold voltage V_{Tn}. The corresponding analysis relies upon semiconductor surface physics and may be skipped if necessary.

18.1.4 Voltage Across the Oxide Layer Before and at the Onset of Strong Inversion

At any $v_{GS} > 0$, the surface voltage is also positive, i.e., $V_S > 0$. The corresponding electric field directed into the body will push the positive holes into the depth of the

substrate and leave immovable negative ions behind; this is seen in Fig. 18.5b–d. Hence, a depletion layer will be formed, similar to the pn-junction depletion layer. Assume that the body is uniformly doped and has an acceptor concentration $N_A >> n_i$ where n_i is the intrinsic concentration of holes and electrons, $n_i \approx 1 \times 10^{10}$ cm^{-3} for Si. The depletion layer is nearly the abrupt region of a uniform negative ion concentration N_A and the width W_d. The depletion layer width W_d may be found analytically as

$$W_d = \sqrt{\frac{2\varepsilon}{q}\frac{V_S}{N_A}} \tag{18.3}$$

Here, ε is the dielectric constant of the substrate; in Si, $\varepsilon = 1.05 \times 10^{-12}$F/cm. The total charge Q of the depletion layer *per unit surface* (units of C/cm^2) is subsequently given by

$$Q = -qW_d N_A = -\sqrt{2\varepsilon q N_A V_S} \tag{18.4}$$

This is the negative charge on one side of the oxide capacitor with capacitance C_{OX} per unit area. The charge on the opposite side (gate) must be positive and of the same absolute value in order to keep the device electrically neutral. The voltage of the oxide capacitor is therefore

$$V_{OX} = -Q/C_{OX} = \sqrt{2\varepsilon q N_A V_S}/C_{OX}, \quad C_{OX} = \varepsilon_{OX}/t_{OX} \tag{18.5}$$

where the dielectric constant of the SiO_2 oxide is $\varepsilon_{OX} = 3.45 \times 10^{-13}$F/cm and t_{OX} is the oxide thickness.

Example 18.1: Given $V_S = 1$ V and $N_A = 5 \times 10^{16}$ cm^{-3} estimate the voltage across the SiO_2 oxide layer with a thickness of 4 nm; the NMOS body is Si.

Solution: We will use centimeters as length units in accordance with generally accepted semiconductor convention. The oxide-layer capacitance is given by

$$C_{OX} = 8.625 \times 10^{-7} \text{ F/cm}^2 \tag{18.6}$$

Substitution into Eq. (18.5) yields

$$V_{OX} = 0.15 \text{ V} \tag{18.7}$$

18.1.5 Voltage Across the Semiconductor Body

At any v_{GS}, the MOS capacitor is still a system *in equilibrium* (no currents of any kind) as long as v_{DS} is zero. Then, the electron and hole concentrations $n(x)$ and $p(x)$ are

$$p(x) = N_A, \quad n(x) = \frac{n_i^2}{N_A} << N_A, \quad n(x)p(x) = n_i^2 \tag{18.8}$$

The last expression in Eq. (18.8) is the mass-action law of a semiconductor. When a positive voltage v_{GS} is applied, an electric field is established in the p-doped material which is the negative spatial derivative of the potential distribution $\varphi(x)$; see Fig. 18.5a. The concentrations are modified by the potential $\varphi(x)$. Since the potential is defined to within a constant, one can select this constant in order to satisfy Eq. (18.8) deep in the body when $\varphi(x) = 0$. Equation (18.8) is therefore transformed to

$$p(x) = N_A \exp\left(-\frac{\varphi(x)}{V_T}\right), \quad n(x) = \frac{n_i^2}{N_A}\exp\left(\frac{\varphi(x)}{V_T}\right), \quad n(x)p(x) = n_i^2 \tag{18.9}$$

where V_T is the thermal voltage. The boundary condition at $x = 0$ is simply $\varphi(x) = \varphi_s = V_S$. At the boundary of the semiconductor, i.e., at $x = 0$, we obtain

$$n = \frac{n_i^2}{N_A}\exp\left(\frac{V_S}{V_T}\right), \quad p = N_A \exp\left(-\frac{V_S}{V_T}\right) \tag{18.10}$$

It is a common agreement to choose the onset of *strong inversion* as a surface voltage at which the electron charge concentration n reaches N_A at the boundary of the semiconductor; this is depicted in Fig. 18.5c. Thus, the surface charge concentration is inverted from $p = N_A$ with no applied voltage to $n = N_A$ when the channel inversion starts. From Eq. (18.10), the surface voltage becomes

$$V_S = \varphi_S = 2V_T \ln\left(\frac{N_A}{n_i}\right) = 2\varphi_F \tag{18.11}$$

where the voltage constant $\varphi_F = V_T \ln N_A/n_i$ is known as the *Fermi potential* of the semiconductor. We emphasize that at the onset of strong inversion the total charge Q of the depletion layer per unit surface given by Eq. (18.4) is still *much greater* than an extra free electron charge brought close to the surface. This is because the surface concentration $n = N_A$ very quickly decreases when the distance from the surface increases.

Exercise 18.2: Given $N_A = 5 \times 10^{16}$ cm^{-3} estimate surface voltage at the onset of strong inversion at room temperature of 25 °C. The NMOS transistor body is Si.

Answer: $V_S = 0.79$ V

When V_S continues to increase even slightly above the value predicted by Eq. (18.11), the surface electron concentration rises exponentially according to Eq. (18.10), and a rich n+ electron channel (or the *inversion layer*) is quickly formed as illustrated in Fig. 18.5d.

When strong inversion takes place, the depletion layer width W_d no longer increases because the inversion layer starts blocking the electric field. Its maximum value is given by Eq. (18.3) with $V_S = 2\varphi_F$. A critical distinction between the NMOS capacitor and the NMOS transistor is the channel formation time. While for an NMOS capacitor it can take minutes to collect the necessary electrons from the p-doped semiconductor with few free electrons, the inversion electrons for the transistor are readily available from two nearby n+ regions—the source and the drain.

18.1.6 Threshold Voltage

The *threshold voltage* V_{Th} of an NMOS transistor is defined as the *gate-source voltage* (18.2) *at the onset of strong inversion* when $V_S = 2\varphi_B$ according to Eq. (18.11). V_{OX} still follows Eq. (18.5). Therefore,

$$V_{Th} = V_{FB} + 2\varphi_B + \sqrt{2\varepsilon q N_A (2\varphi_B)}/C_{OX} \tag{18.12}$$

The new extra term V_{FB} on the right-hand side of Eq. (18.12) is called the *flat-band voltage* of the MOS capacitor. This term is needed for two reasons. The somewhat less important one is the presence of charges in the oxide layer due to ionic contamination. The second, important reason is the built-in voltage or potential of a boundary between two materials. This effect is similar to the built-in potential or voltage of the pn-junction. The built-in voltages of the metal-oxide boundary and of the semiconductor-oxide boundary do not cancel each other; the corresponding voltage difference is known as *a work function difference* ψ_{GS} between the gate and the semiconductor; it appears across the oxide layer (Fig. 18.6). Without going into further details, we may assume $V_{FB} \approx \psi_{GS}$ and write

$$\psi_{GS}|_{Al} \approx -0.66 - 0.03\ln\left(\frac{N_A}{10^{13}}\right)\ [\mathrm{V}], \quad \psi_{GS}|_{n+poly} \approx -0.7 - 0.03\ln\left(\frac{N_A}{10^{13}}\right)\ [\mathrm{V}] \tag{18.13}$$

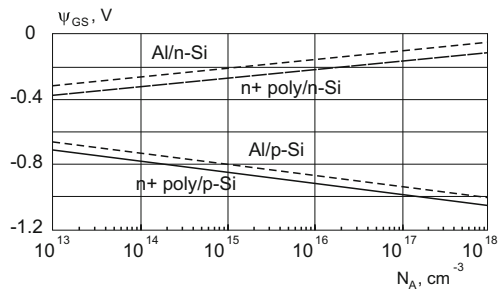


Fig. 18.6. Work function difference ψ_{GS} as a function of body doping for gate electrodes of polysilicon and aluminum, respectively, on a p-Si body of an NMOS transistor.

Example 18.2: Estimate the threshold voltage V_{Th} for a Si NMOS transistor with aluminum gate, $N_A = 1 \times 10^{17}$ cm^{-3}, and the SiO_2 oxide layer with the thickness of 50 nm at room temperature of 25 °C.

Solution: We will use centimeters as length units in accordance with standard semiconductor convention. The surface voltage at the onset of strong inversion is given by Eq. (18.11), i.e.,

$$V_S = 0.83 \text{ V} \tag{18.14a}$$

The oxide-layer capacitance and oxide voltage are given by Eq. (18.5), that is,

$$C_{OX} = 6.9 \times 10^{-8} \text{ F/cm}^2, \quad V_{OX} = 2.42 \text{ V} \tag{18.14b}$$

Finally, we find $\psi_{GS} = -0.94$ V from Eq. (18.13) and substitute all three contributions into the expression for the threshold voltage, $V_{Th} = \psi_{GS} + V_S + V_{OX}$. The result has the form $V_{Th} = 2.31$ V.

It is possible to extend the method of Example 18.2 to arbitrary values of oxide thickness t_{OX} and body doping concentration N_A. The result is shown in Fig. 18.7 where the threshold voltage is plotted as a function of N_A and t_{OX}. When the threshold voltage is positive (heavy body doping), the NMOS transistor is the *enhancement-mode device* (*E-MOSFET*). At light doping and small oxide thickness, the threshold voltage becomes negative. For different enhancement-mode MOSFETs, the V_{Th} values vary in the range

$$0.4 \text{ V} \le V_{Th} \le 4 \text{ V} \tag{18.15}$$

Many different methods exist to measure the threshold voltage. In practice, the threshold voltage is defined as a voltage when the drain current reaches a certain specified value.

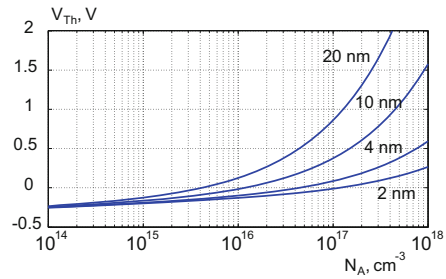


Fig. 18.7. Threshold voltage as a function of N_A and t_{OX} (Al gate).

18.1.7 PMOS Transistor

For a PMOS transistor (p-channel MOSFET), all doping concentrations in Figs. 18.1 and 18.4 are reversed. The substrate is now of n-type, and the source and drain are heavily

doped p+ regions. Consequently, all voltage polarities are reversed relative to their counterparts in the NMOS case. The PMOS and NMOS transistors are two *complementary devices*. Figure 18.8 shows the circuit symbols for the PMOS transistor. We put the source on top in accordance with a more positive voltage applied to it.

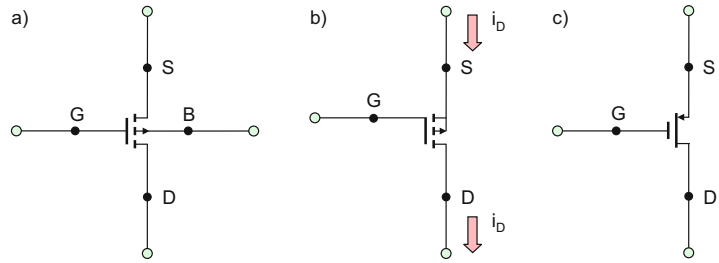


Fig. 18.8. Circuit symbols of (**a**) a four-terminal PMOS transistor, (**b**) a three-terminal asymmetric PMOS transistor with the body tied to the source, and (**c**) the same but simplified symbol.

The threshold voltage between the gate and the source also becomes negative. Specifically, Eq. (18.12) for the PMOS transistor is modified as

$$V_{\mathrm{Th}} = V_{\mathrm{FB}} - 2\varphi_{\mathrm{B}} - \sqrt{2\varepsilon q N_{\mathrm{D}}(2\varphi_{\mathrm{B}})}/C_{\mathrm{OX}} \tag{18.14}$$

where $V_{\mathrm{FB}} \approx \psi_{\mathrm{GS}}$ and ψ_{GS} is given by two *upper* curves in Fig. 18.6.

Exercise 18.3: In Example 18.2, invert all doping concentrations and find the threshold voltage of the corresponding PMOS transistor.

Answer: $V_{\mathrm{Th}} \approx -3.3$ V.

18.1.8 Oxide Thicknesses and Capacitances in CMOS Processes

MOSFETs used in integrated circuits are fabricated in a number of *CMOS processes*. Each process is characterized by the minimum channel length L as seen in Fig. 18.1. Smaller lengths allow us to pack a greater number of transistors per unit area. The CMOS design is constantly evolving so as to *decrease* the channel length. Table 18.1 lists some CMOS device parameters: oxide layer thickness and oxide capacitance used in the design of analog ICs. This information helps to find the threshold voltages of the transistors.

Table 18.1. Minimum channel lengths and oxide layer thicknesses and oxide capacitances for different CMOS processes. 1 $\mathrm{fF/\mu m^2} = 10^{-7}\mathrm{F/cm^2}$ and $\varepsilon_{\mathrm{OX}} = 3.45 \times 10^{-13}\mathrm{F/cm}$ (SiO_2 oxide).

Parameter	0.5-μm process		0.25-μm process		0.18-μm process		0.13-μm process	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
t_{OX} (nm)	9	9	6	6	4	4	2.7	2.7
$C_{\mathrm{OX}} = \frac{\varepsilon_{\mathrm{OX}}}{t_{\mathrm{OX}}}$ $(\mathrm{fF/\mu m^2})$	3.8	3.8	5.8	5.8	8.6	8.6	12.8	12.8

18.1.9 Family Tree of FETs

The MOSFET is not the only member of the field-effect transistor family. In contrast to the BJT, this device family is extensive. Figure 18.9 lists three examples. Let us first discuss the idea of W. Shockley (1952) for the *junction FET* (JFET). We can use a depletion region of the reverse-biased pn-junction to control, i.e., reduce or increase, the net channel opening *b* between the drain and the source in Fig. 18.10a. This is the JFET composition. When current flows from the drain to the source, the device becomes a *voltage-controlled resistor*, with the control voltage being the reverse-bias voltage of the pn-junction. Indeed there is still no gate current since the reverse-biased pn-junction is a very good insulator. A similar situation applies for the MESFET (*metal–semiconductor FET*) in Fig. 18.10b. However, here the origin of the depletion layer is different, i.e., the metal–semiconductor interface and the corresponding Schottky potential barrier. MESFETs constructed with Si, and especially gallium arsenide (GaAs), are typically used in RF power amplifiers. Many additional FET types exist or are still awaiting discovery.

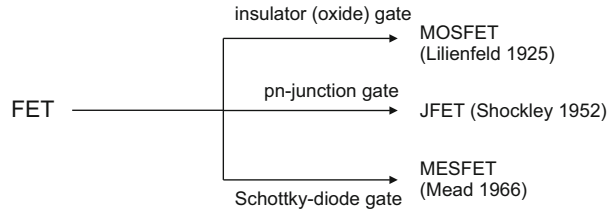


Fig. 18.9. Modifications of the field-effect transistor involving different types of gates.

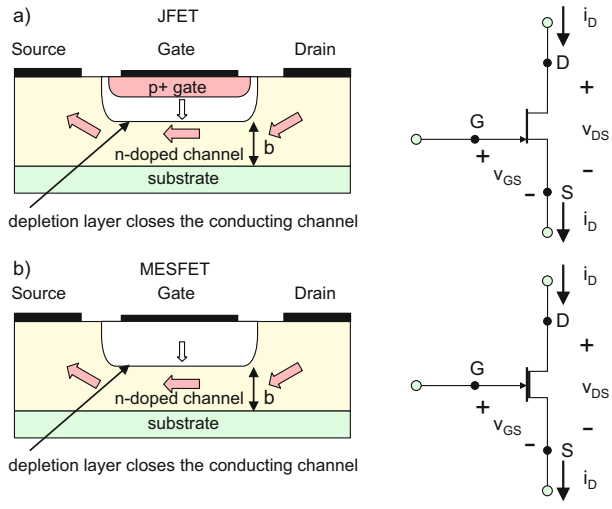


Fig. 18.10. Two schematic FET configurations: (**a**) n-channel JFET and (**b**) n-channel MESFET. A variant for both configurations is the dual gate arrangement. You should note that the corresponding circuit symbols have a continuous gate, denoting the normally "on" state.

Section 18.2 Theoretical Model of a MOSFET

18.2.1 Test Circuit and Operating Regions

Figure 18.11 shows the test circuit for the three-terminal NMOS transistor. Gate-source voltage v_{GS} and drain-source voltage v_{DS} are varied. The drain current i_D is measured at every particular voltage combination. Our goal is to derive analytical expressions for the drain current i_D. The analytical models described below rely on the corresponding measured data, which have been obtained with circuits similar to that in Fig. 18.11.

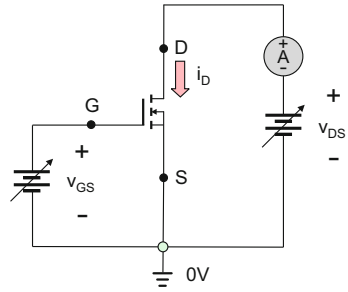


Fig. 18.11. Schematic diagram of the NMOS transistor test circuit.

The NMOS (and PMOS) transistor has three operating regions: *triode*, *saturation*, and *cutoff* listed in Table 18.2. All three regions are used. Most common MOSFET switching circuits like logic gates utilize the cutoff and triode regions in order to characterize two binary steady states—logic 0 and 1. However, during the fast transition between the states, the transistors enter the saturation region. MOSFET amplifier circuits solely utilize the saturation region of operation.

Table 18.2. The three operating regions of an NMOS transistor.

Region	Condition on v_{GS}	Condition on v_{DS}
Triode	$v_{GS} > V_{Th}$	$v_{DS} < v_{GS} - V_{Th} = v_{OV}$
Saturation	$v_{GS} > V_{Th}$	$v_{DS} > v_{GS} - V_{Th} = v_{OV}$
Cutoff	$v_{GS} \leq V_{Th}$	Immaterial

The regions of operation are determined by the value of v_{DS} as compared to the control voltage v_{GS}. The triode region starts with a *linear* (or *ohmic*) *subregion*. Table 18.2 indicates one more useful voltage parameter: the *overdrive voltage* $v_{OV} = v_{GS} - V_{Th}$. The NMOS transistor typically operates at *large* overdrive voltages.

18.2.2 Linear Subregion of Triode Region at Strong Inversion

Let us consider a situation when a large enough gate voltage (typically *significantly larger* than V_{Th}) is applied to induce the inversion layer between the drain and the source. The cross section of the NMOS transistor is shown in Fig. 18.12. This is a two-dimensional structure. For the analytical description, the electric field is conveniently subdivided into two components: one is in the horizontal direction from gate to body termination, and the other is in the vertical direction from drain to source. Henceforth, two sets of associated voltages (potentials) should describe the 2D models. We analyze fields and voltages in the horizontal direction first.

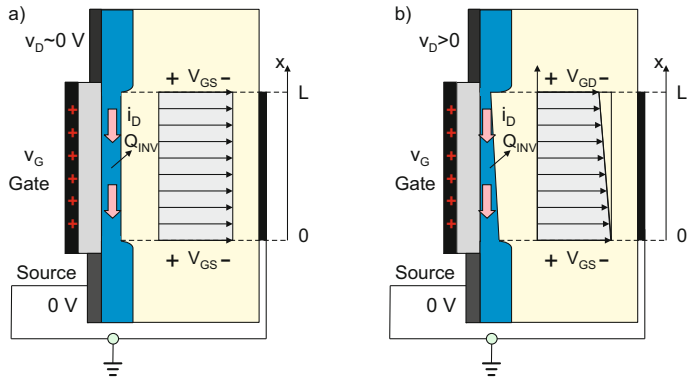


Fig. 18.12. Voltage distribution across the channel in the triode region. The linear charge and voltage profiles in Fig. 18.12b are an approximation.

When the drain is at zero volts or at a *small* positive voltage with respect to the source (body), the gate-source voltage appears to be nearly uniform in space along the length of the channel L; this is seen in Fig. 18.12a. The charge density in the inversion layer per unit area Q_{INV} measured in C/cm^2 is also uniform when the distance x along the channel changes. To find Q_{INV} the following observation is made. The threshold voltage V_{Th} is responsible for creating the depletion layer in the semiconductor body at the onset of strong inversion. Any excess or overdrive voltage $v_{OV} = (v_{GS} - V_{Th})$ thus controls Q_{INV} in the inversion layer since the depletion layer parameters no longer change. Q_{INV} is the negative charge on one side of the oxide capacitor with capacitance C_{OX} per unit area. The charge on the opposite side (gate) must be positive and of the same absolute value in order to keep the device electrically neutral. Therefore,

$$Q_{INV} = -C_{OX}(v_{GS} - V_{Th}) \tag{18.15}$$

We now turn to the vertical fields. The drain current i_D in Fig. 18.12 is the motion of charge Q_{INV} with speed $v = \mu_{ns}E$ in the (vertical) *constant* electric field $E = v_{DS}/L$ where

μ_{ns} is the *electron surface mobility*; $\mu_{ns} \approx 450\,\text{cm}^2/(\text{V}\cdot\text{s})$ or less. The drain current that flows from drain to source is thus given by (W is the channel width)

$$i_D = -WQ_{INV}v = \frac{W}{L}k_n'(v_{GS} - V_{Th})v_{DS}, \quad k_n' = C_{OX}\mu_{ns} \tag{18.16}$$

The constant k_n' with units of A/V^2 (more often mA/V^2) is called the *process transconductance parameter*. The name implies that it is determined by the particular fabrication technology. The constant $k_n = (W/L)k_n'$ with the same units is the *MOSFET transconductance parameter* (also called the *lumped process parameter*); it also includes information about the gate dimensions. Typically, k_n is on order of 1 mA per V^2 or less for small-signal MOSFET transistors. For power MOSFETs, however, it can be much larger: on the order of 100 mA per V^2. Equation (18.16) states that at small positive v_{DS} the NMOS transistor behaves like a *linear resistance* r_{DS}, *which is controlled by the gate-source voltage*,

$$i_D = \frac{v_{DS}}{r_{DS}}, \quad r_{DS} = \frac{1}{k_n(v_{GS} - V_{Th})} \tag{18.17}$$

The resistance r_{DS} can be measured in the laboratory. It is also called *the turn-on resistance*. This resistance of a MOSFET is a key parameter that is typically specified in the manufacturer's datasheets (in contrast to k_n).

18.2.3 Nonlinear Subregion of Triode Region at Strong Inversion

When v_{DS} increases (but still remains less than $v_{GS} - V_{Th}$), the situation depicted in Fig. 18.12b is observed. Close to the source region, the gate still "sees" the absolute source voltage (0 V in this case) as the terminal voltage. However, close to the drain, the gate does not "see" 0 V, but sees the drain voltage as the *terminal voltage*. The resulting voltage becomes $v_{GD} = v_{GS} - v_{DS}$. Therefore, a *variable* gate-source voltage $v_{GS}(x)$ is effectively applied *across* the channel. The tip of the inversion layer becomes thinner, which is schematically shown in Fig. 18.12b. Introducing an as-yet unknown *channel voltage profile* $y(x)$, we have

$$v_{GS}(x) = v_{GS} - y(x)v_{DS}, \quad y(x) = \begin{cases} 0 & x = 0 \\ 1 & x = L \end{cases} \tag{18.18a}$$

Consequently, the charge of the inversion layer given by Eq. (18.15) also becomes a function of x as illustrated in Fig. 18.12b:

$$Q_{INV}(x) = -C_{OX}(v_{GS}(x) - V_{Th}) = -C_{OX}(V_{OV} - y(x)v_{DS}) \tag{18.18b}$$

The vertical potential electric field in the channel is now variable too, that is,

$$E(x) = -\frac{d\upsilon_{\mathrm{GS}}(x)}{dx} = \upsilon_{\mathrm{DS}}\frac{dy}{dx} \tag{18.18c}$$

Next, the current along the inversion layer, $i_{\mathrm{D}} = -WQ_{\mathrm{INV}}\upsilon$, becomes

$$i_D = -WQ_{INV}\mu_{ns}E(x) = Wk_n^{'}\upsilon_{DS}(V_{OV} - y(x)\upsilon_{DS})\frac{dy(x)}{dx} \tag{18.18d}$$

By KCL, the current along the inversion layer must remain *constant*. If this condition is enforced, Eq. (18.18c) becomes a nonlinear ODE augmented with the boundary conditions Eq. (18.18a). It allows us to find the voltage profile $y(x)$ along the channel analytically. The corresponding solution has the form (the proof is suggested as one of the homework problems)

$$y(x) = m - \sqrt{m^2 - (2m-1)\frac{x}{L}}, \quad \frac{dy}{dx} = \frac{1}{L}\frac{m-0.5}{m-y(x)}, \quad m = \frac{\upsilon_{\mathrm{OV}}}{\upsilon_{\mathrm{DS}}} \tag{18.18e}$$

The profile $y(x)$ is quite linear ($\approx x/L$) everywhere in the channel at *small* υ_{DS} and close to the source for *any* υ_{DS}, but it becomes steeper when approaching the drain at large υ_{DS}. Since all channel parameters are now defined, the transistor current can be calculated by picking up any point along the channel. An alternative and more common approach is to integrate Eq. (18.18d) from x to L and use boundary conditions Eq. (18.18a) along with the constant-current condition. Either method gives the simple final expression for the drain current in the form:

$$i_{\mathrm{D}} = k_n\left(\upsilon_{\mathrm{GS}} - \frac{1}{2}\upsilon_{\mathrm{DS}} - V_{\mathrm{Th}}\right)\upsilon_{\mathrm{DS}} \tag{18.19}$$

Equation (18.19) reveals a nonlinear (parabolic) dependence of i_D on υ_{DS}; this is an *exact* result. We could still use Eq. (18.17) too. However, r_{DS} is no longer constant; it becomes voltage dependent, i.e.,

$$r_{\mathrm{DS}} = \frac{1}{k_n\left(\upsilon_{\mathrm{GS}} - \frac{1}{2}\upsilon_{\mathrm{DS}} - V_{\mathrm{Th}}\right)} \tag{18.20}$$

and increases with increasing υ_{DS}. When the drain-source voltage υ_{DS} is small compared to $\upsilon_{\mathrm{GS}} - V_{\mathrm{Th}}$, the nonlinear MOSFET model is reduced to a linear one. Equation (18.19) becomes asymptotically equivalent to Eq. (18.16), and Eq. (18.20) reduces to Eq. (18.17).

18.2.4 Saturation Region

As υ_{DS} continues to increase and eventually reach $\upsilon_{\mathrm{GS}} - V_{\mathrm{Th}}$, the tip of the inversion layer in Fig. 18.12b becomes infinitely thin since the inversion layer charge in Eq. (18.18b) is

exactly zero at $x = L$. This effect is known as the *channel pinch-off*. It determines entering the *saturation region* of a MOSFET. The terminal drain current *(saturation current*) is found from Eq. (18.19) to be

$$i_{\mathrm{Dsat}} = \frac{1}{2} k_n V_{\mathrm{OV}}^2 = \frac{1}{2} k_n (v_{\mathrm{GS}} - V_{\mathrm{Th}})^2 \tag{18.21a}$$

This corresponding drain-source voltage is known as the *drain saturation voltage*:

$$v_{\mathrm{DSsat}} = V_{\mathrm{OV}} = v_{\mathrm{GS}} - V_{\mathrm{Th}} \tag{18.21b}$$

While the MOSFET model correctly estimates the saturation voltage and the saturation current, it has one major drawback: the finite current at zero inversion charge would imply infinite carrier velocity. This contradiction has its roots in semiconductor physics. Figure 18.13 provides an explanation. The carrier velocity in a semiconductor cannot exceed a certain value $v \leq v_{\mathrm{sat}}$, which is known as the *saturation velocity*. An excess electric field (or voltage) applied to accelerate carriers even further will result in the generation of certain *optical phonons* (atom vibrations that light) and the loss of extra kinetic energy. Thus, the artificial carrier-free pinch-off region is in fact a *small velocity saturation region* that appears near the drain in Fig. 18.13.

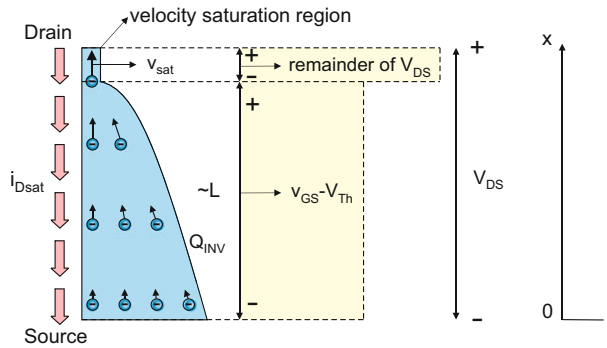


Fig. 18.13. Channel behavior at saturation voltage and beyond and voltage drops across the respective channel areas. The charge profile is an exact nonlinear solution of Eq. (18.18).

The model of the MOSFET in saturation shown in Fig. 18.13 is quantified as follows. A portion of v_{DS} equal to the overdrive voltage, $v_{\mathrm{GS}} - V_{\mathrm{Th}}$, is spent to create the tapered channel with the saturation drain current given by Eq. (18.21a). At the end of this channel, we enter the velocity saturation region. *Any excess portion* of v_{DS} is applied solely to the velocity saturation region. However, such an excess voltage does not change the inversion charge in this region:

$$Q_{\mathrm{INV}} = -i_{\mathrm{Dsat}}/(W v_{\mathrm{sat}}) \tag{18.22}$$

since the carrier velocity is fixed at v_{sat}. Instead, the electric field energy is transformed into lattice vibrations. An important conclusion is that the drain current *does not change* either with increasing v_{DS} above the overdrive voltage, $v_{\mathrm{GS}} - V_{\mathrm{Th}}$. It remains equal to i_{Dsat} from Eq. (18.21a).

18.2.5 The v-i Dependencies

Table 18.3 summarizes the simple yet accurate model of the NMOS transistor established in this section.

Table 18.3. Model of the NMOS transistor.

Region	Conditions on v_{GS} and v_{DS}	Drain current i_{D}
Triode	$v_{\mathrm{GS}} > V_{\mathrm{Th}}$ $v_{\mathrm{DS}} < v_{\mathrm{GS}} - V_{\mathrm{Th}}$	$i_{\mathrm{D}} = k_n\left((v_{\mathrm{GS}} - V_{\mathrm{Th}})v_{\mathrm{DS}} - \frac{1}{2}v_{\mathrm{DS}}^2\right)$ (18.23a)
Saturation	$v_{\mathrm{GS}} > V_{\mathrm{Th}}$ $v_{\mathrm{DS}} \geq v_{\mathrm{GS}} - V_{\mathrm{Th}}$	$i_{\mathrm{D}} = \frac{1}{2}k_n(v_{\mathrm{GS}} - V_{\mathrm{Th}})^2$ (18.23b) (index *sat* is omitted)
Cutoff	$v_{\mathrm{GS}} \leq V_{\mathrm{Th}}$	$i_{\mathrm{D}} = 0$ (18.23c)

Example 18.3: A NMOS transistor has the following parameters: $V_{\mathrm{Th}} = 2$ V and $k_n = 3$ mA/V^2. Plot the drain current for source-drain voltages from the interval $v_{\mathrm{DS}} = [0-9]$ V and at three values of the gate-source voltage $v_{\mathrm{GS}} = 3$, 4, and 5 V on the same figure.

Solution: We determine the saturation voltages first. According to the definition, $v_{\mathrm{DSsat}} = v_{\mathrm{GS}} - V_{\mathrm{Th}} = 1$, 2, and 3 V. Below these voltages, the triode model Eq. (18.23a) is used. It results in a parabola, whose top point is exactly at the saturation voltage. Above those voltages, the current remains constant; it is equal to the saturation current from Eq. (18.23b). The corresponding values are $i_{\mathrm{DGS}} = 1.5$, 6, and 13.5 mA. The result is shown in Fig. 18.14a. Note that the boundary between the two regions (triode and saturation) is another parabola:

$$i_{\mathrm{D}} = 0.5k_n{v_{\mathrm{DS}}}^2 \tag{18.24}$$

Also note the linear subregion of the triode region at small drain-source voltages.

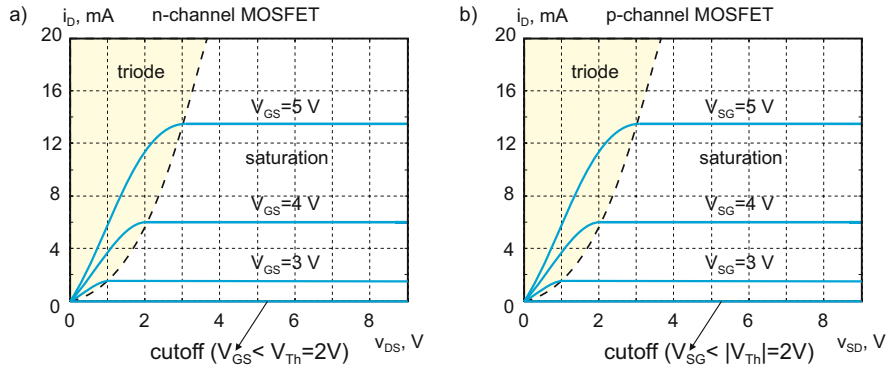


Fig. 18.14. (**a**) Drain current as a function of the drain-source voltage for an NMOS transistor with $V_{\text{Th}} = 2$ V and $k_n = 3$ mA/V^2. (**b**) Drain current as a function of the source-drain voltage for a PMOS transistor with $|V_{\text{Th}}| = 2$ V and $k_{\text{p}} = 3$ mA/V^2.

Example 18.4: An enhancement-mode NMOS transistor is characterized by $k_n = 4$ mA/V^2. For a given set of bias voltages, determine the region of operation and calculate the transistor's drain current:

A. $v_{\text{GS}} = 3$ V, $v_{\text{DS}} = 10$ V, and $V_{\text{Th}} = 2$ V.
B. $v_{\text{GS}} = -2$ V, $v_{\text{DS}} = 10$ V, and $V_{\text{Th}} = 1$ V.
C. $v_{\text{GS}} = 3$ V, $v_{\text{DS}} = 2$ V, and $V_{\text{Th}} = 2$ V.
D. $v_{\text{GS}} = 3$ V, $v_{\text{DS}} = 0.5$ V, and $V_{\text{Th}} = 2$ V.

Solution: We inspect the inequalities from Table 18.3. Case A then corresponds to saturation, Case B to cutoff (irrespective of drain-to-source voltage), Case C to saturation, and Case D corresponds to the triode region. The transistor current (drain current i_{D}) is given by Eq. (18.23). Therefore, one has

A $i_{\text{D}} = 2$ mA, B $i_{\text{D}} = 0$ mA, C $i_{\text{D}} = 2$ mA, and D $i_{\text{D}} = 1.5$ mA.

Exercise 18.4: For the circuit of Fig. 18.11, determine the region of MOSFET operation as well as the drain current i_{D} for each set of conditions given. Assume $k_n = 90$ mA/V^2 and $V_{\text{Th}} = 2$ V for the general-purpose 2 N7000 MOSFET.

A. $v_{\text{GS}} = 4.5$ V, $v_{\text{DS}} = 2$ V.
B. $v_{\text{GS}} = 4.5$ V, $v_{\text{DS}} = 8$ V.
C. $v_{\text{GS}} = 1.5$ V, $v_{\text{DS}} = 8$ V.

Answer:
A) Triode, $i_{\text{D}} = 270$ mA. B) Saturation, $i_{\text{D}} = 281$ mA. C) Cutoff, $i_{\text{D}} = 0$.

18.2.6 PMOS Transistor

A similar analysis can be repeated for the PMOS transistor with inverted doping concentrations. Table 18.4 summarizes the model of the PMOS transistor. The corresponding test circuit is shown in Fig. 18.15. Note that the $|V_{Th}|$ is used since V_{Th} itself is negative. Also note that v_{SG} and v_{SD} are both positive. Table 18.4 is identical to Table 18.3 to within the substitutions $v_{GS} \rightarrow v_{SG}$, $v_{DS} \rightarrow v_{SD}$, and $|V_{Th}| \rightarrow V_{Th}$.

Table 18.4. Model of the PMOS transistor.

Region	Conditions on v_{SG} and v_{SD}	Drain current $i_D \geq 0$
Triode	$v_{SG} > \|V_{Th}\|$ $v_{SD} < v_{SG} - \|V_{Th}\|$	$i_D = k_p\big((v_{SG} - \|V_{Th}\|)v_{SD} - \frac{1}{2}v_{SD}^2\big)$ (18.25a)
Saturation	$v_{SG} > \|V_{Th}\|$ $v_{SD} \geq v_{SG} - \|V_{Th}\|$	$i_D = \frac{1}{2}k_p(v_{SG} - \|V_{Th}\|)^2$ (18.25b) (index *sat* is omitted)
Cutoff	$v_{SG} < \|V_{Th}\|$	$i_D = 0$ (18.25c)

Exercise 18.5: Solve Example 18.3 for the PMOS transistor with $|V_{Th}| = 2$ V, $k_p = 3$ mA/V^2, and $v_{SG} = 3$, 4, and 5 V.

Answer: The solution is shown in Fig. 18.14b.

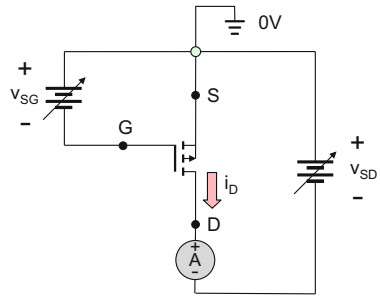


Fig. 18.15. Schematic diagram of the PMOS transistor test circuit.

18.2.7 Large-Signal MOSFET Model in Saturation

The saturation region of a MOSFET is important for amplifier applications and for fast digital switching circuits. Consider the NMOS transistor: according to Table 18.3, the transistor behaves as a *constant-current* source in the saturation region for any value of $v_{DS} > v_{GS} - V_{Th}$. However, if the gate-source voltage v_{GS} is now varied, the MOSFET becomes a *voltage-controlled current source* with respect to v_{GS}, as long as it remains in the saturation region. The corresponding result is given by Eq. (18.23b), which is valid for $v_{DS} > v_{GS} - V_{Th}$ and $v_{GS} > V_{Th}$. This is a parabolic dependence. Figure 18.16

illustrates its behavior for $k_p = 90\ \text{mA/V}^2$ and a threshold voltage of 2 V. The parabola in Fig. 18.16 is known as the *transconductance curve* of the MOSFET, which expresses the output current i_D in terms of v_{GS}. The transconductance curve terminates at $v_{GS} = V_{Th}$.

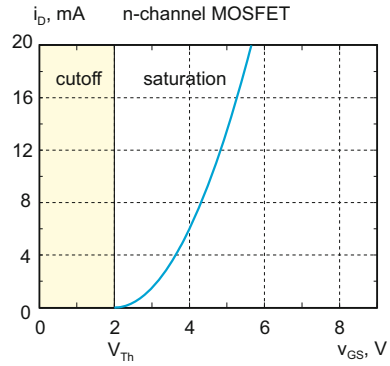


Fig. 18.16. Transconductance curve of the NMOS transistor (i_D versus v_{GS}).

Figure 18.17 shows the equivalent circuit representation of the NMOS transistor in the saturation region. The voltage-controlled nonlinear current source is described by the dependence $i_D = \frac{1}{2}k_n(v_{GS} - V_{Th})^2$. This is the *large-signal MOSFET model in saturation*, which is valid for any values of v_{GS} and i_D, both under DC and AC conditions. A similar model is established for the PMOS transistor.

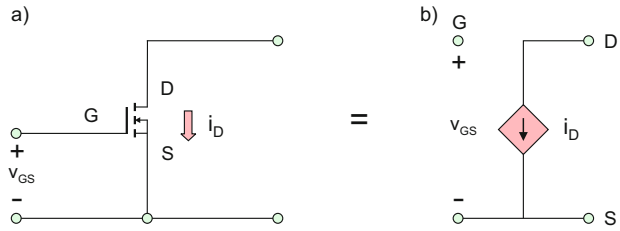


Fig. 18.17. MOSFET large-signal (nonlinear) current source model.

18.2.8 Device Parameters in CMOS Processes

In order to determine the MOSFET model, we need to know the MOSFET transconductance parameter k_n or k_p. Their values are determined by oxide capacitance C_{OX} and electron/hole surface mobility μ_{ns}/ μ_{ps}, along with gate dimensions L and W. Table 18.5 is an extension of Table 18.1; it provides the corresponding information for CMOS processes used in the design of analog ICs. This information may be used to find the corresponding transconductance parameter (the lumped process parameter).

Table 18.5. Minimum channel lengths, oxide capacitances, and surface mobilities for some CMOS processes. Note that 1 $\mathrm{fF}/\mu\mathrm{m}^2 = 10^{-7}\mathrm{F}/\mathrm{cm}^2$, $\varepsilon_{\mathrm{OX}} = 3.45 \times 10^{-13}\mathrm{F}/\mathrm{cm}$ (SiO_2 oxide).

Parameter	0.5-μm process		0.25-μm process		0.18-μm process		0.13-μm process	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
$C_{\mathrm{OX}} = \frac{\varepsilon_{\mathrm{OX}}}{t_{\mathrm{OX}}}$ $(\mathrm{fF}/\mu\mathrm{m}^2)$	3.8	3.8	5.8	5.8	8.6	8.6	12.8	12.8
μ_{ns} $\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ or μ_{ps} $\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$	500	180	460	160	450	100	400	100
V_{Th} (V)	0.7	−0.8	0.5	−0.6	0.5	−0.5	0.4	−0.4

Section 18.3 MOSFET Switching and Bias Circuits

All problems in this section assume DC steady-state analysis. This is also valid for digital switching circuits where we will ignore the transition region between the two stable states. Still, transistor terminal voltages and drain current (in contrast to the supply voltages) will be denoted by *small* letters to emphasize that many results of this section are also applicable to the variable signals, either in the exact form or approximately.

18.3.1 Triode Region for Switching Circuits: Device Parameter Extraction

Turn-On Resistance and Its Behavior

Consider switching applications where values of v_{DS} are expected to be near 0 V and much less than the overdrive voltage $v_{GS} - V_{Th}$. In this case, the v-i characteristic of the MOSFET belongs to the linear subregion of the triode region; this is seen in Fig. 18.18. Therefore, the MOSFET is modeled as a DC resistance (*turn-on resistance*), r_{DS}.

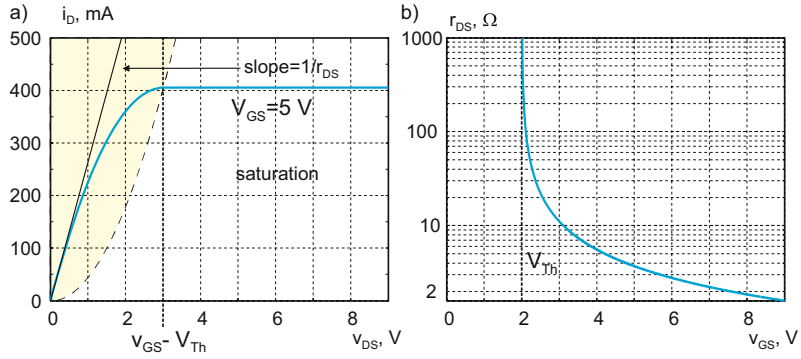


Fig. 18.18. MOSFET turn-on resistance r_{DS} and its dependence on gate-source voltage for a 2 N7000 NMOS device.

The value of this resistance is easily found by finding the slope of the $v_{DS} - i_D$ characteristic at the origin and inverting the result. It is given by Eq. (18.17) of the previous section, i.e.,

$$i_D = \frac{v_{DS}}{r_{DS}}, \quad r_{DS} = \frac{1}{k_n(v_{GS} - V_{Th})} \quad \text{NMOS transistor} \tag{18.26}$$

Example 18.5: A general-purpose 2N7000 NMOS transistor has the lumped process parameter $k_n = 90\ \text{mA/V}^2$ and a threshold voltage of 2.0 V. The gate-source voltage is 5 V. Plot the drain current for drain-source voltages over the interval $v_{DS} = [0-9]$ V and determine the MOSFET's turn-on resistance.

Example 18.5 (cont.):
Solution: We determine the saturation voltage first. According to the definition, $v_{DSsat} = v_{GS} - V_{Th} = 3$ V. Below this voltage the triode model Eq. (18.23a) is used; above this voltage the saturation model Eq. (18.23b) applies, that is,

$$i_D = k_n\left((v_{GS} - V_{Th})v_{DS} - \frac{1}{2}v_{DS}^2\right), \quad v_{DS} < 3 \text{ V} \tag{18.27a}$$

$$i_D = \frac{1}{2}k_n(v_{GS} - V_{Th})^2, \quad v_{DS} \geq 3 \text{ V} \tag{18.27b}$$

The result is shown in Fig. 18.18a. The turn-on resistance from Eq. (18.26) is $r_{DS} = 3.7\ \Omega$.

It is important to emphasize the turn-on resistance has a strong dependence on the gate-source voltage, as seen in Fig. 18.18b. Higher v_{GS} (higher overdrive voltages) lead to smaller resistances, which is usually desirable. The MOSFET turn-on resistance r_{DS} is typically plotted as a function of v_{GS} for quick reference in specification sheets. Often, a logarithmic scale plots the resistance.

Exercise 18.5: Using the data of the previous example, plot r_{DS} as a function of v_{GS}.

Answer: The plot is given in Fig. 18.18b. The threshold voltage is clearly seen.

Device Parameter Extraction

Although most MOSFET specification sheets provide values for V_{Th}, most do not give values for the lumped process parameter k_n. Therefore, one convenient method of determining the threshold voltage V_{Th} and the lumped process parameter k_n from the MOSFET data is to select two distinct data points on the resistive characteristic similar to Fig. 18.18b, insert each into Eq. (18.6), and then solve the resulting system of two equations for V_{Th} and k_n. This technique is often called *MOSFET parameter extraction*; it is used for device modeling.

Exercise 18.6: Determine the threshold voltage V_{Th} and the lumped process parameter k_n for a given MOSFET having the following turn-on resistances at gate-to-source voltages: [$v_{GS} = 4$ V, $r_{DS} = 500\ \Omega$] and [$v_{GS} = 6$ V, $r_{DS} = 100\ \Omega$].

Answer: $V_{Th} = 3.5$ V, $k_n = 4$ mA/V^2.

Since the turn-on resistance of a MOSFET is a key parameter, it is typically specified in manufacturer datasheets for a given pair of v_{GS} and i_D values. This information may also be used to find r_{DS} at other gate-source voltages as illustrated in the example that follows.

Example 18.6: The datasheet for an IRF510 enhanced-mode n-channel power MOSFET reports the drain-source *on-state resistance*:

$$r_{DS} = v_{DS}/i_D = 0.54\ \ \Omega \tag{18.28a}$$

for $i_D = 3.4\,\text{A}$ and $v_{GS} = 10\,\text{V}$. Determine r_{DS} when $v_{GS} = 5$ V and 15 V, respectively. Assume threshold voltage to be 2.0 V.

Solution: From Eq. (18.26), we find

$$k_n = \frac{1}{r_{DS}(v_{GS} - V_{Th})} = 232\ \ \text{mA/V}^2 \tag{18.28b}$$

Therefore, using the same expression for the drain-source resistance, one has

$$r_{DS} = 1.44\ \ \Omega\ \text{ for }\ v_{GS} = 5\ \text{V}, \quad r_{DS} = 0.33\ \ \Omega\ \text{ for }\ v_{GS} = 15\ \text{V} \tag{18.28c}$$

Higher overdrive voltages lead to smaller turn-on resistances of the MOSFET.

Exercise 18.7: Solve the previous example when V_{Th} changes to 4 V.

Answer: $r_{DS} = 4.31\ \ \Omega$ for $v_{GS} = 5$ V, $\quad r_{DS} = 0.39\ \ \Omega$ for $v_{GS} = 15$ V.

18.3.2 Resistor-Switch Model in Triode Region

Equation (18.26) is valid for MOSFET switching applications where the voltage across the MOSFET is expected to be small, $0 < v_{DS} << v_{GS} - V_{Th}$. Under this condition, a simple *resistor-switch model* can be used for the NMOS transistor that is shown in Fig. 18.19a. This model includes an *ideal* switch and a series resistor. Similar to the NMOS transistor, the resistor-switch model for the p-channel MOSFET is developed in exactly the same way; it is shown in Fig. 18.19b. This model is valid for $0 < v_{SD} << v_{SG} - |V_{Th}|$; see Table 18.4 for the PMOS transistor polarities. Care must be taken, however, not to mix the NMOS and PMOS parameters together in the same equations. When both devices are used, an additional subscript of n or p is generally desirable to distinguish between them. In addition, the threshold voltage for the PMOS device is specified as a negative number. Therefore, its absolute value is employed when defining the turn-on resistance in the form

$$i_D = \frac{v_{SD}}{r_{DS}} > 0, \quad r_{DS} = \frac{1}{k_p(v_{SG} - |V_{Th}|)} \quad \text{PMOS transistor} \tag{18.29}$$

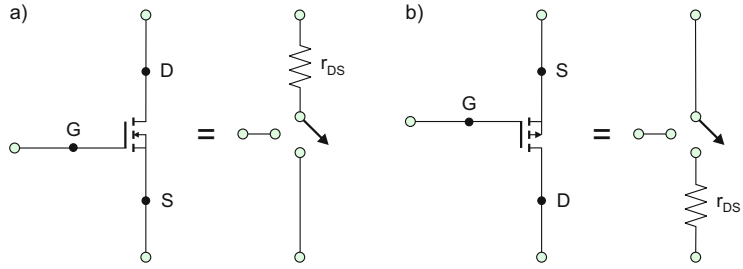


Fig. 18.19. MOSFET resistor-switch model in the triode region.

Exercise 18.8: For the resistor-switch model in Fig. 18.19a, determine r_{DS} given $k_n = 90$ mA/V^2 and the threshold voltage of 2.0 V. The gate-source voltage is 4, 5, and 6 V.

Answer: 5.56 Ω, 3.70 Ω, 2.78 Ω.

The resistor-switch model is applied as follows. When $v_{GS} < V_{Th}$ for the NMOS transistor, the switch in Fig. 18.19a is an open circuit. Otherwise, we assume it is a short circuit. Similarly, when $v_{SG} < |V_{Th}|$ for the PMOS transistor, the switch in Fig. 18.19a is an open circuit. Otherwise, it is a short circuit.

18.3.3 Application Example: Output Resistance of Digital Logic Gates

Use of the Resistor-Switch Model

The MOSFET resistor-switch model from Fig. 18.19 is used extensively as an estimation tool in the design of digital logic gates shown in Fig. 18.20. The particular gate chosen is a CMOS NOT gate or a *logic inverter* comprised of one PMOS and one NMOS device. Such a configuration with two complementary MOSFETs is a ubiquitous circuit in CMOS-based digital logic. This circuit can be implemented as a tiny building block and replicated billions of times as part of microprocessors and memory chips, making possible high-density microelectronic integrated circuits.

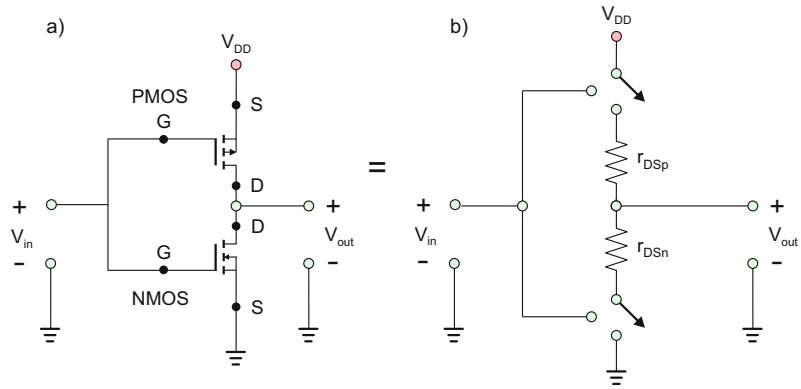


Fig. 18.20. A circuit with a complementary MOSFET pair; the configuration is known as a logic CMOS inverter. Note that the output voltage is open circuited.

The circuit in Fig. 18.20a is replaced by the resistor-switch model in Fig. 18.20b. We assume that $V_{DD} > V_{Th}$ for the NMOS transistor and $V_{DD} > |V_{Th}|$ for the PMOS transistor. The circuit solution implies the inspection of gate-source voltages for either input voltage. It results in the *truth table* 18.6, which indicates the state of each MOSFET for a given input voltage and resulting output voltage. A logic "1" corresponds to a voltage level of V_{DD} and a logic "0" corresponds to 0 V.

Table 18.6. CMOS NOT gate truth table and MOSFET switch states.

Inputs	NMOS switch	PMOS switch	Output
0	OFF	ON	1
1	ON	OFF	0

Gate Output Resistance and Its Value

The *output resistance of the logic gate* is defined as the resistance of the equivalent Thévenin circuit seen by the output terminal. The corresponding Thévenin voltage (either V_{DD} or 0 V) has no influence on the output resistance. The output resistance of the gate will vary. For the NOT gate in Fig. 18.20, $r_{OUT} = r_{DSp}$ when the input is logic 0 and $r_{OUT} = r_{DSn}$ when the input is logic 1. Generally, $r_{DSn} \neq r_{DSp}$. More complicated combinations occur for other gates such as a NAND gate shown in Fig. 18.21. The output resistance of the gate is important in predicting the fundamental parameter of digital circuits, *the gate propagation delay*, which is determined by the time constant of an RC circuit formed by r_{OUT} and MOSFET capacitances. Strictly speaking, the resistor-switch DC model in the triode region loses its validity during the transition between two gate stages, where the MOSFETs enter the saturation region. However, r_{OUT} found with the help of this model will still provide simple and useful design estimates.

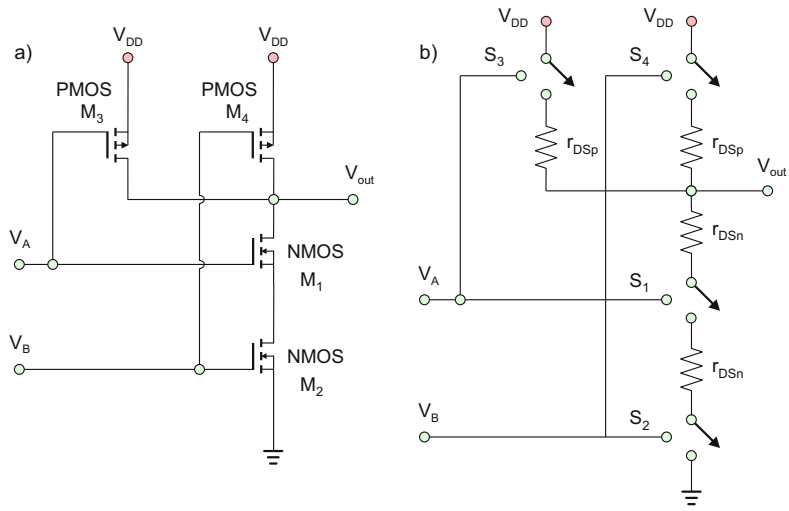


Fig. 18.21. The NAND gate with two identical PMOS transistors and two identical NMOS transistors. The output voltage is open circuited, similar to Fig. 18.20.

Example 18.7: For the NAND gate in Fig. 18.21a, construct the truth table and determine the output gate resistance for every input voltage combination. Assume $V_{DD} > V_{Th}$ for the NMOS transistor and $V_{DD} > |V_{Th}|$ for the PMOS transistor.

Solution: The circuit in Fig. 18.21a is replaced by the resistor-switch model in Fig. 18.21b. The gate-source voltages of every individual transistor are found by inspection. They determine whether the transistor is on or off. If a direct conduction path from V_{DD} to the output results, the output voltage is V_{DD} or logic 1. If a direct conduction path from ground to the output occurs, the output voltage is 0 V or logic 0. The corresponding truth table, Table 18.7, contains an extra column where the gate output resistance is reported. For example, when both A and B are logic 1, both NMOS devices are on, and since they are *in series* the resistance between the output and ground is $r_{DSn} + r_{DSn}$. On the other hand, if both A and B are logic 0, both PMOS devices are on and they are wired *in parallel*, so the output resistance is $r_{DSp} || r_{DSp}$.

Table 18.7. CMOS NAND gate truth table, MOSFET switch states, and output resistances.

Inputs		NMOS		PMOS		Output	r_{OUT}
A	B	M_1	M_2	M_3	M_4		
0	0	OFF	OFF	ON	ON	1	$r_{DS3} \| \| r_{DS4}$
0	1	OFF	ON	ON	OFF	1	r_{DS3}
1	0	ON	OFF	OFF	ON	1	r_{DS4}
1	1	ON	ON	OFF	OFF	0	$r_{DS1} + r_{DS2}$

18.3.4 MOSFET Circuit Analysis at DC

Method of Assumed States

A DC circuit with MOSFET(s) is solved using the *method of assumed states*, similar to the large-signal DC model for the junction transistor. Initially, we assume one of the states—saturation, triode, or cutoff—and solve the resulting circuit. The complete large-signal transistor models, Eq. (18.23) (Table 18.3) for the NMOS transistor and Eq. (18.25) (Table 18.4) for the PMOS transistor, are employed. Then, the inequalities for the transistor voltages are checked. If they are satisfied, the solution is correct. If not, another region of operation is selected. If the transistor state found through inspection is not cutoff, it is often convenient to assume the saturation first and solve for v_{DS}. If this value is larger than the effective voltage of $v_{GS} - v_{Th}$, the solution is correct. Otherwise, the operating region is triode and the quadratic equation applies. After a certain amount of practice, the method of assumed states, which always provides a *unique solution*, becomes easy to apply.

Load-Line Analysis

The *load-line analysis* implies the graphical or analytical representation of the solution in the form of an intersection of two curves: the nonlinear v_{DS}—i_D transistor dependence

and the linear Ohm's law for the (load) resistor expressed in terms of the same two quantities. Examples that follow will illustrate the load-line method.

Example 18.8: Consider a *gate-bias* (or *fixed-gate*) NMOS transistor circuit shown in Fig. 18.22. An NMOS transistor has the lumped process parameter $k_n = 1.0\ \text{mA/V}^2$ and a threshold voltage of 1.0 V. The gate-source voltage is 5 V. Solve the circuit, i.e., find drain-source voltage v_{DS} and current i_D.

Solution: Since $v_{GS} > V_{Th}$, the transistor is ON; it is either in the saturation region or in the triode region. We make a guess and assume that the device operates in the saturation region; this yields

$$i_D = \frac{k_n}{2}(v_{GS} - V_{Th})^2 = 8\ \text{mA} \tag{18.29a}$$

Therefore, $V_{RD} = R_D i_D = 8$ V. The drain-source voltage, by KVL, gives

$$V_{DS} = 20\ \text{V} - 8\ \text{V} = 12\ \text{V} \tag{18.29b}$$

The condition of the saturation region $V_{DS} > V_{GS} - V_{Th} = 4$ V is satisfied; the drain current is 8 mA. The circuit is thus solved.
A check of other operation regions will yield all negative results. The graphical form of the solution is shown in Fig. 18.23a. We plot the transistor current given either by $i_D = k_n\left((v_{GS} - V_{Th})v_{DS} - \frac{1}{2}v_{DS}^2\right)$ in the triode region or by Eq. (18.29a) in the saturation region. Simultaneously, the general *linear load line* $i_D = (V_{DD} - v_{DS})/R_D$ plots the same current but found using the Ohm's law for the resistor R_D. The intersection of two of them corresponds to the solution for the drain-source voltage. This intersection clearly occurs in the saturation region. The boundary between the triode and saturation regions is a parabola $i_D = 0.5k_n' v_{DS}^2$, which follows from Eq. (18.29a) with $v_{DS} = v_{GS} - V_{Th}$.

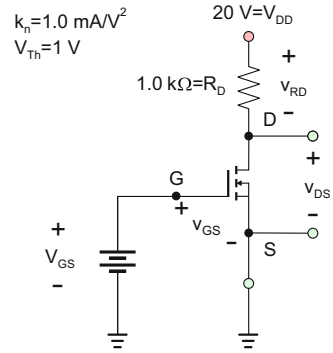


Fig. 18.22. Gate-bias NMOS transistor circuit; it is the bias circuit for the common-source MOSFET amplifier.

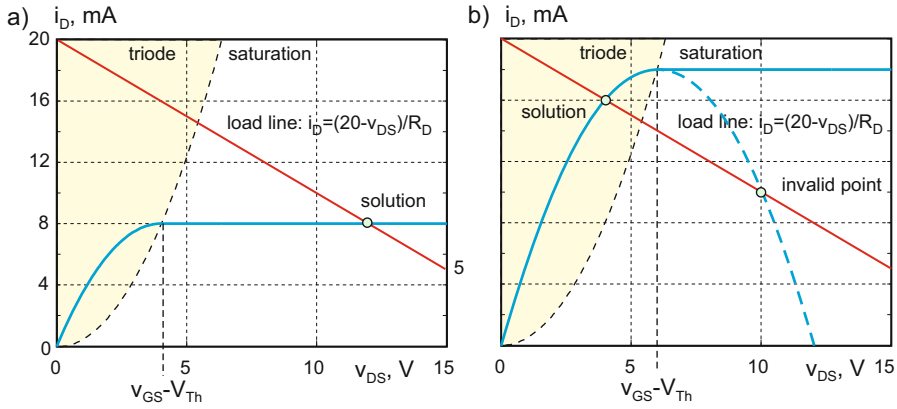


Fig. 18.23. Graphical representation of the solution for the DC circuit in Fig. 18.22 and intersection of the load line with the v_{DS}—i_D curve. (**a**) NMOS transistor in saturation and (**b**) NMOS transistor in triode region.

Example 18.9: Repeat the previous example when the gate-source voltage changes from 5 V to 7 V.

Solution: As long as $v_{GS} > V_{Th}$, the transistor is ON. We select the saturation region and find $i_D = 0.5k_n(v_{GS} - V_{Th})^2 = 18$ mA. Therefore, $V_{DS} = 20\text{ V} - 18\text{ V} = 2$ V. However, the condition of the saturation region $V_{DS} > V_{GS} - V_{Th} = 6$ V is *not* satisfied. The triode region must be therefore chosen. In the triode region, we have to assume $i_D = k_n((v_{GS} - V_{Th})\, v_{DS} - \frac{1}{2}v_{DS}^2)$. However, Ohm's law for the resistor predicts the linear dependence in the form of the load line $i_D = (V_{DD} - v_{DS})/R_D$. Setting both results equal to each other, we obtain a *quadratic* equation in v_{DS}

$$\frac{20\text{ V-}v_{DS}}{R_D} = k_n\left((v_{GS} - V_{Th})v_{DS} - 0.5v_{DS}^2\right) \tag{18.30}$$

This equation is reduced to $20 - v_{DS} = 6v_{DS} - 0.5v_{DS}^2$. It can be solved directly using a calculator. There are two roots: $v_{DS} = 4$ V and $v_{DS} = 10$ V. The second (*larger*) root is non-physical since it is located within the already abandoned saturation region. The first root is the true solution; the corresponding drain current is given by 16 mA. The graphical form of the solution is shown in Fig. 18.23b. We again plot the v_{DS}—i_D transistor curve along with linear load line $i_D = (V_{DD} - v_{DS})/R_D$. There are two intersections corresponding to the two roots for v_{DS} obtained above. The load line method provides physical insight into the problem and the ability to modify the solution in a controlled way if necessary. For example, with reference to Fig. 18.23 we can decide which circuit parameters need to be changed to move the solution from the triode to the saturation region and vice versa.

Exercise 18.9: In the circuit shown in Fig. 18.22 we use the model that represents the 2N7000 NMOS transistor from Fairchild with the lumped process parameter $k_n = 90$ m A/V^2 and the threshold voltage of 2.0 V. Find the drain-source voltage v_{DS} and the drain current i_{D} given $R_{\text{D}} = 25\ \Omega$, $V_{\text{GS}} = 5$ V, and $V_{\text{DD}} = 10$ V.

Answer:
$v_{\text{DS}} = 1.720$ V, $i_{\text{D}} = 331.2$ mA.

The circuit in Fig. 18.22 is the bias circuit for the common-source MOSFET small-signal amplifier considered in the next section. Note that the drain resistor R_{D} and the (variable) transistor resistance r_{DS} essentially form a voltage divider and thus enable proper amplifier operation (sufficient voltage swing). This situation is similar to voltage dividers used as sensors.

Exercise 18.10: The circuit shown in Fig. 18.24a is the *diode-connected* MOSFET. This terminology is adopted from the BJT analysis: the BJT connected in a similar fashion operates like a diode. The configuration shown is a part of the *current mirror* used in integrated circuits. Determine drain current i_{D} given $V_{\text{DD}} = 5$ V, the lumped process parameter $k_n = 10$ mA/V^2, and the threshold voltage of 2.0 V.

Answer:
$i_{\text{D}} = 45$ mA.

Exercise 18.11: The circuit shown in Fig. 18.24b is the *diode-connected* MOSFET with the drain resistance. It can be used to quickly estimate the threshold voltage V_{Th} of a particular MOSFET in the laboratory at condition $v_{\text{GS}} = v_{\text{DS}}$ (which is not exactly the theoretical condition of $v_{\text{DS}} \to 0$) and at a certain (usually very small) value of the drain current. Determine the MOSFET's threshold voltage V_{Th} if the circuit in Fig. 18.24b, with $R_D = 100$ kΩ, $V_{\text{DD}} = 12$ V, measures a current of $i_{\text{D}} = 100$ μA.

Answer:

$V_{\text{Th}} = v_{\text{GS}} = v_{\text{DS}} = 2$ V.

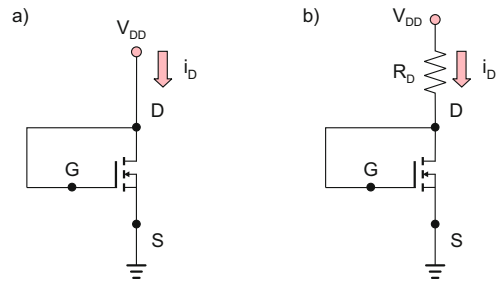


Fig. 18.24. Diode-connected MOSFET circuit with $v_{\text{GS}} = v_{\text{DS}}$.

18.3.5 Application Example: Basic MOSFET Actuator

The circuit shown in Fig. 18.25 is a straightforward modification of the gate-bias circuit from Fig. 18.22. We simply replace the second voltage supply V_{GS} by a voltage divider connected to the gate. This voltage divider operates independently in the sense that it is not affected by the gate connection since there is no current into the gate of the MOSFET. Given the fixed resistor values, this circuit may be employed as a bias circuit for the small-signal MOSFET amplifiers. Its advantage is in using only one voltage supply V_{DD}. Yet another application is a *basic MOSFET actuator device* which turns on the motor or another power load, when the sensor reading – output of the voltage divider with a sensing resistive element R_1—requires doing so. For higher-power loads, a power MOSFET should be used.

Exercise 18.12: For the circuit shown in Fig. 18.25, choose values for R_1 and R_2 to establish a drain current of 20 mA in the MOSFET. Assume $R_D = 0$. You are given $V_{DD} = 5$ V, the lumped process parameter $k_n = 90$ mA/V^2, and the threshold voltage of 2.0 V. Also, limit the voltage divider current to 20 μA.

Answer: $R_1 = 116.7$ kΩ, $R_2 = 133.3$ kΩ.

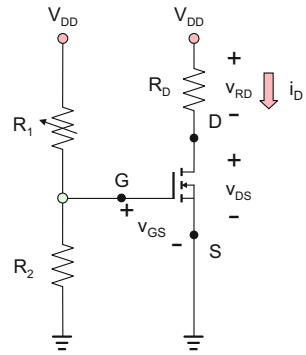


Fig. 18.25. Gate-bias NMOS transistor circuit with the voltage divider.

To be specific, R_1 is the resistance of a NTC-503 thermistor operating as

$R_1 = 50$ kΩ at 25 °C (room temperature)

$R_1 = 30$ kΩ at 37 °C

The second resistance of the voltage divider is fixed at $R_2 = 12$ kΩ. Further, a hypothetical n-channel power MOSFET with $V_{Th} = 2$ V and $k_n = 261$ mA/V^2 is considered as an example. The goal is to turn on a small 5-V DC fan motor of 0.4-W power with the equivalent load resistance $R_D = 80$ Ω if the temperature in a room (or in an enclosure) reaches 37 °C.

Exercise 18.13: Determine the load current i_D and load voltage v_D in Fig. 18.5 when $V_{DD} = 10$ V and

A. $R_1 = 50$ kΩ (room temperature).
B. $R_1 = 30$ kΩ (temperature of 37 °C).

Other device parameters are given in the text above.

Answer: A) Load current and voltages are zero; the transistor is at cutoff.
B) The transistor is in saturation; the load current is 96 mA and the load voltage is 7.7 V.

Various sensing elements (e.g., a photoresistor instead of a thermistor) and various DC motors may be used. Figure 18.26 illustrates the circuit operation with a thermistor and a more powerful 12-V motor. The basic design in Fig. 18.25 is not very practical since it suffers from variations of the MOSFET threshold voltage and other device parameters including the motor's starting current. A modification involves the use of a potentiometer instead of the fixed resistance R_2 and tuning the circuit to the proper operation region.

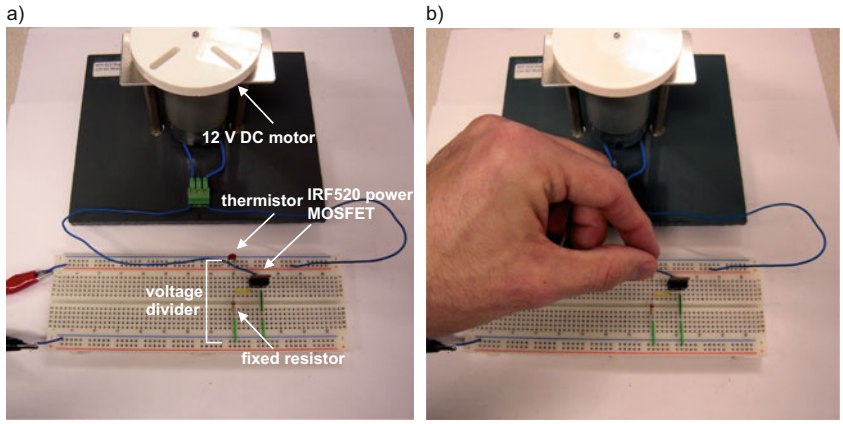


Fig. 18.26. MOSFET actuator circuit with a temperature sensor and a 12-V DC motor.

Section 18.4 MOSFET Amplifier

18.4.1 MOSFET Common-Source Amplifier

For amplifier applications, the MOSFET is typically biased into the saturation region where it behaves as a *voltage-controlled current source*. If a voltage output is desired, the current can be converted to a proportional voltage drop by pulling it through a resistor as shown in Fig. 18.27a. Figure 18.27b shows the equivalent large-signal circuit model of the amplifier. The NMOS transistor in saturation is described by a nonlinear current source following the large-signal model from Fig. 18.17, which is valid at any input voltage $\upsilon_{IN} = \upsilon_{GS}$. The output voltage to the amplifier is $\upsilon_{OUT} = \upsilon_{DS}$. The drain-source path forms a voltage divider between the fixed (R_D) and variable resistors.

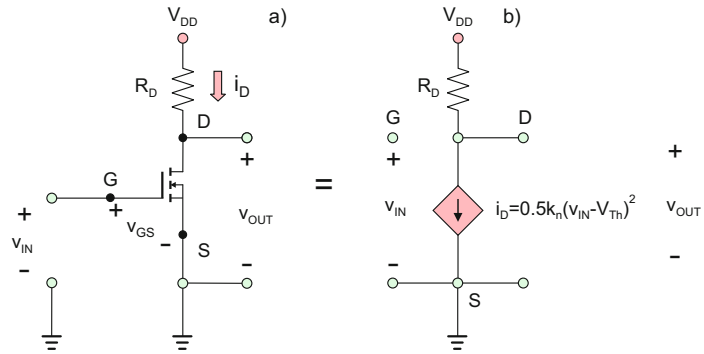


Fig. 18.27. MOSFET common-source amplifier model.

Following traditional naming schemes, when the input is at the gate and the output is at the drain, the amplifier circuit in Fig. 18.17 is identified as the *common-source amplifier*. Other amplifier configurations exist.

18.4.2 Voltage Transfer Characteristic

The *voltage transfer characteristic* of the MOSFET amplifier is obtained when plotting υ_{OUT} versus υ_{IN}. We let υ_{IN} vary from 0 V all the way to V_{DD}. For the amplifier in Fig. 18.27, the plot includes *all* three regions, cutoff, saturation, and triode, when υ_{IN} passes from 0 V to V_{DD}. Only the saturation region is meaningful. Using the large-signal model of the NMOS transistor and the load-line method in saturation, the complete expression for the output voltage as a function of the input voltage may be found analytically. The corresponding calculation results in

$$\begin{array}{lll} 0 \le v_{IN} \le V_{Th} & v_{OUT} = V_{DD} & \text{cutoff} \\ V_{Th} < v_{IN} \le (1+s)V_{Th} & v_{OUT} = V_{DD} - \dfrac{k_n}{2} R_D (v_{IN} - V_{Th})^2 & \text{saturation} \\ v_{IN} > (1+s)V_{Th} & v_{OUT} \approx \min\left((1+s)V_{Th} \ , \ \dfrac{r_{DS}}{r_{DS}+R_D} V_{DD} \right) << V_{DD} & \text{triode} \end{array} \tag{18.31}$$

In Eq. (18.31), the gate-source voltage v_{GS} has been replaced with the input voltage v_{IN} and the drain-source voltage v_{DS} has been replaced with the output voltage v_{OUT}. Equation (18.31) clearly indicates the usefulness of the saturation region: otherwise the output voltage would either not change at all (cutoff) or change very little (triode, r_{DS} is typically ~1 Ω and is much less than R_{DS}). The dimensionless parameter s characterizes the width of the saturation region as a fraction of V_{Th}; it is found by solving the quadratic equation for v_{IN} at the border of the saturation and triode regions, when $v_{OUT} = v_{IN} - V_{Th}$. Its value involves both the circuit parameters and the transistor parameters, i.e.,

$$s = \frac{\sqrt{1 + 2k_n R_D V_{DD}} - 1}{k_n R_D V_{Th}} \tag{18.32}$$

Exercise 18.14: Determine parameter s and the width of the saturation region (amplifier operating region) for the amplifier circuit built with the general-purpose 2N7000 NMOS transistor, which has the lumped process parameter $k_n = 90$ mA/V^2 and the threshold voltage of 2.0 V. The source voltage is $V_{DD} = 10$ V and $R_D = 1.2$ kΩ.

Answer: $s = 0.211$; the saturation (operating) region extends from 2 V to 2.42 V. Thus, the operating region is quite narrow.

Plotting Eq. (18.31) yields the voltage transfer characteristic for the MOSFET common-source amplifier. To be specific, we consider the parameters from Exercise 18.14 where Fig. 18.28a shows the corresponding voltage transfer characteristic.

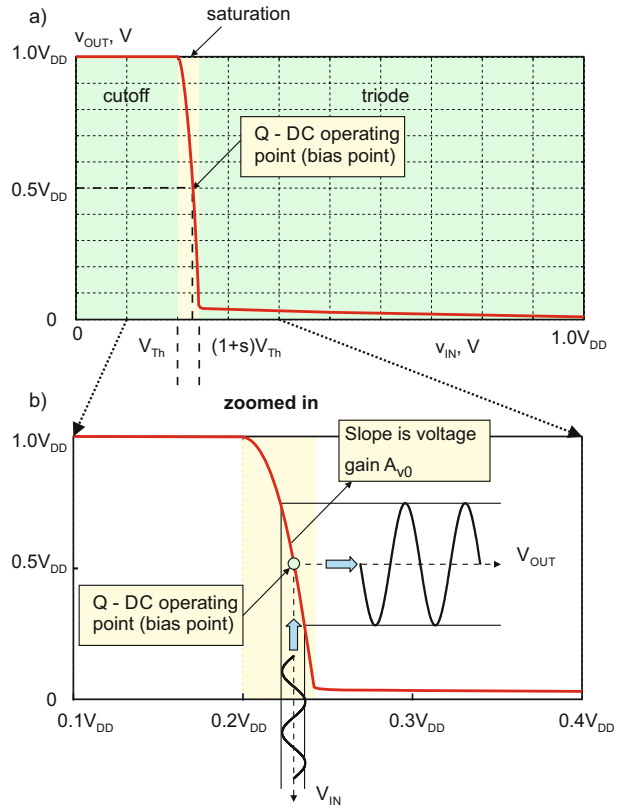


Fig. 18.28. Voltage transfer characteristic of the MOSFET common-source amplifier (**a**) and the amplification principle (**b**). The output sinusoidal signal indicates no distortion, which is a simplification. Circuit parameters are those from Exercise 18.14.

18.4.3 Principle of Operation and Q-Point

The input voltage in Fig. 18.27 is a combination of a certain DC voltage plus (typically relatively small) an input AC signal to be amplified. Then, the output voltage will be a combination of a particular DC voltage plus an amplified replica of the AC signal; see Fig. 18.28b. This is the amplifier concept. Mathematically, the *separation of large DC and small AC quantities* is done in the form (lowercase indexes are used for small AC signals):

$$\begin{aligned} v_{\mathrm{IN}}(t) &= V_{\mathrm{IN}} + v_{\mathrm{in}}(t) \\ v_{\mathrm{OUT}}(t) &= V_{\mathrm{OUT}} + v_{\mathrm{out}}(t) \\ i_{\mathrm{D}}(t) &= I_{\mathrm{D}} + i_{\mathrm{d}}(t) \end{aligned} \quad \text{or (equivalently)} \quad \begin{aligned} v_{\mathrm{GS}}(t) &= V_{\mathrm{GS}} + v_{\mathrm{gs}}(t) \\ v_{\mathrm{DS}}(t) &= V_{\mathrm{DS}} + v_{\mathrm{ds}}(t) \\ i_{\mathrm{D}}(t) &= I_{\mathrm{D}} + i_{\mathrm{d}}(t) \end{aligned} \tag{18.33}$$

The DC parameters in Eq. (18.33) correspond to the point Q in Fig. 18.28, which is known as the *DC operating point* or the *quiescent point of the NMOS transistor amplifier.* Sometimes, the index Q is introduced to underscore this fact. We will not introduce this

index assuming that the DC parameters already correspond to the desired operating point (i.e., are the *quiescent-point parameters*). The quiescent-point parameters may denote the corresponding DC bias sources, for example, $V_{IN} = V_{GS}$. The equations in (18.33) are applicable to all MOSFET small-signal amplifier models. The DC parameters must satisfy the large-signal DC circuit model *separately*, that is,

$$V_{OUT} = V_{DD} - \frac{k_n}{2} R_D (V_{IN} - V_{Th})^2 \tag{18.34}$$

18.4.4 MOSFET Biasing for Amplifier Operation

In order to use the MOSFET as an amplifier, it is necessary to bias the output to a point Q in the saturation region where the transfer characteristic is fairly linear while at the same time providing enough dynamic range for the output voltage to swing in both a positive and negative direction. In the case of Fig. 18.28, this point has been chosen to be

$$V_{Th} = 2 \text{ V} < V_{IN} = 2.3 \text{ V} < (1+s)V_{Th} = 2.42 \text{ V} \tag{18.35}$$

to establish $V_{OUT} = 5.14$ V according to Eq. (18.34). This way, a small variation in V_{IN} will cause a large variation in V_{OUT}, realizing the desired amplification; see Fig. 18.28. The amount of amplification or the *open-circuit small-signal voltage gain* A_{v0} is simply the slope of the voltage transfer characteristic at this point, approximately -30 V/V in Fig. 18.28. The negative sign indicates that the output voltage swing will be *inverted* with respect to the input.

18.4.5 Small-Signal MOSFET Model and Superposition

Our goal is to solve the circuit in Fig. 18.27. In order to do so, we will introduce a *small-signal MOSFET model*. The concept of the linear expansion (18.33) allows us to *split* the large-signal MOSFET model used previously and depicted in Fig. 18.29a into two parts. Both of them are shown in Fig. 18.29b and c respectively. The DC solution is still described by the nonlinear large-signal circuit model. At the same time, the AC solution is described by a *linear small-signal MOSFET model* in Fig. 18.29c. In the small-signal model, the change in output current i_d is equal to a gain factor g_m multiplied by the change in input voltage v_{gs}. The gain factor g_m is known as the *small-signal MOSFET transconductance*. In the small-signal model, all *constant* DC bias sources are replaced by ground (the *small-signal ground condition*) since their voltages do not change with time; the AC signal is thus shorted out.

According to Fig. 18.29, we solve the MOSFET amplifier circuit twice: the first time at DC using the large-signal DC model and the second time at AC using the small-signal model. The DC solution will provide the necessary information for the AC solution. The complete solution is found as the sum of the DC and AC solutions, respectively. In other words, the *superposition principle* applies. This is a remarkable fact given that the DC model is inherently nonlinear.

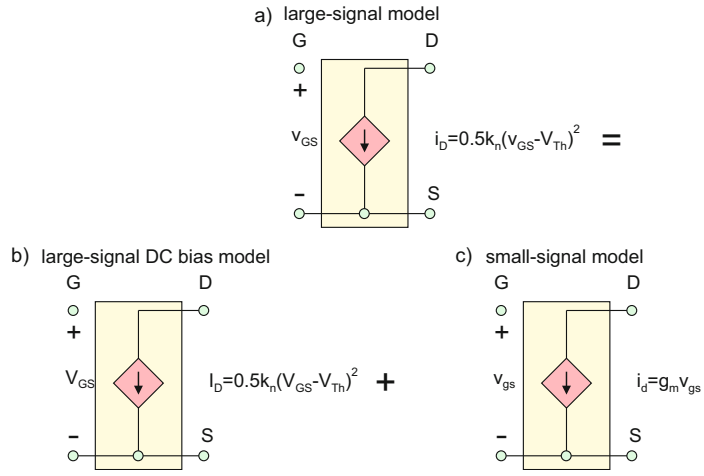


Fig. 18.29. Splitting the large-signal MOSFET model into a large-signal DC model and a small-signal model. This consideration applies to the common-source amplifier and to other circuits.

18.4.6 MOSFET Transconductance

In order to use the small-signal model, a value for the transconductance g_m must be determined. This can be found by plotting the drain current i_D as a function of the gate-to-source voltage v_GS and finding the slope of this characteristic at the bias point. Mathematically, we can use the Taylor series about the selected DC point. Substitution of the expansions $v_\mathrm{GS} = V_\mathrm{GS} + v_\mathrm{gs}$, $i_\mathrm{D} = I_\mathrm{D} + i_\mathrm{d}$ into the saturation equation $i_\mathrm{D} = \frac{k_n}{2}(v_\mathrm{GS} - V_\mathrm{Th})^2$ and the corresponding linearization yields

$$I_\mathrm{D} + i_\mathrm{d} = \frac{k_n}{2}\left(V_\mathrm{GS} + v_\mathrm{gs} - V_\mathrm{Th}\right)^2 = \frac{k_n}{2}(V_\mathrm{GS} - V_\mathrm{Th})^2 + k_n(V_\mathrm{GS} - V_\mathrm{Th})v_\mathrm{gs} + \underbrace{\frac{k_n}{2}v_\mathrm{gs}^2}_{\text{neglected}} \tag{18.36}$$

Therefore, in the general case,

$$g_\mathrm{m} = k_n(V_\mathrm{GS} - V_\mathrm{Th}) \quad [\mathrm{A/V}] \tag{18.37a}$$

or, in a practical circuit to the common-source amplifier with the bias point V_IN, V_OUT,

$$g_\mathrm{m} = k_n(V_\mathrm{IN} - V_\mathrm{Th}) \quad [\mathrm{A/V}] \tag{18.37b}$$

The transconductance can also be expressed conveniently as a function of the drain current bias:

$$g_m = \sqrt{2k_n I_D} \quad [\mathrm{A/V}] \tag{18.37c}$$

Exercise 18.15: Determine transconductance g_m for the common-source amplifier circuit with the general-purpose 2N7000 NMOS transistor, which has $k_n = 90$ mA/V^2, the threshold voltage of 2.0 V, and the Q-point at $V_{IN} = 2.3$ V.

Answer: $g_m = 27$ mA/V.

18.4.7 Analysis of Common-Source MOSFET Amplifier

We apply the formalism of the combined large-signal/small-signal MOSFET model to study and quantify the complete common-source amplifier configuration shown in Fig. 18.30a.

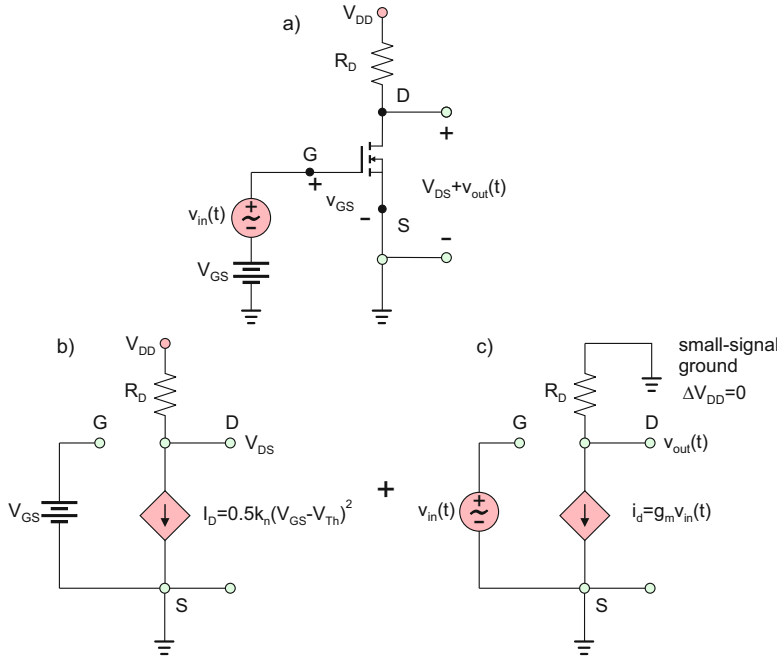


Fig. 18.30. Common-source amplifier circuit and its two equivalent circuit models.

This configuration includes a (small) input AC source $v_{in}(t)$ and a DC bias source $V_{GS} = V_{IN}$ at the input and an amplified AC voltage $v_{out}(t)$ and a DC bias voltage $V_{DS} = V_{OUT}$ at the output. The general procedure is as follows. First, we solve the large-signal DC model of the circuit in Fig. 18.30b with the small-signal sources set to zero, i.e., we find the *DC bias solution*. Substitutions $V_{IN} \leftrightarrow V_{GS}$ and $V_{DS} \leftrightarrow V_{OUT}$ can be used at any time to make the model fully compatible with the previous treatment. This solution gives us the output DC voltage V_{DS}, the DC drain current I_D, and the small-signal MOSFET transconductance g_m; see Eqs. (18.37c). Once g_m is known, we may apply the small-signal MOSFET model in Fig. 18.30c and find the major amplifier parameters of interest, the *open-circuit small-signal voltage gain* A_{v0} defined by

$$A_{v0} \equiv \left.\frac{v_{out}}{v_{in}}\right|_{R_L=\infty} \tag{18.38}$$

where R_L is a load resistance to be connected (in general) to the amplifier's output. Note the small-signal ground in Fig. 20.30c. The voltage of a constant DC source does not change with time. Therefore, this source plays the role of a ground for an AC signal, similar to the physical ground offset by a specific constant voltage. Note that most of the steps for the amplifier design procedure have already been outlined in the preceding section. Also note that a capacitively coupled output voltage may be employed to eliminate the DC voltage bias at the output.

Example 18.10: In a common-source MOSFET amplifier in Fig. 18.30a, $v_{in}(t) = 0.1\cos(\omega t)$ [V]. The general-purpose 2N7000 NMOS transistor is used, with $k_n = 90$ mA/V^2 and $V_{Th} = 2$ V. Furthermore, $V_{DD} = 10$ V and $R_D = 1.2$ kΩ. Design the amplifier by performing the following steps:

1. Solve the large-signal DC circuit model in Fig. 18.30b and determine V_{GS} (and the corresponding V_{DS}) which assures that the Q-point (the DC operating point) is in saturation region and there is enough dynamic range for the output voltage to swing in both a positive and negative direction. Determine the transistor's transconductance.
2. Solve the small-signal circuit model in Fig. 18.30c and determine the amplified AC voltage $v_{out}(t)$ and the open-circuit small-signal voltage gain A_{v0} of the amplifier.
3. Finally, plot the input and output voltages $v_{IN}(t) = V_{GS} + v_{in}(t)$, $v_{OUT}(t) = V_{DS} + v_{out}(t)$ of the amplifier to scale over two periods.

Solution (1): The saturation region is described by Eqs. (18.31) and (18.32). For the present DC circuit, the saturation region extends from $V_{Th} = 2$ V to $(1+s)V_{Th} = 2.42$ V. We select $V_{GS} = 2.3$ V in order to assure that $V_{DS} = V_{DD} - \frac{k_n}{2}R_D(V_{GS} - V_{Th})^2 = 5.14$ V is approximately in the middle of the power supply region. The small-signal transconductance is then given by $g_m = k_n(V_{GS} - V_{Th}) = 27$ mA/V.

Solution (2): The small-signal model in Fig. 18.30c yields

$$v_{out}(t) = 0 \text{ V} - g_m R_D v_{in}(t) = -3.24 \cos(\omega t) \text{ [V]} \tag{18.39}$$

Therefore, the open-circuit amplifier gain is given by (note the units)

$$A_{v0} = -g_m R_D = -32.4 \text{ [V/V]} \tag{18.40}$$

Solution (3): Input/output voltages of the amplifier circuit are finally given by

$$\begin{aligned} v_{IN}(t) &= 2.3 + 0.1\cos(\omega t) \text{ [V]}, \\ v_{OUT}(t) &= 5.14 - 3.24\cos(\omega t) \text{ [V]} \end{aligned} \tag{18.41}$$

They are plotted in Fig. 18.31. Note that Fig. 18.31 indicates no distortion of the output voltage. Such a distortion happens in reality for this particular circuit.

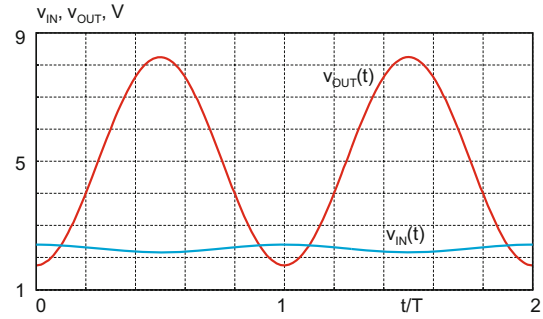


Fig. 18.31. Input and output voltages for the common-source amplifier from Example 18.10.

Summary

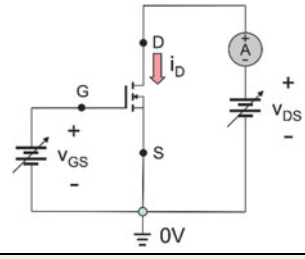
MOSFET physical characteristics

V_{Th}—threshold voltage (0.4–4 V for enhancement-mode n-channel MOSFET) [V]

$k_n = (W/L)C_{OX}\mu_{ns}$—MOSFET transconductance par. (lumped process par.) [mA/V^2]

MOSFET modeling

NMOS test circuit and regions of operations (large-signal model)



Triode $[v_{GS} > V_{Th},\ v_{DS} < v_{GS} - V_{Th}]$:

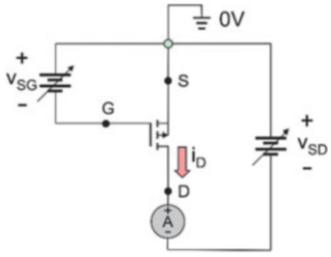
$$i_D = k_n\left((v_{GS} - V_{Th})v_{DS} - \frac{1}{2}v_{DS}^2\right)$$

Saturation $[v_{GS} > V_{Th},\ v_{DS} \geq v_{GS} - V_{Th}]$:

$$i_D = \frac{1}{2}k_n(v_{GS} - V_{Th})^2$$

Cutoff $[v_{GS} \leq V_{Th}]$: $i_D = 0$

PMOS test circuit and regions of operations (large-signal model)



Triode $[v_{SG} > |V_{Th}|,\ v_{SD} < v_{SG} - |V_{Th}|]$:

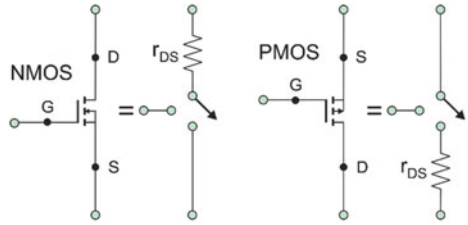
$$i_D = k_p\left((v_{SG} - |V_{Th}|)v_{SD} - \frac{1}{2}v_{SD}^2\right)$$

Saturation $[v_{SG} > |V_{Th}|,\ v_{SD} \geq v_{SG} - |V_{Th}|]$:

$$i_D = \frac{1}{2}k_p(v_{SG} - |V_{Th}|)^2$$

Cutoff $[v_{SG} \leq |V_{Th}|]$: $i_D = 0$

Resistor-switch model in triode region



NMOS: $i_D = \dfrac{v_{DS}}{r_{DS}}$, $r_{DS} = \dfrac{1}{k_n(v_{GS} - V_{Th})}$

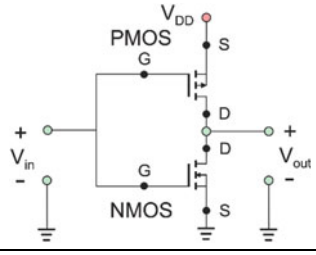
PMOS: $i_D = \dfrac{v_{SD}}{r_{DS}}$, $r_{DS} = \dfrac{1}{k_p(v_{SG} - |V_{Th}|)}$

r_{DS} may be as small as 0.3–0.5 Ω for discrete (small-signal or power) MOSFETS

MOSFET circuits at DC

CMOS Logic gates (two stable states correspond to triode and cutoff regions)

NOT (inverter)



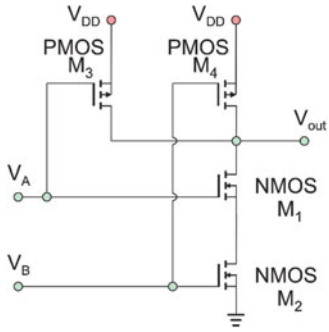
Most basic and most important digital circuit

Inputs	NMOS switch	PMOS switch	Output	r_{OUT}
0	OFF	ON	1	r_{DSp}
1	ON	OFF	0	r_{DSn}

For alternative drawing see Chap. 13

(continued)

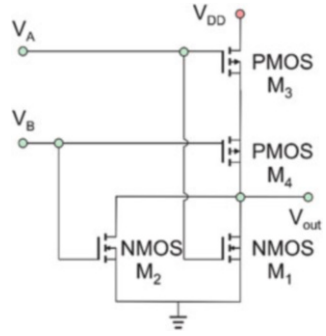
NAND



Inputs		NMOS		PMOS		Out.	r_{OUT}
A	B	M_1	M_2	M_3	M_4		
0	0	OFF	OFF	ON	ON	1	$r_{DS3} \parallel r_{DS4}$
0	1	OFF	ON	ON	OFF	1	r_{DS3}
1	0	ON	OFF	OFF	ON	1	r_{DS4}
1	1	ON	ON	OFF	OFF	0	$r_{DS1} + r_{DS2}$

For alternative drawing see Chap. 13

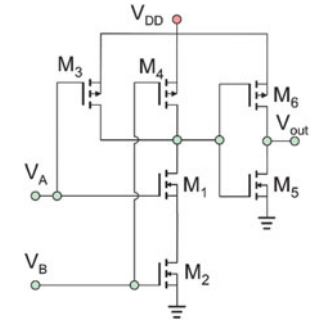
NOR



Inputs		NMOS		PMOS		Out.	r_{OUT}
A	B	M_1	M_2	M_3	M_4		
0	0	OFF	OFF	ON	ON	1	$r_{DS3} + r_{DS4}$
0	1	OFF	ON	ON	OFF	0	r_{DS2}
1	0	ON	OFF	OFF	ON	0	r_{DS1}
1	1	ON	ON	OFF	OFF	0	$r_{DS1} \parallel r_{DS2}$

For alternative drawing see Chap. 13

AND (OR is constructed similarly)



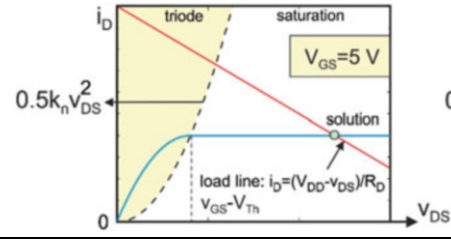
AND = NAND + NOT

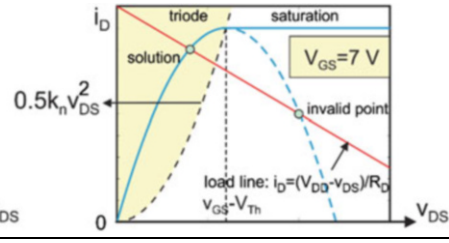
OR = NOR + NOT

Inputs		Output	r_{OUT}
A	B		
0	0	0	r_{DS5}
0	1	0	r_{DS5}
1	0	0	r_{DS5}
1	1	1	r_{DS6}

For alternative drawing see Chap. 15

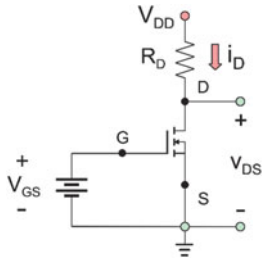
Method of assumed states/Load line method





(continued)

Gate-bias circuit (all three regions are possible)



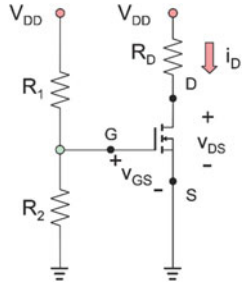
The load line: $i_D = (V_{DD} - v_{DS})/R_D$

If $V_{GS} \le V_{Th}$ then cutoff

If $V_{DD} > \left(1 + \frac{k_n R_D}{2}\right)(V_{GS} - V_{Th})$ then saturation

If $V_{DD} \le \left(1 + \frac{k_n R_D}{2}\right)(V_{GS} - V_{Th})$ then triode

Gate-bias circuit with voltage divider (all three regions are possible)



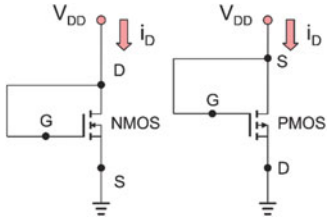
Eliminates the need in the second voltage supply (V_{GS})

Equivalent to the previous circuit when

$$V_{GS} = \frac{R_2}{R_1 + R_2} V_{DD} \text{ or } R_2 = \frac{V_{GS}}{V_{DD} - V_{GS}} R_1$$

May be used as a bias circuit for the amplifier or as a sensor switch when R_1 (or R_2) is variable and R_D is the load (light bulb, motor, etc.)

Diode-connected MOSFETS (current sources, always in saturation or cutoff)



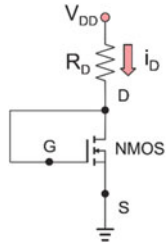
If $V_{DD} \le V_{Th}$, then $i_D = 0$ NMOS

If $V_{DD} > V_{Th}$, then $i_D = \frac{1}{2} k_n (V_{DD} - V_{Th})^2$ NMOS

If $V_{DD} \le |V_{Th}|$, then $i_D = 0$ PMOS

If $V_{DD} > |V_{Th}|$, then $i_D = \frac{1}{2} k_n (V_{DD} - V_{Th})^2$ PMOS

Diode-connected MOSFET with resistance (always in saturation or cutoff)



If $V_{DD} \le V_{Th}$, then $i_D = 0$

If $V_{DD} > V_{Th}$, then

$$i_D = \frac{V_{DD} - V_{Th}}{R_D} + \frac{1 - \sqrt{1 + 2k_n R_D^2 (V_{DD} - V_{Th})}}{k_n R_D^2}$$

Used to estimate threshold voltage:

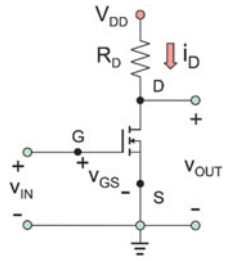
If R_D is sufficiently large (i_D is small) then $V_{Th} \approx v_{GS}$

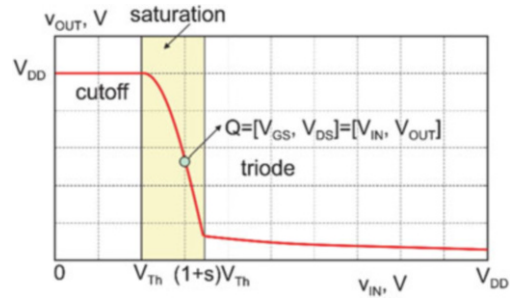
MOSFET common-source amplifier

– Common-source amplifier = small-signal voltage amplifier
– Common-source amplifier is similar to the BJT common-emitter amplifier
– In a MOSFET amplifier, the input resistance can be made infinitely large (or kept finite if necessary)
– An analog of the BJT emitter follower is the MOSFET source follower

(continued)

Voltage transfer function and *Q*-point





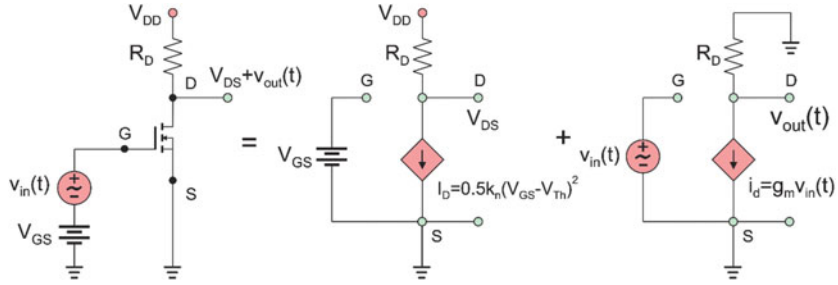
$0 \le v_{IN} \le V_{Th}$ $\quad v_{OUT} = V_{DD}$ $\quad$ cutoff (small v_{IN}, not used)

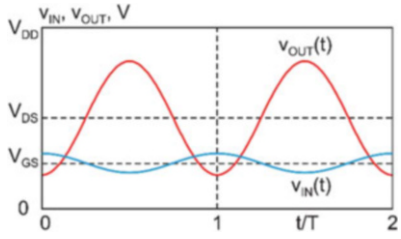
$V_{Th} < v_{IN} \le (1+s)V_{Th}$ $\quad v_{OUT} = V_{DD} - \dfrac{k_n}{2} R_D (v_{IN} - V_{Th})^2$ $\quad$ ***saturation*** $(v_{IN} \ge V_{Th})$

$v_{IN} > (1+s)V_{Th}$ $\quad v_{OUT} << V_{DD}$ $\quad$ triode ($v_{IN} >> V_{Th}$, not used)

$$s = \frac{\sqrt{1+2k_n R_D V_{DD}} - 1}{k_n R_D V_{\text{th}}} > 0, V_{GS} \approx V_{Th} + \sqrt{\frac{V_{DD}}{k_n R_D}}, \quad V_{DS} \approx \frac{1}{2} V_{DD}$$

Amplifier circuit analysis, transconductance, and open-circuit small-signal gain





Transconductance: $g_m = k_n(V_{GS} - V_{Th})$ [A/V]

Small-signal gain: $A_{v0} = -g_m R_D$ [V/V]

Input resistance: $R_{in} = \infty$ [Ω]

Output resistance: $R_{out} = R_D$ [Ω]

Small-signal output: $v_{out}(t) = -A_{0v} v_{in}(t)$

Input with DC bias: $v_{IN}(t) = V_{GS} + v_{in}(t)$

Output with DC bias: $v_{OUT}(t) = V_{DS} - A_{0v} v_{in}(t)$

Problems

18.1 Principle of Operation and Threshold Voltage

18.1.1 Physical Structure: Terminal Voltages and Currents

18.1.2 Simplified Principle of Operation

Problem 18.1. What do the abbreviations FET, MOSFET, and CMOS stand for?

Problem 18.2. Draw circuit symbols of:

A. Four-terminal symmetric NMOS transistor
B. Three-terminal asymmetric NMOS transistor with the body tied to the source and
C. The same but simplified symbol

For B and C, label transistor currents and transistor voltages.

Problem 18.3. Repeat the previous problem for the PMOS transistor.

Problem 18.4. An NMOS transistor has

A. The gate-drain voltage of −2 V and gate-source voltage of 1 V
B. The source current of 1 mA

What is the drain-source voltage? What is the drain current?

Problem 18.5. Repeat the previous problem for the PMOS transistor.

18.1.3 NMOS Capacitor

18.1.4 Voltage Across the Oxide Layer

18.1.5 Voltage Across the Semiconductor Body

18.1.6 Threshold Voltage

18.1.7 PMOS Transistor

18.1.8 Oxide Thicknesses and Capacitances in CMOS Processes

Problem 18.6. Given the semiconductor surface potential $\phi_S = 2$ V and the uniform acceptor concentration 5×10^{16} cm^{-3} for the p-body of the NMOS transistor, estimate the voltage across the SiO_2 oxide layer with the thickness of 10 nm. The NMOS body is Si.

Problem 18.7. Repeat the previous problem when the NMOS body is GaAs and the insulating layer is Al_2O_3.

Problem 18.8. Estimate surface voltage of the semiconductor body at the onset of strong channel inversion at room temperature of 25 °C given $N_A = 5 \times 10^{17}$ cm^{-3}. The NMOS body is Si.

Problem 18.9. Repeat the previous problem when the body material is GaAs.

Problem 18.10. Estimate threshold voltage V_{Th} for a Si NMOS transistor with n+ polysilicon gate, $N_A = 2 \times 10^{16}$ cm^{-3}, and the SiO_2 oxide layer with the thickness of 20 nm at room temperature of 25 °C.

Problem 18.11. Repeat the previous problem for an aluminum gate.

Problem 18.12. Repeat Problem 18.10 for the PMOS transistor with the n-doped body of the same doping concentration.

Problem 18.13. Estimate threshold voltage V_{Th} for Si NMOS transistors used in analog ICs and fabricated in four CMOS processes listed in Table 18.1. Every transistor has the n+ polysilicon gate and the SiO_2 oxide layer. The corresponding doping concentrations are $N_A = [3.5,\ 4.5,\ 7.5,\ 10.5] \times 10^{16}$ cm^{-3}.

Keep at least two significant digits. Compare your solutions with the typical values reported elsewhere: $V_{Th} = [0.7,\ 0.5,\ 0.5,\ 0.4]$ V. Assume room temperature of 25 °C.

18.2 Theoretical Model of a MOSFET

18.2.1 Test Circuit and Operating Regions

18.2.2 Linear Subregion of Triode region at Strong Inversion

Problem 18.14

A. Draw the schematic test circuit for the NMOS transistor. Label transistor terminals. When the gate-source bias voltage

is 0 V, which region of operation is encountered?

B. Repeat the same tasks for the PMOS transistor.

Problem 18.15. Determine the total charge (show units) stored in the inversion layer of the MOSFET transistor with $L = 0.8$ μm, $W = 16$ μm, $C_{OX} = 2.3$ fF/μm^2. The overdrive voltage is 2 V; the drain-source voltage is 0 V. How many electrons are stored in the inversion layer?

Problem 18.16. For a CMOS process of MOSFET fabrication, $L = 0.8$ μm, and $W = 16$ μm. Furthermore, the electron surface mobility is $\mu_n = 550$ cm^2/V · s and the oxide capacitance is $C_{OX} = 2.3$ fF/μm^2. Determine the MOSFET transconductance parameter and show units.

Problem 18.17. An NMOS transistor in the linear subregion of the triode region operates at $v_{OV} = 4$ V. Given $r_{DS} = 100$ Ω determine the lumped process parameter k_n' and show units.

Problem 18.18

A. Determine the MOSFET transconductance parameter (show units) for NMOS transistors used in analog ICs and fabricated in four CMOS processes listed in Table 18.5. Use the given channel length and the channel width ten times greater than the length.

B. Determine turn-on resistances r_{DS} in every case given that the overdrive voltage is equal to the threshold voltage.

Problem 18.19. Repeat the previous problem for the PMOS transistor with parameters listed in Table 18.5. The corresponding resistance is given by $r_{DS} = \frac{1}{k_p(v_{SG} - |V_{Th}|)}$, $v_{OV} = v_{SG} - |V_{Th}|$.

18.2.3 Nonlinear Subregion of Triode Region at Strong Inversion

18.2.4 Saturation Region

Problem 18.20. To avoid complications caused by a nonlinear channel voltage and inversion charge behavior, it is suggested to simplify Eq. (18.18). Namely, the inversion layer of the MOSFET at nonzero drain-source voltages would be described by a straightforward linear voltage dependence $v_{GS}(x) = v_{GS} - \frac{x}{L} v_{DS}$, $x \in [0, \quad L]$ present in some undergraduate texts. Do you see one critical contradiction of this model?

Problem 18.21. Plot variable gate-source voltage $v_{GS}(X)$ to scale over the interval $X = \frac{x}{L} \in [0, \quad 1]$ given that $V_{Th} = 1$ V, $V_{OV} = 1$ V, and

A. $v_{DS} = 0.1 V_{OV}$.

B. $v_{DS} = 0.5 V_{OV}$.

C. $v_{DS} = 1.0 V_{OV}$.

Use the vertical scale from 1 V to 2 V for every figure.

Problem 18.22. Repeat the previous problem for the normalized charge, $Q_{INV}(X)/Q_{INV}(0)$, of the inversion layer.

Problem 18.23. Show that the solution for the channel voltage profile given by Eq. (18.18e) guarantees the condition of the constant current along the channel.

Problem 18.24. An NMOS transistor has $k_n = 2$ mA/V^2 and $V_{Th} = 0.7$ V. The gate-source voltage is 3 V.

A. At which value of v_{DS} does the transistor enter the saturation?

B. What value of i_D is obtained in saturation?

Problem 18.25. An NMOS transistor has (the 0.25-μm Si CMOS process) $L = 0.25$ μm, $t_{OX} = 6$ nm, $\mu_n = 460$ cm^2/(V · s), and $V_{Th} = 0.5$ V. Given $W = 10$ μm find v_{GS}, which assures the operation in the saturation region with the transistor current of 1 mA.

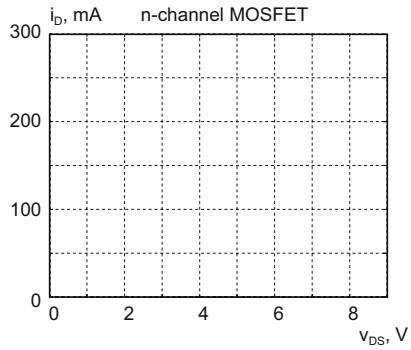
18.2.5 The *v-i* Dependencies

18.2.6 PMOS Transistor

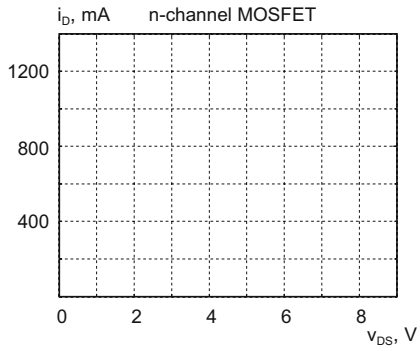
18.2.7 Large-Signal MOSFET Model in Saturation

Problem 18.26. A n-channel power MOSFET has the following parameters: $V_{Th} = 3$ V and $k_n = 100$ mA/V^2.

A. Plot the drain current for source-drain voltages from the interval $v_{DS} = [0-9]$ V and at three values of the gate-source voltage, $v_{GS} = 3,\ 4,$ and 5 V on the same figure.
B. Plot the boundary between the triode region and the saturation region.

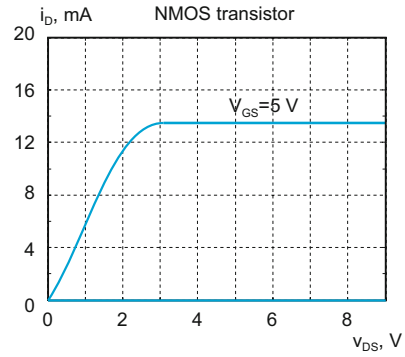


Problem 18.27. Repeat the previous problem for $v_{GS} = 6,\ 7,$ and 8 V.



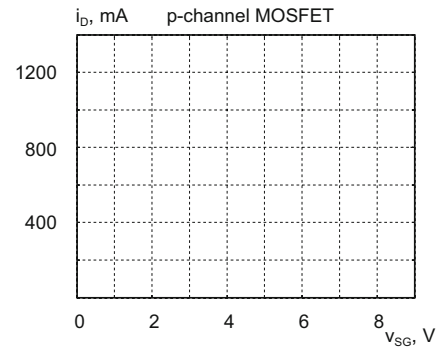
Problem 18.28

A. Based on Table 18.3, construct the similar table for the power dissipated by an NMOS transistor.
B. In the figure that follows, show graphically power dissipated by the transistor at two values of v_{DS}: 2 V and 5 V.
C. Which region, triode or saturation, leads to the smallest power dissipation?



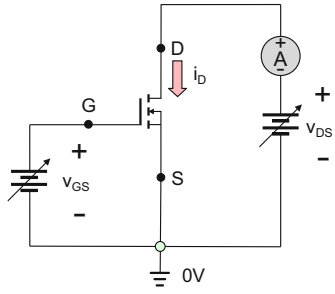
Problem 18.29. A PMOS transistor has the following parameters: $|V_{Th}| = 3$ V and $k_p = 100$ mA/V^2.

A. Plot the drain current for source-drain voltages from the interval $v_{SD} = [0-9]$ V and at three values of the gate-source voltage $v_{GS} = 4,\ 5,$ and 6 V on the same figure.
B. Plot the boundary between the triode region and the saturation region.



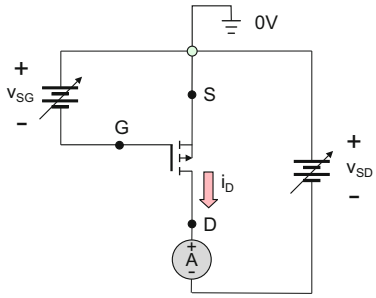
Problem 18.30. For the circuit shown in the figure that follows, determine the region of MOSFET operation as well as the drain current i_D for each set of conditions given. Assume $k_n = 100$ mA/V^2 and $V_{Th} = 3$ V

A. $v_{GS} = -3$ V, $v_{DS} = 3$ V.
B. $v_{GS} = 10$ V, $v_{DS} = 8$ V.
C. $v_{GS} = 5$ V, $v_{DS} = 1$ V.



Problem 18.31. For the circuit shown in the figure that follows, determine the region of MOSFET operation as well as the drain current i_D for each set of conditions given. Assume $k_p = 100$ mA/V^2 and $V_{Th} = -2$ V.

A. $v_{GS} = -3$ V, $v_{DS} = -5$ V.
B. $v_{GS} = 10$ V, $v_{DS} = -8$ V.
C. $v_{GS} = -5$ V, $v_{DS} = -1$ V.



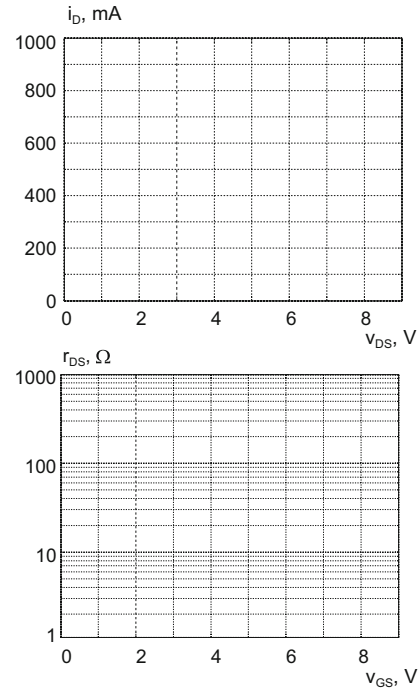
18.3 MOSFET Switching and Bias Circuits

18.3.1 Triode Region for Switching Circuits. Device Parameter Extraction

18.3.2 Resistor-Switch Model in Triode Region

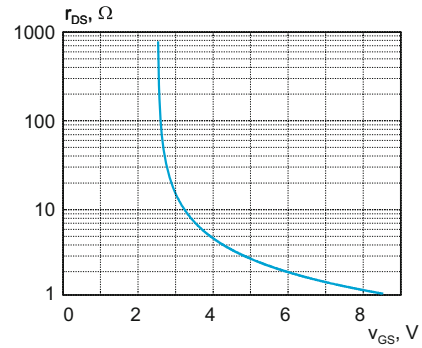
Problem 18.32. A power MOSFET has the lumped process parameter $k_n = 130$ mA/V^2 and the threshold voltage of 2.0 V.

A. Plot the drain current for drain-source voltages from the interval $v_{DS} = [0-9]$ V to scale and determine MOSFET turn-on resistance r_{DS} given the gate-source voltage of 5 V.
B. Plot the boundary between the triode region and the saturation region and indicate the slope $1/r_{DS}$ in the figure.
C. Plot r_{DS} as a function of v_{GS} to scale.

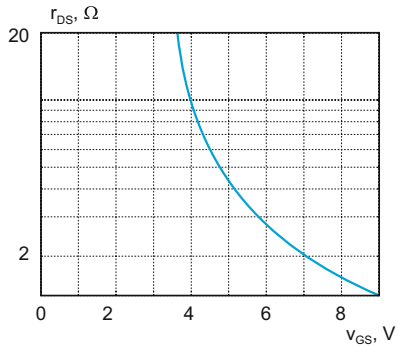


Problem 18.33. Repeat the previous problem when the threshold voltage changes to 3 V.

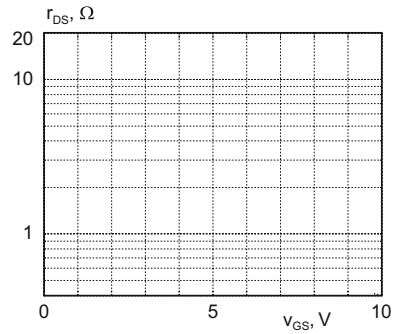
Problem 18.34. A measurement curve for a certain NMOS transistor is shown in the figure below. Approximately determine the threshold voltage V_{Th} and the (MOSFET) lumped process parameter k_n (show units).



Problem 18.35. Repeat the previous problem for the measurement curve shown in the figure that follows.

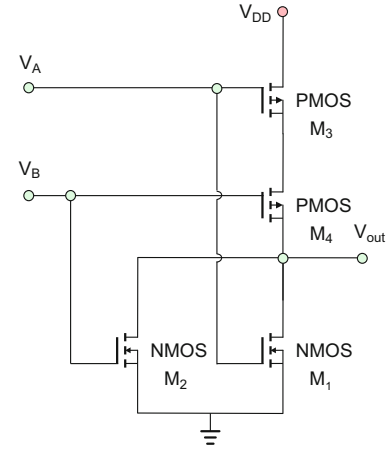


Problem 18.36. The datasheet for an IRF510 enhanced-mode n-channel power MOSFET from Fairchild reports the average drain-source *on-state* resistance $r_{DS} = v_{DS}/i_D = 0.4\ \Omega$ for $i_D = 3.4\,\text{A}$ and $v_{GS} = 10\,\text{V}$. Assuming threshold voltage to be 2.0 V, sketch r_{DS} as a function of v_{GS} to scale.

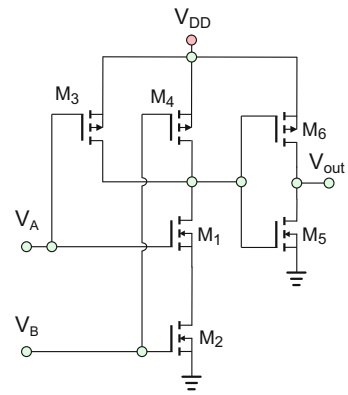


18.3.3 Application Example: Output Resistance of Digital Logic Gates

Problem 18.37. For a logic gate shown in the figure that follows, construct the truth table in the form of Table 18.7 and determine the output gate resistance for *every* input voltage combination. Assume $V_{DD} > V_{Th}$ for the NMOS transistor and $V_{DD} > |V_{Th}|$ for the PMOS transistor. Label turn-on resistances of $M_{1,2,3,4}$ as $r_{DS1,2,3,4}$.



Problem 18.38. For a logic gate shown in the figure that follows, construct the truth table in the form of Table 18.7 and determine the output gate resistance for *every* input voltage combination. Assume $V_{DD} > V_{Th}$ for the NMOS transistor and $V_{DD} > |V_{Th}|$ for the PMOS transistor. Label turn-on resistances of $M_{1,2,3,4,5,6}$ as $r_{DS1,2,3,4,5,6}$.



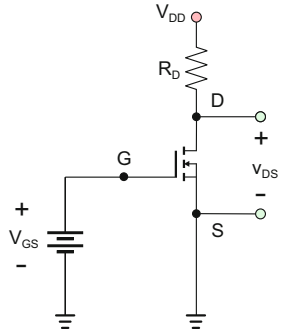
18.3.4 MOSFET Circuit Analysis at DC

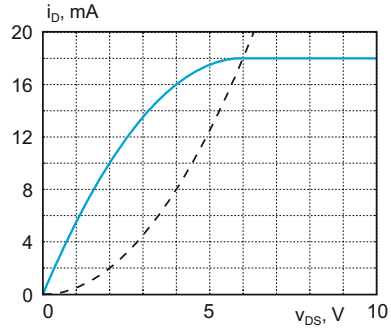
18.3.5 Application Example: Basic MOSFET Actuator

Problem 18.39. In a fixed-gate NMOS transistor circuit, the NMOS transistor has the lumped process parameter $k_n = 1.0\ \text{mA/V}^2$ and the threshold voltage of 1.0 V. Furthermore, $V_{GS} = 7\ \text{V}$, $V_{DD} = 10\ \text{V}$, and $R_D = 1\ \text{k}\Omega$.

The corresponding $v_{DS} - i_D$ curve is shown in the figure that follows.

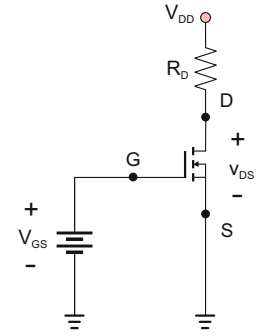
A. Draw the load line in the same figure and find the solution for the drain-source voltage v_{DS} and drain current i_D.
B. Solve the same problem exactly and compare the two answers.





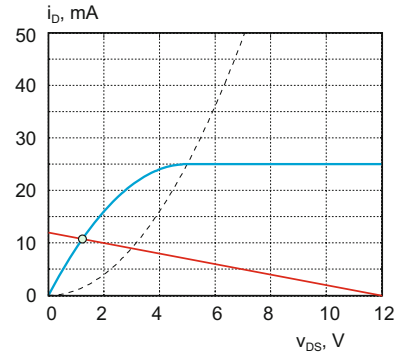
Problem 18.40. In a fixed-gate NMOS transistor circuit shown in the figure that follows, the NMOS transistor has the lumped process parameter $k_n = 1.0$ mA/V^2 and the threshold voltage of 1.0 V. Furthermore, $V_{DD} = 15$ V, and $R_D = 1$ kΩ. Determine the region of operation of the transistor and find the solution for the drain-source voltage v_{DS} and drain current i_D when

A. $V_{GS} = 1$ V.
B. $V_{GS} = 3$ V.
C. $V_{GS} = 5$ V.
D. $V_{GS} = 7$ V.

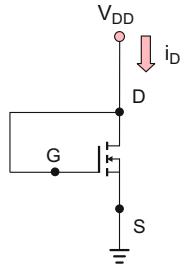


Problem 18.41. A solution for an unknown fixed-gate circuit shown in the previous problem is given in the figure that follows. Restore the transistor and circuit parameters (show units):

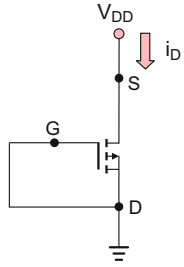
A. V_{DD}
B. $V_{GS} - V_{Th}$
C. R_D
D. k_n



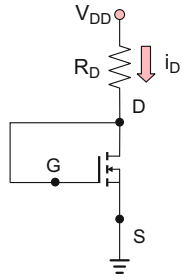
Problem 18.42. In the circuit shown in the figure that follows, the NMOS transistor has the lumped process parameter k_n and the threshold voltage V_{Th}. Derive the analytical expression for the drain current i_D as a function of V_{DD} valid for any values of V_{DD}.



Problem 18.43. In the circuit shown in the figure that follows, the PMOS transistor has the lumped process parameter k_p and the threshold voltage $V_{Th} < 0$. Derive the analytical expression for the drain current i_D as a function of V_{DD} valid for any values of V_{DD}.



Problem 18.44. In the circuit shown in the figure that follows, the NMOS transistor has the lumped process parameter k_n and the threshold voltage V_{Th}. Derive an analytical expression for the drain current i_D as a function of V_{DD} and R_D valid for any values of V_{DD}, R_D.

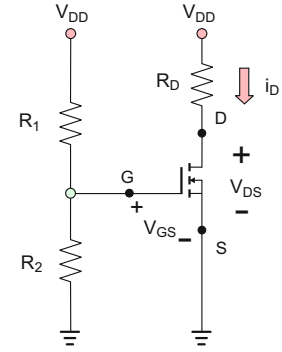


Problem 18.45. In the circuit shown in the figure to the previous problem, a sufficiently large resistance R_D has been chosen so that the drain current is very small. Measured υ_{DS} is 2.5 V. What is approximately the threshold voltage V_{Th} of the transistor?

Problem 18.46. In a fixed-gate NMOS transistor circuit shown in the figure, the NMOS transistor has the lumped process parameter $k_n = 100\ \text{mA/V}^2$ and the threshold voltage of 2.0 V. Furthermore, $V_{DD} = 20$ V, $R_2 = 1\ \text{k}\Omega$, and $R_D = 40\ \text{k}\Omega$. Determine υ_{GS}, the region of operation of the transistor, and the solution for the drain-source voltage υ_{DS} and drain current i_D when

A. $R_1 = 9\ \text{k}\Omega$.
B. $R_1 = 4\ \text{k}\Omega$.
C. $R_1 = 2.33\ \text{k}\Omega$.
D. $R_1 = 1.5\ \text{k}\Omega$.

At which value of the resistance R_1 is the load power (power into R_D) maximized?
At which value of the resistance R_1 is the MOSFET power loss minimized?



Problem 18.47. Repeat the previous problem when the lumped process parameter changes to $200\ \text{mA/V}^2$.

18.4 MOSFET Amplifier

18.4.1 MOSFET Common-Source Amplifier

18.4.2 Voltage Transfer Characteristic

18.4.3 Principle of Operation and Q-point

18.4.4 MOSFET Biasing for Amplifier Operation

Problem 18.48. In the common-source amplifier circuit in Fig. 18.27, the MOSFET has the lumped process parameter $k_n = 100\ \text{mA/V}^2$

and the threshold voltage of 2 V. The source voltage is $V_{DD} = 20$ V.

A. Identify all values of v_{IN} corresponding to the saturation region when

$R_D = 1$ kΩ.

$R_D = 500$ Ω.

$R_D = 100$ Ω.

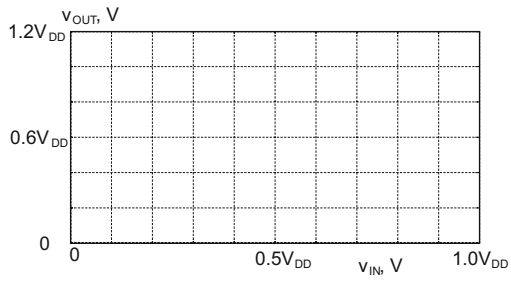
B. Identify the DC Q-point voltage V_{IN} within the saturation region corresponding to $V_{OUT} = V_{DD}/2$ when

$R_D = 1$ kΩ.

$R_D = 500$ Ω.

$R_D = 100$ Ω.

Problem 18.49. Plot to scale the voltage transfer characteristic for the common-source amplifier circuit in Fig. 18.27 built with the general-purpose 2 N7000 NMOS transistor from Fairchild, which has the lumped process parameter $k_n = 90$ mA/V^2 and the threshold voltage of 2.0 V. Indicate the saturation region. The source voltage is $V_{DD} = 10$ V and $R_D = 90$ Ω. Assume that the output voltage is constant in the triode region for simplicity.



18.4.5 Small-Signal MOSFET Model and Superposition

18.4.6 MOSFET Transconductance

18.4.7 Analysis of Common-Source MOSFET Amplifier

Problem 18.50. In a common-source MOSFET amplifier in Fig. 18.30a, the transistor has $k_n = 100$ mA/V^2 and $V_{Th} = 3$ V. Furthermore, $V_{DD} = 20$ V. For

A. $R_D = 5$ kΩ
B. $R_D = 1$ kΩ
C. $R_D = 100$ Ω

design the amplifier by performing the following steps:

1. Identify all values of V_{GS} corresponding to the Q-point in the saturation region.
2. Determine V_{GS} which assures that the Q-point (the DC operating point) is in saturation region and there is enough dynamic range for the output voltage to swing in both a positive and negative direction, i.e., $V_{DS} = V_{DD}/2$.
3. Determine the transistor's transconductance at the Q-point.
4. Determine the open-circuit small-signal voltage gain A_{v0} of the amplifier.

Problem 18.51

A. Repeat the previous problem when $R_D = 120$ Ω.
B. Plot input and output voltages $v_{IN}(t) = V_{GS} + v_{in}(t)$, $v_{OUT}(t) = V_{DS} + v_{out}(t)$ to scale over two periods given that $v_{in}(t) = 0.1 \cos(\omega t)$ [V].

Problem 18.52

A. Repeat Problem 18.50 when $R_D = 120$ Ω and $V_{DD} = 10$ V.
B. Plot input and output voltages $v_{IN}(t) = V_{GS} + v_{in}(t)$, $v_{OUT}(t) = V_{DS} + v_{out}(t)$ to scale over two periods given that $v_{in}(t) = 0.2 \cos(\omega t)$ [V].