Chapter 8 Conditioning Circuits for Capacitive Energy Harvesters

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8.1 Introduction

8.1.1 Generalities

Any sensor converting a physical quantity into electricity needs a minimal electrical conditioning: an appropriate biasing, a readout circuit with an optimal input impedance, etc. However, in many cases, the conditioning is more complex: for example resonant sensors need electrical oscillating circuits, zero displacement accelerometers require PWM or Sigma-Delta modulating feedback loops, etc. The capacitive transducer, being itself a passive device, requires a sophisticated electrical conditioning for electromechanical energy conversion. As was pointed out in Chap. 4, the primary goal of the conditioning is an implementation of a cyclic charge flow synchronized with the variation of the transducer capacitance. Different aspects of practical conditioning circuits are discussed in this chapter.

In Chap. 4, it was shown that the two equations linking the electrical and mechanical quantities (4.2) and (4.13) of an electrostatic transducer are nonlinear. It was also emphasized that an ideal scenario of the electromechanical energy conversion corresponding to a constant voltage QV cycle is implemented by a time variant, i.e., reconfigurable electrical network. As a consequence, a capacitive harvester as a whole can be seen as a nonlinear system. More sophisticated conditioning circuits, e.g., those implementing a rectangular QV cycle based on charge pumps using diodes, are generally nonlinear as well.

In this chapter, we propose a short review of conditioning circuits used for energy conversion with capacitive transducers.

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8.1.2 Classification of Conditioning Circuits for Capacitive Harvesters

As it was shown in Chap. 4, a capacitive transducer needs a dynamic biasing in order to generate electricity. For a capacitive transducer whose capacitance varies periodically following a time law $C_t(t)$, the energy conversion process is completely defined by the charge-voltage cycle Γ . Since the voltage, charge and capacitance of the transducer are bounded by the equation $Q_t = C_t V_t$, if $C_t(t)$ is defined, the energy conversion is defined by the voltage waveform applied to the transducer. A conditioning circuit for an electrostatic transducer can be seen as an electrical dipole, which is connected to the electrical terminals of the transducer, as presented in Fig. 1.3.

Since the past two decades, several architectures of conditioning circuits for eVEHs (electrostatic Vibration Energy Harvesters) were invented. We propose a classification of the conditioning circuits on the basis of the shape of the achieved charge-voltage cycles. Figure 8.1 presents all known basic QV cycles plotted in the same axes, under hypothesis that the maximum voltage V_t applied to the variable capacitor is the same for all cycles (V_{max}). We chose such a basis for the comparison, because in practice, any technology of electronic circuits always impose a maximum allowed voltage. We distinguish three families of conditioning circuits implementing three types of QV cycles



Fig. 8.1 Diagram showing all charge-voltage cycles which have been used to date for conditioning of capacitive transducers in VEHs: OCB (constant-charge), OAB (constant-voltage), DFBE (*rec*-tangular) and "tear drop" cycle corresponding to the continuous conditioning circuit or VEH with electret layer. All cycles are drawn for the same extreme values of the variable capacitance (C_{min} and C_{max}) and for the same maximum voltage V_{max}

- 1. Teardrop, oval, or egg-shaped QV cycle (an example is plotted with dotted lines)
- 2. Triangular QV cycle (OAB, OCB)
- 3. Rectangular QV cycle (DFBE)

In this chapter, we present practical topologies of conditioning circuits implementing these QV cycles.

8.1.3 Frame of the Analysis of Conditioning Circuit

The conditioning circuits are usually studied in electrical domain. It means, that the variation of the transducer capacitance is supposed to be defined and fully characterized by a function of time $C_t(t)$. A usual hypothesis is $C_t(t)$ is periodic with period T_e^{-1} and having only one local maximum and minimum (C_{max} and C_{min}) over a period. This is only a working hypothesis allowing to limit the complexity of the analysis. In reality, because of the electromechanical coupling, $C_t(t)$ depends also on the electrical operation of the conditioning circuit, as it will be shown in examples in Sect. 8.7. However, assuming a predetermined $C_t(t)$ is a necessary step in the study of the harvester as a whole.

In Sect. 8.7, we discuss how the presence of a transducer coupled with a mechanical resonator impacts the operation of the circuit.

8.2 Continuous Conditioning Circuit

The simplest conditioning circuit demonstrating a generation of electrical power out of variation of a capacitance is called "continuous conditioning circuit." Its topology is presented in Fig. 8.2. The circuit is composed of the variable capacitor C_t (the transducer), a resistive load R_L and an initially charged large reservoir capacitor C_{res} , or simply a DC voltage source, when only a laboratory test is aimed. The name of the circuit comes from the fact that all voltages and currents of the circuit are continuous functions of time; this is not the case of more sophisticated circuits which use switches or diodes and which will be considered later in this chapter.

The continuous conditioning circuit presented in Fig. 8.2 was first discussed in [17, 24]. It was proposed as an electric interface between a resistive load and the capacitive transducer provided with an electret layer [24], and later it was used with a passive capacitive transducer [1, 17] biased by a voltage source or by a fixed pre-charged capacitor. In spite of different nature of the transducer devices, these configurations are equivalent: a DC voltage source in series with a passive capacitive transducer is exactly an electrical model of a transducer biased by an electret layer

¹The index "e" in T_e stands for "electrical." This is to emphasize that the variation of C_1 may have a different frequency that the mechanical vibrations, cf. [1].



Fig. 8.2 Schematic of continuous conditioning circuit. In this study the continuous circuit represents all circuit configurations which employ a capacitive transducer, resistive load and some internal or external voltage to provide the initial bias on the transducer

[24]. Without major impact on prediction capability of the model, the DC voltage source may be replaced by a large pre-charged capacitor.

Because of the simplicity of its implementation, this circuit is often used in laboratory tests and characterization of capacitive transducers intended for the energy conversion. In this section we propose a brief analysis of this circuit and its main shortcomings.

8.2.1 Qualitative Discussion on Operation of the Circuit

In this subsection, we explain briefly the circuit operation on the example of a circuit where the biasing is provided by a large fixed capacitor C_{res} initially charged to a voltage V_0 , other capacitors are initially discharged and where the transducer capacitance varies according to some known periodic time law $C_t(t)$ (Fig. 8.2a). We first consider the circuit operation in an extreme case, when R_L is close to zero [1]. It can be seen that as the transducer capacitance varies, there is a charge redistribution among C_t and C_{res} , which corresponds to a current i(t) equal to

$$i(t) = V_0 \frac{\mathrm{d}C_t}{\mathrm{d}t} \tag{8.1}$$

This equation is valid if we can neglect the voltage on R_L comparing to V_0 : that is, indeed the case if $R_L \approx 0$. It can be seen that this current dissipates power on R_L , whose instantaneous value is equal to

$$P_{RL} = i^2(t)R_L. \tag{8.2}$$

After each period of variation of $C_t(t)$, the circuit returns to the same electrical state, since the total electrical charge of C_t and C_{res} is constant, so is their total energy. One should conclude that the energy dissipated on the resistance comes from the conversion of energy from mechanical to electrical domain.

The power P_{RL} is proportional to the load resistance: it increases as R_L increases. However, for large R_L , the voltage on R_L cannot be neglected anymore, and the Eq. (8.1) is not valid.

We consider now the opposite extreme value of the load resistance: very large (infinite). If the power on the load resistance is expressed through the voltage on the load resistance V_L as

$$P_{RL} = V_L^2(t) / R_L, (8.3)$$

we can show that the power tends to zero as $R_L \to \infty$. To prove this, it is enough to show that V_L has an upper bound. Indeed, since the current tends toward zero, the transducer keeps its charge constant. The value of this charge depends on the initial condition. Let it be Q_0 , in this case the voltage on C_t is $Q_0/C_t(t)$, and the absolute value of voltage on the resistor is equal to $|V_0 - Q_0/C_t(t)|$. Evidently, if $C_{min} > 0$, this time function has an upper bound.

So, at zero and infinity values of the load resistance, the power is zero, but not for finite values of R_L . Hence, one should conclude that there is an optimal value of the load resistance, for which the converted power is maximum.

In the next two subsections, we propose a more detailed analysis of the circuit.

8.2.2 Analytical Model in the Electrical Domain

This section presents the mathematical model describing formally the operation of the conditioning circuit.

The governing equations describing the electrical behavior of the simple conditioning circuit are given by the Kirchhoff voltage law and the element equations:

$$R_{\rm L}\frac{dQ_t}{dt} + \frac{Q_t}{C_t(t)} = V_0, \qquad (8.4)$$

where Q_t is the instantaneous charge on the transducer capacitor, $C_t(t)$ is the time evolution law of the transducer's capacitance. The electrical equation of the transducer is simply

$$V_t(t) = Q_t(t)/C_t(t),$$
 (8.5)

where V_t is the voltage on the transducer.

The instantaneous power converted by the transducer is dissipated on the load resistance, and can easily be calculated with Eq. (8.2), where the current is given as

$$i = \frac{\mathrm{d}Q_t}{\mathrm{d}t} \tag{8.6}$$

The average power converted by the transducer is given by the average of (8.2) on one period of $C_t(t)$ variation.

In order to calculate the average converted power, the closed expression of $Q_t(t)$ should be found, and for that the differential Eq. 8.4 should be solved. The work [12] addressed the resolution of this equation. It was concluded that even for simple geometries of the transducer, this equation cannot be solved in closed form, and the analytical solution for $Q_t(t)$ can be expressed as infinite Fourier series, in which, however, the terms above third or forth can be neglected in the most practical cases. The coefficients of the series are expressed through Bessel functions. For this reason, a comprehensive analytical expression relating the converted power to the parameters of the system is difficult to establish.

We present here an example of practical study of the continuous conditioning circuit in the electrical domain. For that, we need to define the function defining the variation of the transducer capacitance over time, $C_t(t)$. In this example, we study the case of a gap closing transducer (see Chap. 4) whose mobile plane moves according to a sinusoidal law. We have:

$$C_t(t) = C_t(x(t)) = \varepsilon_0 \frac{S}{d_0 - x(t)} = \varepsilon_0 \frac{S}{d_0 - X_0 \sin \omega t},$$
(8.7)

where *S* and d_0 are the overlapping area and the initial transducer gap, respectively, X_0 and ω are the amplitude and the angular velocity of mobile electrode motion.

This function is submitted to Eq. (8.4). The steady-state solution of the linear parametric equation (8.4) describes a periodic variation of the charge $Q_t(t)$ and of the current $\dot{Q}_t(t)$. The solution can be obtained by any tool for EDT solving, or by a Spice simulator able to model a variable capacitance. Here, we present the result of numerical resolution of the equation for the values of the parameters presented in Table 8.1.

 Table 8.1
 Values of parameters used for simulation of continuous conditioning circuit with gap closing capacitive transducer

Physical parameters						
	Fixed parameters				Variable parameters	
Parameter name	<i>d</i> (m)	<i>S</i> (m ²)	ω (rad · s ⁻¹)	<i>V</i> ₀ (V)	<i>X</i> ₀ (m)	$R_L(\Omega)$
Parameter value	50×10^{-6}	1×10^{-4}	$2 \cdot \pi \cdot 100$	10	$(30, 40, 45) \times 10^{-6}$	$(1100) \times 10^{6}$



Figure 8.3 presents the plot relating the average power generated on the load resistance in the steady-state mode (after the transient process) to the value of the load resistance. The plot is given for three amplitudes of the mobile mass vibrations. It can be seen that the curves are similar to what is obtained for the power-load characteristic of a real voltage source having some internal resistance R_s . In this case, the power is maximum when the load resistance is equal to the internal resistance of the source. This allows us to consider the load resistance value at which the power on the plot of Fig. 8.3 is at its maximum as the equivalent internal resistance of the power source represented by the transducer and the biasing source. Note, that the internal resistance of such a source depends on the amplitude of the mobile electrode motion, as shows the plot. This highlights nonlinearity of the system: indeed, in a linear system, the impedance matching condition for the load does not depend on the amplitude of the input signal.

Figure 8.4 presents three families of QV cycles in steady-state mode (after the end of the transient process), corresponding to three different amplitudes of the mass displacement X_0 . Each plot contains several QV cycles obtained for different values of the load resistance. The QV cycles drawn with a thick plain line correspond to the values of the load resistance at which the converted power is maximum (cf. Fig. 8.3): this QV cycle has the largest area over all cycles of the family.

Let us have a look on the evolution in the shape of the QV cycle as the load resistance increases. For low R_L , the QV cycles are more "vertical," and as $R_L \rightarrow 0$, the cycle is degenerated to a vertical line (meaning that there is no voltage across the load resistance). On the contrary, for large R_L , the QV cycle is more horizontal, and in the limit case when $R_L \rightarrow \infty$, the QV cycle is a horizontal line (meaning that there is no current flowing through the load resistance). For these two extreme cases, the energy converted by a cycle is zero (cf. discussion in Sect. 8.2.1). The QV cycle has a "tear-drop" shape, which, as we discussed before, can not be expressed by any analytical function written in closed form.



Fig. 8.4 Three families of QV cycles corresponding to steady-state operation of the continuous conditioning circuit used with a gap closing transducer, each family is plotted for a value of the amplitude of mobile electrode motion. The QV cycles on each plot correspond to different load resistances. The optimal QV cycle (those maximizing the converted power and hence having a maximum area) is plotted with *thick solid line*

The plots of Fig. 8.5 presents the time evolution of the transducer capacitance, the transducer voltage and current at the configuration where $X_0 = 45 \,\mu\text{m}$, $R_L = 10 \,\text{M}\Omega$. The transient process lasting for less than one period is observable on these plots. The nonlinear nature of the system can clearly be seen from these curves.

Shortcomings of the Continuous Conditioning Circuit. Auto-Increasing of the Biasing

The main advantage of the continuous conditioning circuit is its simplicity of implementation. Unfortunately, the drawbacks are numerous, and this is the main motivation for study of alternative but more complex solutions. In this conclusion, we summarize the drawbacks of this conditioning circuit.



- The voltage on the load resistance is AC; it can be seen from the current flowing through the transducer in Fig. 8.5. An AC–DC conversion is required; in the case of the electret transducer this may be done by conventional rectifying networks [20].
- The order of magnitude of the voltage on the load and the bias voltage may be the same. In the case of the electret layer, the bias voltage may be of several tens of volts, and a downscale of the voltage is necessary. This is related to generally very large internal impedance (resistance) of the energy source provided by the continuous conditioning circuit (cf. discussion in Sect. 8.2.2). An active impedance matching is required in order to optimally supply an eventually low impedance load.
- However, the main shortcoming of the continuous conditioning circuit is in the case when the available bias voltage is, for some reasons, low. Practical studies highlight that up to tens of volts of bias may be needed for optimal operation [1]. However, the initial charge can only be obtained by a low voltage battery existing in the system, or by a complementary piezoelectric VEH as proposed in [11] (or maybe, by a solar cell), and the generated initial voltage will be not greater than few volts. A low bias voltage means a low output power, since the latter is proportional to the square of the voltage. A similar problem is when the electret layer is weakly biased, for example, because of the depolarization due to the aging.





• If the bias voltage is generated by a large pre-charged capacitor, the leakage reduces its charges with time, and the circuit becomes inactive. Similar problems have been reported with electret layers, which tend to depolarize with time.

The last two points are related to the impossibility of the continuous conditioning circuit to accumulate the energy converted from the mechanical domain, in order to increase its biasing. One of the possible functional diagrams required for a conditioning circuit is presented in Fig. 8.6: there should be a mechanism allowing a generation of a high voltage by using the energy converted from the mechanical domain. This voltage should then be used for biasing of the transducer. Since the biasing does not consume energy (under hypothesis of low leakage of capacitors), the circuit will be able to operate at high biasing, while the start-up may be done from a low voltage. Obviously, at the initial stage, the energy converted from the mechanical domain should be used for generation of the high voltage biasing, and only after the biasing is established, the converted energy can be provided to the load with a high power due to a high voltage biasing. We call the mode in which the conditioning circuit accumulate its energy in order to increase its biasing "the auto-accumulative" or "self-increasing" mode.

The circuits presented in the next sections are free from the drawback of the continuous conditioning circuit, and all provide the possibility to accumulate the converted energy on a storage capacitor, which then can be used for the load supply.

8.3 Conditioning Circuits Implementing Triangular QV Cycles

Two triangular QV cycles are known for conditioning of capacitive transducers in energy converters: a constant voltage QV cycle (OAB in Fig. 8.1), and a constant charge QV cycle (OCB in Fig. 8.1). The two cycles have a very important common property: a discontinuity in time of the voltage on the variable capacitors. It can be obvious from their QV diagrams: the latter include paths on segments corresponding to a fixed value of the transducer capacitances (the lines OA, OC, and OB). Since the transducer capacitance varies in a continuous way (for instance, following the law

given by (8.7)), these lines correspond to instantaneous, and hence, discontinuous variation of the charge and of the voltage. That is physically impossible; in practice, an implementation of such an operation supposes a *fast* variation of the transducer voltage, in comparison with the evolution speed of $C_t(t)$. It can be shown that only inductive DC–DC conversion allows a very fast voltage change on a capacitor without substantial loss of energy. As a consequence, conditioning circuits implementing triangular QV cycles need inductive DC–DC conversion stages synchronized with the variation of the variable capacitance.

8.3.1 Constant Voltage Conditioning Circuit

The constant voltage QV cycle was discussed in Sect. 4.1.5. We showed that the constant voltage QV cycle provides the best energy yield achievable with a given transducer having a given dynamics, supporting a given maximum voltage.

In this subsection, we propose a discussion about how to implement practically a circuit achieving a constant voltage QV cycle on a capacitive transducer. We high-light fundamental difficulties of implementation, and explain the reasons of very limited use of the constant voltage scenario and as a consequence, the motivation for exploring alternative suboptimal solutions.

We summarize the scenario corresponding to the constant voltage QV cycle, and propose a corresponding electrical network (Fig. 8.7). We suppose that a voltage source V_{max} is available. This can be a large fixed capacitance pre-charged to this voltage. At the beginning of the cycle, C_t is discharged, SW is OFF.

(1) When C_t is at its maximum, the transducer is pre-charged to a voltage V_{max} and immediately after that the transducer is connected to the source of voltage V_{max} . Note that the transducer cannot be directly connected to the voltage source, if their voltages are not equal. The only way to avoid losses when charging C_t from 0 to V_{max} is to use an inductive DC–DC converter. This conversion is denoted "Conversion 1" in Fig. 8.7



- (2) When C_t decreases from C_{max} to C_{min} , the transducer is connected to the voltage source (SW is ON). During this time, the voltage source receives charges and energy from C_t . Indeed, the variable capacitor loses charges $\Delta Q = (C_{max} C_{min})V_{max}$, and the source receives the energy $\Delta Q V_{max}$.
- (3) When C_t is at its minimum, the switch becomes OFF, the remaining charges of C_t are transferred to V_{max} , so that the voltage of C_t is zero. The transfer is achieved by an inductive DC–DC conversion denoted as "Conversion 2."
- (4) Since at each cycle V_{res} receives more energy that it delivers, the average energy of V_{res} increases with time. If the voltage source is implemented as a large capacitor, its voltage increases with time: that is not desirable, since, by initial hypothesis, V_{max} is the maximum voltage allowed in the given technology. The circuit should contain a mechanism removing energy from V_{max} , for example, by supplying a load. Since the load is supplied by a low voltage, an inductive DC–DC converter should be implemented, which is denoted as "Conversion 3."

We note that this operation must be precisely synchronized with the variation of C_t . In this description we do not consider how to implement such a synchronization. Summarizing, an implementation of a constant voltage scenario requires:

- a high voltage source,
- three inductive DC-DC conversions at each cycle,
- a switch connecting the transducer and the V_{max} source,
- precise synchronization of the DC–DC conversions with the variation of C_t .

The challenges of implementation of such a circuit are obvious, especially because of very small available energy for the operation of the control electronics.

An example of a successful implementation of a constant voltage conditioning circuit has been reported in [25], by a research group of Georgia Tech University.

8.3.2 Constant Charge Conditioning Circuits

The constant charge energy conversion scenario is similar to the constant voltage scenario, except when the transducer capacitance decreases, the circuit fixes the charge of the transducer, and not the voltage. The corresponding aspect of QV cycle is given in Fig. 8.1, cycle OCB. The energy converted by the cycle is given by the formula:

$$\Delta W = \frac{1}{2} V_0^2 C_{max} \left(\frac{C_{max}}{C_{min}} - 1 \right) = \frac{1}{2} V_{max}^2 \frac{C_{min}}{C_{max}} (C_{max} - C_{min}).$$
(8.8)

where V_0 is the voltage on C_t when $C_t = C_{max}$.



If one compares this formula with Eq. (4.19), it is evident that at the same V_{max} , C_{max} and C_{min} , the constant charge QV cycle converts C_{max}/C_{min} times less energy than the constant voltage QV cycle. This can also be seen from the plot of Fig. 8.1.

However, a conditioning circuit implementing a constant charge QV cycle is simpler than for a constant voltage QV cycle. A schematic of such a circuit is given in Fig. 8.8. The circuit is composed of a large capacitor C_{res} initially pre-charged to the voltage V_{res} , or of a voltage source generating the same voltage, of an inductor and of two externally controlled switches. The operation scenario is the following:

- when C_t is at its maximum and discharged, an inductive DC–DC converter transfers charges from a reservoir capacitor C_{res} to C_t , so that C_t has a charge Q_0 and a corresponding voltage $V_0 = Q_0 C_{max}$. Note that the initial voltage V_0 is determined by the timing of the DC–DC conversion (namely, by the ON time of the switch SW1), and not by the voltage V_{res} . An appropriate command of the switches SW1 and SW2 is required, as described in [18].
- both switches are off, the transducer capacitance reduces while the charge of the transducer remains constant. The internal electrical energy of *C_t* increases.
- when C_t is at its minimum, the DC-DC converter transfers the charge back from C_t to C_{res} , without energy losses. The capacitor C_{res} receives a greater energy that it initially has given to C_t .
- the transducer capacitance increases while its charge is zero (the switches are off), until it reaches the maximum, and the cycle repeats.

In this way, the conditioning circuit operates as a bidirectional DC–DC converter. Two advantages over the constant voltage circuit should be noted:

- (1) The voltage V_{res} may be a low voltage, easy to generate. Nevertheless, the used DC–DC converter is able to generate a higher initial voltage V_0 on C_t , if it is required for optimal energy conversion by the transducer.
- (2) The voltage V_{res} being low, it is compatible with the requirement of the load supply. In this way, one DC–DC conversion is removed (the Conversion 3 in Fig. 8.7).

A need of a precise synchronization of the DC–DC conversion with the motion of the mobile mass is a strong negative point of the constant-charge conditioning scenario, which makes the implementation of the control electronics complex and energy consuming. Study of practical implementation of this solution can be found in [5, 6, 16, 18].

8.4 Circuits Implementing Rectangular QV Cycles

In this section, we propose to study a class of circuits implementing rectangular QV cycle (DFBE in Fig. 8.1). We present here two subfamilies of such circuits: one based on a charge pump firstly proposed by Roundy et al. [22], and one based on the Bennet's doubler [3]. Other circuits which implement such a QV cycle are full wave and half wave diode rectifiers loaded by a reservoir capacitor. They are used with transducer biased by electret layer [20], and are not discussed in this book.

Priorly, to study the circuit topologies, we propose a discussion on the common properties of these circuits, which are due to the geometry of the implemented QV cycle.

8.4.1 Study of the Rectangular QV Cycle

Let us consider a rectangular QV cycle having the following parameters related to the cycle geometry (Fig. 8.9):

- The extreme voltages of the cycle which we call V_{res} , V_{st} , such as $V_{res} < V_{st}$
- The extreme charges of the cycle which we call Q_1 , Q_2 , such as $Q_1 > Q_2$



• The four values of the transducer capacitance corresponding to four points of the rectangle²:

 $C_{max} = Q_1/V_{res}$ (corresponds to the point D) $C_{min} = Q_2/V_{st}$ (corresponds to the point B) $C^* = Q_1/V_{st}$ (corresponds to the point F) $C^{**} = Q_2/V_{res}$ (corresponds to the point E)

If a capacitive transducer is biased so as to follow the electrical state defined by such a cycle, the energy converted in one cycle is easily calculated as the area of the cycle

$$\Delta W = (V_{st} - V_{res})(Q_1 - Q_2) = V_{res}^2 C_{max} \left(\frac{V_{st}}{V_{res}} - 1\right) \left(1 - \frac{V_{st}/V_{res}}{C_{max}/C_{min}}\right)$$
(8.9)

To have a physical meaning, this quantity must be positive. Hence, it is required that

$$\frac{C_{max}}{C_{min}} \ge \frac{V_{st}}{V_{res}}.$$
(8.10)

The expression ΔW is a quadratic form of the variables V_{res} , V_{st} . As a consequence, if one of these voltages is fixed, there is an optimal value of other voltage maximizing ΔW . Also, if there is some limitation applied on the voltages V_{res} and V_{st} (for instance, a maximum allowed value), there is an optimal ratio V_{res}/V_{st} , which is a function of the C_{max}/C_{min} ratio [13].

How practically a rectangular QV cycle can be implemented? It was said in Chap. 1, that a conditioning circuit can be seen as a dipole (Fig. 1.3). We now propose a discussion on main properties of the dipole implementing a conditioning cycle with a rectangular QV cycle, and we define its current-voltage characteristic.

By analyzing the QV diagram (8.9), it can be seen that when $V_{res} < V_t < V_{st}$, the transducer current is zero (since $Q_t = const$). We conclude, that at this operation stage, the conditioning circuit presents a high impedance (an open circuit).

As the transducer voltage reaches V_{st} when the transducer capacitance decreases (the segment DF), the voltage of the transducer is fixed to V_{st} (the segment FB), i.e., the conditioning circuit presents a voltage source V_{st} . Note that the current of transducer is

$$i_t = \frac{\mathrm{d}Q_t}{\mathrm{d}t} = V_{st} \frac{\mathrm{d}C_t}{\mathrm{d}t} < 0 \tag{8.11}$$

since $C_t(t)$ decreases. As a consequence, the transducer gives its charges (and hence its energy) to the conditioning circuit.

²Each point (V, Q) on a QV diagram defines an unique value of the variable capacitor given by Q/V, otherwise, by the slope of the line connecting the point (V, Q) and the origin.

A similar process happens when the transducer capacitance increases and its voltage reduces to V_{res} (the segment BE), while the capacitance continues to increase. In this case, the conditioning circuit behaves as a voltage source V_{res} (the segment ED). In this case

$$i_t = \frac{\mathrm{d}Q_t}{\mathrm{d}t} = V_{res} \frac{\mathrm{d}C_t}{\mathrm{d}t} > 0 \tag{8.12}$$

since C_t increases, and as a consequence, the transducer takes charges and energy from the conditioning circuit.

We can define the current-voltage characteristic (relating i_t and V_t) of the conditioning circuit as follows:

- if $V_{res} < V_t < V_{st}$, $i_t = 0$; (open circuit)
- if $i_t > 0$, $V_t = V_{res}$; (voltage source V_{res})
- if $i_t < 0$, $V_t = V_{st}$; (voltage source V_{st})

Figure 8.10a presents the plot of the corresponding current-voltage characteristic. It can be seen that such a characteristic corresponds to a voltage limiter implemented by the network given in Fig. 8.10b, often used for the ESD protection of integrated circuits, and known as "voltage limiter." The use of this circuit for implementation of a rectangular QV cycle in capacitive energy harvesters was first proposed by Roundy [22]. In the literature addressing the energy harvesting, this circuit is usually drawn as in Fig. 8.11a, and is called "charge pump." Indeed, as follows from our discussion, when this circuit is connected to a variable capacitor with periodic variation of the



Fig. 8.10 Implementation of an ideal rectangular QV cycle: **a** Current-voltage characteristic of a dipole which, when connected to a variable capacitor, implements a rectangular QV cycle, **b** An electrical network having such a characteristic



Fig. 8.11 Schematic of a charge pump implementing a rectangular QV cycle: **a** ideal charge pump, **b** practical implementation

capacitance, the low voltage source V_{res} gives charges, whereas the high voltage source V_{st} receives charges. In such a way, the circuit creates a charge flow from a low potential (V_{res}) to a high potential (V_{st}). The additional energy necessary for such an operation comes from the mechanical domain, thanks to the variation of the transducer capacitor.

The advantage of this circuit with comparison to a constant voltage or constant charge circuit is obvious: the automatic synchronization of the phases of the biasing with the variation of the transducer capacitance, without any need of external control. However, practical use of the charge pump in capacitive energy harvesters requires to answer the following questions:

- How to generate the voltages V_{res} and V_{st} ,
- How to transfer periodically the energy gained by the source V_{st} to some low voltage storage device (a large capacitor or a battery).

In this section, we consider two families of circuit implementing rectangular QV cycle solving these problems.

8.4.2 Practical Implementation of the Charge Pump

An implementation of the charge pump close to the described idealized circuit is obtained with the network of Fig. 8.11b. The voltage sources are implemented by charged fixed capacitances of large values. The values of C_{res} and C_{st} should be chosen so that

$$C_{max} \ll C_{st} \ll C_{res}. \tag{8.13}$$

 C_{res} capacitor is initially charged to a voltage $V_{res} = V_{res0}$, and so are C_{st} and C_t capacitors, because of the charge sharing through the diodes D1 and D2.



Fig. 8.12 Succession of charge-voltage cycles as the charge pump operates starting from the state when $V_{st} = V_{res}$: the first cycle *DBE*, the subsequent cycles $DF_1B_1E_1, DF_2B_2E_2, \dots, DF_nB_nE_n$. If $n \to \infty$, the cycle is degenerated to a line passing through the points $D, F_1, F_2 \dots F_n$

By initially precharging the circuit to a voltage V_{res0} , we implement the configuration of Fig. 8.11a with $V_{res} = V_{st}$, in which the converted energy per cycle is zero, according to (8.9). However, since the V_{st} voltage source is implemented by a capacitor C_{st} , the charge transfer from C_{res} to C_{st} during the first cycle slightly increases the voltage across C_{st} . Hence, the corresponding QV cycle is actually triangular, as shown in Fig. 8.12, cycle *DBE*. The next cycle starts in a configuration with a slightly larger V_{st} , yielding a trapezoidal QV cycle. After each cycle, V_{st} increases, so that all further cycles are different. It can be shown that the slope of the line DB, F_1B_1, \ldots, F_nB_n is $-C_{st}$ (steeper than C_{max} , but exaggerated in the figure): the shape of the cycles is close to rectangular, as $C_{st} \gg C_{max}$. The QV trajectory follows a succession of cycles, starting from $V_{st} \approx V_{res}$ and asymptotically approaching a degenerated cycle represented by a trapeze with a zero area (a horizontal line) corresponding to the V_{st} voltage given by:

$$V_{st\ sat} = V_{res}C_{max}/C_{min}.$$
(8.14)

This value is called the "saturation voltage" of the charge pump.

As a result of the operation of this circuit, the capacitor C_{st} receives energy from C_{res} , and in addition, it receives energy converted from the mechanical domain (the harvested energy). At every QV cycle of the charge pump operation, the overall electrical energy of the circuit increases. In what follows, we present a quantitative analysis of this process.

The voltage V_{st} at the end of the *n*th cycle evolves following the recursive equation [26]:

$$V_{st\ n} = \alpha V_{st\ n-1} + \beta, \tag{8.15}$$

where

$$\alpha = \frac{C_{st}}{C_{st} + C_{min}}, \text{ and } \beta = V_{res} \frac{C_{max}}{C_{st} + C_{min}}.$$
(8.16)

The solution of the discrete equation (8.15) is

$$V_{st\ n} = \left(V_{st0} - V_{res}\frac{C_{max}}{C_{min}}\right) \left(\frac{C_{st}}{C_{st} + C_{min}}\right)^n + V_{res}\frac{C_{max}}{C_{min}},\tag{8.17}$$

where V_{st0} is the voltage on C_{st} capacitor at the zeroth cycle. In this example, it is assumed $V_{st0} = V_{res0}$.

Note that if C_t variations are periodic, the variable n is the operating time of the charge pump divided by the period of C_t variation, T_e . From (8.17) it can be derived that the asymptotic value of $V_{st n}$ as $n \to \infty$ is $V_{st sat}$ is given by (8.14).

As V_{st} increases, the voltage V_{res} slowly decreases, as the amount of charges on C_{res} and C_{st} is constant (as one neglects the charges on C_t). The evolution of V_n is given by:

$$V_{res n} \approx [\text{if } C_{st} \gg C_{max}] \approx V_{res0} - \frac{C_{st}}{C_{res}} \cdot (V_{st n} - V_{res0}) \approx [\text{if } C_{res} \gg C_{st}] \approx V_{res0}.$$
(8.18)

An example of the evolution of V_{res} and V_{st} is given in Fig. 8.13a, where the charge pump starts from the state $V_{res} = V_{st} = V_t = V_{res0}$. From formula (8.15) and (8.16) it can be seen that if $C_{st} \gg C_{max}$, the increment of V_{st} during every cycle is small, and the charge pump runs through cycles for all possible V_{st} , from V_{res0} to the saturation value $V_{st sat}$.

8.4.3 Evolution of the Harvested Energy

Neglecting the energy in the transducer capacitance since it is small, and supposing that the C_{st} voltage is initially V_{res0} , the energy harvested during the *n* first C_t variation periods is stored in the capacitors C_{res} and C_{st} , and is given as

$$W_n = \frac{1}{2}C_{st}V_{st\ n}^2 + \frac{1}{2}C_{res}V_{res\ n}^2 - \frac{1}{2}(C_{res} + C_{st})V_{res0}^2, \tag{8.19}$$

Fig. 8.13 Evolution of the electrical state of the charge pump without flyback. **a** Evolution of V_{st} and V_{res} voltages, **b** evolution of the total converted energy (W_n) and of the energy converted at one cycle (ΔW_n) . The simulation was done with $C_{min} = 200 \text{ pF}$, $C_{max} = 400 \text{ pF}$, $C_{st} = 3.3 \text{ nF}$, $C_{res} = 10 \text{ }\mu\text{F}$, frequency of C_t variation is 300 Hz



where $V_{res n}$ is the C_{res} voltage after *n* vibration cycles and V_{res0} is the initial voltage of C_{res} . At the same time, the sum of charges of C_{st} and C_{res} is constant, so, the following relation holds (neglecting the charge shared with C_t):

$$C_{st}V_{res0} + C_{res}V_{res0} = C_{st}V_{st\ n} + C_{res}V_{res\ n}.$$
(8.20)

Using (8.20), Eq. (8.19) can be simplified

$$W_n = \frac{C_{st}C_{res}}{C_{st} + C_{res}} (V_{st\ n} - V_{res\ n})^2 / 2.$$
(8.21)

This equation suggests that the harvested energy is stored in the capacitor composed of C_{st} and C_{res} connected in series. This formula can be further simplified if $C_{st} \ll C_{res}$ and if C_{res} is large, so that $V_{res n} \approx V_{res0}$. In this case, we can write

$$W_n \approx C_{st} (V_{st n} - V_{res0})^2 / 2.$$
 (8.22)

This equation suggests that the converted energy is mainly stored in the C_{st} capacitor.

8 Conditioning Circuits for Capacitive Energy Harvesters

The value

$$\Delta W_n = W_n - W_{n-1}, \tag{8.23}$$

gives the energy converted during one cycle. For the case when $C_{st} \gg C_{max}$, ΔW_n is equal to ΔW given by Eq. (8.9), if in (8.9) V_{st} and V_{res} are replaced by V_{res0} and $V_{st n}$ corresponding to the cycle.

In the formula (8.22) expressing the energy converted from the state where $V_{st} = V_{res0}$, there is no explicit dependence on discrete time *n* (the cycle number). If $C_{st} \gg C_{max}$, the variation of the voltage V_{st} is negligible at the time scale of one cycle. For this reason, we can state that V_{st} evolves continuously, and consider it as "macroscopic state parameters" defining the energy of the charge pump. It allows us to remove the indices *n* in the Eq. (8.22) and to define the total harvested energy *W* as

$$W(V_{res0}, V_{st}) = C_{st}(V_{st} - V_{res0})^2/2.$$
(8.24)

If, during the operation of the charge pump, the V_{st} voltage increases from some V_1 to some V_2 , the corresponding converted energy is given by

$$\Delta W(V_{res0}, V_1, V_2) = W(V_{res0}, V_2) - W(V_{res0}, V_1) = C_{st}(V_2 - V_1)(V_2 + V_1 - V_{res0})/2.$$
(8.25)

Figure 8.13b presents the plots characterizing the evolution of the energy in the charge pump as a function of the cycle number. During each cycle *n*, the total energy (square dots) increases by the value given by (8.9) calculated for the V_{st} resulting the previous cycle (triangular dots). Only a few cycles convert a significant amount of energy: those corresponding to V_{st} values close to the optimal $V_{st opt}$, (cf. the analysis of Sect. 8.4.1 for fixed V_{res}). This value is situated in-between the extreme values of V_{st} , and a freely running charge pump finishes by entering into the saturation mode, in which $V_{st} \approx V_{st sat}$ and $\Delta W_n \approx 0$.

8.4.4 Shortcomings of the Single Charge Pump

Because of a dynamic evolution of V_{st} voltage leading to a saturation, the charge pump alone is not useful for capacitive VEHs. Practical conditioning circuits should be able to (i) ensure a sustainable energy conversion by fixing the V_{st}/V_{res} ratio to the optimal value as mentioned in Sect. 8.4.1, (ii) accumulate the converted energy. These two very important points are discussed in this subsection.

Need for a Flyback

The plot ΔW_n in Fig. 8.13b can be seen as the average power converted in a cycle. The goal of a harvester is to permanently maintain the converted power close to a **Fig. 8.14** Principle of operation of a charge pump with a mechanism of return of charges from C_{res} to C_{st} , called "flyback"

maximum level. For this reason, a charge pump needs periodic *flyback*: a mechanism returning some of charges from C_{st} to C_{res} so as to keep V_{st} close to the optimal value and to prevent the charge pump from saturation. Possible implementations of the flyback will be discussed in Sect. 8.5.

The action of the charge pump can be seen as the generation of an average current flowing from a low potential (V_{res}) to a higher potential V_{st} (Fig. 8.14). This current is roughly equal to

$$i_{ch\ pump} = \frac{Q_1 - Q_2}{T_e} = \frac{V_{res}C_{max} - V_{st}C_{min}}{T_e}.$$
 (8.26)

The flyback must create an opposite current from C_{st} to $C_{res} i_{fly}$, preventing the accumulation of charges on C_{st} , and so, avoiding the charge pump saturation. This current, flowing from the high-to-low potential, *removes* the electrical energy from the charge pump, and in a practical application, this energy should be transferred to a useful load. In the steady-state mode, the rate at which the energy is removed from the charge pump is equal to the power of the electromechanical conversion.

Auto-Increasing of the Internal Energy

From (8.9) and further analysis of Sect. 8.4.2, it can be seen that the energy converted by a charge pump is proportional to the square of the voltage V_{st} and V_{res} , i.e., proportional to the internal energy of the circuit in Fig. 8.11b. Practical studies highlight that up to tens of volts may be needed for optimal operation [1]. However, the initial charge can only be obtained by a low voltage battery existing in the system, or by a complementary piezoelectric VEH as proposed in [11]. In both cases, the initial voltage generated in this way will certainly be low (few volts).

As a consequence, the conditioning circuit should be able to use a part of the converted energy in order to *increase* its biasing: its internal energy represented by the voltage on the largest capacitor, V_{res} . This is the "accumulative" or "self-increasing" mode discussed in Sect. 8.4.4.

The auto-increasing capability is not offered by the basic charge pump.



8.5 Circuits Derived from the Primitive Charge Pump

In this section, we discuss more sophisticated conditioning circuits which are derived from the architecture of the basic charge pump considered above. All of them implement a rectangular QV cycle. In all these circuits, the basic topology of the charge pump presented in Fig. 8.11 is complemented by networks allowing a return of the charges, so to allow a steady operation providing a fixed ratio V_{st}/V_{res} . Here, we present a short discussion of these solutions.

8.5.1 Resistive Flyback

The simplest way to implement a flyback is to connect a load between C_{res} and C_{st} (Fig. 8.15), originally proposed in [11]. Here, the load is represented with a resistance R_{load} whose current is

$$i_{fly} = \frac{V_{st} - V_{res}}{R_{load}}.$$
(8.27)

A simplified analysis may be done by analyzing independently the charge flows of the charge pump and of the resistor, and then by superimposing them. The point at which both currents are equal to each other $(i_{ch pump} = i_{fly})$ corresponds to steady-state operation. Although it is an approximation based on the averaging method [19], it gives good analytical results.

In the steady state, the average V_{st} voltage on a period T_e is the same for all cycles. The stability of this mode can be easily proven by supposing a perturbation which yields, for example, $i_{ch pump} < i_{fly}$. In this case, the load current consumption outweighs the current due to the charge generation by the pump, and V_{st} decreases. This results in decreasing of i_{fly} , and so in reducing the initial perturbation.

Under these considerations, the average steady-state voltage V_{st} with resistive flyback can be predetermined by equating (8.26) and (8.27). Conversely, the value of R_{load} yielding a desired V_{st} (for example, that yielding a maximum ΔW) can be calculated.





The resistive flyback configuration provides a sustainable energy conversion by preventing the charge pump from the saturation. This is an efficient solution from the point of view of the simplicity of implementation. However, it does not allow an auto-increasing of its internal energy (cf. Sect. 8.4.4), and for this reason, is not usable in practical applications.

8.5.2 Inductive Flyback

The inductive flyback is a Buck DC–DC converter, transferring energy from C_{st} to C_{res} (Fig. 8.16a). The flyback operates in two steps

- (i) When V_{st} is high so that the efficiency of the charge pump decreases, some external control device (cf. the explanation below) activates the switch SW, and the current in the inductor L starts to increase. This results in: (i) charges being transferred from C_{st} to C_{res} , so that V_{st} decreases, (ii) the energy previously generated by the charge pump on C_{st} is transferred to L.
- (ii) As the magnitude of V_{st} decreases, it becomes close to V_{res} , and the same external device cuts the switch, so that the inductor discharges through the flyback diode D3 onto C_{res} . This results in a transfer of the inductor energy to C_{res} , and an *increase* of the C_{res} voltage, since the diode D3 is connected to the ground. In this way, the converted energy is used to extract charges from the ground and to inject new charges into the charge pump.

It can be seen that C_{res} receives charges twice: in the first phase, it receives the charges previously given to C_{st} during the pump operation, and in a second phase, it receives new charges from the ground. In this way, C_{res} receives the energy it has given to C_{st} during the operation of the charge pump, and it receives the energy converted from the mechanical domain. If such an operation is cyclic, the average voltage and energy of C_{res} will grow. In this way, two problems are solved: (i) even if



the capacitors are leaky, the losses are compensated by the charges extracted from the ground, (ii) a large capacitor C_{res} contains the harvested energy available for the load (represented by dotted lines in Fig. 8.16a). If no load is present, C_{res} accumulates the converted energy, and so implements an "auto-increasing" or "accumulative" mode.

The advantage of the charge pump with inductive flyback is the possibility of a precise control of the QV cycle corresponding to the energy conversion. This is achieved by a modulation of the average V_{st} voltage so as to remain in the optimal mode for energy conversion.

A drawback of the circuit is the need of an external command for the switch. However, this command is synchronized not with the mobile mass vibrations, but with the evolution speed of the voltage V_{st} : first, a voltage can easily be measured, and second, the evolution is low compared to the frequency of the capacitance variation. Hence, the cost of such a command is smaller than for circuits implementing constant voltage or constant charge QV cycles (see Sects. 8.3.1 and 8.3.2).

Practical implementation of adaptive architecture in Fig. 8.16 is challenged by the relatively low power available for the control circuitry, and by the need to manage high voltages in the conditioning circuit. Most studies have used an "old" CMOS technology supporting high voltages (e.g., 0.7 μ m CMOS in [14]). The work [9] used a mixed high-voltage/low-voltage 0.35 μ m CMOS technology, where high voltage circuits are used for the interface with the charge pump, and the processing is done by low voltage parts. This allows a minimization of the power overhead of the control electronics. Implementation of a high-side high voltage MOS switch for the flyback control with a low voltage control interface represented a particular difficulty. An advanced study of a fully integrated CMOS implementation of the control architecture, as in Fig. 8.16, was presented in [9, 10]. To date, implementation of a working IC prototype of this architecture is still a subject of ongoing work in several research groups.

8.6 Conditioning Circuits Based on the Bennet's Doubler

8.6.1 Introduction of the Principle

Introduced at the end of the eighteenth century [2], the Bennet's electricity doubler is one of the first devices allowing a measure of a voltage, by amplifying the induced charge. It has recently been proposed by de Queiroz [3] for capacitive kinetic energy harvesters. Since then, several works have further developed this concept, adapting it to microscale VEH [7, 8, 15, 21].

The Bennet's doubler is a switched capacitor network, whose goal is a steady separation of the electrical charges and an accumulation of the separated charges in the capacitors. A steady accumulation of the charges may lead to very high (the-



Fig. 8.17 Principle of the charge doubling in Bennet's doubler: **a** series configuration of capacitors when the current is positive, **b** parallel configuration of capacitors when the current is negative, **c** a diode network allowing an automatic switching between the configurations, depending on the sign of the current

oretically unlimited) voltages. Before analyzing conditioning circuit based on the Bennet's doubler, we propose an analysis of a more simple network widely used as a serial-parallel switched capacitors DC–DC converters. The purpose of the proposed discussion is to help the reader to acquire an intuitive understanding of the operation of the Bennet's doubler based conditioning circuit, whose more detailed analysis will be given in Sects. 8.6.2 and 8.6.3.

Consider an AC current source providing at the first half period a charge ΔQ , and pulling at the second half period the same charge. If during the first half period such a source is connected to a series capacitive network composed of two identical capacitors initially charged to identical voltages (Fig. 8.17a, $V_1 = V_2$), each capacitor receives a charge ΔQ . However, if during the second half period, the network topology is reconfigured and the previously charged capacitors are connected in parallel (Fig. 8.17b), the current source takes a charge $\Delta Q/2$ from each capacitors. At the end, each capacitors. The cyclic reconfiguration of the circuit topology from series to parallel is usually achieved by externally controlled switches. In this case, the circuit can be seen as an AC-DC converter, since the AC current with finite maximum and minimum values is converted to a DC voltage, whose value is controlled by the number of operation cycles.

In order to achieve an automatic cyclic reconfiguration of the circuit between the topologies of Fig. 8.17a and b (i.e., without use of an external control), one may benefit from the fact that in each topology the current has a specific direction. Figure 8.17c presents a topology in which this reconfiguration is automatic thanks to a diode network. When the current is positive, the diode D2 is ON (series configuration), and when the current is negative, the diodes D1 and D3 are ON (parallel configuration). The use of the diodes introduces a new feature to the network: the voltages across C_1 and C_2 may be different (for example, because of the initial charging). In this case, when the current is negative, all the current passes through the branch with the maximum voltage, and the current source generates a voltage $max(V_1, V_2)$.

The requirement applied to the current source is to be able to generate a voltage³ $V_1 + V_2$ during the positive current phase, and a voltage max(V_1 , V_2) during the negative current phase. This is always possible for an *ideal* current source, which, by definition, can generates any voltage necessary to ensure the required current value. This is not the case of a real current source, and it leads to significant consequences when the current source is implemented by a transducer, as it will be discussed later in this chapter.

It can be noticed that on the time scale of one period, the network in Fig. 8.17c implements a voltage limiter with the characteristic as in Fig. 8.10a if C_1 and C_2 are large, and if ΔQ is small comparing to the charges of these capacitors. Indeed, in this case the variation of the charges and hence of the voltages on C_1 and C_2 are negligible at the time scale of one period, and the current source voltage is max (V_1, V_2) when the current is negative, and $V_1 + V_2$ when the current is positive. If, for some reason, the voltage applied to the terminals 1 and 2 of the network in Fig. 8.17c is in-between these limits, all diodes are blocked and the current is zero.

A similarity of the considered network (Fig. 8.17c) with a voltage limiter suggests that it can be used for implementation of a conditioning circuit achieving a rectangular QV cycle. Such a configuration is shown in Fig. 8.18, and was originally proposed by de Queiroz [3]. Its operation principle can be understood if one consider a functional similarity between a variable capacitor $C_t(t)$ and a current source. Consider a variable capacitor whose capacitance $C_t(t)$ reduces in time. When connected to a voltage source V, it generates a positive current $i = V dC_t/dt$: the similarity with a positive current source is obvious. When such a variable capacitor is connected to a open circuit, it generates an increasing voltage $Q_t/C(t)$, where Q_t is the charge of the transducer (which is constant in time, since the current is zero). If the C_t decrease is bounded by some C_{min} , the voltage increase is bounded by Q_t/C_{min} , and if $C_{min} \rightarrow \infty$, the voltage tends to become infinite. A current source connected to a open circuit generates an infinite voltage if the source is ideal, or a voltage limited by IR_S if the source is real, i.e., having an internal resistance R_S . There is hence a similarity in the

³We remind that an ideal current source generates in the external network connected to it a current of a given intensity. For that, it generates a *voltage* necessary to fix such a current. The value of this voltage is determined by the external circuits. For instance, if a resistance R is connected to a current source generating a current I, the source generates a voltage RI.





electrical behavior between a capacitor having an decreasing/increasing capacitance and a positive/negative current source correspondingly.

As a conclusion, a Bennett's doubler conditioning circuit is a series-parallel switched capacitors AC–DC converter, where the input AC current is generated by a variable capacitor. As the analysis presented in the next section will show, this circuit does not experience a saturation like the charge pump in Fig. 8.11b, and as a consequence, doesn't need any external control for steady generation of electricity.

8.6.2 Operation of a Bennet's Doubler in the Electrical Domain

We propose to consider the operation of the Bennet's doubler starting from a state at which one of the capacitors is initially charged to a voltage V_0 , and the other capacitors are discharged. The Bennet's doubler will first experience a transient process during which the voltage of the second fixed capacitor will rise till V_0 , and then, the circuit enters into the steady-state, in which the both voltages increase exponentially with time.

In order to illustrate the operation of the circuit, we performed an Eldo simulation of the circuit with the following configuration: $C_1 = 10 \text{ nF}$, $C_2 = 1 \text{ nF}$, the transducer is a gap closing transducer as presented in Sect. 4.1.1 with $d_0 = 50 \,\mu\text{m}$ and $S = 10^{-4} \text{ m}^2$. Capacitor C_1 is initially charged to $V_0 = 5 \text{ V}$. The mobile electrode of the transducer moves according to sinusoidal law, with amplitude of $X_0 = 30 \,\mu\text{m}$ and frequency f = 100 Hz. In that way, the transducer capacitance C_t varies according to Eq. (8.7). From this equation we calculate $C_{min} = 11.05 \text{ pF}$ and $C_{max} = 44.2 \text{ pF}$. The listing of the used Eldo model is given in Listing 8.1, and the time evolutions of V_1 and V_2 obtained by simulation are given in plots of Fig. 8.19. The plot Fig. 8.19a presents a long-term evolution of the voltages on capacitors C_1 and C_2 , and the plot Fig. 8.19b presents a zoom of the time interval covering the transient and the beginning of the steady-state mode.

```
Listing 8.1 Bennet's doubler with variable capacitance: Eldo netlist
```

```
***** The first line is ignored in spice netlists*****
.model diode1 d level=1
**** The parameter definition *****
*The transducer gap
.param d=50e-6
*The transducer area
.param S=1e-4
*Permittivity of vacuum
.param eps0=8.85e-12
*Simulation time
.param simtime=30
*Amplitude of the mobile plane motion
.param X0=30e-6
*Frequency of the mobile plane motion
.param f=100
*The voltage source defining the trajectory of the mobile electrode
Vx x_value 0 sin 0 X0 f
*The voltage controlled voltage source
*defining the variation of the transducer capacitance
ECt Ct_value 0 value={eps0*S/(d-v(x_value))}
*The transducer
Ct b3 0 value={v(Ct_value)}
*The two fixed capacitances C1 and C2, initially charged
*to 10V and to 0V respectively
C1 b1 0 10e-9 ic=10
C2 b3 b2 1e-9 ic=0
*The three diodes
db1 0 b2 diode1
db2 b2 b1 diode1
db3 b1 b3 diode1
*Transient simulation command,
*with option uic (Use Initial Conditions)
.tran {simtime} {simtime} uic
*Plotting commands
.plot V(b1) V(b2) V(b3)
.plot V(b3,b2)
.plot V(b1,0)
.plot V(Ct_value)
*Writing of waveforms to text files, for the plot drawing
.printfile tran v(b1) file=V2.txt start=0 stop={simtime} step=5e-6
.printfile tran v(b3, b2) file=V1.txt start=0 stop={simtime} step=5e-6
.printfile tran v(Ct_value) file=Ct.txt start=0 stop={simtime} step=5e
    -6
.printfile tran v(b3) file=Vt.txt start=0 stop={simtime} step=5e-6
*simulator options
.options hmax=10e-6
```



Fig. 8.19 Evolution of voltages in the Bennet's doubler: **a** long-term evolution of the voltages V_1 and V_2 , **b** zoom on the time interval covering the end of the transient process and the beginning of the steady-state

Note that in this configuration the values of the fixed capacitors are much larger that the value of the maximum transducer capacitance. It means that the variation of the voltages on C_1 and C_2 at the time scale of one period are small comparing to the voltage variation on C_t .

The analysis of starts from $C_t = C_{max}$ at t = 0. We consider that thanks to the diode D1, the transducer is pre-charged to the same voltage as C_1 . As C_t decreases, diode D_2 is on and both C_1 and C_2 receive charges from the transducer. In this way, the voltage on C_2 increases slightly. As C_t stars to decrease, the capacitor having the highest voltage becomes in parallel with the transducer. Since C_1 was initially charged to 5V and C_2 experienced a small voltage increase, C_1 is the one becoming in parallel to C_1 through the diode D1, and C_1 gives the charges it previously received from C_t . At the end of this cycle, C_1 has the same voltage as in the beginning, and C_2 voltage increased.

The same process continues in the next cycles, till the voltages on the both fixed capacitors become equal. In the presented simulation, it happens at t = 0.4 s. Starting from that cycle, the network enters in the steady-state operation, in which the both voltages increase exponentially, and in average, they are equal. Since the diode network switch so that the voltage applied on the transducer is $max(V_1, V_2)$ and $V_1 + V_2$, the max-to-min ratio of the voltage on the transducer in the steady-state mode is 2. The voltage on C_1 displays a very low ripple, comparing with the voltage on C_2 . This is because of the difference between the value of the capacitances C_1 and C_2 : the charge variation is the approximately the same on both, but the voltage variation given by Q/C is greater on the smaller capacitor.

8.6.3 QV Cycle of the Bennet's Doubler and Approximated Analysis in Steady State

Figure 8.20a present the simulated plot of QV cycle that the Bennet's doubler with the presented configuration achieves in the steady state. The QV diagram is drawn for the cycle corresponding to the time instant 0.8 s (the simulation shown in Fig. 8.19). The vertical segment of the QV cycle correspond to the phases at which the transducer is connected to

- The both fixed capacitors in series (the right segment, D2 is on)
- The smallest of the fixed capacitor of the fixed capacitors (the lower left segment, only diode D3 is on)
- The both fixed capacitors in parallel (the upper left segment, both diodes D1 and D3 are on)

Each of this segment has a slope 1/C, where *C* is the total equivalent capacitance of the capacitive network connected to the transducer by the diodes in each case. It can be noticed a non-infinite slope of the vertical segments of the QV cycle, however, the shape is very close to be rectangular. This is because the fixed capacitors are very large comparing to C_{max} . In order to provide an insight into the operation of the circuit, the same network was simulated with smaller capacitors C_1 and C_2 (Fig. 8.20b), whose values are now of the same order of magnitude as the transducer capacitance. It can clearly be seen that

- The three non-horizontal sections have different and non-infinite slopes,
- The cycle is not closed: the values of Q_t and V_t at $C_t = C_{max}$ at the beginning of the cycle are smaller that at the end of the cycle; this highlights the increase of the internal energy of the network.



Fig. 8.20 QV diagram of Bennet's doubler obtained by simulation with the netlist given in Listing 8.1, with different values of capacitors C_1 and C_2 : **a** $C_1 = 10$ nF, $C_2 = 1$ nF, as in the netlist given in Listing 8.1, **b** $C_1 = 500$ pF, $C_2 = 100$ pF. The corresponding C_{min} and C_{max} are 11.05 pF and 44.2 pF, respectively. It can be seen that when min $(C_1, C_2) \gg C_{max}$, the cycle is very close to be rectangular (**a**). As the fixed capacitances are of the same order of magnitude as the transducer capacitance, the cycle is not exactly rectangular and highlight different stages of the circuit operation corresponding to different states of the diodes

Considering the QV cycle of the Bennet's doubler, it is possible to give an approximated expression of the energy converted in one cycle in the steady-state mode. If $C_{max} \ll C_1$ and $C_{max} \ll C_2$, the voltage on C_1 and C_2 may be considered fixed at the time scale of one cycle, and according to (8.9), we have:

$$\Delta W_{ss} \approx (2V - V)(VC_{max} - 2VC_{min}) = V^2 (C_{max} - 2C_{min})$$
(8.28)

Here, V is the voltage on one of the capacitors C_1 and C_2 : in the steady state these voltages are roughly equal.

The energy ΔW_{ss} is positive if $C_{max} - 2C_{min} > 0$. This is a necessary and sufficient condition allowing the Bennet's doubler to highlight an accumulative mode with exponentially increasing voltages on the fixed capacitors. If this condition is not fulfilled, the Bennet's doubler is still able to generate electricity (i.e., to convert energy) in the transient mode, as far as the following condition holds:

$$\frac{C_{max}}{C_{min}} > \frac{V_1 + V_2}{max(V_1 + V_2)}$$
(8.29)

In this case, the energy converted at each cycle is

$$\Delta W_{tran} \approx (V_1 + V_2 - max(V_1, V_2))(max(V_1, V_2)C_{max} - (V_1 + V_2)C_{min}) \quad (8.30)$$

As shows the plot Fig. 8.19a, in all this energy is accumulated in the capacitor with the smallest voltage, so that at some moment the condition (8.29) is not fulfilled since the smaller voltage increases. Then, the Bennet's doubler saturates, similarly with a classical charge pump of Fig. 8.11b, the voltages on C_1 and C_2 do not increase, the QV cycle is degenerated into a line and no energy conversion is achieved.

8.7 Dynamic behavior and Electromechanical Coupling of Rectangular QV Cycle Conditioning Circuits

Analysis of a conditioning circuit in the electrical domain assumes that the variation of the transducer capacitance is independent from the electrical state of the transducer. As we mentioned in Chap. 4, in practice, this does not hold for real electrostatic transducers connected to microscale mechanical resonators. Indeed, as it was said in Sect. 4.1.6, the electromechanical coupling impacts the dynamic of the mobile mass vibrations. As a consequence, the extreme values of the transducer capacitance C_{max} and C_{min} can also vary with time. As show on the example of charge pump and Bennet's doubler conditioning circuits, the electrical dynamic of the circuits depends on C_{max} and C_{min} which, in turn, depends on the electrical force generated by a dynamically biased transducer. Such a coupled behavior, to be described formally, requires advanced mathematical tools such as nonlinear differential equations, perturbation techniques, etc., which were introduced in Chap. 3. In this paragraph, we only present an example of how electromechanical coupling impacts the operation of a conditioning circuit, by studying the case of the Bennet's doubler.

We chose the example of Bennet's doubler since the difference between its operation in electrical domain and in a context where a real transducer/resonator are connected is flagrant. Indeed, without mechanical coupling, the output voltage of the Bennet's doubler (e.g., the voltage V_1 or V_2 , Fig. 8.18) increases exponentially without any limit. If the variation of the capacitance is due to the motion of a mechanical system, one cannot expect an exponential evolution of the voltages and the energy converted at one cycle, because of the fundamental limit of the power which can be absorbed from the external vibrations, given by Eq. (3.92) from Chap. 3. The mechanism practically limiting the increase of the voltage is the presence of the electrostatic force generated transducer, which impacts the amplitude of the mobile mass vibrations so to reduce C_{max}/C_{min} and to limit the power converted by the transducer. Simulation and experiments highlight two possible behaviors of the system

- a "smooth" saturation. In this case, as the energy of the Bennet's doubler increases, the amplitude of the mobile mass decreases smoothly, and the ratio C_{max}/C_{min} asymptotically approaches 2. That stops the energy conversion by the circuit. Such a behavior was experimentally observed in study [7]. Figure 8.21 presents simulation curves highlighting such a behavior. As the voltages V_1 and V_2 grow, the amplitude of the mobile mass vibration changes in a sophisticated manner: it increases first, reaches a peak and decreases. This mechanical dynamics impacts the variation of the transducer's capacitance. The evolution of the voltages is, in turn, impacted by the C_{max}/C_{min} ratio evolution: the rate is slow at the beginning, increases near the peak of the amplitude, decreases after the peak, and becomes zero as C_{max}/C_{min} approaches 2 after time t = 10 s. The presence of a peak of amplitude at 2.4 s reminds a resonance phenomenon: indeed, we obtain a similar amplitude envelope if a linear resonator is excited by a sinusoidal signal with a frequency sweep. In our model, the frequency of the external acceleration is fixed, but the resonance frequency of the resonator is continuously modified by the voltages V_1 and V_2 responsible for the QV cycle definition. The drift of the resonance frequency is clearly observed in the plot for the displacement x.
- an "abrupt" saturation. In this case, the increase of the output voltage does not produce the reduction of the amplitude of the mobile mass, but creates conditions for a pull-in phenomenon proper to the gap closing transducer (cf. [23]). In this case, as the bias voltage of the circuit increases, the mobile mass sticks to the stoppers, and does not display any significant motion, so that C_{max}/C_{min} ratio is close to 1. This abruptly stops the increase of the output voltage. The resulting evolution is given in Fig. 8.22.





As a consequence, in practice, the Bennet's doubler based conditioning circuit highlights a saturation of the output voltage, similarly with the charge pump considered in Sect. 8.4.2. Hence, for all circuits is it possible to find the value of the output voltage yielding a maximum energy conversion rate. A realistic design requires to take into account the mechanical coupling, which modify the optimal values of the output voltages calculated by the analysis in the electrical domain. This is discussed in the next section.



8.8 Practical Use of Conditioning Circuits with Rectangular QV Cycle

The last question we would like to discuss is the following: how it is possible to maintain the output voltage of a conditioning circuit at the optimal level? The most straightforward and generic technique is presented in Fig. 8.23.



Fig. 8.23 Architecture implementing the control of the internal energy (the output voltage) of the vibration energy harvester in order to maximize the converted power

This architecture is based on a DC-DC converter which interfaces the output capacitance of the conditioning circuit (C_S or C_{res} in the case of the charge pump with flyback) with a low voltage energy reservoir available for the load supply. The output voltage of the harvester is defined by two energy flows: (i) the energy converted from the mechanical domain which tends to increase the output voltage, (ii) the DC–DC conversion removing energy from the conditioning circuit to the load reservoir. By controlling the second flow, it is possible to control the average level of the output voltage, and to guarantee that it corresponds to the optimal value for the maximum power conversion. The technique is very similar with what we proposed for the control of the voltage V_{st} of the charge pump in Sect. 8.5.2 [9]: the definition of the optimal voltage $V_{st opt}$, the definition of the acceptable interval for the output voltage variation, the control of a DC-DC converter in order to remove the extra energy from the output capacitor, when necessary. The energy is accumulated on the load capacitor C_L and when there is enough energy for accomplishing some useful operation, the load is supplied. The most critical block is the one implementing the control of the DC-DC converter (represented as a gray cloud in the diagram), since an complex analog information processing is required, as discussed in Sect. 8.5.2. A simplified version of such an interface with the load is proposed in [3].

The implementation of this technique is a very challenging task, mainly because of the low level of power available for the implementation of the control algorithm. Ultra-low power analog integrated circuits is required to make it possible. This issue is currently being studied in several research groups.

8.9 Conclusion on Conditioning Circuits for eVEHs

This chapter presented essential information about the electrical conditioning of electrostatic transducers for vibration energy conversion. Such use of the capacitive transducer is relatively recent (not more than 10–15 years), and the associated practical knowledge is relatively small. To the date of this book's writing, most of the presented concepts have been essentially validated by prototypes issued from research projects and by simulation. Substantial efforts from the community of researchers and engineers are still necessary in order to elevate the maturity level of these techniques so to employ them into commercial applications.

In many existing studies, the conditioning circuits of vibration energy harvesters have been analyzed without accounting for the mechanical coupling. However, both experiment and the theory emphasize that the electromechanical coupling deeply modifies the behavior of the circuit. In particular, whereas the electrical analysis claims that the bias voltage must be the largest possible in order to maximize the converted power (cf. for instance formulae (8.9) and (8.28)), analysis of the full system, simulations and experiment highlights the existence of an optimal value of the bias voltage [7]. Chapter 3 introduces analytical tools which can be used for the study of the coupling phenomena in capacitive energy harvesters, and provide some examples. The used mathematical tools are quite involved even for simple configurations, and to date, more investigation is required to have a comprehensive and handful representation of the effects of the electromechanical coupling.

Implementation of smart and adaptive behavior of capacitive VEHs like represented in diagrams Figs. 8.16a and 8.23, is mainly impeded by the low amount of power available from a microscale capacitive energy harvester. However, this limitation is specific to the technologies of integrated circuits (IC) which have been available for the studies carried out to date. Future evolutions of the IC technologies will allow the implementation of the control circuitry with an acceptable power overhead. From this standpoint, electrostatic vibration energy harvesting may be seen as an emerging technology, having a strong potential for tomorrow's applications.

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