Chapter 12
Optimization of RF On-Chip Inductors Using Genetic Algorithms

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Abstract This chapter discusses the optimization of the geometry of RF on-chip inductors by means of a genetic algorithm in order to achieve adequate performance. Necessary background theory together with the modeling of these inductors is included in order to aid the discussion. A set of guidelines for the design of such inductors with a good quality factor in a standard CMOS process is also provided. The optimization process is initialized by using a set of empirical formulae in order to estimate the physical parameters of the required structure as constrained by the technology. Then, automated design optimization is executed to further improve its performance by means of dedicated software packages. The authors explain how to use state-of-the-art computer-aided design tools in the optimization process and how to efficiently simulate the inductor performance using electromagnetic simulators.

12.1 Introduction

The design and fabrication of on-chip radio frequency (RF) inductors have constantly demonstrated wide interest due to the need of providing single-chip solutions for integrated transceivers. They are required in matching networks, resonator tanks, baluns, and as inductive loads. The performance of radio frequency integrated circuits (RFIC), including low-noise amplifiers, mixers, and oscillators, is greatly limited by the quality factor of such passive elements. This is particularly

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true in standard silicon processes (e.g., CMOS), whose characteristics (such as substrate coupling) contribute to the relatively poor performance of the available passive components. CMOS processes are often chosen to implement RF circuit blocks due to their low cost, high level of integration, and availability. RFIC designers generally demand for on-chip inductors to have a desirable value with a high self-resonant frequency and high quality factor and occupy a small layout area. In general, passive inductors fabricated in a standard CMOS fabrication process have small inductance in the range of nanohenries.

Inductors are circuit elements which store energy in the form of a magnetic field. In RFIC, spiral inductors are fabricated on the topmost metals available in the process. For instance, Figs. 12.1 and 12.2 illustrate the top and cross-sectional views of a square inductor fabricated in a generic CMOS process [1]. The top metal layer (M1) is used for the spiral, while the lower metal layer (M2) is used for the underpass as depicted in Fig. 12.2.

Spiral inductors are mainly defined by a number of geometrical parameters: the number of turns n, the width of the metal trace w, the turn spacing s, the inner diameter d_{in}, and the outer diameter d_{out}. They can be implemented in different

Fig. 12.1 Layout of a square spiral inductor (*top view*)
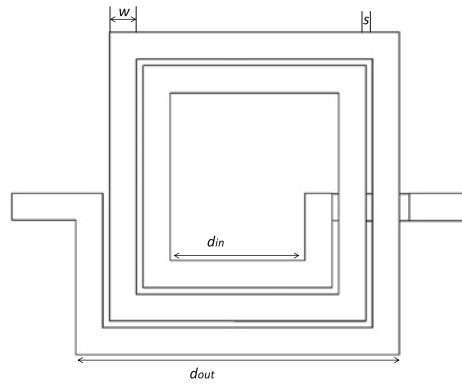
Fig. 12.2 Cross-sectional view of the implementation of a square inductor in a generic CMOS process
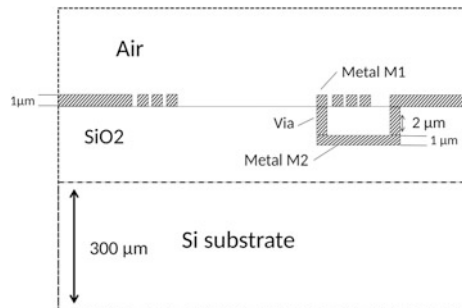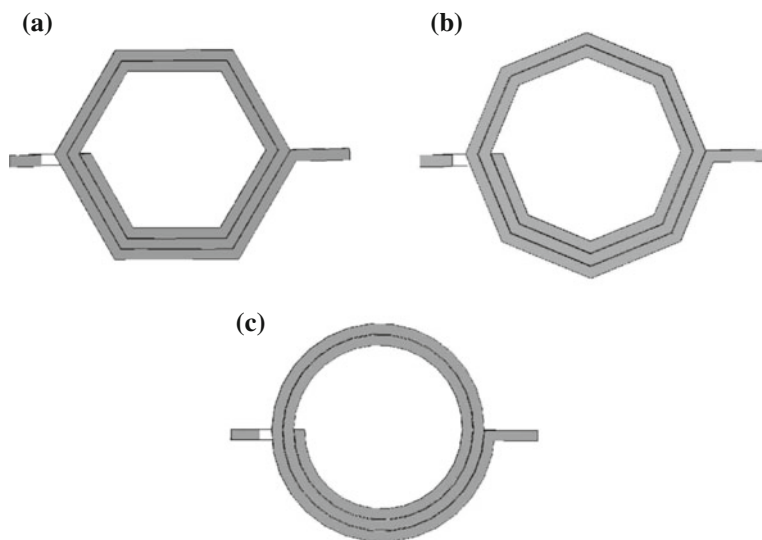
Fig. 12.3 Spiral inductor topologies [1]. **a** A hexagonal spiral. **b** An octagonal spiral. **c** A circular spiral

shapes such as hexagonal, octagonal, and circular configurations as shown in Fig. 12.3. The symmetrical forms of these inductors are often used in differential circuits such as voltage-controlled oscillators and low-noise amplifiers [3].

In order to reduce the substrate losses and enhance the inductor quality factor, a patterned ground shield (PSG) fabricated via a metal layer which is located between the spiral inductor and the substrate can be employed [4]. This is shown in Fig. 12.4.

Fig. 12.4 A spiral inductor with the patterned ground shield [3]
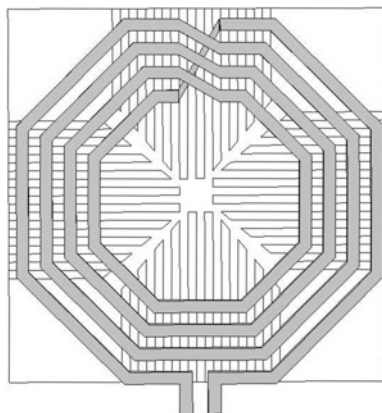
12.2 Losses in CMOS Inductors

Inductors implemented in a standard CMOS technology experience a number of electric and magnetic effects, which limit their performance. When a potential difference is applied to the terminals of the integrated inductor, magnetic and three electric fields appear as illustrated in Fig. 12.5 [5]. A magnetic field $B(t)$ is generated as the ac current flows through the tracks of the spiral. This induces an inductive behavior, while parasitic currents flow in the tracks and the substrate. According to Faraday's law, a time-varying magnetic field induces an electric field in the substrate which forces an image current to flow in the substrate opposite in direction to the current in the winding directly above it. Thus, this adds a loss to the CMOS inductor, since the substrate acts as an undesired secondary winding which loads the coil. In the case of larger inductors, the magnetic field penetrates deeper into the substrate causing higher substrate losses. To minimize the effect of such substrate losses, some technologies provide the possibility to either use nonstandard high-resistivity silicon substrate or have a post-processing micromachining step in order to etch the substrate underneath the inductor [6]. Additionally, f induces eddy currents in the center of winding which affect the inner turns of the inductor. This is also known as current crowding [7].

The electric field $E_1(t)$ appears as the potential difference is applied between the terminals of the spiral. Because of the finite metal resistivity, ohmic losses occur as the current flows through the track. In typical CMOS processes, aluminum (and sometimes copper) is used as the interconnecting metal. Its sheet resistivity lies between 30 and 70 mΩ/sq, depending on the metallization thickness and the type of aluminum alloy. Therefore, the dc resistance of the spiral can be easily calculated by the product of the sheet resistance and the number of spiral turns. An improvement in the quality factor can be achieved by an introduction of a copper metallization track with a thicker upper-level interconnect metal. Also, strapping multiple metallization levels to create a multilayer spiral effectively lowers the dc winding resistance [7].
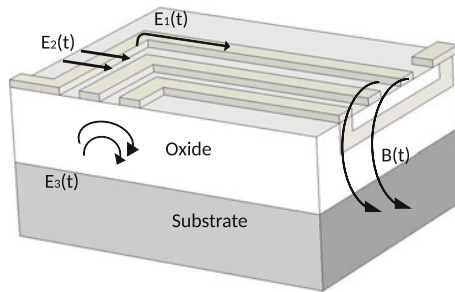
Fig. 12.5 Electric and magnetic fields associated with a square spiral inductor implemented in a generic CMOS process [5]

The potential difference between the turns in the metal that forms the spiral causes an electric field $E_2(t)$. Thus, capacitive coupling is induced between the tracks because of the dielectric material. Usually, the winding of the spirals in a CMOS technology is separated from the substrate by a thin layer of silicon dioxide. The silicon substrate is neither a perfect conductor nor an insulator. Therefore, there are losses in the reactive fields that surround the windings of the spiral. The substrate is a heavily doped p-type material and it is tied to ground such that a potential difference appears between the spiral and the substrate. Therefore, capacitive coupling is created between the inductive structure and the substrate. The induced electric field $E_3(t)$ penetrates into the conductive substrate, causing an ohmic loss. This allows RF currents to interact with the substrate, lowering the inductance value. Additionally, it increases the parasitic capacitance and lowers the self-resonant frequency. Reducing the trace width decreases the effect of this parasitic capacitance but in turn increases the series resistance. Hence, this implies that using wide traces helps to overcome the low thin-film conductivity of the metallization. On the other hand, this limits the possibility of creating large-value inductors. As a conclusion, the major losses in a standard CMOS technology are due to the effect of the substrate. This is still an important limiting factor, even when the conductivity of the spiral windings is not an issue.

12.3 Quality Factor

The quality factor Q is a fundamental parameter associated with energy storing elements and it is the measure of the storage efficiency. Since inductors store magnetic energy, they have an associated quality factor which offers an insight on their performance. It is defined as the ratio of the energy stored per cycle to the energy dissipated per cycle, as given in (12.1).

$$Q = 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated}} \tag{12.1}$$

For inductors, the only form of required energy is that stored in the magnetic field, while any energy stored in the electric field is a loss. In addition, inductors have an associated self-resonant frequency f_{sr} beyond which it starts to behave capacitively. At f_{sr}, the peak magnetic and electric energies are equal, such that Q becomes zero. Q is proportional to the net magnetic energy stored, which is equal to the difference between the peak magnetic and electric energies. Based on this definition and the lumped element π-model (refer to Sect. 12.5), Q is calculated using (12.22) [8].

$$Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p \left(1 - \frac{R_s^2 C_p}{L_s} - \omega^2 L_s C_p \right)}{R_p + \left[\left(\frac{\omega L_s}{R_s} \right)^2 + 1 \right] R_s} \tag{12.2}$$

where L_s, R_s, and C_s represent the series inductance, the metal series resistance, and the capacitive coupling, respectively. C_p and R_p represent the overall parasitic effect of the oxide and the silicon substrate. Inductors implemented in a standard silicon (Si) technology such as CMOS have a low Q resulting from the relativity high-conductivity Si substrate. Planar spirals that are fabricated on GaAs substrates exhibit Q in the range of 20–40, while the Q of inductors implemented on a Si substrate is much lower. Discrete off-chip inductors provide a much higher quality factor, but it is desirable to reduce the board-level complexity and limit the cost by using on-chip inductors. Bond wires are frequently used as an alternative to some on-chip inductors due to their high Q. They provide a higher surface area per unit length when compared to planar spirals, thus having less resistive loss and as a consequence a higher quality factor. However, they also suffer from large variations in the inductance value. Additionally, wire bonding is a mechanical process that cannot be tightly controlled as in the case of a photolithographic process [9]. Remarkably, the inductance of on-chip inductors is solely defined by their physical geometry, since modern photolithographic processes have stringent geometric tolerances limiting any variations in the inductor performance [7].

12.4 Guidelines for On-Chip Inductor Design

The square spiral topology is the most commonly used in the implementation of on-chip inductors. Another frequently used topology is the octagonal spiral topology. As the number of geometry sides increases, both the resistance and the inductance of the structure increase since a larger length of metal track would be used. However, the inductance value increases at a faster rate than that of the resistance, thus resulting in an increase of the quality factor. In this regard, the circular spiral geometry provides the largest perimeter for the same radius, thus maximizing the inductance and quality factor. Although it is preferable to employ a circular configuration, it is often not permitted by standard integrated circuit technologies. Additionally, non-Manhattan geometries are not supported by many technologies [9].

Reducing the resistance per unit length of an inductor trace is imperative to increase the quality factor and this is usually done by making use of thick metal layers. Alternatively, in conventional CMOS processes, two or more metal layers are connected together to thicken the inductor trace to generate a so-called multi-layer spiral inductors. The resistance of the inductors becomes smaller as the number of layers shunted together is increased, thus leading to an increase in the quality factor. In practice, the number of metal layers in a CMOS process may vary and this increase in the quality factor is often limited because of the finite resistance of the interconnecting vias. It is not recommended to use the metal layers closer to the substrate, because this would increase the parasitic capacitance associated with the structure, thus reducing the self-resonant frequency of the inductor.

Due to the eddy current effect, the innermost turns of the coils suffer enormously from a high resistance which affects the overall quality factor. In addition, the innermost turns give minimal contribution to the inductance. Hence, it is recommended to design a hollow coil. The inductor opposite coupled lines must have a $d_{in} \geq w$, in order to enable magnetic flux to pass through the hollow part. In addition, the spacing between the outer spiral inductor turn and any other surrounding metal should be at least $5w$. The width of the inductor should be as wide as the limit where the skin effect starts to be dominant. The wider the metal track, the higher the exhibited quality factor, because the resistance of the inductor decreases, while the inductance value remains constant. However, when the width is significant to the skin effect, the inductor resistance starts to increase. It was observed for spiral inductors operating from 1 to 3 GHz that the Q is optimum for a track width between 10 and 15 μm [10].

Due to mutual coupling between the spiral metal tracks, the spacing between the lines of the inductor should be as close as possible. Large spacing causes a reduction in the mutual coupling, thus lowering the inductance value [5]. Another design factor to take into account is the spiral radius. As the radius increases, the metal area overlapping the substrate increases accordingly and the parasitic capacitance between the spiral and the substrate increases. This results in a reduction of the self-resonant frequency. The substrate losses are also susceptible to the area occupied by the coil. Limiting the area, the magnetic field associated with the coil penetrates less deeply into the substrate, thus reducing the substrate losses.

12.5   Modeling of Two-Port Inductors

A two-port lumped passive element π-type equivalent circuit, shown in Fig. 12.6, can be used to model a spiral inductor implemented on a silicon substrate. This equivalent circuit includes a number of components which altogether model the variation of the inductance with frequency and the loss mechanisms related to the structure of the spiral inductor. In particular, L_s represents the inductance, R_s models the resistance of the metal trace, C_F represents the capacitive coupling between the spiral trace and the underpass, and the magnetic eddy current effect is modeled as an ideal transformer coupled to a resistor $R_{sub}(m)$. In addition, the substrate is represented by three components C_{sub}, R_{sub}, and C_{ox}, where C_{ox} is the oxide capacitance between the spiral and the substrate.

In order to estimate the value of these circuit elements, physically based equations related to the geometry of the spiral inductor and the parameters of the fabrication process can be used [11, 12]:

$$R_s = \frac{1}{\sigma \, \omega \, \delta (1 - e^{(-t/\delta)})} \qquad (12.3)$$

Fig. 12.6 General spiral inductor passive lumped element circuit model
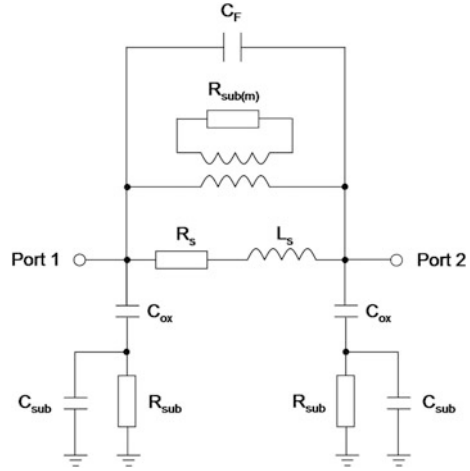
$$C_F = n\,\omega^2\,\frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{12.4}$$

$$C_{ox} = \frac{1}{2}l\,\omega\frac{\varepsilon_{ox}}{t_{ox}} \tag{12.5}$$

$$C_{sub} = \frac{1}{2}l\,\omega C_{sub/A} \tag{12.6}$$

$$R_{sub} = \frac{2}{l\,\omega\,G_{sub/A}} \tag{12.7}$$

where σ is the conductivity of the metal layer, l is the total length of the metal trace, δ is the metal skin depth, t is the metal thickness, t_{ox} is the thickness of the oxide situated between the spiral inductor and the substrate, and $C_{sub/A}$ and $G_{sub/A}$ are the substrate capacitance and conductance per unit area, respectively. The metal skin depth can be calculated using (12.8):

$$\delta = \sqrt{\frac{1}{\sigma\,\pi\,\mu f}} \tag{12.8}$$

where f is the frequency and μ is the permeability of free space. The skin resistance R_s is given by Eq. (12.3), showing that as the frequency of operation increases, the resistance of a metal segment will increase due to the skin effect. The values of the quality factor Q and the inductance L_s can be calculated from the equivalent circuit by converting the measured or simulated two-port S-parameters into Y-parameters and using the equivalent π-network given in Fig. 12.7. For symmetrical inductors, $Y_{12} = Y_{21}$ and $Y_{11} = Y_{22}$.
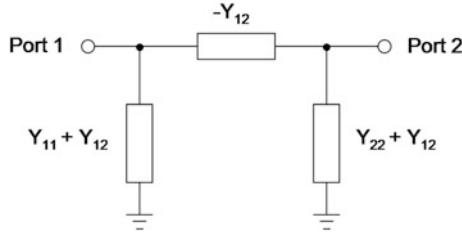
Fig. 12.7 π-equivalent circuit for a two-port network

In order, to define L and Q, one needs to reduce the π-network to single element circuit consisting of an inductor in series with a resistor. For a simple series element $R + jX$ (refer to Fig. 12.8), the inductance and the quality factor can be found using:

$$L = \frac{X}{2\pi f} \qquad (12.9)$$

and

$$Q = \frac{X}{R} \qquad (12.10)$$

Figure 12.8a shows the case in which one of the inductor terminals is grounded such that $Y_{12} + Y_{22}$ is bypassed and the circuit looking into port 1 reduces to an admittance Y_{11} connected to ground.

In this case, the input impedance Z_{in} of the inductor can be calculated by:
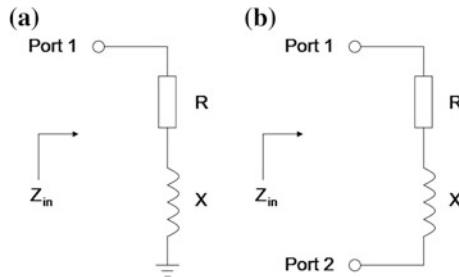
$$R + jX = \frac{1}{Y_{11}} \qquad (12.11)$$

Fig. 12.8 Two methods of simplifying the two-port π-network. **a** Single-ended configuration and **b** differential configuration

Thus, L and Q is defined as follows:

$$L = \text{Im}\left(\frac{1/Y_{11}}{2\pi f}\right) = -\frac{1}{2\pi f \text{Im}(Y_{11})} \tag{12.12}$$

$$Q = \frac{\text{Im}\left(\frac{1}{Y_{11}}\right)}{\text{Re}\left(\frac{1}{Y_{11}}\right)} = -\frac{\text{Im}(Y_{11})}{\text{Re}(Y_{11})} \tag{12.13}$$

Equations (12.12) and (12.13) are valid for an inductor used in a circuit, in which one of its terminals is connected to ground. This is often the case in many RF circuits, such as in low-noise amplifiers and mixers where the inductors are used for degeneration or as a load. L and Q can be calculated by using measured or simulated one-port S-parameters with one terminal of the inductor grounded and converting the reflection coefficient into an input impedance. The series input impedance Z_{in} is given by:

$$R + jX = Z_{\text{in}} = Z_0 \frac{1 + \Gamma_1}{1 - \Gamma_1} \tag{12.14}$$

where $\Gamma_1 = S_{11}$ and Z_0 is the port characteristic impedance. In other applications, such as differential voltage-controlled oscillators, the on-chip inductors are used in a differential configuration, where both ports are not at a ground potential (refer to Fig. 12.8b). In this case, a different approach is required to determine Q and L and the input impedance is referred to as floating impedance seen between port 1 and port 2 of the π-network. Therefore, the differential input impedance is given by:

$$R + jX = \left(-\frac{1}{Y_{12}}\right) \| \left(\frac{1}{Y_{11} + Y_{12}} + \frac{1}{Y_{22} + Y_{12}}\right) = \frac{Y_{11} + Y_{22} + 2Y_{12}}{Y_{11}Y_{22} - Y_{12}^2} \tag{12.15}$$

In this case, where the shunt elements $Y_{11} + Y_{12}$ and $Y_{22} + Y_{12}$, which are related to the substrate networks, can be neglected, L and Q can be calculated using:

$$L = \text{Im}\left(\frac{1/Y_{12}}{2\pi f}\right) = -\frac{1}{2\pi f \text{Im}(Y_{12})} \tag{12.16}$$

$$Q = \frac{\text{Im}\left(\frac{1}{Y_{12}}\right)}{\text{Re}\left(\frac{1}{Y_{12}}\right)} = -\frac{\text{Im}(Y_{12})}{\text{Re}(Y_{12})} \tag{12.17}$$

When the shunt elements $Y_{11} + Y_{12}$ and $Y_{22} + Y_{12}$ are not negligible, as in standard CMOS processes, the effective inductance L_{diff} and Q_{diff} are obtained using (12.19–12.19) [3].

$$R + jX = \frac{4}{Y_{11} + Y_{22} - Y_{12} - Y_{21}} \tag{12.18}$$

$$L_{\text{diff}} = \frac{\text{Im}\left(\frac{4}{Y_{11} + Y_{22} - Y_{12} - Y_{21}}\right)}{2\pi f} \tag{12.19}$$

$$Q_{\text{diff}} = -\frac{\text{Im}(Y_{11} + Y_{22} - Y_{12} - Y_{21})}{\text{Re}(Y_{11} + Y_{22} - Y_{12} - Y_{21})} \tag{12.20}$$

For symmetrical inductors, Y_{22} and Y_{21} are equal to Y_{11} and Y_{12}, respectively, such that Eqs. (12.21) and (12.22) are simplified as follows:

$$L_{\text{diff}} = \frac{\text{Im}\left(\frac{2}{Y_{11} - Y_{12}}\right)}{2\pi f} \tag{12.21}$$

$$Q_{\text{diff}} = -\frac{\text{Im}(Y_{11} - Y_{12})}{\text{Re}(Y_{11} - Y_{12})}. \tag{12.22}$$

12.6 Inductance Estimation

The inductance of a planar spiral inductor is a complex function which mainly depends on its geometry. An accurate estimation of the inductance can be made either by using expressions based on a numerical method or by using a field solver. There are two methods which may be used to calculate the inductance of a spiral using a closed-form equation. One of the basic methods is based on the self-inductance and the mutual coupling in single wires and is known as the greenhouse method. The other method relies on empirical equations applied for inductance calculations. A summary of comprehensive formulas is presented in [13], illustrating the tables for inductance estimation.

According to the greenhouse theory, the inductance of a square spiral inductor can be calculated by splitting up the different inductor sections into single wires. Then, the self-inductance of each wire is calculated and finally summed up. The self-inductance of a single wire with a rectangular cross section is given by the following equation [2]:

$$L_{\text{self}} = 2l \ln\left(\frac{2l}{w + t} + 0.5 + \frac{w + t}{3l}\right) \tag{12.23}$$

where L_{self} is the self-inductance in nH, the wire length l is in cm, w is the wire width in cm, and t is the wire thickness in cm. This equation is valid when the wire length is at least greater than twice the cross-sectional dimension. Additionally, to

calculate the overall inductance, the mutual inductance (positive or negative) between parallel lines is included. The mutual inductance between two parallel wires can be expressed as follows [14]:

$$M = 2lQ_m \tag{12.24}$$

where M is the mutual inductance in nH, l is the wire length in cm, and Q_m is the mutual inductance parameter which is calculated by (12.25):

$$Q_m = \ln\left(\frac{l}{\text{GMD}} + \sqrt{1 + \left(\frac{l}{\text{GMD}}\right)^2}\right) - \sqrt{1 + \left(\frac{\text{GMD}}{l}\right)^2} + \frac{\text{GMD}}{l} \tag{12.25}$$

where GMD is the geometric mean distance between the track center of the two wires and its exact value is given by:

$$\ln(\text{GMD}) = \ln(d) - \left[\frac{1}{12\left(\frac{d}{w}\right)^2} + \frac{1}{60\left(\frac{d}{w}\right)^4} + \frac{1}{168\left(\frac{d}{w}\right)^6} + \frac{1}{360\left(\frac{d}{w}\right)^8} + \cdots\right] \tag{12.26}$$

where d is the center to the center separation between the conductors and w is the width of the conductors. Thus, the inductance of a conductor is given by:

$$L_T = L_0 + M_+ - M_- \tag{12.27}$$

where L_T is the total inductance of the spiral inductor, L_0 is the sum of self-inductances, M_+ is the positive mutual inductance (where the current in two parallel segments is in the same direction), and M_- is the sum of the negative mutual inductance (where the current in two parallel wires is in the opposite direction) [2]. For instance, the inductance for a two-turn square spiral inductor shown in Fig. 12.9 can be calculated as follows:

$$\begin{aligned} L_T = {} & L_1 + L_2 + L_3 + L_4 + L_5 + L_6 + L_7 + L_8 \\ & + 2(M_{1,5} + M_{2,6} + M_{3,7} + M_{4,8}) \\ & - 2(M_{1,7} + M_{1,3} + M_{5,7} + M_{5,3} + M_{2,8} + M_{2,4} + M_{6,8} + M_{6,4}) \end{aligned} \tag{12.28}$$

where L_i is the self-inductance of wire i and M_{ij} is the mutual inductance between wires i and j.

The second method often used to estimate the inductance of a spiral coil is based on empirical equations. One such empirical equation is (12.29), which is based on the modified Wheeler formula [15] and is valid for planar spiral integrated inductors:

Fig. 12.9 Application of the greenhouse method to a two-turn square spiral inductor
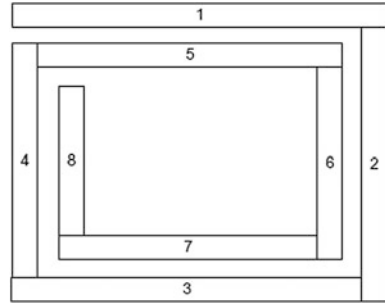
Table 12.1 Coefficients for the modified Wheeler expression

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

$$L_{\mathrm{mw}} = K_1\,\mu_0\,\frac{n^2\,d_{\mathrm{avg}}}{(1 + K_2\,\rho)} \qquad (12.29)$$

where L_{mw} is the inductance calculated by the modified Wheeler formula, the coefficients K_1 and K_2 are layout-dependent parameters presented in Table 12.1, n is the number of turns, d_{avg} is the average diameter defined as $d_{\mathrm{avg}} = 0.5(d_{\mathrm{in}} + d_{\mathrm{out}})$, and ρ is the filling ratio defined as $\rho = (d_{\mathrm{out}} - d_{\mathrm{in}})/(d_{\mathrm{out}} + d_{\mathrm{in}})$.

Another empirical expression is based on the current sheet approximation [15]. This method approximates the sides of the spirals by symmetrical current sheets of equivalent current densities. Since sheets with orthogonal current have zero mutual inductance, the inductance estimation is then reduced to just the evaluation of the self-inductance of a sheet and the mutual inductance between opposite current sheets. The self- and mutual inductances are established using the concepts of geometric mean distance (GMD), arithmetic mean distance (AMD), and arithmetic mean square distance (AMSD) [15]. The formula for this method is given by:

$$L_{\mathrm{gmd}} = \frac{\mu n^2 d_{\mathrm{avg}} c_1}{2}\ln((c_2/\rho) + c_3\rho + c_4\rho^2) \qquad (12.30)$$

where c_i are layout-dependent coefficients provided in Table 12.2. As the ratio s/w increases, the accuracy of this equation degrades exhibiting a maximum error of 8 % for $s \leq 3w$. Practical integrated spirals are designed $s \leq w$.

Table 12.2 Coefficients for the current sheet expression

Layout	c_1	c_2	c_3	c_4
Square	1.27	0.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

Table 12.3 Coefficients for the inductance monomial expression

Layout	β	α_1	α_2	α_3	α_4	α_5
Square	1.62×10^{-3}	−1.21	−0.147	2.40	1.78	−0.030
Hexagonal	1.28×10^{-3}	−1.24	−0.174	2.47	1.77	−0.049
Octagonal	1.33×10^{-3}	−1.21	−0.163	2.43	1.75	−0.049

The monomial expression is another empirical equation and it is based on a data-fitting technique which yields the following expression [15]:

$$L_{\mathrm{mon}} = \beta \, d_{\mathrm{out}}^{\alpha_1} \, w^{\alpha_2} \, d_{\mathrm{avg}}^{\alpha_3} \, n^{\alpha_4} \, s^{\alpha_5} \qquad (12.31)$$

where L_{mon} is the inductance in nH, d_{out} is the outer diameter in μm, n is the number of turns, and s is the turn-to-turn spacing in μm. The coefficients β and α_i are layout dependent and are given in Table 12.3. This expression can be solved using geometric programming which is an optimization method that applies monomial models.

Although the greenhouse method offers sufficient accuracy to estimate the inductance value [17], this method cannot provide a direct design for given specifications and it is a slow approach for a preliminary design. Additionally, simple inductor expressions may predict the correct order of magnitude of the inductance value, but they incur errors in the range of 20 % which is unacceptable for circuit design and optimization [17]. The three aforementioned empirical equations are accurate, with typical errors of 2–3 % [17]. Consequently, they present an excellent candidate for a design and synthesis tool. These equations can provide expressions for the inductance of square, hexagonal, octagonal and circular planar inductors.

Commercial 3D electromagnetic simulators can be used to estimate the inductance of planar spiral inductors, via the extracted Y-parameters of the two-port π-equivalent circuit model (refer to Sect. 12.5) using (12.32) [18]:

$$L_s = -\frac{1}{2\pi f} \mathrm{Im}\left(\frac{1}{Y_{12}}\right) \qquad (12.32)$$

where f is the frequency. The formulae used in the extraction of the inductor π-equivalent lumped circuit parameters are presented in [19]. The accuracy and limitations of such calculation are inherent to the inductor π-equivalent circuit model.

12.7 Boundary Conditions for the Spiral Inductor Optimization

The bounding of the layout parameters of the spiral inductor required for the optimization procedure can be expressed as follows [14]:

$$\text{maximize} \qquad Q(d_{\text{out}}, w, s, n)$$

$$
\begin{aligned}
\text{subject to} \quad & L_{s,\min} \leq L_s(d_{\text{out}}, w, s, n) \leq L_{s,\max} \\
& (2n+1)(s+w) \leq d_{\text{out}} \\
& d_{\text{out min}} \leq d_{\text{out}} \leq d_{\text{out max}} \\
& w_{\min} \leq w \leq w_{\max} \\
& s_{\min} \leq s \leq s_{\max} \\
& n_{\min} \leq n \leq n_{\max}
\end{aligned}
\qquad (12.33)
$$

where Q-factor is the objective function and d_{out}, w, s, and n are the optimization variables related to the spiral geometry, in which n is the number of turns, s is the track-to-track distance, and w is the track width. The domain of the design search space is determined by the lower and upper bounds of these variables. It is important to set these variables to restricted feasible values in order to reflect the limitations of the technology.

The geometry of the spiral inductor needs to be optimized in order to maximize its quality factor Q at a particular frequency. The inductance value is bounded by the first constraint. The boundary of the layout size is ensured by the second constraint. The other four constraints are the geometric constraints. Many optimization methods have been proposed to solve (12.33), such as the exhaustive enumeration, sequential quadratic programming (SQP), mesh adaptive direct search (MADS), genetic algorithm, and geometric programming (GP) [1]. Considering that the design parameters of the spiral inductor are independent from each other, it is important to constraint them together. The outer diameter can draw a correlation between n, w, and s governed by (12.34):

$$d_{\text{out}} = d_{\text{in}} + 2\,n\,w + 2(n-1)s \qquad (12.34)$$

where d_{in} is the inner diameter.

12.8 Optimization of Inductors via a Genetic Algorithm

A genetic algorithm (GA) optimization is a stochastic search method which replicates the natural biological evolution by applying the principle of survival of the fittest, in order to achieve the best possible solution to a given problem. In the context of integrated spiral inductor design, GA is being proposed as an adequate optimization tool since it does not rely on formal mathematical derivations or prior knowledge of the problem, is resistant to being trapped in local optima, and can handle noisy functions. In addition, GA has proven to be able to handle large variations within the boundary conditions and is able to search at specific point rather than at regions across the searched space [20].

The main principle behind the applied GA optimization is that it takes into consideration heuristic constraints regarding the inductor design. It offers a way to determine the various parameters of the inductor layout. Due to the technology and topology constraints, the layout parameters are inherently discrete and so discrete variable optimization techniques are used. In this chapter, two approaches are presented. In this section, the GA-based integrated inductor design is based on the lumped element two-port π-model (refer to Sect. 12.5) and the modified Wheeler formula given by (12.29) which is used to calculate the inductance value.

This approach can be implemented using the MATLAB GA toolbox in order to yield technology-feasible design parameters [21]. The design generated by this method can then be verified through an EM simulator. For the π-model inductor, the quality factor is defined as given by Eq. (12.22) and the evaluation of R_s, $R_{\mathrm{si}} = R_{\mathrm{sub}}$, $C_s = C_F$, C_{ox} and $C_{\mathrm{si}} = C_{\mathrm{sub}}$ can be obtained from Eqs. (12.3), (12.7), (12.4), (12.5), and (12.6), respectively. The shunt resistance R_p and capacitance C_P can be estimated by:

$$R_p = \frac{1}{\omega^2 C_{\mathrm{ox}}^2 R_{\mathrm{si}}} + \frac{R_{\mathrm{si}}(C_{\mathrm{ox}} + C_{\mathrm{si}})^2}{C_{\mathrm{ox}}^2} \tag{12.35}$$

$$C_p = C_{\mathrm{ox}} \frac{1 + \omega^2 (C_{\mathrm{ox}} + C_{\mathrm{si}}) + C_{\mathrm{si}} R_{\mathrm{si}}^2}{1 + \omega^2 (C_{\mathrm{ox}} + C_{\mathrm{si}})^2 R_{\mathrm{si}}^2} \tag{12.36}$$

The restricted technological constraints are defined as follows: minimum values for the track width w, track-to-track spacing s, and input diameter d_{in}. Moreover, the correlation between the layout parameters is considered as heuristic design rules for reducing the parasitic phenomena due to proximity effect [20] given by (12.37)

$$0.2 < d_{\mathrm{in}}/d_{\mathrm{out}} < 0.8, d_{\mathrm{in}} > 5w \tag{12.37}$$

For a GA optimization procedure, a cost function is required in which it formulates the optimization problem as follows (12.38):

$$
\begin{aligned}
\text{minimization of} \quad & \text{Cost}(n, d_{\mathrm{in}}, w) \\
\text{subject to} \quad & (1 - \delta)L_{\exp} \leq L_s(d_{\mathrm{in}}, w, n) \leq (1 + \delta)L_{\exp} \\
& w \in [w_{\min} : step_w : w_{\max}] \\
& d_{\mathrm{in}} \in [d_{\min} : step_d : d_{\max}] \\
& n \in [n_{\min} : step_n : n_{\max}]
\end{aligned}
\tag{12.38}
$$

where $\text{Cost}(n, d_{\mathrm{in}}, w)$ is the cost function, $L_s(n, d_{\mathrm{in}}, w)$ is the inductance of the spiral, $L_{\exp}$ is the targeted inductance value, and δ is the tolerance limit for the inductance, which is the value by which it may deviate from the targeting value.

There are three different scenarios that can be applied to the cost function at a particular frequency of operation: either the minimization of the tolerance δ, the minimization of the device area d_{out}, or else the maximization of the quality factor Q. In this work, the cost function is related to the maximization of the quality factor

Fig. 12.10 Block diagram of the numerical GA used for the design optimization of the spiral inductor
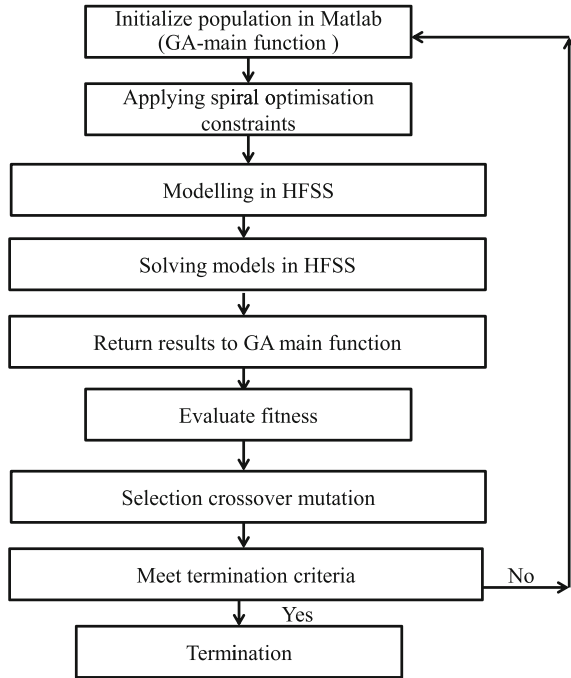
[20]. Initially, the GA optimization algorithm randomly generates the initial population. Each individual constitutes three variables (w, d_{in}, n), representing the layout geometry parameters. Each gene is formulated to real parameters, to abide to the objective boundaries' constraints. Following that, every quality factor and inductance of each particular gene (which refers to an inductor design) is evaluated. If these are not compliant, a fitness function is applied to pay a penalty so that it has a very low probability for being elected for the next population. If the termination condition is verified, the algorithm stops there, else the next steps create a new population, where selection and reproduction functions are used. For the selection, the roulette method is chosen, while afterward mutation is made. Figure 12.10 represents the flowchart of GA process to design the RFIC inductor.

To show the performance of the GA-based integrated inductor, an example of 1 nH square spiral inductor is shown. The technological parameters used to estimate R_{si}, C_s, C_{ox}, and C_{si} are shown in Table 12.4. The determination of the layout parameters is obtained through the constraints presented in Table 12.5. The GA optimization procedure was utilized to maximize the quality factor, given the tolerance for the required inductance. The result of GA optimization procedure is shown in Table 12.6.

The validity of the obtained design layout parameters was checked against a simulation performed using HFSS yielding the results shown in Table 12.7. The frequency response of the quality factor and inductance of the designed square

Table 12.4 Technology parameters

Parameter	Value	Parameter	Value
ε_0 (F/m)	8.85e−12	t_{ox} (μm)	11.8
ε_r	11.9	C_{sub} (F/m^2)	4.0e−6
σ (S/m)	2.7e−7	G_{sub} (S/m^2)	2.43e−5

Table 12.5 Design constraints

Parameter	Min	Max
w_{in} (μm)	2	20
d_{in} (μm)	70	90
n	2	7

Table 12.6 GA optimization results

w_{in} (μm)	d_{in} (μm)	n	N
15	48	2.5	4

Table 12.7 Comparison of estimated and simulated results

$L_{GA}(nH)$	L_{HFSS} (nH)	Error (%)	Q_{GA}	Q_{HFSS}	Error (%)
1.2	1.15	4.2	6.8	7.2	5.8

Fig. 12.11 Variation of the inductor's quality factor with frequency obtained using HFSS
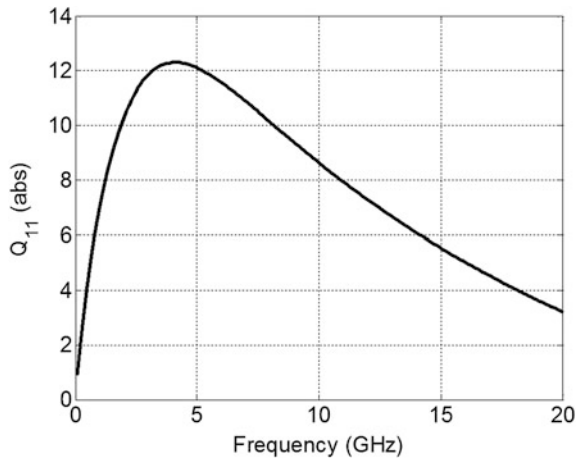
inductor are inductor is illustrated in Figs. 12.11 and 12.12, respectively. The inductor HFSS design model generated model is depicted in Fig. 12.13. The comparison between the HFSS simulation results and the GA estimations demonstrates a good agreement, where the GA inductance value is 1.2 nH and the simulations predict an inductance of 1.15 nH. The Q estimated via the GA is 6.8, while the simulations show that the inductor exhibits a Q of 7.2.
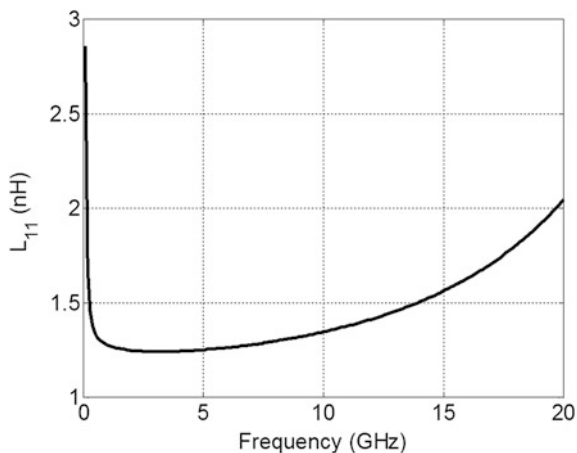
Fig. 12.12 Variation of the inductance with frequency obtained using HFSS
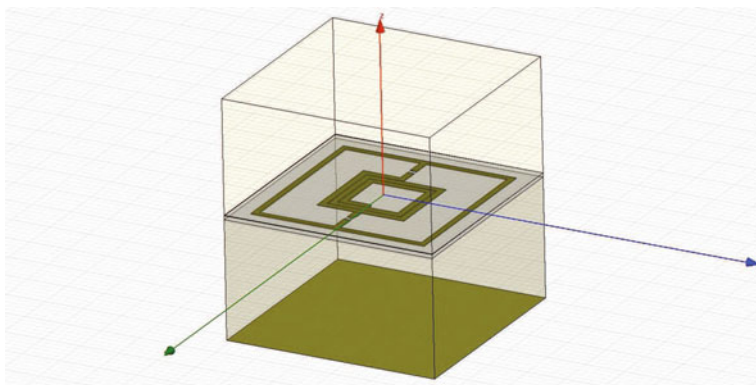

Fig. 12.13 HFSS square spiral inductor model

12.9   Optimization of Inductors via Geometric Programming

Geometric programming (GP) has a significant feature of determining if a design is feasible and if so finding the best possible inductor layout parameters [2]. Its main advantage is that it relates the sensitivity of the design objectives to its constraints, thus offering a rapid searching tool which enables the RFIC designer to spend more exploring and tuning the fundamental design trade-offs.

A GP problem has a form

$$
\begin{aligned}
\text{minimize} \quad & f_0(x) \\
\text{subject to} \quad & f_i(x) \le 1, i = 1, 2, \ldots, m, \\
& g_i(x) = 1, i = 1, 2, \ldots, p, \\
& x_i > 0, i = 1, 2, \ldots, n,
\end{aligned}
\tag{12.39}
$$

where $f_i(x)$, $i = 0, 1, \ldots, m$, are posynomial functions and $g_i(x)$, $i = 1, 2, \ldots, P$, are monomial functions. The posynomial function is defined as

$$
f(x_1, \ldots, x_n) = \sum_{k=1}^{t} c_k x_1^{\alpha_{1k}} x_2^{\alpha_{2k}} \ldots x_n^{\alpha_{nk}}
\tag{12.40}
$$

where $c_j \ge 0$ and $\alpha_{ij} \in R$. When $t = 1$, f is called a monomial function. Thus, for example, $0.7 + 2x_1/x_3^2 + x_2^{0.3}$ is a posynomial and $2.3(x_1/x_2)^{1.5}$ is a monomial. Posynomials are closed under sums, products, and nonnegative scaling.

Indeed, an initial point is unnecessary for it has no effect on the optimization algorithm procedure. The GP problem is solved globally and efficiently, converting it into a convex optimization problem. This is specifically done through the transformation of the objective and constraint functions using a set of new variables defined as $y_i = \log x_i$, such that $x_i = e_i^{y_i}$ [22]. For a monomial function f given by (12.41)

$$
f(x) = c_1 \, x_1^{\alpha_{1k}} \, x_2^{\alpha_{2k}} \ldots x_n^{\alpha_{nk}}
\tag{12.41}
$$

Then,

$$
\begin{aligned}
f(x) &= f(e^{y_1}, \ldots, e^{y_n}) \\
&= c(e^{y_1})^{a_1} \ldots (e^{y_n})^{a_n} \\
&= e^{a^T(y+b)}
\end{aligned}
\tag{12.42}
$$

where $b = \log c$.

Using the variable $y_i = \log x_i$ transforms a monomial function to an exponential form of an affine function, as follows:

$$
f(x) = \sum_{k=1}^{K} e^{a_k^T y + b_k}
\tag{12.43}
$$

where $a_k = (a_{1k}, \ldots, a_{nk})$ and $b_k = \log c_k$. Hence, a posynomial can be changed to a sum of exponentials of affine functions, and the GP problem is expressed in terms

of the new variable y. Then, the objective and constraint functions are transformed by taking the logarithm resulting in a convex optimization form

$$
\begin{aligned}
\text{minimize} \quad & \overline{f}_0(y) = \log\left(\sum_{k=1}^{K_0} e^{a_{0k}^T y + b_{0k}}\right) \\
\text{subject to} \quad & \overline{f}_i(y) = \log\left(\sum_{k=1}^{K_i} e^{a_{ik}^T y + b_{ik}}\right) \leq 0, \quad i = 1, \ldots, m \\
& \overline{h}_i(y) = g_i^T y + h_i = 0, \quad i = 1, \ldots, p.
\end{aligned}
\tag{12.44}
$$

where the functions $\overline{f}_0(y)$ are convex and $\overline{h}_i$ are affine. Hence, this problem is referred to as geometric programming in convex form.

The formulation of spiral inductor optimization problem as a GP optimization problem was presented in [16], based on the monomial expression for inductance introduced in [15]. According to two-port lumped element circuit model, the monomial expression for the inductance is represented in terms of geometrical parameters $(d_{\text{out}}, w, d_{\text{avg}}, n$ and $s)$ [16], which has the form given by 31 [15].

Where the series resistance can be formulated as

$$
R_s = \frac{l}{\sigma w \delta(1 - e^{-t/\delta})} = 4 f(\omega) k_1 d_{\text{avg}} n / w
\tag{12.45}
$$

The spiral–substrate oxide capacitance C_{ox} that takes into consideration inductor's parasitic capacitance is given by the following monomial expression:

$$
C_{\text{ox}} = \frac{\varepsilon_{\text{ox}} l w}{2 t_{\text{ox}}} = 4 k_2 d_{\text{avg}} n w
\tag{12.46}
$$

The series capacitance C_s that represents the capacitance between the spiral and the metal underpass required to connect the inner end of the spiral inductor to external circuitry. It is specified as a monomial expression

$$
C_s = \frac{\varepsilon_{\text{ox}} n w^2}{t_{\text{ox},M1-M2}} = k_3 n w^2
\tag{12.47}
$$

where $t_{\text{ox},M1-M2}$ is the oxide thickness between the spiral and the underpass.

The substrate capacitance C_{si} that refers to the substrate resistance can be modeled as a monomial equation

$$
C_{\text{si}} = \frac{C_{\text{sub}/A} l w}{2} = 4 k_4 d_{\text{avg}} n w
\tag{12.48}
$$

The monomial expression of the substrate resistance is R_{si}

$$R_{si} = \frac{2}{G_{sub/A} l\, w} = k_5/(4\, d_{avg}\, n\, w) \tag{12.49}$$

where L_s is the inductance in nH, d_{out} is the outer diameter in μm, n is the number of turns, s is the turn-to-turn spacing in μm, k_1 to k_5 are coefficients dependent on technology, and $f(\omega)$ is the coefficient dependent on frequency and technology

$$f(\omega) = \frac{1}{\sqrt{\frac{2}{\omega \mu_0 \sigma}}(1 - e^{-t/\sqrt{2/(\omega \mu_0 \sigma)}})} \tag{12.50}$$

The shunt resistance R_p and capacitance C_p are frequency dependent, expressed as monomials as follows:

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{C_{ox}^2} = k_6/(4 * d_{avg}\, n\, w) \tag{12.51}$$

$$C_p = C_{ox}\frac{1 + \omega^2(C_{ox} + C_{si}) + C_{si}R_{si}^2}{1 + \omega^2(C_{ox} + C_{si})^2 R_{si}^2} = 4k_7\, d_{avg}\, n\, w \tag{12.52}$$

where k_6 and k_7 are coefficient dependent on technology and frequency. According to the π-model, the quality factor of a spiral inductor accounting for substrate loss factor and self-resonance factor is given by

$$Q_L = \frac{\omega L_s}{R_s} \cdot \frac{\overline{R_p}\left(1 - \frac{R_s^2 \overline{C_{tot}}}{L_s} - \omega^2 L_s \overline{C_{tot}}\right)}{\overline{R_p} + \left[\left(\frac{\omega L_s}{R_s}\right)^2 + 1\right]R_s} \tag{12.53}$$

where $\overline{R_p} = 2R_p$ and $\overline{C_{tot}} = C_{tot}/2$ for two-port device, while for one-port device, it is $\overline{R_p} = R_p$ and $\overline{C_{tot}} = C_{tot}$. When the inductor is used as one-port inductor, the total shunt capacitance is posynomial $C_{tot} = C_s + C_p$ because C_s and C_p are monomial expressions. The quality factor represents the objective function in GP and can not be as a posynomial function of the design parameters. By introducing a new variable, the specification for minimum quality factor ($Q_L \geq Q_{L,min}$) was written in [16] as a posynomial inequality in the design variables and $Q_{L,min}$

$$\frac{Q_{L,min}R_s}{\omega L_s \overline{R_p}} \cdot \left[\overline{R_p} + \frac{(\omega L_s)^2}{R_s} + R_s\right] + \frac{R_s^2(C_s + C_p)}{L_s} + \omega^2 L_s(C_s + C_p) \leq 1 \tag{12.54}$$

This is because only inequality constraints in monomial form are allowed in GP. Accordingly, the GP design problem is formulated as

$$
\begin{aligned}
\text{maximize} \quad & Q_{\min} \\
\text{s.t.} \quad & Q \geq Q_{\min} \\
& L = L_{\text{req}}, L_{s,\min} \leq L_s \leq L_{s,\max} \\
& (2n + 1)(s + w) \leq d_{\text{out}} \\
& d_{\text{ang}} + n(s + w) \leq d_{\text{out}} \\
& d_{\text{out min}} \leq d_{\text{out}} \leq d_{\text{out max}} \\
& w_{\min} \leq w \leq w_{\max} \\
& s_{\min} \leq s \leq s_{\max} \\
& n_{\min} \leq n \leq n_{\max}
\end{aligned}
\tag{12.55}
$$

Since the design parameters d_{out}, w and s are independent, an inequality constraint to correlate them together $d_{\text{ang}} + n(s + w) \leq d_{\text{out}}$ has been imposed. Also, the inductor area can be constrained by using the monomial inequality, $d_{\text{out}}^2 \leq A_{\max}$. The minimum self-resonant frequency can be handled by adding the following posynomial inequality:

$$
\omega_{\text{sr},\min}^2 L_s \overline{C_{\text{tot}}} + \frac{R_s^2 \overline{C_{\text{tot}}}}{L_s} \leq 1.
\tag{12.56}
$$

Yet, there are some cases that apply PGS beneath the inductor to eliminate the resistive and capacitive coupling to the substrate at the expense of the increased oxide capacitance. Hence, the inductor exhibits an improvement in its performance. In this case, the inductor lumped model parameters become $R_p = \infty$, $C_p = C_{\text{ox}} = (\varepsilon_{\text{ox}} \, l \, w)/(2t_{\text{ox,po}})$, where $t_{\text{ox,po}}$ is the oxide thickness between the spiral and the polysilicon layer.

A simple MATLAB toolbox for solving geometric programming problems is proposed in [23]. This toolbox can be used to evaluate Eq. (12.55) and find feasible optimal parameters to model spiral inductors via geometric programming optimization method.

An optimal design of a 1-nH spiral inductor using the GP optimization is presented here, where the GP optimization tool maximizes the Q-factor for the inductor operating at 1 GHz. The GP tool was presented with the following constraints: Maximize μm subject to $L_s = 1$ nH, $s \geq 2$ μm, $\omega_{\text{sr}} \geq 10$ GHz.

Figure 12.14 illustrates the maximum Q-factor for 1-nH square inductor at 1 GHz without PSG, as a result of the GP optimization method. The corresponding geometrical dimensions are all in a feasible technological range, shown in Table 12.8. In order to verify GP results, commercial FEM simulation software of HFSS was used with the layout parameters depicted in Table 12.8. The results of HFSS verification are presented in Table 12.9, which show a very good agreement
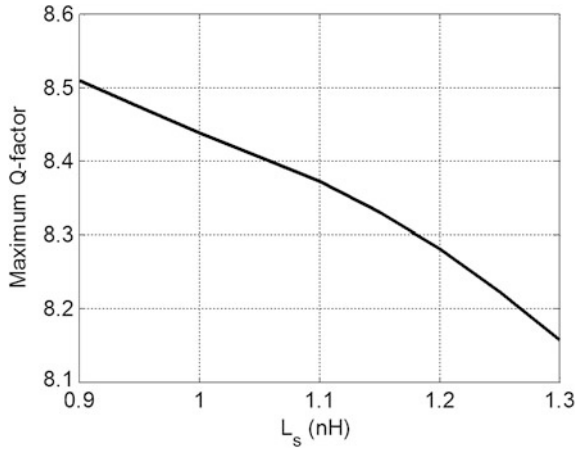
Fig. 12.14 Variation of the maximum quality factor with inductance

Table 12.8 Maximum Q-factor and optimal value of geometry parameters for the 1-nH square inductor

L_s (nH)	d_{out} (μm)	w (μm)	d_{avg} (μm)	n	s (μm)
1	167.3	17	110	2.5	2

Table 12.9 Comparison of the estimated and simulated results obtained using HFSS

L_{GP} (nH)	L_{HFSS} (nH)	Q_{GP}	Q_{HFSS}
1	1.1	6	7.3

with the GP estimated results. The GP algorithm gave an inductance of 1 nH with a Q-factor of 8.4, while HFSS reported that the designed inductor exhibits an inductance of 1.1 nH with a Q-factor of 7.3. The HFSS square spiral model is shown in Fig. 12.15.

Fig. 12.15 Geometry of a square spiral inductor in HFSS
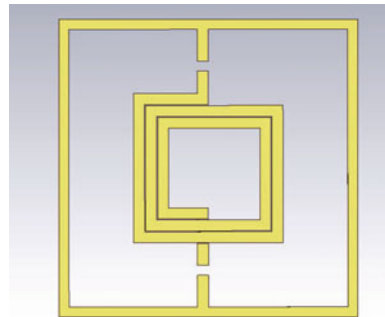
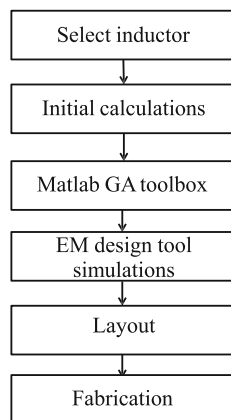## 12.10 Genetic Algorithm Optimization Using EM Solvers

The implementation of integrated spiral elements relies on approximate quasi-static models that need to be verified by electromagnetic field solvers. The design of RF spiral inductors can be accomplished by integrating the use of a 3D electromagnetic (EM) solver together with an optimization method. A 3D EM solver is a CAD tool which can be used to compute multiport parameter data for a particular RF structure by using 3D electromagnetic field simulation. In this work, a new methodology of using the GA optimization MATLAB toolbox integrated with HFSS is presented, in order to demonstrate the implementation of an optimal RF CMOS inductor design. The proposed design procedure for the RFIC inductor is summarized in Fig. 12.16.

As discussed in Sect. 12.5, Q and L can be easily evaluated by simulating the inductor spiral and extracting the Y-parameters. However, Q is very sensitive to the simulation settings and environment. For an accurate determination of the Q value, the internal parts of the conductors should be finely meshed in order to account for the exponential decay of the current inside the conductors. The optimization boundary constraints employed in this approach are based on the set presented in (12.38), and a GA optimization is scripted so as to implement a spiral inductor. Using the extracted Y-parameter data, Q and L are estimated, and the results are automatically sent to the GA main function. A cost function is defined in order to eliminate genes with a low probability of achieving a maximum Q given by (12.57).

$$F(f) = \begin{cases} -Q, & \text{for } Q \geq 2 \\ 0, & \text{for } Q < 2 \end{cases} \qquad (12.57)$$

To restrict the inductance value during the optimization procedure, a bounding condition is defined before calling the fitness function:

**Fig. 12.16** Design flow for an RFIC inductor

- Select inductor
- Initial calculations
- Matlab GA toolbox
- EM design tool simulations
- Layout
- Fabrication

$$
\begin{cases}
\text{if } (1 - \delta) \, L_{\text{exp}} \leq L_s(d_{\text{in}}, \, w, \, N, \, n) \leq (1 + \delta) \, L_{\text{exp}} \\
Q_L = -\dfrac{\text{Im}(Y_{11} - Y_{12})}{\text{Re}(Y_{11} - Y_{12})} \\
\text{else} \\
Q = 0
\end{cases}
\tag{12.58}
$$

An optimum spiral inductor designed for a given inductance value at a particular operating frequency is targeted for a maximum Q and a minimum area consumption with an adequate self-resonant frequency. The physical characteristics of an inductor, such as the metal width w, outer diameter d_{out}, spacing s, and the number of turns n, are optimized in order to yield the required inductor. In addition, it was imperative to take into consideration the guidelines presented in Sect. 12.4. In practice, the values of on-chip inductors used in RF circuits fall in the range of 1–10 nH due to considerations in area utilization.

The CMOS process is modeled by drawing the substrate and the metal layers in a 3D-box-like fashion, where each layer is defined by its relative permittivity and bulk conductivity. The inductor layout is drawn by scripting HFSS commands through MATLAB using a library proposed in [24]. Figure 12.17 illustrates the main parameters of the generic CMOS process used in the simulations. The spiral is implemented using the top metal layer, and the underpass is made from the next metal layer level. A ground ring was added connecting each port of the inductor.

The block diagram of the genetic algorithm function used in this procedure is shown in Fig. 12.18. As a starting point of the optimization process, the initial population is created randomly, in which binary strings are generated from layout parameters. The GA is implemented in a way to code these layout parameters into genes via a binary-string coding. The four optimized parameters are s, w, n, and d_{in}, such that the chromosome structure is a four-part string, where each string

Fig. 12.17 Layers in a generic CMOS process
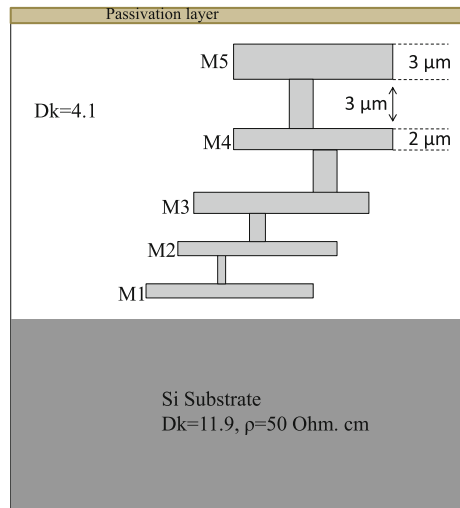
Fig. 12.18 Block diagram of the genetic algorithm used for the design optimization of the spiral inductor
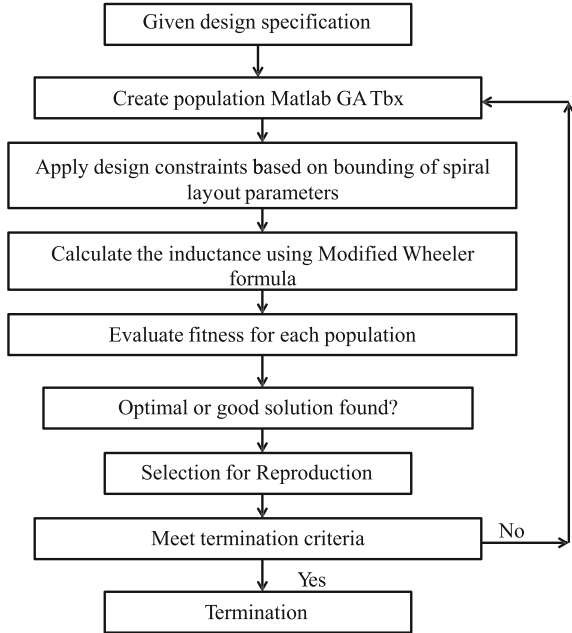
corresponds to a parameter. The model is then created in HFSS according to the decoded parameters and is used to estimate the *Y*-parameters. The inductance is then evaluated using Eq. (12.21), while abiding to the condition given by (12.58). Following that, the algorithm automatically returns the *Q* value to the main function which applies the fitness function given by (12.57) to each individual in the GA population. Successive generations are produced by the application of selection, crossover, and mutation operators, until the optimal or a relatively optimal solution is found or termination criterion is met.

The 3D tool improves the design methodology of the on-chip inductors. Though it provides full freedom in implementation, it shows to be slower tool due to modeling through geometric construction and it uses the finite element method which requires many iterations in order to achieve convergence [18]. A relation was used to account for the accuracy in the quality factor estimated from the HFSS simulation results [25], where a cross-sectional solver was used to estimate the losses in coupled transmission lines, thus correcting the estimation.

The proposed optimization methodology is demonstrated through the design of a rectangular spiral inductor targeted for an operating frequency of 1 GHz. The design constraints and the technology parameters are given in Tables 12.10 and

Table 12.10 Optimization constraints

Parameter	Values
Desired inductance	1 nH
Operating frequency	1 GHz
Outer diameter	≤400 μm

Table 12.11 Technology parameters

| Parameter	Values
Substrate resistivity	10 Ω cm
Silicon dielectric constant	11.9
Oxide thickness	4.5 μm
Conductivity of the metal	2.8×10^5 $(\Omega$ cm$)^{-1}$
Metal thickness	3 μm

12.11. The determination of the upper and lower bounds of the width w, the number of turns n, and spacing s is based on an initial estimation of the inductance and layout parameters from the GP optimization; hence, a sweep is performed around these values. The GP optimization layout design parameters used in this example are those given in Table 12.8. The number of turns was varied from 2 to 4, w from 10 to 20 μm, while d_{in} from 40 to 70 μm.

The parameters of the square inductor design are given in Table 12.12, while the simulation results obtained from HFSS are illustrated in Figs. 12.19 and 12.20, where the variation of the inductance and quality factor with frequency is reported. The value of the quality factor and the inductance obtained from this procedure are compared with those obtained from the GP optimization procedure in Table 12.13.
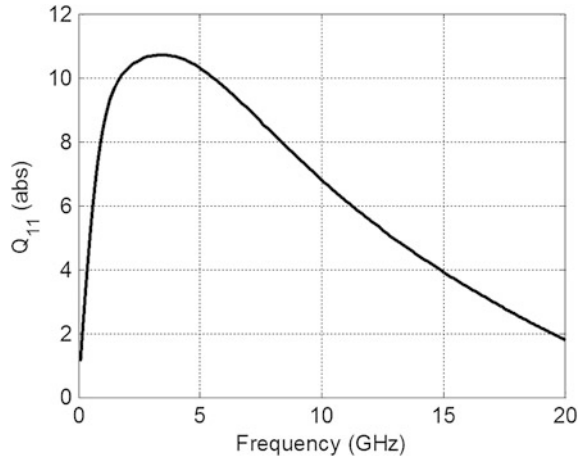
Table 12.12 Optimization constraints

Parameter	Values
w	17 μm
s	2 μm
n	2.5
d_{in}	65 μm

Fig. 12.20 Variation of the inductance with frequency obtained using HFSS
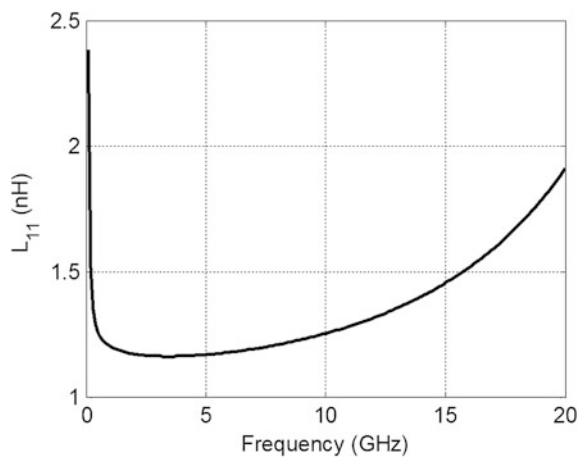
Fig. 12.19 Variation of the
inductor's quality factor with
frequency obtained using
HFSS

Table 12.13 GA
optimization results

$L_{\text{GA-HFSS}}$ (nH)	L_{GP} (nH)	$Q_{\text{GA-HFSS}}$	Q_{GP}
1.1	1	6.5	6

12.11   Conclusion

In this chapter, computational techniques employed to model and optimize radio
frequency on-chip spiral inductors on a silicon substrate were presented and dis-
cussed. This work presents an efficient tool for analyzing, designing, and imple-
menting any arbitrary inductor arrangement or topology. The optimization strategy
is initialized by using a set of empirical formulae in order to estimate the physical
parameters of the required structure as constrained by the technology, layout, and
design specifications. Then, automated optimization using numerical techniques,
such as genetic algorithms or geometric programming, is executed to further
improve the performance of the inductor by means of dedicated software packages
such as MATLAB. The optimization process takes into account substrate coupling,
current constriction, and proximity effects. The results of such an optimization are
then verified using a 3D EM simulator. This strategy was shown to be convenient in
synthesizing optimal spiral inductors with adequate performance parameters such as
the quality factor, area utilization, and self-resonant frequency, by combining
lumped element model estimation with computational techniques within an EM
simulation environment. This strategy provides a time-efficient and accurate design
flow. A further improvement to this work would be to incorporate a method for
correcting the inaccuracy of the EM simulators in calculating the quality factor of
the spiral inductors.

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