Chapter 13
Semiconductor Growth Techniques and Device Fabrication

Abstract This chapter presents a brief outline of the technology associated with semiconductor processing. The production of highly pure electronic-grade silicon from raw feedstock is presented. Different techniques of semiconductor crystal growth are given. Czochralski (CZ) method and Bridgman method are explained. Zone refining process is also described. Semiconductor fabrication technology, and thin film micro-electronic circuit fabrication are presented. Preparation of wafers, epitaxy, masking, photolithography, interconnection by metalizing are discussed. Methods of ion-implantation, molecular beam epitaxy (MBE), sputtering and etching are explained. Semiconductor p–n junction (diode) formed by different methods, are described. Stepwise procedure for the formation of a semiconductor p–n junction, and transistor manufacturing processes (of grown junction, alloy formation, diffusion) are briefly narrated. Minute insight into the various topics are given through solved numerical and theoretical examples. Review questions, numerical problems and objective type questions are also given with their answers.

Keywords Production of EGS · Crystal growth · Bridgman method · Czochralski method · Zone refining · Micro-electronic circuit construction · Wafer manufacturing · Ion-implantation · Epitaxy · Sputtering · Masking · Photo-lithography · Etching · Fabrication of p–n junction · Transistor manufacturing process

13.1 Introduction

A large number of processes are involved in the fabrication of semiconductor materials and devices. For example, the semiconductor to be used is prepared in single-crystal form and then is purified to electronic grade. The semiconductor crystal growth is accomplished by using different techniques. It is sliced into wafers that are further processed to obtain defect-free and highly polished surfaces. Subsequently, desired impurities are introduced into selected regions of a wafer, sometimes in conjunction with oxidation and masking, and sometimes without these to form appropriate junctions. This step is then followed by a metallization

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process to realize ohmic contacts, separation of devices into individual dies, lead attachment, and device encapsulation (packaging).

13.2 Production of Element Form of Silicon (Si)

The raw feedstock for Si crystal is silicon dioxide (SiO_2). SiO_2 is reacted with *C* in the form of coke in an arc furnace at very high temperatures (≈1800 °C) to reduce SiO_2 according to the following reaction:

$$SiO_2 + 2C \rightarrow Si + 2CO \tag{13.1}$$

This forms the metallurgical grade Si (MGS) which has impurities such as Fe, Al and heavy metals at levels of several hundred to several thousand parts per million (ppm). It is worth mentioning that 1 ppm of Si corresponds to an impurity level of $5 \times 10^{16}/cm^{+3}$. While the MGS is clean enough for metallurgical applications such as using Si to make stainless steel, it is not pure enough for electronic applications. It is also not a single crystal.

The MGS is refined further to yield semiconductor-grade or electronic-grade Si (EGS), in which the levels of impurities are reduced to parts per billion or ppb (1 ppb = $5 \times 10^{13}/cm^{+3}$). This involves reacting the MGS with dry HCl according to the following reaction to form trichlorosilane, $SiHCl_3$, which is a liquid having boiling point of 32 °C.

$$Si + 3HCl \rightarrow SiHCl_3 + H_2 \tag{13.2}$$

Along with $SiHCl_3$, chlorides of impurities such as $FeCl_3$ are also formed which fortunately have boiling points that are different from that of $SiHCl_3$. This allows a technique called fractional distillation to be used, in which the mixture of $SiHCl_3$ and the impurity chlorides is heated, and condense the vapours in different distillation towers held at appropriate temperatures. Thus the pure $SiHCl_3$ is separated from the impurities. $SiHCl_3$ is then converted to highly pure EGS by reaction with H_2,

$$2SiHCl_3 + 2H_2 \rightarrow 2Si + 6H \tag{13.3}$$

13.3 Semiconductor Bulk and Thin Films Growth Technologies

The semiconductor crystal growth using various techniques ranging from bulk crystal growth to the epitaxial growth of quantum dots include the following.

- Liquid-encapsulated Czochralski (LEC),
- Horizontal Bridgman (HB),
- Liquid-encapsulated Kyropoulos (LEK), and
- Vertical gradient freezing (VGF) methods.

There are also many improved methods available for the growth of bulk semiconductor crystals. For example,

- Magnetic LEC
- Direct synthesis LEC
- Pressure-controlled LEC, and
- Thermal baffle LEC methods are all variations of the original LEC technique, but with improved growth conditions.

Other bulk growth techniques include

- Dynamic gradient freezing,
- Horizontal gradient freezing,
- Magnetic LEK, and
- Vertical Bridgman methods.

The widely used epitaxial growth techniques are

- Molecular beam epitaxy (MBE)
- Metal-organic chemical vapour deposition (MOCVD), and
- Liquid-phase epitaxy (LPE).

The term epitaxy is of Greek origin and is composed of two words, epi (placed or resting on), and taxis (arrangement). Thus, epitaxy refers to the formation of single-crystal films on top of a substrate.

The growth techniques of bulk semiconductor crystals are designed to produce large-volume crystals under equilibrium conditions with almost no flexibility in the production of alloy composition. The ability of bulk semiconductor growth techniques to produce large single crystals that can be cut into submillimeter-thick wafers, subsequentially to be used for epitaxial growth, is invaluable.

Preparing wafers from the boules is called the wafering process and includes slicing, lapping, polishing, and cleaning. Since most wafers are used as substrates for epitaxial growth, the wafering process and the bulk crystal growth are very important for successful epitaxial growth. For many epitaxial growths, wafers can be used without any treatment prior to the growth. There are many technologies available to prepare ready-to-use wafers. For example,

(i) thermal oxidation and/or ultraviolet/ozone oxidation processes have been effective in producing thin oxide layers, which protect the wafer surface. These oxide layers can be removed by heating prior to epitaxial growth.
(ii) Packaging the wafers in nitrogen gas is an effective method used to reduce residual oxidation of polished surfaces during storage.

Semiconductor alloys, heterojunctions, and other quantum structures such as superlattices are currently grown by two main epitaxial growth techniques, namely, MBE and MOCVD. These growth techniques enable the synthesis of high-quality single-crystal thin film deposited layer by layer on suitable substrates.

13.4 Semiconductor Crystal Growth

Element form of Si and Ge are obtained by chemical decomposition of compounds such as $SiCl_4$, $SiHCl_3$ and GeO_2 etc. After isolation from these compounds, the Si and Ge are purified. They are melted (melting points of Si is 1410 °C and that of Ge is 937 °C) and then casted into ingots. When the casted ingots are cooled down, the Si and Ge are obtained in poly-crystalline form. It is now the turn of crystal growth. For growth of a single crystal, a very careful control has to be maintained at the boundary of 'solid form of material during cooling' and 'molten material'. Different methods are adopted for growth of crystals from molten material. These are listed below.

1. Bridgman method (or the method of growth from the melt)
2. Czochralski (CZ) method
3. Floating zone method

These three methods will be described now in subsequent sections.

13.4.1 Bridgman Method

Common technique for growing single crystal from the melt involves selective cooling of molten material so that the solidification occurs along a particular crystal direction as shown in Fig. 13.1. Here the silica crucible containing molten Si or Ge is pulled slowly through the furnace. Consequently, the solidification begins at one end and slowly proceeds down the length of the bar. To increase crystal growth, a

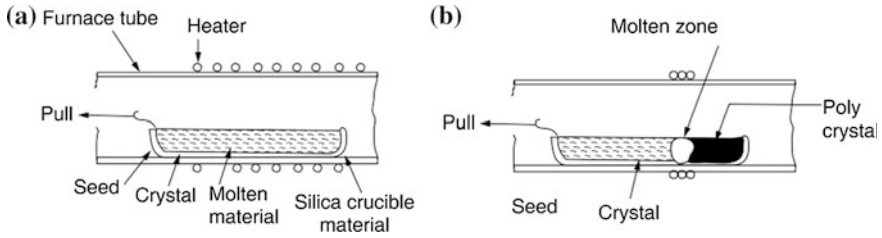

Fig. 13.1 Bridgman method of crystal growth from the melt in a crucible. Reproduced with permission from [1]

small seed crystal is placed at the end which is cooled first. Ge, GaAs and other semiconductor crystals are grown using this method.

As shown in Fig. 13.1b, a small region of polycrystalline material is melted and the molten zone is moved down the crucible at such a rate that a crystal is formed behind the zone, as it moves. This method is not suitable for growth of Si, as it has high melting point and sticks to the crucible.

13.4.2 Czochralski Method

In this method, a seed crystal is lowered down into molten material and is raised slowly, allowing the crystal to grow on to the seed. The crystal is rotated slowly as it grows to provide slight stirring of the melt and to correct any temperature variation. This arrangement is shown in Fig. 13.2.

The polysilicon material is kept in either a quartz or a graphite crucible and is melted by heating. The crystal growth is started by dipping a seed of single-crystal silicon into the melt. The seed is suspended over the crucible in a holder attached to a rotating arm and is inserted into the melt by lowering the arm. As the bottom of the seed begins to melt, the downward motion of the arm is reversed. The crystal is then pulled from the melt by slowly rotating and lifting the seed as the crystal grows at its lower end. The arm continues its upward movement forming a larger crystal. The crystal growth terminates when the melt in the crucible is depleted. During the pulling, provision is made to rotate the crucible. This provides stirring of the melt and avoids asymmetries in the heating. Material with desired impurity concentration is obtained by adding appropriate impurities to the melt prior to crystal growth. The atmosphere around the crystal puller is made inert by enclosing the entire assembly in a chamber that is flushed with an inert gas such as argon.

The CZ technique can also be used to grow single crystals of Ge, GaAs, and other compound semiconductors. In pulling crystal of a semiconductor such as GaAs from the melt, it is necessary to prevent volatile As atoms from vapourizing.

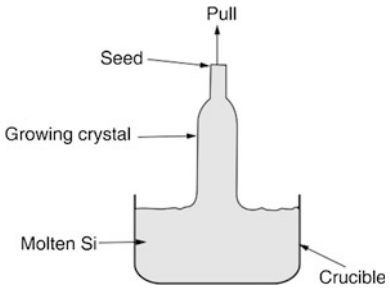

Fig. 13.2 Czochralski method of crystal growth. Reproduced with permission from [1]

13.4.3 Float Zone Method

The float zone (FZ) process shown in Fig. 13.3, uses a rod of ultrapure polycrystalline Si. The rod is maintained in a vertical position with the help of two chucks and is enclosed in a chamber in which an inert atmosphere is maintained by a flow of argon. An rf (radio frequency) heater coil is placed around the chamber. A single-crystal seed is clamped at the lower end of the rod, which is rotated around its axis during the growth process. The coil melts a small length of the rod starting with the seed crystal. The molten zone is then slowly moved upward along the length of the rod by moving the rf coil. As the coil is moved upward, recrystallization of the molten zone at the bottom occurs while the new material begins to melt at the top. The recrystallized region assumes the crystal structure of the seed. The molten zone is held together by surface tension of the liquid. The diameter of the growing crystal is controlled by the motion of the heater coil. The desired impurity level is obtained by starting with an appropriately doped polycrystalline material.

Comparison of FZ method with CZ process. The absence of a crucible in the FZ process offers many advantages over the CZ process. Not only is impurity contamination from the walls of the crucible eliminated, but also many volatile impurities can be removed by crystal growth in reduced atmospheric pressure. However, it is difficult to obtain large-diameter crystals using this method.

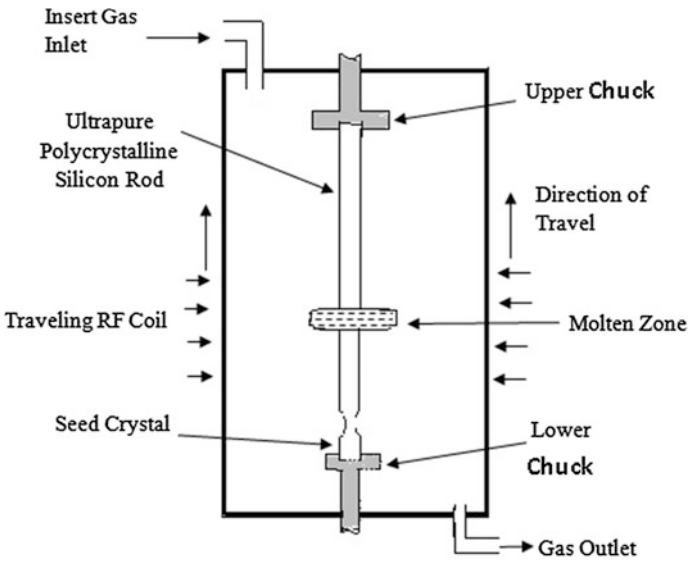

Fig. 13.3 Arrangement of a typical float zone system. Modified from [2] and self drawn

13.5 Processing of Semiconducting Materials

We have discussed earlier that a ppm (parts per million) addition of impurity (dopant) alters the electrical conductivity of semiconductors tremendously, hence this addition has to be minutely controlled to get a refined quality of extrinsic semiconductor. This necessitates an effective application of different refining techniques. The semiconductors can be refined by zone refining method. The *Zone refining* method is based on phase separation. Ultrapure single crystal silicon can be produced by this method.

13.5.1 Zone Refining Process

Although it is necessary to have acceptor or donor impurities, yet a practical semiconductor must be as far as possible chemically pure and crystallographically perfect. Thus, the *p–n* junction should occur in a single crystal because a grain boundary at the junction might contribute extra levels, thereby can complicate the matters. Recombination centres traps, and local distortion of the band structure may exist around a grain boundary. If a *p–n* junction occurs at a grain boundary, the operation of rectification is hindered or prevented.

Dislocations also have similar effects. In transistor materials, the lifetime of excess minority carriers should be as large as possible because, the operation of transistors depends on minority carrier injection across the base from the emitter base junction, to the base collector junction. If the excess minority carriers are arrested in their passage through the base by traps or recombination centres, the transistor operation is impossible. Impurities and imperfections are, therefore, highly undesirable. For practical purposes, it is also advantageous to control the resistivity of the material.

The level of undesirable impurities must, therefore, be of the order of parts per billion (ppb) before the donor is added, if real control of resistivity is so achieved. To attain the highest purity possible, zone refining is employed after chemical processing. Without zone refining, very little transistor grade material would be available. The zone refining process is based on the segregation of dissolved impurities during *non-equilibrium solidification.* Figure 13.4 describes the zone-refining process in nearly pure material where only one impurity is present.

Since the concentration of the impurity in solid and liquid are very small, the liquidus and solidus curves can be approximated by two straight lines. The ratio between the impurity concentration in the solid and that in the liquid is then a constant;

$$\frac{C_S}{C_l} = C_{seg} \tag{13.4}$$

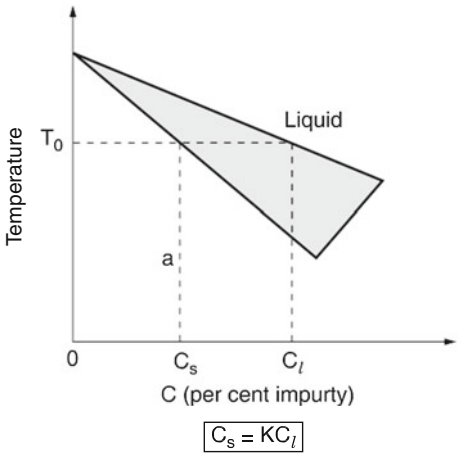

Fig. 13.4 The straight liquidus and solidus imply that the ratio of impurity concentration in the solid to that of the liquid is a constant C_{seg}, called segregation. Reproduced with permission from [1]

The constant C_{seg} is called the *distribution or segregation coefficient*. If the solidifying liquid is of the composition C_l, the first solid to emerge from the liquid has the composition $C_{seg}C_l$. If C_{seg} is less than one, as in Fig. 13.4, the solid is purer than the liquid. The material can be purified by partially solidifying and then pouring off the liquid. The first material to solidify is again the purest. A rod solidified from one end by moving the solid liquid interface continuously, leaves the purest and most useful material at the initial end.

13.5.2 Zone Refining Apparatus

Schematic representation of a zone-refining apparatus is shown in Fig. 13.5. Only a section of the bar of semiconductor material is melted at any one time. The source of heat is usually a high frequency induction coil. As the coil is moved along the bar, the molten zone moves with it. The liquid which no longer lies in the hot region, solidifies. The length of the zone remains constant if the power input of the induction coil and the environment of the bar remain constant.

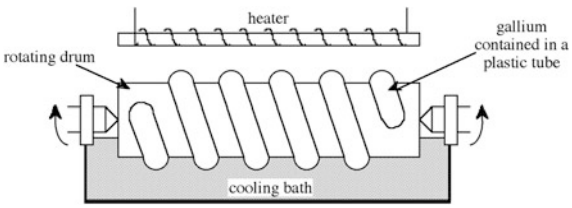

Fig. 13.5 Schematic set-up of a zone-refining apparatus. Reproduced from [3]

Example 13.1 A Si crystal is to be grown by the Czochralski method and it is desired that the ingot contain 10^{16} phosphorus atoms/cm^3. Determine the (a) concentration of phosphorus atoms that the melt should contain to give this impurity concentration in the crystal during the initial growth? For *P* in Si, $C_{seg} = 0.35$. (b) If the initial load of Si in the crucible is 5 kg, how many grams of phosphorus should be added? The atomic weight of phosphorus is 31.

Solution. (a) Using Eq. 13.4, the initial concentration of *P* in the melt is found as

$$\frac{10^{16}}{0.35} = 2.86 \times 10^6/\text{cm}^3 \tag{i}$$

(b) The *P* concentration is so small that the volume of melt can be calculated from the weight of Si. The density of Si is 2.33 g/cm^3. On neglecting the difference in density between solid and molten Si, we write

$$\frac{5000\,\text{g of Si}}{2.33\,\text{g/cm}^3} = 2146\,\text{cm}^3 \text{ of Si} \tag{ii}$$

Considering Eqs. (i) and (ii), we get

$$2.86 \times 10^{16}/\text{cm}^{+3} \times 2146\,\text{cm}^3 = 6.14 \times 10^{19}\text{P atoms}$$

$$\therefore \quad \frac{6.14 \times 10^{19}\text{atoms} \times 31\,\text{g/mole}}{6.02 \times 10^{23}\,\text{atoms/mole}} = 3.16 \times 10^{-3}\text{g of P}$$

13.6 Semiconductors Fabrication Technology [1]

The development of large-scale integrated circuits (LSICs) and decreasing size of electronic devices are remarkable achievements of semiconductor technology. A single piece of semiconductor can connect more than 1000 transistors on an area of about 1 cm^2. This has become possible due to advances in fabrication and processing techniques for semiconductors. In this regard, the processes of microelectronics may be grouped as follows.

1. Semiconductor microelectronics, and
2. Thin film microelectronics.

Diodes, *pnpn* switches, transistors and resistors belong to semiconductors of microelectronics group while the interconnections of various electronic circuits and capacitors are the product of thin *film microelectronics*.

13.6.1 Microelectronic Circuit Construction [1]

A semiconductor microelectronic circuit requires following sequential processes in its construction.

(i) Production of highly purified *n* or *p* type silicon.
(ii) Single crystal growth from the melt.
(iii) Manufacturing of 0.25–0.40 mm thick *wafer*.
(iv) Polishing of wafers to a thickness of 0.15–0.20 mm.
(v) Oxidation to isolate pockets in a wafer.
(vi) *Photoengraving* for cutting windows in the oxide layer.
(vii) Diffusion by doping via a vapour phase of B_2O_3, B_2H_6 or PH_3 in a stream of hydrogen, results in pn and *pnp* junctions.
(viii) *Epitaxy* for growing a new layer of same crystal orientation using hydrogen as carrier gas, and silane (SiH_4), dichlorosilane (SiH_2Cl_2) etc. as vapour sources.
(ix) Chemical processing such as etching to remove mask and oxide layers.
(x) *Masking i.e.* repeating the above operations a number of times on the surface of the wafer. The surface is then separated into chips. The circuit component per chip exceeds 1 million.
(xi) Interconnections by metalizing with aluminium which is deposited by vacuum evaporation.

13.6.2 Thin Film Circuit Fabrication

In fabricating thin film microelectronic circuits, glazed ceramics and glass substrates are used. The *substrate* is a polished surface on which many hundred I.Cs may be located. Deposition of I.Cs on thin films can be done by one or more of the following processes.

(i) Vacuum deposition,
(ii) Silk screening,
(iii) Vapour plating, decomposition,
(iv) Electron beam
(v) Plasma decomposition,
(vi) Sputtering, and
(vii) Anodization.

Thin film resistors employ metallic film while the thin film conductors employ film of gold or aluminium, and capacitors use a dielectric film. Ion implantation is a most modern method of doping microelectronic devices such as in MOSFET.

Readers are advised to refer particular references on specific topics as further information will be beyond the scope of this book.

13.7 Manufacturing of Wafers [1]

The single-crystal ingot is mechanically processed to manufacture wafers. It involves several steps, as listed below.

1. The first step involves mechanically grinding of the more-or-less cylindrical ingot into a perfect cylinder. This is important because in a modern integrated circuit fabrication, many processing tools and wafer handling robots require tight tolerances on the size of the wafers.
2. Then using X-ray crystallography, crystal planes in the ingot are identified. Most Si ingots are grown along the <100> direction.
3. For such ingots, a small notch is ground on one side of the cylinder to delineate a {110} face of the crystal. This is useful because for <100> Si wafers, the {110} cleavage planes are orthogonal to each other. This notch then allows the individual integrated circuit chips to be made oriented along {110} planes. Due to this; the chips are sawed apart, there is less chance of spurious cleavage of the crystal.
4. Next, the Si cylinder is sawed into individual wafers about 775 μm thick, by using a diamond-tipped inner-hole blade saw, or a wire saw.
5. The resulting wafers are mechanically lapped and ground on both sides to achieve a flat surface, and to remove the mechanical damage due to sawing. The flatness of the wafer is critical from the point of view of "depth of focus" or how sharp an image can be focussed on the wafer surface during photolithography.
6. The Si wafers are then rounded or chamfered along the edges to minimize the likelihood of chipping the wafers during processing.
7. Finally, the wafers undergo chemical-mechanical polishing using slurry of very fine SiO_2 particles in a basic NaOH solution to give the front surface of the wafer a mirror-like finish. The wafers are now ready for integrated circuit fabrication.

The economic value added in this process is impressive as from sand (SiO_2), we obtain Si wafers on which we can make hundreds of microprocessors. Thus the very cheap sand is converted into very costly products costing several hundred dollars.

13.8 Ion-Implantation

The process of ion-implantation is frequently used as an alternative to pre-deposition for introducing dopant atoms into the desired region of a semiconductor. The implanted impurities are then diffused using a drive-in step. The ion-implantation technique offers the advantage of precisely controlling the amount of dopant and its depth below the surface. And also, it is a low-temperature process that eliminates deformation of wafer caused at high temperatures.

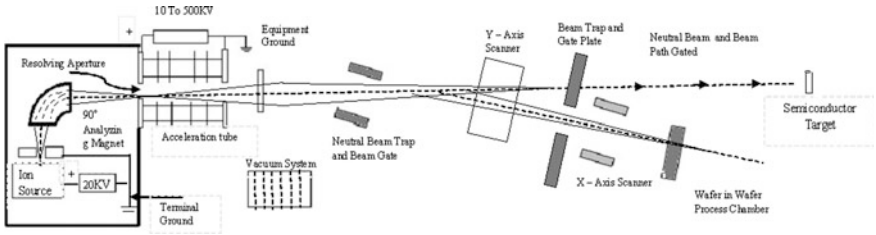

Fig. 13.6 Arrangement of an ion-implantation system. Modified from [2] and self drawn

In this technique, a beam of ionized atoms is accelerated through a desired potential (10–500 kV) and is made incident on a semiconductor target as shown in Fig. 13.6. A gas, containing the atoms of the desired impurity is introduced into a chamber where the atoms are ionized by collisions with high-energy electrons. The ion beam emerging from the chamber contains the desired dopant ions, as well as the ions of unwanted species. Now, the dopant ions are separated from the unwanted ions by passing the beam through a strong magnetic field that bends the desired ions through a 90°. The selected ions are then accelerated using an electric field and are made to strike the semiconductor target which is kept at ground potential. The beam is deflected horizontally and vertically so that it sweeps across the target to ensure homogeneous doping. Both the beam and the target are maintained under a high vacuum.

When the accelerated ions enter the semiconductor, they lose their kinetic energy through collisions with the electron cloud of the semiconductor atoms and the positively charged nuclei of the atoms. An ion comes to rest when its kinetic energy is reduced to zero. The total path length of the ion in the semiconductor is called its range, and the penetration depth of the ion in the target is called its projected range R_p.

13.9 Lithography

Lithography is a process in which the transfer of an image is done from the mask to the surface of the wafer. Lithography may be accomplished in different ways. These are:

1. Photolithography
2. Electron-beam lithography
3. X-ray lithography

Photolithographic process involves the transfer of an image from the mask to the surface of the wafer through the use of ultraviolet (UV) light and a photoresist. In *electron-beam lithography*, the E-beam systems may be either a scanning E-beam pattern generator or an E-beam projection system. The *X-ray lithography* uses the short wavelength X-rays instead of UV light.

13.9.1 Photoresists

Polymeric photoresist materials are generally used as a spin cast film as part of a photolithographic process. The film is modified by exposure to radiation such as visible light, ultraviolet light, X-rays of electrons. Exposure is usually conducted through a mask so that a pattern can be created in the photoresist layer and subsequently on the substrate through an etching or deposition process. Resists are either positive or negative depending on whether the radiation exposure weakens or strengthens the polymer. In the developer step, chemicals are used to remove the weaker material leaving a patterned photoresist layer behind. Important photoresist properties include resolution and sensitivity, particularly as feature sizes decrease.

13.9.2 Photolithography

Photolithography is a process of planar technology to fabricate an IC in which a desired pattern of doping is transferred onto the silicon wafer. The entire process involves:

(i) coating of SiO_2 layer with a film of photosensitive emulsion called *photoresist,*
(ii) blackening the portions to be doped on a transparent sheet, placing this sheet on photoresist layer and then exposing to ultraviolet light
(iii) removing the mask and dipping the wafer in trichlorothylene, and
(iv) *etching* the SiO_2 with hydrofluoric HF solution.

13.10 Epitaxy

Epitaxy means the processes which are used to grow a crystalline layer of semiconductor on a crystalline substrate in such a way that, the layer grown has the same lattice structure as the substrate. Epitaxial growth provides an alternative to the diffusion process for obtaining appropriately doped semiconductor regions. An added advantage of this process is that the impurity concentration in the grown layer can be adjusted independently of that in the substrate. The main processes of epitaxial growth are following.

- Vapour phase epitaxy (VPE)
- Liquid phase epitaxy (LPE), and
- Molecular beam epitaxy (MBE).

VPE has been used to grow Si and III–V compounds, whereas the LPE is mainly used with III–V compounds. MBE is more versatile and allows a precise control of doping profile.

13.10.1 Vapour Phase Epitaxy

Silicon epitaxy is accomplished using the chemical vapour deposition (CVD) technique which has been used to deposit Si from $SiCl_4$, silane (SiH_4), SiH_2Cl_2, SiH_3Cl, and some other compounds. Figure 13.7 shows a schematic of the growth system using $SiCl_4$ in which the liquid $SiCl_4$ is kept in a bubbler whose temperature is carefully controlled near 0 °C. H_2 gas is passed through the bubbler. The temperature of the bubbler and the flow rate of H_2 through it determine the concentration of the $SiCl_4$ in the mixture. The $SiCl_4 + H_2$ vapour is mixed with more H_2 near the mouth of the furnace and is passed through the quartz tube. The Si wafers are placed on a graphite susceptor kept in the quartz tube which is heated to a temperature in excess of 1100 °C by an rf induction coil. The following reaction takes place on the wafer surface:

$$SiCl_4 + 2H_2 \rightleftharpoons Si + 4HCl \tag{13.5}$$

The Si is deposited on the silicon substrate, whereas the HCl gas leaves through a suitable vent. The rf coil heats the graphite but not the quartz tube, therefore, there is no deposition on the walls of the tube. Since the reaction occurs in a chamber, the arrangement of Fig. 13.7 is called a reactor chamber or simply a reactor. The reaction represented by Eq. (13.5) is reversible. The reverse reaction etches Si and is used to clean the substrate prior to the start of deposition. This etching is performed by passing HCl through the reactor. The growth process is started by stopping the HCl flow and introducing the $SiCl_4 + H_2$ mixture into the reactor. In order to grow doped

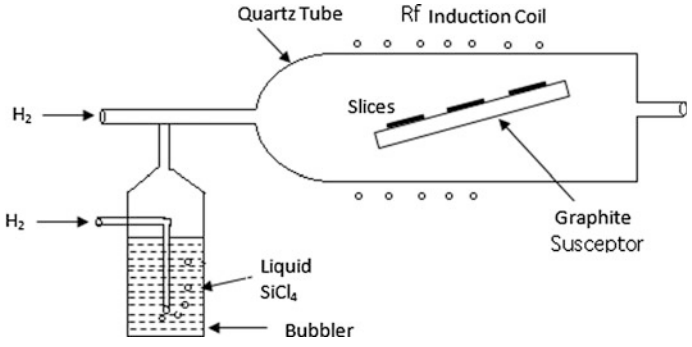

Fig. 13.6 Schemantic arrangement of an epitaxial growth system. Modified from [2] and self-drawn

Si with a desired resistivity and conductivity, dopant atoms are introduced into the gas system. Gases like PH_3, AsH_3, and SbH_3 are used for n-type doping; whereas diborane (B_2H_6) is used for p-type doping.

13.10.2 Liquid Phase Epitaxy

LPE is used to fabricate multilayer structures of ternary and quaternary compounds for use in LEDs and lasers. In this technique, a mixture of semiconductor with a second element may melt at a lower temperature than the semiconductor itself and thus may be used to grow a crystal from solution at the temperature of the mixture.

13.10.3 Molecular Beam Epitaxy (MBE)

MBE technique employs an evaporation method as a means of obtaining the epitaxial layer of desired constitution. The substrate is held in an ultrahigh vacuum, and the molecular or atomic beams of the constituents are made to impinge on its surface. Figure 13.8 depicts the arrangement for growth of AlGaAs epitaxial layers on a GaAs substrate. The components Al, Ga, and As of the compound and the dopants Sn and Be are heated in separate cells. Each of the source vessels has a controllable shutter port. Collimated beams of these substances are directed onto the substrate which is held at a temperature between 500 to 600 °C. The rate at which the atomic beams of the constituent atoms strike the substrate surface can be

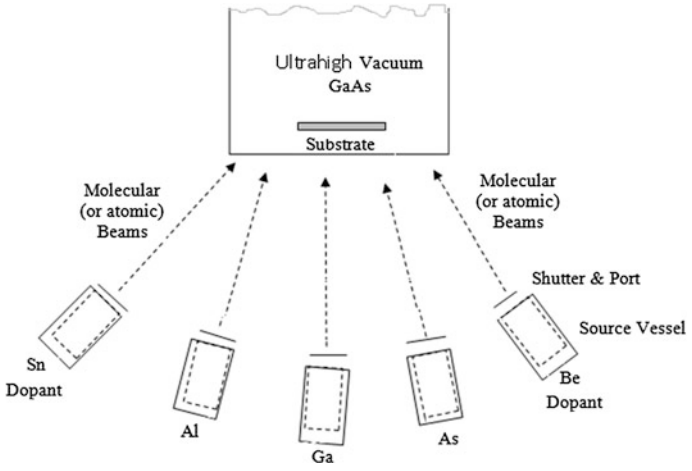

Fig. 13.8 Arrangement of molecular beam epitaxy method illustrating the growth of AlGaAs. Modified from [2] and self drawn

precisely controlled. High-quality films can be grown using this method. Because ultrahigh vacuum and close controls are involved, MBE setup remains a sophisticated one. However, its main advantages are

i. a low substrate temperature that minimizes the diffusion from the substrate, and
ii. a very precise control of dopant's profile.

13.11 Chemical Vapour Deposition (CVD)

In some cases, the thermal growth of SiO_2 is not possible such as when a substrate material other than Si is used. When thermal growth is not possible, a CVD technique offers an important alternative. For example, SiO_2 layers can be prepared by the reaction of SiH_4 and O_2 at temperatures between 250 and 500 °C.

$$SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O \uparrow \tag{13.6}$$

The reaction may occur in a reactor similar to one as shown in Fig. 13.7 A gas mixture containing either N_2 or Ar with O_2 and about 1 % SiH_4 is used. The SiO_2 growth rate depends upon the substrate temperature and the rate of gas flow. This method also allows the deposition of SiO_2 layers doped with dopants such as As, P, and B. The doped oxide can then be used as a diffusion source.

13.12 Sputtering

In this method, the ions of a gas like Argon (Ar) produced in a glow discharge, are accelerated through a potential gradient and are then bombarded on a target. Atoms near the surface of the target become volatile and are transported as a vapour to the substrate where they condense and form a film of the material. A schematic diagram of a sputtering system is shown in Fig. 13.9. The material to be sputtered is made the cathode, while anode holds the substrate. Sputtering can be performed using either a D.C. or an rf power source. For SiO_2 deposition, a SiO_2 block is made the cathode, and the substrates are placed on the anode which is kept at the ground potential (Fig. 13.9). An rf voltage at about 10 MHz is applied between the cathode and the anode. The electrons in the plasma have a much higher mobility than the Ar-ions in the rf field. Consequently, electrons flow to the SiO_2 cathode, which then becomes negatively charged. Ar-ions bombard the cathode target, and SiO_2 is deposited on the substrates. These layers are very dense and can be used as insulating layers in various applications.

A problem common to all deposited SiO_2 layers is that the interface between the SiO_2 and the semiconductor is not as perfect as the Si–SiO_2 interface for thermally grown oxide.

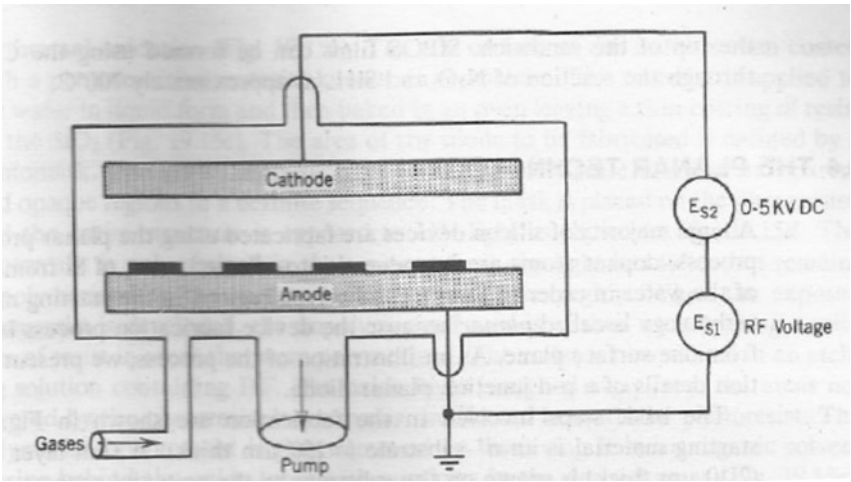

Fig. 13.9 Arrangement depicting an rf diode sputtering setup. Reproduced from [2]

13.13 Masking

The photomasking process can be divided into two distinct areas viz.

i. the generation of a mask whose image is to be transferred to the Si wafer; and
ii. the transfer of an image from the mask to the surface of the wafer.

For most present-day integrated circuits, mask making is done by using computer-controlled drawing boards and other equipment. In either case, copies of the circuit patterns are photographically reduced until they are ten times the ultimate size. The final mask is made from the 10× plate, using a step and repeat camera that has a reduction factor of 10. The step and repeat process results in rows and columns of identical images being transferred to a glass plate called a 'master'. The primary mask is used to make contact copies again using photosensitized glass plates. These copies are then used for the actual image transfer to a semiconductor wafer.

Another method utilizes the computer-controlled light flashes to generate the desired pattern on a photographic film by writing with a light pencil. The resulting pattern is then reduced and handled in a step and repeat system to create the production mask. Another method involves the use of an electron beam exposure system that can directly write the pattern in its final size onto an electron-sensitive photoresist in a hard surface mask.

13.14 Etching

Etching techniques are used for the selective removal of undesired dielectric and metallic layers. Different etching techniques are:

- Wet chemical etching
- Electrochemical etching,
- Sputter etching,
- Plasma etching, and
- Reactive ion etching.

A brief account of a few of these techniques is provided ahed.

Wet etching. Wet chemical etching is most widely used technique for selective removal of the regions of semiconductor material, metal, SiO_2, and Si_3N_4. For selective etching of different materials, the SiO_2 is etched in a buffered solution of HF + NH_4F; Si_3N_4 is etched in hot H_3PO_4; while Al is etched in either H_3PO_4, HNO_3, or acetic acid. A common method of etching is to immerse the wafer in the etching solution at a predetermined temperature. The etch time is determined by the etching rate of the solution.

Electrochemical etching. In electrochemical etching, a voltage is applied between the etchant and the material to be etched. Then the etching is performed at a controlled rate.

13.15 Metal Deposition Techniques

After a device has been fabricated on a semiconductor substrate, the ohmic contacts onto the various regions of the device are made by metal deposition. In case of an integrated circuit, all devices forming the circuit are suitably connected together with metallization to perform the intended circuit functions. The metal that is used to provide ohmic contacts for devices and interconnections for integrated circuits need to have high electrical conductivity and able to make good ohmic contacts with the semiconductor. Furthermore, it should have good adherence to the underlying surface and must not corrode under normal operating conditions. No single metal is known to perfectly meet all these requirements for a given semiconductor. However, in case of silicon, Al meets most of the requirements to a sufficient degree and is widely used for device interconnections, and in many cases for making ohmic contacts. Pure Al has a tendency to react with Si, hence to prevent this occurrence, some Si is added to Al-metallization.

Subsequent to metal deposition, the semiconductor wafer is placed in a furnace to alloy the metal to the semiconductor to ensure good electrical contact. It is then diced into separate pieces, each containing one or more semiconductor devices. Each chip is then soldered to a package, and wires from the package leads are

connected to the metal on the semiconductor. Finally, the package is sealed with a ceramic or a metal cover.

13.16 Fabrication Techniques of P–N Junction

Based on the fabrication technique adopted, the semiconducting p–n junctions (diodes) may be of following types.

1. Grown junction.
2. Alloy type (or fused) junction.
3. Diffused junction.
4. Epitaxial grown (or planar diffused) junction.
5. Point contact diode junction

13.16.1 Grown Junction Diode

Diodes of this type are formed during the crystal pulling process. P- and N-type impurities can be alternately added to the molten semiconductor material in the crucible, which results in the formation of a P–N junction. After slicing, the larger area device can be cut into a large number (say in thousands) of smaller-area semiconductor diodes. Though such diodes, because of larger area, are capable of handling large currents but larger area also introduces more capacitive effects, which are undesirable. Such diodes are used for low frequencies.

13.16.2 Alloy Type (or Fused) Junction

Such a diode is formed by first placing a P-type impurity (a tiny pellet of aluminium or some other P-type impurity) into the surface of an N-type crystal and heating the two until liquefaction occurs where the two materials meet. An alloy will form that on cooling, will give a P–N junction at the boundary of the alloy substrate. Similarly, an N-type impurity may be placed into the surface of a P-type crystal. Alloy type diodes have a high current rating and large PTV (peak inverse voltage) rating. The junction capacitance is also large, due to the large junction area.

Alloyed junctions are made by heating a semiconductor slice in contact with an impurity that becomes liquid at the temperature used for heating and dissolves some of the semiconductor. As the liquid is cooled, the semiconductor recrystallizes with impurity atoms substituted in the semiconductor lattice. The fabrication process of a p–n junction formed by alloying Ge with In, is shown in Fig. 13.10a. A small pellet of In is placed on the surface of a slab of n-type Ge. The semiconductor slab is then

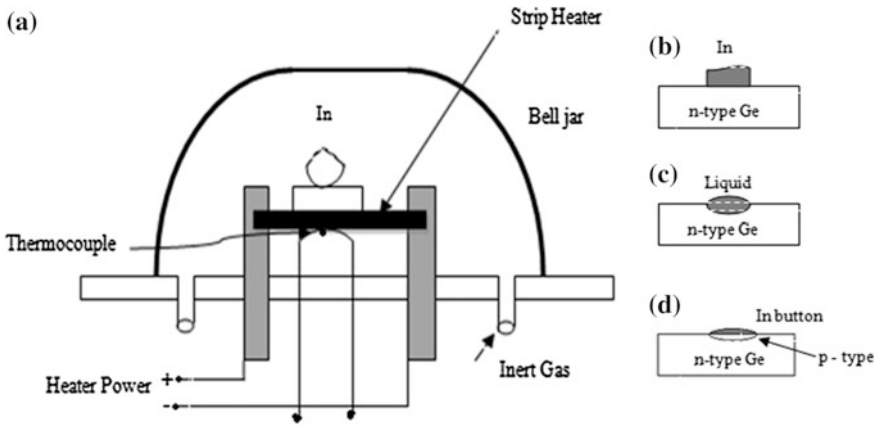

Fig. 13.10 Illustration of p–n junction formation by alloying. **a** Experimental setup, **b** Indium In–pellet on Ge before melting, **c** melting of into form a In–Ge mixture, and **d** the p–n junction formed after recrystallization. Modified from [2] and self-drawn

placed on a carbon strip heater that is covered with a glass bell jar. An inert atmosphere is maintained in the space covered by the bell jar by introducing an inert gas like argon or nitrogen. When the temperature of the strip heater is raised to about 500 °C, the In pellet on the surface of the Ge slab melts and dissolves some of the Ge (Fig. 13.10b) and forms a small puddle of a molten In–Ge mixture (Fig. 13.10c). When the temperature is lowered, the molten mass begins to solidify. The initial portion of the recrystallized material will be a single crystal of p-type Ge doped with In. As the solidification proceeds, the remaining mass becomes increasingly rich in In. Finally, when all the Ge is consumed, the material frozen at the outer surface of the recrystallized mass is pure In, which serves as the ohmic contact to the p-type Ge in Fig. 13.10d.

In the case of Si, p–n junctions can be made in a similar way by alloying Al to n-type Si. Alternatively, Au with about 0.1 % Sb can be prepared in the form of a thin disk which may then be alloyed to p-type Si to produce the n-region of the p–n junction. The alloy process is a simple and efficient method of making p–n junctions. However, it does not permit tight control on the area and the depth of the junction and thus has found only limited use.

13.16.3 Diffused Junction

Diffusion is a process in which a heavy concentration of particles diffuse into surrounding region of lower concentration. The main difference between the diffusion and alloy process is the fact that the liquefaction is not reached in the

diffusion process. In the diffusion process, heat is applied only to increase the activity of elements involved.

For the formation of such junctions, either the solid or gaseous diffusion process can be employed. The process of solid diffusion starts with formation of layer of an acceptor impurity on an N-type substrate and heating the two until the impurity diffuses into the substrate to form the P-type layer. A large P–N junction is divided into parts by cutting process. Metallic contacts are made for connecting anode and cathode leads. Solid-state impurity diffusion is the most widely used technique for making p–n junctions, especially in silicon. The diffusion of dopant impurity atoms into a semiconductor is governed by the same basic laws as the diffusion of free carriers.

In the process of gaseous diffusion instead of layer formation of an acceptor impurity, an N-type substrate is placed in a gaseous atmosphere of acceptor impurities and then heated. The impurity diffuses into the substrate to form P-type layer on the N-type substrate. The process is illustrated in Fig. 13.11a, b. Though, the diffusion process requires more time than the alloy process; but it is relatively inexpensive, and can be very accurately controlled.

The diffusion technique leads itself to the simultaneous fabrication of many hundreds of diodes on one small disc of semiconductor material. It is most commonly used in the manufacture of semiconductor diodes. This technique is also used for the production of transistors and ICs.

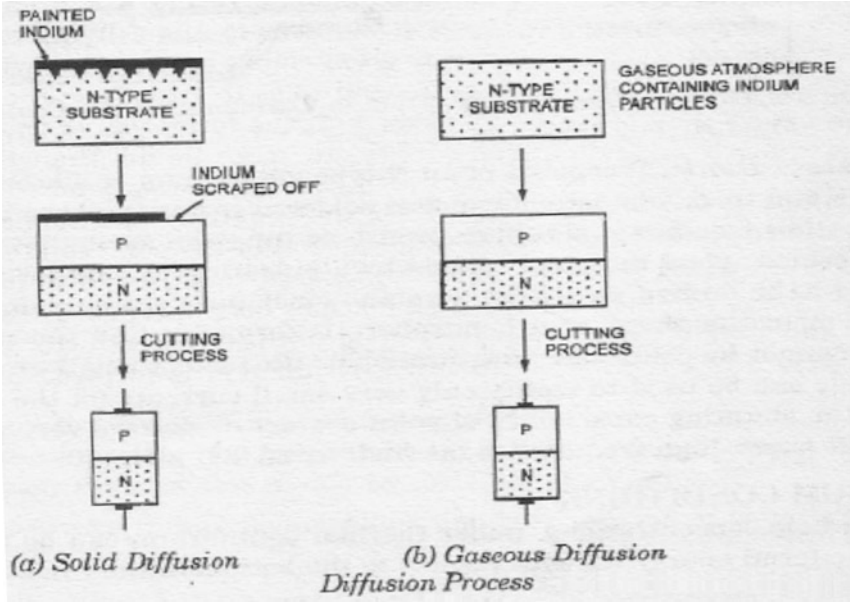

Fig. 13.11 Schemantic illustration of the formation of diffused junction by **a** solid diffusion process, and **b** gaseous diffusion process

13.16.4 Epitaxial Growth (or Planar Diffused) Junction (Fig. 13.12)

To construct an epitaxially grown junction diode, a very thin (single crystal) high impurity layer of semiconductor material (silicon or germanium) is grown on a heavily doped substrate (base) of the same material. This complete structure then forms the N-region on which the P-region is diffused. SiO_2 layer is thermally grown on the top surface, photo-etched and then aluminium contact is made on to the P-region. A metallic layer at the bottom of the substrate forms the cathode to which lead is attached. This process is usually employed in the fabrication of IC chips.

13.16.5 Point Contact Junction (Fig. 13.13)

It consists of an N-type germanium or silicon wafer about 12.5 mm × 12.5 mm square and 0.5 mm thick, one face of which is soldered to a metal base by radio-frequency (rf) heating. The other face has a phosphor bronze or tungsten spring pressed against it. A barrier layer is formed around the point contact by a pulsating current forming process. This causes a P-region to be formed round the wire and since pure germanium is N-type, a very small P–N junction in the shape of a hemisphere is formed round the point contact. This forming process cannot be controlled with precision. Because of small area of the junction, the point contact diode can be used to rectify only very small currents, of the order of mA.

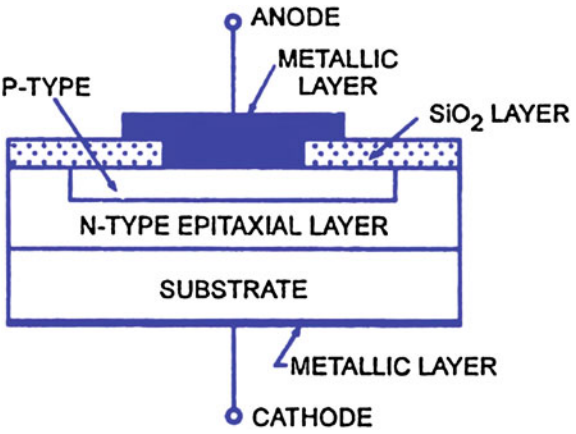

Fig. 13.12 Epitaxially grown (or planar diffused) diode

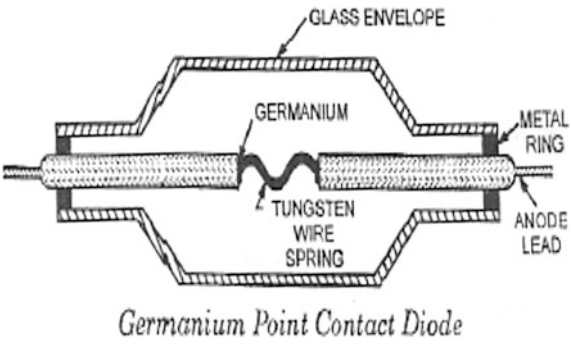

Fig. 13.13 Schematic arrangement of a point contact diode junction

13.17 Summary of the Fabrication of a Semiconductor P–N Junction

The main steps involved in the fabrication of a *p–n* junction are given below in Fig. 13.14. The diagrams show a typical case in which only four diodes per wafer are shown for simplicity. Also the relative thicknesses of the oxide, photoresist, and Al-layers are exaggerated.

13.18 Transistor Manufacturing Processes

Majority of the methods employed in transistor fabrication are the extensions of the methods employed in the manufacture of semiconductor diodes. The methods most commonly used for fabrication of transistors include point-contact, alloy junction, grown junction and diffusion. Various techniques adopted to manufacture a transistor, are displayed stepwise in Fig. 13.15. The details are self-explanatory.

13.19 Solved Examples

Example 13.2 Semiconductor materials are the natural choices for electronic devices—why?

Solution. Semiconductor materials are the natural choices because their conductivity and other electrical properties can be easily varied to suit the requirements of desired electronic devices. For example, their conductivity can be varied by following means.

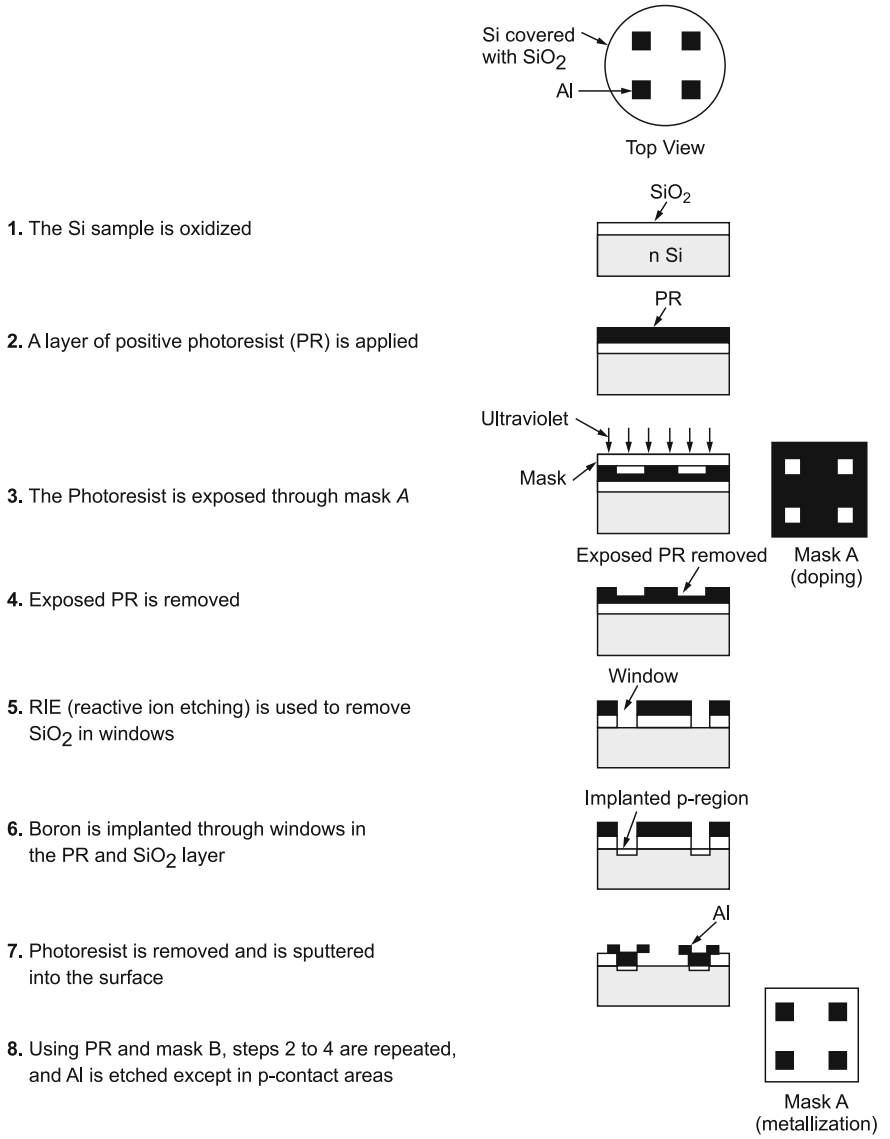

Fig. 13.14 Simplified description of steps in the fabrication of *p–n* junctions. Reproduced with permission from [1]

- By controlling the impurity content
- By optical excitation
- By change in temperature

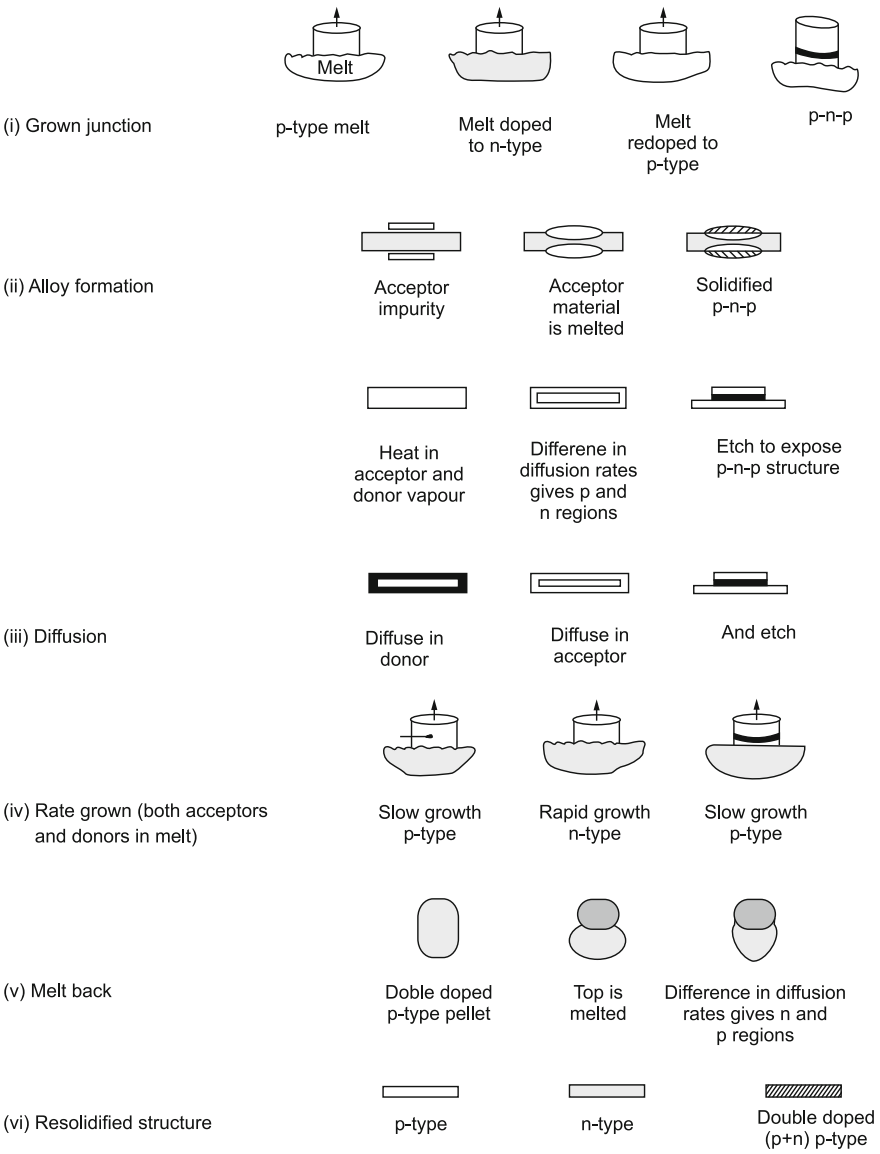

Fig. 13.15 Schematic arrangement of transistor manufacturing technique. Reproduced with permission from [1]

Example 13.3 How does a metallurgical grade Si (MGS) differ from an electronic grade Si (EGS)? Which grade is more suitable for making semiconductor devices?

Solution. A MGS is an output product obtained from the reaction of SiO_2. The MGS contains impurities such as Al, Fe and other heavy metals of the order of

100–1000 ppm. The MGS is an input product to obtain the EGS. EGS is highly pure semiconductor containing impurities of the order of a few ppb (1 ppb[1] = 10^{-3} ppm). Due to its high level purity, the EGS grade is more suitable for making semiconductor devices.

Example 13.4 Differentiate between the Bridgman's method and Czochralski's method of recrystallization.

Solution. In *Bridgman's recrystallization method*, the material is melted in a vertical cylinder that tapers conically to a point at the bottom. The vessel is gradually lowered in the cold zone where crystallization begins at the tip and the growth continues from the nucleus. In *Czochralski's method*, a single crystal is introduced on the surface of the melt and is drawn slowly upward, in the cold zone. The grown crystal usually acquires the form of container through which it has been drawn.

Example 13.5 Why the impurity concentration in extrinsic semiconductor is kept very small?

Solution. The electrical conductivity of pure semiconductors is primarily of electron carrier type. The hole conductivity is comparatively weaker. This makes the semiconductors extremely sensitive to the presence of any impurity. Hence impurity concentration is kept very small, about 1:10^6 to 1:10^9.

Example 13.6 Give a brief account of, as to how the p–n junction is formed?

Solution. In practice, the P–N junction is formed from a single monocrystalline structure by adding carefully controlled amounts of donor and acceptor impurities. The first and foremost requirement is to obtain an extremely pure germanium or silicon. Impurity of less than one part in ten billion (10^{10}) is required for most semiconductor device fabrication to-day. For obtaining pure semiconductor material, it is first purified chemically. For reducing the impurities further, and to ensure the formation of a monocrystalline structure, technique of floating zone is quite often employed. Once a pure monocrystalline semi-conductor is produced, carefully controlled amount of donor and acceptor impurities are added to the semiconductor without disturbing the orderly monocrystalline structure. Thus a P–N junction is formed.

Review Questions

1. What do you mean by metallurgical grade silicon and electric grade silicon? How is the element form of silicon produced?

[1] 1 ppb = 1 part per billion.

2. What are different processing techniques of semiconducting materials? Briefly describe them.
3. Explain the meaning of crystal growth. What are its different techniques? Explain any one of them.
4. Explain the Bridgman method of growing single crystal with the help of suitable diagram.
5. Describe the working of 'Czochralski method' crystal growth in semiconductor material with the help of suitable diagram.
6. Describe the float zone method of crystal growth with the help of suitable diagram.. Write its merits and demerits as compared to CZ method.
7. What is meant by zone refining? Why is it necessary for semiconducting materials?
8. Describe the technique of zone refining with the help of a suitable sketch and apparatus. How is this process accomplished?
9. Discuss any one technique of 'zone refining' in semiconductor material.
10. Describe in brief, the stepwise methodology to construct a semiconductor microelectronic circuit.
11. Explain the methodology of wafer manufacturing and the process of lithography.
12. What is the process of ion- implantation? With the help of suitable diagram, explain its process.
13. What is lithography? What are its different kinds? Discuss the 'photoresist' and photolithography.
14. What is/are the function(s) of epitaxy? Name its different processes, and explain the various phase epitaxy.
15. With the help of suitable diagram, explain the technique of molecular beam epitaxy.
16. What is sputtering? What is its importance in semiconductor fabrication? With the help of suitable diagram, explain this process.
17. Explain the following.
    (a) Chemical vapour deposition
    (b) Masking
    (c) Etching
    (d) Metal deposition techniques

18. Explain the procedure of manufacturing of a p-n junction.
19. Explain the procedure of manufacturing of a p-n-p or n-p-n junction.
20. Discuss in detail the various fabrication techniques of fabrication for p-n junctions. Compare the merits and demerits of each technique.
21. Write notes on the following:
    (a) Grown junction (b) Fused junction
    (c) Diffused junction (d) Planer diffused junction

Objective Questions

1. The silicon used for electrical purposes have silicon percentage of
   (a) 0.5%. (b) 2.5%.
   (c) 3.5%. (d) 4%
2. Consider the following functions:
   1. To mask against diffusion or ion implant.
   2. To act as a component in MOS devices.
   3. To provide low resistivity paths.
   4. To facilitate the entry of dopants.
   The function of an oxide layer on a silicon wafer would include
   (a) 1 and 2. (b) 2 and 3.
   (c) 3 and 4. (d) 1 and 4.
3. The correct sequence of processes involved in fabrication of a p-n junction diode is (out of many, only 4 to 5 processes are written)
   (a) thermal oxidization, photolithography, diffusion, etching
   (b) chemical vapour deposition, ion implantation, rapid thermal processing, diffusion
   (c) metallization, etching, photolithography, oxidization
   (d) oxidization, rapid thermal processing, ion implantation, etching, metallization

Answers

1. (c) 2. (a) 3.(d)

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