Blood Group Determination Using Vivado System Generator in Zynq SoC

Athmasri B. Krishnan and K.P. Peeyush

Amrita School of Engineering, Amrita Vishwa Vidyapeetham, Coimbatore, India

Abstract— **Blood grouping is an essential procedure in blood transfusions, donations and other emergencies. An error in grouping or a cross match can have adverse effect on the patient. Conventional way of blood grouping is performed manually on the basis of agglutination of blood in reaction with chemical reagents. The above method can lead to human errors while handling a large number of samples. Various systems have been developed to automate blood typing, but their excess testing time made it difficult during emergencies. This work emphasizes the FPGA implementation of an image processing algorithm to determine the blood group of a person. To do so, it uses plate test and image processing techniques using Vivado System Generator. Edge detection algorithm is performed in the image captured from the plate test. The number of edges determines whether the sample has agglutination or not. By comparing the number of edges in the image, blood group is classified. The proposed algorithm is implemented on a standard FPGA Development Board and its performance is evaluated by calculating accuracy of classification.**

Keywords— **Plate test, Agglutination, Simulink, System Generator, FPGA**

I. Introduction

Blood is the most important element in the human body which helps in the transportation of substances like nutrients, oxygen, metabolic wastes etc. It also helps in body regulation functions and system protection. Blood differs among humans in terms of its type or blood group. A blood group system is defined by the International Society of Blood Transfusion (ISBT) as the system where "one or more antigens controlled at a single gene locus or by two or more very closely linked homologous genes with little or no observable recombination between them"[1].

Blood type is determined by the presence or absence of certain protein molecules called antigens and antibodies in the blood. ABO is the most important blood group having A, B, AB and O as the blood groups. These groups will give the details of antigens present on the surface of Red Blood Cells (RBCs). Rh system is also important which determines the presence of “Rhesus factor” on the surface of RBCs.

Plate test or slide test is the common method to determine the blood group of a person. In plate test, antigen containing blood sample is exposed to commercially available chemical reagents having antibodies. These reagents are Anti-A, Anti-B and Anti-D. The result of plate test is interpreted by the occurrence or the non-occurrence of agglutination, which occurs due to the reaction of antigen and antibodies. The combination of agglutination in the reagents will determine the blood group of the sample. This process is done manually by technicians. Only a few numbers of samples can be tested by these methods [2]. While handling a large number of samples and during emergencies, the above method causes human errors. These errors can cause severe effects in patients during blood transfusion.

Different methods have been used to determine blood group automatically using spectrophotometric methods [3], mechatronic devices [4] having both mechanical and electronic parts, but by these methods, complexity increases and time taken for obtaining the result is more. Image processing techniques, especially segmentation can also be used to classify the blood groups [5].

This paper presents an image processing algorithm which is implemented on Zynq 7000 SoC to determine the blood group. The continuous growth in parallelism and functionality of Field Programmable Gate Arrays (FPGAs) in the last few years has contributed to an increasing interest in their use as an implementation platform for various image processing algorithms.

For simplified approach of hardware implementation, the Vivado System Generator is used. System Generator is a part of the Vivado system edition design suite. It is a high-level tool for designing high performance DSP systems using Xilinx All Programmable devices. It helps in automatic code generation of VHDL (VHSIC Hardware Description Language) and Verilog from Simulink. It quickly imports Vivado High-Level Synthesis IP for modeling with Simulink. It automatically generates IP and exports to the Vivado IP Catalog for easy design reuse and model sharing. System Generator supports JTAG communication between a hardware platform and Simulink [6]. This helps in easy implementation of the algorithm in hardware.

This paper is prepared as follows: Part II describes the materials and methods used, part III presents the results and discussions after the implementation of the proposed algorithm in hardware and part IV concludes the paper.

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II. Materials and Method

Plate test is a method in which mixing of blood sample (antigens) with reagents (antibodies) is done to determine the blood group. Based on the reaction between antigen and antibodies, agglutination occurs in the plate test. Fig. 1 shows agglutination with reagents Anti-A and Anti-D and Fig. 2 shows agglutination with Anti-B and Anti-D

Blood samples of 30 individuals having 20-25 years age and with different blood groups were collected and plate test was performed. Image of plate test result was captured using a camera of 5 Mega pixel resolution. The proposed algorithm was applied to the images captured.

A Simulink model containing image processing techniques is designed in Matlab (version 2013a) with the help of Simulink library browser. One of the blocks provided in its library is System Generator, which is configured for Zynq SoC. The image pre-processing and the post-processing uses Simulink blocks from computer vision and DSP toolbox. Edge detection algorithm uses Xilinx reference blocks. The process is carried out in a computer system having Windows XP as the operating system, Intel Core™ i5 processor @ 3.10GHz, system type is 64bit operating system and 4GB of RAM.

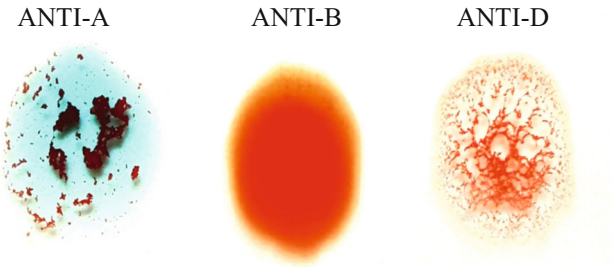

Fig. 1 Plate test for A+ blood group

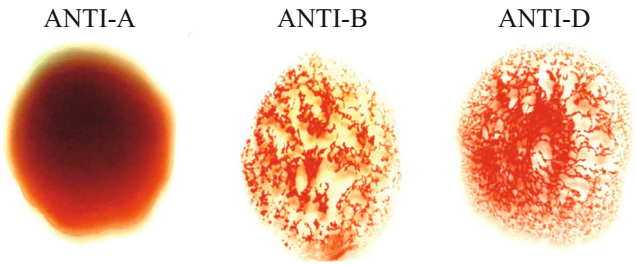

Fig. 2 Plate test for B+ blood group

The model designed is simulated with suitable simulation time and the code generated by System Generator is downloaded to Zynq board. Fig. 3 shows the general design flow of System Generator.

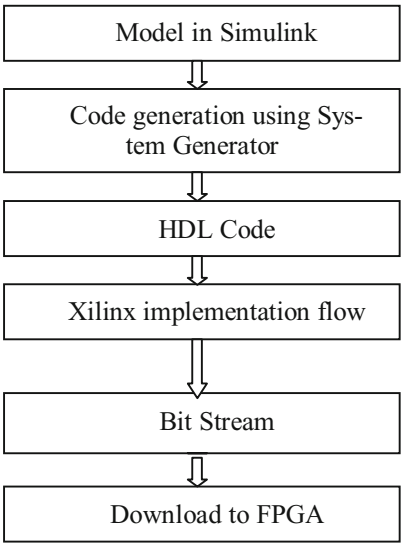

Fig. 3 Design flow of System Generator

A. Image Pre-processing

'Image from File' block reads the input image captured from plate test. From the color image, green plane alone is taken for processing [2]. The System Generator is not able to process the image in 2-D and for easy implementation, 1D is preferred. Thus 2-D to 1-D conversion is applied here.

B. Edge Detection using System Generator

The Xilinx Gateway In and Gateway Out are the boundaries for FPGA or the input and output to the Xilinx portion of Simulink design. So the proposed algorithm should be processed using Xilinx blockset, which is placed in between Gateway In and Gateway Out. Edge detection algorithm is applied to the image using Xilinx blockset.

Edges are a set of connected edge pixels, in which intensity of the image changes abruptly. When agglutination occurs in the plate test, there will be a variation in the intensity of the image. So the number of edges in the image will indicate the occurrence or non-occurrence of agglutination in the plate test [5].

Sobel edge detection algorithm is applied for the image taken. It is the most common method for edge detection of an image. Sobel operator calculates the gradient at each point of the image intensity and it gives the largest possible increase from light to dark and the rate of change in the above direction. It is a first order edge detection operator [7].

$$G_x=\begin{bmatrix}-1 & 0 & 1\\ -2 & 0 & 2\\ -1 & 0 & 1\end{bmatrix}\quad G_y=\begin{bmatrix}1 & 2 & 1\\ 0 & 0 & 0\\ -1 & -2 & -1\end{bmatrix} \tag{1}$$

G_x and G_y are the convolution kernels for sobel operator which is sensitive to changes in x and y directions respectively. Gradient magnitude is given by:

$$G = \sqrt{G_X^2 + G_Y^2} \tag{2}$$

But in some cases, due to the computational burden for implementing squares and square roots, approximation of the gradient magnitude is given by its absolute values [7]. i.e

$$G \approx |Gx| + |Gy| \tag{3}$$

In Xilinx blocksets, 5x5 filter mask gives the coefficients for Sobel edge detection. It contains 5 n-tap MAC FIR filters, counters, addressable shift register, coefficient ROM, MAC engine and capture register [6]. These filters are clocked 5 times faster than input rate. The throughput of the design is 213 MHz/5 = 42.6 million pixels/second [6] .The values will change depending on the size of the image taken.

C. Image Post-processing

The Post-processing part has the data type converter block, which converts the data type of input image to required output data type. In the System Generator part i.e using Xilinx blocksets, only 1-D signal can be processed. To view the output, 1-D to 2-D conversion is done. Classification of blood group based on the edges detected is included in the post-processing subsystem.

Fig. 4 shows the whole model, containing both image Pre-processing and Post-processing along with the algorithm in Xilinx blocks.

Two video viewers are used to compare the edge detected image by Simulink simulation and to the edge detected image which is implemented on Zynq SoC. The System Generator token in the model is the block which generates the HDL code and it helps in cramming a large number of pixels to smaller spaces. This helps in implementing various image processing techniques for an image of larger size.

III. Results and Discussion

The implementation of the proposed algorithm in Zynq SoC requires the conversion of entire model of edge detection (Xilinx blocks) to JTAG hardware co-simulation using Vivado System Generator (Fig. 4). In the System Generator token, Zynq xc7z020 and VHDL are selected as part (FPGA part to be used) and language respectively.

After generating the bit file, by providing specific parameters of clocking tab in System Generator, JTAG hardware co-simulation block is created.

From the edge detection, the count of edges is calculated in each region of the 3 reagents. If the count is more with respect to a fixed value, then it indicates the occurrence of agglutination in that particular region [5]. So depending on the count of edges and the sequence of agglutination occurred in the image, blood group is determined.

Fig. 5 shows the input image and the edge detected output image for the blood group A+. The Anti-A and Anti-D region is having more number of edges compared to Anti-B. Thresholding the image gives the real edges which comes in foreground and all other particles in the image goes to background. The output image shown below is the 'output image from FPGA' in Fig. 4.

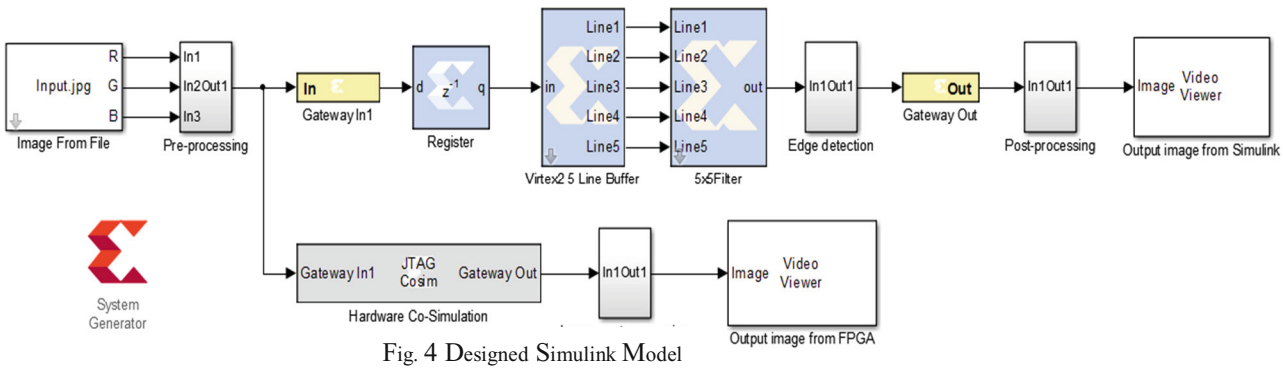

Fig. 4 Designed Simulink Model

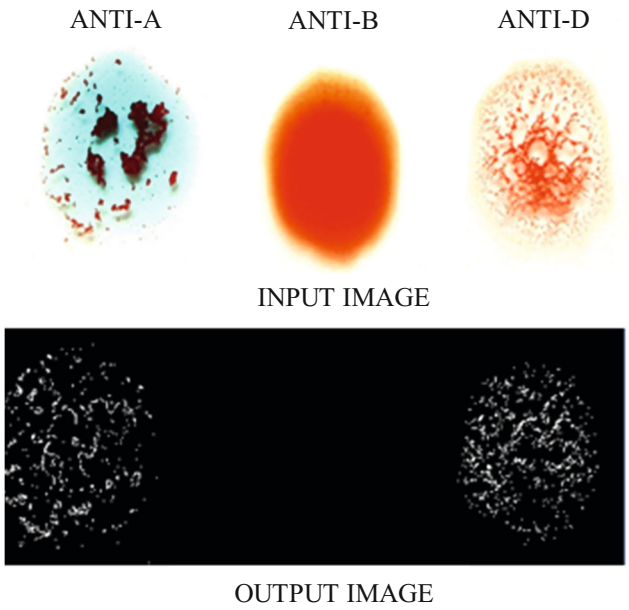

Fig. 5 For blood group A+

The proposed algorithm is applied to the 30 images captured. The hardware system achieved an accuracy of 96.6% in classifying the blood group for the above mentioned images when compared with the results obtained from the conventional techniques used in laboratories. The final hardware implementation requires only 239mW for the total on-chip power and it takes only 30 seconds for getting the results. Table 1 shows the utilization summary of hardware resources on the chip.

Table 1 Device utilization

Resource	Utilization	Available
Flip flops	837	106400
LUTs	479	53200
Memory LUT	45	17400
I/O	2	200
BRAM	6	140
DSP48	5	220
BUFG	4	32
MMCM	1	4

For the proposed hardware, the number of flip flops, memory LUT, LUTs and I/O utilizes only 1% of the resources. DSP48 utilizes only 2% and BRAM utilization is 4%.

IV. Conclusion

The hardware implementation of an image processing algorithm, which is used to determine the blood group of an individual, was presented. The proposed method uses Vivado System Generator for various image processing techniques. The implementation on Zynq 7000 consumes less power with minimum resource utilization. For future works, image acquisition can be done using onboard camera of the Zynq SoC and the proposed algorithm can be used to fully automate a portable device to determine the blood group.

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References

1. ISBT International Society of Blood Transfusion, 'Blood Group Terminology' at http://www.isbtweb.org
2. A. Ferraz, V. Carvalho, F. Soares, and C. P. Leao, (2011), " Characterization of blood samples using image processing techniques," *Sensors Actuators A. Phys.*, vol. 172, pp. 308–314.
3. S. Pimenta, J. M. Nobrega, F. M. Duarte, G. Minas, and F. O. Soares, (2012) "Automatic Electronic System to Human Blood Typing," *Procedia Eng.*, vol. 47, pp. 647–650.
4. K. Bezerra, A. Ferraz, V. Carvalho, F. Soares, T. Romanian, and R. Precision, (2012), "Advanced design of a mechatronic system for human blood typing," *4th Int. Conf. Innov. ,recent Trends Mechantronics,Mechanical Eng. New High-Tech Prod. Dev* ,Bucharest, Romania, (2012), no. 41, pp. 1–7.
5. T. Zarifi and M. Malek, (2013) "FPGA implementation of image processing technique for blood samples characterization," *Comput. Electr. Eng.*, vol. 40, no. 5, pp. 1750–1757.
6. Xilinx, (2010) "Xilinx System Generator for DSP Reference Guide," *Interface*, vol. 638, pp. 1–504.
7. R. Gonzalez, R. E. Woods, (2008), Digital Image Processing, Pearson Education, New Jersey.

Author: K.P. Peeyush
Institute: Amrita School of Engineering
Street: Ettimadai
City: Coimbatore
Country: India
Email: peeyushkp@gmail.com