Chapter 1
Silicon Nanowires: Fabrication and Applications

Thomas Mikolajick and Walter M. Weber

Abstract Due to the high surface to volume silicon ratio and unique quasi one-dimensional electronic structure, silicon nanowire based devices have properties that can outperform their traditional counterparts in many ways. To fabricate silicon nanowires, in principle there are a variety of different approaches. These can be classified into top-down and bottom-up methods. The choice of fabrication method is strongly linked to the target application. From an application point of view, electron devices based on silicon nanowires are a natural extension of the downscaling of a silicon metal insulator semiconductor transistor. However, the unique properties also allow implementing new device concepts like the junctionless transistor and new functionalities like reconfigurability on the device level. Sensor devices may benefit from the high surface to volume ratio leading to a very high sensitivity of the device. Also, solar cells and anodes in Li-ion batteries can be improved by exploiting the quasi one-dimensionality. This chapter will give a review on the state-of-the-art of silicon nanowire fabrication and their application in different types of devices.

1.1 Introduction

Silicon nanowires are quasi one-dimensional (1D) structures with a diameter of less than 100 nm. The very small diameter results in a large surface to volume ratio. This can be exploited in many ways in electronic devices [1]. When a gate is wrapped

T. Mikolajick (✉) · W.M. Weber
NaMLab GmbH, Nöthnitzer Strasse 64, 01187 Dresden, Germany
e-mail: thomas.mikolajick@namlab.com

T. Mikolajick
Institute of Semiconductor and Microsystems, TU Dresden,
Nöthnitzer Strasse 64, 01187 Dresden, Germany

T. Mikolajick · W.M. Weber
Center for Advancing Electronics Dresden (CfAED), TU Dresden,
Nöthnitzer Strasse 64, 01062 Dresden, Germany

around the nanowire, the optimum control of the nanowire potential by the gate potential is ensured. This makes nanowires an excellent choice for the ultimate silicon metal insulator semiconductor (MIS) devices [2]. However, the same feature also allows implementing device concepts that would have very poor properties in a conventional planar configuration. The junctionless transistor [3] and tunnel field effect transistors [4] are two prominent examples. Additionally, new types of functionalities can be exploited by making the devices reconfigurable [5]. When it comes to sensing devices, the small volume will allow effectively controlling the potential of the nanowire by even a very small input signal, making the approach very sensitive specifically for chemical sensing and bio-sensing [6, 7]. But also the field of energy generation and storage can benefit from the quasi 1D structure. In the solar cells the nanowires allow to more efficiently collect the incoming solar radiation [8] whereby in Li-ion batteries the structure allows for volume expansion [9].

A large number of techniques exist to fabricate silicon nanowires. These can be classified into bottom-up and top-down fabrication techniques. In top-down fabrication, lithography is used to define the fabricated structure that is then transferred from the photo-resist to the substrate by etching or a similar way of structuring the already available material. In the bottom-up approach, the material is added to the substrate in a self-organized way.

This chapter will review the current status of silicon nanowire technology. In the first part the silicon nanowire fabrication techniques will be summarized and there advantages and disadvantages will be discussed. The second part will then review the very important field of silicon nanowire based electron devices. Devices that are targeted to extend the current semiconductor roadmap are discussed together with approaches that are intended to add new functionality to semiconductor devices. The section on silicon nanowire based sensors will then focus on devices that can take full advantage of the know-how from integrated circuit manufacturing and illustrate further concepts. Finally, the possibilities for enhancing solar cells and Li-ion batteries will be discussed. The summary will include the concepts that may also gain importance and that are not covered in the previous sections. In all sections silicon technology is used as the starting point due to the well-established device technologies. However, it has to be considered that one of the advantages of the nanowire approach is the simplicity in which different semiconductor materials can be combined. Therefore, the prospects for even improving the device properties by e.g. using germanium or III–V semiconductors will be discussed where appropriate as well.

1.2 Fabrication Techniques for Silicon Nanowires

Traditionally semiconductor technology is driven by top-down fabrication using photo lithography. This approach has successfully enabled to scale down device dimensions all the way to the 10 nm range [10]. In contrast, bottom-up techniques

have the potential to construct very complex structures without the need of defining them in all details by a mask [11]. Nevertheless, there are still some missing links to make the bottom-up approach a manufactural alternative. When it comes to silicon nanowires, both paths are possible and have their advantages and drawbacks. In the top-down fabrication, a clear path from today's planar and FinFET devices to nanowire devices can be drawn. However, the etching of the nanowire out of the bulk silicon results in non-perfect geometry and requires advanced lithography. The bottom-up approaches, on the other hand, may lead to excellent crystal quality and small diameter using a very simple process. The precise placement and generation of highly complex structures as integrated circuits still remains elusive. Therefore, also combinations of both paradigms are considered. Another alternative is to use a template made from an insulating material like silicon dioxide or aluminium oxide, etch holes into the layer and fill the holes with silicon or the desired semiconductor material. This can be considered as a top-down fabrication process for vertical nanowires. The traditional top-down process, in contrast, will result in horizontal nanowires although etching wires out of a bulk crystal is in principle also possible.

The most prominent nanowire synthesis method is named the vapor liquid solid (VLS) growth mechanism. The VLS growth first described by Wagner and Ellis [12] the growth occurs via phase changes that are mediated through a catalyst particle. That means that the material to be grown, in this case silicon, is delivered in the gas phase, either molecularly or in the form of a gas compound that is introduced into the growth chamber. Figure 1.1 shows a schematic sketch illustrating the widely adopted VLS growth.

In the case of Si, molecular Si precursors can be evaporated either by Si effusion cells, or pulsed vapor deposition. Silicon gas precursors include mono-silane (SiH_4), trichlorosilane ($SiHCl_3$) or higher order silanes. The catalyst particle acts as a collector of silicon. In the case of employing gas precursors, the catalytic nature leads to lowering of the dissociation energies of the gas. Consequently, a high
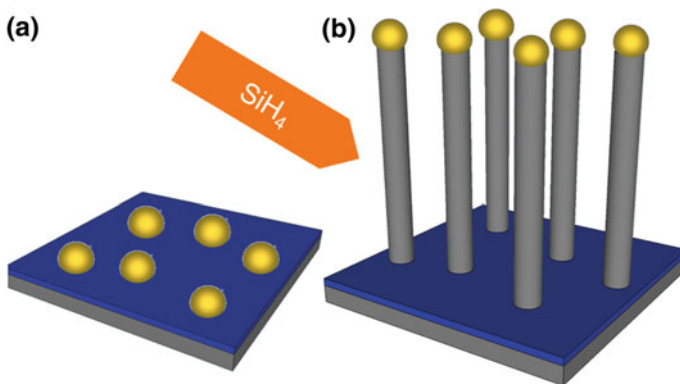

Fig. 1.1 Schematic view of VLS growth of silicon nanowires. **a** Gold particles formed on the growth substrate. **b** VLS growth using silane as silicon precursor
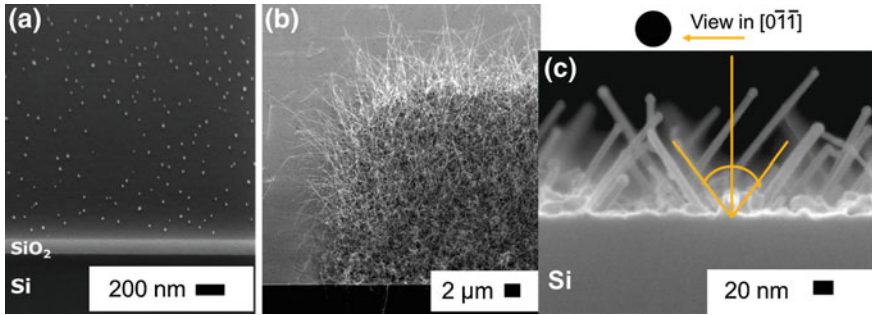
Fig. 1.2 Nanowires grown by the VLS process. **a** Shows the catalytic gold particles formed by sub–nanometer sputter deposition of Gold and a subsequent coalescence with a combination of a thermal anneal in hydrogen atmosphere at 450 °C for 300 s and a subsequent plasma treatment [13]. **b** Shows nanowires grown on an oxidized silicon substrate and **c** shows a close-up of nanowires grown on a (100) oriented single crystalline silicon substrate

concentration of silicon atoms is found at the catalyst particle´s surface, leading to diffusion into the cluster. In the case of employing gold catalyst clusters, the gold-silicon system can become liquid at temperatures above the eutectic point (363 °C), provided that sufficient fraction of Si is present (e.g. 18.6 at.% at the eutectic temperature). In case of a constant silicon flow, silicon atoms will continue to diffuse into the Au–Si melt, although this is thermodynamically unstable. To reduce energies, the super-saturated or excess silicon atoms condense into the solid-phase. Nucleation of Si occurs at the footprint of the Au–Si catalyst layer by layer. Consequently, a silicon monolith or nanowire is formed. Figure 1.2 shows the starting gold catalysts in Fig. 1.2a, silicon nanowires grown on an oxidized silicon wafer in Fig. 1.2b and a close up view of $\langle 110 \rangle$ oriented silicon nanowires lattice-matched grown on a crystalline silicon (100) wafer. An important implication of the VLS mechanism is that the size of the Au cluster defines the diameter of the nanowire without the tedious need of further lithographic means. In addition, the catalyst position on the substrate dictates the nanowire placement.

As explained above, in most cases gold particles are used as catalyst that decorates the substrate's surface. This is either done by dispersion of previously synthesized Au particles or by the coalescence of thin Au films. The latter are often done by depositing a very thin sub-nanometer layer of the catalyst film using physical vapor deposition being followed by a coalescence step using thermal annealing or a plasma treatment or the combination of both [13]. However, for compatibility reasons with normal CMOS device fabrication, also gold-free processes have been developed [14–16]. In the 1970's, it was postulated by Givargizov, that due to thermodynamic considerations there is a minimal critical diameter for growth [17]. It lasted until 1998 that Morales and Lieber [18] showed that silicon nanowires with diameters below 20 nm could be grown. A very detailed overview on the growth aspects of nanowires can be found in [11].

One advantage of the VLS method is that the growth can be done on different types of substrates. It has been shown, that thermodynamics dictate the crystal growth direction of the nanowire, even if growth occurs on amorphous substrates, i.e. without pre-defined lattice orientation. In addition, a correlation between crystal direction and nanowire diameter is clearly visible [19, 20]. Schmidt attributed this to the strong contribution of outer silicon atoms on the overall formation energies. When a silicon substrate is used, epitaxial growth can be achieved as well. Moreover, the grown wires can be subsequently transferred to any substrate even if the direct growth on that substrate is not possible. In that case, however, the original vertical nanowire arrangement cannot be maintained.

As alternative to CVD growth a wide variety of other growth methods can be applied using catalysts [9]. Among them are the annealing in a reactive atmosphere like hydrogen to form the nanowires directly from a silicon substrate [21], laser ablation [22] and molecular beam epitaxy [23].

For top-down fabrication of nanowires well-established technologies from silicon VLSI circuit technology can be applied. To form horizontal nanowires that are electrically isolated from the substrate, two approaches are commonly used. In the simplest approach, a SOI substrate is used and the nanowire is etched into the thin active silicon layer using an anisotropic etching process [24]. In the other approach bulk silicon and a deep reactive ion etch (DRIE) process are used together to structure a stack of nanowires [25]. Figure 1.3 shows both approaches schematically. The latter approach has the beauty that the footprint is small and there will be several parallel nanowires to carry the current in a device using nanowires from such a procedure. Figure 1.4 shows examples of nanowires created by both techniques.
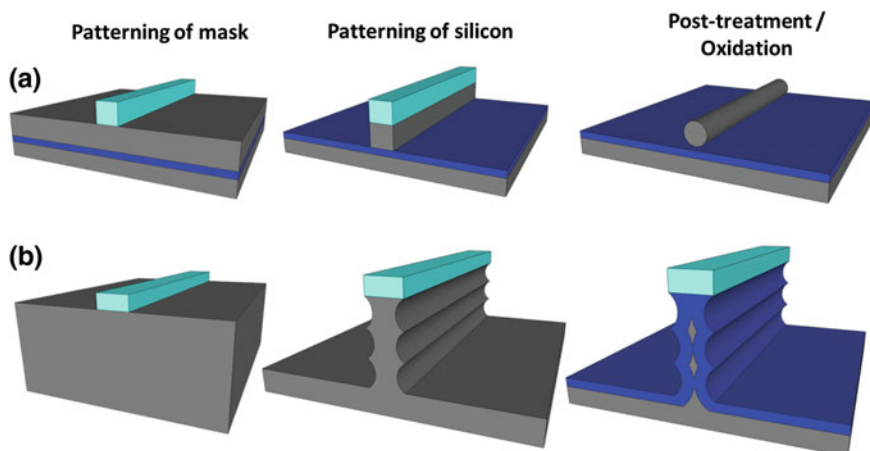

Fig. 1.3 Horizontal silicon nanowires fabricated by top down fabrication. **a** Starting with SOI substrate and etching using anisotropic reactive ion etching. **b** Starting with bulk substrate and etching with deep reactive ion etching and subsequent oxidation. Copyright © 2013 WILEY-VCH Verlag GmbH & Co. KGaA [1]
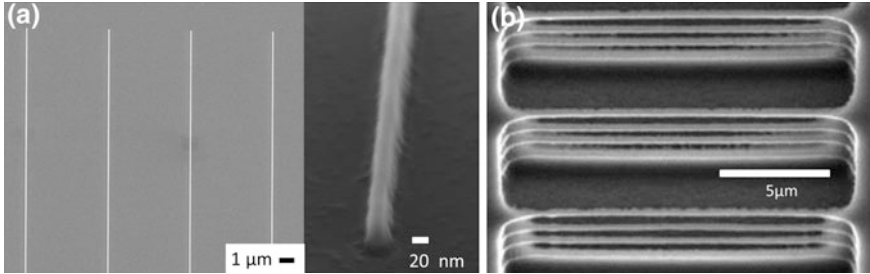
Fig. 1.4 Examples of horizontal silicon nanowires achieved by top-down fabrication. **a** Nanowires with 20 nm height and 25 nm widths produced using an SOI substrate. **b** Close up view of the nanowires form on the SOI substrate. **b** Nanowires formed using the deep reactive ion etch (DRIE) process © 2009 IEEE. Reprinted, with permission, from [25]

According to the above-described procedures the bottom-up fabrication will lead to a vertical arrangement of nanowires and the top-down arrangement will lead to a horizontal arrangement of nanowires. If horizontal nanowires have to be fabricated by the bottom-up technique, the alignment is very critical. In general the nanowires will be dispersed on the receiving substrate. For basic research, it can be sufficient to simply use a direct writing lithography technique to further built the required device. However, for mass fabrication an alignment of the structures will be required. Although some promising approaches have been shown, so far no technique for reliable mass fabrication is available. Therefore, the top-down approach seems to be the approach of choice for the mass fabrication of horizontal silicon wires using a silicon substrate. Also vertical wires can be achieved by using lithography and a subsequent anisotropic etching [26, 27], this technique has the drawback that very high aspect ratios have to be etched and dimensional control is very critical. On the other hand, the bottom-up approach naturally yields vertical devices [28] and the precise positioning can be controlled by a defined positioning of the catalyst particles. As an alternative, a template approach can be used to flexibly define vertical nanowire structures [29]. In that approach first a template layer has to be deposited. In [29] many different bottom-up techniques are described to fabricate such templates. The most popular being anodized aluminum oxidized (AAO) templates. However, also a suitable dielectric may be deposited and holes are etched into the layer using a top-down lithography process to form the template. Then the holes can be filled with the required nanowire material using a chemical vapour deposition process or epitaxial growth process. The drawback is that in case of a semiconducting nanowire like silicon the resulting nanowire will be poly-crystalline rather than a single crystal [30]. To achieve single crystals, the technique can be combined with bottom-up nanowire growth using a catalyst. If the holes are generated by a self-organization process, this again can be considered as a true bottom-up fabrication method.

Besides the fabrication of the nanowires themselves, a few critical processing steps have to be available to fabricate electron devices. The most important are: the

previous mentioned alignment of nanowires in case that bottom-up grown nanowires will be used, the doping of nanowires, the formation of contacts to the nanowires and finally the formation of a well-defined dielectric shell.

For alignment, a number of techniques have been proposed [31, 32]. Polar nanowires can be aligned in strong electric fields [33]. Dielectrophoresis has been used successfully for wire alignment [34, 35]. Microfluidic alignment [36], contact printing [37, 38] and Langmuir-Blodgett techniques can also be used [39–41]. Recently a nanoscale combing technique [42] showed encouraging results. However, all methods still face issues with either wire density for high integration or rather low yield of the desired structures or both [31]. Therefore, for high device densities comparable or beyond the state of the art, CMOS top-down approach is still the more preferred choice to define the nanowire location. However, for applications on flexible substrates or in sensors with parallel nanowires [38] some of the available procedures like contact printing could already be sufficient.

Doping of nanowire structures is also a critical issue. In modern CMOS fabrication, most doping steps are done using ion implantation. This, however, is not straightforward due to the geometry of silicon nanowires. Specifically the defined doping in a vertical arrangement is problematic. In bottom-up grown structures different options exist to dope the wires during growth. In case of catalyst-enabled growth, it is an intriguing idea to use the catalyst itself as dopant for the nanowire. In most cases only very low concentrations of the catalyst are actually transferred to the nanowire [10, 14]. Nevertheless, especially p-doping by using aluminum catalysts has recently shown very promising results [16]. In vapor phase processes, the doping can also be supplied by an additional precursor gas [43–45]. Care has to be taken to control the doping distribution both in radial an axial dimension [43].

To contact the nanowires a metal to nanowire contact is required. This can be the limiting factor for the device construction [46]. Using a metal silicide is very favorable method [47, 48]. Specifically intruded nickel silicide contacts offer a very technologically simple method of fabricating the metal to silicon nanowire contacts with sharp interfaces [48–50].

Finally in order to achieve reproducible device properties it is important to passivate the nanowire surface and form a good gate insulator for a field effect transistor (FET). The natural oxide of silicon is one of the main reasons why silicon has considerably outperformed every other semiconductor for high density and high performance circuits and systems [51]. Therefore, it is natural to also use silicon dioxide in silicon nanowire devices and indeed it can deliver excellent properties [52]. However, also here the higher k value of materials like hafnium dioxide (HfO_2), which is established in CMOS technologies today, is of benefit [53]. Atomic layer deposition (ALD) is the technique best suited to deposit dielectrics on nanowires since it can form conformal films on arbitrary geometries. Nanowire devices with aluminum (Al_2O_3), oxide and HfO_2 gate dielectrics have been demonstrated for device [54, 55], sensor [56] and nonvolatile memory applications [57]. Care has to be taken to carefully engineer the silicon/dielectric interface to avoid interface traps and charge trapping in the high-k layer. Another advantage of

deposited dielectrics is the possibility to combine them with different semiconductors like germanium or GaAs and enable their use despite of the absence of a high performance natural oxide like in the case of silicon.

1.3 Electron Devices Based on Silicon Nanowires

Silicon exhibits unique properties when it acquires a 1D shape. Quantum confinement of electrons and holes is predicted to be substantial only at aggressive diameters below of 3 nm [58]. Note that this is in contrast to III–V semiconductors, where confinement is visible already at larger diameters. Therefore, it makes sense to denote the behavior of Si nanowires as quasi 1D. The band structure is strongly modified for Si nanowires with diameters below of ~ 10 nm. The band gap increases for smaller diameters and a direct band gap can be obtained for sufficiently small diameters [58, 59]. The quasi 1D behavior of silicon nanowires with very small dimensions can be utilized in devices in many different ways. For field effect devices, when the gate electrode is wrapped around the nanowire, the optimum geometric gate coupling can be provided to the active region. In addition to this, if the silicon thickness is small enough to allow a full depletion at low voltages the best scaling behavior of the device can be achieved [60]. A useful parameter to characterize the gate control over the channel is the natural or screening length [61]. It describes the efficiency of bending the energy bands and depends on the gate geometry, gate dielectric, nanowire thickness and doping concentration. Depending on the density of states nanowire field effect devices can be designed to operate either in a classical gate capacitance limited mode or the quantum capacitance limit. In the latter the channel charge remains constant when scaling down the gate oxide thickness leading to an improved power to delay product [62].

Using scaled nanowires, very promising circuit demonstrations have already been shown [63, 64]. Another more conventional approach comes from semiconductor memories, especially NAND Flash. For decades, the dilemma between fast erase and retention is hindering the full success of charge trapping devices [65]. The underlying physical reason is that the field in the tunnel oxide and the top oxide cannot be controlled independently of each other like this can be done in a floating gate device. Generally speaking, it is necessary to enhance the field in the tunnel oxide and possibly at the same time reduce the field in the top oxide. Nanowires and to a lower extent tri-gates [66] offer a unique opportunity here, since the geometry will automatically generate a higher field at the bottom oxide and the extension of the field increase can be controlled by the diameter of the nanowire. Figure 1.5 illustrates that situation. Therefore, nanowire devices have been extensively explored for charge trapping devices. An excellent overview on the literature on that subject can be found in Chap. 3 of [67]. However, up to now the technological hurdle for introducing nanowires to push charge trapping applications is too high, as long as a cheaper scaling can be achieved using floating gates. Since almost ten years intense research has been started to explore the third dimension in NAND
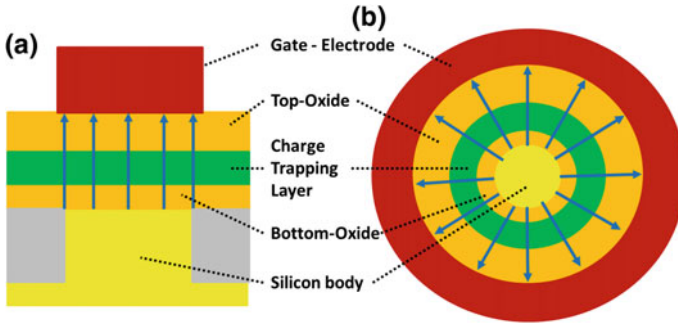
Fig. 1.5 Schematic cut in width direction of a planar (**a**) and a nanowire based (**b**) charge trapping memory cell. The *arrows* indicate the field lines in the device in programing or erase operation. In the nanowire device the field lines are denser in the bottom oxide. Therefore the exchange of carriers between the charge trapping layer and the silicon transistor body is enhanced and the charge exchange between the charge trapping layer and the gate-electrode is reduced

Flash memories, [30, 67] which might turn this cost per function relation. It was shown that by using concepts where many layers can be fabricated and then connected by a single or a few lithography steps is necessary to scale the cost into the desired range.

Many concepts have been proposed to reach that goal [67, 68]. In most of these, a charge-trapping layer is much easier to integrate then a floating gate. Here the nanowire geometry is beneficial. It has further been shown, that for the particular application the small dimensions enable the use of polycrystalline material for the transistor body [69]. This enables a rather simple fabrication technique where holes are etched into the layer stack and the holes are subsequently filled with polysilicon [30, 70]. The basic process is illustrated in Fig. 1.6. One variant of this concept has reached the market recently [71] and more devices are expected in the near future. Besides NAND Flash, the general concept can also be extended to other devices like resistive RAM (RRAM) [72]. Although not all applications can benefit from the nanowire geometry in the same way the charge trapping memory cell does, in most cases a nanowire like structure will be the result of this type of integration scheme.

Also logic devices benefit largely from the excellent gate control when implemented in a nanowire structure. However, for viable applications additional requirements have to be fulfilled. Thus, alternative concepts to the conventional MOSFET have emerged. The most important of these are illustrated in Fig. 1.7. With ever decreasing device dimensions doping becomes more and more problematic. On the one side the doping profiles need to be controlled much more precisely. However, due to diffusion during dopant activation an ideal steplike profile is hard to achieve even if very short millisecond annealing is used. Second, the number of dopants in the active channel region decreases. Since the relative variability will scale with $N^{-1/2}$ [73] doping fluctuations will make the control of the threshold voltage nearly impossible [74]. In addition to these difficulties, it has
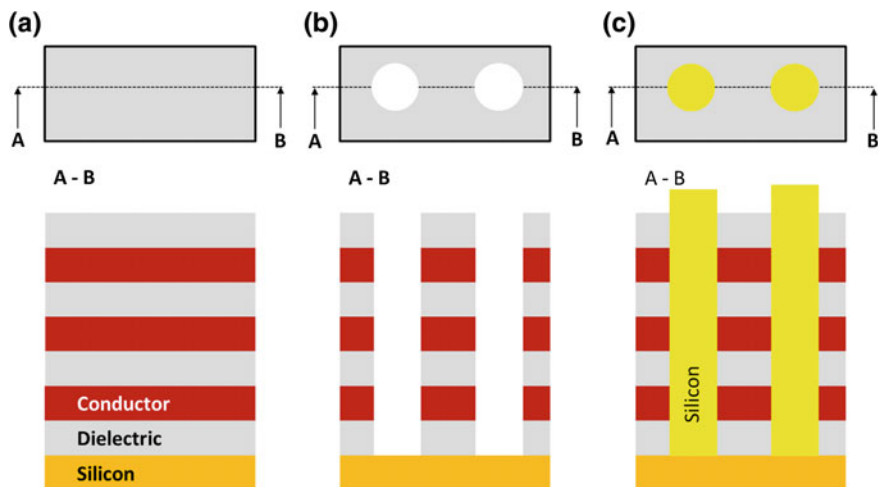
Fig. 1.6 Principle of stacking several layers and connecting them using a single lithography and etching step. The *upper row* shows the top view and the *lower row* shows the cross section according to the cut line A-B as indicated in the top view. The starting layer stack is shown in (**a**). After defining holes by lithography and etching the structure in (**b**) results. Finally the holes are filled again and the filling layer is polished back resulting in a nanowire structure inside the holes (**c**). The flow is strongly simplified to illustrate the basic principle and details like functional layers are omitted
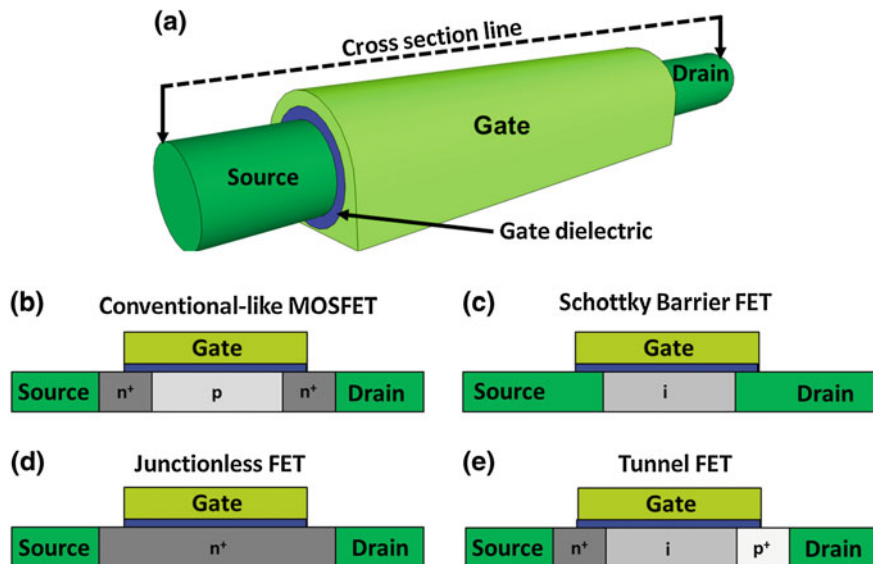

Fig. 1.7 Different options for electron devices using silicon nanowires. The top drawing **a** shows a generic 3-D view of a silicon nanowire device with metallic source/drain regions and the surrounding gate. The cross sections **b–e** illustrate different device concepts: **b** Conventional nanowire MOSFET, **c** Schottky Barrier FET, **d** Junctionless FET and **e** Tunnel FET. Copyright © 2013 WILEY-VCH Verlag GmbH & Co. KGaA [1]

been proven by calculations and experiments, that for certain nanowire geometries, the ionization energies of dopants are higher than in bulk [75, 76]. For nanowires without a surrounding gate dopant deactivation takes place, i.e. to achieve the same doping effect, a higher dopant concentration is needed, especially for thin nanowire diameters.

Both the Schottky barrier field effect transistor (SBFET) [77, 78] and the junctionless transistor [3] can help to control these issues. In the SBFET, the highly doped source and drain regions are replaced by metal-semiconductor Schottky junctions, and the silicon body of the transistor can be undoped. The device benefits from the nanowire geometry since very sharp and defined silicide junctions can be used [79]. For charge transport this implies that two energy barriers are introduced along the current path. The thickness of these barriers is efficiently controlled by the gate due to the electric field enhancement at the tip-like metal electrode geometry. The on-state for sufficiently small gate lengths is given by tunneling through the Schottky barriers, while the off-state is controlled by thermionic emission over a high and thick energy barrier. The undoped channel eliminates issues of threshold voltage control caused by doping fluctuations. In the junctionless device, the whole nanowire is highly doped. Thus, the formation of a very sharp junction in the scaled device is elegantly avoided. In contrast to conventional FETs, the on-state is driven in the accumulation mode, and the charge carriers flow throughout the complete nanowire cross-section. Doping fluctuation issues are reduced due to the much higher doping of the channel region.

One of the biggest challenges for further device scaling is the inability to scale the threshold voltage due to the thermal limit of 60 mV/dec for the subthreshold slope [80]. Since lowering the supply voltage is of very high importance both for physical device scaling and reduction of the power consumption it is one of the most pressing issues to find ways in order to reduce the subthreshold slope below this value. One promising option is the tunneling field effect transistor (TFET) [4, 81].

The TFET would also greatly benefit from the nanowire geometry. From an electrostatic point of view, the nanowire geometry with a surrounding gate stack facilitates sufficient band bending for band-to-band tunneling. Furthermore, for sufficiently small diameters the energy distribution of density of states exhibits van Hoove singularities. Hence, a comparatively high amount of states are available for band to band tunneling at the conduction and valence band edges. As the energetic window for band to band tunneling cuts the high energy tail of the Fermi distribution function, the tunnel FET principally enables a switching behaviour with a reduced subthreshold swing below 60 mV/dec at room temperature. However, like in Schottky FETs, the tunneling transmissibility through the energy barriers limits the on-current through the device. Therefore, from today's point of view TFET are alternatives for low operating power. Recently, encouraging results have been shown demonstrating a performance that is coming close to the requirements for an actual implementation [82, 83]. In a recent publication [84] the combination of a junctionless transistor and a tunnel FET is described, combining features of both device types.

There are two more aspects that make the use of nanowires in such devices very attractive. First, it is much easier to combine different semiconductors with
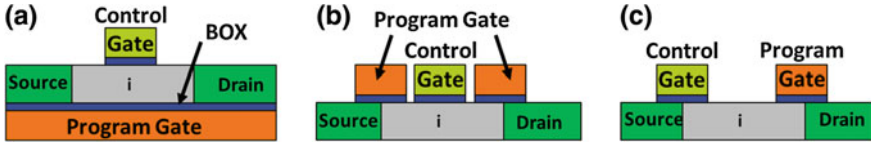
Fig. 1.8 Schematic cross sections of the different concepts for reconfigurable silicon nanowire devices. In the electrostatic doping device (**a**) the back gate is used to adjust the barrier heights and a top gate controls the current trough the device. The simultaneous control of both Schottky barriers (**b**) can also be accomplished by using top gates and an additional control gate in the middle then controls the carrier flow. In the RFET (**c**) approach the program gate above the drain junction and the control gate above the source junction control the polarity and the current flow respectively

considerable lattice mismatch in nanowires [85]. Second, nanowire devices can be constructed both in a horizontal and vertical arrangement. Both features have been exploited in [86, 87] where CMOS compatible nanowire structures using a Si/InAs heterostructure as a building block for TFETs are demonstrated.

All those devices target an improvement of the classical CMOS technology, exploiting the enhanced electrostatic control within the nanowire geometry. However, silicon nanowires also enable a new type of transistor, in which the device polarity can be controlled by an electrical signal [5, 52, 88, 89]. Therefore the same physical device can be used at different times as p-channel or n-channel transistor. These so called reconfigurable field effect transistors (RFET) hold the potential to lower the transistor count needed for the same functionality. The different concepts to build such a device are illustrated in Fig. 1.8 and briefly introduced in the following. Detailed discussions on the different concepts can be found in [1, 5].

In the electrostatic doping approach [88, 90–93], shown in Fig. 1.8a, the back-gate is used as program gate to select electron or hole transport. The program gate bends the silicon bands at both junctions simultaneously. Negative program gate voltages increase the barrier height at the conduction band and thereby block electrons. At the same time the energy barrier height for holes is the natural Schottky barrier height. Albeit, its thickness is diminished and thermal assisted tunneling of holes can take place. Correspondingly, positive program gate voltages block holes and enable electron injection. Once the program gate is set to a specific polarity, the top gate is then used to adjust the amount of current flowing from source to drain. The use of buried and common gates, as employed in Fig. 1.8a, implies having a comparatively weak gate coupling to the active region and therefore a high gate operation voltage. Moreover, the independent operation of neighboring devices, as required in integrated circuitry, can only be solved by substantial technological means leading to a limited scalability of this structure.

In the approach sketched in Fig. 1.8b [89, 94, 95], the two outer top gates are kept at the same potential and provide a similar function as the back gate in Fig. 1.8a. Thus, this concept allows the individual control of different devices in one chip. In the top-down realization a surrounding gate architecture is provided for both control and program gates [94]. Moreover, in a single device numerous
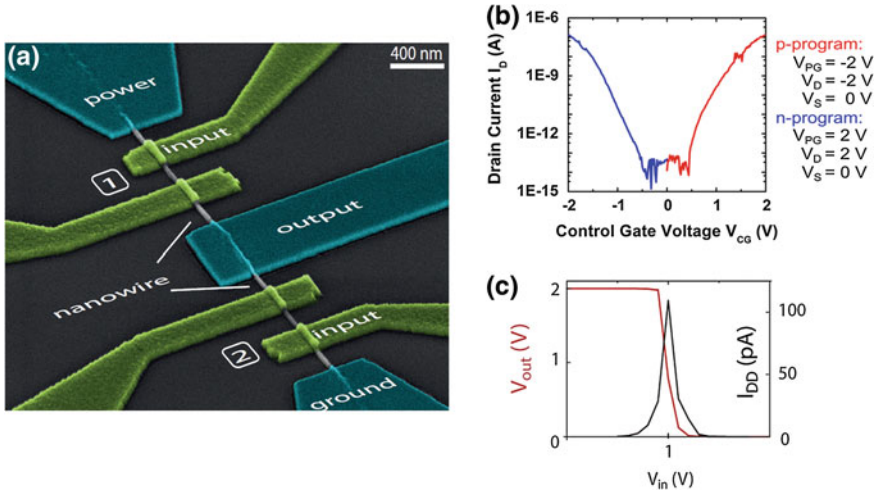
Fig. 1.9 Complementary inverter based on a symmetrical reconfigurable field effect transistor. **a** SEM image of the two identical RFET devices integrated into a single nanowire. In **b** the resulting transfer characteristics of the p-channel and the n-channel programmed devices is shown. In **c** the inverter transfer characteristic is shown together with the current through the inverter demonstrating that a cross current is flowing only during switching

nanowire channels are vertically stacked in parallel to enhance the drive current. The three gates can also be connected independently to allow the control of the threshold voltage of the device [95].

The RFET device shown in Fig. 1.8c uses two independent top gates each overlapping one of the Schottky junctions [52, 96]. One of them is used to control the polarity. The other is used to control the amount of current flowing through the device. In contrast to the other polarity control concepts and to conventional CMOS, the main part of the active region is ungated.

Recently significant progress has been made both in understanding and designing the appropriate transport mechanisms [97–99] and showing the benefit of building circuits out of the reconfigurable devices [100–102]. If CMOS circuits are to be constructed from such devices, it has to be considered, that the geometry cannot be adjusted according to an unbalanced current output of *p*-channel and *n*-channel devices since the same device has to be usable in both configurations. Therefore, the output has to be symmetrical for both carrier types. Using stress engineering this could be demonstrated in the approach with two top gates illustrated in Fig. 1.8c [103]. Figure 1.9 shows an inverter implemented in a single bottom-up fabricated nanowire using this symmetrical RFET device. CMOS functionality can be shown and identical characteristics are achieved if the role of the two devices is interchanged [103]. When comparing the performance of such devices to CMOS there is still a considerable gap due to the Schottky barrier approach. Here, again, the flexibility of integrating different materials into nanowires can be exploited by using germanium nanowires [104].

1.4 Silicon Nanowire Based Sensors

Generally speaking, a sensor device transforms a physical or chemical signal of the environment into an electrical signal [105]. Normally, the sensor device can be split into the active sensing part, which translates the input signal into an intermediate signal and the transducer that translates the intermediate signal into the final electrical signal. In many cases, the two parts are closely linked. The quasi 1-D properties of nanowires can be utilized in transducers and in some cases also for the active sensing part of the chain. Especially chemical and biochemical sensor research has intensively utilized silicon nanowires in the last decade [106]. But also mechanical sensors can benefit especially from the very high piezoresistance effect observed in silicon nanowires [107]. For example, accelerators that utilize the piezoresistance effect for transduction can be significantly improved [108]. Moreover, freestanding nanowires can be very good oscillators. Combined with the high piezoresistance this enables new classes of devices [109, 110].

The research on chemical and biochemical sensors is again strongly driven by the exploitation of the extremely high surface to volume ratio combined with excellent mechanical stability. Having in mind that excellent field effect transistor devices can be constructed, it is a natural consequence to apply the idea which Bergveld first explored in 1971 [111] in the ion sensitive field effect transistor (ISFET) to place the impedance conversion in potentiometric devices in direct vicinity of the measurement. Using classical planar devices, derivatives of this idea have been established as transducers for chemical [112] and biochemical sensors [113]. The transfer of these ideas to nanowire-based devices was therefore already demonstrated more than a decade ago [114]. For biochemical sensors the diameter of the nanowires can be as small as the species to be detected. As illustrated in Fig. 1.10. This enables a very high sensitivity of the sensor device even if parallel
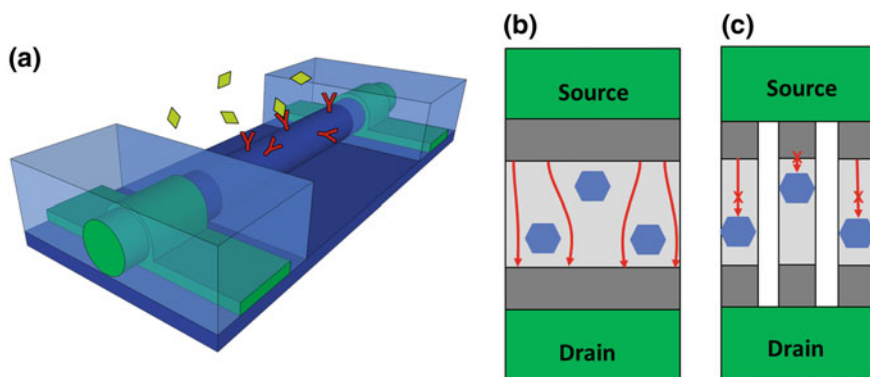

Fig. 1.10 Illustration of a chemical or biochemical sensor based on a nanowire field effect device. **a** Schematic showing the FET transducer receptors immobilized at the surface. **b** Top view of a sensor using conventional planar silicon technology. **c** Top view of nanowire sensor constructed from three parallel nanowires. *Red arrows* indicate current paths
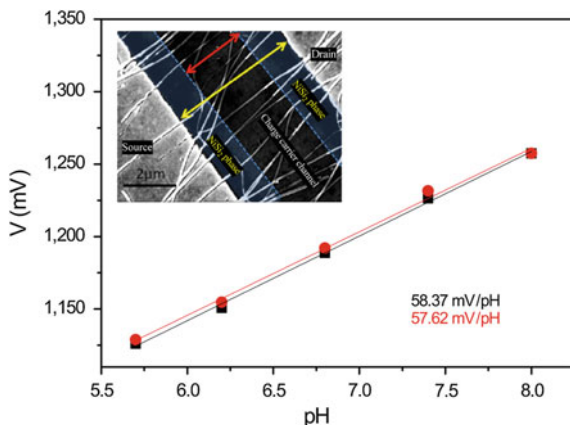
Fig. 1.11 Output voltage of a pH sensor using a parallel nanowire SBFET coated with aluminum oxide as a function of pH. The *red symbols* represent the values for rising pH and the *black symbols* show the values for decreasing pH. The *inset* shows an SEM top view of the used sensor. Reprinted with kind permission from Springer Science+Business Media: [116]

nanowires are used in order to increase the device current, since the current percolation paths are effectively blocked already by a single molecule per nanowire. Looking at a single nanowire this situation paves the way to single molecule detection as demonstrated in [115].

In Fig. 1.11, the response of a pH sensor using a Schottky barrier field effect device with parallel nanowires [38] and an aluminum oxide pH sensitive layer is shown [116]. Nearly Nernstian response is demonstrated for both rising and falling pH. A large number of different biosensors has been demonstrated using nanowire-based transducers, especially FETs [117–121]. The details of the sensing mechanisms and functionalization are beyond the scope of this chapter and the reader is referred to the references given. However, it is important to point out that nanowire based devices have their specific advantage when it comes to a very sensitive detection in small volumes and therefore can enable biosensors that are not possible using a planar transducer.

The small size, flexible fabrication and mechanical properties of nanowires can also be utilized to extend the functionality of biological sensors. Nanoscale FET devices can be integrated at the tip of a kinked silicon nanowire, as it is reported in [122–124]. Here, the nanoscale connections are made by the arms of the kinked nanostructure. However, the spatial resolution of such a device is limited. Therefore, the same group has presented an approach in which a SiO_2 nanotube is synthetically integrated on top of a nanowire FET. This nanotube penetrates the cell membrane, bringing the cell cytosol into contact with the FET, which is then able to record the intracellular trans-membrane potential [123].

1.5 Silicon Nanowire Based Solar Cells and Anodes for Li-Ion Batteries

Energy generation from renewable sources and storage of electrical energy are among the most pressing technical challenges for our society. These fields can benefit from silicon nanowires [9] as well, as they have the potential to increase the optical absorption and collection efficiency in solar cells [8, 125, 126]. Single nanowire solar cells can be used to study the parameters that influence the performance of nanowire based photovoltaics [126–129]. Additionally, they allow a seamless integration with nanowire based electronics and sensors [127, 128]. For doing general purpose solar cells, however, the single wire elements have to be arranged in large arrays [8, 131]. The potential of the single element to enable such a large scale assembly is therefore a strong differentiator for the different concepts. Therefore, the low cost bottom-up growth, which is compatible with different types of substrates, is the fabrication method of choice for such devices. In order to accomplish all the requirements, a coaxial structure is beneficial. First of all, the possibility to fabricate radial pn-junctions has shown promising results [132]. Figure 1.12 shows a schematic view of a silicon nanowire array based solar cell using this concept. Moreover, the flexibility of combining different materials in the nanowire arrangement is utilized as can be seen, for example, in [128]. Also classical heterojunction concepts using crystalline and amorphous silicon can easily be implemented [131].

Li-ion batteries are currently one of the best technical solutions to store electrical energy and retrieve it on a short and flexible timescale [133]. Up to date graphite is the standard anode material used in such batteries. However, theoretical calculations predict that silicon can improve the capacity by almost one order of magnitude.

The increased Li accommodation of up to 3.75 Li atoms per silicon atom comes together with a huge lattice expansion upon lithiation which results in more than 250 % volume expansion [9, 133]. This will lead to the pulverization of the anode during cycling. Figure 1.13a illustrates this for the case of a thin film anode. The
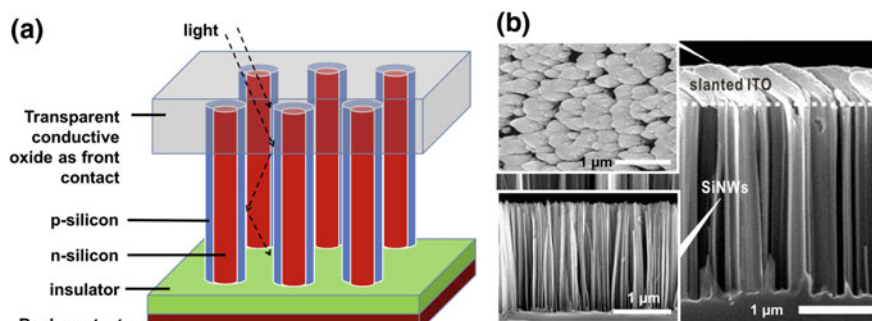

Fig. 1.12 a Schematic view of a silicon nanowire based solar cell with a radial pn-junction. **b** SEM micrographs from top view and cross section of the solar cell, as well as from the silicon nanowire array. © Optics Express, reprinted with permission from [130]
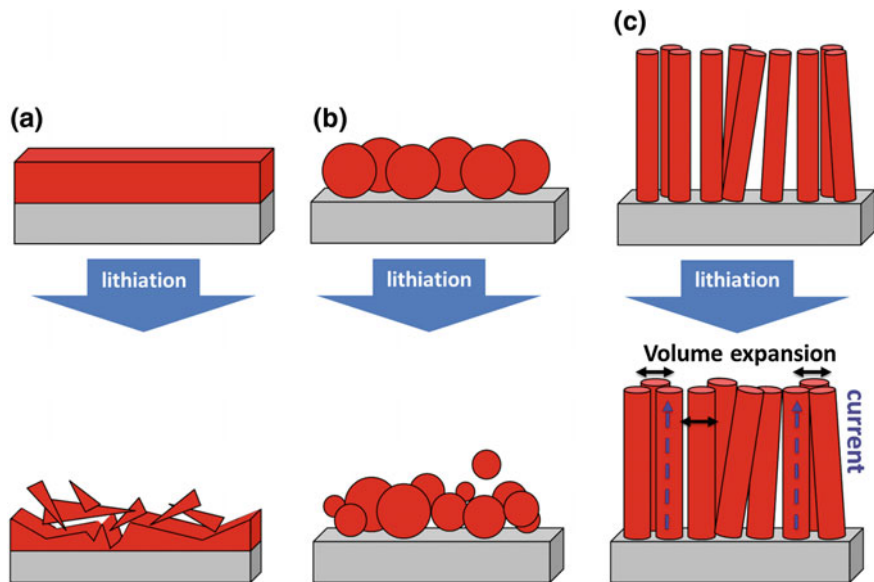
Fig. 1.13 Schematic illustration of the effect of volume expansion during lithiation of silicon [133]. Silicon applied as a thin film (**a**). The massive volume expansion destroys the film. Silicon applied as silicon nanoparticles (**b**). In this case there is room for expansion, but the electrical connection is lost. Silicon applied as silicon nanowires (**c**). For nanowires a radial expansion is possible while maintaining the vertical connection to the underlying substrate

breaking of the structure leads to an interruption of the current flow through the anode. Using silicon nanoparticles (Fig. 1.13b) can improve the cyclability. However, a certain amount of particles is released to the electrolyte and current flow towards the collector is limited. A nanowire on the other side can expand laterally and still maintain the current transport in the vertical direction (Fig. 1.13c) [108]. Excellent research results have been shown in half-cells, but the enhanced cyclability in full cells remains to be shown [9, 134–137]. Promising results with nanowires directly grown on carbon meshes were recently demonstrated [138]. For full cell operation, also the formation of the solid-electrolyte interface (SEI) at the silicon surface needs to be controlled, in order to tune the electrochemical reactions. Again, the flexibility in forming heterostructures including different materials can be utilized to enhance charge storage batteries [139, 140].

1.6 Summary

Silicon nanowires are quasi 1D structures with a diameter below 100 nm. They can be grown with high precision using bottom-up techniques. In addition, today's top down fabrication technology has reached the sub 100 nm nanoelectronic era in

2004 [141]. Therefore also classical lithography techniques can be used to fabricate silicon nanowires. Different devices can strongly benefit from the quasi 1D feature that is reflected by the high surface to volume ratio. The scaling of today's electronics can be enhanced by the ultimate gate control and the possibility to reduce the subthreshold slope below the thermal limit of 60 mV/dec. The vertical NAND Flash device is a first demonstration of nanowire like structures in mass production [71]. Though, in this case the nanowire results from a development coming from top-down microelectronics, but the effect of the nanowires is clearly present. It is expected that we will see more similar examples, where the top-down technologies are developed to a point such that the learning from the bottom-up nanowire research can be exploited in volume manufacturing. Additional, functionalities like reconfigurability can be added to silicon devices as well, based on the precise control of electrical field in such structures. Additionally in nanowire devices different semiconductor and insulator materials can be combined both in a radial and longitudinal fashion much more flexible than in bulk semiconductor technologies. In the framework of electron devices, this feature will allow to implement high mobility materials in a simpler way than in bulk technologies.

The high surface to volume ratio has the potential to design sensors that are much more sensitive than their planar counterparts. Especially biosensors, where very small amounts of analytes have to be detected in very small volumes, can benefit from this feature.

In solar cells, the light trapping is enhanced by forming radial structures, as the pn-junction can be placed much closer to the carrier generating region. In Li-ion batteries the potential of the very high lithium incorporation in silicon cannot be exploited in planar structures. Silicon nanowires also hold a unique opportunity in that field.

Besides the examples given in this chapter, there are many more potential applications like optical devices [142, 143], thermoelectric devices [144], catalysts [145] and even more [146]. It is therefore expected that silicon nanowire technology will evolve as a very versatile supplement to the existing silicon technology.

References

1. T. Mikolajick, A. Heinzig, J. Trommer, S. Pregl, M. Grube, G. Cuniberti, W.M. Weber, Silicon nanowires—a versatile technology platform. Phys. Status Solidi Rapid Res. Lett. **7**, 793–799 (2013)
2. N. Singh, K.D. Buddharaju, A. Agarwal, S.C. Rustagi, C.Q. Lo, N. Balasubramanian, D.L. Kwong, Fully gate-all-around silicon nanowire CMOS devices. Solid State Tech. **51**, 34 (2008)

3. J.-P. Colinge, C.-W. Lee, A. Afzalian, N.D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neil, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, R. Murphy, Nanowire transistors without junctions. Nat. Nanotechnol. **5**, 225–229 (2010)
4. M.T. Björk, J. Knoch, H. Schmid, H. Riel, W. Riess, Silicon nanowire tunneling field-effect transistors. Appl. Phys. Lett. **92**, 193504 (2008)
5. W.M. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube, T. Mikolajick, Reconfigurable nanowire electronics—a review. Solid State Electron. **102**, 12–24 (2014)
6. J. Izuan, A. Rashid, J. Abdullah, N.A. Yusof, R. Hajia, The development of silicon nanowire as sensing material and its applications. J. Nanomater. **2013**, 328093–32119 (2013)
7. F. Patolsky, C.M. Lieber, Nanowire nanosensors. Mater. Today **8**, 20–28 (2005)
8. M.D. Kelzenberg, S.W. Boettcher, J.A. Petykiewicz, D.B. Turner-Evans, M.C. Putnam, E.L. Warren, J.M. Spurgeon, R.M. Briggs, N.S. Lewis, H.A. Atwater, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications. Nat. Mater. **9**, 239–244 (2010)
9. K.-Q. Peng, X. Wang, L. Li, Y. Hu, S.-T. Lee, Silicon nanowires for advanced energy conversion and storage. Nano Today **8**, 75–97 (2013)
10. C. Mack, The future of semiconductor lithography? Look to flash. J. Micro/Nanolith. MEMS MOEMS **12**, 030101 (2013)
11. V. Schmidt, J.V. Wittemann, S. Senz, U. Goesele, Silicon nanowires: a review on aspects of their growth and their electrical properties. Adv. Mater. **21**, 2681–2702 (2009)
12. R.S. Wagner, W.C. Ellis, Vapor-liquid-solid mechanism of single crystal growth. Appl. Phys. Lett. **4**, 89–90 (1964)
13. W. Weber et al., Silicon nanowires: catalytic growth and electrical characterization. Phys. Stat. Sol. (b) **243**, 3340–33451-6 (2006)
14. F. Iacopi, P.M. Vereecken, M. Schaekers, M. Caymax, N. Moelans, B. Blanpain, O. Richard, C. Detavernier, H. Griffiths, Plasma-enhanced chemical vapour deposition growth of Si nanowires with low melting point metal catalysts: an effective alternative to Au-mediated growth. Nanotechnology **18**, 505307 (2007)
15. I. Zardo, S. Conesa-Boj, S. Estradé, L. Yu, F. Peiro, P. Roca i Cabarrocas, J.R. Morante, J. Arbiol, A. Fontcuberta i Morral, Growth study of indium-catalyzed silicon nanowires by plasma enhanced chemical vapor deposition. Appl. Phys. A **100**, 287–296 (2010)
16. O. Moutanabbir, D. Isheim, H. Blumtritt, S. Senz, E. Pippel, D.N. Seidman, Colossal injection of catalyst atoms into silicon nanowires. Nature **496**, 78–82 (2013)
17. E.I. Givargizov, Fundamental aspects of VLS growth. J. Cryst. Growth **31**, 20 (1975)
18. A.M. Morales, C.M.L. Lieber, A laser ablation method for the synthesis of crystalline semiconductor nanowires. Science **279**, 208–211 (1998)
19. V. Schmidt, S. Senz, U. Gösele, Diameter dependent growth direction of epitaxial silicon nanowires. Nano Lett. **5**, 931–935 (2005)
20. Y. Cui, L.J. Lauhon, M. Gudiksen, J. Wang, C.M. Lieber, Diameter controlled synthesis of single-crystal silicon nanowires. Appl. Phys. Lett. **78**, 2214–2216 (2011)
21. A.V. Sandulova, P.S. Bogoyavlenskii, M.I. Dronyuk, Preparation and some properties of whisker and needle-shaped single crystals of germanium, silicon and their solid solutions. Sov. Phys.-Sol. State **5**, 1883 (1964)
22. Y.F. Zhang, Y.H. Tang, N. Wang, D.P. Yu, C.S. Lee, I. Bello, S.T. Lee, Silicon nanowires prepared by laser ablation at high temperature. Appl. Phys. Lett. **72**, 1835–1837 (1998)
23. P. Werner, N.D. Zakharov, G. Gerth, L. Schubert, U. Gosele, On the formation of Si nanowires by molecular beam epitaxy. Int. J. Mat. Res. **97**, 1008–1015 (2006)
24. F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao, Y.-C. Yeo, Y. Li, J.-W. Lee, P. Chen, M.-S. Liang, C. Hu, 5 nm-Gate nanowire FinFET. IEEE Symposium VLSI Technology, pp. 196–197 (2004)
25. D. Sacchetto, M.H. Ben-Jamaa, G. De Micheli, Y. Leblebici, Fabrication and characterization of vertically stacked gate-all-around Si nanowire FET arrays. IEEE

Proceedings European Solid State Device Research Conference ESSDERC, pp. 245–248 (2009)

26. C. Pan, Z. Luo, C. Xu, J. Luo, R. Liang, G. Zhu, W. Wu, W. Guo, X. Yan, J. Xu, Z.L. Wang, J. Zhu, Wafer-scale high-throughput ordered arrays of Si and coaxial Si/Si1–xGex wires: fabrication, characterization, and photovoltaic application. ACS Nano **5**(8), 6629–6636 (2011)

27. J. Nakamura, K. Higuchi, K. Maenaka, Vertical Si nanowire with ultra-high-aspect-ratio by combined top-down processing technique. Microsyst. Tech. **19**, 433–438 (2013)

28. J. Goldberger, A.I. Hochbaum, R. Fan, P. Yang, Silicon vertically integrated nanowire field effect transistors. Nano Lett. **6**, 973–977 (2006)

29. H. Shang, G. Cao, Template-based synthesis of nanorod or nanowire arrays. Handbook of Nanotechnology, pp. 161–178 (Springer, New York, 2007)

30. H. Tanaka, M. Kido, K. Yahashi, M. Oomura, R. Katsumata, M. Kito, Y. Fukuzumi, M. Sato, Y. Nagata, Y. Matsuoka, Y. Iwata, H. Aochi, A. Nitayama, Bit cost scalable technology with punch and plug process for ultra high density flash memory. IEEE Symposium VLSI Technology, pp. 14–15 (2007)

31. R.G. Hobbs, N. Petkov, J.D. Holmes, Semiconductor nanowire fabrication by bottom-up and top-down paradigms. Chem. Mater. **24**, 1975–1991 (2012)

32. M.C.P. Wang, B.D. Gates, Directed assembly of nanowires. Mater. Today **12**, 34–43 (2009)

33. C.H. Lee, D.R. Kim, X. Zheng, Orientation-controlled alignment of axially modulated pn silicon nanowires. Nano Lett. **10**, 5116–5122 (2010)

34. E.M. Freer, O. Grachev, X. Duan, S. Martin, D.P. Stumbo, High-yield self-limiting single-nanowire assembly with dielectrophoresis. Nat. Nanotechnol. **5**, 525–530 (2010)

35. S. Raychaudhuri, S.A. Dayeh, D. Wang, E.T. Yu, Precise semiconductor nanowire placement through dielectrophoresis. Nano Lett. **9**, 2260–2266 (2009)

36. Y. Huang, X. Duan1, Q. Wei, C.M. Lieber. Directed assembly of one-dimensional nanostructures into functional networks. Science **291**, 630–633 (2001)

37. Z. Fan, J.C. Ho, Z.A. Jacobson, R. Yerushalmi, R.L. Alley, H. Razavi, A. Javey, Wafer-scale assembly of highly ordered semiconductor nanowire arrays by contact printing. Nano Lett. **8**, 20–25 (2008)

38. S. Pregl, W.M. Weber, D. Nozaki, J. Kunstmann, L. Baraban, J. Opitz, T. Mikolajick, G. Cuniberti, Parallel arrays of Schottky barrier nanowire field effect transistors: nanoscopic effects for macroscopic current output. Nano Res. **6**, 381–388 (2013)

39. D. Whang, S. Jin, Y. Wu, C.M. Lieber, Nano Lett. **3**, 1255–1259 (2003)

40. A. Tao, F. Kim, C. Hess, J. Goldberger, R. He, Y. Sun, Y. Xia, P. Yang, Nano Lett. **3**, 1229–1233 (2003)

41. S. Acharya, A.B. Panda, N. Belman, S. Efrima, Y. Golan, A semiconductor-nanowire assembly of ultrahigh junction density by the Langmuir-Blodgett technique. Adv. Mater. **18**, 210–213 (2006)

42. J. Yao, C.M. Lieber, A nanoscale combing technique for the large-scale assembly of highly aligned nanowires. Nat. Nanotechnol. **8**, 329–335 (2013)

43. S.T. Picraux, S.A. Dayeh, P. Manandhar, D.E. Perea, S.G. Choi, Silicon and germanium nanowires: growth, properties, and integration. JOM **62**, 35–43 (2010)

44. J. Wallentin, M.T. Borgström, Doping of semiconductor nanowires. J. Mater. Res. **26**, 2142–2156 (2011)

45. V. Robbins, D. Taylor, C. Wanqing, A. Fischer-Colbrie, P. Chungdee, S. Ahmed, D. Stumbo, VLS growth of Si nanowires with in-situ doping for MOS transistors. IEEE-NANO Conference Nanotechnology, pp. 326–329 (2009)

46. H. Park, R. Beresford, R. Ha, H.-J. Choi, H. Shin, J. Xu, Evaluation of metal–nanowire electrical contacts by measuring contact end resistance. Nanotech. **23**, 245201 (2012)

47. Y. Cui, Z. Zhong, D. Wang, W.U. Wang, C.M. Lieber, High performance silicon nanowire field effect transistors. Nano Lett. **3**, 149–152 (2003)

48. W.M. Weber, L. Geelhaar, E. Unger, C. Chèze, F. Kreupl, H. Riechert, P. Lugli, Silicon to nickel-silicide axial nanowire heterostructures for high performance electronics. Phys. Status Solidi (b) **244**, 4170–4175 (2006)
49. W.M. Weber, L. Geelhaar, A.P. Graham, E. Unger, G.S. Duesberg, M. Liebau, W. Pamler, C. Chèze, H. Riechert, P. Lugli, F. Kreupl, Silicon-nanowire transistors with intruded nickel-silicide contacts. Nano Lett. **6**, 2660–2666 (2006)
50. W. Tang, B.M. Nguyen, R. Chen, S.A. Dayeh, Solid-state reaction of nickel silicide and germanide contacts to semiconductor nanochannels. Semicond. Sci. Technol. **29**, 054004 (2014)
51. A.I. Kingon, J.-P. Maria, S.K. Streiffer, Alternative dielectrics to silicon dioxide for memory and logic devices. Nature **406**, 1032–1038 (2000)
52. A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, W.M. Weber, Nano Lett. **12**, 119–124 (2012)
53. S.T. Chandra, N.B. Balamurugan, Performance analysis of silicon nanowire transistors considering effective oxide thickness of high-k gate dielectric. J. Semicond. **35**, 044001-1 (2014)
54. P. Hashemi, J.T. Teherani, J.L.Hoyt, Investigation of hole mobility in gate-all-around Si nanowire p-MOSFETs with high-κ/metal-gate: effects of hydrogen thermal annealing and nanowire shape. IEEE International Electron Devices Meeting (IEDM), Digest Technology Papers, pp. 34.5.1–34.5.4 (2010)
55. J.W. Sleight, S. Bangsaruntip, G. Cohen, A. Majumdar, Y. Zhang, S. Engelmann, N. Fuller, L. Gignac, S. Mittal, J. Newbury, T. Barwicz, M.M. Frank, M. Guillorn, High performance and highly uniform metal Hi-K gate-all-around silicon nanowire MOSFETs. ECS Trans. **28**, 179–189 (2010)
56. B.R. Dorvel, B. Reddy Jr, J. Go, C.D. Guevara, E. Salm, M.A. Alam, R. Bashir, Silicon nanowires with high-k hafnium oxide dielectrics for sensitive detection of small nucleic acid oligomers. ACS Nano **6**, 6150–6164 (2012)
57. X. Zhu, D. Gu, Q. Li, D.E. Ioannou, H. Baumgart, J.S. Suehle, C.A. Richter, Silicon nanowire NVM with high-k gate dielectric stack. Microelectron. Eng. **8**, 1957–1960 (2009)
58. Y.M. Niquet, A. Lherbier, N.H. Quang, M.V. Fernández-Serra, X. Blase, C. Delerue, Electronic structure of semiconductor nanowires. Phys. Rev. B **73**, 165319 (2006)
59. D.D.D. Ma, C.S. Lee, F.C.K. Au, S.Y. Tong, S.T. Lee, Small-diameter silicon nanowire surfaces. Science **299**, 1874–1877 (2003)
60. K.J. Kuhn, Considerations for ultimate CMOS scaling. IEEE Trans. Electron Devices **59**, 1813–1828 (2012)
61. C.P. Auth, J.D. Plummer, Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's. IEEE Electron Device Lett. **18**, 74 (1997)
62. J. Knoch, M.T. Björk, H. Riel, H. Schmidt, W. Riess, One-dimensional nanoelectronic devices—towards the quantum capacitance limit. IEEE Proceedings Device Research Conference, pp. 173–176 (2008)
63. S. Bangsaruntip, A. Majumdar, G.M. Cohen, S.U. Engelmann, Y. Zhang, M. Guillorn, L.M. Gignac, S. Mittal, W.S. Graham, E.A. Joseph, D.P. Klaus, J. Chang, E.A. Cartier, J.W. Sleight, Gate-all-around silicon nanowire 25-stage CMOS ring oscillators with diameter down to 3 nm. IEEE Symposium VLSI Technology, pp. 21–22 (2010)
64. S.C. Rustagi, N. Singh, W.W. Fang, K.D. Buddharaju, S.R. Omampuliyur, S.H.G. Teo, C.H. Tung, G.Q. Lo, N. Balasubramanian, D.L. Kwong, CMOS inverter based on gate-all-around silicon-nanowire MOSFETs fabricated using top-down approach. Electron Device Lett. **28**, 1021–1024 (2011)
65. T. Mikolajick, M. Specht, N. Nagel, T. Mueller, S. Riedel, F. Beug, T. Melde, K.-H. Küsters, The future of charge trapping memories. Proceedings VLSI-TSA, pp. 130–133 (2007)
66. M. Specht, R. Kömmling, F. Hofmann, V. Klandzievski, L. Dreeskornfeld, W. Weber, J. Kretz, E. Landgraf, T. Schulz, J. Hartwich, W. Rösner, M. Städele, R.J. Luyken, H. Reisinger, A. Graham, E. Hartmann, L. Risch, Novel dual bit tri-gate charge-trapping memory devices. IEEE Electron Device Lett. **25**, 810 (2004)

67. B. Prince, *Vertical 3D Memory Technologies* (Wiley, Chichester, 2014)
68. Forward Insights, How 3D NAND stacks up, Report No. FI-NFL-3DM-0114 2014
69. J. Fu, Y. Jiang, N. Singh, C.X. Zhu, G.Q. Lo, D.L. Kwong, Polycrystalline Si nanowire SONOS nonvolatile memory cell fabricated on a gate-all-around (GAA) channel architecture. IEEE Electron Device Lett. **30**, 246–249 (2009)
70. M. Ishiduki, Y. Fukuzumi, R. Katsumata, M. Kito, M. Kido, H. Tanaka, Optimal device structure for pipe-shaped BiCS flash memory for ultra high density storage device with excellent performance and reliability. IEEE International Electron Devices Meeting (IEDM) Technology Digest, pp. 625–628 (2009)
71. K.-T. Park et al., Three-dimensional 128 Gb MLC vertical NAND flash-memory with 24-WL stacked layers and 50 MB/s high-speed programming. IEEE International Solid-State Circuits Conference (ISSCC) Digest Technology Papers, pp. 334–335 (2014)
72. A. Nitayama, H. Aochi, Bit cost scalable (BiCS) technology for future ultra high density memories. International Symposium VLSI Technology, Systems, and Applications (VLSI-TSA), pp. 1–2 (2013)
73. T. Mikolajick, H. Ryssel, Influence of statistical dopant fluctuations on MOS transistors with deep submicron channel lengths. Microelectron. Eng. **21**, 419–422 (1993)
74. T. Mikolajick, V. Häublein, H. Ryssel, The effect of random dopant fluctuations on the minimum channel length of short-channel MOS transistors. Appl. Phys. A **64**, 555–560 (1997)
75. M. Diarra, Y.-M. Niquet, C. Delerue, G. Allan, Ionization energy of donor and acceptor impurities in semiconductor nanowires; importance of dielectric confinement. Phys. Rev. B **75**, 045301 (2007)
76. M.T. Björk, H. Schmid, J. Knoch, H. Riel, W. Riess, Donor deactivation in silicon nanostructures. Nat. Nanotech. **4**, 103–107 (2009)
77. S.M. Koo, M.D. Edelstein, Q. Li, C.A. Richter, E.M. Vogel, Silicon nanowires as enhancement mode Schottky barrier field effect transistors. Nanotech. **16**, 1482–1485 (2005)
78. J. Knoch, J. Appenzeller, Impact of the channel thickness on the performance of Schottky barrier metal–oxide–semiconductor field-effect transistors. Appl. Phys. Lett. **81**, 3082 (2002)
79. W. Tang, S.A. Dayeh, S.T. Picraux, J.Y. Huang, K.-N. Tu, Ultrashort channel silicon nanowire transistors with nickel silicide source/drain contacts. Nano Lett. **12**, 3979–3985 (2012)
80. M.B. Das, Physical limitations of MOS structures. Solid-State Electron. **12**, 305–336 (1969)
81. A.M. Ionescu, H. Riel, Tunnel field-effect transistors as energy-efficient electronic switches. Nature **479**, 329–337 (2011)
82. L. Knoll, M. Schmidt, Q.T. Zhao, S. Trellenkamp, A. Schäfer, K.K. Bourdelle, S. Mantl, Si tunneling transistors with high on-currents and slopes of 50 mV/dec using segregation doped $NiSi_2$ tunnel junctions. Solid-State Electron. **84**, 211–215 (2013)
83. L. Knoll, Q.-T. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schafer, D. Esseni, L. Selmi, K.K. Bourdelle, S. Mantl, Inverters with strained Si nanowire complementary tunnel field-effect transistors. IEEE Electron Device Lett. **34**, 813–815 (2013)
84. B. Ghosh, M.W. Akram, Junctionless tunnel field effect transistor. IEEE Electron Device Lett. **34**, 584–586 (2013)
85. J.K. Hyun, S. Zhang, L.J. Lauhon, Nanowire heterostructures. Ann. Rev. Mater. Res. **43**, 451–479 (2013)
86. M. Borg, H. Schmid, K.E. Moselund, G. Signorello, L. Gignac, J. Bruley, C. Breslin, P. Das Kanungo, P. Werner, H. Riel, Vertical III–V nanowire device integration on Si(100). Nano Lett. **14**, 1914–1920 (2014)
87. K.E. Moselund, H. Schmid, C. Bessire, M.T. Björk, H. Ghoneim, H. Riel, InAs-Si nanowire heterojunction tunnel FETs. IEEE Electron Device Lett. **33**, 1453–1455 (2012)
88. F. Wessely, T. Krauss, U. Schwalke, CMOS without doping: multi-gate silicon-nanowire field-effect-transistors. Solid State Electron. **70**, 33–38 (2012)

89. M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici, G. De Micheli, Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs. IEEE International Electron Devices Meeting (IEDM), pp. 8–4 (2012)
90. U. Schwalke, T. Krauss, F. Wessely, CMOS without Doping on SOI: multi-gate Si-nanowire transistors for logic and memory applications. ECS J. Solid State Sci. Technol. **2**, Q88–Q93 (2013)
91. A. Colli, A. Tahraou, A. Fasoli, J.M. Kivioja, W.I. Milne, A.C. Ferrari, Top-gated silicon nanowire transistors in a single fabrication step. ACS Nano **3**, 1587–1593 (2009)
92. F. Wessely, T. Krauss, U. Schwalke, Reconfigurable CMOS with undoped silicon nanowire midgap Schottky-barrier FETs. Microelectron. J. **44**, 1072–1076 (2013)
93. M. Mongillo, P. Spathis, G. Katsaros, P. Gentile, S. De Franceschi, Multifunctional devices and logic gates with undoped silicon nanowires. Nano Lett. **12**, 3074–3079 (2012)
94. M. De Marchi, D. Sacchetto, J. Zhang, S. Frache, P.-E. Gaillardon, Y. Leblebici, G. De Micheli, Top-down fabrication of gate-all-around vertically-stacked silicon nanowire FETs with controllable polarity. IEEE Trans. Nanotec. **13**, 1029–1038 (2014)
95. J. Zhang, M. De Marchi, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, G. De Micheli, Polarity-controllable silicon nanowire transistors with dual threshold voltages. IEEE Trans. Electron Devices **61**, 3654–3660 (2014)
96. W.M. Weber, A. Heinzig, J. Trommer, M. Grube, F. Kreupl, T. Mikolajick, Reconfigurable nanowire electronics-enabling a single CMOS circuit technology. IEEE Trans. Nanotech. **13**, 1020–1028 (2014)
97. J. Beister, A. Wachowiak, A. Heinzig, J. Trommer, T. Mikolajick, W.M. Weber, Temperature dependent switching behaviour of nickel silicided undoped silicon nanowire devices. Phys. Status Solidi (c) **11**, 1611–1617 (2014)
98. D. Martin, A. Heinzig, M. Grube, L. Geelhaar, T. Mikolajick, H. Riechert, W.M. Weber, Direct probing of Schottky barriers in Si nanowire Schottky barrier field effect transistors. Phys. Rev. Lett. **107**, 216807 (2011)
99. J. Zhang, M. De Marchi, P.E. Gaillardon, G. De Micheli, A Schottky-barrier silicon FinFET with 6.0 mV/dec subthreshold slope over 5 decades of current. Proceedings International Electron Devices Meeting (IEDM) 2014
100. J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick, W.M. Weber, Elementary Aspects for circuit implementation of reconfigurable nanowire transistors. IEEE Electron Device Lett. **35**, 141–143 (2014)
101. M. De Marchi, J. Zhang, S. Frache, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici, G. De Micheli, Configurable logic gates using polarity controlled silicon nanowire gate-all-around FETs. IEEE Electron Device Lett. **35**, 880–882 (2014)
102. P.-E. Gaillardon, L. Amáru, J. Zhang, G. De Micheli, Advanced system on a chip design based on controllable-polarity FETs. Design, Automation Test Europe Conference (DATE) 2014
103. A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm, W.M. Weber, Dually active silicon nanowire transistors and circuits with equal electron and hole transport. Nano Lett. **13**, 4176–4181 (2013)
104. J. Trommer, A. Heinzig, A. Heinrich, P. Jordan, M. Grube, S. Slesazeck, T. Mikolajick, W. M. Weber, Material prospects of reconfigurable transistor (RFETs)—from silicon to germanium nanowires. MRS Proceedings, p. 1659 (2014)
105. W. Göbel, J. Hesse, J.N. Zerne (eds.), *Sensors, a Comprehensive Survey*, vol. 1. Fundamentals (VCH-Verlag, Weinheim, 1989)
106. J.I.A. Rashid, J. Abdullah, N.A. Yusof, R. Hajian, The development of silicon nanowire as sensing material and its applications. J. Nanomater. **3**, 1–16 (2013)
107. R. He, P. Yang, Giant piezoresistance effect in silicon nanowires. Nat. Nanotechnol. **1**, 42–46 (2006)
108. M. Messina, J. Njuguna, Potential of silicon nanowires structures as nanoscale piezoresistors in mechanical sensors. IOP Conference Series Material Science Engineering **40**, 012038 (2012)

109. X.L. Feng, R. He, P. Yang, M.L. Roukes, Very high frequency silicon nanowire electromechanical resonators. Nano Lett. **7**, 1953–1959 (2007)
110. R. He, X.L. Feng, M.L. Roukes, P. Yang, Self-transducing silicon nanowire electromechanical systems at room temperature. Nano Lett. **8**, 1756–1761 (2008)
111. P. Bergveld, Development of an ion-sensitive solid-state device for neurophysiological measurements. IEEE Trans. Biomed. Eng. **17**, 70 (1970)
112. P.-K. Shin, T. Mikolajick, H. Ryssel, pH sensing properties of ISFETs with silicon nitride sensitive-gate. J. Electrical Eng. Inf. Sci. **2**, 82–87 (1997)
113. T. Vering, W. Schuhmann, H.-L. Schmidt, T. Mikolajick, T. Falter, H. Ryssel, J. Janata, Field-effect transistors as transducers in biosensors for substrates of dehydrogenases. Electroanalysis **6**, 953–956 (1995)
114. Y. Cui, Q. Wei, H. Park, C.M. Lieber, Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species. Science **293**, 1289–1292 (2001)
115. F. Patolsky, G. Zheng, O. Hayden, M. Lakadamyali, X. Zhuang, C.M. Lieber, Electrical detection of single viruses. Proc. Natl. Acad. Sci. USA **101**, 14017–14022 (2004)
116. F.M. Zörgiebel, S. Pregl, L. Römhildt, J. Opitz, W. Weber, T. Mikolajick, L. Baraban, G. Cuniberti, Schottky barrier-based silicon nanowire pH sensor with live sensitivity control. Nano Res. **7**, 263–271 (2014)
117. K.-I. Chen, B.-R. Li, Y.-T. Chen, Silicon nanowire field-effect transistor-based biosensors for biomedical diagnosis and cellular recording investigation. Nano Today **6**, 131–154 (2011)
118. G.-J. Zhang, Y. Ning, Silicon nanowire biosensor and its applications in disease diagnostics: a review. Anal. Chim. Acta **749**, 1–15 (2012)
119. B.-R. Li, C.-W. Chen, W.-L. Yang, T.-Y. Lin, C.-Y. Pan, Y.-T. Chen, Biomolecular recognition with a sensitivity-enhanced nanowire transistor biosensor. Biosens. Bioelectron. **45**, 252–259 (2013)
120. T.-S. Pui, A. Agarwal, F. Ye, Y. Huang, P. Chen, Nanoelectronic detection of triggered secretion of pro-inflammatory cytokines using CMOS compatible silicon nanowires. Biosens. Bioelectron. **26**, 2746–2750 (2011)
121. A.K. Wanekaya, W. Chen, N.V. Myung, A. Mulchandan, Nanowire-based electrochemical biosensors. Electroanalysis **18**, 533–550 (2006)
122. B. Tian, T. Cohen-Karni, Q. Qing, X. Duan, P. Xie, C.M. Lieber, Three-dimensional, flexible nanoscale field-effect transistors as localized bioprobes. Science **13**, 830–834 (2010)
123. X. Duan, R. Gao, P. Xie, T. Cohen-Karni, Q. Qing, H.S. Choe, B. Tian, X. Jiang, C.M. Lieber, Intracellular recordings of action potentials by an extracellular nanoscale field-effect transistor. Nat. Nanotech. **7**, 174–179 (2012)
124. Q. Qing, Z. Jiang, L. Xu, R. Gao, L. Mai, C.M. Lieber, Free-standing kinked nanowire transistor probes for targeted intracellular recording in three dimensions. Nat. Nanotech. **9**, 142–147 (2014)
125. L. Tsakalakos, J. Balch, J. Fronheiser, B.A. Korevaar, O. Sulima, J. Rand, Silicon nanowire solar cells. Appl. Phys. Lett. **91**, 233117 (2007)
126. M.D. Kelzenberg, D.B. Turner-Evans, B.M. Kayes, M.A. Filler, M.C. Putnam, N.S. Lewis, H.A. Atwater, Photovoltaic measurements in single-nanowire silicon solar cells. Nano Lett. **8**, 710–714 (2008)
127. B. Tian, X. Zheng, T.J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, C.M. Lieber, Coaxial silicon nanowires as solar cells and nanoelectronic power sources. Nature **449**, 885–889 (2007)
128. T.J. Kempa et al., Semiconductor nanowires: a platform for exploring limits and concepts for nano-enabled solar cells. Energy Environ. Sci. **6**, 719–733 (2013)
129. B.Z. Tian, T.J. Kempa, C.M. Lieber, Single nanowire photovoltaics. Chem. Soc. Rev. **38**, 16–24 (2009)
130. Y.-J. Lee, Y.-C. Yao, C.-H. Yang, Direct electrical contact of slanted ITO film on axial p-n junction silicon nanowire solar cells. Opt. Express **21**, A7–A14 (2012)

131. X. Hua, Y. Zeng, W. Wang, W. Shen, Light absorption mechanism of c-Si/a-Si Half-coaxial nanowire arrays for nanostructured heterojunction photovoltaics. IEEE Trans. Electron Devices **61**, 4007–4013 (2014)
132. E.C. Garnett, P. Yang, Silicon nanowire radial p-n junction solar cells. J. Am. Chem. Soc. **130**, 9224–9225 (2008)
133. C.M. Hayner, X. Zhao, H.H. Kung, Materials for rechargeable lithium-ion batteries. Annu. Rev. Chem. Biomol. Eng. **3**, 445–471 (2012)
134. C.K. Chan, H. Peng, G. Liu, K. McIlwrath, X.F. Zhang, R.A. Huggins, Y. Cui, High-performance lithium battery anodes using silicon nanowires. Nat. Nanotech. **3**, 31–35 (2008)
135. R. Szczech, S. Jin, Nanostructured silicon for high capacity lithium battery anodes. Energy Environ. Sci. **4**, 56–72 (2011)
136. V. Etacheri, R. Marom, R. Elazari, G. Salitra, D. Aurbach, Challenges in the development of advanced Li-ion batteries: a review. Energy Environ. Sci. **4**, 3243–3262 (2011)
137. H. Wu, Y. Cui, Designing nanostructured Si anodes for high energy lithium ion batteries. Nano Today **7**, 414–429 (2012)
138. A. Krause, M. Grube, J. Brueckner, H. Althues, T. Mikolajick, W.M. Weber, Stability and performance of heterogeneous anode assemblies of silicon nanowires on carbon meshes for battery applications. MRS Proceedings (2015)
139. T.D. Bogart, D. Oka, X. Lu, M. Gu, C. Wang, B.A. Korgel, Lithium ion battery performance of silicon nanowires with carbon skin. ACS Nano **8**, 915–922 (2014)
140. L.-F. Cui, R. Ruffo, C.K. Chan, H. Peng, Y. Cui, Crystalline-amorphous coreshell silicon nanowires for high capacity and high current battery electrodes. Nano Lett. **9**, 491–4955 (2009)
141. B. Hoefflinger, Chips 2020: a guide to the future of nanoelectronic. Springer Science and Business Media (2012)
142. D. Ramos, E. Gil-Santos, O. Malvar, J.M. Llorens, V. Pini, A. San Paulo, M. Calleja, J. Tamayo, Silicon nanowires: where mechanics and optics meet at the nanoscale, Sci. Rep. **3**, 3445 (2013)
143. E. Baek, S. Pregl, M. Shaygan, L. Römhildt, W.M. Weber, T. Mikolajick, D.A. Ryndyk, L. Baraban, G Cuniberti, Optoelectronic switching of nanowire-based hybrid organic/oxide/semiconductor field-effect transistors. Nano Research (2014)
144. A.I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W.A. Goddard, J.R. Heath, Silicon nanowires as efficient thermoelectric materials. Nature **451**, 168–171 (2008)
145. Y. Liu, G. Ji, J Wang, X. Liang, Z. Zuo, Y. Shi, Fabrication and photocatalytic properties of silicon nanowires by metal-assisted chemical etching: effect of H_2O_2 concentration. Nanoscale Res. Lett. **7**, 663 (2012)
146. M. Shao, D.D.D. Ma, S.-T. Lee, Silicon nanowires—synthesis, properties, and applications. Eur. J. Inorg. Chem. **27**, 4264–4278 (2010)