Chapter 5
Conclusions and Recommendations

Abstract This chapter presents the conclusions and gives recommendations for future research based on the insight gained during this study.

5.1 Conclusions

As most of the ADCs nowadays are designed for a specific application, exploiting signal and system properties which are a priori known offers opportunities for architecture innovation to further enhance the ADC performance in terms of better accuracy, higher speed, lower power consumption and smaller die size. Previous works that exploit specific properties of signals and systems for this purpose were studied and summarized in Chap. 2. We conclude that this so-called '*signal-aware*', '*system-aware*' or '*application-aware*' ADC design approach that exploits specific properties of signals and systems to enhance performance is promising.

Power reduction techniques at circuit and architecture level for thermal noise limited ADCs in advanced CMOS technologies were studied and summarized in Chap. 3. We conclude that the approach of improving the voltage efficiency of thermal noise limited ADCs is an effective way to enhance the ADC power efficiency for a desired SNR.

By exploiting the statistical amplitude properties of multi-carrier signal and combined with architecture innovation, a parallel-sampling architecture was introduced to enhance the voltage efficiency of the ADC for multi-carrier systems. The knowledge of the parallel-sampling architecture for multi-carrier signals is upgraded by analytical analysis and simulations. We conclude that the parallel-sampling architecture can improve significantly the linear input signal range of an ADC (even beyond the linear signal range of the ADC sampling stage and internal amplifier stages) and it can also be used to improve the SNCDR of an ADC for multi-carrier signals in a power and area efficient way. Four implementation options of the parallel-sampling ADC architecture were proposed, which include an implementation

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option with run-time adaptation to allow sub-ADCs sharing between different signal paths to further improve ADC power efficiency compared to previous works [1, 2].

Architecture studies and circuit implementations of a parallel-sampling first stage for a 200MS/s 12 b switched-capacitor pipeline ADC using 65 nm CMOS technology and a parallel-sampling frontend stage for a 4GS/s 11 b time-interleaved ADC using 40 nm CMOS technology were presented in Chap. 4. From circuit simulations and analysis, we prove that the linear input signal range of the proposed ADCs with a parallel-sampling stage can be enlarged by a factor of two or even more compared to their sub-ADCs without getting excessive clipping distortion. Simulation results showed at least 6 dB improvement of the ADC's dynamic range and about 6 dB improvement of NPR for a multi-carrier signal. This improvement is achieved by less than half the power consumption and silicon area that would have been required when using the conventional approach with larger devices to lower the noise power, which proves the parallel-sampling ADC architecture can effectively improve the power efficiency of noise limited ADCs for multi-carrier signals.

A prototype IC was implemented to demonstrate the feasibility of designing a GHz sample rate and noise-limited ADC with the parallel-sampling architecture and the advantage of this architecture in enhancing the power efficiency of noise-limited ADCs for multi-carrier systems. The experimental IC contains two 1 GS/s 11 b sub-ADC with a parallel-sampling frontend and a run-time signal-range detection path. Experimental results show that each of its sub-ADCs achieves thermal-noise limited SNR of above 54 dB for input frequencies up to 1.5 GHz (third Nyquist zone) and the frontend stage of the ADC demonstrates state-of-the-art linearity performance (SFDR > 65 dB up to 1.5 GHz and >55 dB up to 3 GHz). Experimental results show that the dynamic range of the ADC is improved by 6 dB compared to its sub-ADC for both a single sinusoid signal and a broadband multi-carrier signal, and the NPR is improved by 5 dB compared when digitizing a multi-carrier signal with large crest factors at a cost of only about two times increase in power and area (compared to at least four times using the conventional approach with larger devices to lower the noise power). The experimental results are compared with prior art with similar performance (with sample rate at least 1GS/s and SNDR more than 48 dB), using the Schreier FOM and the conversion efficiency (P/f_s). This experiment proofs the feasibility of designing a parallel-sampling ADC in this performance range and the advantage of this architecture in enhancing the power efficiently of a state-of-art GS/s ADC (refers to its sub-ADC, reused from [5]) for a better performance for multi-carrier systems.

5.2 Recommendations for Future Research

Due to the demand and challenges observed, designing more advanced ADCs will still be an active research topic and the concept of exploiting specific signal and system properties to enhance ADC performance for a specific application will be

useful to bridge the gap. We suggest several directions for further work based on the insight gained during this research:

- The parallel-sampling architecture can be extended to include signal conditioning blocks in front of the ADC. Signal conditioning blocks, such as analog filters, LNA and PGA, require a high dynamic range and high sensitivity simultaneously. They also consume significant power and occupy large chip area compared to the ADC. Previous works have demonstrated enhancement techniques for analog filters based on similar ideas [3, 4]. It would be an interesting research topic to combine these techniques to yield a better baseband solution.
- Other ADC performance enhancement techniques for specific signals and systems, as summarized in Chap. 2 can also be combined with the parallel-sampling ADC architecture to further enhance the performance of ADCs in terms of better accuracy, higher flexibility or lower power consumption for a specific application.
- The signal-to-thermal-noise-power ratio of the ADC for converting multi-carrier signals is improved with the parallel sampling technique, but this does not include the noise due to jitter of the clocking circuits. Reducing jitter noise for high sample rate ADC requires significant power. Future work could also investigate the feasibility of applying the signal/system aware design approach to develop enhancement techniques for clocking circuits for a specific application.
- Furthermore, the concept of developing enhancement techniques for ADCs based on a priori information of the signal and system can also be applied to DACs which can be an interesting research topic as well.

References

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