# TEAChER: TEach AdvanCEd Reconfigurable Architectures and Tools

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**Abstract.** This paper presents an on-going collaboration project, named TEAChER for providing breakthrough knowledge to students and young researchers on reconfigurable computing and advanced digital systems. The project is intended to cover topics like architectures and capabilities of field-programmable gate arrays, languages for the specification, modeling, and synthesis of digital systems. Furthermore design methods, computer-aided design tools, reconfiguration techniques and practical applications are taught. The virtual laboratory enables the remote students to easily interact with a set of reconfigurable platforms in order to control experiments through the internet. By using the user-friendly interface, the remote user can change predefined system parameters and observe system response either in textual, or graphical format. In addition such a virtual laboratory includes a booking system, which enables remote users to conduct experiments in advance.

**Keywords:** Engineering education · Reconfigurable computing · Virtual prototyping · 3-D Architecture · CAD Algorithms · FPGA Prototyping

## 1 Introduction

The reconfigurable architectures and more specifically the Field-Programmable Gate Arrays (FPGAs) carry out a true revolution in the world of digital circuits. After being initially reserved almost exclusively for prototyping tasks, they are now very quickly evolving as an implementation medium for a great number of different demanding application domains. The key to their popularity is their feature to support application implementation by appropriately (re-)configuring the functionality of hardware resources. This allows FPGAs to provide higher flexibility, rapid product prototyping and significantly reduced non-recurring engineering (NRE) costs, as compared to Application-Specific Integrated Circuit (ASIC) devices.


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The characteristics and capabilities of these architectures have changed and improved significantly the last two decades from arrays of Look-Up Tables (LUTs), to heterogeneous devices that integrate a number of hardware components (e. g., LUTs with different sizes, microprocessors, DSP modules, RAM blocks, etc.). In other words, the logic fabric of an FPGA changed gradually from a homogeneous and regular architecture to a heterogeneous (or piece-wise homogeneous) device.

Such architectureal enhancements have been already taken into consideration from educational perspective, since the impact of FPGAs on different development directions is growing continuously. When FPGAs were first introduced, they were predominantly used for implementing simple random and glue logic, whereas nowadays even undergraduate students are capable of constructing quite complex digital devices on a single FPGA chip.

Usually, in the classical university curriculum there is a hard distinction between hardware and software: the former is under the responsibility of the electrical engineering (EE) or computer engineering (CE) department, whereas the latter is taught at the computer science (CS) department. However, nowadays with hardware/software co-design this clear-cut frontier is dissolving, requiring a fundamental change in the engineering curriculum. Towards this direction, a number of universities introduce lessons related to design of embedded systems, which has inherent the concept of hardware/software co-design.

In addition to this, there is a deep chasm between reconfigurable computing and the way, how classical computer science people look at parallelism. This situation is similar to the well-known hardware/software chasm. In education until recently reconfigurable computing has been subject of embedded systems, or System-on-Chip (SoC) design within EE departments, whereas most classical CS departments have ignored the enormous speed-up opportunities which can be obtained from this field. Only a few departments provide special courses mostly attended by a small percentage of graduate students.

Teaching reconfigurable architectures and CAD tools as part of embedded systems domain, are key driving innovation factor in leading European industry sectors, whereas the increased awareness of designing efficient embedded systems is also stated into a number of reports and road maps (e. g., ARTEMIS, HIPEAC, EUROPE2020, ITRS, etc). These documents highlight also the strategic decision about enhancing both the excellence, as well as the design of embedded systems in Europe, in order to improve the competitiveness of companies.

This paper describes a collaborative project between German (Karlsruhe Institute of Technology) and Greek (National Technical University of Athens) universities for developing educational material related to advanced reconfigurable architectures and CAD algorithms lessons. The emphasis (short and long term) for the outcomes of TEAChER project are summarized as follows:

- Increase the availability of educational material for topics related to the embedded systems community. This is further improved with the e-learning services introduced with the virtual laboratory.
- Provide training to young engineers, as well as to researchers through the transfer of breakthrough knowledge in embedded system technology. For this

purpose, lessons will be based on state-of-the-art reconfigurable architectures and CAD tools.
- Enable research and development of future and emerging technologies, such as 3-D integration, optical on-chip interconnects and system virtualization.
- Bring novel ideas in the embedded systems domain, which is one of the flagships of European industry. This is also expected to support the enhancement of Europe's position in the embedded system market.

Towards these directions, two complementary flavors of educational material will be developed during the TEAChER project. The first of them affects the programming of reconfigurable architectures. The second one deals with the design of reconfigurable architecture and the development of CAD algorithms used for architecture-level exploration and application mapping onto FPGA devices. Both of these flavors exhibit a lot of challenges that have to be sufficiently addressed in order to produce high-quality educational material. Among others, it is crucial to manage the distribution and the interactions between the technical and conceptual parts. For instance, in case the focus was mainly directed at technical skill development, then students would not have the ability to adapt their experience to other programming languages and environments, as well as to reuse programming strategies.

The educational material for programming reconfigurable architectures covers all the necessary programming models that enable students to ease the design of an ad-hoc component structure for a specific digital application. Furthermore, all the necessary mechanisms for improving performance (e. g., through parallelization, pipeline, etc), or reducing the development time (e. g., with the usage of a high-level synthesis tool) will also be covered. In contrast, the material for the second flavor puts emphasis on academic toolflows that enable the simulation of reconfigurable architectures. The requirement for academic tools relies mostly on the availability of source code for the employed CAD algorithms, which in turn enables students to model either more advanced reconfigurable platforms, or to introduce novel algorithms for application implementation onto them.

The paper is organized as follows: Section 2 highlights the motivation for this initiative, as well as the objectives that we aim to address during this 3-years project. The framework for designing 2-D/3-D reconfigurable architectures and the supported (both for exploration phase and for application mapping) CAD algorithms/tools are discussed in Section 3. Section 4 summarizes the topics of educational material. Sections 5 describes the underline platforms for supporting the customization of existing reconfigurable devices. The employed educational and pedagogical methods are described in Section 6. In Section 7 we show how emerging research fields can benefit from the TEAChER framework. Finally, Section 8 concludes the paper.

## 2 Motivation and Objectives of the TEAChER Project

The TEAChER project focuses clearly on modern learning and teaching methods to optimally provide state-of-the-art knowledge to young engineers and

researchers in order to enhance later their career prospects. For this purpose, within TEAChER project we aim to develop educational material, as well as to organize university lessons, for the domain of reconfigurable architectures and the supporting CAD algorithms/tools. Instead of focusing exclusively on conventional techniques found in existing lessons, we plan to incorporate in-house technology developed from other E.U. funded research projects that the consortium of TEAChER participated, in order to teach young researchers about how it is possible to employ state-of-the-art technologies to their designs.

This section highlights the open issues found in teaching reconfigurable architectures and CAD tools and proposes how these are addressed within this project.

*Transfer knowledge to young researchers, students, etc., based on the markets needs:* Since the participant laboratories from the German and Greek universities have already established a tight co-operation (through research activities and projects) with research institutes and R&D departments of companies in the domain of reconfigurable architectures across the whole Europe, it is expected that the students that attend these lessons will earn industry-oriented skills, which potentially would be crucial for new jobs. Moreover, by strengthening the state-of-the-art knowledge in the domain of reconfigurable architectures and the supporting CAD tools, we expect to improve the competitiveness of young researchers not only inside Germany and Greece, but worldwide.

*Disseminate the knowledge and tools developed during this project to the community of reconfigurable architectures:* This objective is one of the most important goals of the TEAChER project. By disseminating the educational material (e. g., books, software tools, etc) to the research community, it is possible to achieve the maximum possible visibility for the outcomes of this project. Such a selection was already applied by the two partners regarding the former version of toolflows developed during the AMDREL project, which are publicly available to the internet for online execution [16].

*Help universities with similar studies to improve their educational procedure:* Towards this goal, either the educational material developed from TEAChER project could be shared to other universities, or the partners of this project may participate to specialized lessons/workshops at these universities.

## 3 The TEAChER Framework

The consortium of the TEAChER project comprises partners with an impressive academic track record and proven expertise on a variety of fields related to reconfigurable architectures and CAD tools. Through joining of the above partners' fields of expertise, the TEAChER project will focus on the development of an educational material for teaching advanced topics in the design of reconfigurable architectures, as well as the software tools that automate the procedures

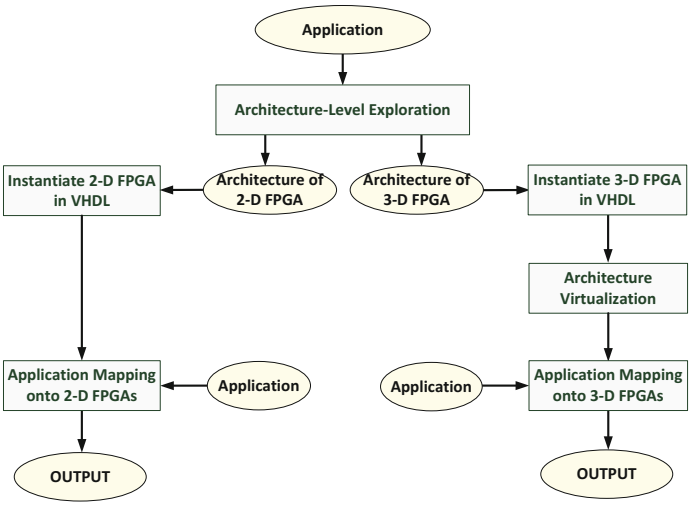


**Fig. 1.** Flow diagram for the topics addressed during the TEAChER project

of architecture-level exploration of these platforms and perform application mapping onto them, with the usage of state-of-the-art technologies.

Starting from an application, initially we perform architecture-level exploration in order to determine the most suitable reconfigurable architecture for application implementation. During this analysis, a number of application properties are identified. Among others, the memory requirements, the demands for supporting high-speed connectivity among distinct kernels, as well as the existence, or not, of complex arithmetic operations (e. g., floating-point operations) are identified.

The conclusions of this step provide an overview for the architectural organization of the target reconfigurable device. These parameters are appropriately handled in order to instantiate the FPGA implementation using the Hardware Description Language VHDL. An initial form of this description regarding the 2-D FPGA instantiation was already available to the consortium, due to previous collaboration between participating universities. However, for the scopes of the TEAChER project, this description should be appropriately modified in order to be used also for academic purposes.

In case we are studying the 2-D flow (see Figure 1 left), then the VHDL description of the Virtual FPGA (V-FPGA) is mapped onto an existing reconfigurable platform (e. g., provided by Altera or Xilinx), whereas the application mapping onto the V-FPGA is performed with the extended version of 2-D MEANDER flow [5]. Otherwise, when looking at the 3-D branch (see Figure 1 right), the VHDL description of the V-FPGA has to be appropriately modified in order to take into consideration inherent constraints posed by the third dimension (i. e., the existence of vertical connections that minimize the wire length of

long connections). Then, the V-FPGA is mapped onto an appropriate hardware platform (i. e., Virtex-7), which is aware about the 3-D integration Finally the actual application is implemented for the V-FPGA target platform (similar to the 2-D flavor of our methodology). The concept of V-FPGA is described in more detail in section 5.

## 4 Development of Educational Material for 3-D Reconfigurable Architectures and CAD Tools

For decades, semiconductor manufacturers have been shrinking the transistor size in Integrated Circuits (ICs) to achieve the yearly increases in performance described by Moores Law, which exists only because the RC delay was negligible, as compared to the signal propagation delay. For sub-micron technology, however, the RC delay becomes a dominant factor. Furthermore, a study by Magen et. al. has shown that at 130nm technology node approximately 51 % of the microprocessor's power is consumed by interconnect fabric [4]. This has generated many discussions concerning the end of device scaling as we know it today and has hastened the search for solutions beyond the perceived limits of current 2-D devices.

Three dimensional (3-D) chip stacking is considered by many as the silver bullet technology that will accommodate for all the aforementioned requirements [6]. Stacking multiple dies in the vertical axis and interconnecting them by using very fine-pitch Through Silicon Vias (TSVs) enable the creation of chips with very diverse functionalities implemented in different process technologies in a very small form factor. Introducing locality along the $z$-axis enables on average shorter interconnections between system components, which in turn leads to reduced signal propagation delay compared to conventional, i. e., 2-D, architectures [6]. Additionally, by stacking smaller dies rather than manufacturing a large planar die also leads to yield, hence cost, improvement because the probability that a die is defective is positively correlated with its size. Consequently, the shift from horizontal to vertical stacking of circuits has the potential to rewrite the conventions of electronics design. Although 3-D integration promises considerable benefits, several challenges need to be satisfied. Among others, new methodologies and software tools that support efficient design space exploration are required.

The educational material that will be developed towards this direction will cover the following topics:

- Improve interconnection networks for 3-D reconfigurable architectures [10].
- Design customized interconnection networks for 3-D reconfigurable architectures [11].
- Quantify the impacts of 3-D architectures with commercially available physical prototyping CAD tools (e. g., Cadence SoC Encounter) [1].
- Perform architecture-level exploration of 3-D reconfigurable architectures [8].
- Support fault-tolerance for 3-D reconfigurable architectures [13].

- Model thermal and reliability degradation in 3-D reconfigurable architectures [12].
- Design heterogeneous 3-D reconfigurable architectures [9].
- Develop CAD algorithms for application mapping onto 3-D reconfigurable architectures [7].
- Customize 3-D reconfigurable architectures through virtualization [14].
- Enhance 3-D reconfigurable architectures with Network-on-Chip topology [17].

## 5 Virtual Laboratories

The reconfigurable architecture and CAD algorithms courses in university departments face a significant challenge: the migration from theory to practice. This is especially crucial for lessons, which deal with boards that are usually difficult and too expensive to be bought by students. Any engineering curricula should present a significant level of practical component. The developed practical skills should inspire the students to, among other issues, test learned theoretical concepts, interact with equipment, and analyze experimental data. Within engineering disciplines, laboratory experiments are essential to apply the studied theory and observe the differences between studied models and real equipment.

Working in real laboratories, where the user interacts directly with the equipment by performing physical actions (e. g., manipulating with the hands, turning knobs, pressing buttons, etc) and receiving sensory feedback (e. g., visual, audio and tactile), similar to the case depicted in Figure 2(a) has become more and more expensive. Even though interacting with real equipment offers a higher level of training, more advanced educational techniques are absolutely necessary to be employed. In order to overcome the limited resources (human and material), the large number of students allocated to each experiment, as well as the time and space restrictions, alternative approaches for laboratory exercises have to be considered.

Towards this direction, it is feasible to provide the same interaction at a distance with the assistance of the remote infrastructure. This is a new layer that sits in between the student and the laboratory equipment. Such a layer is responsible for conveying user actions and receiving sensory information from the equipment, similar to the case depicted in Figure 2(b). The derived virtual laboratories incorporate also simulation environment in order to become an alternative to overcome the real laboratory disadvantages. Hence, they can be a good interactive medium, providing a good explanation of learned theoretical concepts.

A number of features are provided with the usage of such a virtual laboratory. Among others, the equipment is available worldwide 24 hour per day, there are no time or place restrictions, the laboratory infrastructure is maintained at a considerable low cost. Furthermore it provides flexibility and friendly user interface, while the students can, at any time, repeat the experiment and reevaluate their results.

We have to mention that the concept of virtual laboratory does not rely only on simulation environment. More specifically, even though such an approach can

accurately simulate real equipment (depending on the considered and/or developed models), the use of real laboratory experiments has an extra educational and pedagogical value, ensuring the reliability of the experiment.

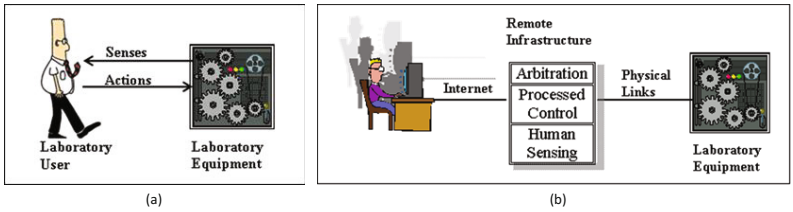


**Fig. 2.** Differences between traditional and virtual laboratories

### 5.1 Virtual 2D/3D FPGAs

Key role in this procedure plays the virtualization, which as we already mentioned recently becomes mainstream in the product development tool-chain. Thus, virtual platforms can sufficiently support concurrent hardware/software system design. In more details, the usage of virtualization enables to model a hardware platform, which might include different processing cores, memories, interconnection schemes, as well as various peripherals, in a form of a simulator. Figure 3 (left) depicts a schematic view of the employed architecture. Fundamental role in this architecture is given to the virtual FPGA (V-FPGA) architecture, which is an island-style FPGA. The architectural properties (e. g., the LUT size and the number of LUTs per slice) of each V-FPGA are customizable depending on the applications requirements.

The architecture of these V-FPGAs was developed at generic HDL-level and then mapped onto a Virtex-7 FPGA board. This, allows our system to incorporate features, such as partial reconfiguration at slice level, or the interconnection with 3-D process technology, which otherwise would not be available. Hence, the V-FPGA interacts as an intermediate layer for our solution, between the actual (fabricated) Virtex-7 platform and the applications. Additional details about the architecture of V-FPGA can be found in [3,15].

The educational material planned to be developed during the TEAChER project pays effort to teach students and new researchers about how to use such a virtual hardware (V-FPGA) in order to introduce additional features to existing (fabricated) devices, which would otherwise not be supported. Students will gain deep knowledge on FPGA architectures and will be able to build highly efficient systems with custom embedded FPGA fabrics. They will get deep insight in the special 2D/3D toolflow for future design methodologies, comprising computer aided design space exploration and dealing with trade-offs in area, performance, power, costs. Furthermore the students will learn and experience the design of heterogeneous system-on-chip solutions with hardware/software

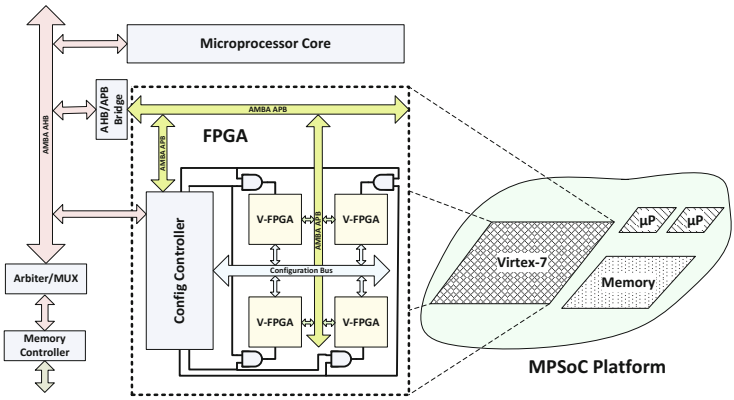


**Fig. 3.** The concept of V-FPGA

co-design methodologies, where one or more processor cores are interconnected on-chip with the reconfigurable hardware fabric, interacting with each other. Due to the virtualization layer, students will be able to quickly prototype the application specific system on off-the-shelf physical FPGAs.

### 5.2 Development of Academic Tools

During this project, a number of new tools will be released in order to support the educational procedure. The new tools will be developed under the GPL license in order to be easily redistributed to other universities with similar lessons, as well as to the interested researchers. This selection will contribute to the broad acceptance of the new tools, whereas the researchers (e. g., master/PhD students, engineers, etc) are expected to contribute also with content refinements and updates based on the actual demands posed by the research community.

Such an approach was already applied to the MEANDER framework [5], in which a number of CAD algorithms were actually developed from PhD students from different other than the original contributors' universities.

## 6 Employed Educational and Pedagogical Methods

Apart from conventional educational methodologies applied in the electrical engineering domain, during the TEAChER project we will develop also an e-learning solution. Thus the students will be able to remotely use the educational material, as well as the laboratory infrastructure (e. g., FPGA boards, CAD tools, etc). Towards this goal, a 'hybrid learning' approach is proposed, which refers to a solution, in which the traditional classroom time is reduced but not eliminated, and it is complemented with some online learning.

Next we summarize the main features of our online educational platform:

- Support synchronous e-learning, where all the participants (i. e., students) interact simultaneously in real-time.
- Support asynchronous e-learning, where the students are self-paced, allowing among other participants to engage in the exchange of ideas or information without the dependency of other participants' involvement at the same time.

Apart from the conventional technologies, which are used to facilitate e-learning, such as books, CD/DVD, etc, throughout the TEAChER project, we propose to use the virtual classroom. More specifically, the virtual classroom is formed by mixing a number of different communication technologies, such as web-conference software that enables students and instructors to communicate with each other via web cam, microphone, and real-time chatting in a group setting. Participants to this classroom are able to write on the board and even share their desktop, when given rights by the teacher. Similar communication technologies that are available in a virtual classroom include text notes, microphone rights, and breakout sessions, which enable the participants to work collaboratively in a small group setting to accomplish a task as well as allow the teacher to have private conversations with his or her students. The virtual classroom also will provide the opportunity for students to receive direct instruction from a qualified teacher in an interactive environment. Consequently, the students will be able to have direct and immediate access to their instructor for instant feedback and direction. In addition to this, the virtual classroom will provide a structured schedule of classes, which can be helpful for students who may find the freedom of asynchronous learning to be overwhelming. Another feature provided by the virtual classroom affects the opportunity to record a lesson. In such a case, each class is recorded and stored on a server, which allows for instant playback of any class over the course of the school year. This can be extremely useful for students to review material and concepts for an upcoming exam. This also provides students with the opportunity to watch any class that they may have missed, so that they do not fall behind.

## 7 Towards Future FPGA Technologies

The proposed TEAChER framework is able to address groups of various expertise level. Undergraduate students, new to the field of reconfigurable hardware, start with application development for a given hardware architecture. More advanced students dive into design space exploration with varying architectural parameters, tuning the target platform for specific objectives (e.g., performance, power, area, thermal distribution, etc.). Furthermore, the TEAChER framework encourages experts and researchers to cross the boundaries of state-of-the-art by developing and exploring future FPGA technologies. This is supported by deep parameterizable technology process models, as well as APIs for customizing the CAD toolflow. An emerging field of research that can early benefit from the TEAChER framework is Teratronics, which is briefly introduced in the following subsection.

### 7.1 Teratronics

Terahertz technology has become a highly emerging research field, surfacing the known knowledge of the advancing world and making it to step into the unexploited gap called Terahertz gap, that lies in full potential, sandwiching itself between the microwave and infrared frequency ranges. This unharnessed gap has led to the birth of a new field called Teratronics which convolves within the key aspects of electronics and photonics. The continuously growing FPGA domain with the blooming parallelization, pipelining and reconfiguration facilities is aimed to make its mark in the future scientific world by bringing terahertz frequency application into reality. However, for now, advances in the context of Teratronics are mainly on fundamental physical layer, dealing with low complexity. There is a big gap to the application domain and the system level, because today's and near future FPGAs are not meeting the Terahertz demands.

The TEAChER framework can support the researchers to close this gap by developing and exploring future FPGA technologies that incorporate latest promising breakthrough physical technologies, such as optical on-chip interconnects and 3D integration, combined with tailored reconfigurable architectures.

Furthermore, the Helmholtz International Research School of Teratronics [2] can use the TEAChER framework to train the young researchers on future FPGA technologies and toolflows, that are not yet manufactured and marketed, thus leveraging the advance in research. The first step of learning about reconfiguring the functionality of the hardware resources will motivate the students to peep into the frequency hopped region which lay as a stepping stone for the future innovations. The intelligence of system virtualization will not only aid the students in designing 3D architectures but also will facilitate them to implement their designed model with the required interconnects in virtual FPGAs (V-FPGAs). These highly efficient systems built on V-FPGAs will thereby assist the students to get connected to a higher bandwidth in a cost effective way, thereby triggering the terahertz frequencies into life.

## 8 Conclusions

In this paper we have presented a project, we call TEAChER, for developing educational material for teaching reconfigurable computing to undergraduate and postgraduate students. Since reconfigurable computing is a fast evolving discipline, such an approach is expected to be a key issue in order to offer companies well-educated, innovation aware, and highly concerned engineers. Moreover, newly developed tools will be released under the GPL license in order to be easily redistributed to other universities with similar lessons, as well as to the interested researchers or companies.

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