DynamIA: Dynamic Hardware Reconfiguration in Industrial Applications

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Abstract. This paper presents the work that will be done in the research project "DynamIA: Dynamic Hardware Reconfiguration in Industrial Applications". The project focuses on transferring knowledge on partial and dynamic reconfiguration of FPGAs from the academic partners to small and medium enterprises (SMEs), because the success stories on partial and dynamic reconfiguration were mainly only realized in large companies with a substantial amount of R&D activities. The reason is that the technology is still perceived as being difficult to adopt and expensive in terms of NRE costs. Therefore, the goal of the DynamIA project is two-fold. (1) It develops a number of use cases and guidelines in different application domains, tailored to the activities of the SMEs in the user group and in the broader target group. These use cases demonstrate a number of benefits of partial and dynamic FPGA reconfiguration, namely a faster startup, a faster design cycle and a lower occupation of resources leading to a lower static power consumption. (2) It develops a low-cost, vendor-independent emulation environment for dynamic and partial reconfiguration, which is non-existing in commercial and academic EDA tools. Another benefit of this emulation environment is that it can also be used for static designs. This allows SMEs to have a low-cost emulation environment for their applications instead of developing their own emulation environment manually (which is very time-consuming) or buying big cost-intensive commercial emulators.

Keywords: FPGA · Dynamic reconfiguration · Partial reconfiguration · Emulation platform

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1 Introduction

Dynamic and partial reconfiguration of FPGAs was introduced in the mid '90s [3,7]. By 'dynamic' reconfiguration we mean the reconfiguration of an FPGA at run-time. When a specific part of the FPGA is static, the reconfiguration is referred to as 'partial'. Typically, in systems that are partially dynamically reconfigurable, the static part contains a component that controls the reconfiguration of the dynamic part of the FPGA.

In the last decade, dynamic and partial reconfiguration of SRAM-based FPGAs has made major scientific and application-oriented progress through faster reconfiguration time, smaller granularity of the reconfigurable partitions, a large diversity of FPGAs that supports the technology and easier access to the technology through improved EDA tools. This resulted in a number of success stories that were mainly based on faster startup, faster design cycle, lower occupation of resources and lower static power consumption.

Faster startup. The larger the FPGA, the longer it takes to be reconfigured and operative after power-up. Many protocols such as PCI Express or CAN bus have very strict timing requirements, which cannot be fulfilled by starting up large FPGAs. In these cases partial reconfiguration can be used to allow a fast startup of the needed functionality, e.g. by first loading the PCI Express or CAN interface using partial reconfiguration and afterwards reconfiguring the rest of the FPGA. A method to improve the startup time of Xilinx FPGA is described in [4]. The approach described in this paper enables the startup of FPGA within 10ms, independently to the size of the device. This feature allows the deployment of large FPGAs in more applications as it was possible before.

Faster design cycle. Processing a large design takes a lot of time. A small modification in a subsystem of the design, forces the designer to go through the synthesis and place & route process all over again. Partial reconfiguration can offer a solution to this problem through an incremental design approach in which subsystems can be processed separately. This significantly decreases the time-to-market of FPGA-based electronic systems.

Lower occupation of resources and lower static power consumption. Dynamic and partial reconfiguration is very beneficial for systems, which have mutual exclusive functions. These functions can then be swapped in and out depending on the run-time requirements of the application. This way, smaller FPGAs can be used to save both costs as well as power consumption. One of the first applications benefiting from dynamic and partial reconfiguration was Software Defined Radio. Another application domain is image processing. Here dynamic and partial reconfiguration is used to reconfigure the digital image filters depending on the image content. The advantage for these kinds of systems are (1) no frames will be lost, as the camera interface stays active while the digital filter is reconfigured, and (2) as only parts of the FPGA are reconfigured this can happen so fast that between two frames the digital filter can be modified.

It turned out, however, that these success stories were mainly only realized in large companies with a substantial amount of R&D activities, while a lot of SMEs could also benefit from the use of the technology. The reason is that the

technology is still perceived as being difficult to adopt and expensive in terms of NRE costs. Therefore, the goal of this project is two-fold:

- It develops a number of use cases and guidelines in different application domains, tailored to the activities of the SMEs in the user group and in the broader target group. These use cases demonstrate the abovementioned benefits of partial and dynamic FPGA reconfiguration.
- It develops a low-cost, vendor-independent emulation environment for dynamic and partial reconfiguration, which is non-existing in commercial and academic EDA tools. Another benefit of this emulation environment is that it can also be used for static designs. This allows SMEs to have a low-cost emulation environment for their applications instead of either making their own emulation environment manually (which is very time-consuming) or buying big cost-intensive commercial emulators. On the other hand, the project shows that professional emulators like for example Synopsys' ChipIT are also capable to emulate dynamic and partial reconfigurable systems. A first approach was presented in [5].

This project was submitted to the CORNET call in September 2013. CORNET stands for COllective Research NETworking. It is a network for information exchange and collaboration between national and regional programmes for collective research in Europe. The objective is to promote close cooperation between the responsible national/regional ministries and agencies and to create opportunities for transnational collective research with national/regional funding. This means that CORNET partners in the participating countries/regions are working together to align programme conditions and procedures.

The CORNET coordination activities are financially supported by the German Federal Ministry of Economics and Technology (BMWi). The Belgian partners will receive funding from the Agency for Innovation by Science and Technology (IWT Flanders) and the German partners will receive funding from the German Federation of Industrial Research Associations (AiF). The project period is from January 1, 2015 to December 31, 2016. The consortium partners are the Katholieke Universiteit Leuven, the Vrije Universiteit Brussel, the Ruhr-University Bochum, the Hahn-Schickard-Gesellschaft e.V. (HSG-IMIT) and 10 SMEs in Flanders and Germany that support the project with their experience and use cases.

2 Economic Relevance for SMEs

2.1 Targeted Market Sector

The technology of dynamic and partial reconfiguration is commercially offered by Xilinx and Altera - vendors of FPGAs and tools that, together, represent almost 90% of the market share [2]. They represent an even larger market share in SRAM-based FPGAs, i.e. the only type of FPGAs with the technological capability of being dynamically reconfigured. After a company buys FPGAs and licenses, it can freely use dynamic and partial reconfiguration [1,8].

The direct target group of the project consists of SMEs that are active in the development of FPGA-based systems and sometimes also tools. In Flanders this means around 50 SMEs that have the absorption capacity to apply the project results in future products. In Germany we talk about several hundreds. The technology of dynamic and partial reconfiguration has only recently become mature enough to be beneficial in several application domains. Nevertheless, it requires a substantial effort for SMEs to adopt the technology. This project helps SMEs taking the first steps to product innovation based on dynamic and partial reconfiguration. The indirect target group are hundreds of companies and organizations that use FPGA-based end products. Through dynamic and partial reconfiguration these products become more efficient in terms of startup speed, power consumption and/or cost. The project DynamIA especially targets the development of cost effective possibilities to emulate dynamic reconfigurable systems. The current development process of dynamic and partial reconfigurable systems goes more or less over a trial and error process. A prototype is developed and the system is tested on it. In case of a re-design, a complete new prototype has to be developed. For prototyping, many solutions are on the market. E.g. Cadence and Synopsys offer systems which allow to prototype and emulate a digital system on several FPGAs. However, these systems don't support dynamic and partial reconfiguration. A recent research work however showed, that also these systems are capable to provide this feature [5]. With the introduction of this degree of freedom, also partially and dynamically reconfigurable systems can be emulated with these machines. However, the costs of such emulators are immense. Therefore DynamIA also targets to develop a cost efficient substitute for these professional emulators. For this purpose, standard off-the-shelf FPGA boards will be used to build the emulator architecture. Like in the professional emulators, the design has to be distributed over several FPGAs in case the design doesn't fit on one board. The dynamic and partial reconfiguration will be enabled with specific IP cores using the internal configuration access port of the used FPGAs. Fast interconnections between the boards are used to enable the communication of the distributed modules. A host PC is utilized as data source and sink. A tool flow, which will be developed within the project, performs the partitioning of the application and the generation of the different configuration bitstreams for the several boards and the partial bitstreams which will be loaded on demand. A scheduler on chip level performs the download of the bitstreams as described in [6]. The application scenarios come from different domains and are provided by the SMEs participating in the project as a part of the user group.

2.2 Economic Impact

The goal of the project is to improve the competitive position of Flemish and German SMEs by enabling them to develop products with a better performance (faster startup behavior, low power consumption, lower cost) and with a shorter design cycle (through an incremental design approach). The improved products and reduced NRE costs increase the turn-over of the companies and contribute to their growth. Furthermore, it is mandatory to enable SMEs in Belgium and

Germany the entry in an upcoming market which will definitely increase significantly in the next years. Reasons for this are the next revolution of the industry called Industry 4.0. Here novel kinds of embedded systems need to provide a computational platform which is able to keep strict deadline requirements, reliability and robustness. A further important requirement is the combination of domains such as process automation, factory automation, production and logistics. This comes into our daily lives with the "Internet of Things". If the SMEs are not ready as soon as these new systems are required, the huge companies take over this important market leading to another reduction of SMEs in Europe, which is definitely a huge drawback. DynamIA wants to help to lower the barrier for an entrance of SMEs into this beneficial and promising technology.

3 Research Approach and Expected Results

3.1 Research Approach

The innovation target consists of two aspects: (1) innovation of the SMEs' products and (2) development of an innovative emulation platform. The product innovation consists of designing and implementing new FPGA architectures that provide dynamic and partial reconfiguration and support run-time adaptation. On the one hand, these architectures increase the startup speed, shorten the design cycle, decrease the power consumption and/or reduce the resource occupation. On the other hand, the novel architectures need to have sufficient internal and/or external memory to store the configuration data. The use cases are chosen in different application domains and contain different architectural challenges such as intensive internal/external memory access, real-time processing requirements, computation intensive algorithms, specific interfacing requirements. The variety in the application domain and the architecture of the use cases guarantees the applicability for the SME target group. The SMEs in the user committee will be involved in fine-tuning the use cases in the first phase of the project. In parallel to the development of the use cases, techniques for emulating dynamic reconfiguration will be developed. For this purpose, a CHIPit prototyping system which consists of 6 large FPGAs in one system will be used to demonstrate the feature of dynamic and partial reconfiguration. CHIPit from Synopsys is originally meant for developing ASICs. However, it is possible to introduce dynamic reconfiguration into this emulator box. For this purpose the internal configuration access port is used to update the FPGA partially at run-time. This approach is fully new and would lead to a novel use case of this emulator. In a further step, the technique is used with individual FPGA evaluation boards. These boards, which can be obtained at low costs from e.g. Digilent, Avnet and Xilinx, can also be used as emulators. For this purpose, a novel technique to bring these boards into a network and distribute the reconfigurable system on it will be developed. The reason why the consortium wants to target this approach is the fact that cheaper boards are more attractive to SMEs and universities. However, the two options are envisioned in this project to be able to make a performance comparison between the CHIPit and the novel low-cost solution.

3.2 Expected Project Results

The result of DynamIA is the analysis, implementation and evaluation of applications using dynamic and partial reconfiguration. For the implementation and evaluation, tools and hardware methods will be developed in order to test the dynamicity of the system before an application-specific prototype is built. For this purpose, a design flow using the Synopsys CHIPit system will be developed which enables to perform dynamic and partial reconfiguration. In a further step, such a design flow will be developed for standard off-the-shelf FPGA boards. A free version of the flow will be provided for SMEs and academics. The implemented use cases will be described in application notes that allow reproduction.

4 Conclusion

DynamIA focuses on translating knowledge and expertise on dynamic and partial reconfiguration to Belgian and German SMEs. This will be done through the development of four use cases that represent different benefits of the technology. The use cases are from domains like sensor signal processing, embedded security, network of systems and image processing. This variety of applications enables a full exploration of the capability of dynamic reconfiguration and the required gain in experience to provide valuable feedback to the SMEs within the project. Low-cost emulation platforms will be developed and demonstrated through the use cases. These platforms can also be used for static designs and can be adopted by the SMEs as an alternative for expensive emulation platforms.

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