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Saleh Faruque

Radio Frequency Source Coding Made Easy

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Radio Frequency Source Coding Made Easy

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Preface

In communications engineering, source coding is the first step of processing input signals before transmission. The main focus of source coding is to:

- Identify
- Quantify
- Band limit
- Convert analog signals into digital format

The next step after source coding is to use:

- Forward error control coding (FECC) to detect and correct errors
- A suitable modulation scheme to transmit the modulated signal through an antenna.

Figure 1 illustrates the process. At the transmit side, the source coding is referred to as encoder. At the receive side, it is referred to as source decoder. It is a reverse process, which is not shown in the figure.

In this book, source coding is discussed in detail. Later books in this series will cover FECC and modulation.

Presented in this book are the salient concepts, underlying principles, and practical applications of source coding. In particular, this book will address the following topics as related to source coding:

- Identification and characterization of input signals such as analog signal, digital signal, and noise
- Signal-to-noise ratio and its effects in communication channels
- Shannon's capacity theorem and its attributes
- Measurement and quantification of signals
- Band limit filters based on active analog and MOS switched capacitor technology
- Nyquist sampling theorem
- Shannon's capacity theorem
- Quantization: linear and nonlinear

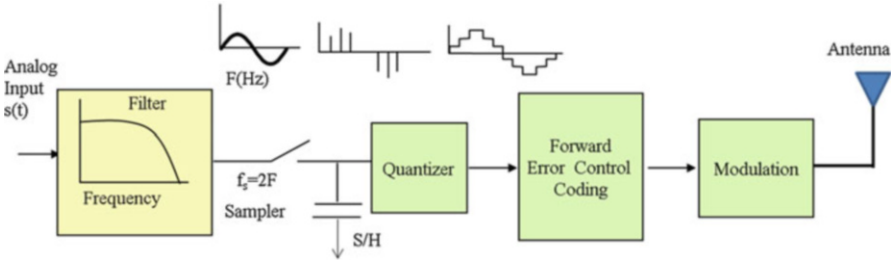

Fig. 1 A typical wireless communication system showing the source coding block along with FECC and modulation blocks

- Signal formats such as non-return to zero (NRZ) and return to zero (RZ) and their attributes
- Pulse code modulation (PCM)
- PCM hierarchy, T1-DS1, DS2, DS3, DS4, etc.
- PCM frame structure
- Frame synchronization
- PCM bandwidth
- Time division multiple access (TDMA). Both North American and European versions (GSM) are discussed to illustrate the multiplexing concepts used in different standards
- In the concluding chapter, a new multiple access technique, phase division multiple access (PDMA), is described to improve channel capacity
- The Fourier series and Fourier transform are integral parts of digital signal transmission in wireless communication in quantifying transmission bandwidth.
- As such, we have placed the Fourier series in Appendix A and the Fourier transform in Appendix B

This text has been primarily designed for electrical engineering students in the area of telecommunications and microelectronics. However, engineers and designers working in the area of active filters in the audio frequency range would also find this text useful. It is assumed that the student is familiar with the general theory of active networks: analog and digital.

In closing, I would like to say a few words about how this book was conceived. It came out of my long industrial and academic career. During my teaching tenure at the University of North Dakota, I developed a number of graduate-level elective courses in the area of telecommunications that combine theory and practice. This book is a collection of my courseware and research activities in wireless communications.

I am grateful to UND and the School for the Blind, North Dakota, for affording me this opportunity. This book would never have seen the light of day had UND and the State of North Dakota not provided me with the technology to do so. My heartfelt salute goes out to the dedicated developers of these technologies, who have enabled me and others visually impaired to work comfortably.

Finally, I would like to thank my beloved wife, Yasmin, an English Literature buff and a writer herself, for being by my side throughout the writing of this book and for patiently proofreading it. My darling son, Shams, an electrical engineer himself, provided technical support when I needed it. For this, he deserves my heartfelt thanks.

In spite of all this support, there may still be some errors in this book. I hope that my readers forgive me for them. I shall be amply rewarded if they still find this book useful.

Grand Forks, ND, USA Saleh Faruque

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Chapter 1
Introduction to Source Coding

Topics

- Introduction to Source Coding
- Signals and Spectra
- Noise and Interference
- Effects of Noise on Communication Circuits and Shannon's Capacity Theorem
- Measurement and Quantification of signals in Noise, Interference and Fading

1.1 Source Coding Defined

In communications engineering, source coding is the first step of processing input signals, (analog and/or digital). It identifies, quantifies, band limits, and converts the analog signals into Digital formats. Figure 1.1 shows the conceptual block diagram of a modern wireless communication system, where the source coding block is shown in the inset of the dotted block. At the transmit side, the source coding is referred to as encoder and at the receive side, it is referred to as source decoder.

Figure 1.2 shows the basic functional block diagram of a typical source coding. It Involves:

- Identification and Characterization of input signals
- Band limiting the input signal by means of filters
- Sampling and Quantization the input signal
- A/D-D/A Conversion
- Estimation of Bandwidth

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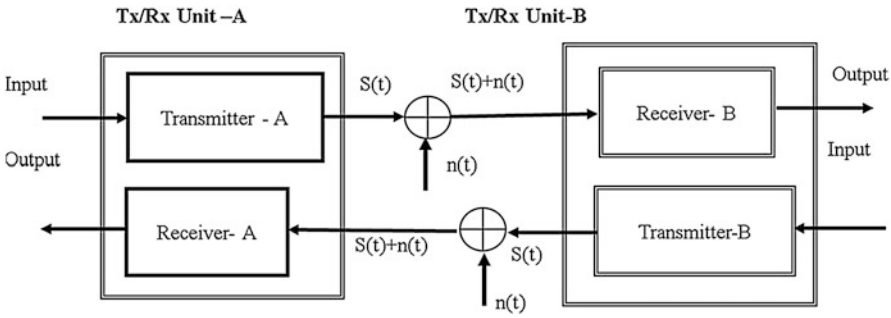


Fig. 1.1 Block diagram of a modern full-duplex communication system. The source coding stage is shown as a dotted block

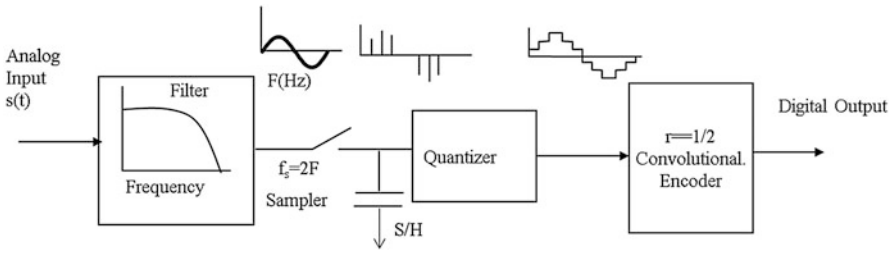


Fig. 1.2 Source coding functional block diagram

This book presents the salient concepts, underlying principles and practical applications of the contents of the source coding block listed above. In particular, this chapter will address the following topics:

- Identification and Characterization of Input Signals such as analog signal, digital signal and noise.
- Signal to Noise Ratio and its Effects in Communication Channels
- Shannon's Capacity theorem and its attributes [1]
- Measurement and Quantification of signals

1.2 Identification and Characterization of Input Signals

In modern multimedia communication systems, the input signal generally contains:

- Voice
- Data and
- Video

While voice is still the primary service, data and video are becoming increasingly popular due to the advent of cellular technology [2–4]. Since the transmission medium is limited, it is necessary to identify and quantify these signals so that we can transmit these signals reliably through the available bandwidth, which is limited.

First and foremost is the identification of the type of signals. It can be either an analog signal or a digital signal. An analog signal is a time-varying signal, which can be periodic or non-periodic. A digital signal is also a time-varying signal, which can be periodic or non-periodic as well. Sine waves and square waves are two common periodic signals.

1.2.1 Periodic Analog Signals

A Periodic analog signal is continuous with respect to time. It has one frequency component. For example a Sine wave is described by the following time domain equation:

$$V(t) = V_p \sin(\omega t) \tag{1.1}$$

Where,

- Vp = Peak voltage
- $\omega = 2\pi f$
- f = Frequency in Hz

Figure 1.3 shows the characteristics of a sine wave and its spectral response. Since the frequency is constant, its spectral response is located in the horizontal axis and the peak voltage is shown in the vertical axis. The corresponding bandwidth is zero.

It is often desired to estimate the power delivered into a load resistance as shown in Fig. 1.4. This is given by the following equation:

$$P = (V_{rms})^2/R \tag{1.2}$$

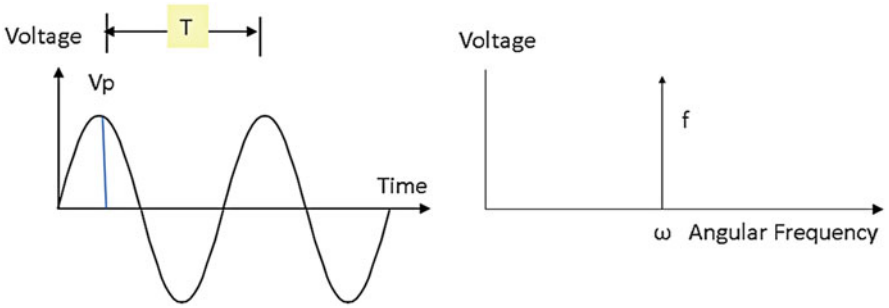


Fig. 1.3 A sine wave and its frequency response

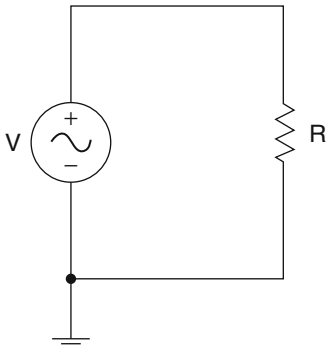


Fig. 1.4 Power delivered by a sine wave into a resistor R

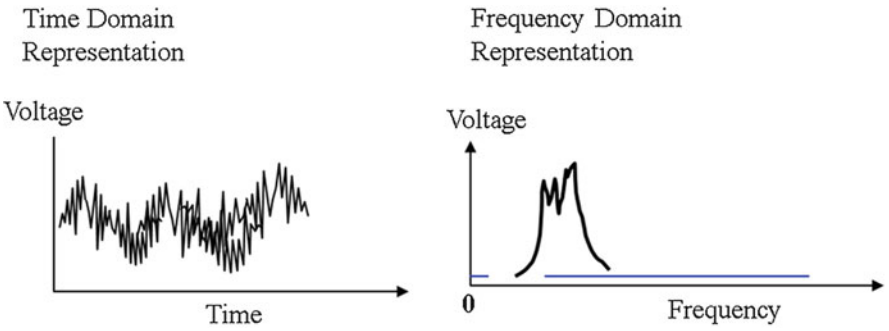


Fig. 1.5 A non-periodic analog signal and its frequency response

Where,

- P = Power delivered into R in Watts
- R = Resistance in Ohms
- $V_{rms} = V_p/\sqrt{2}$ volts
- V_p = Peak voltage volts

1.2.2 Non-periodic Analog Signals

A Non-Periodic analog signal is also continuous with respect to time. It has many frequency components. It is complex. Occupied Bandwidth (BW) is greater than zero ($BW \gg 0$). For example, human voice signal is non-periodic and its bandwidth is typically less than 1 kHz. Figure 1.5 shows an example of a non-periodic analog signal to illustrate the characteristics of a non-periodic signal.

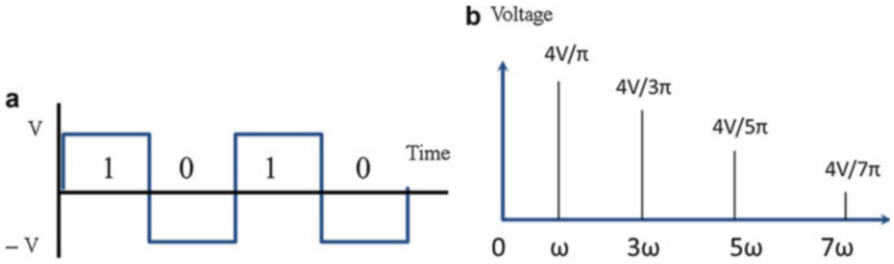


Fig. 1.6 A periodic digital signal and its spectral components

1.2.3 Periodic Digital Signals

A periodic digital signal is continuous with respect to time. It has an infinite number of harmonically related sinusoidal waveforms. For example a square wave, having a 50 % duty cycle, is represented by a waveform as shown in Fig. 1.6a and its spectral response in Fig. 1.6b. The square wave is described by the following time domain equation:

$$V(t) = V_p[\text{Sin}(\omega t)] + V_{p/3}[\text{Sin}(3\omega t)] + V_{p/5}[\text{Sin}(5\omega t)] + \ldots \quad (1.3)$$

Where,

- Vp = Peak voltage
- ω = 2πf
- f = Frequency in Hz

Figure 1.6a shows the characteristics of the square wave and its spectral response in Fig.1.6b. The spectral response is located in the horizontal axis and the peak voltage is shown in the vertical axis.

From the above, we see that a digital signal has an infinite number of harmonically related spectral components. Therefore, the occupied bandwidth is infinity. We also note that the peak voltages are also related as follows:

$$\begin{aligned} V_{p1} &= 4V/\pi \text{ at } \omega \quad (\text{Fundamental}) \\ V_{p3} &= 4V/3\pi \text{ at } 3\omega \quad (3^{\text{rd}} \text{ harmonic}) \\ V_{p5} &= 4V/5\pi \text{ at } 5\omega \quad (\text{Fifth harmonic}) \\ V_{p7} &= 4V/7\pi \text{ at } 7\omega \quad (7^{th} \text{ harmonic}) \end{aligned}$$

Furthermore, we note that the higher order spectral components are negligible. Therefore, techniques such as filtering signal formatting etc. can be used to limit the bandwidth. We shall revisit this again later in this chapter.

Next, let's examine the power delivered into a resistor R, where the source is a periodic square wave as shown in Figure 1.7. We know that a discrete time signal has an infinite number of harmonically related sinusoidal waves. Therefore, the

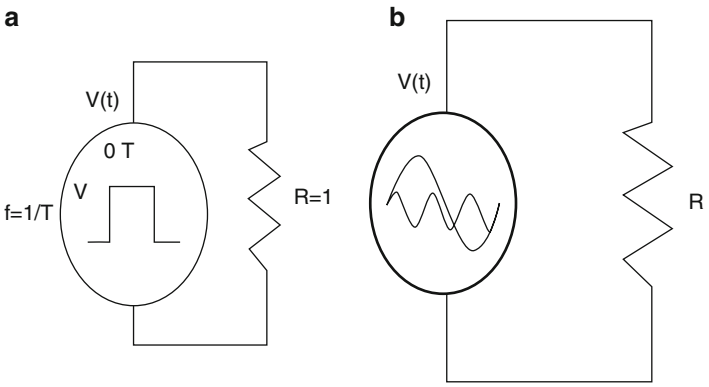


Fig. 1.7 Power delivered into a resistor. (**a**) A square wave loaded by a resistor. (**b**) The equivalent circuit having an infinite number of harmonically related sine waves

power delivered into a resistor from a periodic square wave will be due to an infinite number of harmonically related sinusoidal waves. This is conceptually shown in Fig. 1.7b.

The power delivered into the resistor R can be determined as a sum of each odd harmonic component. Thus we write,

$$P\ (\text{total}) = P_1 + P_3 + P_5 + P_7, \ldots.$$

Where,

- P_1 = Power due to the fundamental wave
- P_3 = Power due to the 3rd harmonic
- P_5 = Power due to the 5^{th} harmonic

etc.

Since the power delivered by a sinusoidal waveform into a load resistor is given by the following equation:

$$P = (V_{rms})^2/R$$

Where,

- P = Power delivered into R in Watts
- R = Resistance in Ohms
- $V_{rms} = V_p/\sqrt{2}$ volts
- V_p = Peak voltage volts

We write, for the square wave:

$$P_1 = \left(V_{p1}/\sqrt{2}\right)^2/R = \left(4V/\pi\sqrt{2}\right)^2/R \quad \text{(Fundamental)}$$
$$P_3 = \left(V_{p3}/\sqrt{2}\right)^2/R = \left(4V/3\pi\sqrt{2}\right)^2/R \quad \text{(Third harmonic)}$$
$$P_5 = \left(V_{p5}/\sqrt{2}\right)^2/R = \left(4V/5\pi\sqrt{2}\right)^2/R \quad \text{(Fifth harmonic)}$$

The total power will be,'

$$\begin{aligned} P(\text{total}) &= \left(4V/\pi\sqrt{2}\right)^2/R + = \left(4V/3\pi\sqrt{2}\right)^2/R + \left(4V/5\pi\sqrt{2}\right)^2/R + \ldots \\ &= (8/\pi)(V/R)[1 + 1/9 + 1/25 + 1/49 + \ldots.] \end{aligned}$$

Which is an infinite series, Where,

$$[1 + 1/9 + 1/25 + 1/49 + \ldots.] = \pi/8$$

Therefore, the total power is given by,

$$P(\text{total}) = V^2/R \tag{1.4}$$

Problem 1.1

This problem verifies Fourier series.
Given:

- Square wave
- V = 10 V
- T = 1 ms.

Find:

(a) The spectral components of the square wave (up to the 9^{th})
(b) Show that the sum of all the spectral components in part (a) of this problem approximates a square wave.

Solution:

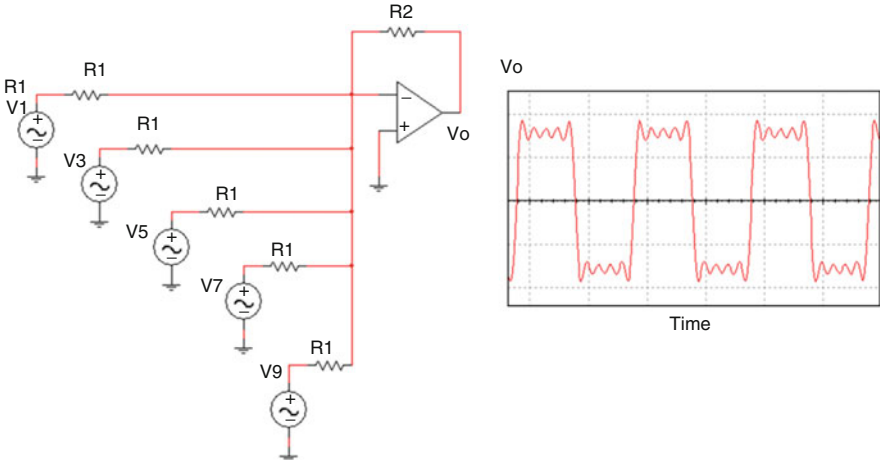
(a) For the square wave we have: V = 10 V, f =1/T = 1/1 ms = 1 kHz. Therefore, the spectral components are:

$$V_1 = 4V/\pi\, Sin\,(2\pi \times 1000t) = 12.739 Sin\,(2\pi \times 1000\text{t}) \quad \text{(Fundamental)}$$
$$V_3 = 4V/3\pi\, Sin\,(2\pi \times 3000t) = 4.246\, Sin\,(2\pi \times 3000\text{t}) \quad (3^{\text{rd}}\text{harmonic})$$
$$V_5 = 4V/5\pi\, Sin\,(2\pi \times 5000t) = 2.547 Sin\,(2\pi \times 5000\text{t}) \quad \text{(Fifth harmonic)}$$
$$V_7 = 4V/7\pi\, Sin\,(2\pi \times 7000t) = 1.819 Sin\,(2\pi \times 7000\text{t}) \quad (7^{\text{th}}\text{harmonic})$$
$$V_9 = 4V/9\pi\, Sin\,(2\pi \times 9000t) = 1.415 Sin\,(2\pi \times 9000\text{t}) \quad (9^{\text{th}}\text{harmonic})$$

(b) Use a summing amplifier to add the voltages having harmonically related wave forms. The output voltage is given by:

$$V_o = -[V_1 + V_3 + V_5 + V_7 + V_9](R_2/R_1)$$

Where R1 = R2. The negative sign indicates voltage inversion. The circuit was simulated by means of "Multisim"™. Notice that the output voltage approximates a square wave only with five harmonic components. Closer approximations can be achieved by adding more harmonic components.



1.2.4 A Non-periodic Digital Signals

In digital communications, data is generally referred to as a non-periodic digital signal as shown in Fig. 1.8. The data has two values:

- Binary-1 = High, Period = T
- Binary-0 = Low, Period = T
- Known as Non-Return to Zero (NRZ) Data

It has many frequency components, which can be determined by means of Fourier transform.

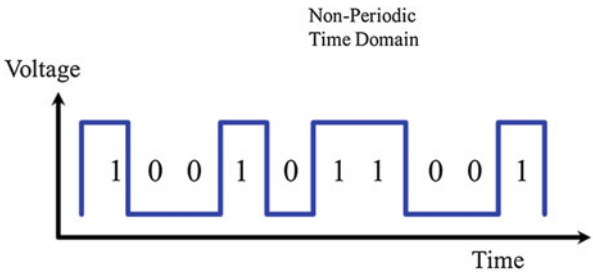


Fig. 1.8 A non-periodic digital signal

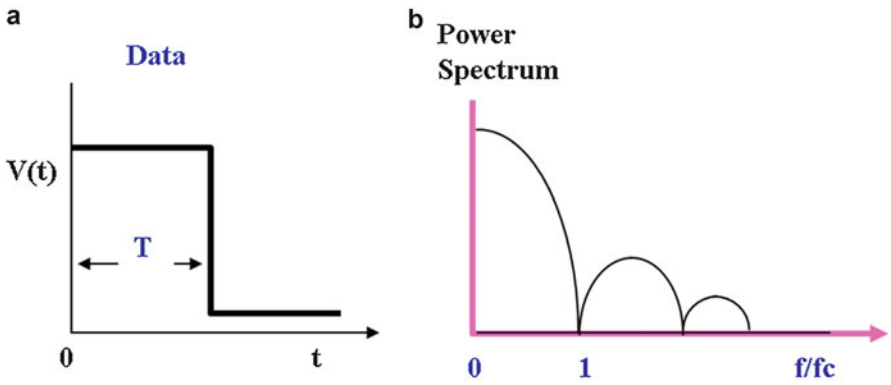


Fig. 1.9 (**a**) Discrete time digital signal and (**b**) it's one-sided power spectral density

Data can be represented in two ways:
Time domain representation (Fig. 1.9a):

$$\begin{aligned} V(t) &= V \quad < 0 < \mathrm{t} < \mathrm{T} \\ &= 0 \quad \text{elsewhere} \end{aligned} \tag{1.5}$$

Frequency domain representation is given by: "Fourier Transform":

$$V(\omega) = \int_0^T V \cdot e^{-j\omega t} dt \tag{1.6}$$

$$|V(\omega)| = VT\left[\frac{Sin\,(\omega T/2)}{\omega T/2}\right] \tag{1.7}$$

$$P(\omega) = \left(\frac{1}{T}\right)|V(\omega)|^2 = V^2 T\left[\frac{Sin\,(\omega T/2)}{\omega T/2}\right]^2 \tag{1.8}$$

This is plotted in Fig. 1.9b. The main lobe corresponds to the fundamental frequency side lobes correspond to harmonic components. The bandwidth of the power spectrum is proportional to the frequency.

The general equation for two sided response is given by:

$$V(\omega) = \int_{-\infty}^{\infty} V(t) \cdot e^{-j\omega t} dt \tag{1.9}$$

In this case, V(ω) is called two sided spectrum of V(t). This is due to both positive and negative frequencies used in the integral. The function can be a voltage or a current

1.2.5 Clock and Data

Clock is a periodic square waveform. It has a 50 % duty cycle, where T is the period of the waveform and f is the frequency. They are related by the following equation:

$$\begin{aligned} T &= \text{Period} = 1/f_c \\ f_c &= \text{frequency} \end{aligned} \tag{1.10}$$

In digital communications, the clock signal is used to:

- synchronize digital signals
- Upload and Download data
- Shift data serially
- Converts data into a parallel stream
- Converts data back to serial stream
- Etc.

Figure 1.10 shows the relationship between a clock and data. Data is the digital information. It has two values:

- Binary-1 = High, Period = T
- Binary-0 = Low, Period = T

Data has several formats [5]:

- NRZ (Non-Return to Zero)
- RZ (Return to Zero)
- AMI (Alternate Mark Inversion)
- Etc.

For NRZ data, logic-1 and Logic-0 are represented by the entire duration of the clock T. On the other hand, for Rz data, Logic 1 is represented by T/2 as shown in Fig. 1.10. Logic changes are triggered either by the rising edge or the falling edge of the clock. The bit rate is governed by the clock rate. For example, a 10 kb/s NRZ data requires a 10 kHz clock.

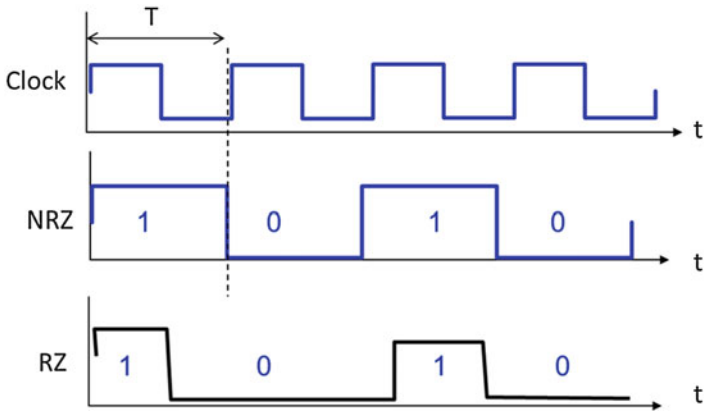


Fig. 1.10 Relationship between clock and data

Problem 1.2

Given:

- Clock Period T = 1 ms.
- NRZ Data

(a) Derive an expression for the power spectral density using the Fourier Transform
(b) Find the bit Rate R_b
(c) Calculate the two sided Bandwidth

Solution:

(a) Time domain representation of the NRZ data is given by:

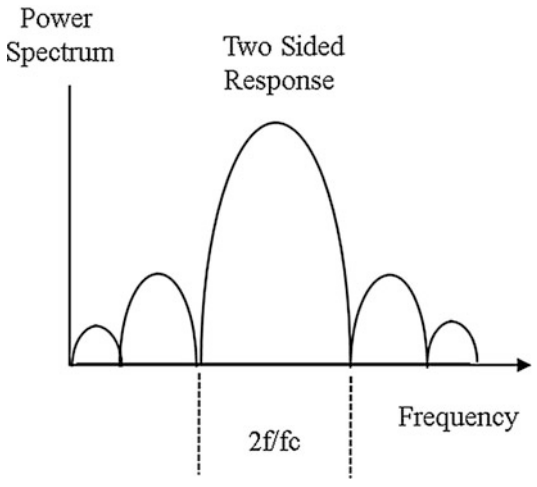
$$\begin{aligned} V(t) &= V \quad < 0 < \mathrm{t} < \mathrm{T} \\ &= 0 \quad \text{elsewhere} \end{aligned}$$

Frequency domain representation (One sided) is given by:

$$\begin{aligned} V(\omega) &= \int_0^T V \cdot e^{-j\omega t} dt \\ |V(\omega)| &= VT\left[\frac{Sin\,(\omega T/2)}{\omega T/2}\right] \\ P(\omega) &= \left(\frac{1}{T}\right)|V(\omega)|^2 = V^2 T\left[\frac{Sin\,(\omega T/2)}{\omega T/2}\right]^2 \end{aligned} \tag{1.11}$$

(b) Bit Rate $R_b = 1/T = 1/1$ ms = 1 kb/s
(c) Bandwidth (BW) = 2Rb = 2 × 1 kb/s = 2 kHz.

Note: This is the two sided bandwidth, i.e. first null to first null. As illustrated below:



1.3 Noise

1.3.1 Background

When we transmit a signal via a medium, it gets corrupted due to noise, which is an undesired random signal in communication systems [6–8]. Figure 1.11 shows a typical communication system and the source of noise. The effect of noise is measured as:

- Signal to Noise Ratio (S/N)
- Carrier to Interference Ratio (C/I)
- Carrier to Interference and Noise Ratio [S/(N + I)]
- Signal to Noise and Distortion Ratio (SINAD)
- Energy per Bit to Noise Spectral Density (EB/No), causing Bit Error Rate (BER) in digital communication system.

Figure 1.12 shows the characteristics of noise and its bandwidth occupancy, which is nearly flat across the channel. In order to recover the true signal from a

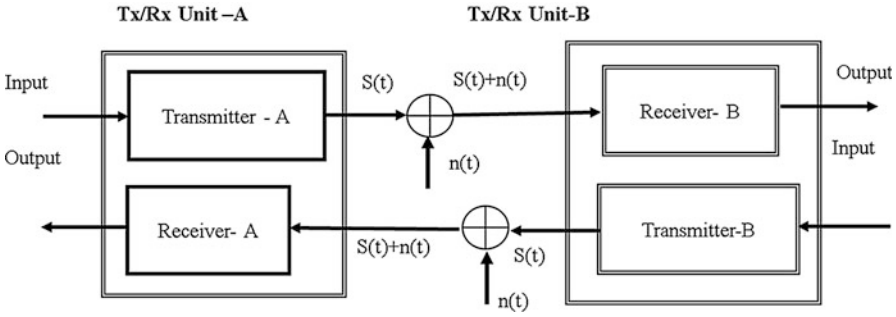


Fig. 1.11 Channel model and source of noise

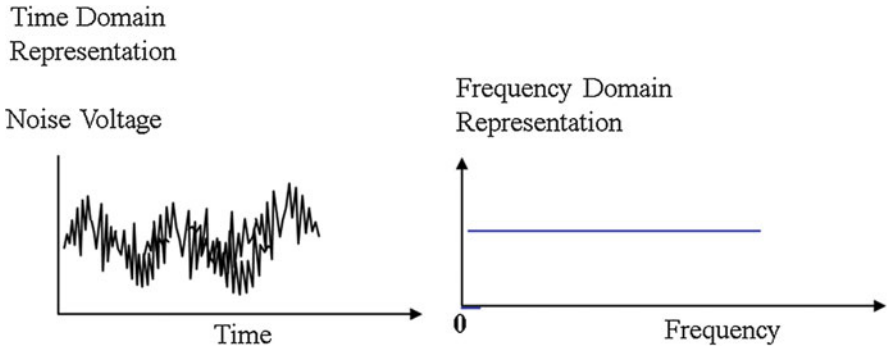


Fig. 1.12 The characteristics of noise and its bandwidth occupancy

noisy environment, we need to understand the source of noise and its characteristics.

The source of noise can be:

- Natural: Thermal noise and Shot noise.
- Unintentional: Co-Channel and Adjacent channel Interference (CCI and ACI) from cellular communication
- Intentional: Jamming from an adversary

A brief description of some of these noise parameters are described below:

1.3.2 Thermal Noise

Thermal noise is generated by the random motion of charge carriers inside an electrical conductor. The power spectral density is flat throughout the frequency spectrum. See Fig. 1.12. For this reason, it is also known as "white". The amplitude of thermal noise also exhibits a Gaussian probability density function. As a result, a communication channel affected by thermal noise is often modeled as an Additive White Gaussian noise (AWGN).

The root mean square (RMS) voltage due to thermal noise, generated in a resistance R, is given by:

$$v_n = \sqrt{4kTB} \tag{1.12}$$

Where

- k= Boltzmann's constant (joules per kelvin) and
- T = Absolute temperature (kelvin).
- B = Noise bandwidth

1.3.3 Shot Noise

Shot noise in electronic devices is due to random fluctuations of charges. The flow of these charges is relatively continuous but they arrive at random, causing a fluctuation in current flow. The root-mean-square value of the shot noise current i_n is given by the Schottky formula

$$i_n = \sqrt{2iqB} \tag{1.13}$$

Where

- i = Current
- q = Electron charge
- B = Bandwidth in hertz.

1.4 Interference

1.4.1 Co-Channel Interference

In cellular communications, frequencies are reused in different cells, which mean that another mobile can use the same frequency from a distant location. This is known as "Frequency Reuse" [2, 4], Frequency reuse enhances channel capacity. This is accomplished at the expense of unintentional interference, which is also known as "Co-channel Interference or Carrier to Interference (C/I)].

As an illustration, we consider Fig. 1.13, where the same frequency is used in Cell-A and Cell-B. Therefore, a mobile communicating with Cell-A will also receive the same frequency from the distant Cell-B. This is analogous to the "Near-Far" problem, causing co-channel interference. We use the following method to determine this interference.

Let,

RSL_A = Received signal level at the mobile from Cell -A

d_A = Distance between the mobile and Cell-A

RSL_B = The received signal level at the mobile from Cell -B

d_B = Distance between the mobile and Cell-B

γ = Path loss exponent

Then we can write,

$$\begin{aligned} RSL_A &\propto (d_A)^{-\gamma} \\ RSL_B &\propto (d_B)^{-\gamma} \end{aligned} \tag{1.14}$$

Where,

- RSL = Received signal level
- d = Distance between the transmitter and the receiver
- γ = Received signal decay constant

The ratio of the signal strengths at the mobile will be:

$$\frac{RSL_A}{RSL_B} = \left(\frac{d_A}{d_B}\right)^{-\gamma} = \left(\frac{d_B}{d_A}\right)^{\gamma} \tag{1.15}$$

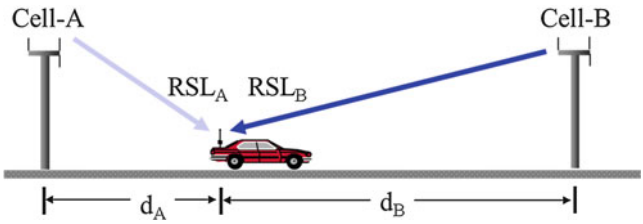


Fig. 1.13 Carrier to Interference ratio (C/I) due to a single interferer

In the above equation, RSL_A is the RF signal received from the serving cell. Therefore, this is the desired signal and we redefine this signal as the carrier signal power C. We also assume that the mobile is at the cell edge from the serving cell-A, which is the cell radius R ($d_A = R$). On the other hand, RSL_B is the undesired signal received from $Cell_B$ and we redefine this signal as the interference signal power I. The corresponding interference distance $d_B = D$; D being the reuse distance. Therefore, above equation can be written as a carrier to interference ratio (C/I), due to a single interferer, as:

$$\frac{C}{I} = \left(\frac{D}{R}\right)^{\gamma} \tag{1.16}$$

In decibel, it can be written as:

$$\frac{C}{I}(dB) = 10Log\left(\frac{D}{R}\right)^{\gamma} \tag{1.17}$$

Where,

- C = Signal power from the serving carrier
- I = Signal power from the interferer
- γ = Received signal decay constant
- R = Cell radius
- D = Reuse distance

1.4.2 C/I Due to Multiple Interferers

In hexagonal cellular geometry, each hexagonal cell is surrounded by six hexagons as shown in Fig. 1.14. Therefore, in a mature cellular system, there can be six primary interferers. The total interference from all six interferers will be [2, 4]:

$$\begin{aligned} &6RSL_B \propto (d_B)^{-\gamma} \\ &\text{or} \\ &RSL_B \propto \frac{1}{6}(d_B)^{-\gamma} \end{aligned} \tag{1.18}$$

Therefore, the effective interference ratio is:

$$\frac{C}{I} = \frac{RSL_A}{RSL_B} = \frac{1}{6}\left(\frac{d_A}{d_B}\right)^{-\gamma} = \frac{1}{6}\left(\frac{d_B}{d_A}\right)^{\gamma} = \frac{1}{6}\left(\frac{D}{R}\right)^{\gamma}$$

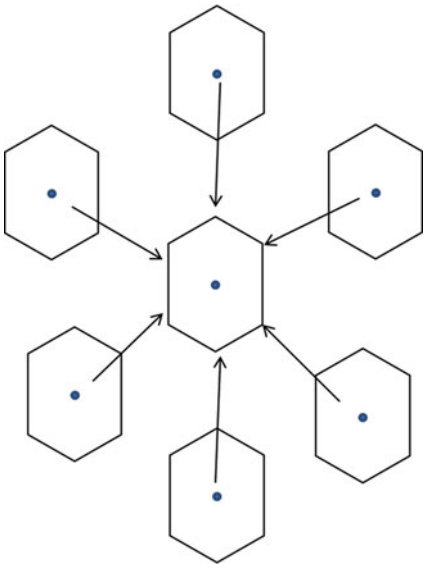


Fig. 1.14 C/I due to multiple interferers. Group of frequencies used in the center cell are reused in the surrounding six cells

And in decibel,

$$\frac{C}{I}(dB) = 10Log\left[\frac{1}{6}\left(\frac{D}{R}\right)^{\gamma}\right] \tag{1.19}$$

Therefore, by knowing the reuse distance, the C/I ratio can be determined. Or, by knowing the C/I requirement, the reuse distance can be determined in a given propagation environment. The reuse distance D can be determined from plane geometry and the cell radius can be obtained from the propagation model.

Typical path loss slopes are:

- $\gamma = 2$ (Free Space)
- $\gamma = 2.5$ (Rural environment)
- $\gamma = 3$ (Sub-urban environment)
- $\gamma = 3.5$ (Typical urban environment)
- $\gamma = 4$ (Dense urban environment)

Problem 1.3

Given:

- Pathloss slope $\gamma = 4$ (Dense urban environment-typical)
- 6 Co-Channel Interferers
- D/R = 4.6

Find: The carrier to interference ratio C/I.

Solution:

$$\frac{C}{I}(dB) = 10Log\left[\frac{1}{6}\left(\frac{D}{R}\right)^{\gamma}\right]$$

With $\gamma = 4$ and D/R = 4.6, we obtain:
C/I $\underline{\sim}$ 18 dB.

1.4.3 The Effect of Noise in Communication Channels and Shannon's Capacity Theorem

The effect of noise on communication channel was best described by Claude Shannon [1]. Shannon's capacity theorem states that, when transmitting a signal in the presence of noise, we need to ensure that the signal power is greater than the noise power, so that the signal can be recovered without an error. Shannon showed that, in a noisy environment, the maximum bit rate that can be achieved is given by the following formula:

$$C = WLog_2\left(1 + \frac{S}{N}\right)\text{bits/s.} \tag{1.20}$$

Where,

- C = Channel capacity (bits/s)
- W = Bandwidth in Hz
- S/N = Signal to Noise Ratio

Since the noise power is proportional to the bandwidth, we write:

- $N = N_o W$
- N_o = Noise spectral density at room temperature

Therefore, we can write,

$$C = WLog_2\left(1 + \frac{S}{N}\right)\text{bits/s.}$$
$$C = WLog_2\left(1 + \frac{S}{N_0 W}\right)\text{bits/s.}$$

Since C = Bit rate, we define C = R (b/s) and express the capacity theorem as follows:

$$C = WLog_2\left(1 + \frac{S}{N_0 W}\right)\text{bits/s.}$$
$$\text{OR} \tag{1.21}$$
$$\frac{R}{W} = Log_2\left(1 + \frac{S}{N_0 W}\right)\text{bits/s per channel}$$

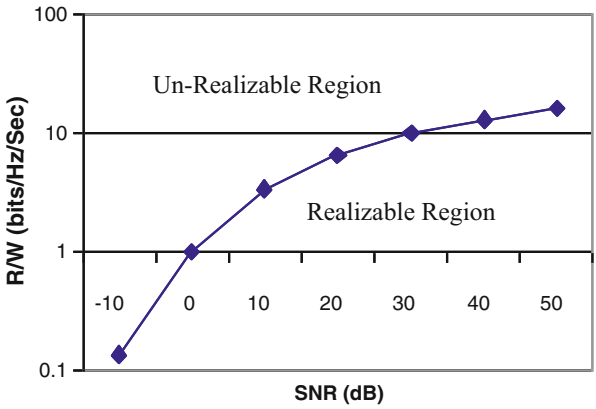


Fig. 1.15 Channel capacity as a function of S/N

The Ratio R/W is Known As "Channel Capacity, which is a function of S/N. This is plotted in Fig. 1.15.

We Observe the Following:

- To increase the capacity we need more S/N ratio
- More S/N ratio can be achieved by:
  - Increasing the signal power
  - Reducing the noise
  - Defeating the noise by means of "Error Control Coding"
- However, there is a diminishing return, requiring a compromise between several parameters, e.g., Available bandwidth, Forward Error Control Coding, Modulation etc. These topics will be discussed in this series of books.

1.5 Measurement and Quantification of Signals

Measurement of Information is a discipline that quantifies information. We need this because the transmission medium is limited. Information can be quantified by means of:

- Decimal System (Analog Info.)
- Binary System (Digital Info.)

Both systems are equally good and widely used to quantify information for further processing.

1.5.1 Decimal System

In decimal system, the information is quantified as:

$$N = 10^m \quad \text{Where}, \quad m = 1,\ 2,\ 3,\ \ldots. \tag{1.22}$$

As a result, the value of N increases rapidly as a power of 10. This is given by:

$$\begin{aligned} N &= 10^0,\ 10^1,\ 10^2,\ 10^3,\ 10^4,\ 10^5,\ \ldots \\ &= 1,\ 10,\ 100,\ 1000,\ 10000,\ 100000,\ \ldots. \end{aligned}$$

Since the number N increases rapidly, it is inconvenient. As such we use Logarithmic Scale with a base of 10:

$$\begin{aligned} M &= Log_{10}(N) \\ &= 0,\ 1,\ 2,\ 3,\ \ldots \end{aligned} \tag{1.23}$$

Where N==1, 10, 100, 1000, ...
This number (M) is Small and convenient to use.

1.5.2 Binary System

In Binary system, the information is quantified as:

$$N = 2^m \tag{1.24}$$

Where $m = 1, 2, 3, \ldots$.
As a result, the value of N increases rapidly:,

$$\begin{aligned} N &= 2^0,\ 2^1,\ 2^2,\ 2^3,\ 2^4,\ 2^5,\ \ldots \\ &= 1,\ 2,\ 3,\ 4,\ 8,\ 16,\ 32,\ \ldots \end{aligned} \tag{1.25}$$

Since the number N also increases rapidly, it is inconvenient. As such we use Logarithmic Scale with a base of 2:

$$\begin{aligned} M &= Log_2(N) \\ &= 0, 0.301,\ 0.602,\ 0.903,\ \ldots \end{aligned} \tag{1.26}$$

Where, $N = 1, 2, 4, 8, \ldots$
This number (M) is also Small and convenient to use.
The relationship between binary and decimal systems is given by:

$$Log_2(N) = \frac{Log_{10}(N)}{Log_{10}(2)} = 3.32\ \mathrm{Log}_{10}(N)$$

Problem 1.4:

Given:

- 26 Letters in English Language: A, B, . . . Z
- Each Letter is Equally Likely

Find: The Average Number of Bits Needed to Transmit a Single Letter

Solution:

$$m = [Log_{10}(26)]/[Log_{10}(2)] = 4.7 \simeq 5$$

Therefore, we need 5 bits per letter.

1.6 Conclusions

- Source Coding defined
- Reviewed Signals and spectra
- Discussed Signal to Noise Ratio and Effects of Noise on Communication Circuits
- Shannon's Capacity Theorem indicates that there is a diminishing return
- In light of Shannon's capacity theorem, it may be concluded that communication systems engineering is partly science, partly engineering and mostly art. It has to adapt to changing technology such as channel coding, modulation, Frequency reuse and C/I management etc.

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Chapter 2
Baseband Filters: Active RC Filters

Topics

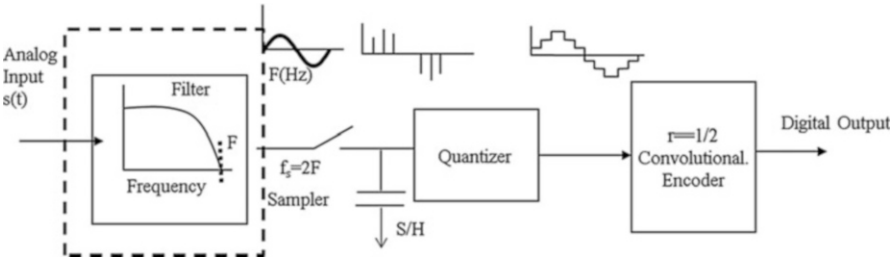
- Introduction
- Voltage and Current Sources
- Voltage to Current Transducers
- Amplifiers and Integrators
- Simulation of Inductors
- Active Filter Design based on simulated inductors
- Higher Order Active Filters Based on Simulated Inductors

2.1 Introduction

In telecommunications, voice transmission is a primary service (e.g., digital telephones, cellular communications). Since human voice occupies a spectrum from 300 Hz to 3.4 kHz, a baseband filter is used to pass this frequency band and reject all others. To realize these filters, the traditional networks used inductors, capacitors and resistors to perform analog functions [1, 2]. In this frequency region, the inductors are heavy and expensive. Efforts have been made to replace them by networks consisting of active elements, capacitors and resistors [3, 4]. This development was very successful and active RC networks are now widely used by industry.

In an attempt to contribute in opening the way for scholarly research in the area of analog low frequency simulation on a chip, this text develops first the idea of transconductance models of network building blocks known from the analog world: amplifiers with prescribed gain integrators and inductors. All these networks are derived from their continuous time counterparts [5, 6]. It is assumed that the student is familiar with the basic concept of circuit theory.

S. Faruque, *Radio Frequency Source Coding Made Easy*, SpringerBriefs
in Electrical and Computer Engineering, DOI 10.1007/978-3-319-15609-5_2



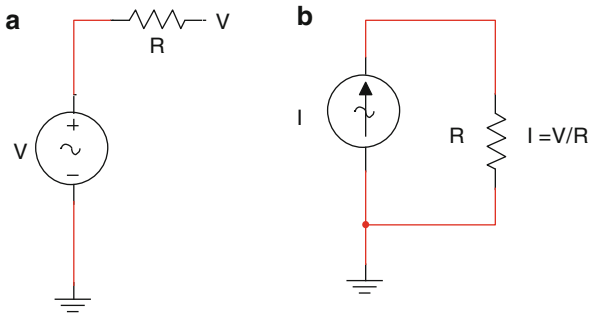


Fig. 2.1 (**a**) A voltage source, (**b**) A current source

2.2 Voltage to Current Source

The most commonly used voltage source is given in Fig. 2.1a where R_s is the source resistance. The voltage V is ideal which means that it is independent of loading. The equivalent current source is given in Fig. 2.1b in which

$$I = V/R \tag{2.1}$$

where the generated current I is also ideal.

2.3 Voltage to Current Transducer (Transconductance)

A Transconductance is a two-port network whose output current is proportional to the input voltage. The symbolic representation is given in Fig. 2.2 in which g_m is the transconductance.

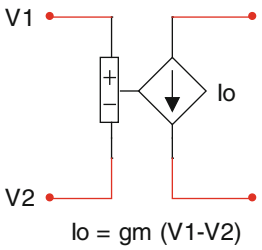


Fig. 2.2 Symbolic representation of a transconductance

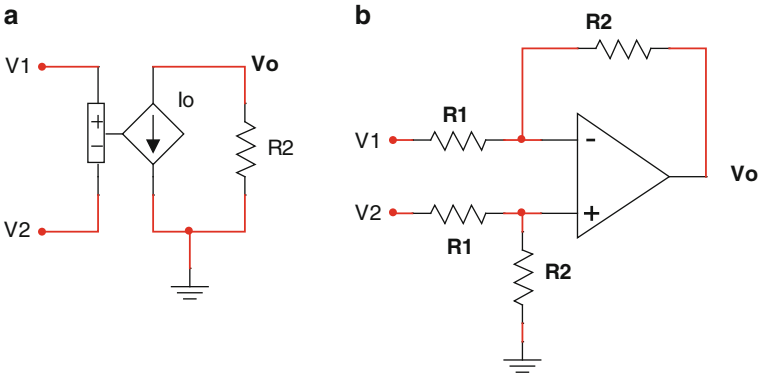


Fig. 2.3 (**a**) A differential transconductance amplifier and (**b**) its active realization by means of operational amplifier

The input–output relation is expressed as

$$I_0 = g_m(v_1 - V_2) \tag{2.2}$$

The element is also known as "Voltage to Current Transducer" (VCT).

2.4 Amplifiers

2.4.1 Differential Amplifier

A Transconductance, when loaded by a resistance, becomes an amplifier. Thus consider the Transconductance circuit as shown in Fig. 2.3a where R_2 is the load resistance. The current Equation of this circuit can be written as

$$I_o = g_m(V_1 - V_2) = -V_0/R_2 \tag{2.3}$$

The differential voltage gain is therefore

$$A_V = V_0/(V_1 - V_2) \ = -g_m R_2 \tag{2.4}$$

The polarity of the output voltage can be reversed simply by reversing the input voltages:

$$A_V = V_0/(V2 - V1) = g_m R_2 \tag{2.5}$$

Now consider the OpAmp realization of the differential amplifier as shown in Fig. 2.3b. The Voltage gain of this amplifier is given by,

$$A_v = V_o/(V_1 - V_2) = -R_2/R_1 \tag{2.6}$$

Comparing this with the transconductance model, we have,

$$g_m = 1/R_1 \tag{2.7}$$

2.4.2 *Inverting Amplifier*

Figure 2.4 shows an inverting transconductance amplifier and its active realization by means of operational amplifier. From the transconductance amplifier, we obtain,

$$I_o = g_m V_{in} = -V_0/R_2 \tag{2.8}$$

The voltage gain is therefore

$$A_V = V_0/V_{in|} = -g_m R_2 \tag{2.9}$$

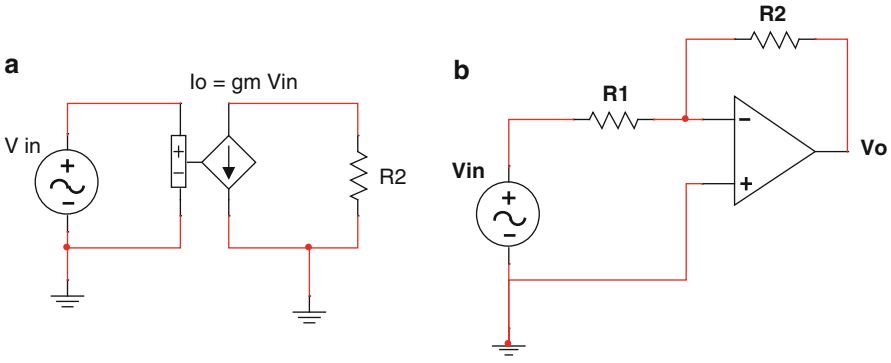


Fig. 2.4 (**a**) An inverting transconductance amplifier and (**b**) its active realization by means of operational amplifier. Operational amplifier

Now consider the OpAmp realization of the inverting amplifier as shown in Fig. 2.4b. The voltage gain of this amplifier is given by,

$$A_v = V_o/V_{in} = -R_2/R_1 \tag{2.10}$$

Comparing this with the transconductance model, we have,

$$g_m = 1/R_1 \tag{2.11}$$

2.4.3 *Non-inverting Amplifier*

A non-inverting amplifier can be realized as shown in Fig. 2.5. From the transconductance model, the voltage gain of this amplifier is,

$$Av = g_m R_2$$

where $gm = 1/R_2$.

From the OpAmp realization of the non-inverting amplifier as shown in Fig. 2.5b, the Voltage gain becomes,

$$A_v = V_o/V_{in} = R_2/R_1 \tag{2.12}$$

Comparing this with the transconductance model, we have,

$$g_m = 1/R_1 \tag{2.13}$$

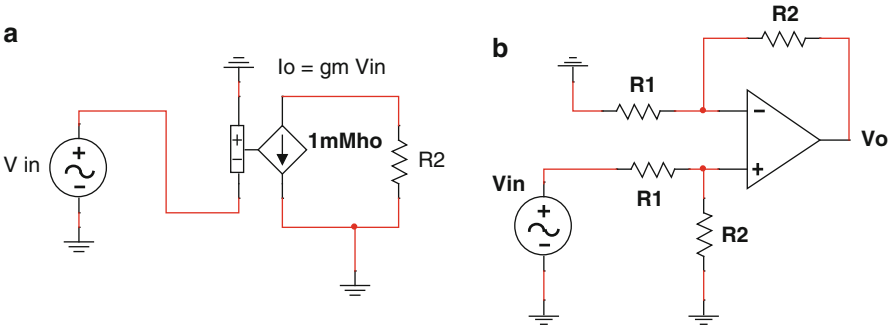


Fig. 2.5 (**a**) A non-inverting transconductance amplifier and (**b**) its active realization by means of operational amplifier

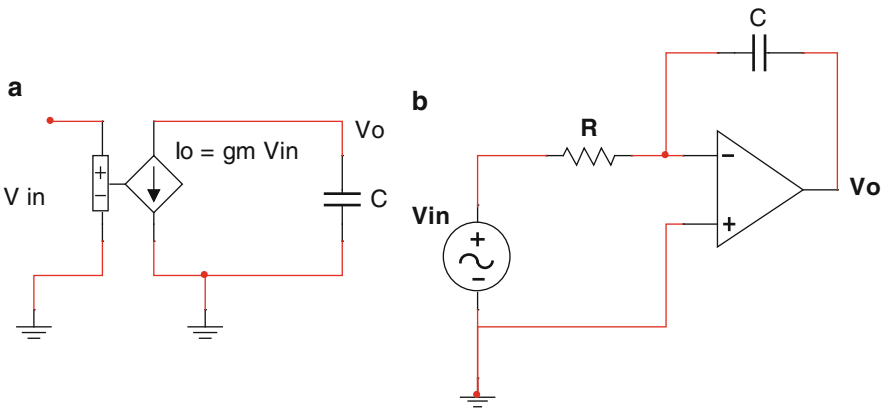


Fig. 2.6 (**a**) An inverting transconductance integrator and (**b**) its active realization by means of OpAmp

2.5 Integrators Based on Transconductances

A Transconductance, when loaded by a capacitor, becomes an integrator. Figure 2.6 shows an Inverting transconductance integrator and its active realization by means of an Operational Amplifier. The corresponding transfer Functions are:

$$T(s) = V_0/V_{in} = -g_m/sC \tag{2.14}$$

$$T(s) = V_0/V_{in} = -1/(sCR) \tag{2.15}$$

where gm = 1/R.

Next, consider a non-inverting transconductance integrator and its active realization by means of Operational amplifier as shown in Fig. 2.7. The voltage Transfer functions of these integrators are respectively,

$$T(s) = g_m/sC \tag{2.16}$$

$$T(s) = 1/(sCR) \tag{2.17}$$

where gm = 1/R.

2.6 Differential Integrators

A differential integrator, based on transconductance, is given in Fig. 2.8a. The output voltage transfer function is given by

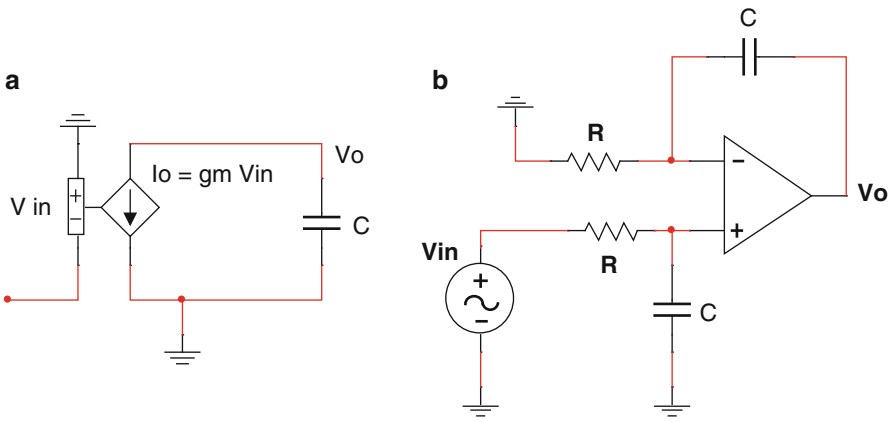


Fig. 2.7 (**a**) A non-inverting transconductance integrator and (**b**) its active realization by means of OpAmp

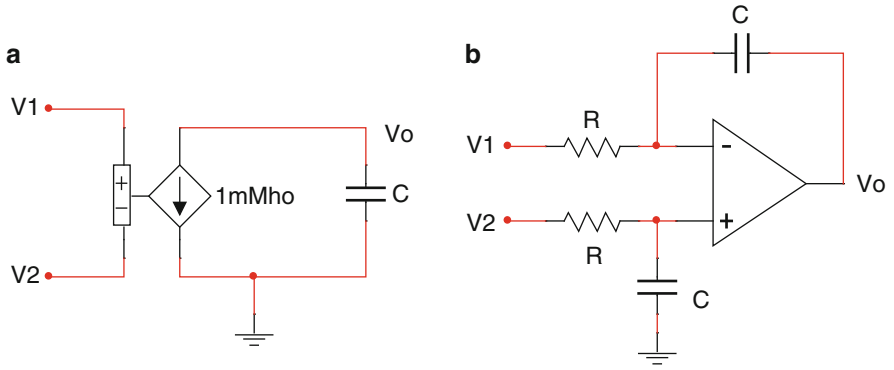


Fig. 2.8 (**a**) A differential transconductance integrator and (**b**) its active realization by means of OpAmp

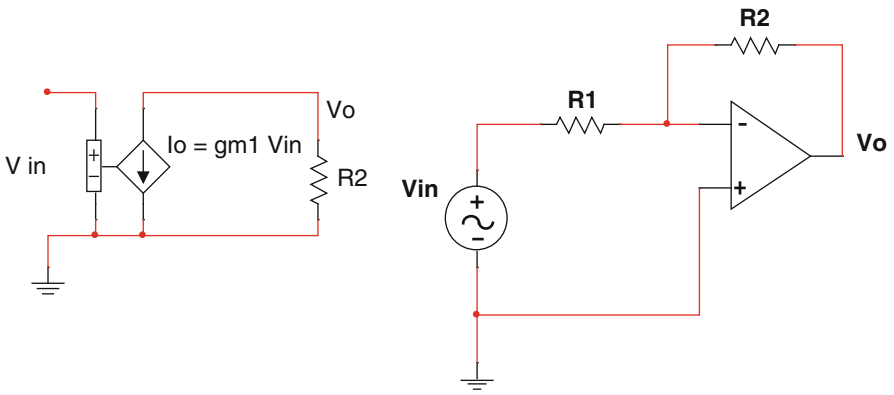
$$T(s) = V_0(s)/(V_1 - V_2) = -g_m/sC \tag{2.18}$$

The equivalent active realization, based on OpAmp, is in Fig. 2.8b. Its transfer function is given by

$$T(s) = V_0(s)/(V_1 - V_2) = -1/sCR \tag{2.19}$$

where $g_m = 1/R$.

Problem 2.1
Consider the transconductance amplifier and its OpAmp realization as Shown below:



(a) Design the transconductance amplifier to deliver a voltage gain of 20 dB.
(b) Design the OpAmp amplifier to deliver a voltage gain of 20 dB.

Solution to Problem 2.1:

(a) The voltage gain is given by

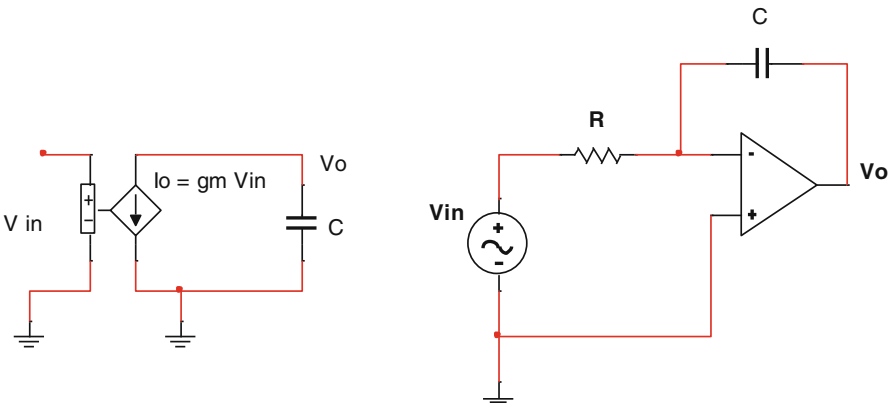
$$A_v = -g_{m1}R_2$$

For $Av(dB) = 20\,dB$, $Av(v/v) = 10^{20/20} = 10\,v/v$
$|Av| = |g_{m1}R_2| = 10$. Let $R_2 = 10k$. Then, $g_{m1} = 1$ mMho.

(b) For the OpAmp amplifier, the voltage gain is given by,
$A_v = -V_o/V_{in} = -R_2/R_1 = -10$. Therefore, the voltage gain in dB is given by:

$$|Av(dB)| = 20\,Log(10) = 20\,dB.$$

Problem 2.2
Consider the transconductance integrator and its OpAmp realization as shown below:



(a) Design the transconductance integrator to deliver a time constant of 1 ms.
(b) Design the OpAmp integrator to deliver a time constant of 1 ms.

Solution 2.2:
From the transconductance circuit we obtain the nodal equation

$$g_m V_{in} = -V_0 sC \text{ where } s = j\omega,\ \omega = 2\pi f,\ f = \text{Frequency}$$

The voltage transfer function is given by,

$$T(s) = V_o/V_{in} = -g_m/sC$$

From the OpAmp integrator, we have,

$$T(s) = V_o/V_{in} = -1/sCR$$

Therefore, For $R = 1/g_m$, both the integrators are functionally identical.
The 1 ms time constant, can be realized as:

$$\tau = RC = C/g_m = 1\,\text{ms}\ \left(R = 10^3\,\text{Ohm}, C = 10^{-6}\,\text{F}, g_m = 10^{-3}\,\text{Mho}\right)$$

2.7 Simulation of Grounded Inductor

The transconductance models of integrators, developed in the previous chapter, will now be used to simulate various building blocks such as grounded inductors, floating inductors, LC sections etc. Various second order and more complex filter functions can be realized by using these building blocks.

A grounded inductor can be realized by means of two transconductances, as shown in Fig. 2.9.

From Fig. 2.9 we derive,

$$I_1 = g_{m1} V_2 \tag{2.20}$$

$$I_2 = g_{m2} V_1 = V_2 sC_2 \tag{2.21}$$

From (2.21) V_2 we get

$$V_2 = g_{m2} V_1/sC_2 \tag{2.22}$$

Substituting (2.22) into (2.20), for V_2, I_1 can be written as

$$I_1 = g_{m1} g_{m2} V_1/sC_2 \tag{2.23}$$

Solving for the input impedance $Zin = V_1/i1$ we obtain

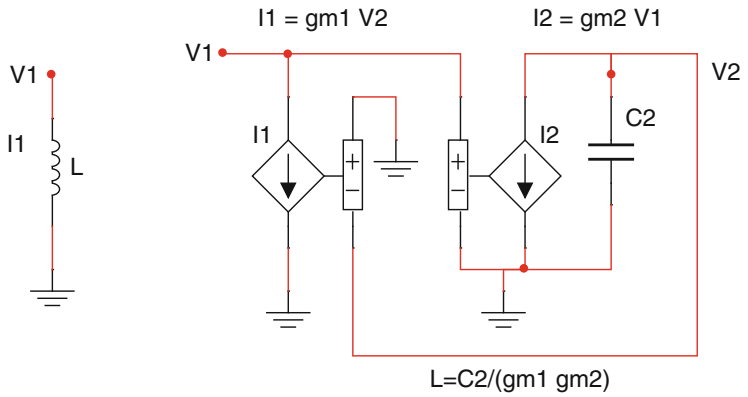


Fig. 2.9 A grounded inductor and its transconductance model

$$Z_{in} = V_1/I_1 = sC_2/g_{m1}g_{m2} \tag{2.24}$$

Thus the element simulates a grounded inductor of value

$$L = C_2/g_{m1}g_{m2} \tag{2.25}$$

2.8 Simulation of Floating Inductor

A floating inductor can be represented by a two-port network comprising transconductances as shown in Fig. 2.10.

The impedance of a floating inductor is given by,

$$Z_L = \backslash sL = (V_1 - V_3)/I \tag{2.26}$$

where,

- $s = j\omega$, $\omega = 2\pi f$, f = frequency
- V1 − V3 is the voltage across the inductor, and
- I is the current through the inductor

From the transconductance model of the floating inductor we have,

$$I_1 = g_{m1}V_2 \tag{2.27}$$

$$I_2 = g_{m2}(V_1 - V_3) = sC_2V_2 \tag{2.28}$$

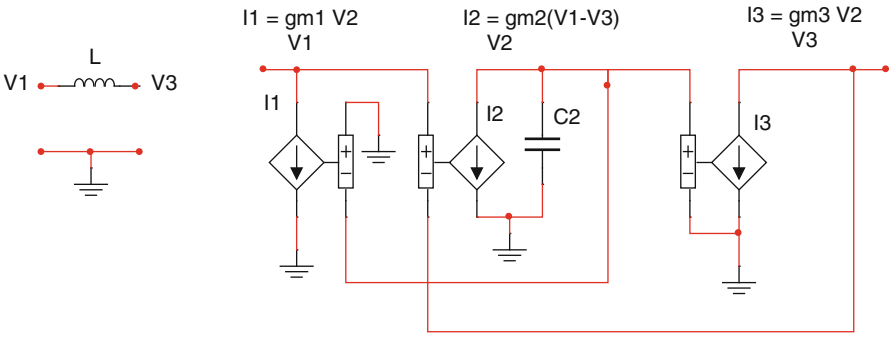


Fig. 2.10 A floating inductor and its transconductance model

$$I_3 = g_{m3} V_2 \tag{2.29}$$

From (2.28) we get,

$$V_2 = g_{m2}(V_1 - V_3)/sC_2 \tag{2.30}$$

Substituting (2.30) for V_2 in (2.27) and (2.29), we get,

$$I_1 = g_{m1} g_{m2}(V_1 - V_3)/sC_2 \quad \text{and} \tag{2.31}$$

$$I_3 = g_{m3} g_{m2}(V1 - V_3)/sC_2 \tag{2.32}$$

The condition for an equivalent inductor is

$$g_{m1} = g_{m3} \tag{2.33}$$

Therefore,

$$\begin{aligned} I &= g_{m1} g_{m2}(V_1 - V_3)/sC_2 \\ Z_L &= (V_1 - V_3)/I = sC_2/g_{m1} g_{m2} \end{aligned} \tag{2.34}$$

The value of the inductor is then

$$L = C_2/g_{m1} g_{m2} \tag{2.35}$$

where $g_{m1} = g_{m3}$.

2.9 Second Order Filters: *The Biquad*

A biquad (bi-quadratic) filter is a second order filter which can provide various second order transfer functions. A biquad transfer function is the one whose numerator and denominator polynomials are quadratic in nature. This section will briefly review some of the most useful second order transfer functions derived from the general biquad transfer function as given below:

$$T(s) = \frac{s^2 + \left(\frac{\omega z}{Qz}\right)s + \omega z}{s^2 + \left(\frac{\omega p}{Qp}\right)s + \omega p} \tag{2.36}$$

where,

$s = j\omega$ Laplace transform variable
ω_z = zeroes of the transfer function
ω_p = poles of the transfer function
Q_z = quality factor of the zeroes
Q_p = quality factor of the poles

Zeros are described by the numerator polynomial and Poles are described by the denominator polynomial. Most frequently used transfer functions are described in the following:

2.9.1 Lowpass Filter

A Lowpass filter is described by the following transfer function:

$$T(s) = \frac{\omega z}{s^2 + \left(\frac{\omega p}{Q p}\right)s + \omega p} \tag{2.37}$$

The frequency response is shown in Fig. 2.11. The pole frequency ω_p is measured when the voltage transfer function |T(s) is 70 % of its maximum value.

2.9.2 High Pass Filter

A high pass filter is described by its transfer function as shown below:

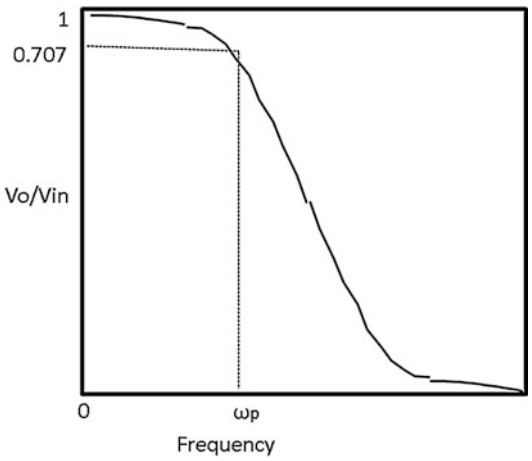


Fig. 2.11 A lowpass response. ω_p is the pole frequency

$$T(s) = \frac{s^2 k}{s^2 + \left(\frac{\omega p}{Q p}\right)s + \omega p} \tag{2.38}$$

which has a frequency response as shown in Fig. 2.12, where ω_p is the pole frequency.

2.9.3 Bandpass Filter

A band pass filter is described by its transfer function

$$T(s) = \frac{\left(\frac{\omega z}{Q z}\right)s}{s^2 + \left(\frac{\omega p}{Q p}\right)s + \omega p} \tag{2.39}$$

It has a frequency response as shown in Fig. 2.13, where ω_p is the pole frequency.

2.9.4 Band Reject Filters

A band reject function is described by

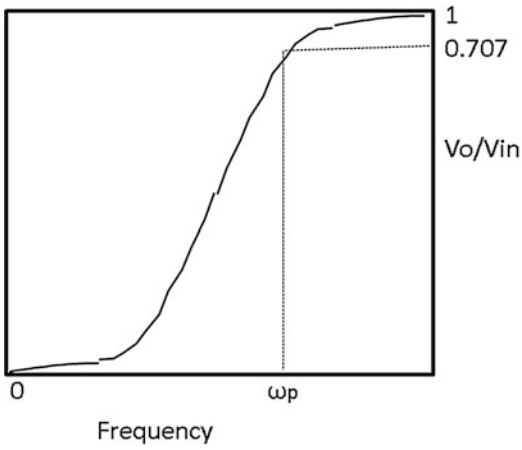


Fig. 2.12 A highpass response. ω_p is the pole frequency

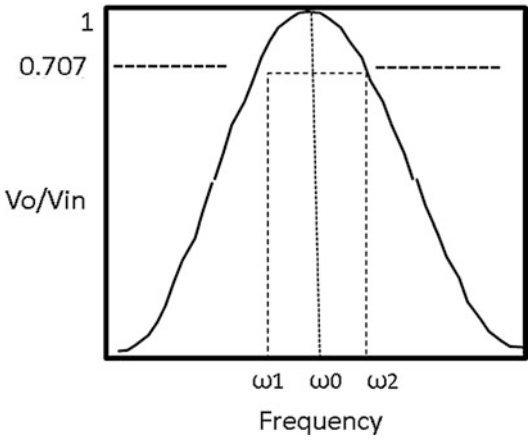


Fig. 2.13 Bandpass response

$$T(s) = \frac{s^2 + \omega z2}{s^2 + \left(\frac{\omega p}{Q p}\right)s + \omega p} \tag{2.40}$$

The frequency response of this function is shown in Fig. 2.14.

Problem 2.3
Show that the bandwidth of signal is determined by the signal attenuation by a factor of 0.707 (−3 dB) from its maximum value.

Solution:
In order to examine this, we consider a simple RC circuit as shown below:

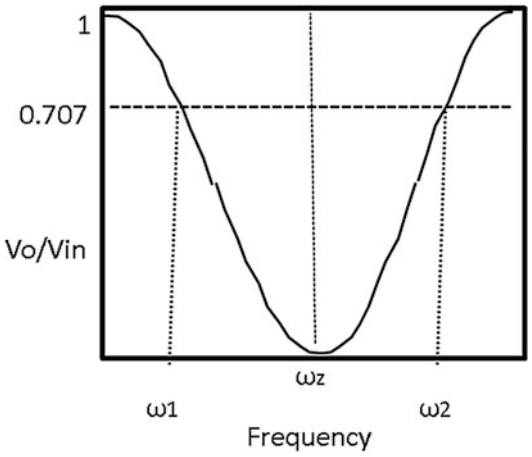
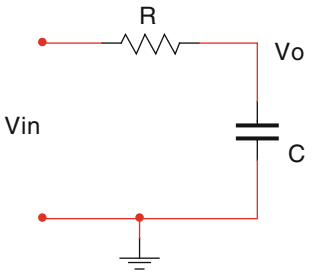


Fig. 2.14 Band reject response



The voltage transfer function is given by,

$$T(s) = V_o/V_{in} = 1/(1 + j\omega RC) = 1/\left(1 + j\omega/\omega_p\right)$$

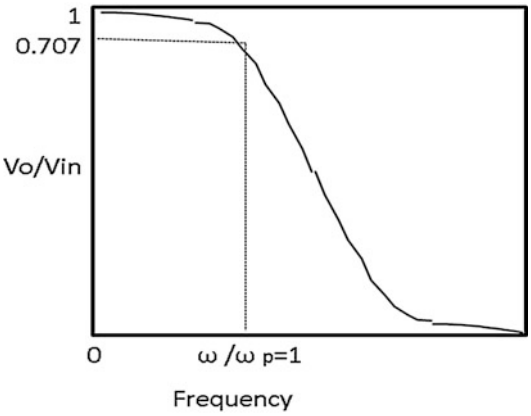
The magnitude response is given by,

$$|T(s)| = 11/\left[\left(1 + \left(\omega/\omega_p\right)^2\right]^{1/2}\right.$$

where $\omega = 2\pi f$, f = frequency and $\omega_p = 1/RC$.

- For $\omega/\omega_p = 0$: $|T(s)| = 1$ or $20\text{Log}(1) = 0$ dB
- For $\omega/\omega_p = 1$: $|T(s)| = 1/(2)^{1/2} = 0.707$ or $20\text{Log}(0.707) = -3$ dB
- For $\omega/\omega_p =$ Infinity: $|T(s)| = 0$

The frequency response is given below.



2.10 Active Filters Based on Simulated Inductors

Active filter design, based on simulated inductors, is a three step process:

- It begins with a LC prototype filter as shown in Fig. 2.15a.
- Next, the inductor is replaced by its transconductance model as shown in Fig. 2.15b, where the inductor model is shown in the dotted box.
- Finally, the transconductance model is replaced by its active equivalent circuit as shown in Fig. 2.15c.

2.10.1 LC Prototype Filter

We begin with the LC prototype filter as shown in Fig. 2.15a.

The nodal equation is given by,

$$V_1(G_1 + sC_1 + 1/_{sL1}) = G_1 V_{in} \tag{2.41}$$

where $_{G1} = 1/R_1$. The voltage transfer function is given by

$$H(s) = \frac{V_1}{V_{in}} = \frac{s/(R1C1)}{s^2 + s(C1/R1) + 1/L1C1} \tag{2.42}$$

which is a Bandpass function (see the previous section)? Comparing the denominator with the following characteristics equation:

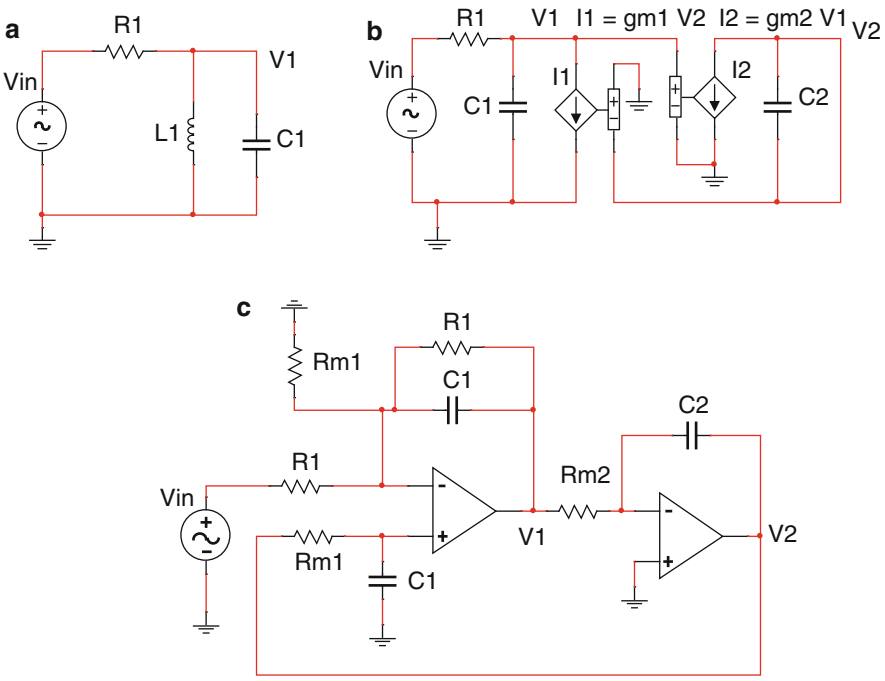


Fig. 2.15 (**a**) An LC prototype filter, (**b**) its transconductance model and (**c**) the corresponding active realization by means of OpAmps

$$s^2 + s(C1/R1) + 1/L1C1 = s^2 + s\,(\omega_o/Q) + \omega o2 \tag{2.43}$$

We obtain,

$$\omega_o = (1/L_1C_1)^{1/2} \tag{2.44}$$

$$Q = R_1(C_1/L_1)^{1/2} \tag{2.45}$$

where ω_o is the center frequency and Q is the quality factor, which is also known as selectivity.

2.10.2 *Transconductance Model of the Prototype Filter*

Next, consider the transconductance model of the LC prototype filter as shown in Fig. 2.15b. Here, the simulated inductor L_1 is given by:

$$L_1 = C_2/(g_{m1}g_{m2})$$

where, the transconductances g_{m1} and g_{m2} are realized as:

- $g_{m1} = I_1/V_2$ and
- $g_{m2} = I_2/V_1$

It is interesting to observe that the LC prototype filter has a single transfer function while the transconductance model has two transfer functions. The corresponding nodal equations are given by:

$$V_1(_{sC1} + G_1) + V_2 g_{m1} = V_{in} G_1$$
$$-V_1 g_{m2} + V_2 sC_2 = 0$$

where, G1 = 1/R1. The above equations can be written as a 2×2 matrix:

$$\begin{bmatrix} (sC1 + G1) & gm1 \\ -gm2 & sC2 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix} = \begin{bmatrix} VinG1 \\ 0 \end{bmatrix}$$

In order to find the solution for V_1 and V_2, we will use Cramer's rule [7]. The process is as follows:

Step 1: Find the determinant D:

$$D = \begin{bmatrix} (sC1 + G1) & gm1 \\ -gm2 & sC2 \end{bmatrix} = s^2 C_1 C_2 + sC_2 G_1 + g_{m1} g_{m2}$$

where,

- D is the denominator of the second order polynomial.
- It determines ω_o and Q

Step 2: Replace the first column of the matrix by the right hand side of the equation and find the determinant D1.

$$D_1 = \begin{bmatrix} VinG1 & gm1 \\ 0 & sC2 \end{bmatrix} = VinsC2G1$$

where,

- D_1 finds the solution for V1 and determines the numerator polynomial for the first transfer function H1(s).
- It also determines the type of the filter

Step 3: Replace the second column of the matrix by the right hand side of the equation and find the determinant D_2.

$$D_2 = \begin{bmatrix} (sC1 + G1) & VinG1 \\ -gm2 & 0 \end{bmatrix} = \text{Vin gm1gm2}$$

where,

- D_2 finds the solution for V_2 and determines the numerator polynomial for the second transfer function H2(s).
- It also determines the type of the filter

Step 4: Find the Solutions for V_1 and V_2:
The solution for V_1 and V_2 are:

$$V_1 = D_1/D = \text{Vin}\, sC_2G_1/(s^2C_1C_2 + sC_2G_1 + g_{m1}g_{m2})$$
$$V_2 = D_2/D = \text{Vin}\, g_{m1}g_{m2}/(s^2C_1C_2 + sC_2G_1 + g_{m1}g_{m2})$$

The corresponding voltage transfer functions are:

$$H_1(s) = V_1/V_{in} = sC2G_1/(s^2C_1C_2 + sC_2G_1 + g_{m1}g_{m2})$$
$$H_2(s) = V_2/V_{in} = g_{m1}g_{m2}/(s^2C_1C_2 + sC_2G_1 + g_{m1}g_{m2})$$

Therefore, $H_1(s)$ is a bandpass function and $H_2(s)$ is a lowpass function. Comparing the denominator with the characteristics equation $s^2 + s(\omega_o/Q) + {\omega_o}^2$, we obtain,

- $\omega_0 = [(g_{m1}g_{m2})/\ (C_1C_2)]^{1/2}$ (2.46)
- $Q = R_1 g_m (C1/C_2)^{1/2}$ (2.47)
- $g_{m1} = g_{m2} = g_m$

2.10.3 RC Active Equivalent of the LC Prototype Filter

Finally, the equivalent active RC filter is obtained by replacing the transconductance integrators by their equivalents as developed earlier. This is shown in Fig. 2.15c.

- The first stage has a non-inverting integrator and an inverting amplifier. The non-inverting integrator has a pair of 1k resistors, realizing g_{m1} (1 mMho). This stage is realized by means of a differential transconductance integrator shown in the figure. The amplifier stage has a pair of 10k resistors, realizing a d.c. voltage gain of -1 ($V_1/V_{in} = 10k/10k = -1$).
- The second stage is an inverting integrator. This stage is realized by means of an inverting integrator. Realizing the second transconductance g_{m2} ($g_{m2} = 1$ mMho).

The voltage transfer functions are:

$$H1(s) = V_1/V_{in} = sC2G1/(s^2C_1C_2 + sC_2G_1 + 1/R_{m1Rm2})$$
$$H1(s) = V_2/V_{in} = g_{m1}g_{m2}/(s^2C_1C_2 + sC_2G_1 + 1/R_{m1Rm2})$$

Therefore, H1(s) is a bandpass function and H2(s) is a lowpass function. Comparing the denominator with the characteristics equation $s2 + s(\omega_o/Q) + \omega o2$, we obtain,

- $\omega_0 = 1/(R_{m1}R_{m2}C_1C_2)\big]^{1/2}$
- $Q = R_1/R_m(C_1/C_2)^{1/2}$
- $g_{m1} = g_{m2} = g_{m=1/}R_m$

Problem 2.4
Consider the LC prototype as shown in Fig. 2.15a with the following design parameters:

- $R_1 = 10k$
- $C_1 = 1nF$
- $L_1 = 0.81\,H$

Find: f_o and Q

Solution:

$$\omega_o = (1/L_1C_1)^{1/2}$$
$$f_o = (1/2\pi)\big[1/(0.81\,H \times 1\,nF)^{1/2} = 5,594.971\,Hz$$
$$Q = R_1(C_1/L_1)^{1/2} = 10^4 \times \left(10^{-9}/0.81\right)^{1/2} = 0.351364$$

Problem 2.5
Consider the transconductance model of the LC prototype filter as shown in Fig. 2.15b and calculate the values of transconductances and capacitors.

Solution:
The inductor is given by the following equation:

$$L_1 = C_2/g_{m1}g_{m2} = 0.81\,H$$

The value of the inductor can be realized by means of C_2, g_{m1} and g_{m2} as follows:

- $C_2 = 0.81 \times 10^{-6}F$
- $g_{m1} = g_{m2} = 10^{-3}Mho$
- $L_1 = C_2/g_{m1}g_{m2} = 0.8 \times 10^{-6}/\left(10^{-3} \times 10^{-3}\right) = 0.81\,H$

Therefore, the transconductance model of the filter has the following design parameters:

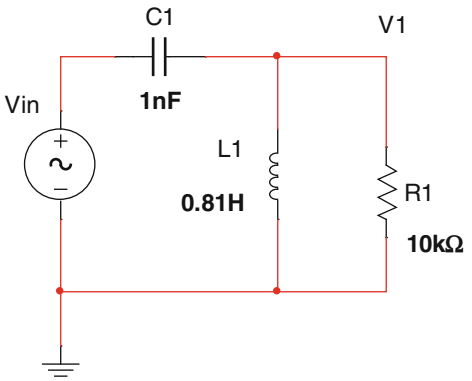
- $R_1 = 10k$
- $C_1 = 1nF$
- $C_2 = 0.81\,\mu F$
- $g_{m1} = g_{m2} = mMho$

Problem 2.6
Consider the active RC equivalent of the LC prototype filter as shown in Fig. 2.15c and calculate the values of resistors and capacitors. Assume ideal OpAmp.

Solution:
The active RC filter is obtained by replacing the transconductance integrators by their equivalents. Therefore, the active RC filter has the following design parameters:

- $R_1 = 10k$
- $C_1 = 1nF$
- $C_2 = 0.81\,\mu F$
- $R_{m1} = R_{m2} = 1k\,Ohm$

Drill Exercise
Consider the LC prototype circuit as shown below:



(a) Show the transconductance model of the LC prototype and its active equivalent circuit
(b) Simulate and verify that they are functionally identical.

2.11 Higher Order Filters

2.11.1 Third Order Lowpass Ladder Filter

The transconductance model of the floating inductor can be used to describe an LC section of type Fig. 2.16a. Replacing the floating inductor by its transconductance model, we obtain Fig. 2.16b. There are three integrators with the directions of the current sources as indicated in the figure. At this point we are able to transform the transconductance circuit into an active RC equivalent circuit. This can be achieved simply by replacing the three transconductance integrators by their equivalent models. Figure 2.16c shows the active RC third order filter.

Step-By-Step-Design
Step 1: Obtain a prototype LC filter as shown in Fig. 2.16a. The filter has the following design values:

- $R = 10k$
- $C_1 = C3 = 9.91\,nF$
- $L_1 = 0.809\,H$

Step 2: Transform the LC prototype filter in to an equivalent transconductance model [see Fig. 2.16b]:

The transconductance model of the third order filter can be realized by replacing the floating inductor by its transconductance model. This is given in Fig. 2.16b. The filter parameters are:

- $R = 10k$
- $C_1 = C3 = 9.91\,nF$
- $C2 = 0.81\,\mu F$
- $g_{m1} = g_{m2} = gm3\text{-} = 1\,mMho$
- $L_1 = C2/g_{m1}g_{m2} = 0.81\,\mu F/1\,\mu uMho = 0.81\,H$

Step 3: Transform the Transconductance model of the filter in to an equivalent RC active filter [see Fig. 2.16c]:

The active equivalent circuit of the transconductance model can be obtained by replacing the transconductances by their active equivalent circuits. The result is presented below.

- $R_1 = 10k$
- $C_1 = C3 = 9.91\,nF$
- $C_2 = 0.81\,\mu F$

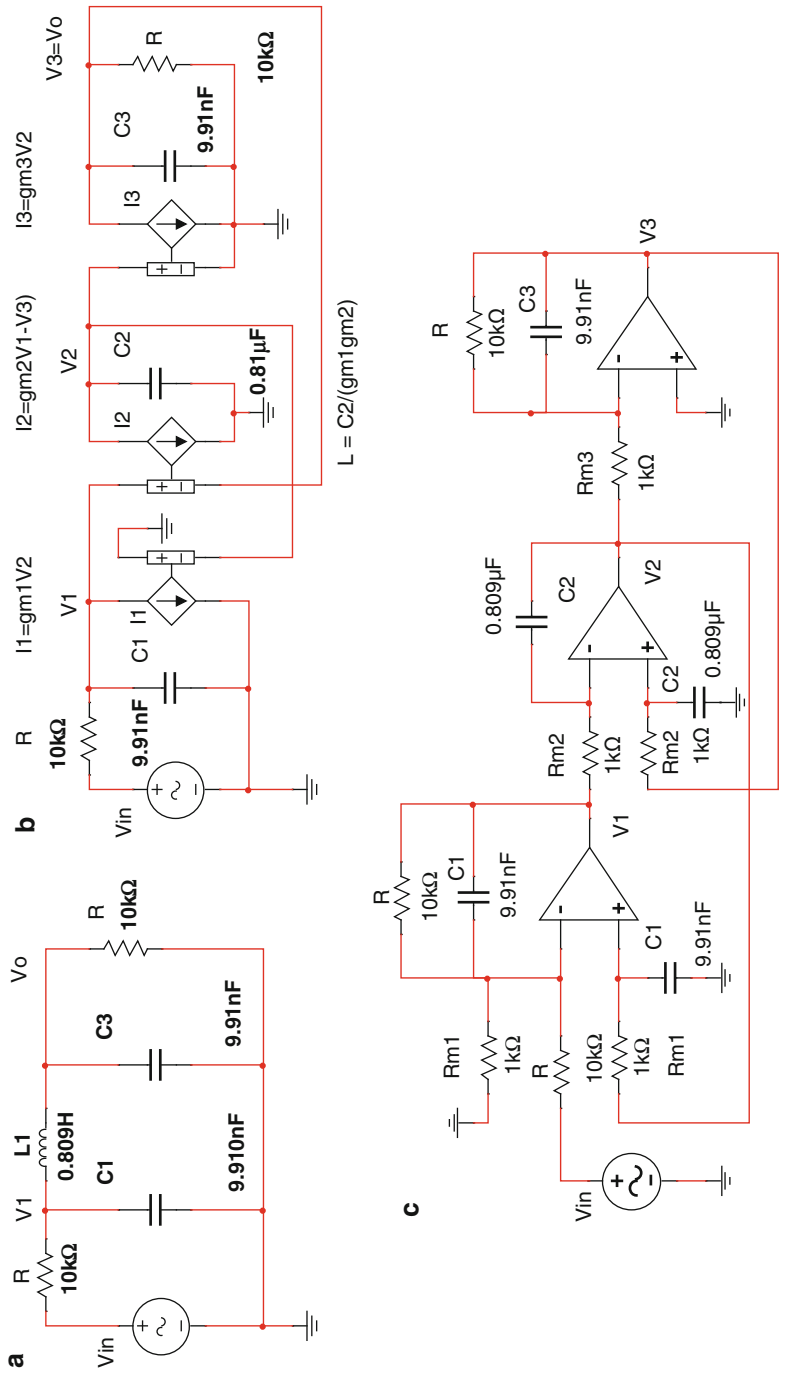


Fig. 2.16 (**a**) A third order LC lowpass filter (**b**) the transconductance model and (**c**) the active equivalent circuit of the third order lowpass filter

- $R_{m1} = 1/g_{m1} = 1k$
- $R_{m2} = 1/g_{m2}\text{-} = 1k$
- $R_{m3} = 1/g_{m3}\text{-} = 1k$
- $L_1 = R_{m1}R_{m2}C_2 = 1k \times 1k \times 0.81\,\mu F = 0.81\,H$

The design is complete.

2.11.2 *Fifth Order Lowpass Ladder Filter*

The design methods developed in the previous section can be used to construct higher order ladder filters such as all pole ladder filters. Let's consider a fifth order LC prototype as shown in Fig. 2.17a. Replacing the floating inductor by its transconductance model, we obtain Fig. 2.17b. There are five integrators with the directions of the current sources as indicated in the figure. The active RC equivalent circuit can be obtained simply by replacing the corresponding transconductance integrators by their equivalent models. Figure 2.17c shows the active RC fifth order ladder filter.

Step-By-Step-Design
Step 1: Obtain a prototype LC filter as shown in Fig. 2.17a. The filter has the following design values:

- $R = 10k$
- $C_1 = C_3 = C_5 = 9.91\,nF$
- $L_1 = L_2 = 0.81\,H$

Step 2: Transform the LC prototype filter in to an equivalent transconductance model [see Fig. 2.17b]:

The transconductance model of the fifth order filter can be realized by replacing the floating inductors by their transconductance models. This is given in Fig. 2.17b. The filter parameters are:

- $R = 10k$
- $C_1 = C3 = C5 = 9.91\,nF$
- $C2 = C4 = 0.81\,\mu F$
- $gm1 = gm2 = gm3 = gm4 = gm5 = 1\,mMho$
- $L1 = C2/(gm1gm3) = 0.81\,\mu F/\mu Mho = 0.81\,H$
- $L2 = C4/(gm3gm5) = 0.81\,\mu F/\mu Mho = 0.81\,H$

Step 3: Transform the Transconductance model of the filter in to an equivalent RC active filter [see Fig. 2.17c]:

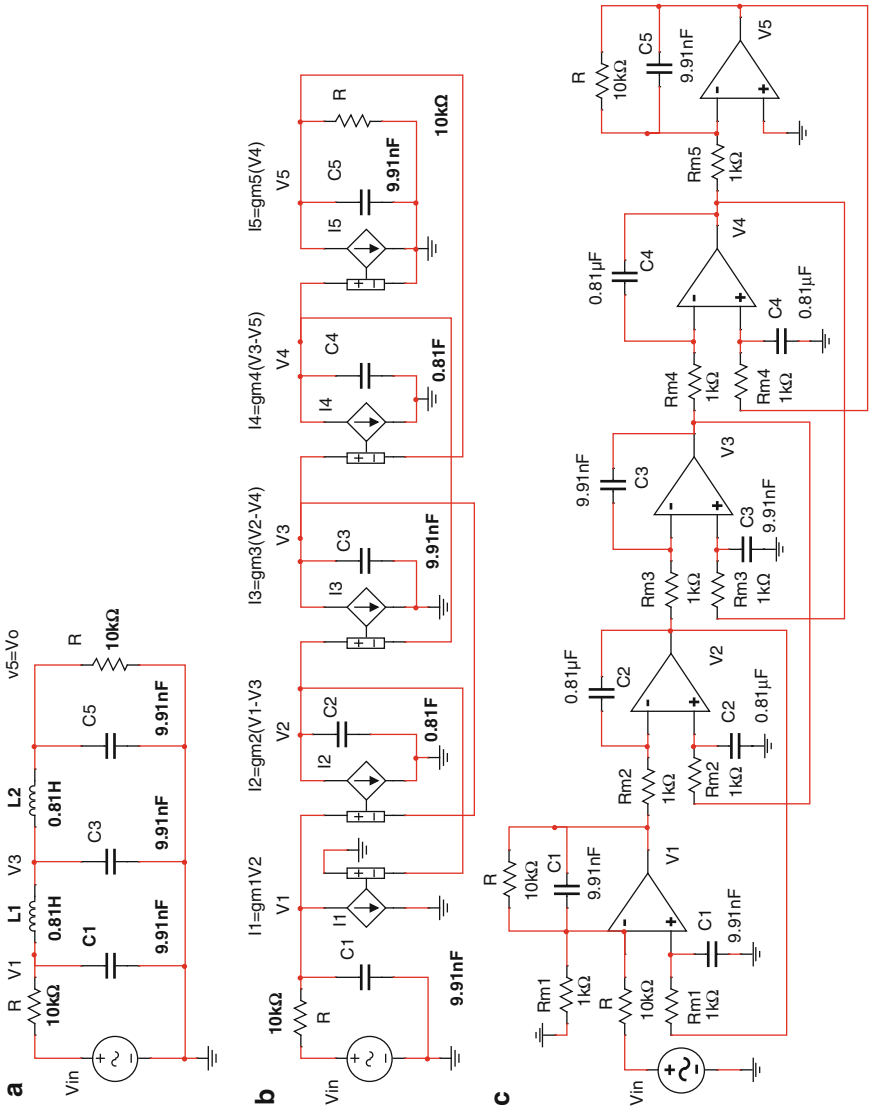


Fig. 2.17 (**a**) A fifth order all-pole LC filter. (**b**) Transconductance model (**c**) Active RC equivalent circuit

The active equivalent circuit of the transconductance model can be obtained by replacing the transconductances by their active equivalent circuits. The result is presented below.

- $R = 10k$
- $C_1 = C3 = C5 = 9.91\,nF$
- $C2 = C4 = 0.81\,\mu F$
- $R_{m1} = R_{m2} = R_{m3} = R_{m4} = R_{m5} = 1k$
- $L_1 = R_{m1}R_{m3}C_2 = 0.81\,\mu F/\mu Mho = 0.81\,H$
- $L_2 = R_{m3}R_{m5}C_4 = 0.81\,\mu F/\mu Mho = 0.81\,H$

The design is complete.

2.12 Conclusions

- Introduces transconductances as filter building blocks
- Grounded and floating inductors are simulated using transconductance models
- Shows how to design active filters from LC prototype filters
- Examples are given to design Higher Order Active Filters Based on Simulated Inductors

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Chapter 3
Switched Capacitor Building Blocks and Filters

Topics

- Switched Capacitor Resistor
- Switched Capacitor Integrators
- Switched Capacitor Filter Building Blocks
- Higher order Switched Capacitor Filters

3.1 Switched Capacitor Resistor

In MOS (Metal Oxide Semiconductor) integrated technology, it is relatively simple to produce transistors and capacitors but resistors present problems. This led a group of researchers [1, 2] to the idea of replacing resistors by periodically Switched-Capacitors [1, 2]. Assuming that the clock frequency used to operate the switches is much higher than the signal frequency a resistor R of value given by the following equation:

$$R = 1/f_c Cr \tag{3.1}$$

can be generated by means of the arrangement shown in Fig. 3.1b, where

- f_c = Clock frequency
- Cr = Switched capacitor
- Φ1 and Φ2 are two complementary non-overlapping clocks (see Fig. 3.1d, generated by the arrangement as shown in Fig. 3.1c).

The operation of the switched capacitor circuit is as follows:

- In phase 1, S_1 is closed (S_2 is open). The switched capacitor C_r charges to V_1. The value of the charge is given by:

S. Faruque, *Radio Frequency Source Coding Made Easy*, SpringerBriefs
in Electrical and Computer Engineering, DOI 10.1007/978-3-319-15609-5_3

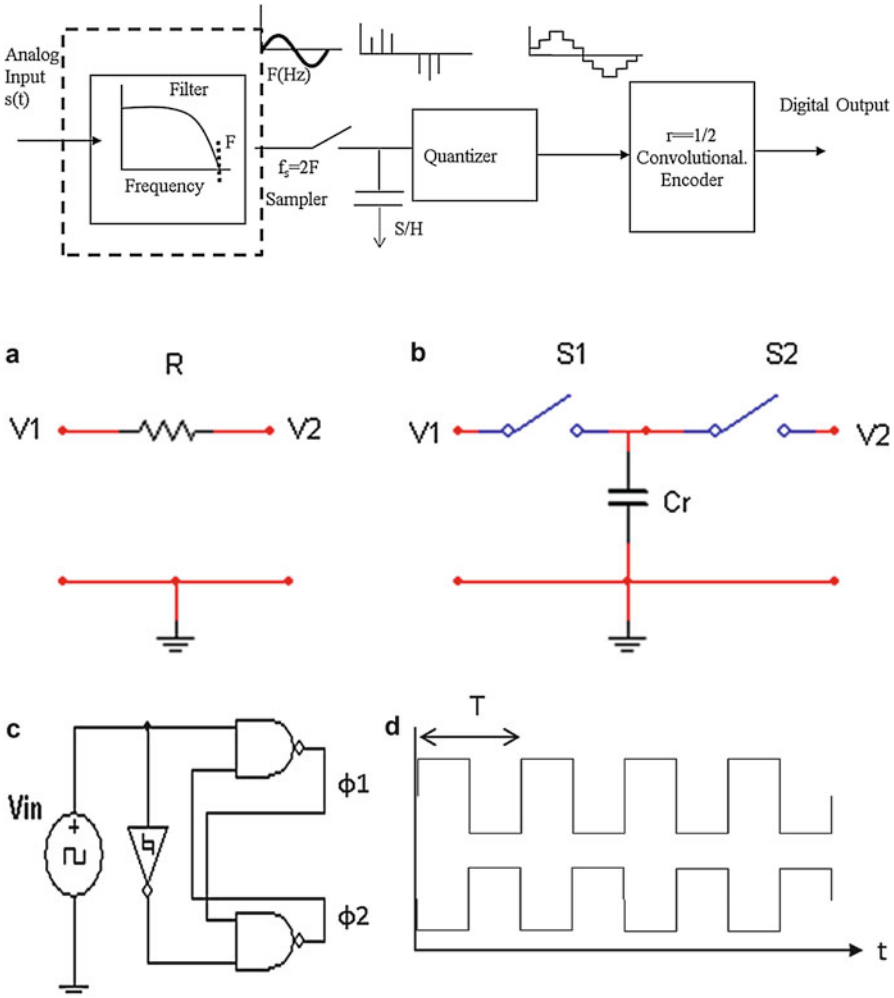


Fig. 3.1 (**a**) A conventional resistor, (**b**) Switched-capacitor resistor, (**c**) Two-phase clock generator and (**d**) Two-phase non-overlapping clocks

$$Q_1 = C_r V_1 \tag{3.2}$$

- In phase 2, S_2 is closed (S_1 is open). The capacitor now discharges to V_2 (assume $V_1 > V_2$). The value of the charge into Cr is given by:

$$Q_2 = c_r V_2 \tag{3.3}$$

Since V1 > V2, the transfer of charge from V1 to V2 will be:

$$\Delta Q = Q_1 - Q_2 = C_r(V_1 - V_2) \tag{3.4}$$

If this operation repeats periodically at a rate $f_c = 1/T$, where T is the clock period and fc is the clock frequency, the average current flow from V_1 to V_2 will be:

$$I = \Delta Q/T = f_c C_r(V_1 - V_2) \tag{3.5}$$

The value of the simulated resistance will be:

$$R = (v_1 - V_2)/I = 1/(f_c C_r) \tag{3.6}$$

Therefore, a capacitor, switching between two nodes, where the nodal voltages are V_1 and V_2, simulates a resistor, Which is inversely proportional to the value of Cr. This is very attractive in IC technology since a large value of resistance can be realized in a small silicon area. Moreover, the value of the simulated resistor can be controlled by the clock frequency fc.

3.2 Switched-Capacitor Integrators and Transconductances

The idea of Switched-Capacitor Transconductance (SCT) was developed earlier [3, 4]. In this section we consider a similar approach to develop transconductance models of various SC-Integrators.

Let us consider the conventional RC-Integrator as shown in Fig. 3.2a. Replacing the resistor by a switched-capacitor resistor, we obtain the SC-Integrator as shown in Fig. 3.2b. Two-phase clock is assumed with the left switch S1 closed in phase 1 and the right switch S2 closed in phase 2.

During phase-1, the capacitor Cr is charged to the voltage V_{in}. During phase 2, it is connected at the negative input of the operational amplifier which is at the virtual ground. Now the capacitor sees a zero potential between its terminals and it is discharged instantaneously.

The amount of charge which is transferred into the feedback capacitor C will be $\Delta Q = CrV_{in}$. It is assumed that the operational amplifier is ideal.

If this operation is repeated at a clock rate T, the average value of current flowing through the capacitor C will be given by

$$I = \Delta Q/T = C_r V_{in}/T = f_c C_r V_{in} = g_m V_{in} \tag{3.7}$$

where

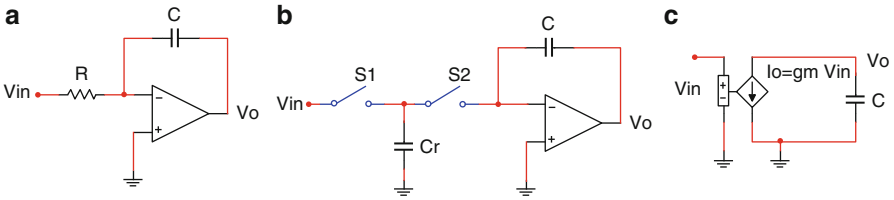


Fig. 3.2 (**a**) An RC integrator. (**b**) Switched-capacitor integrator (**c**) The equivalent transconductance model

- $R = 1/(f_c C_r)$
- $g_m = f_c C_r; \quad f_c = 1/T$ (3.8)
- $R = 1/g_m$

Here g_m is the Transconductance. Thus the switched-capacitor integrator may equally be described by the circuit of Fig. 3.2c.

The transfer functions of these integrators may be expressed separately as follows:

- RC-Integrator : $V_o = -V_{in} \cdot 1/sCR$ (3.9)
- SC-Integrator : $V_o = V_{in} f_c Cr/sC$ (3.10)
- SCT-Integrator : $V_o = V_{in} \cdot g_m/sC$ (3.11)

where

$$R = 1/f_c Cr = 1/g_m$$

The above three integrators are functionally identical.

3.3 Differential Integrator

A differential integrator integrates the difference between two voltages. The conventional RC-integrator is shown in Fig. 3.3a which requires two identical resistors and two identical capacitors. In switched capacitor technique, it is quite simple to obtain a differential integrator because a single capacitor can sample the difference between two voltages. Moreover, a single feedback capacitor is used to store the difference of charges. This is shown in Fig. 3.3b. The transconductance model is in Fig. 3.3c which is obtained in a similar manner as described at the beginning of this section. The voltage transfer functions are expressed as:

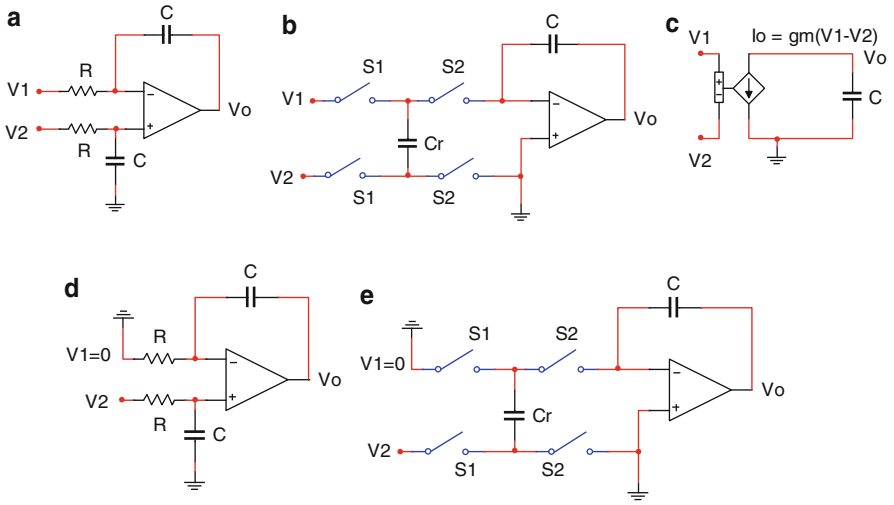


Fig. 3.3 (**a**) An RC-differential integrator. (**b**) Switched capacitor differential integrator. (**c**) The transconductance model (**d**) Non-inverting integrator, (**e**) SC non-inverting integrator

- RC-Integrator : $V_o = -(V_1 - V_2)1/sCR$ (3.12)
- SC-Integrator : $V_o = -(V_1 - V_2)\, f_c Cr/sC$ (3.13)
- SCT-Integrator : $V_o = -(V_1 - V_2)g_m/sC$ (3.14)

Once again, the three integrators are functionally identical.

Other realization of integrators such as non-inverting summing, multi-input etc. will follow an obvious pattern. An example of a non-inverting integrator with $V_1 = 0$, is given in Fig. 3.3d and its SC counterpart in Fig. 3.3e.

3.4 Z-Domain Analysis

3.4.1 Switched Capacitor (Sc) Resistor

A switched-capacitor network is essentially a sampled-data network. Therefore for an accurate result, z-domain analysis is required. The resemblance between a sampled-data network and its continuous time counterpart depends primarily on the type of transformation which describes the sampled-data system. One such transformation is the LDI-Transformation (Loss-less Digital Integrator) [5]. In order to examine the behavior of a capacitor in the switching mode, let us consider the switched-capacitor resistor simulation circuit once again. This is shown in Fig. 3.4 along with the switching scheme.

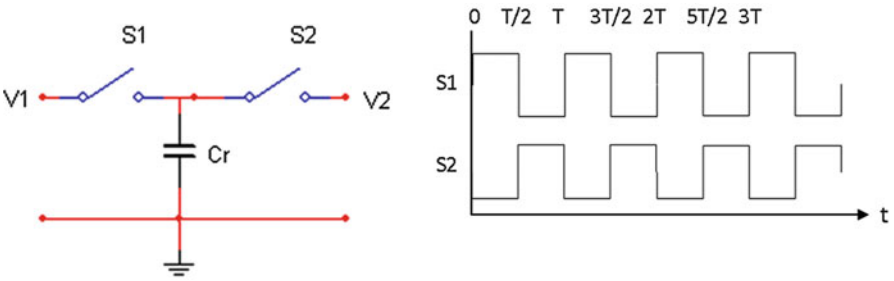


Fig. 3.4 A switched-capacitor resistor and its timing diagram

During phase 1, Cr samples the Voltage $V_1(nT)$. During phase 2, it is discharged to the voltage $V_2(n+½)T$. The amount of charge flowing from port 1 to port 2 is given by:

$$q_{1,2}(nT) = CrV_2(n+½)T - CrV_1(nT) \tag{3.15}$$

If we start from the second port of Fig. 3.4, we obtain by similar reasoning

$$q_{2,1}(nT) = CrV_1(n+½)T - CrV_2(nT) \tag{3.16}$$

The above equations can be expressed in terms of delays as well:

$$q_{1,2}(nT) = CrV_2(nT) - CrV_1(n-½)T \tag{3.17}$$

$$q_{2,1}(nT) = CrV_1(nT) - CrV_2(n-½)T \tag{3.18}$$

In the z-domain, the above equations are expressed as:

$$Q_{1,2}(z) = CrV_2(z) - CrV_1(z)Z^{-½} \tag{3.19}$$

$$Q_{2,1}(z) = CrV_1(z) - CrV_2(z)Z^{-½} \tag{3.20}$$

In the above Z-domain equations, $Z^{-½}$ represents a half delay.

3.4.2 Switched Capacitor (sC) Integrator

Let us now introduce an ideal operational amplifier in conjunction with the switched-capacitor as shown in Fig. 3.5.

Operation of the SC-Integrator is as follows:

During phase-1, the capacitor Cr is charged to the voltage V_{in}. The amount of charge sampled at the sampling instant nT will be:

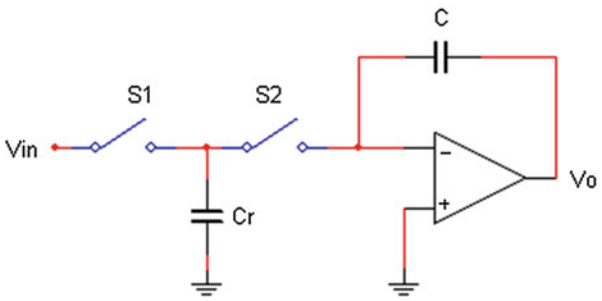


Fig. 3.5 The switched-capacitor integrator

$$Q(nT) = CrV_{in}(nT) \tag{3.21}$$

During phase 2, Cr is connected to the negative input of the operational amplifier at $(n - 1/2)T$.

Since the OpAmp is ideal, the capacitor sees a zero potential between its terminals and it is discharged instantaneously at the time instant $(n - ½)T$. The amount of charge which is transferred into the feedback capacitor C will be:

$$CrV_1(n - ½)T \tag{3.22}$$

This value of charge will be added to the previously held charges by the integrating capacitor C. Therefore we can write: the following charge equation:

$$CrV_{in}(n - ½)T + [CV_0(nT) - CV_0(n - 1)T] = 0 \tag{3.23}$$

Applying z-transform in (7.10) yields

$$CrV_in(z)Z^{-½} + \left[CV_0(z) - CV_0(z)Z^{-1}\right] = 0 \tag{3.24}$$

The voltage transfer function of the SC-Integrator is therefore,

$$H(z) = \frac{V_o}{V_{in}} = -\left(\frac{C_{ro}}{C}\right) \frac{Z^{-1/2}}{1 - Z^{-1}} \tag{3.25}$$

It is assumed that the output is taken in phase 2 of the clock.

It was pointed out earlier that the resemblance between a sampled-data network and its continuous time counterpart depends primarily on the type of transformation which describes the sampled-data systems. The "Lossless Discrete Integrator" (LDI) was first introduced by Bruton [5] in the digital filter design. It is represented by a special z-domain transformation whose properties are such that a discrete time integrator which has only a half delay ($Z^{-1/2}$) has exactly the same phase shift as a continuous time integrator. The transformation is given by

$$S = \frac{1}{T}\frac{1 - Z^{-1}}{Z^{-1/2}} \tag{3.26}$$

Substituting for $Z = e^{j\omega T}$, we obtain

$$S = \frac{j2}{T}\mathrm{Sin}\,(\omega T/2) \tag{3.27}$$

which is purely imaginary? Thus the discrete time integrator has the same phase shift as an analog integrator. The discrete time voltage transfer function can be expressed as:

$$\begin{aligned} H(z) &= H(s) = -(Cr/C)1/ST \\ &= -f_c Cr/sC \\ &= -g_m/sC \end{aligned} \tag{3.28}$$

Thus the transconductance concept which was developed in the previous section is valid through the LDI transformation.

3.4.3 Frequency Response of SC-Integrator

In order to evaluate the frequency response of the SC-Integrator, consider the z-domain transfer function as s given below:

$$H(z) = V_0/V_{in} = -\frac{Cr}{C}\frac{Z^{-½}}{1 - Z^{-1}} \tag{3.29}$$

Substitute for $Z = e^{j\omega T}$ to obtain

$$H\left(e^{j\omega T}\right) = -\frac{(C_m/C)(\omega T)}{2\,j\omega T[\mathrm{Sin}\,(\omega T/2)]} \tag{3.30}$$

This transfer function should be compared with the conventional analog integrator which has a transfer function

$$H(j\omega) = -\frac{1}{j\omega RC} \tag{3.31}$$

They both are purely imaginary. The amplitude response Is similar as well if ω is chosen so small that $\mathrm{Sin}(\omega T/2) \underline{\sim} \omega T/2$.

3.5 Switched-Capacitor Biquad Filters

A biquad (bi-quadratic) filter is a second order filter which can provide various second order transfer functions. A biquad transfer function is the one whose numerator and denominator polynomials are quadratic in nature. Chapter 2 provides some of the most useful second order transfer functions and their frequency responses. In this section we will briefly review lowpass and bandpass functions and realize them by means of switched capacitor technique.

3.5.1 Lowpass Filter

A Lowpass filter is described by the following transfer function:

$$T(s)\frac{\omega z}{s^2+\left(\frac{\omega p}{Q p}\right)s+\omega p} \tag{3.32}$$

where,

$s = j\omega$ Laplace transform variable
ω_z = zeroes of the transfer function
ω_p = poles of the transfer function
Q_p = quality factor of the poles

Zeros are described by the numerator polynomial and Poles are described by the denominator polynomial. Most frequently used transfer functions are described in the following:

The frequency response is shown in Fig. 3.6. The pole frequency ω_p is measured when the voltage transfer function |T(s) is 70 % of its maximum value.

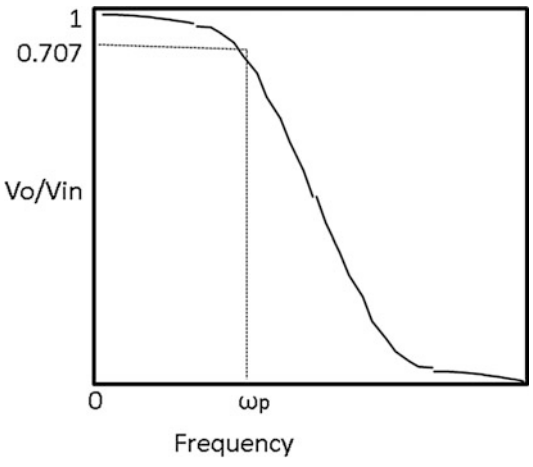


Fig. 3.6 A lowpass response. ω_p is the pole frequency

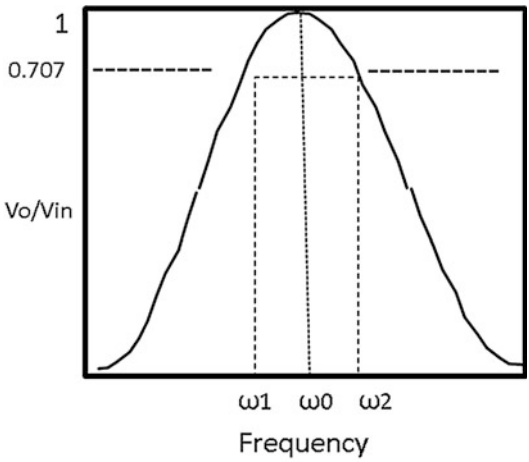


Fig. 3.7 Bandpass response

3.5.2 Bandpass Filter

A band pass filter is described by its transfer function

$$T(s) = \frac{\left(\frac{\omega z}{Qz}\right)s}{s^2 + \left(\frac{\omega p}{Qp}\right)s + \omega p} \tag{3.33}$$

It has a frequency response as shown in Fig. 3.7, where ω_p is the pole frequency.

3.5.3 Switched Capacitor Biquad

Let us consider the RC active Biquad filter as shown in Fig. 3.8a. This circuit has two voltage transfer functions as follows:

- $H_1(s) = V_1/V_{in}$ and
- $H_2(s) = V_2/V_{in}$.

For the above voltage transfer functions, we need to find solutions for V1 and V2. Since there are two equations and two unknowns V1 and V2, we will use Cramer's rule to find the solution for V1 and V2 [6]. We will also use resistors as conductors G ($G = 1/R$) and capacitors as frequency dependent conductance sC (impedance $= 1/sC$) where $s = j\omega$. It is assumed that the students are familiar with Cramer's rule. Briefly, Cramer's rule is an explicit formula for the solution of a system of linear equations. It finds the solution in terms of determinants of matrices.

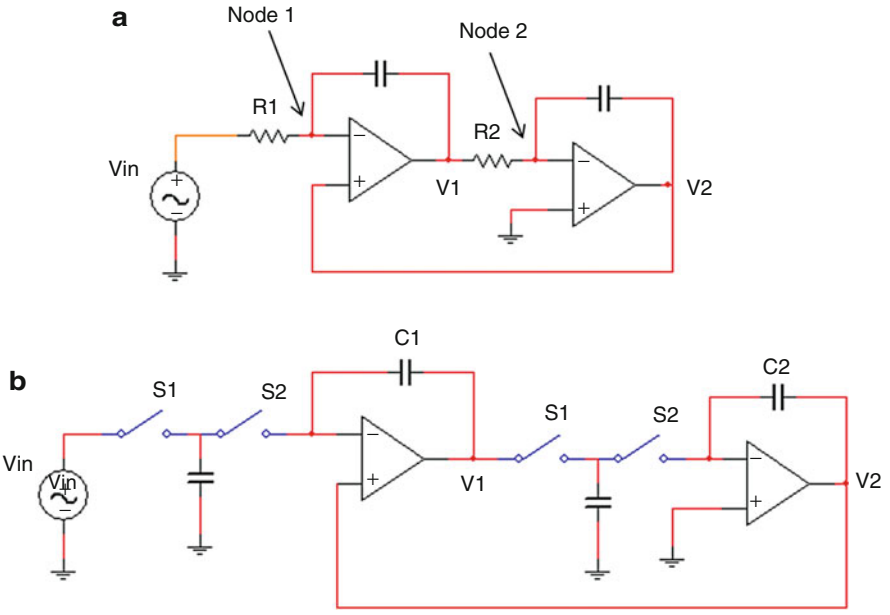


Fig. 3.8 Second order filter. (**a**) A second order b-quadratic (biquad) filter. (**b**) Switched capacitor biquad

Now, consider the second order Biquad filter as shown in Fig. 3.8a. Here, we need to find the solution for V1 and V2. We will use nodal equations, which is essentially KCL. There are two nodal equations: one at the negative input of the first OpAmp (Node 1) and the other at the negative input of the second OpAmp (Node 2). Note that there are no nodal equations at v_{in}, V_1 and V_2, since there ideal voltage sources.

At node 1, the nodal equation is given by:

$$V_2(G_1 + sC_1) - V_1 sC_1 - V_{in}G_1 = 0$$

At node 2, the nodal equation is:

$$0(G_2 + sC_2) - V_1 G_2 - V_2 sC_2 = 0$$

Notice that the first term is stricken out since it is multiplied by zero. This is due to the fact that this node is virtual ground.

The above equations can be written as a 2×2 matrix:

$$\begin{bmatrix} -sC1 & G1 + sC1 \\ -G2 & -sC2 \end{bmatrix} \begin{bmatrix} V1 \\ V2 \end{bmatrix} = \begin{bmatrix} VinG1 \\ 0 \end{bmatrix}$$

In order to find the solution for V1 and V2, we will use Cramer's rule. The process is as follows:

Step 1: Find the determinant D as:

$$\mathrm{D} = \begin{bmatrix} -sC1 & G1 + sC1 \\ -G2 & -sC2 \end{bmatrix} = \mathrm{s^2C_1C_2 + sC_1G_2 + G_1G_2}$$

where,

- D is the denominator of the second order polynomial.
- It determines ω_o and Q

Step 2: Replace the first column of the matrix by the right hand side of the equation and find the determinant D1.

$$\mathrm{D1} = \begin{bmatrix} VinG1 & G1 + sC1 \\ 0 & -sC2 \end{bmatrix} = -\mathrm{V_{in}SC_2G1}$$

where,

- D1 finds the solution for V1 and determines the numerator polynomial for the first transfer function H1(s).
- It also determines the type of the filter

Step 3: Replace the second column of the matrix by the right hand side of the equation and find the determinant D2.

$$\mathrm{D2} = \begin{bmatrix} -sC1 & VinG1 \\ -G2 & 0 \end{bmatrix} = \mathrm{Vi_nG_1G_2}$$

where,

- D2 finds the solution for V2 and determines the numerator polynomial for the second transfer function H2(s).
- It also determines the type of the filter

Step 4 : Find the Solutions for V1 and V2:

$$\mathrm{V1} = \frac{D_1}{D} = \frac{-\mathrm{Vin\,sC2G1}}{D}$$

$$\mathrm{V2} = \frac{D_2}{D} = \frac{\mathrm{VinG1G2}}{D}$$

Step 5: Find the voltage transfer functions:

$$\mathrm{H1(s)} = \frac{V1}{Vin} = \frac{-\mathrm{sC2G1}}{D}$$

$$\mathrm{H2} = \frac{V2}{Vin} = \frac{\mathrm{VinG1G2}}{D}$$

where,

$$\mathrm{D} = \mathrm{s^2C_1C_2} + \mathrm{sC_1G_2} + \mathrm{G_1G_2}$$

Therefore,

- H1(s) is a bandpass function and
- H2(s) is a lowpass function

Notice that D is a quadratic function, common to both transfer functions. It is the numerator which determines the type of filter. In this case, H1(s) is a second order bandpass filter and H2(s) is a second order lowpass filter.

Comparing the denominator with the characteristics equation, we can write:

$$\mathrm{S^2} + \mathrm{s}(\omega_o/\mathrm{Q}) + \omega_o^2 = \mathrm{s^2C_1C_2} + \mathrm{s}/(\mathrm{C_2R_2}) + 1/(\mathrm{R_1R_2C_1C_2})$$

where,

$$\omega_0 = \sqrt{\frac{1}{\mathrm{R1R2C1C2}}}$$

$$\mathrm{Q} = \sqrt{\frac{\mathrm{R2C2}}{\mathrm{R1C1}}}$$

The equivalent switched capacitor filter is obtained simply by replacing the resistors by their sC circuit. This is shown in Fig. 3.8b. The values of the sc resistors are:

- $\mathrm{R_1} = 1/(\mathrm{f_cC_{r1}})$
- $\mathrm{R_2} = 1/(\mathrm{f_cC_{r2}})$
- $\mathrm{f_c}$ = Clock frequency.

3.6 Switched-Capacitor Filters Based on Simulated Inductors

In this section we shall consider the design of switched-capacitor filters based on simulated inductors. The step-by-step design process is as follows:

- Obtain an LC prototype filter
- Model the LC prototype filter by means of transconductances

- Design the active RC equivalent circuit by means of OpAmps, resistors and capacitors.
- Replace RC active integrators by means of SC equivalent integrators.

In order to simplify the design we shall consider identical examples and will refer to Chap. 2 whenever it is necessary.

3.6.1 SC Realization of Second Order LC Filters

Let us consider the second order active RC filter as shown in Fig. 3.9a. This is the same circuit which was designed from a second order passive LC prototype (see Chap. 2). The SC equivalent circuit is obtained by replacing the active RC integrators by means of their SC equivalent circuits. This is shown in Fig. 3.9b. Here, SC resistors are simulated as follows:

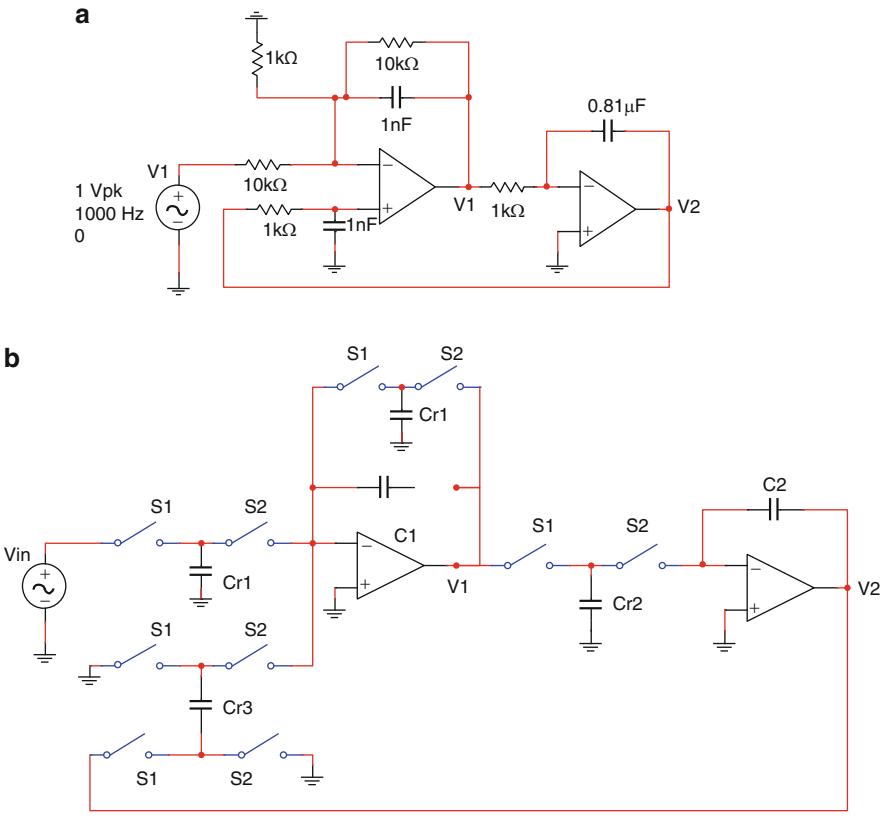


Fig. 3.9 (**a**) A second order active RC filter and (**b**) SC-equivalent circuit

- The first stage has a non-inverting integrator and an inverting amplifier. The non-inverting integrator has a pair of 1k resistors. This stage is realized by means of a differential switched capacitor scheme as shown in the figure. The amplifier stage has a pair of 10k resistors. This stage is realized separately by means of two SC resistors.
- The second stage is an inverting integrator. This stage is realized by means of an inverting SC integrator.

The values of the resistors are given by:
For the first state:

- 10k = 1/fcCr1
- 1k = 1/FcCr3

For the second stage:

- 1 k = 1/fcCr2

The clock frequency fc is the same for both the stages.

3.6.2 SC Realization of Third Order LC Ladder Filters

Let us consider the third order active RC filter as shown in Fig. 3.10a. This is the same circuit which was designed from a third order passive LC prototype filter (see Chap. 2).

The SC equivalent circuit is obtained by replacing the active RC integrators by means of their SC equivalent circuits. This is shown in Fig. 3.10b. Here, SC resistors are simulated as follows:

- The first stage has a non-inverting integrator and an inverting amplifier. The non-inverting integrator has a pair of 1k resistors. This stage is realized by means of a differential switched capacitor scheme as shown in the figure. The amplifier stage has a pair of 10k resistors. This stage is realized separately by means of two SC resistors.
- The second stage is a differential integrator. This stage is realized by means of a differential SC-integrator.
- The third stage is an inverting integrator. This stage is realized by means of an inverting SC integrator.

The values of the resistors are given by:
For the first stage:

- 10 k = $1/f_cC_{r1}$
- 1 k = $1/f_cC_{r11}$

For the second stage:

- 1 k = $1/f_cC_{r2}$

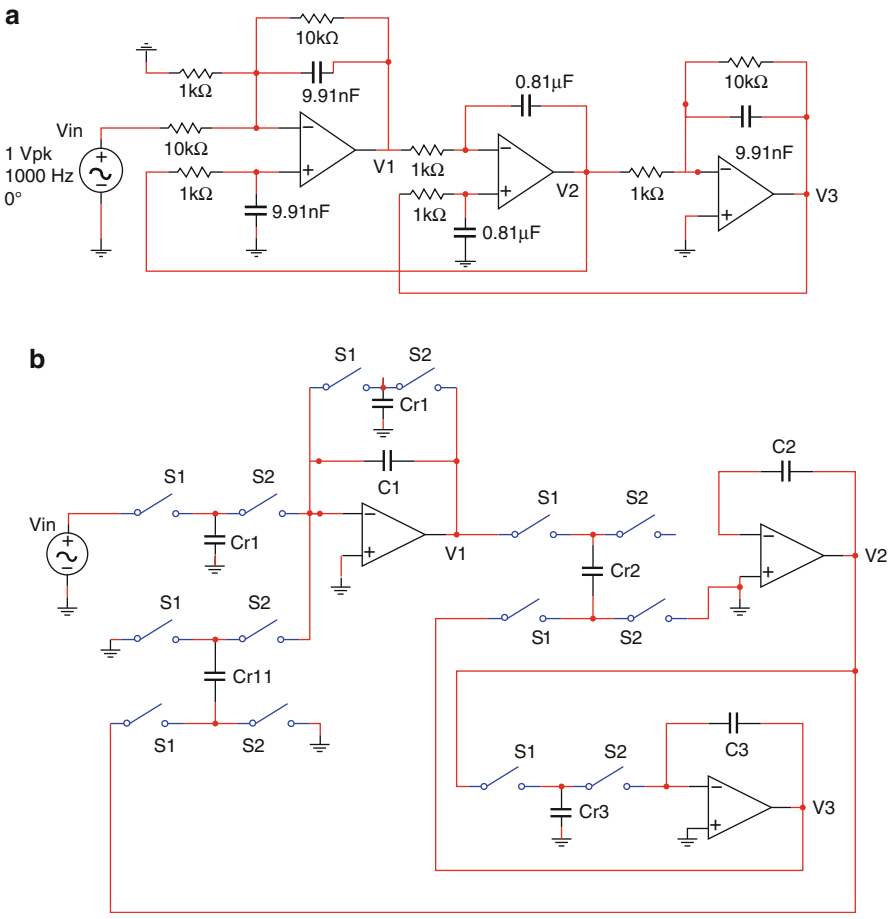


Fig. 3.10 (**a**) A third order active RC filter and (**b**) SC-equivalent circuit

For the third stage:

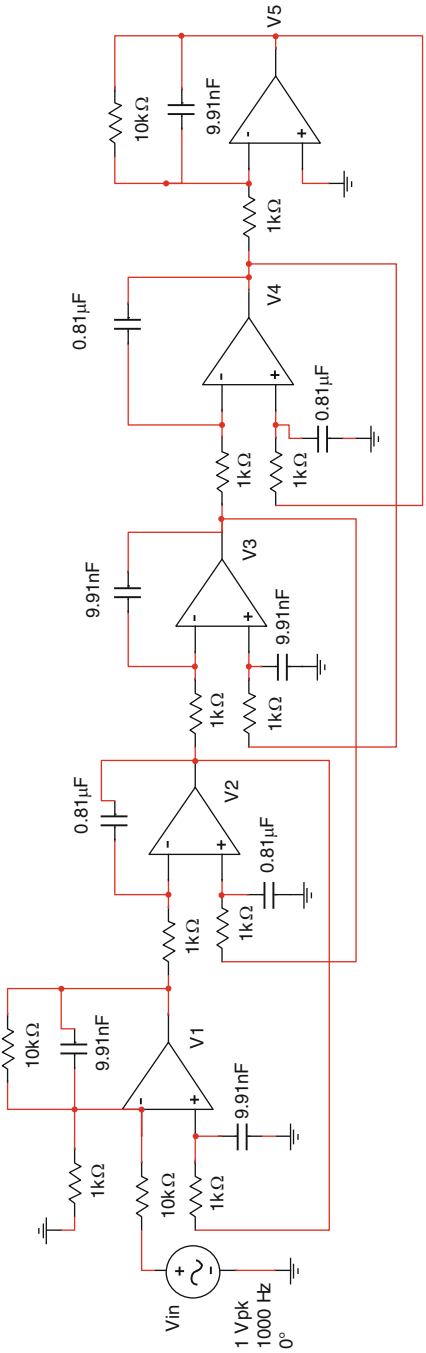
- $1\ \mathrm{k} = 1/f_c C_{r3}$

The clock frequency fc is same for all the stages.

Problem

Consider the fifth order ladder filter as shown below:

(a) Find the frequency response by means of simulation (Use Multisim or PSpice).
(b) Design the equivalent fifth order SC ladder Filter
(c) Calculate the values of SC resistors for $f_c = 20$ kHz.


V5
10kΩ
9.91nF
1kΩ
V4
0.81µF
0.81µF
1kΩ
1kΩ
V3
9.91nF
9.91nF
1kΩ
1kΩ
V2
0.81µF
0.81µF
1kΩ
1kΩ
V1
10kΩ
9.91nF
9.91nF
1kΩ
10kΩ
1kΩ
Vin
1 Vpk
1000 Hz
0°

3.7 Conclusions

- Described the realization of Switched Capacitor Resistor and its use in IC technology
- Presented switched capacitor integrators and various switched capacitor building blocks for filter design
- Examples are given to illustrate the concept

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Chapter 4
Pulse Code Modulation (PCM)

Topics

- Introduction to PCM
- Sampling
- Quantization-Linear and Non-Linear
- A/D and D/A Converter
- Bit Rate and Bandwidth

4.1 Introduction to PCM

Pulse Code Modulation (PCM), also known as baseband transmission, converts the input analog signal into digital format and transmits over a digital communication channel. Figure 4.1 shows the basic functional block diagram of a typical PCM system. It Involves:

- Band limiting the input analog signal (See Chaps. 2 and 3)
- Sampling
- Quantization
- A to D conversion
- Signal shaping

Several PCM channels can be multiplexed to forms a single bit stream and transmit over a single digital channel. This is known as time Division Multiplexing (TDM). For example, the classical land telephone system is a TDM system where 24 digital channels are multiplexed to form a single digital channel. Similar multiplexing techniques are also used in modern cellular communication systems. We will discuss this further in this book. This chapter brings readers up-to-date in key concepts and underlying principles of PCM so that they can readily apply it to the industry.

S. Faruque, *Radio Frequency Source Coding Made Easy*, SpringerBriefs
in Electrical and Computer Engineering, DOI 10.1007/978-3-319-15609-5_4

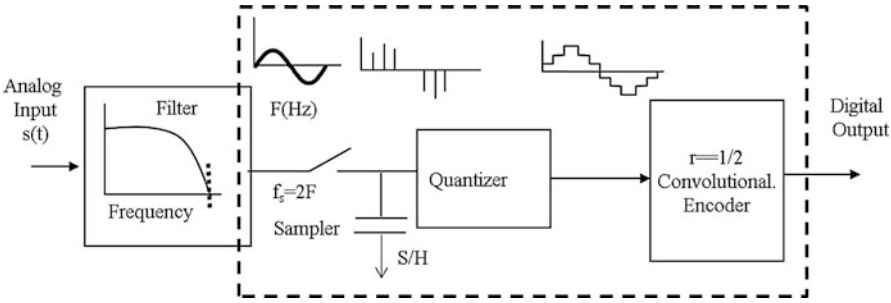


Fig. 4.1 PCM functional block diagram

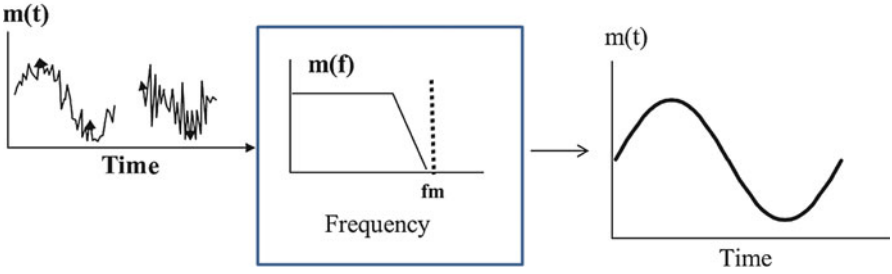


Fig. 4.2 Band-limit filter rejects unwanted signals by means of a lowpass filter and keeps the desired signal. The maximum frequency available for sampling is f_n

4.2 Input Band-Limit Filter

This topic has already been detailed in the preceding chapter. This brief summary is included so that readers may connect it to the topic which follows. As shown in Fig. 4.2, the input analog signal may contain undesired signals along with the desired signal. The transmission bandwidth is also limited. Therefore, we need a lowpass filter to remove the undesired signals. These filters are known as band-limit filters. The output of the lowpass filter is the desired signal, which is band limited for further processing.

Once the desired analog signal is recovered, the next step of the process is sampling. The maximum frequency available for sampling is f_m, which is the output of the band limit filter as shown in the figure. These band limit filters, also known as antialiasing filters, play an important role in sampling, as we shall see in the following section.

4.3 Sampling [1, 2]

In PCM, sampling is the conversion of continuous signal to a sequence of a discrete time signal as shown in Fig. 4.3.

In Fig. 4.3:

- m(t) is the input signal
- S(t) is the sampled output signal, before and after Sample & Hold (S/H)
- $f_s = 1/T_s$ is the sampling frequency
- $T_s = 1/f_s$ is the sample period.

According to Nyquist sampling theorem [1]:

- Nyquist Rate is defined as: $f_s = 2f_m$
- Nyquist Criterion is defined as: $f_s \geq 2f_m$

The sampling frequency or sampling rate, f_s, is the average number of samples obtained in 1 s (samples per second). In this mechanism, the analog signal amplitude is sampled (measured) at regular time intervals. The sampling rate, or number of samples per second, is several times the maximum frequency of the analog waveform in cycles per second. The following problem will show how sampling frequency governs the reconstruction of the analog signal.

Problem 4.1

Given:

- Analog signal frequency $f_m = 1$ kHz

Show the sampled analog signal S(t) for the following sampling frequencies:

- $f_s = 8$ kHz

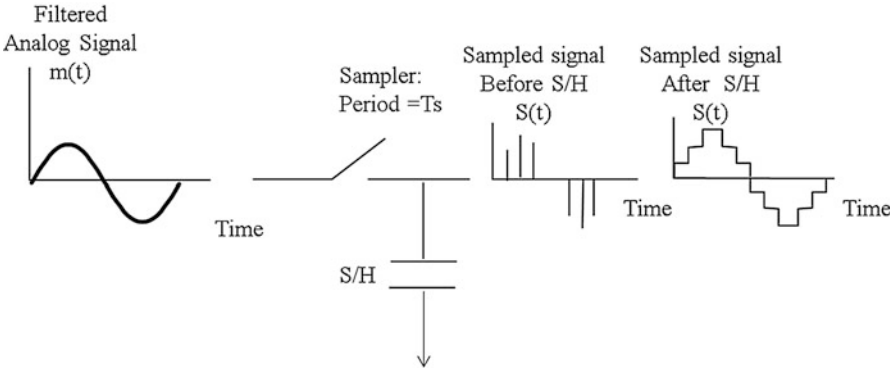


Fig. 4.3 Illustration of sampling. According to Nyquist criterion, the sampling frequency should be greater than twice the input signal frequency to reconstruct the input signal m (t). S(t) is the sampled signal before and after sample and hold (S/H)

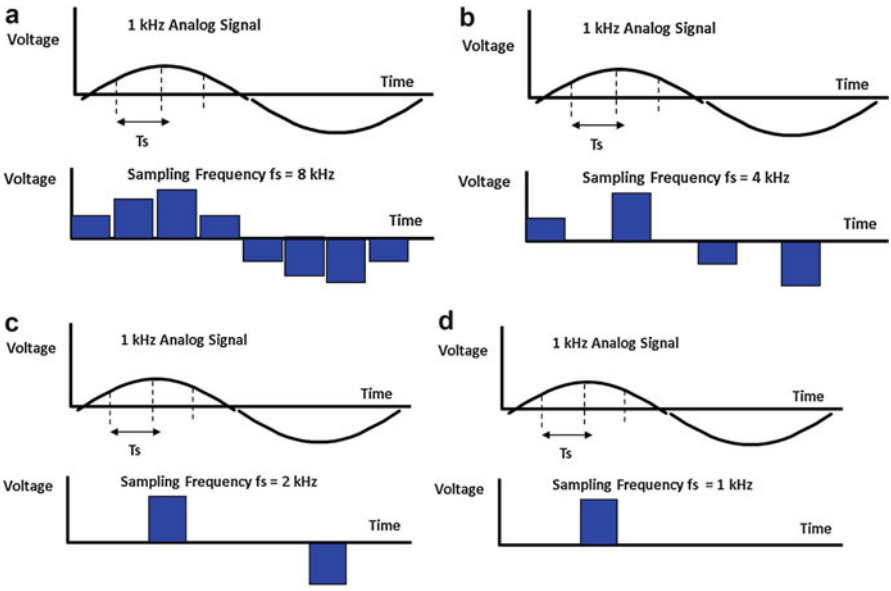


Fig. 4.4 illustration of sampling. A 1 kHz analog signal sampled at different sampling rate

- $f_s = 4$ kHz
- $f_s = 2$ kHz
- $f_s = 1$ kHz

Solution:

(a) fm = 1 kH and fs = 8 kHz. fs/fm = 8/1 = 8. Therefore, there are eight samples to represent the 1 kHz analog signal. See Fig. 4.4a.

(b) fm = 1 kH and fs = 4 kHz. fs/fm = 4/1 = 4. Therefore, there are four samples to represent the 1 kHz analog signal. See Fig. 4.4b.

(c) fm = 1 kH and fs = 2 kHz. fs/fm = 2/1 = 2. Therefore, there are 2 samples to represent the 1 kHz analog signal. See Fig. 4.4c.

(d) fm = 1 kH and fs = 1 kHz. fs/fm = 1/1 = 1. Therefore, there is only 1 sample to represent the 1 kHz analog signal. See Fig. 4.4d. Notice that this signal cannot be recognized as a sinusoidal signal.

4.4 Aliasing

4.4.1 Spectrum of Analog Signals Before Sampling

The effectiveness of sampling is determined by the Nyquist criterion, requiring $f_s \geq 2f_m$. If the sampling rate $f_s < 2f_m$, the fidelity of the signal is reduced, causing

aliasing. Therefore, reconstruction of a continuous signal from samples requires satisfying the Nyquist criterion ($f_s \geq 2f_m$) to avoid aliasing. This topic has been extensively addressed by many authors [3–7]. In this section we will illustrate this with a simple example. Let's consider a set of four time domain analog waveforms ranging from 1 kHz to 4 kHz, in 1 kHz steps, as given below:

- $m_1(t) = Ac\ Sin\ (2\pi 1{,}000t)$
- $m_2(t) = Ac\ Sin\ (2\pi 2{,}000t)$
- $m_3(t) = Ac\ Sin\ (2\pi 3{,}000t)$
- $m_4(t) = Ac\ Sin\ (2\pi 4{,}000t)$

Figure 4.5 shows the respective frequency domain responses separately. The composite response is given in Fig. 4.6 after the band-limit filter, which is also known as anti-aliasing filter. Notice the residual signals beyond 4 kHz, which is limited to f_m. This is because of non-ideal filter characteristics. Without an anti-aliasing filter, frequencies higher than the Nyquist frequency will cause aliasing. We will use this analogy to examine aliasing.

4.4.2 *Spectral Response Due to Nyquist Sampling*

Sampling theorem [1–3] states that, when a band limited analog signal f_m is sampled at the Nyquist rate fs, where $f_s = 2f_m$, it creates spectral components $(f_s \pm f_m)$, $(2f_s \pm f_m)$, . . . as shown in Fig. 4.7 [3]. The occupied bandwidth is 2fm centered around fs, 2fs, ...

4.4.3 *Spectral Response Due to Oversampling ($f_s > 2$ fm)*

When the band limited signal f_m is sampled above the Nyquist rate, where $f_s > 2f_m$, we obtain the spectral response as shown in Fig. 4.8. Notice the occupied bandwidth, which is still $2f_m$ centered around fs, 2fs, ...but shifted. This is because of over sampling, requiring more transmission bandwidth [3]. This is undesirable since it is spectrally inefficient.

4.4.4 *Spectral Response Due to Under Sampling (Aliasing)*

When the band limited signal f_m is sampled below the Nyquist rate, where $f_s < 2f_m$, we obtain the spectral response as shown in Fig. 4.9. Also, notice the occupied bandwidth, which is still $2f_m$ centered around fs, 2 fs, ...but overlapped. This is because of under-sampling, causing aliasing [3]. This is also undesirable, since it causes distortion.

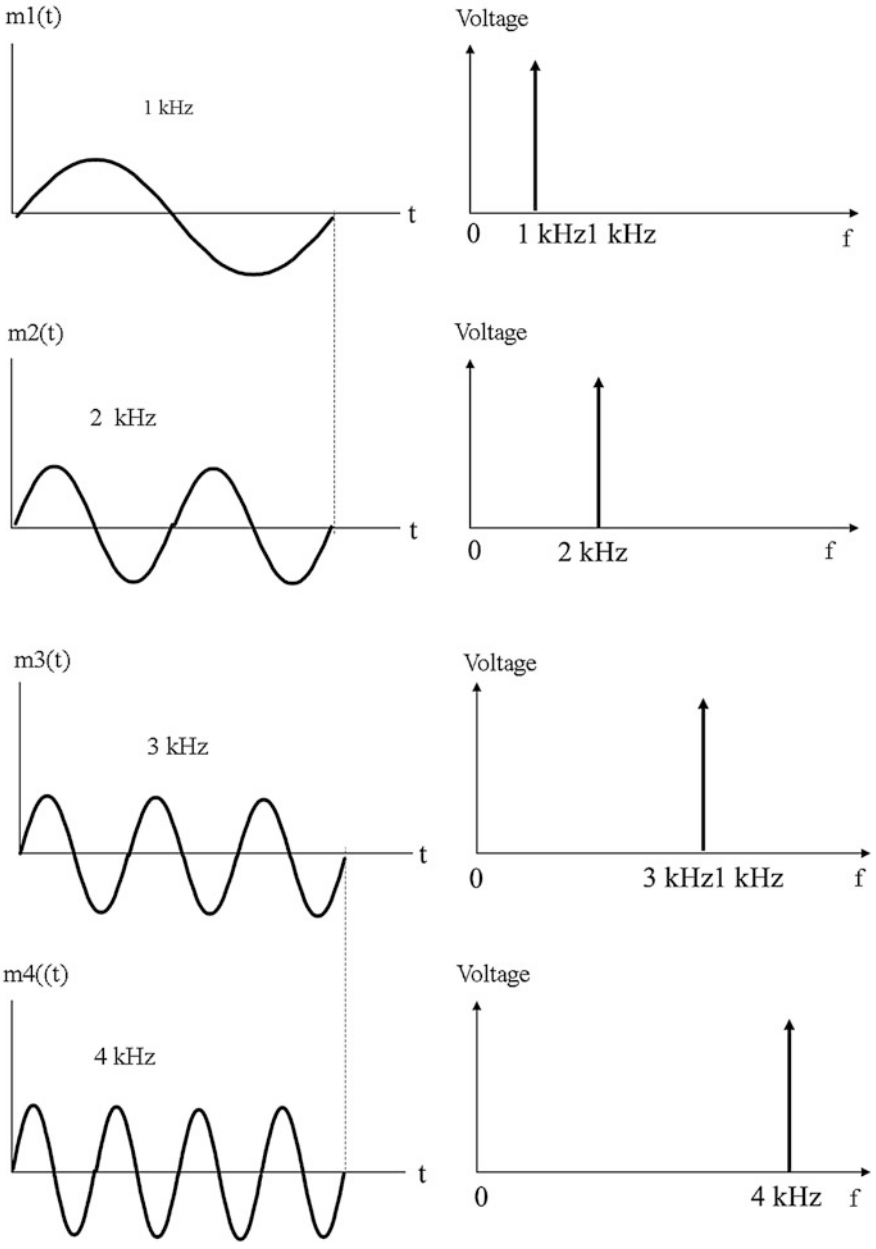


Fig. 4.5 Time domain analog signals and the corresponding frequency domain representation

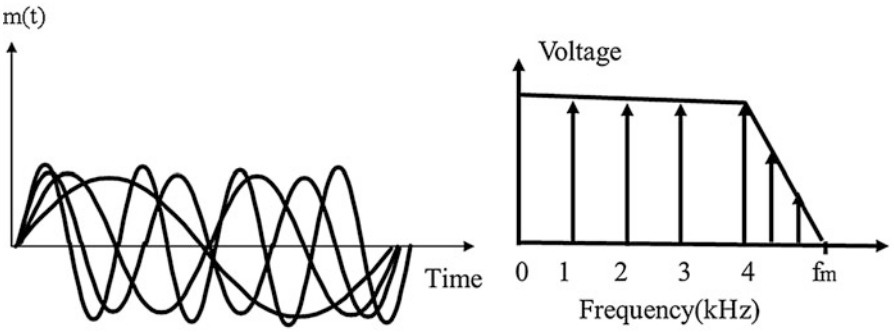


Fig. 4.6 The Composite spectral response after band-limit filter

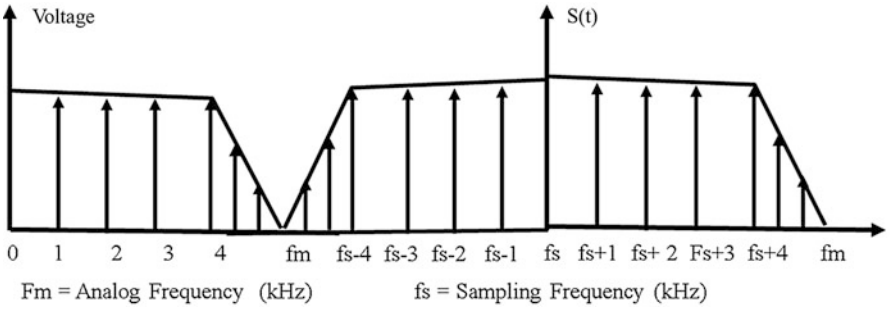


Fig. 4.7 Spectral response due to sampling at the Nyquist rate $fs = 2f_m$

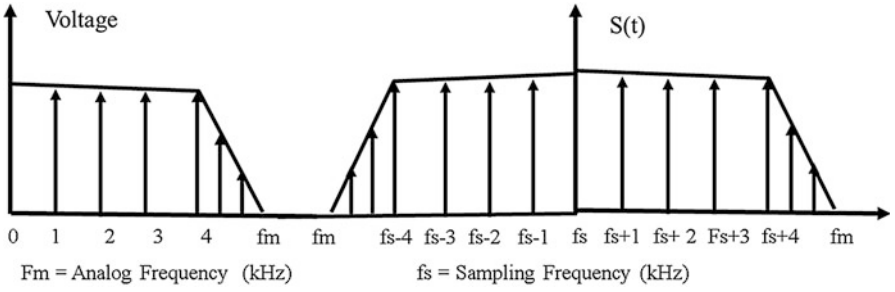


Fig. 4.8 Spectral response due to over sampling, $fs > 2f_m$

Problem 4.2

Given:

- Single tone analog frequency $fm = 1$ kHz
- Sampling frequency $fs = 8$ kHz

Find:

(a) Number of sample cycle of the analog frequency
(b) The occupied bandwidth

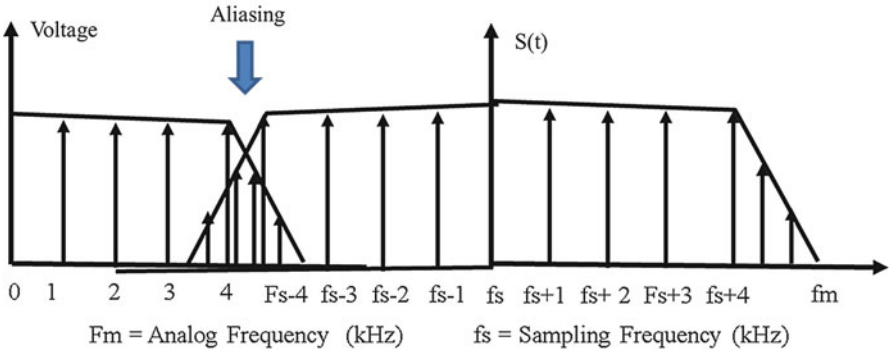


Fig. 4.9 Spectral response due to under sampling, $fs < 2f_m$ (Aliasing)

Solution:

(a) Analog frequency fm = 1 kHz, Sampling frequency fs = 8 kHz. Therefore the number of samples per cycle of the analog frequency is 8.
(b) Occupied Bandwidth = 2 fm = 2 × 1 kHz = 2 kHz, which is centered around 8 kHz.

4.5 Quantization

The instantaneous amplitude of the analog signal at each sampling is rounded off to the nearest of several specific, predetermined levels. This process is called quantization [8–12]. There are linear quantization and non-linear quantization. These are briefly presented below:

4.5.1 Linear Quantization

Quantization is a process that converts the sampled value into discrete steps. If all steps are equal, then it is a linear quantizer as shown in Fig. 4.10.

The quantization step is determined as follows:

If the input voltage is bounded by ±V, then the quantization step size q will be given by:

$$q = 2V/N \tag{4.1}$$

where

N = Number of quantization levels
V = Input voltage

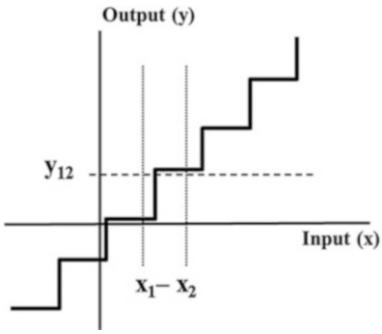


Fig. 4.10 Illustration of linear quantization

Therefore, the number of binary digits that can be represented, will be given by the following equation:

$$N = 2^n \tag{4.2}$$

Where

$$n = \text{Number of binary digits}(1, 2, \ldots)$$

4.5.2 *Drawback of Linear Quantization*

In Fig. 4.10, If the input voltage is between 0.5 and 1 V, then Output = 1 V. This is to say that:

- y = 0 V if 0 V < x < 0.5 V
- y = 1 V if 0.5 V < x < 1 V

All samples will fall into a particular quantization interval. This will cause Quantization error, depending on the interval. Quantization error is high when the input voltage is low. Quantization error is low when the input voltage is high. Let's examine these by means of the following examples:

Example 1

- x = 0.1 to 0.2
- Step Size = 0.1 V
- y = 0.2 (two steps)
- Error = 0.1/0.2 = 0.5 (50 %)

Example 2

- x = 0.9 to 1
- Step Size 0.1 V
- y = 1
- Error = 0.1/1 = 0.1 (10 %)

Therefore the error is non-Uniform, which is not good.

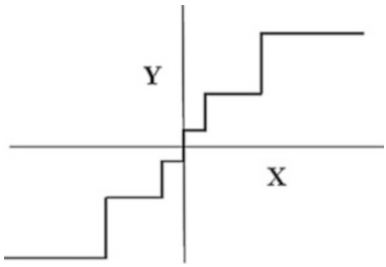


Fig. 4.11 Illustration of non-linear quantization

4.6 Non-linear Quantization

A non-linear quantizer, shown in Fig. 4.11, uses:

- Small steps for low input voltages and
- Large steps for large input voltages

Example 1

- x = 0.1 to 0.11
- Step Size 0.01 V
- y = 0.2
- Error = 0.01/0.2 = 0.05 (5 %)

Example 2

- x = 0.95 to 1
- Step Size 0.05 V
- y = 1
- Error = 0.05/1 = 0.05 (5 %)

Thus, the quantization error is the same in both cases, which is good.

4.7 Companding

Companding is a process of compression and expansion of signals amplitudes. In telecommunications, the signal to be transmitted is compressed before transmission and expanded at the receiver to recover the original signal [13–16]. See Fig. 4.12.

Companding allows signals with a large dynamic range over a channel having small dynamic range capabilities. Non-uniform quantization can be achieved by first compressing the samples of the input signal and then expanding at the receiver. One such method commonly used in PCM is called "Logarithmic Companding". It is also known as μ-Law, which is given by the following formula [8]:

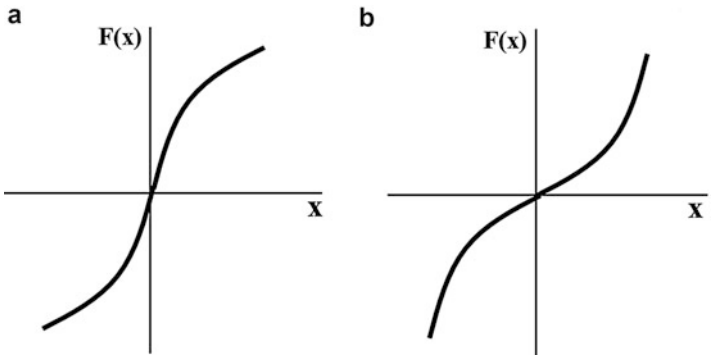


Fig. 4.12 Illustration of (**a**) Logarithmic compression and (**b**) logarithmic expansion

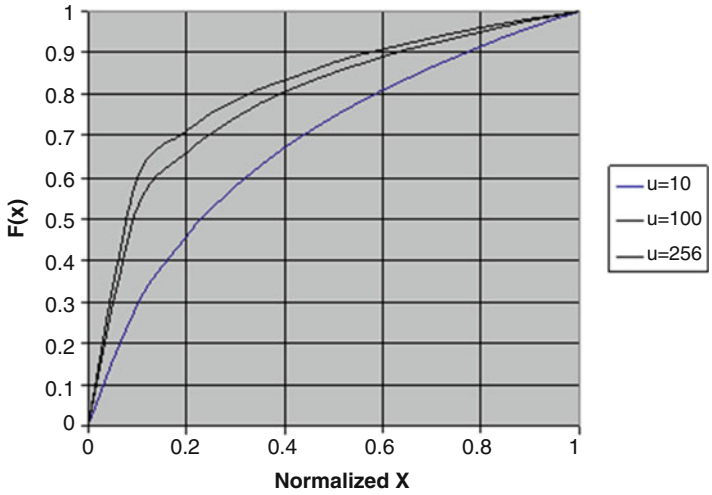


Fig. 4.13 Illustration of logarithmic companding known as μ-law

$$F(x) = \frac{\ln(1+\mu x)}{\ln(1+\mu)} \tag{4.3}$$

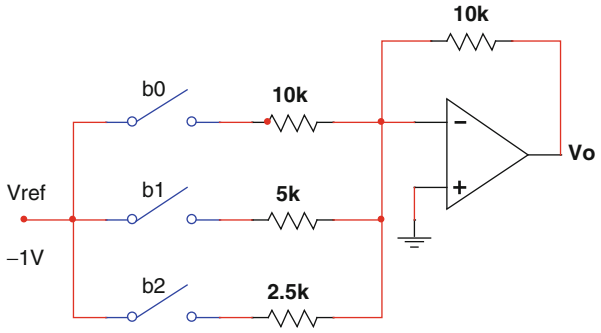
Where

- F(x) = Output quantized level
- x = Input voltage steps
- μ = 0 to 255(Quantization levels)

For μ = 0, it is linear (no companding) and for μ > 0, it is non-linear. Figure 4.13 shows the output quantized level F(xxxx) as a function of input voltage steps x for several values of μ.

4.8 Digital to Analog Converter

A digital to analog converter (A/D) converter is essentially a summing amplifier where the voltage gains are binary weighted [9]. In order to understand this, let's consider the inverting amplifier as shown in Fig. 4.14. The output voltage of this amplifier is given by,



$$V_0 = -V_1(R_2/R_1) = A_v V_1 \tag{4.4}$$

Where,

$A_v = R2/R1$ is the voltage gain.

Next, consider the summing amplifier as shown in Fig. 4.15. The output voltage of this amplifier is given by,

$$\begin{aligned} V_0 &= -V_{ref}\left[((R_2/R_1) + 2(R_2/R_1) + 4(R_2/R_1) + 8(R_2/R_1)\right. \\ &= -V_{ref}A_v[1 + 2 + 4 + 8] \end{aligned} \tag{4.5}$$

For a given reference voltage Vref and R2/R1 ratio, the output voltage Vo is binary weighted. Therefore, we can select a set of binary numbers to generate a desired analog output voltage. The desired binary number can be selected by controlling the binary weighted resistors as shown in Fig. 4.16, which is a 4-bit D/a converter.

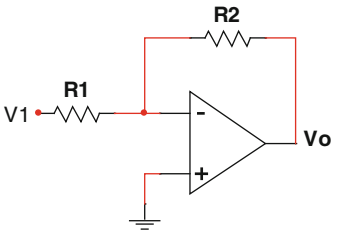


Fig. 4.14 Inverting amplifier

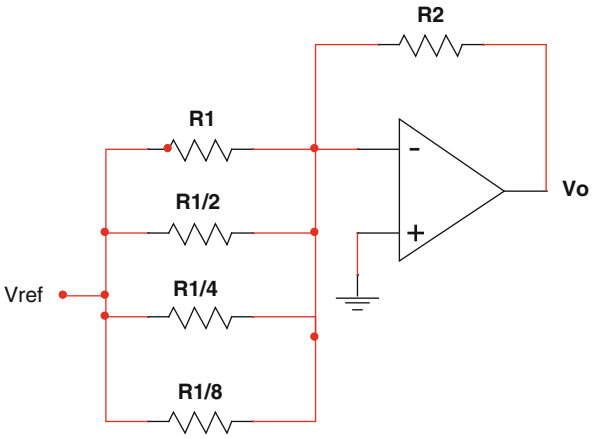


Fig. 4.15 Summing amplifier

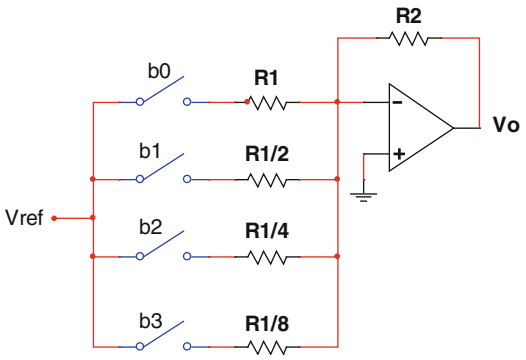


Fig. 4.16 4-bit D/A converter

In Fig. 4.16, each binary weighted resistor can be selected independently by closing the corresponding switches. This is a 4-bit D/A converter, where bo, b1, b2 and b3 are the bit values. The operation of the switches is as follows:

- When the bit value is 0, the switch is open, the corresponding resistor is out and it does not play any role in the voltage gain.
- When the bit value is 1, the switch is closed and the corresponding resistor is connected to the circuit to play a role in the voltage gain.

Therefore, the output voltage of the D/A converter can be written as follows:

$$V_0 = -V_{ref}\, A_v[b_0 + 2b_1 + 4b_2 + 8b_3] \tag{4.6}$$

Where,

- $b_0 = 0$ or 1
- $b_1 = 0$ or 1
- $b_2 = 0$ or 1
- $B_3 = 0$ or 1

Problem 4.3

Given:

- $V_{ref} = -1$ V
- $A_v = 1$

(a) Design a 3-bit D/A converter.
(b) Calculate the analog voltage and the corresponding digital input.

Solution:

(a) With $Vr_{ef} -1$ V and $A_v = 1$, the 3-bit D/A converter appears as follows:
(b) The output voltage for a 3-bit D/A converter is given by,

$$\begin{aligned} V_0 &= -V_{ref}(R_2/R_1)\,[b_0 + 2b_1 + 4b_2] \text{ Volts} \\ &= [b_0 + 2b_1 + 2b_2] \text{ Volts} \end{aligned}$$

Table 4.1 shows the analog output corresponding to input digital data.

4.9 Analog to Digital Converter

Analog to digital Converter (ADC) converts the quantized voltage into a bit pattern, typically 8-bit A/D converter. Figure 4.17 shows the basic block diagram of an n-bit analog to digital (A/D) converter [9]. It comprises:

- A voltage comparator
- An up-down counter and
- A D to A converter

The operation of the circuit is briefly presented below:

Table 4.1 Output voltage as a function of input data

$b_2\ b_1\ b_0$	$V0 = [b_0 + 2b_1 + 4b_2]$ volts
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7

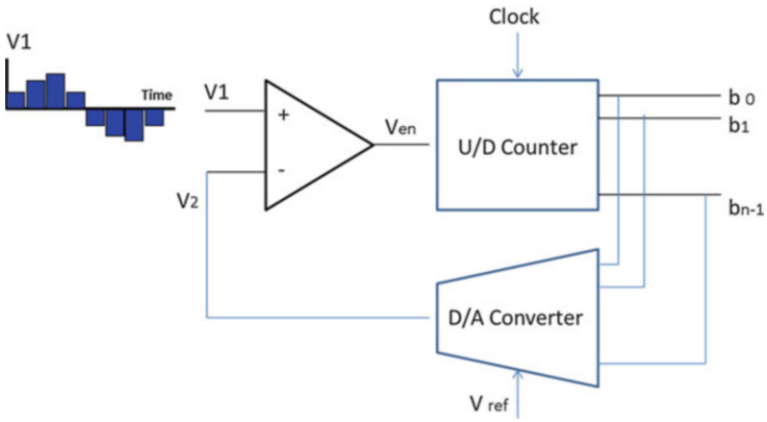


Fig. 4.17 Block diagram of A to D converter

4.9.1 Function of the Comparator

The analog comparator compares V1 and V2 and generates the output voltage Ven where,

$$V_{en} = A(V1 - V2) \tag{4.7}$$

Where,

- A = Open loop voltage gain
- V1 = The quantized input voltage
- V2 = Output voltage of the D/A converter
- V_{en} = Output voltage of the comparator that enables the UP/Down counter to count up or down.

  This is governed by the following logic:

- If V1 > V2, then Ven=1, Count up
- If V1 < V2, then Ven = −1, Count down
- If V1 = V2, then Ven = 0: Stop counting

4.9.2 Function of the Up/Down Counter

The function of the up/down counter is to count up or down, based on the input voltage Ven. This is governed by the following logic:

- If Ven = 1, Count up
- If Ven = −1, Count down

- If Ven = 0: Stop counting

Initially, the output of the counter is all zeros. Therefore, for an n-bit up/down counter, there are n bits: b_o, b_1, . ., b_{n-1}, as shown in Fig. 4.17. The counting rate is governed by the clock.

4.9.3 Function of the D/A Converter

The construction of D/A converter was presented earlier in Sect. 4.8. We will now examine its function within an A/D converter as shown in Fig. 4.17. Here, the D/A converter uses the n-bit digital signal from the output of the A/D converter to generate an analog signal V2, which is given by,

$$V_2 = V_{ref} A_v \left[b_0 + 2b_1 + \ldots + 2^{N-1} b_{N-1}\right] \tag{4.8}$$

Where,

- V_2 = Analog voltage at the output of the D/A converter
- V_{ref} = reference voltage
- Av = Voltage gain
- b_0 = 0 or 1
- b_1 = 0 or 1

  :
  :

- b_{N-1} = 0 or 1

Therefore, for an 8-bit D/A converter, there are:

- $2^8 = 256$ voltage levels
- $2^8 - 1 = 255$ Voltage steps (0 to 255)

These voltage steps are available from the output of the D/A converter. Upon receiving V_2, the comparator compares these voltages with the input voltage V1 and generates V_{en} to control the U/D counter.

4.9.4 Overall Function of the A/D-D/A Converter

We will now describe the overall function of the A/D-D/A converter as shown in Fig. 4.18. It has the following design parameters:

- V_1 = 0 V, 1 V, 2 V and 3 V
- 2 bit A/D-D/A converter

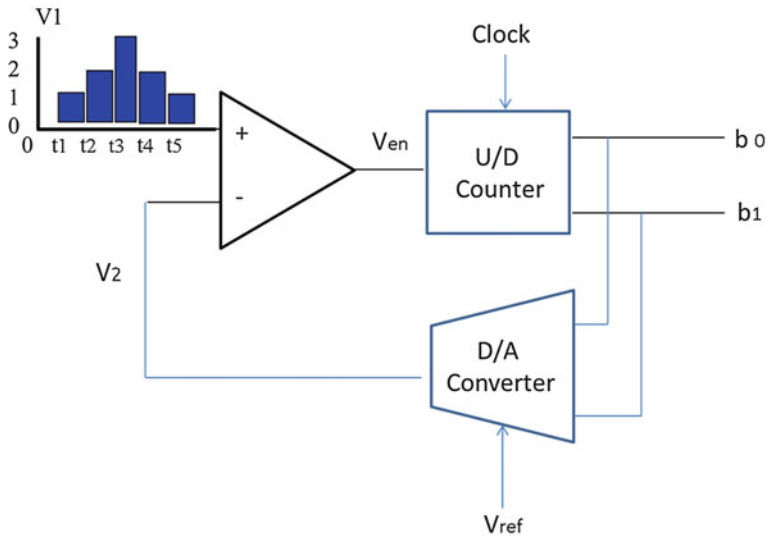


Fig. 4.18 Block diagram of a 2-bit A/D converter

- $V_{ref} = 1$ V
- $A_v = 1$

The 2 bit A/D converter, shown in Fig. 4.18 can be described as,

$$V_2 = V_{ref} A_v [b_0 + 2b_1] = b_o + 2b_1 \tag{4.9}$$

Table below shows the analog voltage corresponding to the 2-bit digital input.

b_1	b_2	V_2
0	0	0
0	1	1
1	0	2
1	1	3

ANALYSIS
Initial state:
At t = 0: Let $V_1 = 0$ V
Then,

- Analog Input: $V_1 = 0$ V (Positive Input of the comparator)
- Digital Output: $b_1 = 0$ and $b_0 = 0$ (U/D counter output)
- D/A Input: 0 0 (This is also the output of the counter)
- D/A Output: $V_2 = b_o + 2b_1 = 0 + 0 = 0$ V (Negative input of the comparator)
- Therefore, $V_2 = V_1 = 0$ V
- Comparator Output is: $V_{en} = 0$
- Counter output is = 0 0 (this is the digital signal)

Therefore, when the input analog voltage $V_1 = 0$ V, The digital output is 0 0.
At t = 1: Let $V_1 =$ rises to 1 V while V_2 is still at 0 V.
Then,

- $V_1 = 1$ V and $V_2 = 0$ (because of propagation delay)
- Therefore, $V_1 > V_2$
- The comparator output is: $V_{en} = 1$
- The counter counts up: $b_1 = 0$ and $b_0 = 1$ (Digital output = 0 1)
- D/A input is 0 1
- D/A output becomes: $V_2 = b_o + 2b_1 = 1 + 0 = 1$ V (After a delay)
- Comparator input (At the negative port) is: $V_2 = 1$ V
- Since $V_2 = V_1$, $V_{en} = 0$: Stop counting
- Digital output stays at 0 1

Therefore, when the input analog voltage $V_1 = 1$ V, the digital output is 0 1.
At t_2: Let V_1 rises to 2 V while V_2 is still at 1 V:
Then,

- $V_1 = 2$ V and $V_2 = 1$ (because of propagation delay)
- Therefore, $V_1 > V_2$
- The comparator output is: $V_{en} = 1$
- The counter counts up: $b_1 = 1$ and $b_0 = 0$ (Digital output = 1 0)
- D/A input is 1 0
- D/A output becomes: $V_2 = b_o + 2b_1 = 0 + 2 = 2$ V (After a delay)
- Comparator input (At the negative port) is: $V_2 = 2$ V
- Since $V_2 = V_1$, $V_{en} = 0$: Stop counting
- Digital output stays at 1 0

Therefore, when the input analog voltage $V_1 = 2$ V, the digital output is 1 0.
At t3: Let V_1 rises to 3 V while V_2 is still at 2 V:
Then,

- $V_1 = 3$ V and $V_2 = 2$ (because of propagation delay)
- Therefore, $V_1 > V_2$
- The comparator output is: $V_{en} = 1$
- The counter counts up: $b_1 = 1$ and $b_0 = 1$ (Digital output = 1 1)
- D/A input is 1 1
- D/A output becomes: $V_2 = b_o + 2b_1 = 1 + 2 = 3$ V (After a delay)
- Comparator input (At the negative port) is: $V_2 = 3$ V
- Since $V_2 = V_1$, $V_{en} = 0$: Stop counting
- Digital output stays at 1 1

Therefore, when the input analog voltage $V_1 = 3$ V, the digital output is 1 1.
At t4: Let V_1 reduces to 2 V while V_2 is still at 3 V:
Then,

- $V_1 = 2$ V and $V_2 = 3$ (because of propagation delay)
- Therefore, $V_1 < V_2$

- The comparator output is negative: $V_{en} = -1$
- The counter counts Down: $b_1 = 1$ and $b_0 = 0$ (Digital output = 1 0)
- D/A input is 1 0
- D/A output becomes: $V_2 = b_o + 2b_1 = 0 + 2 = 2$ V (After a delay)
- Comparator input (At the negative port) is: $V_2 = 2$ V
- Since $V_2 = V_1$, $V_{en} = 0$: Stop counting
- Digital output stays at 10

Therefore, when the input analog voltage $V_1 = 2$ V, the digital output is 1 0.
At t5: Let V_1 reduces to 1 V while V_2 is still at 2 V:
Then,

- $V_1 = 1$ V and $V_2 = 2$ (because of propagation delay)
- Therefore, $V_1 < V_2$
- The comparator output is negative: $V_{en} = -1$
- The counter counts Down: $b_1 = 0$ and $b_0 = 1$ (Digital output = 0 1)
- D/A input is 0 1
- D/A output becomes: $V_2 = b_o + 2b_1 = 1 + 0 = 1$ V (After a delay)
- Comparator input (At the negative port) is: $V_2 = 1$ V
- Since $V_2 = V_1$, $V_{en} = 0$: Stop counting
- Digital output stays at 0 1

Therefore, when the input analog voltage $V_1 = 1$ V, the digital output is 0 1.
At t6: Let V_1 reduces to 0 V while V_2 is still at 1 V:
Then,

- $V_1 = 0$ V and $V_2 = 1$ (because of propagation delay)
- Therefore, $V_1 < V_2$
- The comparator output is negative: $V_{en} = -1$
- The counter counts Down: $b_1 = 0$ and $b_0 = 0$ (Digital output = 0 0)
- D/A input is 0 0
- D/A output becomes: $V_2 = b_o + 2b_1 = 0 + 0 = 0$ V (After a delay)
- Comparator input (At the negative port) is: $V_2 = 0$ V
- Since $V_2 = V_1$, $V_{en} = 0$: Stop counting
- Digital output stays at 0 0

Therefore, when the input analog voltage $V_1 = 0$ V, the digital output is 0 0.
This is the original state of the A/D-D/A converter.

4.10 Resolution

The resolution is determined by the number of voltage steps needed to reach the maximum input voltage V_1 (max) using an n-bit A/D converter. Let's take a closer look:

- For example, in a 2-bit A/D-D/A converter, there are $2^2 = 4$ levels (0–3). This is to say that there are $2^2–1 = 3$ steps. Therefore, if V1 (max) = 3 V, the number of steps needed to reach 3 V will be $3/(2^2–1) = 1$ V per step.
- Similarly, in a 3-bit A/D-D/A converter, there are $2^3 = 8$ levels (0–7). This is to say that there are $2^3–1 = 7$ steps. Therefore, if V1 (max) = 3 V, the number of steps needed to reach 3 V will be $3/(2^3–1) = 3/7$ V per step.
- Likewise, In an 8-bit A/D-D/A converter, there are $2^8 = 256$ levels (0–255). This is to say that there ar or $2^8–1 = 255$ steps. Therefore, if V1 (max) = 3 V, the number of steps needed to reach 3 V will be $3/(2^8–1) = 3/255$ V per step.

From the above examples we see that the step size decreases rapidly as the number of bits increases. This step size is known as resolution. In general, the resolution is defined as,

$$R = \frac{V_1(\max)}{2^n - 1}$$

Where, n is the number of bits.

Exercise 1

(a) Design an 8-Bit D/A converter with the following specifications:

- V_2 (max) = 10 V
- Vref = 1 V
- $A_v = 1$

(b) Estimate the resolution

Exercise 2

(a) Consider the previous exercise again and design an 8-Bit A/D converter.
(b) Estimate the resolution.

4.11 Binary Line Coding and Power Spectrum

The A/D output is a digital signal represented by a Binary 1 or a Binary 0. Before these binary signals can be used, they are generally conditioned (converted into different formats) before transmission. The process of formatting is called “Binary Line Coding” [17]. Commonly used binary codes are:

- Non-return to Zero (NRZ)
- Return to Zero (RZ)

- Unipolar
- Bipolar
- Manchester

Etc.
We will consider some popular line coding, and evaluate their power spectrum.

4.11.1 Popular Binary Signaling Formats

Figure 4.19 shows the popular binary signals along with the clock. Here,

- Clock is a periodic waveform.
- Data is synchronized with the clock.
- NRZ data takes the full period of the clock. It does not return to zero along with the clock. Its power spectrum is narrower than the clock.
- RZ data takes half the period of the clock. It returns to zero along with the clock. Its power spectrum is wider than the NRZ data.

This brings us to a well-known topic known as "Fourier Transform", which can be used to determine the power spectrum associated with digital signals [xxx]. As shown in Fig. 4.19, NRZ data has a period T. Therefore, the Fourier transform will be as follows:

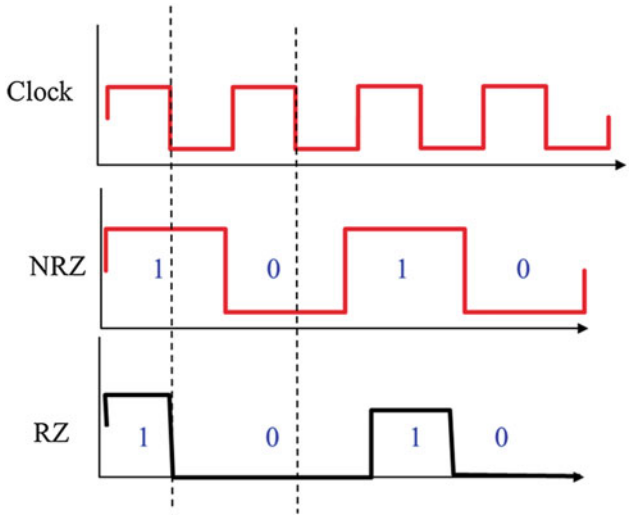


Fig. 4.19 Popular binary signals and the clock

$$V(\omega) = \int_0^T V(t) \cdot e^{-j\omega t} dt \tag{4.10}$$

$$P(\omega) = V^2 T \left[\frac{Sin\,(\omega T/2)}{\omega T/2} \right]^2 \tag{4.11}$$

Where,

- V(t) is the time domain signal of the NRZ data
- V(ω) is the frequency domain expression of the NRZ data
- P(ω) is the power spectral density associated with the NRZ data

On the other hand, RZ data has a period T/2. Therefore, the Fourier transform equation will be

$$V(\omega) = \int_0^{T/2} V(t) \cdot e^{-j\omega t} dt \tag{4.12}$$

$$P(\omega) = V^2 T \left[\frac{Sin\,(\omega T/4)}{\omega T/4} \right]^2 \tag{4.13}$$

Where,

- V(t) is the time domain signal of the RZ data
- V(ω) is the frequency domain expression of the RZ data
- P(ω) is the power spectral density associated with the RZ data

Figure 4.20 shows the power spectral densities of NRZ and RZ data, where P (w) is plotted as a function fb/fc with $T = 1/f_c = 1$. Notice that the first null for NRZ

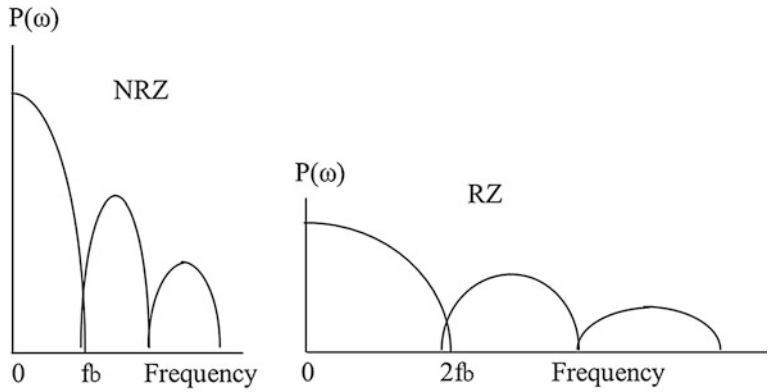


Fig. 4.20 One sided power spectrum of NRZ and RZ data. The first null at f_b/f_c ($T = 1/f_c = 1$) determines the bandwidth. Note: $f_c = 1/T$ is constant and fb is variable

data is at f_b ($f_b = 1/T$) and RZ data is at $_{2fb}$ (Period = T/2). Therefore, NRZ data is spectrally efficient. For this reason, NRZ data is more popular in wireless communication.

4.12 Bit Rate

In A/D converter, the analog signal is sampled, quantized and converted into bit streams by means of an n-bit A/D converter. Figure 4.21 shows a simplified version to illustrate this.

The bit rate depends on:

- Sampling rate fs and
- Number of bits per sample (depends on A/D-D/A converter)

Therefore, the bit rate will be given by,

$$R_b = nf_s \tag{4.14}$$

Where,

- R_b = Bit rate in bits per second
- fs = Sampling frequency in cycle per second (Hz)
- n = Number of bits per sample

For example, a 1 kHz analog signal, sampled at fs = 8 kHz, will generate eight samples per cycle of this analog signal. Therefore the bit rate will be Rb = 8 × 8 = 64 kb/s.

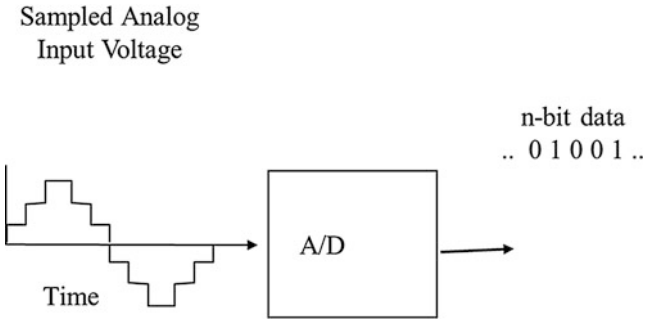


Fig. 4.21 Illustration of PCM bit rate

4.13 Bandwidth

We know from the Fourier Transform, and subsequently from NRZ and RZ data, that the spectrum depends on the data type (NRZ, RZ, Bipolar, Manchester etc.). After performing the one sided Fourier transform, we have noticed that the bandwidth is primarily determined by the first "Null" of the Fourier Spectrum.

The total bandwidth associated with the data will be due to the two-sided bandwidth, i.e., from first null first null, which is governed by the following Fourier integral:

$$V(\omega) = \int_{-T}^{T} V(t) \cdot e^{-j\omega t} dt \tag{4.15}$$

Figure 4.22 shows the corresponding two-sided spectral response. The total bandwidth is given by the main lobe, determined by first null to first null, as shown in the figure. In practical realization, the side lobes are filtered out, since they are small.

The bandwidth depends on:

- Bit rate in cycles per second (Hz)
- Two sided power spectral density and
- Signal formats: NRZ, RZ, ...

Therefore, the bandwidth can be written as,

$$BW = 2R_b = 2nf_s \tag{4.16}$$

For example, if the 64 kb/s data in the previous example is converted into NRZ data, the bandwidth will be $2\text{Rb} = 2 \times 64$ kb/s $= 128$ kHz. Note that the higher order spectral components are filtered out.

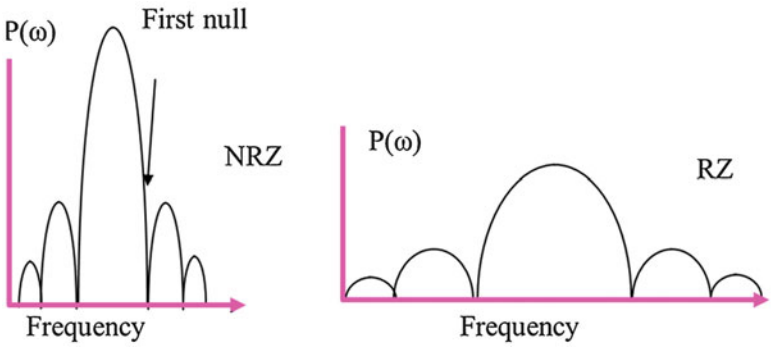


Fig. 4.22 Bandwidth is determined by the main lobe, which is from the 1st null to 1st null. Side lobes are filtered out since they are small

Problem 4.5

Given:

- $fm = 1$ kHz
- $f_s = 8$ kHz (sampling rate)
- $n = 8$ bit/sample
- NRZ data

Find:

(a) Bit Rate
(b) Bandwidth

Solution:

(a) $R_b = nf_s = 8 \times 8 = 64$ kb/s
(b) $BW = 2R_b = 2 \times 64$ kb/s $= 128$ kHz

4.14 Conclusions

- We have presented a brief overview of PCM.
- Various PCM functional blocks such as Sampling, Linear and non-linear quantization, A/D and D/A converters etc. were presented with examples.
- Method of estimating bit rate and bandwidth were presented.

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Chapter 5
Time Division Multiplexing (TDM)

Topics

- Introduction
- TDM Structure
- TDM Frame and Frame Hierarchy
- Frame Synchronization
- North American TDM Standard for Land Telephone System
- The T1(DS1) System
- TDMA for Wireless Communications
- TDMA Frame and Frame Hierarchy
- TDMA BER Performance Analysis

5.1 Introduction

Time-division multiplexing (TDM) is a method of transmitting and receiving k independent signals over a single transmission channel [1–3]. Figure 5.1 provides a simplified block diagram to illustrate the concept. In this scheme, the TDM at the transmit side is known as multiplexer and the TDM at the receive side is known as de-Multiplexer. The TDM at the transmit side assigns k-channels in pre-assigned time slots, where k-time slots constitute a frame. Frame synchronization bits are inserted to identify the "Start' and Stop" of the frame. The synchronization bit pattern is unique and used for frame synchronization. The TDM at the receive side, known as the de-multiplexer, separates the incoming composite signal into k parallel streams as shown in the figure. Both multiplexer and de-multiplexer are synchronized by a common clock to receive data in accordance with the transmit sequence.

The limitation in TDM scheme is that, when one signal occupies the channel, other signals are idle. Therefore there is a delay in TDM system. As a result, the

S. Faruque, *Radio Frequency Source Coding Made Easy*, SpringerBriefs
in Electrical and Computer Engineering, DOI 10.1007/978-3-319-15609-5_5

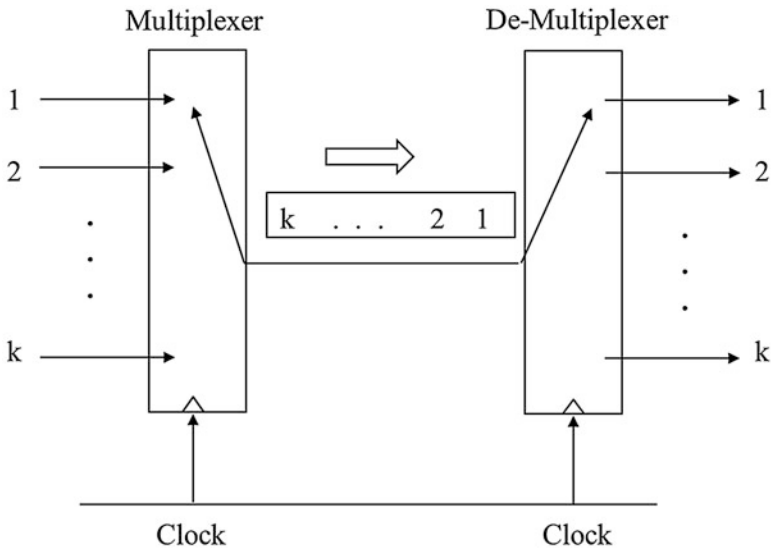


Fig. 5.1 Time division multiplexing. K data streams are time shared in a single transmission channel, one at a time. Switches are controlled at both ends synchronously by means of a clock. Data is formatted in a frame. Synchronization bits are inserted to synchronize the frame

number of signals that can be time shared is limited. Another limitation is the channel bandwidth. For example, ten parallel data streams, having 10 k b/s data stream each, will produce a 100 k b/s data stream after multiplexing, requiring a wider transmission bandwidth.

Applications include:

- North American digital telephony, where 24 channels are time shared, one at a time [1].
- European digital telephony, where 32 channels are time shared, one at a time [1].

We will revisit this topic in more details in this chapter.

Problem 5.1

Given:

- North American PCM System
- 24 users multiplexed to form a single composite bit stream
- Frame length = 125 μs (micro second)
- Each user generates 64 kb/s data

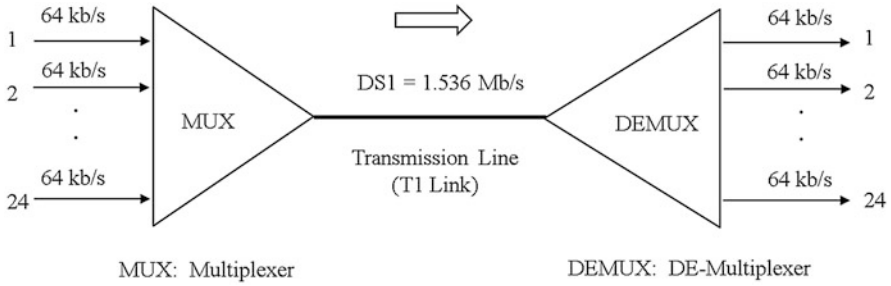
(a) Calculate the composite bit rate after multiplexing
(b) Show the multiplexing and de-multiplexing scheme

Solution:

(a) Total Bit Rate after Multiplexing:

- The total bit rate after multiplexing = 24 × 64 k = 1.536 Mb/s.
- This is known as: "Digital Signal-1 or DS1".
- When the DS1 signal (1.536 MHz) is transmitted through a transmission line, the transmission line is known as "T1 link". See figure below:

(b) Multiplexing and De-Multiplexing Scheme:



With the advent of cellular technology [4–6], the TDM system was further extended to support multiple users in the wireless domain known as TDMA (Time Division Multiple Access). Figure 5.2 shows the basic concept used in wireless communications. In this scheme, the radio transmitter combines data from several users according to the TDM protocol and transmits one at a time in a cyclic fashion. The receiver recovers the clock for synchronization and delivers the data to the respective recipient one at a time. Applications include:

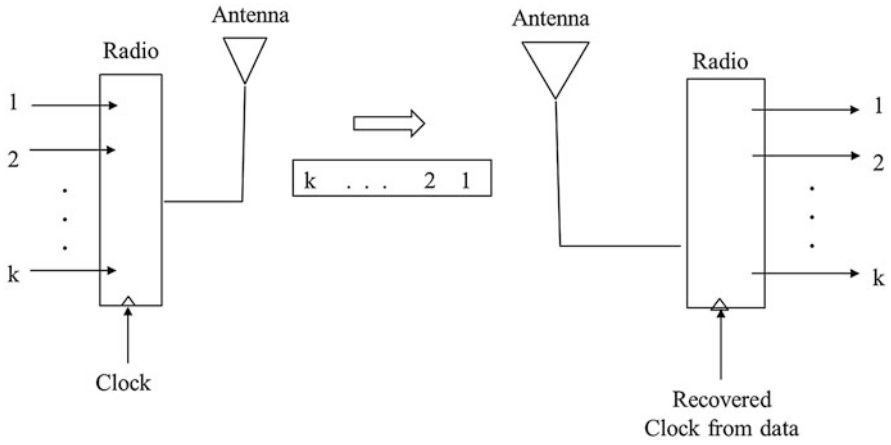


Fig. 5.2 TDMA concept for wireless communications. At the transmitter, k users are time shared and transmitted by a radio, one at a time. At the receiver, the clock is recovered from the received data for synchronization

- North American second generation (2G) cellular telephony. In this scheme, each 30 kHz RF (Radio Frequency) channel is time shared by three users, one at a time, in a cyclic fashion [4–6].
- GSM cellular system, where eight users can time share a 200 kHz RF channel one at a time in a cyclic fashion [7–10].

We will revisit this topic later in more details in this chapter.

5.2 North American TDM in Digital Telephony

5.2.1 The Basic TDM Structure

The North American TDM [1–3] for digital telephony is a hierarchical system which supports 24 PCM channels per frame as shown in Fig. 5.3, where each PCM is a 64 kb/s channel.

At the transmit side (Multiplexing):

- 24-channels are interleaved in preassigned time slots
- 24-channels form a frame
- Frame bits are inserted to identify the "Start' and Stop" of the frame
- These frame bit pattern is unique and used for frame synchronization. (a topic yet to be discussed)
- The frame length = 125 μs (ITU Standard)
- Each frame contains 24 channels
- Each channel is also called DS-0 (Digital Signal-0)
- DS-0 Rate = 64 kbps
- Each DS-0 channel has 8-bits
- 1 Sync bit is added at the end
- Total Number of bits/Frame = (8 × 24) + 1 = 193 bits
- Bit rate = 193/125 μs = 1.544 Mb/s

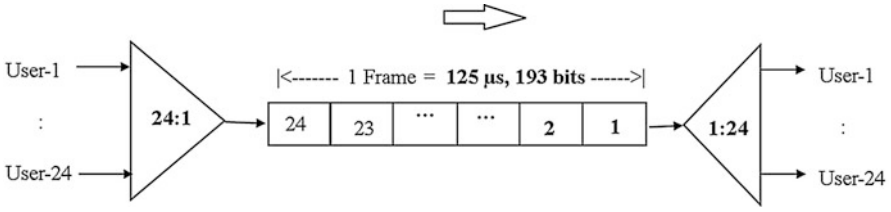


Fig. 5.3 The North American TDM system for digital telephone system. 24 PCM channels form a 125 μs frame

At the receive side (DE multiplexing):

- The De-multiplexer receives successive frames
- Each frame has a "header frame bit pattern" which is unique
- The De-multiplexer synchronizes with the frame bit pattern and recovers all the channels and puts them in the right order

There are two types of frame structure:

- Distributed, where Frame synchronization bits are inserted one at a time at the beginning or at the end of the frame. Each frame contains data + 1 frame-bit.
- Bunched, where All the frame sync. bits are inserted in one time slot.

Both Distributed and Bunched structure have advantages and disadvantages.

5.2.2 *Distributed Frame Structure*

A distributed frame is constructed by distributing 12 sync bits among 12 frames, 1 sync bit per frame. This is shown in Fig. 5.4. In this scheme, the distributed frame structure is specified as follows:

- Frame length = 125 μs
- One Frame contains 24-Channels and a frame bit: The total number of bits per frame is

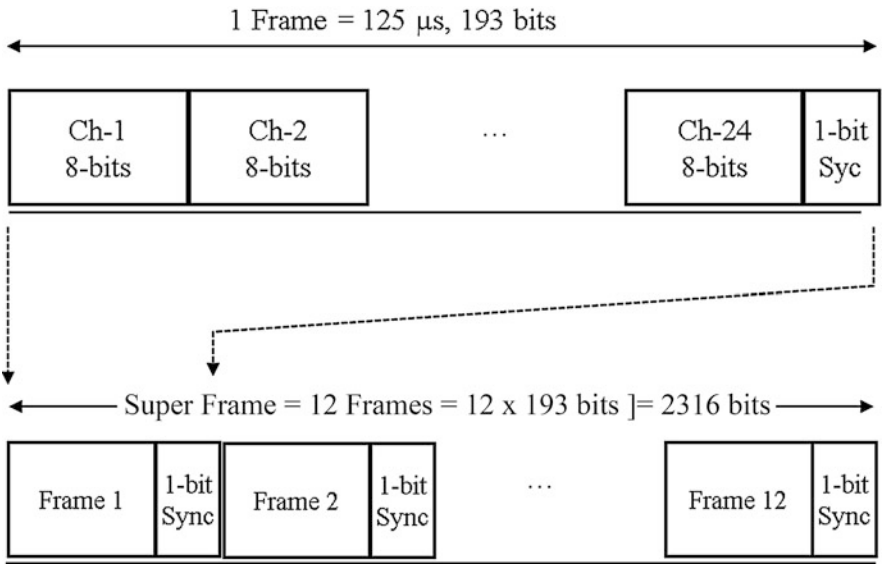


Fig. 5.4 Distributed frame structure. 12 sync bits are distributed among 12 frames

$$F = 24 \times 8 + 1 = 193 \text{ bits per frame}$$

- A Super Frame (Multi Frame) contains 12 Frames:

$$S = 12 \times 1,193 = 2,316 \text{ bits per super frame}$$

Advantages:

- Immune to burst errors. Because frame bits are distributed
- Synchronizer has enough time to compute

Disadvantages:

- It takes a long time to synchronize. Because all the sync. bits are needed in the computation.

5.2.3 Bunched Frame Structure

A bunched frame is constructed by placing 12 sync bits in one time slot. This is shown in Fig. 5.5.

In this scheme, the bunched frame is specified as follows:

- A Channel contains M-bits (e.g., 8-bits)
- One Frame contains 12-Channels

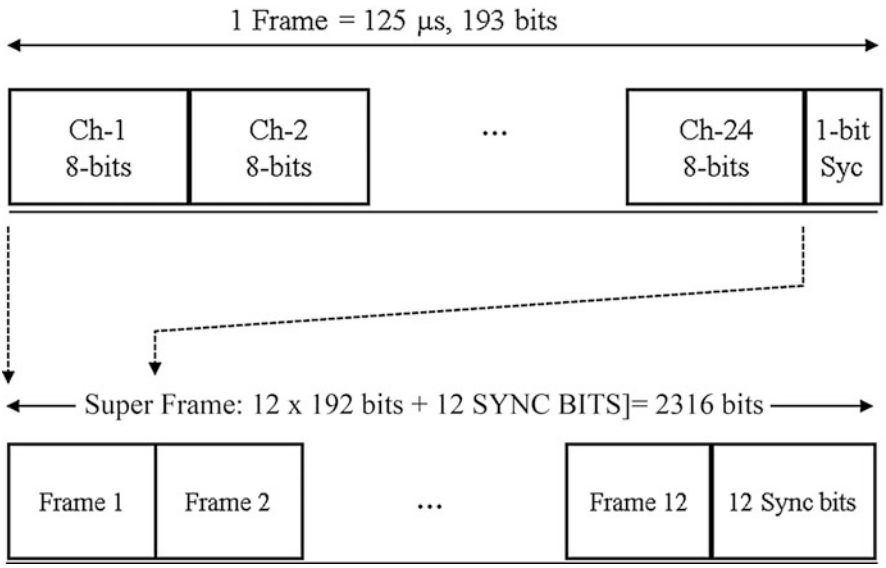


Fig. 5.5 Bunched frame structure.12 sync bits are bunched together at the end of the super frame

- $F = 24 \times 8 = 192$ bits per frame
- A Super Frame (Multi Frame) contains 12-Frames + 12 sync bits bunched

$$S = 192 \times 12 + 12 = 2,316 \text{ bits per super frame}$$

Therefore the total number of bits is the same in both cases

Advantages and Disadvantages of Bunched Frame Structure:

Advantages:

Faster synchronization if sync. bits are inserted in every frame.

- Sync. Maintenance in the frame level

Disadvantages:

- Poor performance in jamming. Because frame bits are bunched.

5.3 European TDM in Digital Telephony

The European TDM [1, 2] for digital telephony supports 32 TDM channels per frame, where each TEM channel is a 64 kb/s channel. The frame and super frame structure is shown in Fig. 5.6. At the transmit side (Multiplexing):

- 32-channels are interleaved in preassigned time slots, 8-bits per time slot.
- 32-channels form a frame.
- Time slot 1is reserved for synchronization.
- Time slot 16 is reserved for signaling.

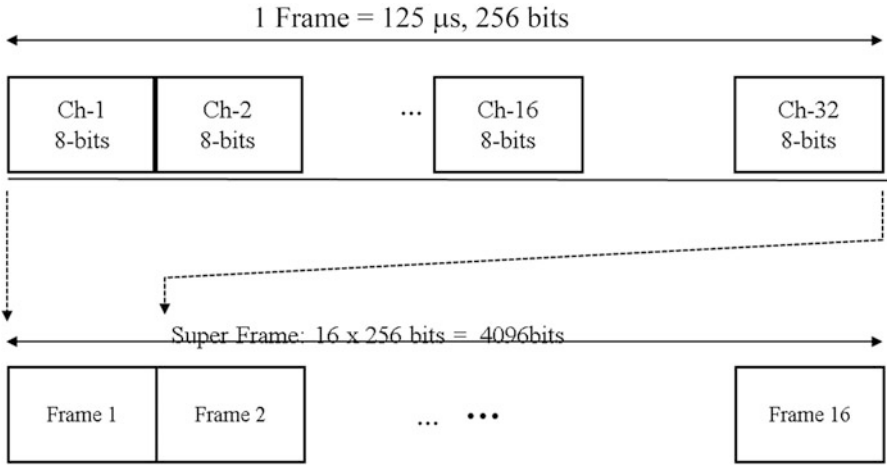


Fig. 5.6 The European frame and super frame structure. There are 32 time slots per frame. Time slot 18is reserved for synchronization. Time slot-16 is reserved for signaling. Rest of the time slots are used for data. The super frame contains 16 frames

- Rest of the time slots are for data.
- DS-0 Rate = 64 kbps.
- Each DS-0 channel has 8-bits.
- Total Number of bits/Frame = $8 \times 32 = 256$ bits.
- The frame length = 125 μs.
- bit rate=256/125 μs = 2,048 Mb/s.

At the receive side (DE multiplexing):

- The De-multiplexer receives successive frames
- Each frame has a "header frame synchronization pattern" which is unique
- The De-multiplexer synchronizes with the frame bit pattern and recovers all the channels and puts them in the right order

5.4 Frame Synchronization

5.4.1 Synchronization Process

There are two modes of operation in frame synchronization circuits:

- Mode-1: Frame Search Mode or Frame Acquisition Mode
- Mode-2: Frame Maintenance Mode

In Frame Acquisition Mode:

- It searches through the candidate frames
- Looks for the unique frame pattern
- It keeps looking until a valid pattern is detected
- If valid, it accepts the frame, if not, it rejects the frame
- The accept/reject criteria is based on a "Correlation Process"

In Frame Maintenance Mode:

- After synchronization, each frame is continuously monitored and a frame quality indicator is generated as "Frame Error Rate (FER)"
- If FER $\leq$ Threshold, it maintains the synchronization
- If FER $>$ Threshold, it declares loss of sync and
- The synchronization process begins again

5.4.2 Estimation of Frame Error Rate

The estimation of frame error rate is based on a correlation process. In this process, it performs the following:

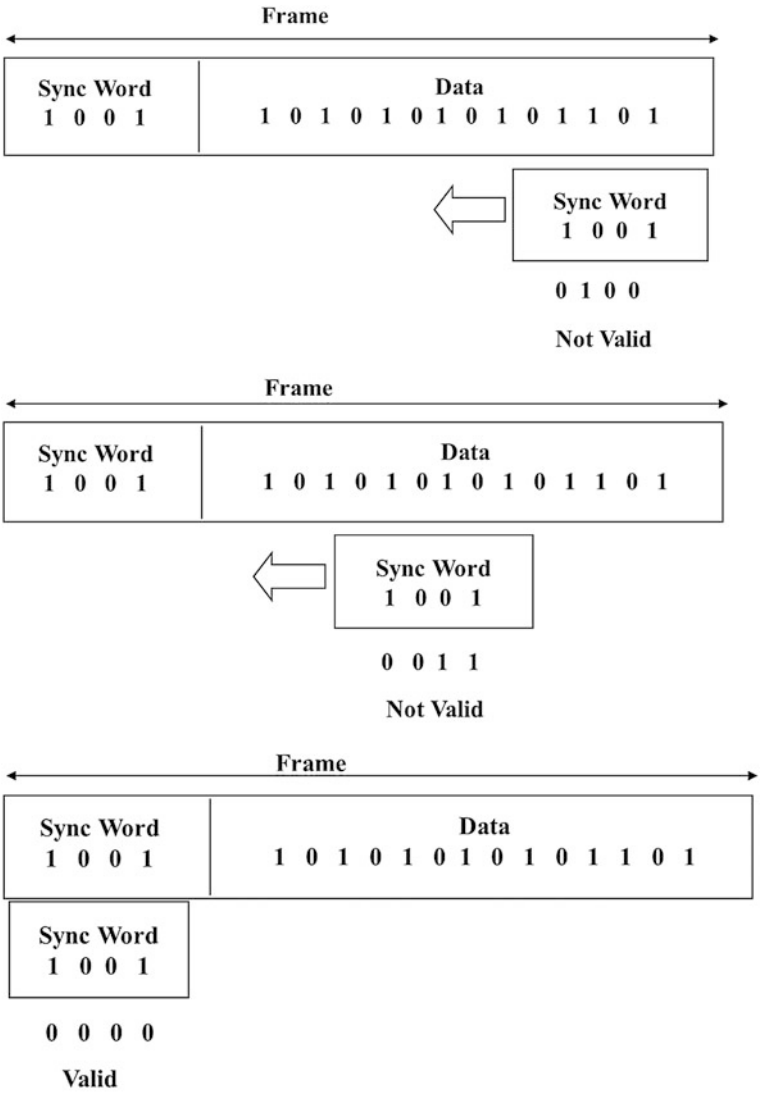


Fig. 5.7 Sliding correlator. The sync word is compared with the received data for correlation, as it slides

- It compares k-bit sync word with a k-bit data block by means of a sliding correlator as shown in Fig. 5.7.
- It begins with the k-bit sync word and compares with a k-bit word. If it matches, the receiver declares a success and begins tracking. If not, the sync word is shifted by one bit and compared with the next k-bit data word for a possible match.

- For every shift, it counts the number of mismatches and computes the error rate as:

$$P_e = \text{Number of errors/k (per sample)}$$

- The process continues until the correct sync word is found with the least error
- At the end it also computes the average error
- This average error is used as a pass/fail criteria

The theoretical estimation of frame error is done by means of a process called "False Detection Probability (P_f)" as follows:

- There are k-bits in the correlation process
- It is also a binary system: Probability of a False 1 = Prob. of a False 0 = 0.5. Therefore in a k-bit comparison we must have:

Where,

$$P_f = \left(\frac{1}{2}\right)^k$$

$$k \frac{\log_{10}(P_f)}{\log_{10}(0.5)} \tag{5.1}$$

Therefore by knowing the required value of P_f, the length of the sync word can be found. This is plotted in Fig. 5.8.

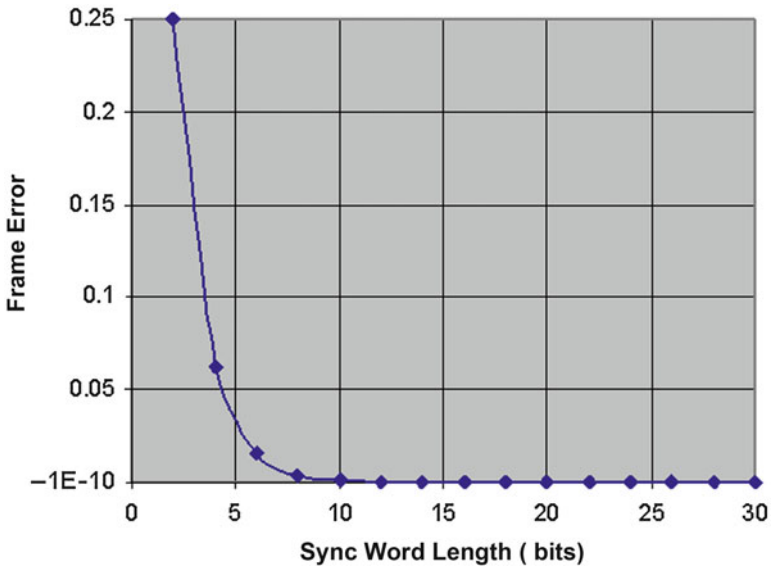


Fig. 5.8 BER Performance as a function of word length

5.5 North American TDM Hierarchy

The TDM hierarchy is composed of a multi-frame structure known as super frame as shown in Fig. 5.9.

- The super frame contains 12 Frames
- Each frame has a sync bit
- Total number of sync bit = 12
- These 12 sync bits are used to synchronize the frames and multi frames
- Number of bits/multi frame = 193 × 12 = 2,316 bits
- Fraction used by Sync = 12/2,316 = 0.005181
- This gives rise to Frame Error Rate, which is given by, FER, also known as the probability of frame error rate:

$$P_f = (0.5)^{12} = 2.44 \times 10^{-4} \tag{5.2}$$

DS-1 (T1) Rate can be estimated as:

- Number of information bits/Frame = 193 bits/frame
- Frame Length = 125 μs
- Bit Duration T_b = 125 μs/193
- DS-1 Rate = $1/T_b$ = 1.544 Mbps

Higher rates can be obtained from DS-1 by successive multiplexing as shown in Fig. 5.10. These rates are estimated as follows:

- DS2 Rate = 4 × DS1 = 4 × 1.544 Mbps = 6.312 Mbps
- DS3 Rate = 7 × DS2 = 7 × 6.312 Mbps = 44.736 Mbps
- DS4 Rate = 6 × DS3 = 6 × 44.736 Mbps = 274.176 Mbps
- DS5 Rate = 2 × DS4 = 2 × 274.176 Mbps = 560.160 Mbps

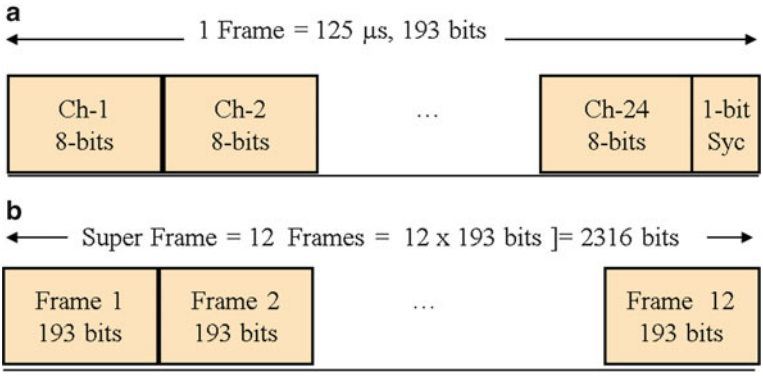


Fig. 5.9 The North American TDM multi frame structure. (**a**) The frame. (**b**) Super frame containing 12 frames

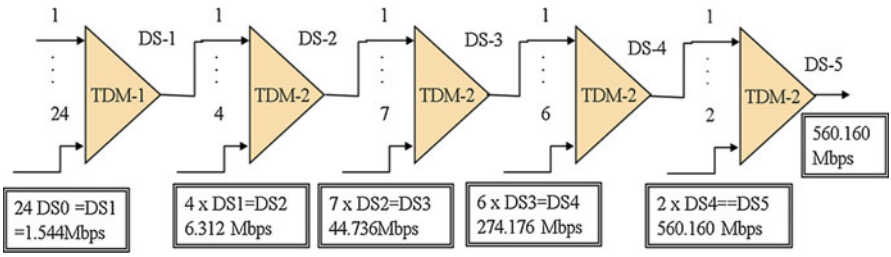


Fig. 5.10 The North American TDM hierarchy

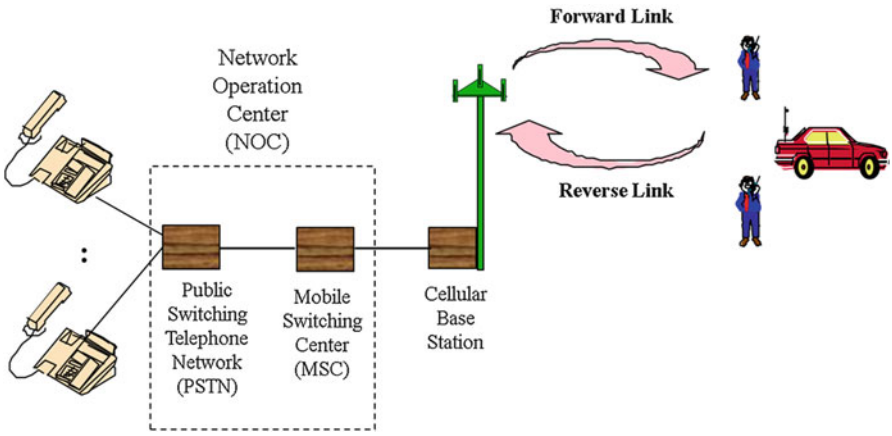


Fig. 5.11 The basic land-mobile cellular communication system

5.6 Time Division Multiple Access (TDMA)

5.6.1 The North American TDMA

The North American TDMA is a narrow band (30 kHz) mobile cellular system, which supports dual-mode (1G & 2G) cellular communication systems [4–7]. Since the transmission bandwidth is only 30 kHz, the digitized 64 kb/s voice data is first compressed by means of a Vocoder, encoded for error control coding, modulated and finally transmitted over the air as depicted in Fig. 5.11.

At the transmit side, the voice is first digitized and then compressed by means of a vocoder to form a low bit rate data stream. The compressed data is then encoded by means of rate 1/2 convolutional encoder and interleaved. Together with frame overhead, the composite bit rate becomes 16.2 kb/s for each user. This 16.2 kb/s data is distributed within two 6.66 ms time slots, 8.1 kb/s data per time slot. Three of these 16.2 kb/s subscriber data are combined to form a 48.6 kb/s TDMA frame.

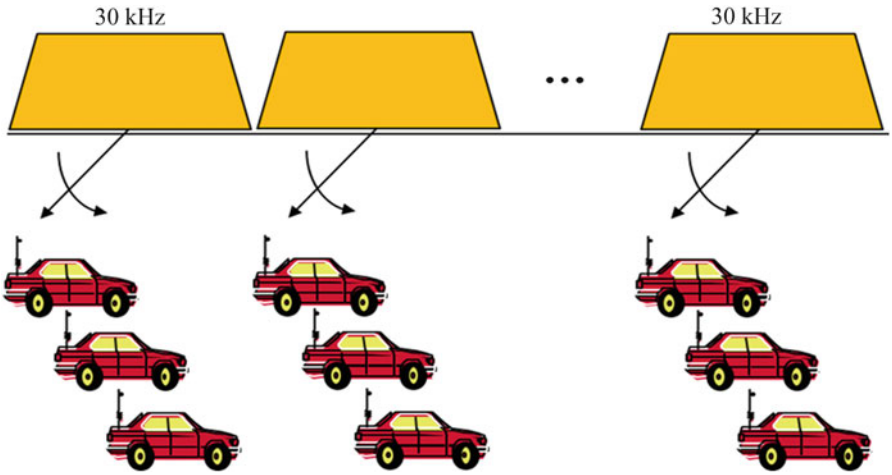


Fig. 5.12 The North American TDMA scheme where each FDMA channel is time shared by three mobiles

In the forward link (base station to mobile), the base station modulates the composite 48.6 kb/s data stream by means of a π/4 DQPSK modulator for transmission [5–7]. In the reverse link (mobile to base station), the mobile modulates the 16.2 kb/s data by means of a π/4 DQPSK modulator for transmission. In the receive side, the data is recovered by means of a reverse process. In this section, we will examine the underlying principle of communication of the digital cellular system.

5.6.2 North American TDMA Scheme

The North American TDMA is a hybrid process where each FDMA channel is time-shared by three mobiles to accomplish TDMA, as shown in Fig. 5.12. It implies that when one mobile has access to the channel, the other two mobiles are idle. This is achieved by means of a special frame structure, which is yet to be discussed. TDMA Channel capacity is therefore 3 × FDMA in TDMA.

The TDMA has several advantages over FDMA:

- Increased channel capacity
- Greater immunity to noise and interference
- Secure communication
- More flexibility and control

Moreover, it allows the 1st generation analog cellular system to coexist in the same TDMA platform, sharing the same RF spectrum. The detailed technology, adopted as the North American TDMA standard, is presented in the following sections.

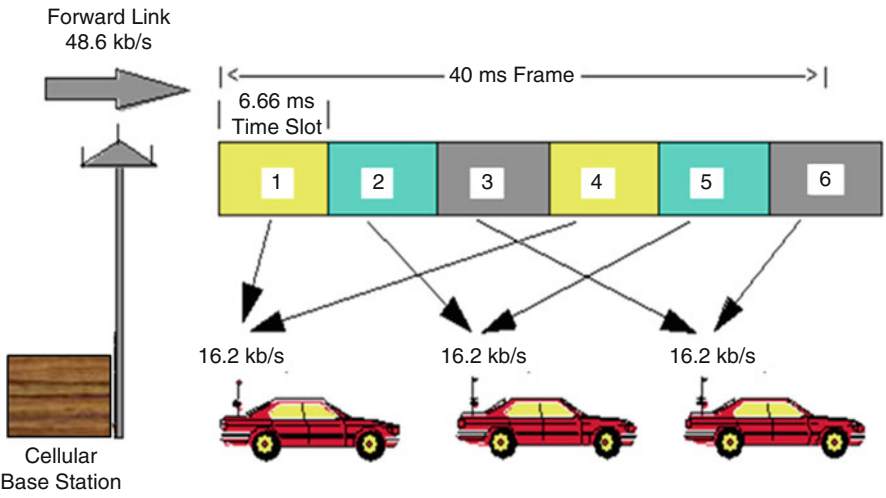


Fig. 5.13 TDMA forward link format

5.6.3 TDMA Transmission Format

The TDMA air link is based on a 40 ms frame structure, equally divided into six time slots, 6.667 ms each. Each of the six time slots contains 324 gross bit intervals, corresponding to 162 symbols (1 symbol = 2 bits of information). Figures 5.13 and 5.14 show the TDMA frame structure for the forward link (base to mobile) and the reverse link (mobile to base) respectively. In TDMA-3, the time slots are paired as 1–4, 2–5 and 3–6 where each disjoints pair of time slots are assigned to a mobile. This arrangement enables three mobiles to access the same 30 kHz channel one at a time. In TDMA-6 (not yet implemented), each time slot will be assigned to a single mobile for a total of six mobiles per channel.

The TDMA-3 forward link uses a rate 1/2 Convolutional encoding with interleaving. The encoded 48.6 kb/s data bit stream is modulated by means of a $\pi/4$ DQPSK modulation and then transmitted from the base station to the mobile where each mobile receives data at 16.2 kb/s.

At the receive side the RF signal is demodulated, decoded and finally the original data is recovered. Since this is a radio channel, the recovered data is impaired by noise, interference and fading. As a result, the information is subject to degradation. Although error control coding greatly enhances the performance, the C/I (Carrier to Interference ratio) is still the limiting factor. The TDMA-3 reverse link is exactly the reverse process as shown Fig. 5.14.

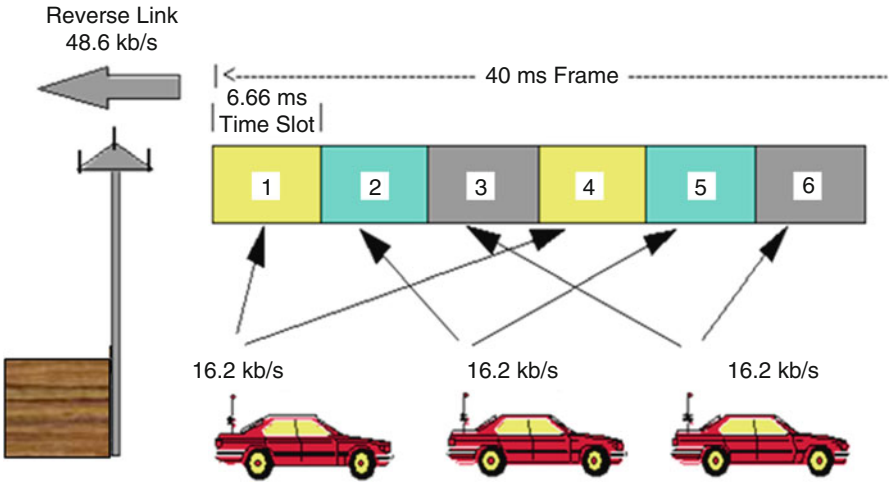


Fig. 5.14 TDMA reverse link format

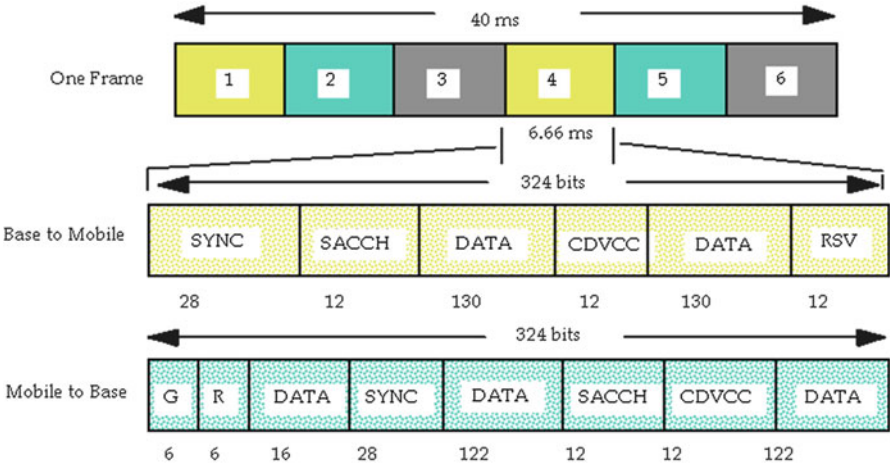


Fig. 5.15 TDMA time slot and data field structure

5.6.4 TDMA Time Slots and Data Field Structure

Each 6.66 ms time slot is subdivided into several sub-fields as shown in Fig. 5.15. Each sub-field is different and has its own data field to define the message structure. These data fields and their functions are briefly described below:

G (Guard Time): Duration = 6 bits (3 symbols). Used by mobiles at the beginning of the frame to avoid time slot collisions.

R (Ramp Time): Duration = 6 bits (3 symbols), Power ramp time, used by the mobile to accommodate delays associated with power ramp.

SYNC.: Duration = 28bits (14 symbols). Used by both base & mobiles for time slot synchronization, equalizer training and time slot identification.

DATA: User information, compressed by vocoder, rate 1/2 convolutionally encoded, interleaved data, Used by base & mobiles. This time slot is also shared by FACCH (Fast Associated Control Channel).

FACCH: Fast Associated Control Channel. Used for signaling message exchange between the base & the mobile. No message is transmitted during this process. As a result, there is a minor impact on voice quality. FACCH is generally used for hand-off messaging. Many other messaging requiring immediate responses is also sent via FACCH. Error protection is the same as data.

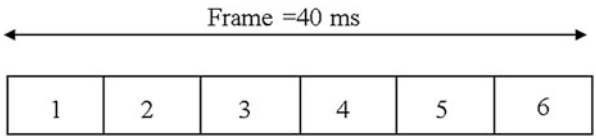
SACCH: Slow Associated Control Channel. A dedicated continuous channel used for signaling message exchange between the base & the mobile. SACCH is present in all designated slots regardless of the presence of data or FACCH. It is a 12 bit (6 symbol) field, rate 1/2 convolutionally encoded and interleaved.

CDVCC: Coded Digital Verification Color Code. A 12 bit (6 symbol) data field. It is generated from an 8 bit DVCC (Digital Verification Color Code) having 255 distinct values. The DVCC is analogous to the SAT frequencies in AMPS system. It is used to distinguish a serving channel from a reuse channel. The 12 bit CDVCC generated from the 8 bit DVCC field by adding four protection bits.

Problem 5.2

Given:

- Frame length = 40 ms (Figure below).
- The frame contains Six time slots and supports three users.
- Each user originates 16.2 kbps data.



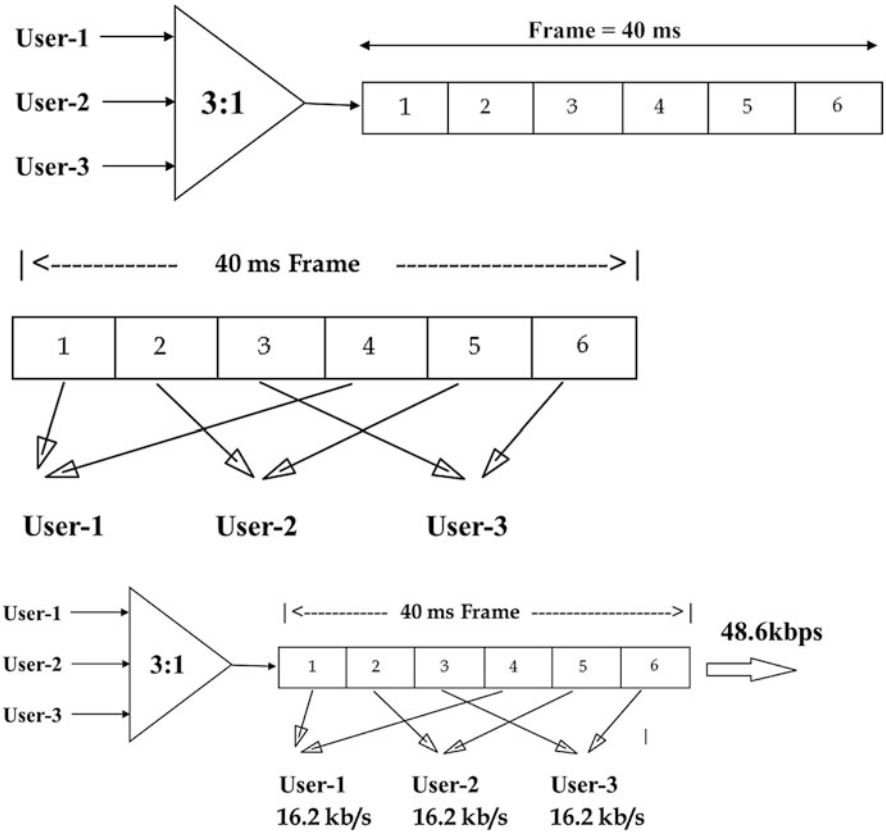
Find:

(a) A suitable multiplexing structure
(b) The composite data rate in the channel
(c) Number of bits/Frame

Solution:

(a) We have 3 users and 6-Time Slots. Therefore we can assign 2-time slots/user:

- User-1: Time slot 1 and 4
- User-2: Time slot 2 and 5
- User-3: Time slot 3 and 6



(b) Composite Data Rate:
16.2 kbps/user × 3 = 48.6 kbps
(c) Number of bits/Frame = Frame length /Bit duration
=40 ms/(1/48.6 kbps) = 1,944 bits/Frame

Problem 5.3
Consider the previous problem again and construct a de-multiplexing scheme to recover three users.
Answer:

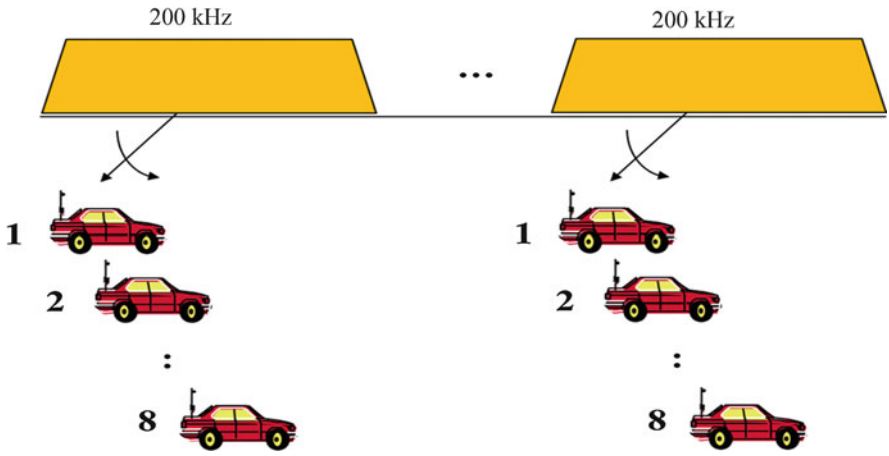


Fig. 5.16 The European GSMTDMA scheme. Each 200 kHz channel is time shared by eight users

5.7 Global System for Mobile Communication (GSM)

5.7.1 GSM TDMA Schème

GSM (Groupe Spécial Mobile) also known as Global System for Mobile Communications, is a second generation (2G) digital cellular communication standard developed in Europe [7–10]. In GSM, a given frequency band is divided into 200 KHz per carrier, where each carrier is time shared by eight users as depicted in Fig. 5.16.

Since each RF carrier frequency is time shared between 8 users, there are 8 time slots in the GSM frame. According to the GSM communication protocol, the time slot is assigned to a mobile during the channel assignment Session. Therefore, when one mobile is active, other mobiles remain idle. Each mobile waits for their turn.

5.7.2 GSM TDMA Frame (4.615 ms)

The GSM frame is constructed by multiplexing 8 time slots as shown in Fig. 5.17. It has the following design specifications:

- Frame duration: 4.615 ms
- Frame length: 8 time slots
- Duration of Time slot = 0.576875 ms = 0.577 ms
- Number of bits per time slot: 156.25 bits
- Bit rate: 270.833 kb/s

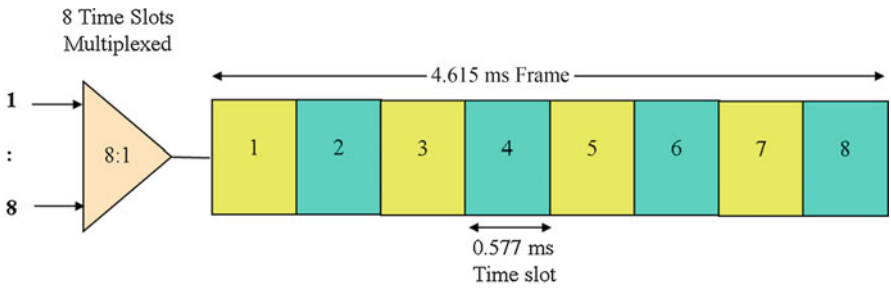


Fig. 5.17 GSM TDMA frame structure. Eight time slots multiplexed to construct a frame

5.7.3 GSM TDMA Frame Hierarchy

GSM Multiframe

The GSM TDMA hierarchy is composed of two types of multi-frame structure known as:

- Control Multi-Frame for messaging and signaling (51 time slots, 0.577 ms/time slot)
- Traffic Multi-Frame for voice and data (26 time slots, 0.577 ms/time slot)

The Control multi-frame, shown in Fig. 5.18, has 51 time slots-Called control multiframe, composed of 51 bursts in duration of 235.4 ms. The time slots are used for messaging and control function such as channel assignment, handoff, paging etc.

The Traffic multi-frame, also shown in Fig. 5.18, has 26 time slots—Called traffic multiframe, composed of 26 bursts in duration of 120 ms. These time slots are used voice and data communication.

GSM Superframe (6.12 s)

GSM superframe is constructed by multiplexing several multiframes. There are two schemes in the superframe:

- 51 traffic multiframes and 26 control multiframes. OR
- 26 traffic multiframes and 51 control multiframes.

When the scheme interchanges, the different number of traffic and control multiframes within the superframe, the time interval within the superframe remains the same. See Fig. 5.18a, b.

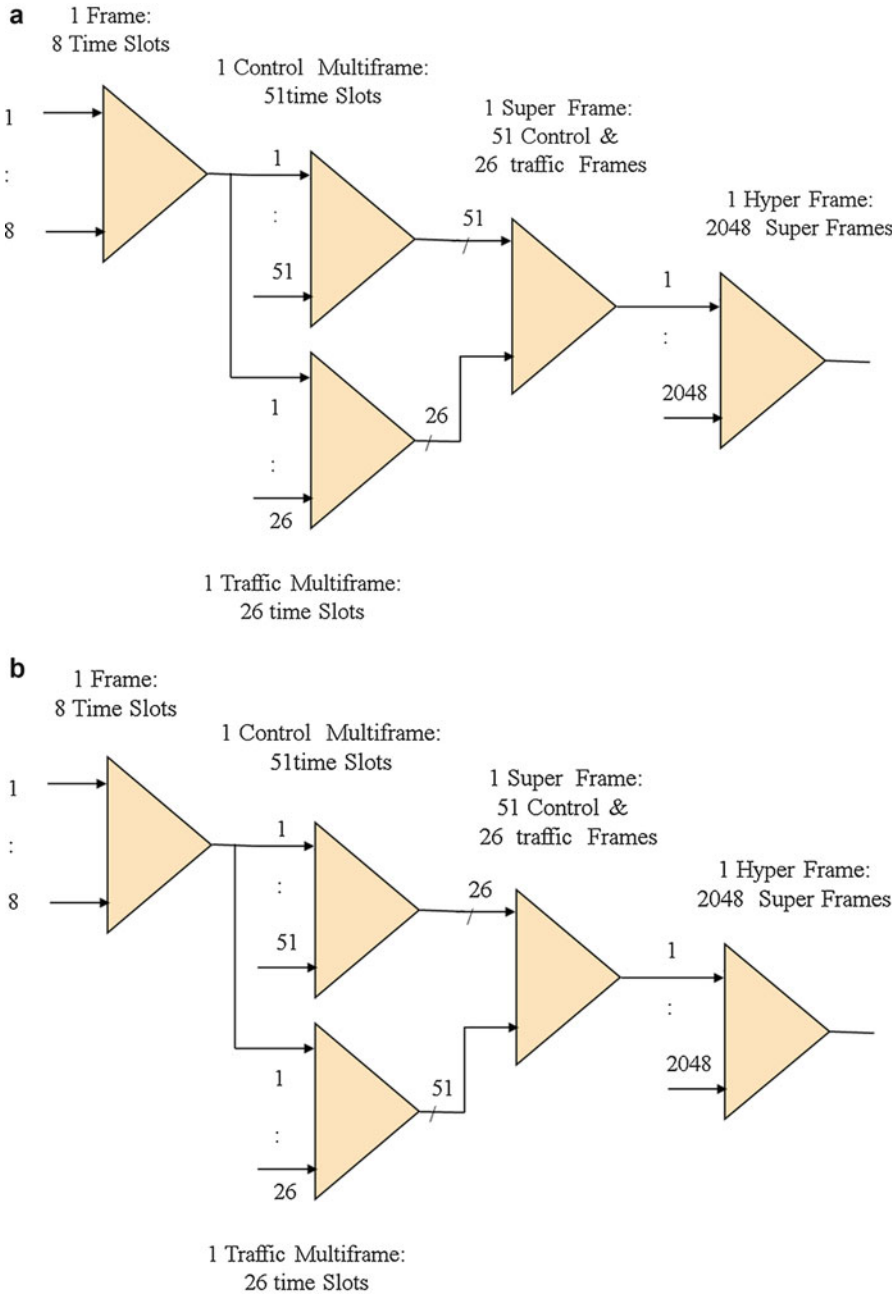


Fig. 5.18 GSM frame hierarchy, composed of frame, multiframe, superframe and hyperframe

GSM Hyperframe

GSM hyperframe is constructed by multiplexing 2,048 Super Frames. The hyperframe is used to:

- Maintain different schedules in order.
- Synchronize and maintain encryption.
- Synchronize frequency hopping between the transmitter and the receiver so that they hop to a new frequency at the same time. This is a low frequency hopping feature in GSM.

5.8 TDMA Performance

5.8.1 Uncoded and Coded BER

Performance analysis provides an early prediction of potential problems and offers successful deployment of cellular networks. For TDMA, this is generally accomplished by means of estimating the channel BER (Bit Error Rate). We examine this by using a simplified channel model with and without coding. An exact analysis of this problem is fairly complex. However, an approximation can be made using the following assumptions:

- The radio is assumed to be a coded, interleaved communication system
- The interleaver depth is infinite so that the error bits are evenly distributed
- Rate ½ convolutional encoding with constraints length = 5
- Viterbi decoder on the receiver side
- M-ary PSK modulation/demodulation with M = 4

A model of the receiver that closely approximates the above set of assumptions is shown in Fig. 5.19. We further assume that the receiver is operating in additive white Gaussian noise (AWGN).

For equally likely coherently detected M-ary signaling, the probability of symbol error is given by [11–14]:

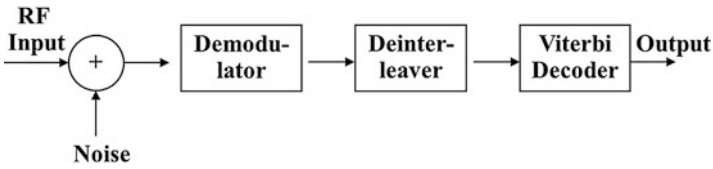


Fig. 5.19 TDMA channel model for performance analysis

$$P_e(M) = 2Q\left(\sqrt{\frac{2E_s}{N_o}}\sin\frac{\pi}{M}\right) \tag{5.3}$$

where

$E_s = E_b\log(M) =$ Energy per symbol
$E_b =$ Energy per bit
$N_o =$ Noise spectral density

$$Q(x) = Q\left(\sqrt{\frac{2E_s}{N_o}}\sin\frac{\pi}{M}\right) = \text{Complementary error function} \tag{5.4}$$

$$x = \sqrt{\frac{2E_s}{N_o}}\sin\frac{\pi}{M} \tag{5.5}$$

Since Q(x) cannot be evaluated in closed form, we use the following approximation:

$$Q(x) \approx \frac{1}{x\sqrt{2\pi}}\exp\left(-\frac{x^2}{2}\right) \tag{5.6}$$

For QPSK modulation we have $M = 4$ and $E_s = 2E_b$. Therefore, from the above equations, we obtain the uncoded BER as,

$$P_e(4) = \frac{1}{\sqrt{\frac{E_b}{N_o}\pi}}\exp\left(-\frac{E_b}{N_o}\right) \tag{5.7}$$

and the coded BER as,

$$P_e(Coded) = k\{P_e(4)\}^m \tag{5.8}$$

Where $k = 1{,}290$ and $m = 4.44$; obtained by means of curve fitting [6, 14].

The uncoded and coded BER equations are plotted as a function of E_b/N_o in Fig. 5.20. The improvement in BER performance is clearly evident. We also note that the coded BER > Uncoded BER at $E_b/N_o < 2.5$ dB. This is due to decoder break down at low E_b/N_o.

5.8.2 *BER as a Function of Mobile Speed*

Fading occurs when the mobile is in motion. The fade duration is inversely proportional to the mobile speed. Figure 5.21b shows a qualitative representation

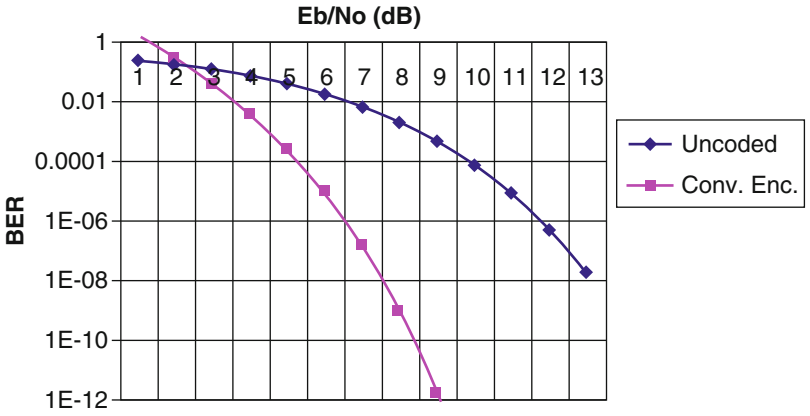


Fig. 5.20 TDMA BER performance with and without coding

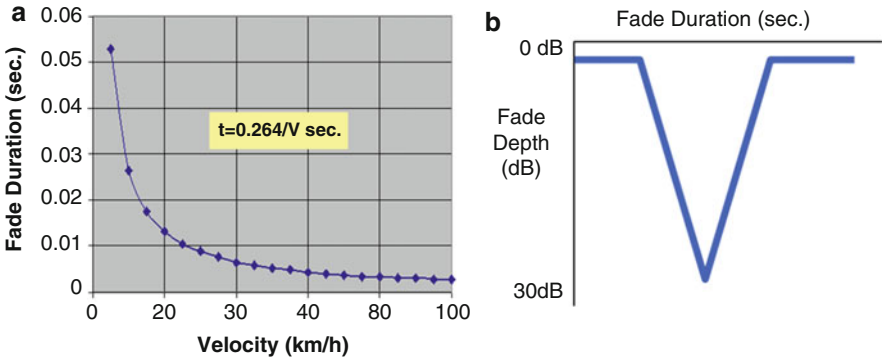


Fig. 5.21 (**a**) Fade duration as a function of mobile speed and (**b**) Qualitative representation of fade depth as a function of fade duration

of fade depth as a function of fade duration. This can be estimated by means of the following equation [5]:

$$t \approx \frac{0.264}{v} \tag{5.9}$$

Where t is the fade duration and v is the velocity of the mobile. The above equation is plotted in Fig. 5.21a, which shows that fade duration decrease with increasing mobile speed. We also note that fade duration = 6.6 ms @ 40 km/h which is exactly one time slot of the North American TDMA frame (40 ms/6 = 6.6 ms). This implies that the entire time slot is subject to impairments. Since the bit rate is 48.6 kb/s, the 6.6 ms time slot translates into 120 bits. In other words, 120 bits will be jammed @ 40 km/h. However, it does not mean that there will be an outage. This is due to the

fact that survivability depends on fade duration, depth of fading and the built-in error control coding.

We will now estimate the BER performance by means of the illustration shown in Fig. 5.17b where the depth of fading is shown as a function of fade duration. We see that a deep fade is associated with a short duration while a shallow fade is associated with long duration. This implies that a deep fade (short duration) is less vulnerable due to the presence of FECC, which will detect and correct errors. Likewise, a shallow fade (long duration) is also less vulnerable since Eb/No will be adequate to achieve the BER objective. It follows that a fading that is neither shallow nor deep is a point of concern.

The uncoded BER that follows the above logic can be expressed as

$$P_\alpha(4) = \frac{\alpha}{\sqrt{\frac{E_b}{N_o}\pi}} \exp\left(-\frac{E_b}{N_o}\alpha\right) \tag{5.10}$$

and the coded BER as

$$P_\alpha(Coded) = k\{P_\alpha(4)\}^m \tag{5.11}$$

Where $0 < \alpha < 1$ is the fractional jamming (interference), k = 1,290 and m = 4.44 [xx]. Figure 5.22 shows the BER as a function of fractional interference for several values of E_b/N_o. A close inspection reveals that a worst-case performance appears around 20 % fractional jamming. Therefore the fraction of the time slot that is being jammed is 6.6 ms × 0.20 = 1.32 ms. The 1.32 ms fractional jamming corresponds to a mobile velocity of 20 km/h. Therefore, in IS-54/136, the worst-case performance can be expected at mobile velocity of 20 km/h. The survivability then depends on Eb/No.

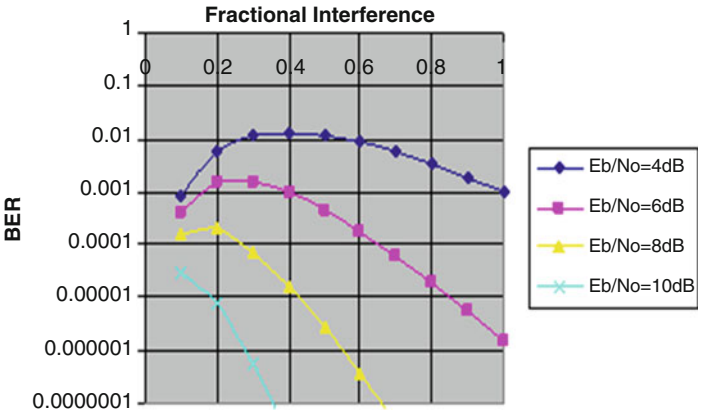


Fig. 5.22 BER as a function of fractional jamming

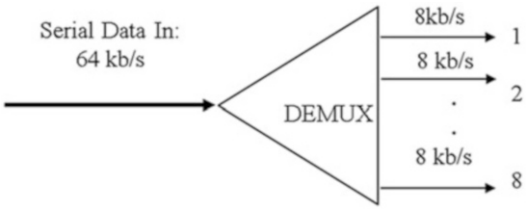
Problem 5.4

Given:

A 64 kb/s serial data is converted into 8 parallel streams. What is the output bit rate after serial to parallel conversion?

Solution:

The output bit rate after 1:8 serial to parallel conversion will be 64 kbps/8 = 8 kb/s/ as shown in the figure below:



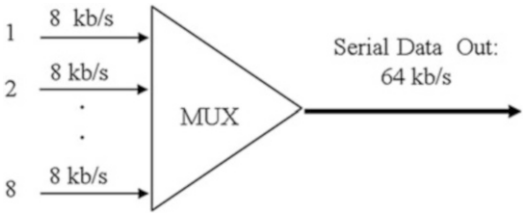
Problem 5.5

Given:

Eight parallel data streams, having 8 kb/s each, is parallel to serial converted to form a composite bit stream. What is the output bit rate after 8:1 parallel to serial conversion?

Solution:

The output bit rate after 8:1 parallel to serial conversion will be 8 kb/s × 8 = 64 kb/s/ as shown in the figure below:



5.9 Conclusions

- Defined TDM and TDMA
- Described TDM frame and frame hierarchy used in North American and European Land Telephone System
- Illustrated Frame Synchronization Process
- Reviewed North American TDMA and European GSM TDMA System used in Wireless Communications

- Illustrated TDMA Frame and Frame Hierarchy
- Presented TDMA BER Performance Analysis

QUIZ:

1. A PCM system needs to process analog signals ranging from 300 to 3,400 Hz. What type of band limiting filter is needed? (Select one)

   a. Band reject filter
   b. Band pass filter
   c. Low pass filter
   d. High pass filter

2. The filtered signal in problem-1 is sampled at 8 kHz. Each sample is then converted into 8bits. What is the output bit rate?

   a. 32 kb/s
   b. 64 kb/s
   c. 128 kb/s
   d. 256 kb/s

3. According to the Nyquist theorem, the sampling frequency should be:

   a. More than the analog frequency
   b. More than twice the analog frequency
   c. Equal to the analog frequency,

4. In an 8-bit PCM, the number of quantization levels are given by:

   a. 255
   b. 256
   c. 257

5. In an 8-bit PCM, the number of quantization steps are given by:

   a. 255
   b. 256
   c. 257

6. In an 8-bit PCM, the voltage (V) per step is given by:

   a. V/255
   b. V/256
   c. 2V/255
   d. 2V/256

7. A PCM signal is band limited up to 3.4 kHz and then sampled at 8,000 times per second. If each sample is converted into 8-bits, What is the output bit rate?

   a. 34 kb/s
   b. 64 kb/s
   c. 128 kb/s

8. A given residential area has 1,000 homes. Each home has a land-line telephone. If each telephone originates 64 kb/s data, construct a PCM hierarchical system to support the traffic.

   Answer:

9. A distributed frame structure is constructed having 40 ms per frame, sync word = 12 bits. Specify the sync time.

   Answer:

10. A full duplex communication system provides one of the following:

    a. One way communication
    b. Two way communication, one at a time
    c. Two way communications, simultaneously
    d. None of the above

11. A TDM wireless communication system combines data from three users to form a composite data stream. If each user generates 16.2 kb/s data, what is the composite bit rate?

    a. 16.2 kb/s
    b. 32.4 kb/s
    c. 48.6 kb/s

12. A TTDMA frame structure has the following specifications:

    a. Frame length = 40 ms
    b. Bit rate = 48.6 kb/s
    c. Sync. Word = 48 bits (at the beginning of the frame).

    Find:

(a) The probability of false detection.
(b) The maximum sync. time needed to validate the frame. (Assume sliding correlator)

    Answer:

13. The North American TDMA standard allocates 30 kHz per channel. In the FCC allocated frequency band is 12.55 MHz, calculate the number of users supported by the band.

    Answer:

14. The GSM standard allocates 200 MHz per channel If each channel supports eight users one at a time, calculate the total number of users that can be supported.

    Answer:

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Chapter 6
Phase Division Multiple Access (PDMA)

Topics

- Introduction to PDMA
- Error Control Properties of Orthogonal codes
- Construction of Multi User PDMA
- Hybrid TDMA—PDMA Structure
- BER Performance of PDMA
- Conclusions

6.1 Introduction

Phase Division Multiple Access (PDMA) is a technique where data from multiple users are multiplexed in the phase domain and transmitted over a channel. Figures 6.1 and 6.2 show simplified diagrams to illustrate the concept. As shown in these figures, PDMA is a coded Multi Phase Shift Keying modulation technique, where multiple users have access to the same carrier frequency through the phase constellation. In the proposed scheme, the input digital signal is mapped into a block of orthogonal codes. The encoded data, which is in orthogonal space, modulates the carrier frequency by means of MPSK modulator. For example, in QPSK modulation, there are four paces or four symbols, two bits per symbol. Therefore we can support two users per symbol, one bit from each user. Similarly, in 8PSK, there are eight symbols, three bits per symbol. Therefore, we can support three users per symbol. Likewise a 16PSK modulator can support 4 users per symbol. In this manner we can increase the number of users as long as the symbol errors are within the acceptable limit. At the receiver the data is recovered by means of code correlation. This modulation technique offers multiple error correction with bandwidth efficiency.

S. Faruque, *Radio Frequency Source Coding Made Easy*, SpringerBriefs
in Electrical and Computer Engineering, DOI 10.1007/978-3-319-15609-5_6

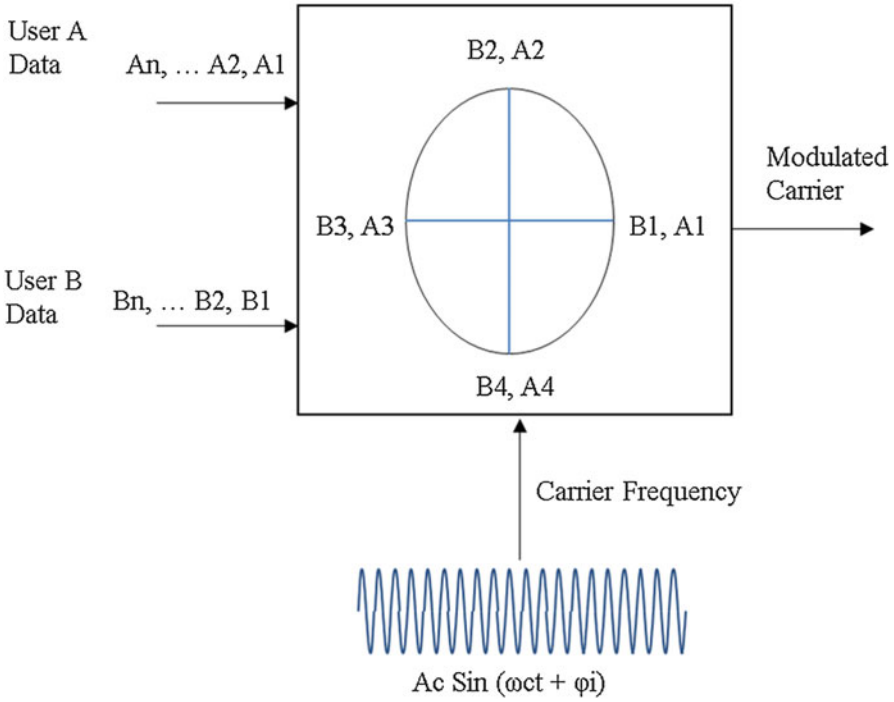


Fig. 6.1 Phase division multiple access. Encoded data from two users are multiplexed in the phase domain. There are four phases (symbols). Each symbol supports two users

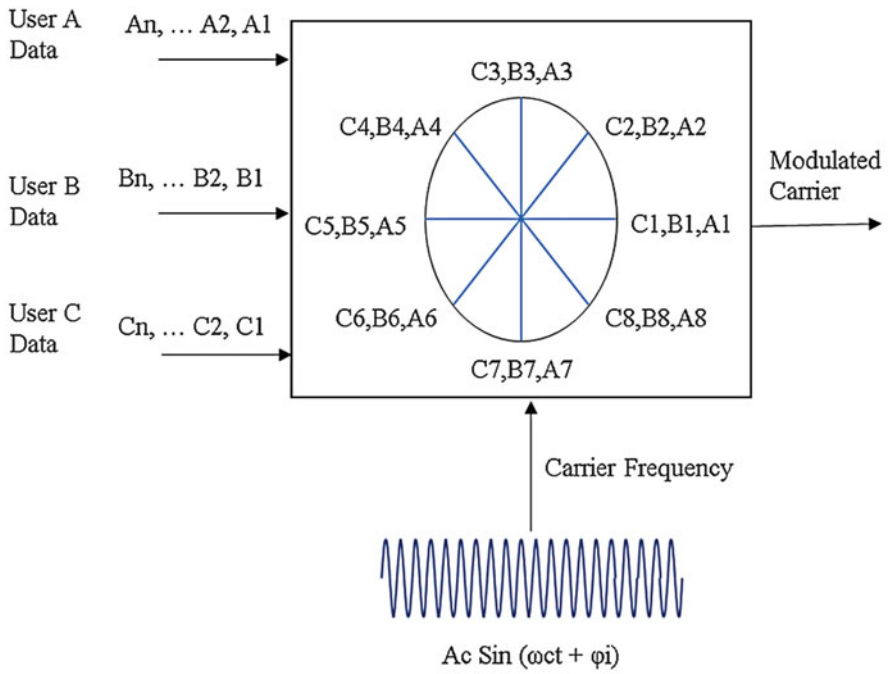


Fig. 6.2 Phase division multiple access. Encoded data from three users are multiplexed in the phase domain. There are eight phases (symbols). Each symbol supports three users

Our objective in this chapter is to show that:

- Multiple users can share the same carrier frequency in the phase domain, realizing Phase Division Multiple Access (PDMA).
- Orthogonal codes can be used to detect and correct multiple errors with bandwidth efficiency.
- Phase Division Multiple Access (PDMA), along with Orthogonal codes, is a possible solution to utilize spectrum efficiently with multiple error correction capabilities.
- Construction of a PDMA2 supporting 2 users and a PDMA4 supporting four users are presented to illustrate the concept.

6.2 Properties of Orthogonal Codes

6.2.1 Orthogonal and Biorthogonal Codes

Orthogonal codes are binary valued and have equal numbers of 1's and 0's. Antipodal codes, on the Other hand, are just the inverse of orthogonal codes. Antipodal codes are also orthogonal among themselves. Therefore, an n-bit orthogonal code has n-orthogonal codes and n-antipodal codes, for a total of 2n biorthogonal codes. For example an 8-bit orthogonal code has 16 bi-orthogonal codes as shown in Fig. 6.3.

Since there are an equal number of 1's and 0's, each orthogonal code will generate a zero parity bit. Antipodal codes are also orthogonal among themselves. Therefore, each antipodal code will generate a zero parity bit as well. We also note

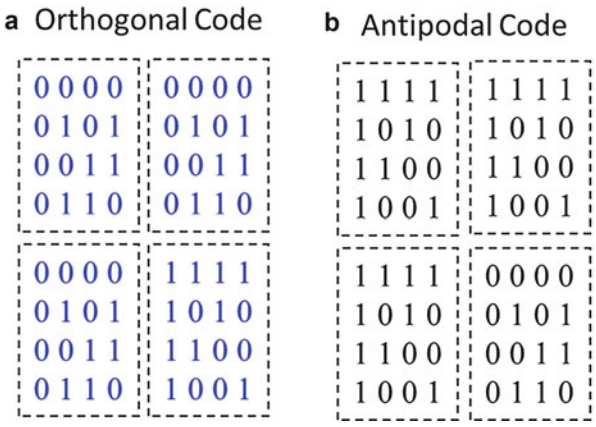


Fig. 6.3 Illustrations of Bi-Orthogonal codes. (**a**) An 8-bit orthogonal code has 8 orthogonal codes and (**b**) 8-antipodal codes for a total of 16 bi-orthogonal codes

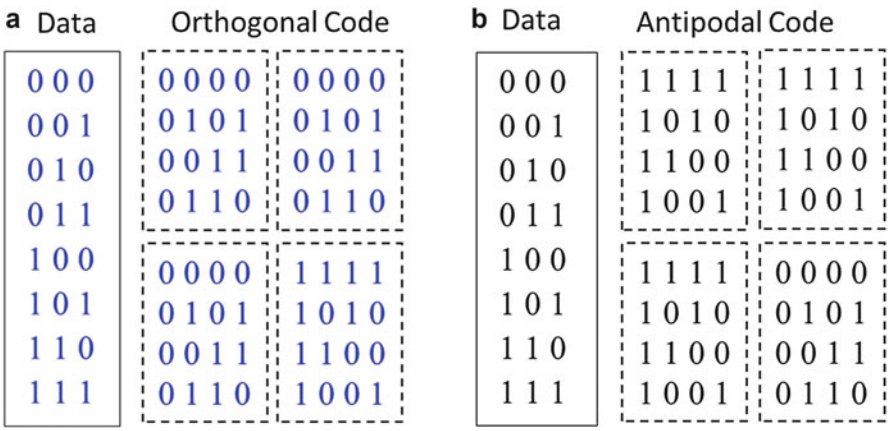


Fig. 6.4 Illustration of data mapping. (**a**) A 3-bit dataset is mapped into a block of 8-bit orthogonal code set. (**b**) A 3-bit data set is mapped into an 8-bit antipodal code set

that there are equal number of 1's and 0's in orthogonal and antipodal codes (except all 0's and all 1's) and that the distance between two orthogonal codes is n/2, where n is the code length. For example, for the 8-bit orthogonal code as shown in the figure has 4 zeros and 4 ones. This distance property offers a mechanism to detect and correct errors in data communications. This is governed by the following encoding and decoding process:

ENCODING [See Fig. 6.4]:

- A k-bit data-set is mapped into 2n Bi-Orthogonal codes, where n is the code length.
- This is similar to (n, k) block coding.
- Code Rate is given by $r = k/n$.
- For example: if $k = 3$, and $n = 8$, then $r = 3/8$ See Fig. 6.4.

DECODING:

The decoding is a correlation process. At the receiver the incoming code is compared with the code block for possible match. This mechanism offers error detection and correction as we shall see later in the following section. It will be shown that the number of errors that can be corrected in this process is given by $t = (n/4) - 1$, where n is the code length. Therefore the minimum code length that can be used is 8. The error correction capability increases as the code length increases. We will show that orthogonal codes offer PDMA with bandwidth efficiency.

6.2.2 Cross-Correlation Properties of Orthogonal Codes

A pair of codes are said to be orthogonal if the cross-correlation is zero. For two m-bit codes:

- $x_1, x_2, \ldots, x_m$ and
- $y_1, y_2, \ldots, y_m$,

The cross-correlation is given by the following equation:

$$R_{xy}(0) = \sum_{i=1}^{m} x_i y_i = 0 \tag{6.1}$$

It follows that an n-bit orthogonal code has n/2 1's and n/2 0's; i.e., there are n/2 positions where 1's and 0's differ [1–5]. Similarly, an n-bit antipodal code has n/2 1's and n/2 0's; i.e., there are n/2 positions where 1's and 0's differ. Therefore, the distance between two orthogonal codes is also n/2. For n = 8, these properties can be directly verified from Fig. 6.1 where the distance between any orthogonal code is 8/2 = 4 while the distance between an orthogonal code and an antipodal code is 8. This distance property can be used as a method of error control, as presented in the following sections.

6.2.3 *Error control Properties of Orthogonal Codes*

An n-bit orthogonal code has n/2 1 s and n/2 0 s; i.e., there are n/2 positions where 1 s and 0 s differ. Therefore, the distance between two orthogonal codes is d = n/2. This distance property can be used to detect an impaired received code by setting a threshold midway between two orthogonal codes as shown in Fig. 6.5, where the received coded is shown as a dotted line. This is given by:

$$d_{th} = \frac{n}{4} \tag{6.2}$$

Where n is the code length and dth is the threshold, which is midway between two valid orthogonal codes. Therefore, for the given 8-bit orthogonal code, we have

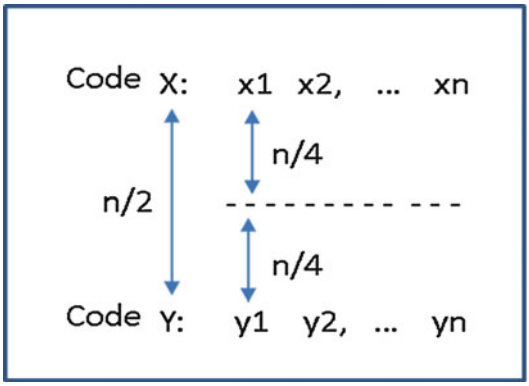


Fig. 6.5 Illustration of code correlation

Table 6.1 Orthogonal codes and the corresponding chip error control capabilities

n	t
8	1
16	3
32	7
64	15
:	:

$d_{th} = 8/4 = 2$. This mechanism offers a decision process, where the incoming impaired orthogonal code is examined for correlation with the neighboring codes for a possible match.

The received code is examined for correlation with the neighboring codes for a possible match. The acceptance criterion for a valid code is that an n-bit comparison must yield a good auto-correlation value; otherwise, a false detection will occur. The following correlation process governs this, where an impaired orthogonal code is compared with a pair of n-bit orthogonal codes to yield [2–5],

$$R(x, y) = \sum_{i=1}^{n} x_i y_i \leq d_{th} - 1 \tag{6.3}$$

Where R(x,y) is the auto correlation function, n is the code length, d_{th} is the threshold as defined earlier. Since the threshold is in the midway between two valid codes. An additional 1-bit offset is provided in the above equation to avoid ambiguity. The average number of errors that can be corrected by means of this process can be estimated by combining Eqs. (6.2) and (6.3), yielding, [3–5]:

$$t = R(x, y) = \frac{n}{4} - 1 \tag{6.4}$$

In Eq. (6.4), t is the number of errors that can be corrected by means of an n-bit orthogonal code. For example, an 8-bit orthogonal code can correct one error. Similarly, a 16-bit orthogonal code can correct three errors etc. (Table 6.1).

6.3 Multiple User PDMA

6.3.1 Construction of PDMA2

A PDMA2, supporting two users with n = 8, can be constructed by mapping 3 bits per user with an eight bit orthogonal (antipodal) code as shown in Fig. 6.6.

According to the communication protocol, the serial bit streams from each user, is serial to parallel converted into three bit streams (1:3 demultiplexed). The output bit rate, now reduced in speed by a factor of 3, is used to address $2^3 = 8$ eight-bit orthogonal (antipodal code). These codes are stored in two 8×8 ROMs. The output

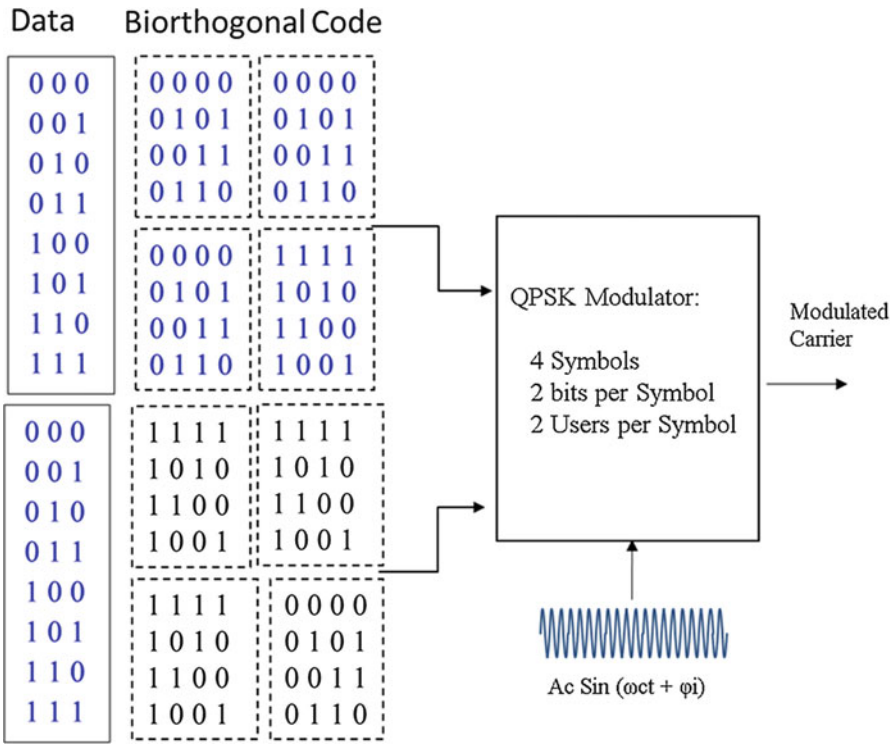


Fig. 6.6 Construction of PDMA2 based on QPSK modulator with n = 8. There are four phases or four symbols, Each symbol represents two code bits, one from each code. Therefore, a QPSK modulator can support two users

of each ROM is a unique eight-bit orthogonal code, which is then modulated by a QPSK modulator and transmitted through a channel, where the modulated waveform is in orthogonal space.

In the QPSK signal constellation, there are four symbols; each symbol represents two code bits, one bit per code. Therefore QPSK can support 2 users (N = 2) as shown below:

$$N = \frac{Log(4)}{Log(2)} = 2 \tag{6.5}$$

Since there are two orthogonal waveforms, the number of errors (t) that can be corrected is given by t = 2 [(n/4)−1] = 2, where n = 8 is the code length.

6.3.2 *Construction of PDMA4*

A PDMA4, supporting four users with n = 8, can be constructed by mapping two bits per user with an eight bit orthogonal (antipodal) code as shown in Fig. 6.7. According to the communication protocol, the serial bit streams from each user, is serial to parallel converted into two bit streams (1:2 demultiplexed). The output bit rate, now reduced in speed by a factor of two, is used to address $2^2 = 4$ eight-bit orthogonal (antipodal code). These codes are stored in four 4×8 ROM. The output of each ROM is a unique 8-bit orthogonal code, which is then modulated by a 16PSK modulator and transmitted through a channel, where the modulated waveform is in orthogonal space. In the 16PSK signal constellation, there are 16 symbols;

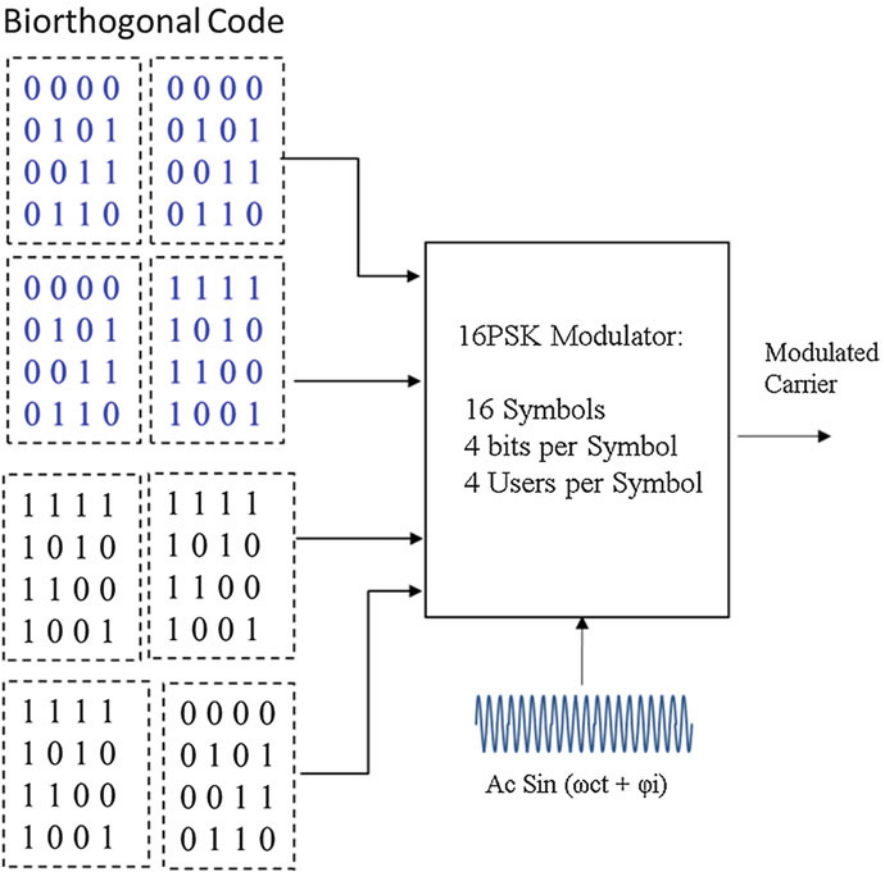


Fig. 6.7 Construction of PDMA4 based on QPSK modulator with n = 8. There are 16 phases or 16 symbols. Each symbol represents four code bits, one from each code. Therefore, a 16PSK modulator can support four users

each symbol represents four code bits, one bit per code. Therefore, a 16PSK modulator can support four users per symbol (N = 4) as shown below:

$$N = \frac{Log(16)}{Log(2)} = 4 \tag{6.6}$$

Since there are four orthogonal waveforms, the number of errors (t) that can be corrected is by t = 4 [(n/4)−1] = 4, where n = 8 is the code length. We also need to explore the possibility of using longer codes and higher order modulation schemes, such as 256 QAM and higher.

6.3.3 Hybrid TDMA-PDMA Structure

A hybrid TDMA-PDMA system with MPSK modulation, where M = 2, 4, 8, 16, . . ., can be constructed as shown in Fig. 6.8. Here, k-PDMA signals (k = 1, 2, 3, 4, . . .) are time shared and transmitted over a single carrier frequency. The total number of users per carrier is given by mk, where m is the number of users per symbol. For example, if:

- Number of users = 4
- Modulation scheme = 2^4 = 16 PSK
- Number of symbols = 16

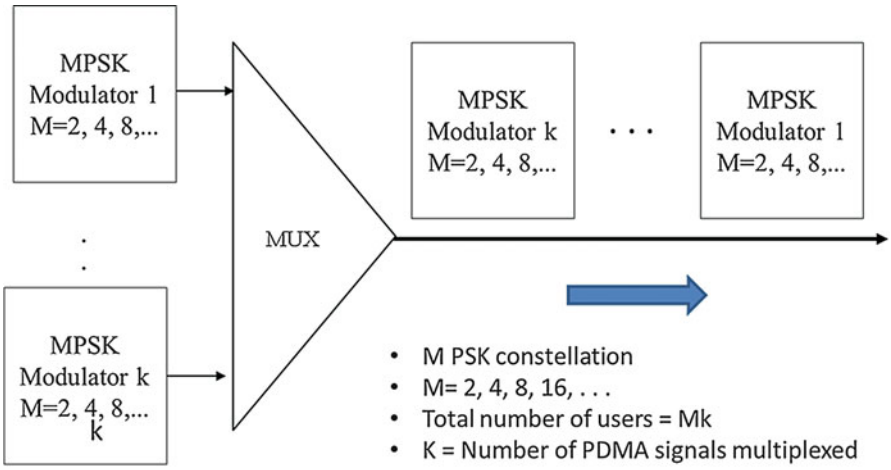


Fig. 6.8 Hybrid TDMA-PDMA. k PDMA signals are time shared in a single carrier frequency. Total number of users per carrier frequency is mk, where m is the number of users per symbol, which is determined by the MPSK modulator ($M = 2^m$, m=2, 4, 8, 16, . . .)

- Each symbol supports 4 users. 1 bit at a time
- Total number of users = 4 k

6.4 Ber Performance Analysis

We have established that an n-bit orthogonal code can correct t errors where t = (n/4) − 1. A measure of coding gain is then obtained by comparing the uncoded word error WER_U, to the coded word WER_C. We examine this by means of the following analytical means [6]:

With B PSK modulation, the Uncoded BER is given by:

$$BER_U = 0.5\text{Exp}(1 - E_b/2\,N_o) \tag{6.7}$$

The probability that the uncoded k-bit word (WER_U) will be received in error is 1 minus the product of the probabilities that each bit will be received correctly. Thus, we write:

$$WER_U = 1 - (1 - BER_U)^k \tag{6.8}$$

Since n > k, the coded bit energy to noise ratio will be modified to E_c/N_o.

Where

$Ec/N_o(dB) = E_b/N_o(dB) + 10\log(k/n)$. Therefore, the coded BERc will be:

$$BER_c = 0.5\text{Exp}(-E_c/2N_o) \tag{6.9}$$

The corresponding coded word error rate is:

$$WER_C = \sum_{k=t+1}^{n} \binom{n}{k} BER_C^K (1 - BER_C)^{n-k} \tag{6.10}$$

When $BER_c < 0.5$, the first term in the summation is the dominant one; therefore, Eq. (6.5) can be simplified as

$$WER_C \approx \binom{n}{k} BER_c^k (1 - BER_c)^{n-k} \tag{6.11}$$

Using n = 8, 16 and 64, we obtain the coded and the uncoded WER as shown in Fig. 6.9. Coding gain is the difference in Eb/No between the uncoded and the coded word error. Notice that at least 3–4 dB coding gain is available in this example.

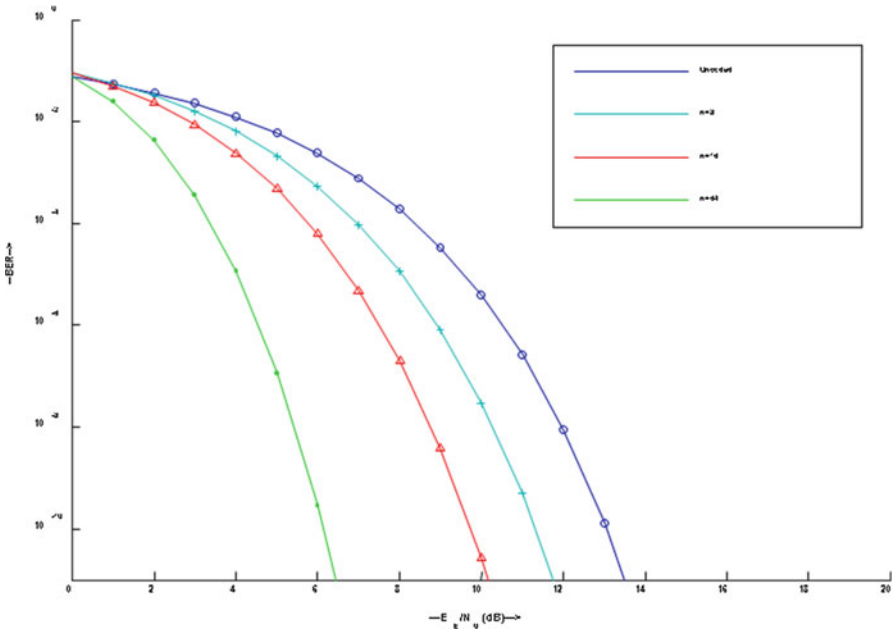


Fig. 6.9 BER performance

Problem 6.1

Given:

- 16 bit orthogonal code
- Number of users = 2

Find:

- Number of errors that can be corrected by a 16 bit orthogonal code
- A suitable PDMA structure to support two simultaneous users

Solution:

(a) A 16 bit orthogonal code has:

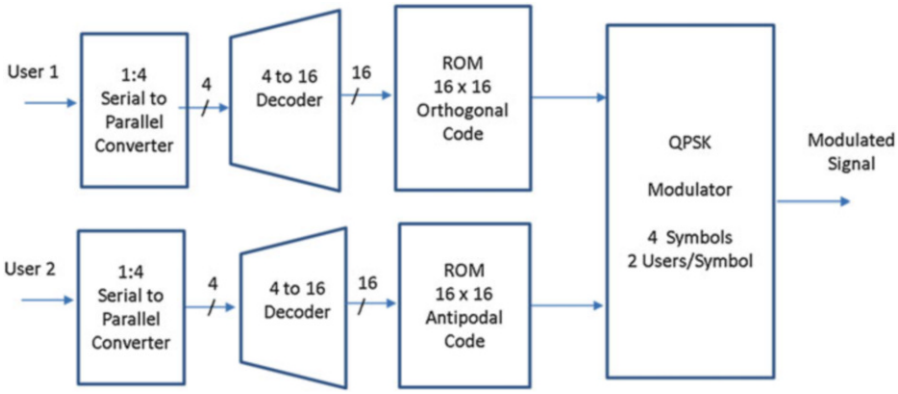
- 16 Orthogonal codes and
- 16 Antipodal codes
- Number Of Biorthogonal codes = 32

Therefore, the number of errors that can be corrected is given by:

$$t = n/4 - 1 = 16/4 - 1 = 3$$

(b) Since there are two users and we have 16 orthogonal codes and 16 antipodal codes, we can assign 16 orthogonal codes to user 1 and 16 antipodal codes to user 2. See figure below. The circuit can be designed as follows:

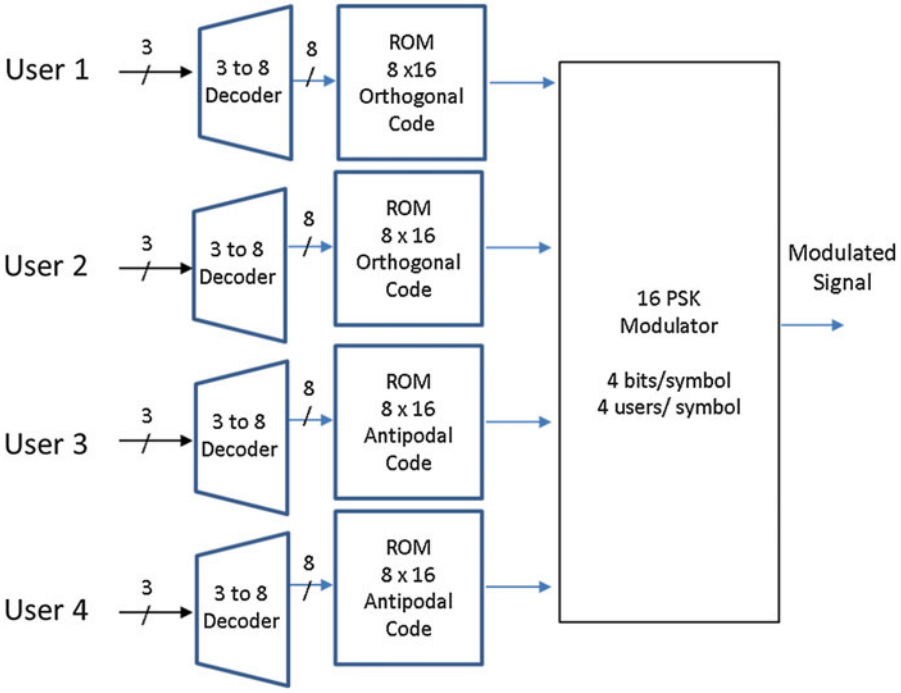
- The incoming data from each user is serial to parallel converted into four parallel streams. These four parallel bit streams are the address bit of the 4:16 decoder. Therefore, depending on the address bit, one of 16 outputs of each decoder is enabled to address the 16×16 ROM.
- The output of each ROM is a unique 16 bit orthogonal or antipodal code. These pair of codes is then used to modulate the QPSK modulator, having four symbols (four phases), two bits per symbol, one bit from each user.
- Therefore, there are two users/symbol



Problem 6.2
Consider the previous problem again and construct a suitable PDMA structure to support four users.

Solution:
Since there are four users and we have 16 orthogonal codes and 16 antipodal codes, we can assign 16 orthogonal codes to two users and 16 antipodal codes to two users. See figure below for illustrations. The circuit can be designed as follows:

- The incoming data from each user is serial to parallel converted into three parallel streams. These three parallel bit streams are the address bit of the 3:8 decoder. Therefore, depending on the address bit, one of eight outputs of each decoder is enabled to address the 8×16 ROM.
- The output of each ROM is a unique 16 bit orthogonal or antipodal code. These four output codes are then used to modulate the 16PSK modulator, having 16 symbols (16 phases), 4 bits per symbol, 1 bit from each user.
- Therefore, there are four users/symbol



6.5 Conclusions

- A method of phase division multiple access (PDMA) is presented.
- In the proposed technique, multiple users have access to the same carrier frequency through the phase constellation of M PSK modulation.
- Construction of PDMA2 and PDMA4 are presented to illustrate the concept.
- It is also shown that orthogonal codes play an important role in detecting and correcting multiple errors.
- The proposed PDMA utilizes a block of bi-orthogonal code to map a block of data from multiple users. The transmission protocol is such that, when a block of data needs to be transmitted, the corresponding block of bi-orthogonal code is transmitted by means of MPSK modulator, where each symbol supports multiple users, one bit at a time.
- At the receiver, the data is recovered by means of code correlation.

- We have examined the distance properties of orthogonal codes and have shown that orthogonal codes can be used to detect and correct errors with bandwidth efficiency.
- A hybrid-TDMA-PDMA scheme is also developed to improve spectrum usage.
- We have also presented BER Performance of PDMA.

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Appendix A

Fourier Series

Fourier series is a mathematical function that applies to periodic signals. It states that, a continuous time periodic signal contains an infinite number of harmonically related sinusoidal waveforms. Fourier showed that, if the function f(t) is periodic, then it can be represented by an infinite series as given below:

$$f(t) = \frac{a_0}{2} + a_1 \cos(\omega_0 t) + a_2 \cos(2\omega_0 t) + \ldots + b_1 \sin(\omega_0 t) + b_2 \sin(2\omega_0 t) + \ldots \tag{A.1}$$

Or more conveniently as:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left\{ \left(a_n \cos(n\omega_0 t) + \left(b_n \sin\left(n\omega_0 t\right)\right\}\right. \tag{A.2}$$

Here,

$$\omega_0 = 2\pi \mathrm{f} = 2\pi/\mathrm{T}$$

The Objective is to Determine Fourier Coefficients: a's and b's. Here is the step-by-step process:

S. Faruque, *Radio Frequency Source Coding Made Easy*, SpringerBriefs
in Electrical and Computer Engineering, DOI 10.1007/978-3-319-15609-5

Step 1: Determine a_0

The Fourier coefficient a_0 can be determined by integrating the Fourier series over T:

$$\int_0^T f(t)dt = \int_0^T \frac{a_0}{2}\,dt + \sum_{n=1}^{\infty} \int_0^T \left\{ \left(a_n \cos\left(n\omega_0 t\right) + \left(b_n \sin\left(n\omega_0 t\right)\right\}dt \right. \right. \tag{A.3}$$

Next, we use the following formula:

$$\int_0^T \cos\left(n\omega t + \alpha\right)dt = 0 \quad \int_0^T \sin\left(n\omega t + \alpha\right)dt = 0 \quad (\omega = 2\pi/\mathrm{T}) \tag{A.4}$$

Therefore every term in the summation is ZERO and we have

$$\begin{aligned} &\int_0^T f(t)dt = \int_0^T \frac{a_0}{2}\,dt = \frac{a_0}{2}\int_0^T dt = \frac{a_0}{2}T \\ &\therefore a_0 = \frac{2}{T}\int_0^T f(t)dt \end{aligned} \tag{A.5}$$

Therefore, by knowing the function f(t), the Fourier coefficient a_0 can be determined by using Eq. (A.5)

Step 2: Determine a_n

Determine the Fourier coefficient a_n by multiplying both sides of Eq. (A.2) by $\{\cos(n\omega_0 t)\}$, where n is an integer and Integrate:

$$\begin{aligned} \int_0^T f(t)\cos\left(n\omega_0 t\right)dt = &\int_0^T \frac{a_0}{2}\cos\left(n\omega_0 t\right)dt \\ &+ \sum_{n=1}^{\infty} a_n \int_0^T \left\{ \left(\cos\left(n\omega_0 t\right)\cos\left(n\omega_0 t\right)dt\right\} \right. \\ &+ \sum_{n=1}^{\infty} b_n \int_0^T \left\{ \left(\cos\left(n\omega_0 t\right)\sin\left(n\omega_0 t\right)dt\right\} \right. \end{aligned} \tag{A.6}$$

Using the following formula:

$$\int_0^T \cos(n\omega t + \alpha)dt = 0, \quad \int_0^T \sin(n\omega t + \alpha)dt = 0,$$
$$\int_0^T \cos(n\omega t + \alpha)\sin(n\omega t + \alpha)dt = 0 \tag{A.7}$$
$$\int_0^T \cos(n\omega t + \alpha)\cos(n\omega t + \beta)dt \neq 0$$

We obtain:

$$\int_0^T f(t)\cos(n\omega_0 t)dt = a_n \int_0^T \cos^2(n\omega_0 t)dt$$
$$= a_n \frac{\pi}{\omega_0} = a_n \frac{T}{2} (T = 2\pi/\omega)$$

Solving for a_n:

$$a_n = \frac{2}{T}\int_0^T f(t)\cos(n\omega_0 t)dt \quad n = 1, 2, 3, \ldots \ldots \ldots \ldots \tag{A.8}$$

Formula:

$$\int_0^T \cos^2(\omega t + \alpha)dt = \frac{\pi}{\omega}$$
$$\mathrm{T} = 2\pi/\omega$$

Eq. (A.8) is the solution for a_n

Step 3: Determine b_n

Determine the Fourier Coefficient bn by multiplying both sides of Eq. (A.2) by {sin ($n\omega_0 t$)}, where n is an integer and Integrate:

Using the same procedure as before, we obtain:

$$b_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega_0 t)dt \quad n = 1, 2, 3 \ldots \ldots \ldots \ldots \tag{A.9}$$

Formula:

$$\int_0^T \sin^2(\omega t + \alpha)dt = \frac{\pi}{\omega}$$

$$\mathrm{T} = 2\pi/\omega$$

Eq. (A.9) is the solution for b_n

Step 4: Substitute the Coefficients

Substitute the Fourier coefficients into the Fourier series given below:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left\{\left(a_n \cos(n\omega_0 t) + \left(b_n \sin(n\omega_0 t)\right\}\right.\right.$$

Summary

The Fourier series is given by:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left\{\left(a_n \cos(n\omega_0 t) + \left(b_n \sin(n\omega_0 t)\right\}\right.\right.$$

Fourier coefficients are given by:

$$a_0 = \frac{2}{T}\int_0^T f(t)dt$$

$$a_n = \frac{2}{T}\int_0^T f(t)\cos(n\omega_0 t)dt \quad n = 1, 2, 3, \ldots$$

$$b_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega_0 t)dt \quad n = 1, 2, 3, \ldots$$

Guidelines to Find Fourier Spectrum

- Determine the Coefficient

$$a_0 = \frac{2}{T}\int_0^T f(t)dt$$

$$a_n = \frac{2}{T}\int_0^T f(t)\cos(n\omega_0 t)dt$$

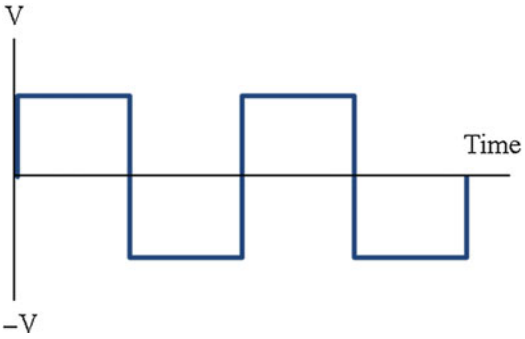
$$b_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega_0 t)dt$$

$$n = 1, 2, 3, \ldots$$

- Substitute the coefficient into the Fourier Series

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left\{\left(a_n\cos(n\omega_0 t) + \left(b_n\sin(n\omega_0 t)\right\}\right.\right.$$

Problem: Square Wave



Given:

$$\begin{aligned} f(t) &= V \quad 0 < t < 1 \\ &= -V \quad 1 < t < 2 \\ f(t) &= f(t+2) \end{aligned}$$

Find the Fourier series

Solution to Problem-1

Step 1: Find a_0:

$$\begin{aligned} f(t) &= V \quad 0 < t < 1 \\ &= -V \quad 1 < t < 2 \\ \omega_0 &= \pi \quad T = 2 \end{aligned}$$

Since $f(t) = f(t+2)$, We have:

$$\begin{aligned} T &= 2 \\ \omega_0 &= 2\pi/T = 2\pi/2 = \pi \end{aligned} \tag{A.10}$$

Therefore, the coefficient a_0 can be determined as:

$$\begin{aligned} a_0 &= \frac{2}{T}\int_0^T f(t)dt = \frac{2}{2}\left[\int_0^1 V dt + \int_1^2 -V dt\right] \\ &= Vt|_0^1 - Vt|_1^2 = V(1-0) - V(2-1) = V - V = 0 \\ &\therefore a_0 = 0 \end{aligned}$$

Step 2: Find a_n:

$$\begin{aligned} f(t) &= V \quad 0 < t < 1 \\ &= -V \quad 1 < t < 2 \\ \omega_0 &= \pi \quad T = 2 \end{aligned}$$

$$\begin{aligned} a_n &= \frac{2}{T}\int_0^T f(t)\cos\ n\omega_0 t dt \\ &= \frac{2}{2}\left[\int_0^1 V\cos\ n\pi t dt - \int_1^2 V\cos\ n\pi t dt\right] \\ &= V\frac{\sin n\pi t}{n\pi}\Big|_0^1 - V\frac{\sin n\pi t}{n\pi}\Big|_1^2 \\ &= \frac{V}{n\pi}\left[\sin n\pi t\Big|_0^1 - \sin n\pi t\Big|_1^2\right] = 0 \\ &\therefore a_n = 0 \end{aligned}$$

Step 3: Find b_n:

$$\begin{aligned} f(t) &= V \quad 0 < t < 1 \\ &= -V \quad 1 < t < 2 \\ \omega_0 &= \pi \quad T = 2 \end{aligned}$$

$$b_n = \frac{2}{T}\int_0^T f(t)\sin n\omega_0 t dt$$

$$= \frac{2}{2}\left[\int_0^1 V\sin n\pi t dt - \int_1^2 V\sin n\pi t dt\right]$$

$$= -V\frac{\cos n\pi t}{n\pi}\Big|_0^1 + V\frac{\cos n\pi t}{n\pi}\Big|_1^2$$

$$= -\frac{V}{n\pi}\left[\cos n\pi t\Big|_0^1 - \cos n\pi t\Big|_1^2\right]$$

$$b_n = -\frac{V}{n\pi}[(\cos n\pi - 1) - (\cos 2n\pi - \cos n\pi)]$$

$$= -\frac{4}{n\pi}[2\cos n\pi - \cos 2n\pi - 1] = \frac{4V}{n\pi}(n = 1, 3, \ldots)$$

$$= 0(n = 2, 4, \ldots.)$$

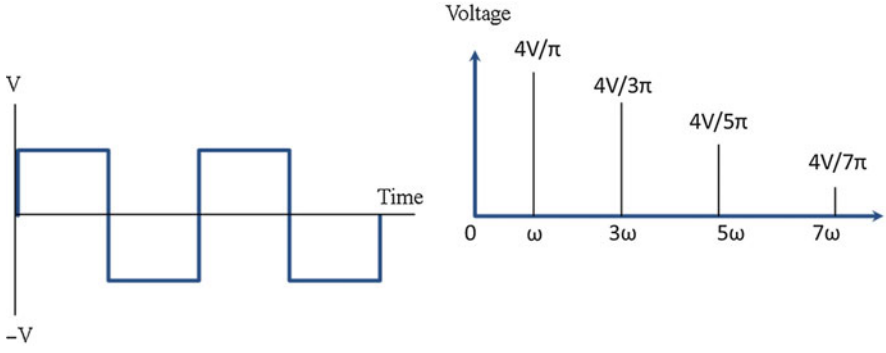
$$\therefore b_n = \frac{4V}{n\pi}$$

Step 4: Substitute a_0, a_n and b_n into the Fourier series f(t):

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}\{(a_n\cos(n\omega_0 t) + (b_n\sin(n\omega_0 t)\}$$

$$= 0 + \sum_{n=1}^{\infty} 0 + \frac{4V}{n\pi}\text{sign}(n\omega_0 t)$$

$$= \frac{4V}{n\pi}\sum\nolimits_{n=1}^{\infty}\frac{1}{n}\text{sign}(n\omega_0 t) \quad n = 1, 3, 5, \ldots\ldots\ldots\text{ZX}$$

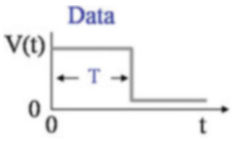


Appendix B

Fourier Transform

Fourier transform is a mathematical function that applies to non-periodic signals. It states that, a discrete time non-periodic signal contains an infinite number of harmonically related sinusoidal waveforms. Fourier showed that, if the function f (t) is non-periodic, then it can be represented in two ways:

- Time domain representation:
  $V(t) = V \quad < 0 < \mathrm{t} < \mathrm{T}$
  $= 0 \quad$ elsewhere



- Frequency domain representation: "Fourier Transform"

$$V(\omega) = \int_0^T V \cdot e^{-j\omega t} dt$$

The above frequency domain expression can be expanded to obtain an infinite number of harmonically related sinusoidal waveform as follows:

S. Faruque, *Radio Frequency Source Coding Made Easy*, SpringerBriefs
in Electrical and Computer Engineering, DOI 10.1007/978-3-319-15609-5

$$V(\omega) = \int_0^T V \cdot e^{-j\omega t} dt = \left(\frac{V}{-j\omega}\right) \left| e^{-j\omega t} \right|_0^T$$
$$= \left(\frac{V}{-j\omega}\right) [e^{-j\omega T} - 1] = \left(\frac{V}{j\omega}\right) [1 - e^{-j\omega T}]$$

Now use the following trigonometric identity:

$$e^{j\omega T} = Cos(\omega T) + jSin(\omega T)$$

and evaluate V(ω), which is given by:

$$V(\omega) = \left(\frac{V}{j\omega}\right) [1 - Cos(\omega T) + jSin(\omega T)]$$
$$|V(\omega)| = \left(\frac{V}{\omega}\right) \sqrt{\{1 - Cos(\omega T)\}^2 + Sin^2(\omega T)}$$
$$NOTE:$$
$$In\, complex\, Variable\, Magnitude = \sqrt{(Real)^2 + (Imaginary)^2}$$

Now, use trigonometry and some manipulation to obtain:

$$|V(\omega)| = 2\left(\frac{V}{\omega}\right) Sin\left(\frac{\omega T}{2}\right) = VT\left[\frac{Sin\,(\omega T/2)}{\omega T/2}\right]$$

This is the magnitude of the voltage waveform as a function of angular frequency Where,

ω = 2πf
f = Frequency of the sinusoidal wave
T = Period of the clock ($1/f_c$)
f_c = Clock frequency

Power Spectrum

Power spectrum associated with the signal is given by:

$$P(\omega) = \left(\frac{1}{T}\right) |V(\omega)|^2 = V^2 T\left[\frac{Sin\,(\omega T/2)}{\omega T/2}\right]^2$$

where

$$|V(\omega)| = VT\left[\frac{Sin\,(\omega T/2)}{\omega T/2}\right]$$

Where,

- V(t) = Voltage, which is a function of time
- T = Period

The power spectrum has an infinite number of harmonically related components

General Expression for Two Sided Response

A more general equation (Two Sided) is:

$$V(\omega) = \int_{-\infty}^{\infty} V(t) \cdot e^{-j\omega t} dt$$

In this case, V(ω) is called two sided spectrum of V(t). This is due to both positive and negative frequencies used in the integral. The function can be a voltage or a current.