Chapter 11
Radiation Effects in 65 nm Flash-Based Field Programmable Gate Array

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11.1 Introduction

Since it was first introduced, Flash-based FPGA had been well received by digital designers in aerospace and high-reliability applications. Its popularity owes to, unlike other commercially available FPGA based on antifuse or SRAM technologies, that the Flash-based FPGA has the unique advantage of being both non-volatile and reprogrammable. It is advantageous to antifuse-based for programmability and to SRAM-based for non-volatility. This characteristic warrantees small foot-print and resiliency in hazardous operating environment, especially against bit-errors by particle radiations.

Its development has been successfully following footsteps of continuously scaled CMOS technologies. Architecturally the first product, 0.25 μm ProASIC, is simple. It has tiles of user logic and embedded-SRAM blocks which have dual usage either as two-port SRAM or FIFO. The second product, 0.22 μm ProASIC^{PLUS}, is an improved ProASIC with similar capability. The third product, 130 nm ProASIC3, has many new and advanced features and it quickly replaces the previous FPGAs as the main force to present day. The most significant improvement in ProASIC3 is using standard digital-CMOS power supply of 3.3 VDC to perform the in-system programming. This is achieved by integrating a charge pump to provide high voltage on-chip for the programming. Also, the derived siblings, Igloo, Fusion, and SmartFusion1, have special features of low-power operation, and embedded Intellectual Properties (IPs) to provide wide spectrum of functions [1]. The introduction of SmartFusion1 is a significant milestone because it is the first Flash-based

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FPGA to be also an SOC. Indeed, it has and embedded hard-wired ARM Cotex-1 microcontroller to enable the full function of a digital system.

Radiation-induced TID effects in Flash-based FPGA have been studied by research groups [2–9]. These TID effects include Flash cell V_T shift, propagation delay degradation, power-supply current increase, FPGA function failure, and programming failure. In general, all radiation-induced changes of parameters can be related to known physical mechanisms: charge loss/gain in floating gate of irradiated Flash cell, which can cause threshold-voltage shift [10]; leakage current increase, timing skew and functional failures in CMOS transistors [11, 12].

The studies on single event effects (SEE) of Flash-based FPGA are abundant [13–21], especially on heavy-ion induced single event transients (SET) in 130 nm Flash-based FPGA. Even an SET-mitigation software package is available for ProASIC3 users [19]. Beside the practical usage reason, there is a valid motivation studying SET by using Flash-based FPGAs: first the continuing decreasing transistor sizes exacerbates the SET effects; second using Flash-based FPGA to study SET is very convenient because it is reprogrammable but doesn't have radiation-induced configuration upset which will plague the operation of SRAM-based FPGA.

This chapter will focus on the radiation effects in 65 nm Flash-based FPGA-SOC: The characteristics of this new Flash-based FPGA will be introduced; similarities and differences between the Flash cell used in FPGA and Memory applications will be highlighted; radiation tests results showing TID and SEE effects will be presented and discussed. Qualitative models will be constructed to elucidate how the physical mechanisms caused the observed radiation effects. Based on test data, single event upsets on the Flash configuration cell, fabric flip-flop, and fabric SRAMs are evaluated. A novel 3D-TCAD simulation generated SEU cross-sections on fabric FF will be compared with the test data, and its usefulness in the future will be contemplated.

11.2 Flash Configuration Cell

The Flash memory technology, meaning floating-gate (FG) technology here, had been studied and published extensively in recent years. The motivation mainly was driven by enormous commercial activities. Relevant knowledge such as device physics, circuit design, programming system operation, and reliability can be found in review literatures (e.g. see reference [22]). In this section, the Flash configuration cell in FPGA will be introduced and its references to Flash memory are often made.

The Flash configuration cell has similarities and differences when compared to a Flash memory cell. Like a memory cell, it also uses floating-gate NMOS transistor as the basic device to enable non-volatility. The physical mechanisms, in Write mode, for both Program and Erase action, are the well-known channel Fowler-Nordheim tunneling. However, its geometry is significantly different from that of a memory cell: the Flash cell enabling configuring, named "sense" device, combines with a Flash cell gating critical signals, named "switch" device, to form a twin

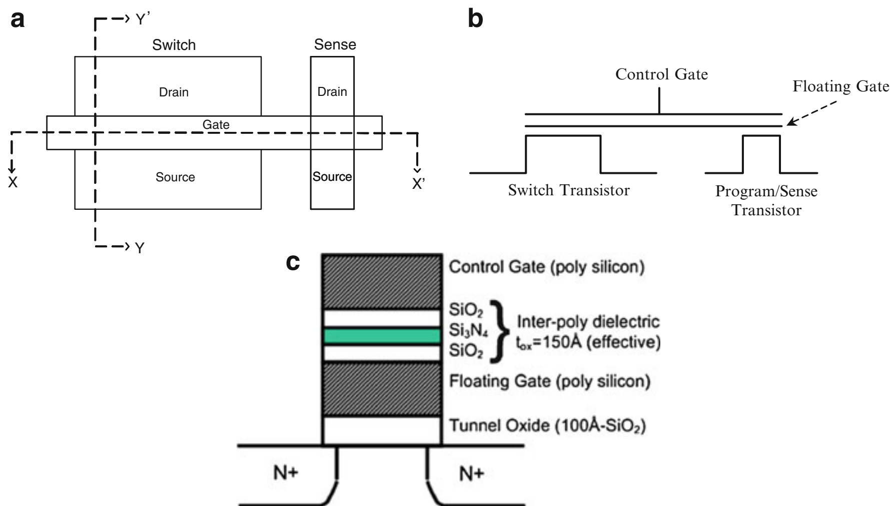


Fig. 11.1 (**a**) Layout of the Flash cell: each cell contains one switch and one sense FG transistor; the control gate and FG are shared by both the switch and sense transistor. (**b**) Schematic showing the cross-section of X-X′ cut. (**c**) Schematic showing the cross-section of Y-Y′ cut

structure shown in Fig. 11.1. The floating and control gate are shared by sense and switch devices. Note that the switch is the wider one for ease passing of signals.

When a Flash-based FPGA is used in a system, during configuration programming and testing Write/Read is performed through the sense device, and during normal operation Read is performed on the switch device. Figure 11.2 depicts a 2×2 array of Flash configuration cells to illustrate these actions. It also shows that by using the sense-switch construct in a single cell greatly simplifies the design enabling the FPGA operation while leaves the implementation of the Flash technology very much the same as that of the Flash memory. Indeed, the sense devices are arranged exactly the same as a typical NOR-Flash memory. The reason of using NOR architecture is that FPGA is performing normal operation function by reading code stored in Flash cell in executed-in-place (XIP) mode. The drawback is that, in radiation environments, NOR-Flash is more sensitive to TID effects than NAND [23].

Similar to Flash-memory operation, Write action programs the Flash-configuration cell into one of the state of Erase or Program. The FG transistor of a cell at the Erase state has a low threshold voltage (V_t) and at Program state high V_t. Note that the V_t measurement in Flash-configuration cell can be performed on either sense or switch device. Another difference, in FPGA the FG at Erase state is in the depletion mode (Fig. 11.3) while in memory it is usually not programming Erase-state into depletion mode.

Finally, during normal operation switch device at Erase state is the On-state passing signals and Program state the Off-state isolating logic circuits from adverse effects during operation. To pass robust signal, the switch device is designed to have a large enough width and this makes the total area of a Flash-configuration cell

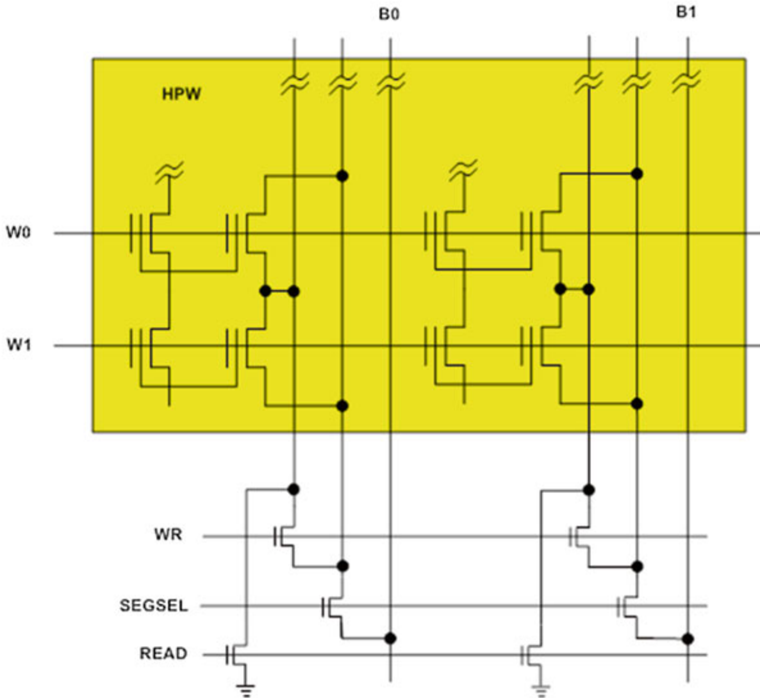


Fig. 11.2 Schematic of a 2×2 flash-cell array shows sense transistors arranged in typical NOR Flash-memory architecture

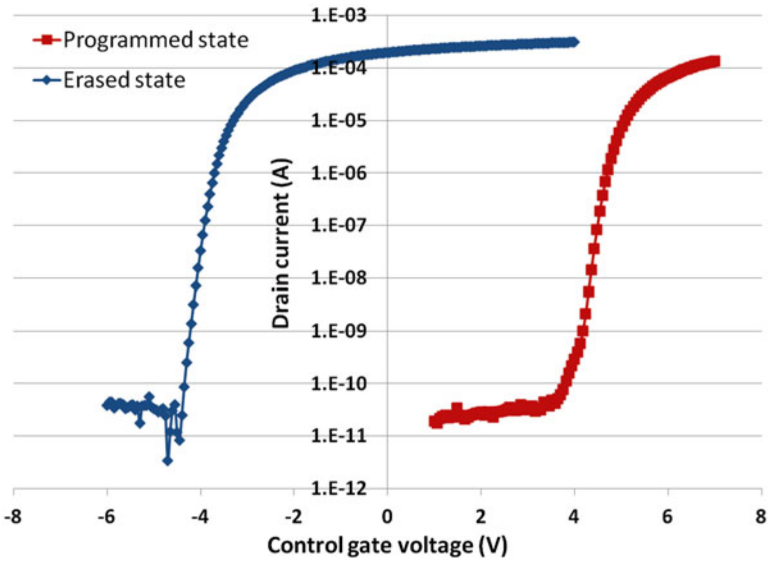


Fig. 11.3 Id-Vg plot of typical Program state and Erase state of a Flash configuration cell in 65 nm Flash-based FPGA

large, approximately 35 μm^2 in area, and significant larger than that of a Flash-memory cell. This area difference will be reflected in the difference between their radiation effects to be discussed in the following sections.

11.3 Radiation Testing

A device in SmartFusion2 family, coded M2S050, was radiation tested for total ionizing dose (TID) effects and single event effects (SEE). It is true silicon-on-chip (SOC) device manufactured by United Microelectronics Corporation (UMC) using 65 nm wafer-fabrication technologies. Figure 11.4 shows its floor plan indicating the location of each functional block. The device reliable Flash-based fabric logic and SRAM, and embedded with an ARM® Cortex™-M3 microprocessor together with instruction cache and advanced security processing accelerators, digital signal processing (DSP) blocks, eSRAM, eNVM, and industry-required high-performance communication interfaces. SmartFusion2 also differentiates itself from FPGAs using other configuring technologies by low power capabilities, high reliability and advanced security which is particularly important for military, aviation, communication and medical applications.

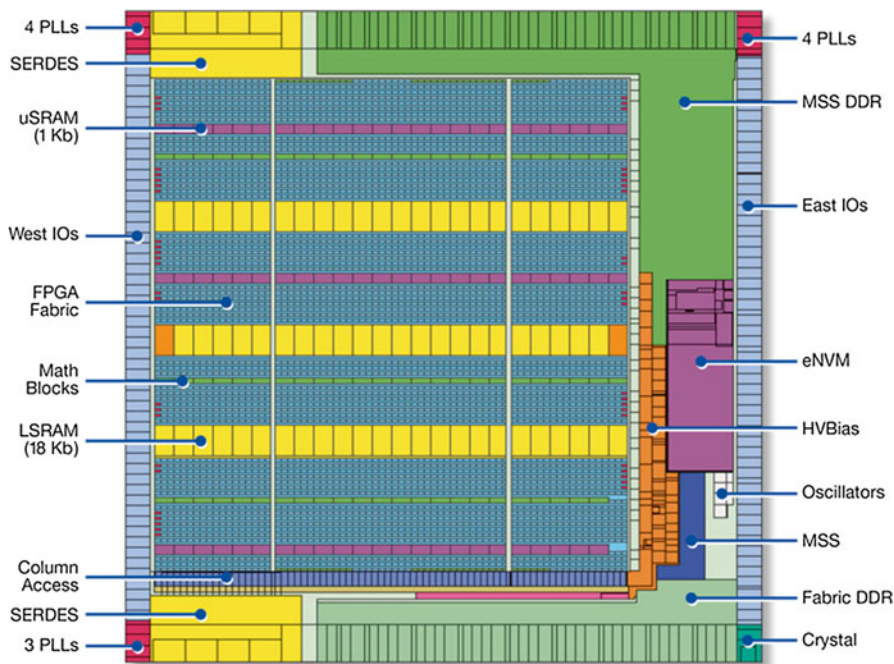


Fig. 11.4 Plot shows floor plan of M2S050 device and the location of each functional block

By no means can radiation effects, especially SEE, of an FPGA-SOC be completely tested at this moment. Here the focus is on the core configurable part of FPGA designed by Microsemi, which is often referred as fabric. The extra embedded IPs to make FPGA an SOC are hard-wired ASICs; their radiation tests, albeit very important, will be investigated in the future and not in the scope of this chapter.

SmartFusion2 family is not designed for applications operated in harsh radiation environments such as satellite operating in geosynchronous orbit. However, for moderate radiation environments, e.g. in particle accelerator, it can be very attractive for its non-volatile configuring ability and mild resistance to radiation effects.

Test dies with transistor level devices as well as FPGA dies are co-manufactured by wafer fabrication processes. Their purpose is to be tested standalone to facilitate the understanding of radiation effects at the transistor level, and subsequently helps to elucidate the radiation effects at the circuit and system levels.

11.3.1 Radiation Testing for TID Effects

The radiation testing performed on test chips was conducted at Vanderbilt University in Nashville, Tennessee, using ARACOR X-ray Irradiator. The testing on FPGA was at defense microelectronics activity (DMEA) in McClellan, California, using gamma ray irradiator. Both testing were performed at ambient temperature.

On the test chip, the Flash cell are programmed and tested by an Agilent 4156 controlled by a laptop PC. The CMOS transistors are tested using the same hardware/software. For propagation delay measurement, the design programmed in FPGA is a long inverter-string with 7,200 stages. Electrical data are recorded over the entire irradiation duration to finally more than 100 krad(SiO_2). The input signal is supplied from a function generator and waveforms of the input/output signals are observed and the propagation delay is recorded on the oscilloscope. The in-flux standby power-supply currents I_{DD} are monitored by an Agilent 6629 power supply and recorded by the laptop PC.

11.3.2 Radiation Testing for Single Event Effects

The test designs, illustrated in Fig. 11.5: shift registers consisted of various stages of configured fabric-flip-flops (FF) and fabric-SRAM blocks which include both μSRAM and LSRAM types. Figure 11.6 depicts a fabric Logic Element from which D-type FF with active low clear (DFN1C0) [24] is configured to be the testing target for SEU. The test setup is illustrated in Fig. 11.7 where the function of each subsystem is shown.

Heavy-ion irradiations were performed on FPGA and conducted at two facilities: 10 MeV/n cocktail beam [25] was used in vacuum at 88-inch Cyclotron facility of

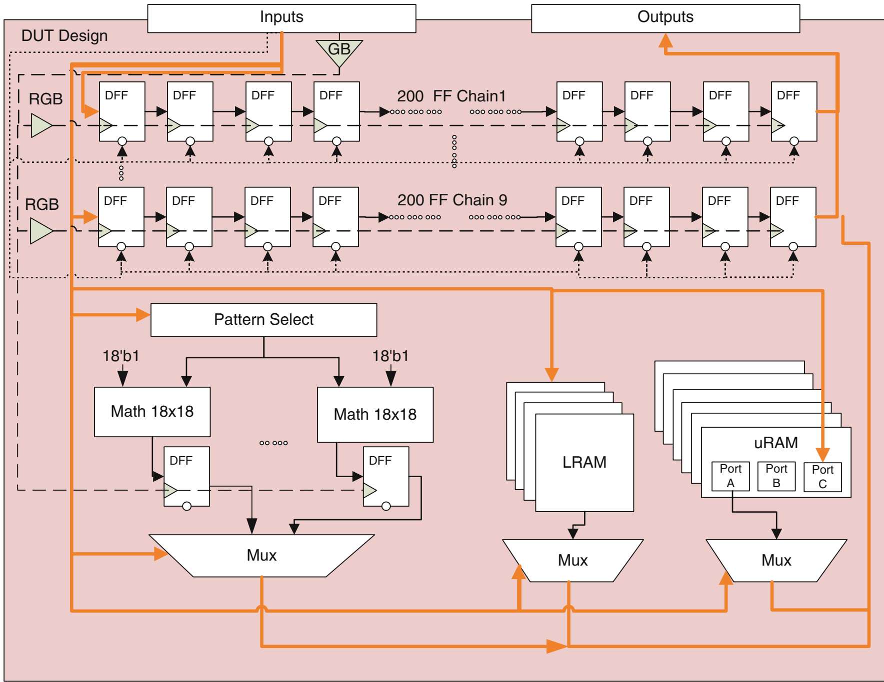


Fig. 11.5 Block diagram shows the FPGA design for radiation testing for SEU effects

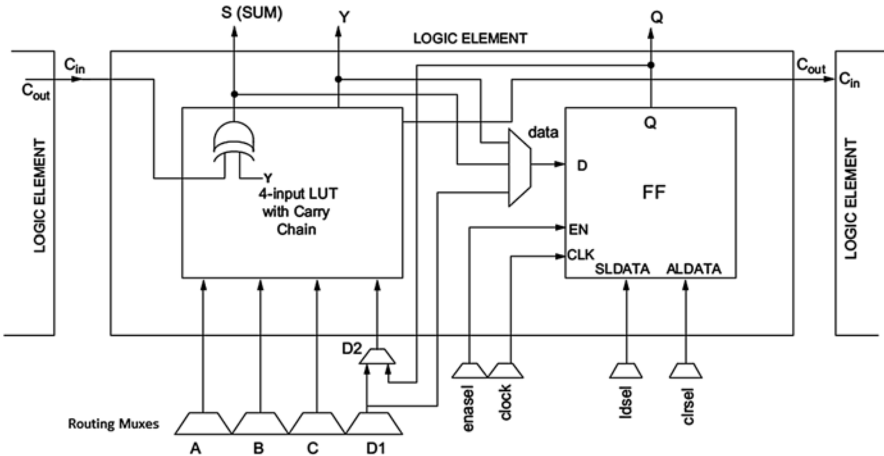


Fig. 11.6 Block diagram shows contents of Logic Element which includes FF, 4-input LUT and Routing-Mux connections [1]

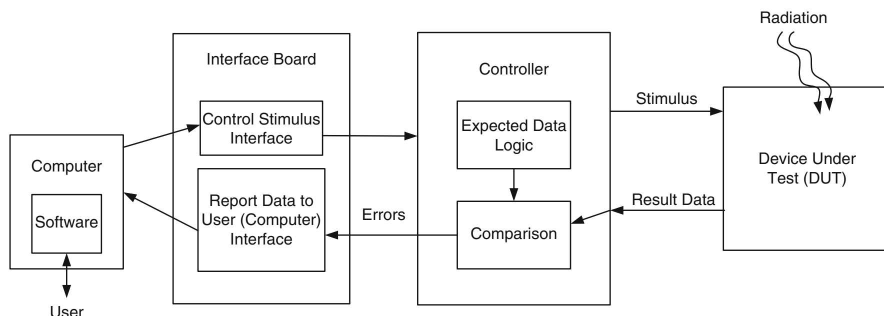


Fig. 11.7 Block diagram illustrates the SEE testing setup and data flow

Lawrence Berkeley National Laboratory in Berkeley, California; 15 MeV/n beam [26] was used in air at Cyclotron Center of Texas A&M University in College Station, Texas. For testing SEL effect, FPGA is biased to maximum operating voltages (nominal + 5 %) and tested at temperature up to 95 °C. Testing SEU effect is under nominal operating bias at ambient temperature.

11.4 Radiation Test Results on TID Effects

In this section the TID characteristics of the Flash cell and CMOS transistors used in FPGA will be presented, and followed by TID effects on two key FPGA electrical parameters which are propagation delay and standby power-supply current. It has been established that, in Flash-based FPGA [2–5], these two parameters determine the FPGA TID tolerance on the performance and power consumption. They degrade significantly before FPGA fails to function. These degradations owing to the ramification of Flash cell and transistor TID effects will also be discussed.

11.4.1 TID Effects on Flash Cells

In general TID effects on 65 nm Flash configuration cell are neutralizing the charge storage in the floating gate. As shown in Fig. 11.8, where both sense and switch device data are displayed, the Erase state V_t shifts to higher and Program state lower with TID. In principal these two states will finally neutralized by TID to a neutral state. However, the transistor effects will be strong at high dose level and render the V_t measurement impractical. The mechanisms responsible for these V_t shifts can be found in published literatures [2–5, 10].

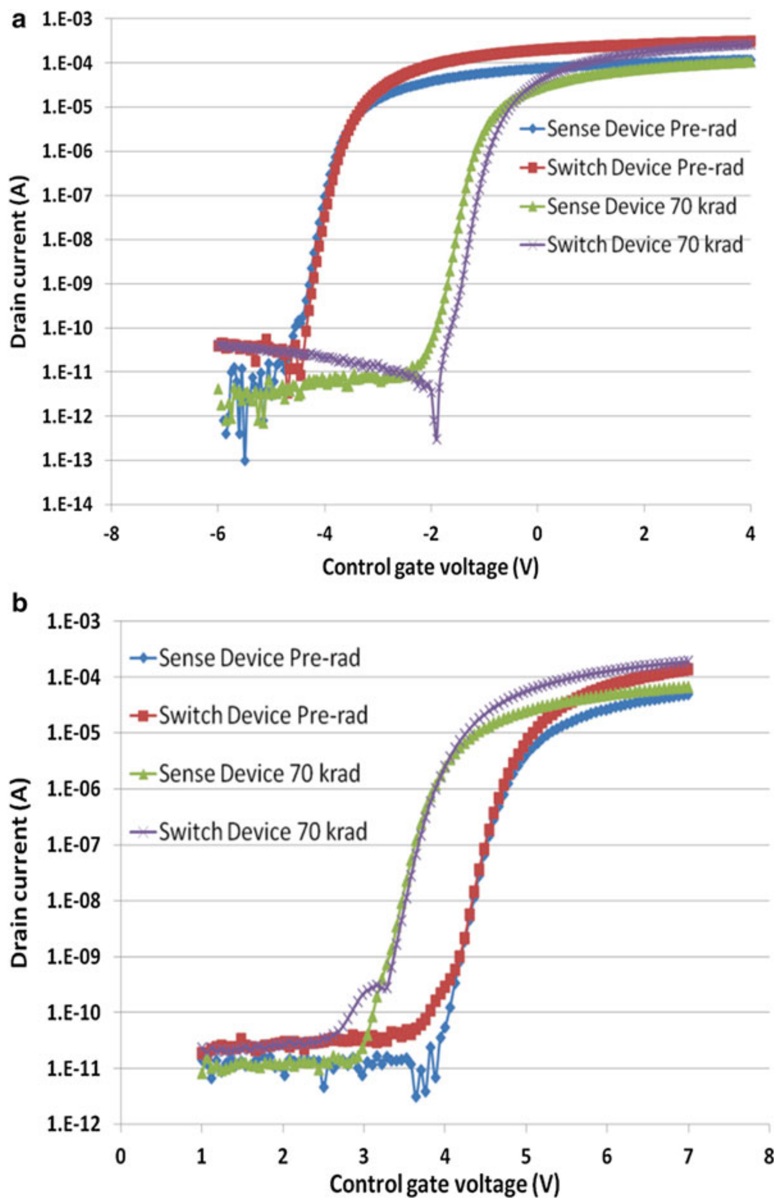


Fig. 11.8 Pre- and post-irradiation Id-Vg characteristics of Flash cell at (**a**) Erase state showing Vt increasing with TID, and (**b**) Program state Vt decreasing with TID

11.4.2 TID Effects on CMOS Transistors

In normal operation the Read action applies a bias to the control gate of switch devices. The circuit feeding the bias to the Flash cell contain thick oxide NMOSFET because they also pass high voltage (>15 V) during Write. If the driving ability of these high voltage devices is compromised, the bias on the switch will be degraded. Figure 11.9 plots Id-Vg curves of pre- and post-irradiated high-voltage device.

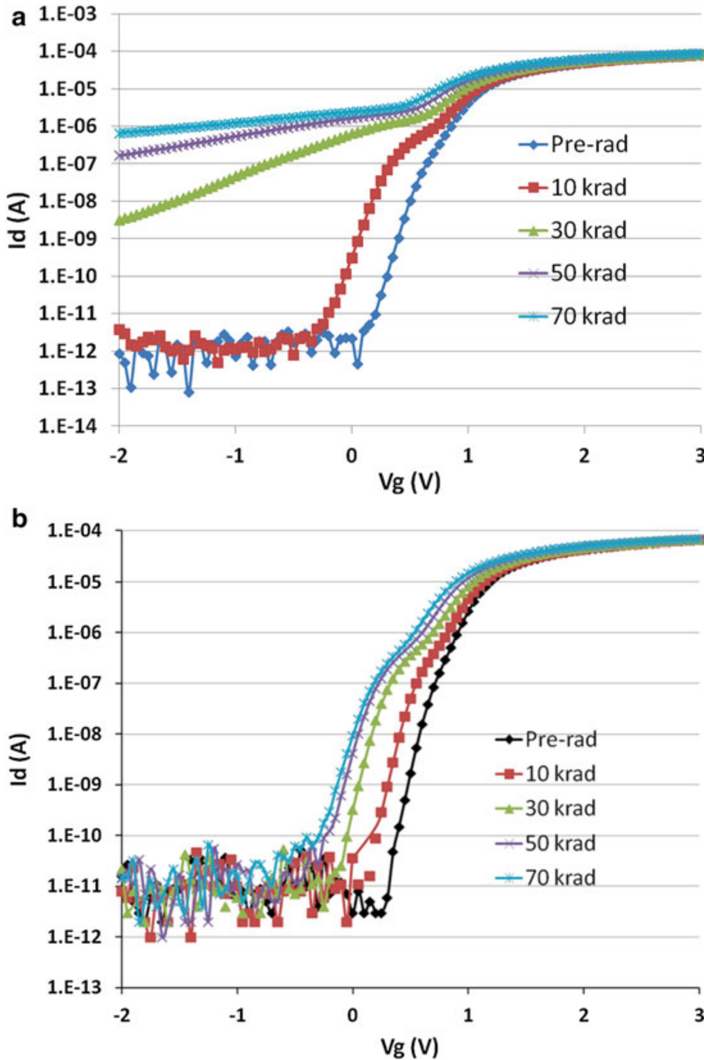


Fig. 11.9 Pre- and post-irradiation Id-Vg characteristics of high voltage NMOS device, with W/L = 10/0.68, and Vds = 0.1 V: (**a**) On-state irradiation bias Vg = VDD and Vd = Vs = Vb = GND; (**b**) Off-state irradiation bias Vd = VDD and Vg = Vs = Vb = GND

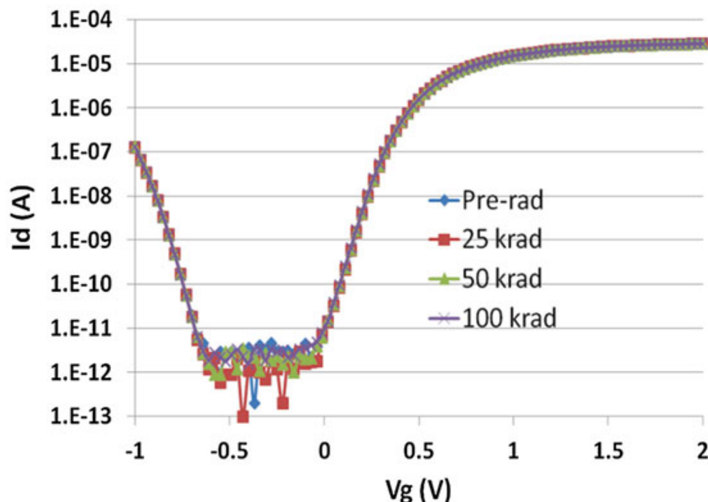


Fig. 11.10 Pre- and post-irradiation IdVg characteristics of low voltage NMOSFET, with W/L = 1/1 and Vds = 0.1 V, irradiated at on-state

Two bias conditions exist during normal operation, on-state and off-state. The on-state shows significant radiation-induced V_t shift and sub-threshold leakage current while off-state only V_t shift. Obviously the on-state has the worst case bias condition under irradiation.

For comparison, the radiation effects of low-voltage NMOS transistor used for logic functions are also tested and its irradiated I_d-V_g characteristics are illustrated in Fig. 11.10. Even irradiated under the worst case bias, there is no significant radiation effect on it.

In the following two sub-sections, these radiation effects at the transistor level will be used to elucidate the radiation effects on critical electrical parameters, propagation delay and standby power supply current, for FPGA function.

11.4.3 TID Effects on Propagation Delay

The in-flux propagation delay measured on the inverter-string is shown in Fig. 11.11. The propagation delay reaches 10 % degradation after 24–29 krad(SiO_2); it reaches 100 % after approximately 70 krad(SiO_2). All parts remain functional after 100 krad(SiO_2).

To relate TID effects on propagation delay to Flash cells, the signal path in Fig. 11.12 shall be examined. For an inverter string configured in the FPGA, the two $V_{control_gate}$-biased switch devices in the signal path are at the Erase state to pass the signal. The TID effects on a switch at the Erase state as shown in Fig. 11.5a increase

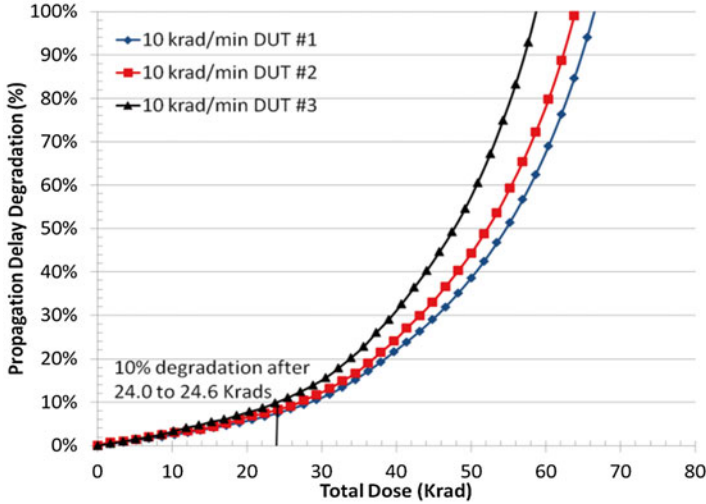


Fig. 11.11 Percentage of propagation-delay degradation versus TID at 10 krad(SiO_2)/min for three DUT

its V_t and decrease the driving strength. Consequently, the propagation delay in the inverter string increases.

High-voltage NMOS transistors also play an important role in the propagation delay degradation. Referring to Fig. 11.12 again, the first $V_{control_bias}$ is provided by the V_{DD} input through the multiplier (MUX) with the V_{DD} input through M1 and GND through M0. Indeed, during operation, the level shifter (LS) is configured to connect V_{PP} to X_outb and GND to X_out to pass V_{DD} through the MUX, then M2, to bias the first Flash switch with $V_{control_bias}$ on its gate. Note that during operation V_{DD} and V_{PP} are biased to 1.2 and 3.3 V respectively. Also, in this circuit, every NMOS transistor to be biased by V_{PP} has to sustain high voltage (>15 V) during programming. Therefore aforementioned thick oxide NMOS transistor has to be used on M0, M1 and M2.

As indicated in Fig. 11.12a, the radiation effects of M1 and M2, being biased at on-state, will increase their current drive and not degrade the propagation delay. On the other hand, Fig. 11.12b indicates that M0, being biased at off-state, will be turned on gradually by irradiation. Consequently, V_{DD} passing M1 will be comprised leading to the degradation of $V_{control_bias}$ and subsequently degrades the propagation delay.

11.4.4 TID Effects on Standby Power-Supply Currents

The radiation effect on static power supply currents is dominated by the core power supply current I_{DDA}; hence it is the only component discussed here. Figure 11.13a plots I_{DDA} versus TID of the same three irradiated DUT as those mentioned in

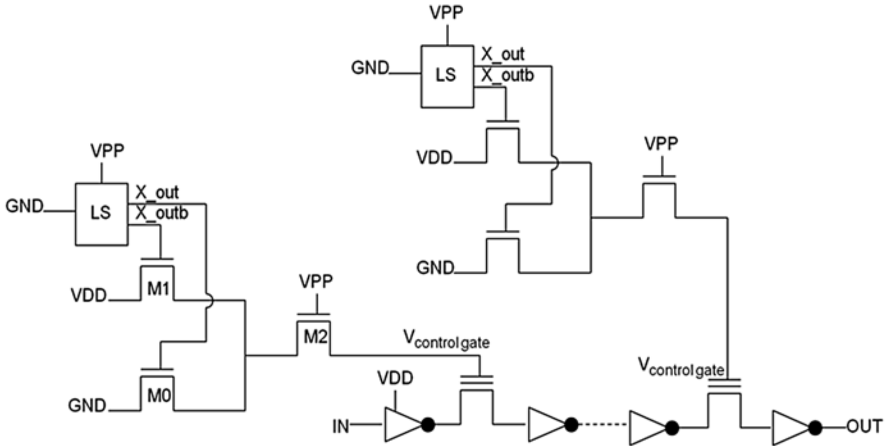
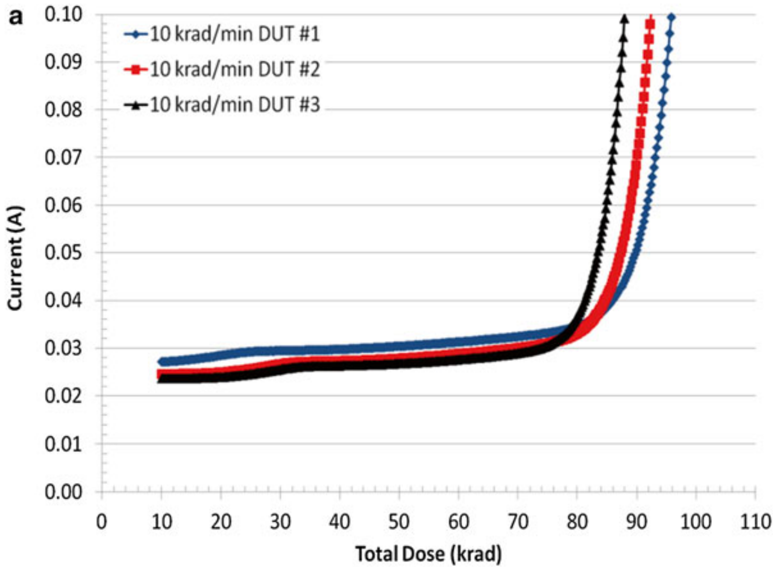


Fig. 11.12 Simplified schematics of DUT design for TID testing, VPP = 3.3 V and VDD = 1.2 V



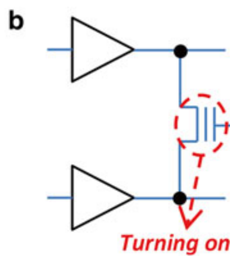


Fig. 11.13 (**a**) IDDA versus TID at 10 krad(SiO_2)/min for three DUT. (**b**) Simplified schematic shows root-cause of radiation induced IDDA due to turning on programmed Flash switch which originally isolates outputs of two drivers

previous sub-section. Initially the currents increase mildly but increase significantly suddenly when certain TID level is reached. All three DUT exhibit this threshold behavior and their threshold total doses are all very close to 80 krad(SiO_2).

This radiation-induced I_{DDA} can also be explained by the radiation effects on the Flash cell and high-voltage NMOS transistor. A simplified schematic in Fig. 11.13b aids to explain the Flash cell case. In an FPGA, a Flash cell is often connected as this schematic, e.g. in a routing multiplier (routing MUX) made of Flash cells (see Fig. 11.6), in which a Flash cell in Program-state isolates two drivers. Radiation degrades the isolation and consequently induced current flows from the driver output high to the driver output low. The case due to radiation effects of high-voltage NMOS has been exposed previously. In Fig. 11.12, the leakage due to M0 will connect V_{DD}, which is the power supply for I_{DDA}, through M1 and M0 to GND, and subsequently contributes to the increase of I_{DDA}. Although not quantitatively proven, it is believed that the Flash cell degradation caused driver contention is the dominant effect. For two reason, there are more cases of Fig. 11.13b than Fig. 11.12, and the threshold behavior in Fig. 11.13a fits better to the model of driver contention by Flash cell degrading to a certain level. Further analysis on this topic is beyond the scope of this paper and will be presented in the future.

11.5 Radiation Test Results on Single Event Effects

This section presents the results of first phase of SEE testing. The SEL of the FPGA is tested to prove its avionics worthy; SEU of the Flash cell is extracted from tests targeted for fabric SEU; fabric FF and SRAM SEUs are tested for static data pattern and dynamic patterns up to 10 MHz.

3D-TCAD simulation is also performed to calculate the cross-section of fabric FF and compared data with test results. The intention is using it to extend the boundary by which heavy-ion testing can reach.

11.5.1 FPGA SEL

The linear energy transfer (LET) threshold for SEL acquired by heavy-ion irradiated FPGA, biased at maximum operating V_{DD} and heated up to 95 °C, is above 15 MeV-cm^2/mg. Indicating the FPGA is immune to neutron-induced SEL and suitable for avionics. Five DUT were tested with total fluence on each DUT higher than 5×17 ions/cm^2.

11.5.2 Flash-Cell SEU

Here the SEU is defined as the single-event induced Flash-cell state flip: Program state flip to Erase state, or Erase to Program. However, from user point of view only flips causing functional failure will be detected. Therefore this is the Flash SEU measured. FPGA programed with SEU testing designs for fabric FF and SRAM were tested to not exceeding a TID limit, usually 10 krad(Si), to ensure performance and functionality. With this restrain, every FPGA been heavy-ion irradiated so far didn't fail functionality. Based on this result, the standard SEU cross-section versus LET plot of Flash cell at Erase state can be generated. Since the FPGA functionality depends on the critical Flash cell at Erase state passing the critical signal, the number of sampling bits has to be estimated from the programming architecture.

The aggregate Flash-cell SEU rates of numerous tested FPGA are plotted as cross section per flash cell versus LET. Figure 11.14 shows the data points. Each point represents an irradiation run. Since no functional failure has ever been observed, there is no SEU in the critical Flash cells. Therefore the cross section is the inverse of the total fluence on a critical Flash cell. In other words, the cross section for each irradiated LET is smaller than the lowest boundary data on this plot. For example, at the maximum tested LET of approximately 90 MeV-cm^2/mg the cross section is below 10^{-13} cm^2. For SEU of Flash cell at Program state, the correlation between state flip and FPGA functionality is not easily established. But nevertheless, non-existence of functional failure after more than 50 runs indicates very low SEU sensitivity for Program state too. In conclusion, these data practically show Flash cell immune to SEU.

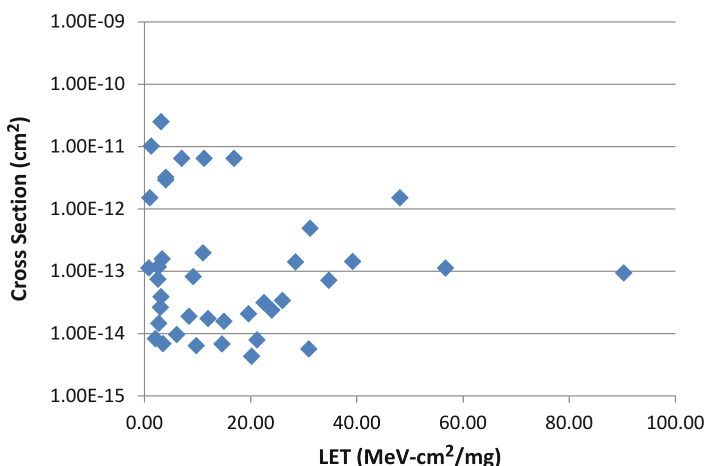


Fig. 11.14 Plot of heavy-ion test results, it displays critical Flash-cell SEU cross-section versus LET

11.5.3 Fabric-Embedded SRAM SEU

Figures 11.15 and 11.16 show the SEU cross-section versus LET plot and Weibull fitting curves of fabric µSRAM and LSRAM respectively. Both SRAM cells have LET_{TH} of 0.85 MeV-cm²/mg. The saturated cross section for µSRAM and LSRAM are 4.5×10^{-9} cm²/bit and 3.0×10^{-9} cm²/bit respectively. Using the Weibull fitting parameters and Crème 96, the upset rate for µSRAM and LSRAM is calculated, for solar minimum and geosynchronous orbit with 100 mils aluminum shielding, to be 2.79×10^{-8} upset/bit/day and 4×10^{-8} upset/bit/day respectively.

11.5.4 Fabric Flip-Flop SEU

Figure 11.17 shows the measured SEU cross-section as a function of LET for the fabric FF, and the corresponding Weibull fitting curve with threshold LET (LET_{TH}) 0.74 MeV-cm²/mg and saturated cross section 1.0×10^{-7} cm²/bit. The signal passing through the shift registers are checkerboard data-pattern running at clock rates of 1, 3 and 10 MHz, and static data all-1 and all-0 patterns. Hundreds of errors are captured to gain a good confidence level in results. Each data point represents an average of three test results. There is no observable frequency dependence; hence data of different frequency are lumped together. Using the Weibull fitting parameters and

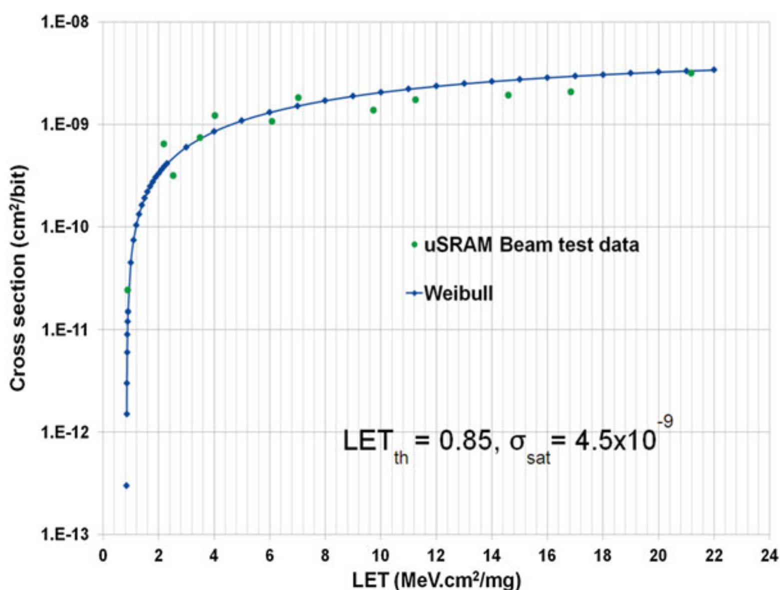


Fig. 11.15 Plot of heavy-ion test results, it displays SEU cross-section of µSRAM versus LET and Weibull fitting curve

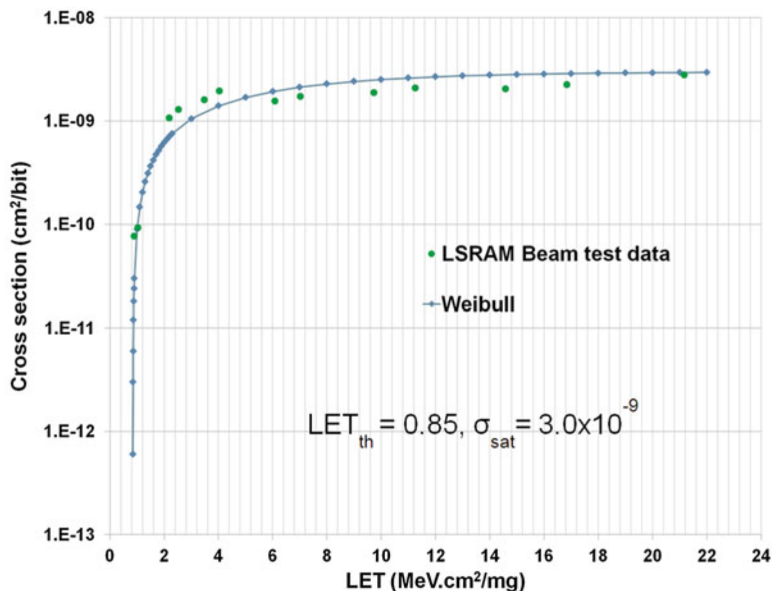


Fig. 11.16 Plot of heavy-ion test results, it displays SEU cross-section of LSRAM versus LET and Weibull fitting curve

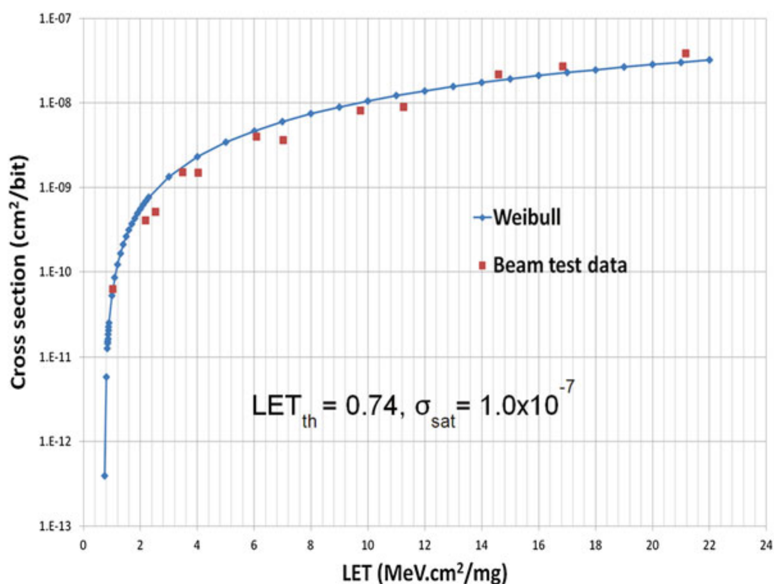


Fig. 11.17 Plot of heavy-ion test results, it displays SEU cross-section of fabric FF versus LET and the corresponding Weibull fitting curve

Crème 96, the upset rate is calculated, for solar minimum and geosynchronous orbit with 100 mils aluminum shielding, to be 1.76×10^{-7} upset/bit/day.

3D TCAD simulations using Robust Chip Inc (RCI) tools are performed to compare with test results. Figure 11.18a shows the 3D structure, which includes the

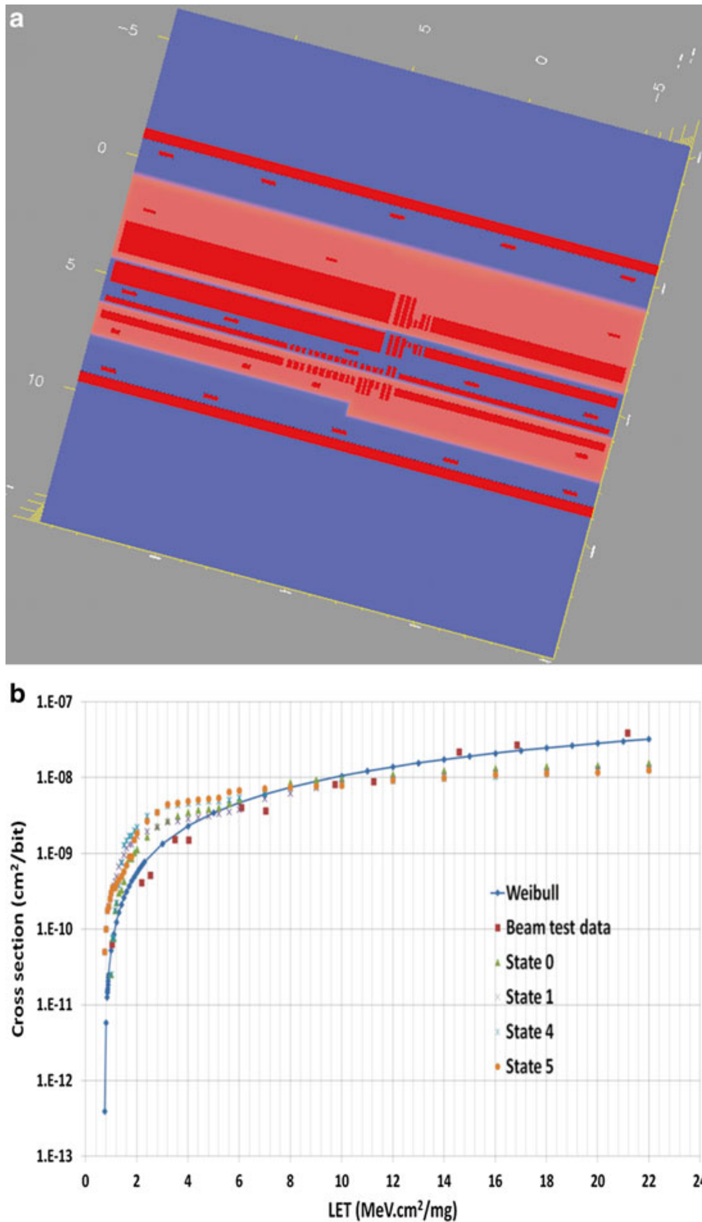


Fig. 11.18 (**a**) Simulated 3D TCAD structure including the FF cell and a simplification of the FF surrounding cells (represented by added "source-ties") existed in the real layout. (**b**) 3D-TCAD simulation results compare to heavy-ion test

fabric FF cell and the relevant neighboring cells, referred to as “source-ties”. This FF is configured to a master-slave edge-triggered D-type FF for SEU testing. Its layout is more complex and with more transistors than a typical hardwired ASIC FF because it can be configured to many variants.

Extensive simulations follow to generate the cross-section as a function of LET. The results for different states (blanket 1 and 0 patterns) of the FF cell are plotted in Fig. 11.18b to compare with heavy-ion test results. The simulation results show a good agreement with test data, especially data near LET_{TH}.

11.6 Future Works

For TID effects, the physical mechanisms causing the propagation delay degradation and power supply current increase, the V_t shifts in the Flash cell and V_t shifts and sub-threshold leakages in the high-voltage NMOS transistors, will be modeled in the context of SPICE simulation. Then quantitative investigations can be performed to reach the finally goal of predicting TID tolerance.

For SEE effects, the next phase of heavy-ion testing will target IPs in which MSS, SerDes and high-speed DDR interface are especially interested by FPGA users. Also high-speed testing up to few 100 MHz on fabric logic and IO will be performed to complete the evaluation.

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