Flexible Displays: Substrate and TFT Technology Options and Processing Strategies

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Contents

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Abstract

Thin film transistor (TFT) technologies developed for fabricating active matrix backplanes on rigid glass substrates for conventional flat panel displays cannot readily be used for fabricating active matrix backplanes on flexible substrates and displays. In addition to mechanical handling issues, flexible substrates impose many additional constraints such as process temperature limitation and thermal stress issues due to CTE mismatch with the TFT thin films for fabricating backplanes for flexible displays. In this chapter we will discuss the flexible substrate options and TFT processing strategies for fabricating flexible backplanes and flexible displays using various display media. Current status on TFT fabrication by printing and roll-to-roll fabrication for flexible displays is also discussed.

Acronyms

AM LCD	Active matrix liquid crystal display
AM OLED	Active matrix organic light emitting diode
AM EPD	Active matrix electrophoretic display
a-Si:H	Hydrogenated amorphous silicon
CNT	Carbon nanotubes
ELA	Excimer laser annealing
EPD	Electrophoretic display
LCD	Liquid crystal display
LTPS	Low temperature polysilicon
MEMS	Micro electro-mechanical systems
MOSFET	Metal oxide semiconductor field effect transistor
OLED	Organic light emitting diode
OTFT	Organic thin film transistor
OSC-TFT	Oxide semiconductor thin film transistor
PEN	Polyethelene naphthalate
PI	Polyimide
RTR	Roll-to-roll
TCE	Thermal coefficient of expansion
TFT	Thin film transistor
ULTPS	Ultra low temperature polysilicon

Introduction

Flexible thin film transistor (TFT) backplane is a crucial enabler for fabricating flexible displays. Once the flexible TFT backplane is fabricated, it is integrated with the display media, such as LCD, EPD, or OLED and appropriate drive electronics to complete the flexible display fabrication. There are several TFT technology options that include a-Si TFT, LTPS TFT, OTFT, and OSC-TFT. The selection of the appropriate TFT option depends primarily on the display media selected and the

display specifications such as size, resolution, and refresh rate. While a full color, high resolution flexible OLED display with high speed video is the holy grail of the flexible display development efforts, there are many applications such as for example an e-reader, where a flexible, low power, monochrome, bistable display using electrophoretic display media may be better suited.

In this chapter we will discuss flexible substrate options, barrier layers, TFT technology options, TFT processing strategies, and the remaining technical issues for realizing various types of flexible displays of interest.

Substrate Options

Thin metal foils such as stainless steel, and thin polymer materials are the main candidate substrates for fabricating flexible backplanes and displays (Erlat et al. 2009). In the following, we will discuss the relative advantages and issues associated with these two options.

Thin/Flexible Metal Foils

Metal foil substrates offer the advantages of higher process temperature capability (for TFT fabrication), dimensional stability (no shrinkage of the substrate during high temperature processing associated with the TFT fabrication), and being impervious to oxygen and moisture (inherent barrier for the ambient oxygen and moisture). The high thermal conductivity of a metal foil substrate is also an advantage for heat extraction and thermal management which is discussed in more detail in section "Other Technical Challenges for Flexible Displays." The disadvantages and limitations of the metal foil substrate include:

1. Being opaque, it cannot be used for transmissive displays or bottom emission OLED displays.
2. Poor surface smoothness characteristics.
3. Capacitive coupling effects.
4. Compatibility issues with the TFT process chemicals.

Not being transparent limits the use of metal foil substrates to reflective displays and top emission OLED displays. Stainless steel such as STS 304 and STS 430 are popular candidate metal foil substrates for use in flexible displays. The surface of these starting stainless steel substrates is very rough with large ($>$0.1 μm) surface protrusions which is not acceptable for flexible display applications because they result in TFT defects in the backplane and also defects in the display media (pixels) integrated on these surfaces. The thickness of thin films employed in the TFT structure are typically in the range of ~100 nm, and the thickness of the thin films employed in OLED media (pixels) can be as low as ~10 nm. Substrate surface protrusions can cause shorts across the TFT electrodes and the display pixels

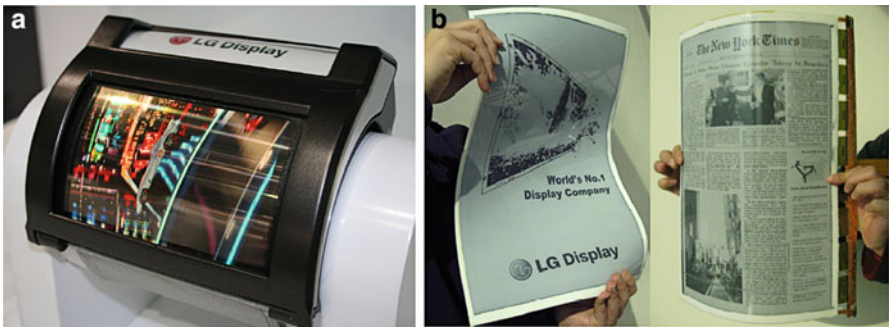

Fig. 1 Photographs of flexible low-temperature a-Si TFT (**a**) 4.3″ AM OLED and (**b**) 19″ AM EPD displays fabricated using backside thinning of stainless steel substrates (Paek et al. 2010)

(e.g., OLED device), or create leakage paths in the TFT and the pixel structures. The starting stainless steel substrates are typically polished to remove the surface protrusions and improve the surface smoothness. In addition, typically the polished stainless steel substrates are coated with a planarizing/buffer layer (Jin et al. 2006a) to improve the surface smoothness and make them suitable for fabricating the flexible backplanes and displays, without defects and with high yield.

Compatibility with the TFT process chemicals can be addressed by using an appropriate protective film at the backside of the stainless steel substrate. Metal foil substrate, by itself, is a good barrier (for oxygen and moisture) and thus it does not require an additional barrier layer. However, the display fabricated using the metal foil substrate would still require a good barrier (encapsulation) layer to be applied on top of the fabricated TFT and the display media such as OLED. Another consideration in the use of metal foil substrate is the parasitic coupling capacitance due to coupling of the backplane electronics to the conductive substrate. The planarizing/buffer layer used for improving surface smoothness of the substrates can also serve to isolate it electrically from the TFT circuit, and reduce the parasitic capacitance between the stainless steel substrate and the TFT and pixel circuits. Stainless steel is being actively investigated as a substrate for the flexible backplanes using LTPS TFT (e.g., Jin et al. 2006a) as well as a-Si TFT for reflective (e.g., Paek et al. 2006; Raupp et al. 2006; Raupp 2007) and top emission mode OLED (e.g., Jin et al. 2006a, b; Chwang et al. 2006) display applications. Paek et al. (2010) report on an interesting method of fabricating a-Si TFT backplanes on thick rigid STS430 stainless steel substrates, and subsequently thinning the backside of the stainless steel substrate by etching down to a thickness of 0.1 mm. These backplanes are then used to fabricate and demonstrate flexible 4.3″ QVGA AM OLED, 11.5″ UXGA AM OLED, and 19″ AM EPD displays. Figure 1 shows the 4.3″ AM OLED and 19″ AM EPD demonstrated. This process is used on a Gen 2 line (370 mm × 470 mm) line to demonstrate fabrication of flexible OLED and EPD displays on a conventional TFT manufacturing line. However, the concerns on the approach include thinning process yield, cost, and scalability.

Flexible Polymer/Plastic Substrates

A transparent plastic substrate has the advantage of being compatible with transmissive as well as reflective displays. Thus it is compatible with both top and bottom emitting OLED device architectures, thereby making it suitable for a broader range of display applications. The technical challenges in the development of plastic substrates for active matrix display application are, however, extremely demanding. The plastic substrates, while being flexible, need to offer glass-like properties and must therefore have high transmission, low haze, smoothness of surface, and excellent dimensional and thermal stability, and low coefficient of thermal expansion (CTE) mismatch with the TFT thin films, and be excellent barriers for oxygen and moisture transport.

Table 1 shows the properties of some of the common candidate plastic substrate materials for flexible backplane and display fabrication. These candidate substrates include polyethylene terephthalate (PET, e.g., Melenix® from DuPont Teijin Films), polyethylene naphthalate (PEN, e.g., Teonex®, Q65, from DuPont Teijin Films), polycarbonate (PC, e.g., GE's Lexan®), polyethersulfone (PES, e.g., Sumilite® from Sumitomo Bakellite), and polyimide (PI, e.g., Kapton® from DuPont). While Kapton has high Tg, it absorbs in the visible (yellow color), and thus is not suitable for transmissive displays or bottom emission OLED displays. Higher process temperature (>350 °C) capable clear plastic substrates are also being developed and investigated (Long et al. 2006) for use as a drop-in replacement for glass with conventional (high-temperature) a-Si TFT fabrication process. However, as these high temperature clear plastic substrates are not commercially available at this time, we will not discuss them further.

Table 1 Available candidate plastic substrates

	PET (Melinex®) ST506	PEN (Teonex®), Q65FA	PC	PES (Sumilite)	PI (Kapton)
Tg, °C	78	120	150	223	410
Upper process temp. (°C)	150	220			
CTE (−55 to 85 °C), ppm/°C	20–25	18–20	60–70	54	30–60
% transmission (400–700 nm)	89	87	90	90	Yellow
Moisture absorption (%)	0.14	0.14	0.4	1.4	1.8
Young's modulus, Gpa	4	5	1.7	2.2	2.5
Tensile strength, Mpa	225	275		83	231
Density, g/cm^3	1.4	1.36	1.2	1.37	1.43
Refractive index	1.66	1.5–1.75	1.58	1.66	
Birefringence, nm	46		14	13	

Table 2 Comparison of PEN and stainless steel substrates to glass substrates

	Glass	PEN	Stainless steel
Weight, gm/m^2 (for 100 μm thick film)	220	120	800
Transmission in the visible range	92 %	90 %	0 %
Maximum process temperature (°C)	<600	<200	>1000
TCE (ppm/°C)	3	18–20	~10
Elastic modulus (Gpa)	70	5	200
Permeability for O_2 and H_2O	No	Yes	No
Coeff. of hydrolytic expansion (ppm/%RH)	0	11	0
Surface roughness (nm)	2	~5	~100
Planarization necessary	No	No	Yes
Electrical conductivity	None	None	High
Thermal conductivity (W/m °C)	1	0.1	16

Limitations of the available plastic substrates include: limited process temperature capability, lack of dimensional stability (during TFT processing involving high temperatures), and significant differences in the linear thermal coefficient of expansion (TCE) between the plastic substrate and the TFT thin films. Plastic substrates are believed to have a lower cost potential compared to the metal foil substrates. Based on availability and the broad range of desirable film properties (in comparison to the other candidate polymer substrate materials) DuPont Teijin Film's (DTF) PEN substrates are widely used in the development of flexible TFT backplanes for flexible OLED and electrophoretic displays (e.g., Raupp et al. 2006; Raupp 2007; Sarma et al. 2003, 2004, 2007; Hwang et al. 2007). Table 2 show a comparison of the properties for the stainless steel and PEN substrates against the standard rigid glass substrates for use in TFT backplane applications. Major advantages of the stainless steel in comparison to PEN plastic films include higher process temperature capability (allowing direct fabrication of conventional a-Si or LTPS TFT arrays) and lower TCE mismatch with the TFT thin films. In comparison to the TCE values for stainless steel (10) and PEN (18), the TCE values for the common TFT materials are in the following range: glass = 5, SiNx = 1.5, Si = 3.4, Cr = 6.5, Mo = 5, and Al = 24 ppm/°C. This significant difference in TCE of the substrate and the TFT thin films can result in excessive thermal stresses that lead to substrate bowing, warping, and breakage. The oxygen and moisture barrier properties of stainless steel (while being excellent), are not believed to be compelling, as it does not obviate the need for an additional effective barrier layer for encapsulating the top side of the display media built on these substrates.

Based on availability and continuing development and improvements, and suitability for a broad range of flexible displays, PEN plastic substrate has a potential for being a viable candidate for flexible displays. In the following sections we will discuss the characteristics of the PEN plastic substrates in detail as they relate to TFT backplane fabrication processes.

PEN Plastic Substrates

Polyester films (e.g., PET and PEN from DTF) are well-known substrates for a wide range of electronic applications such as membrane touch switches and flexible circuitry (MacDonald et al. 2002). New developments in polyester film substrates are contributing to the successful development of PEN plastic substrates (Teonex® brand) for use in flexible active matrix display applications. These PEN based substrates offer a unique combination of excellent dimensional stability, low moisture pickup, good solvent resistance, high clarity, and very good surface smoothness. This combination of attributes makes PEN a more promising substrate in comparison to the other available plastic substrates. The characteristics of the presently available PEN substrates that relate to the requirements of TFT backplane and display applications are discussed below.

Optical Characteristics

Good optical properties are achieved with Teonex® Q65 films by close control of the polymer recipe (MacDonald 2004; MacDonald et al. 2006). Typically Teonex® Q65 has a total light transmission (TLT) of 87 % over 400–700 nm coupled with a haze of less than 0.7 %. The substrate is optically clear and colorless, and thus can be used for transmissive or reflective displays and bottom as well as top emitting OLED displays. They are not, however, suitable for the LCDs because of their birefringence. As PEN is a semicrystalline biaxially oriented thermoplastic material, it is birefringent and thus is not a suitable substrate for the LCD media that depends on the polarization control of the propagated light. Amorphous polymer substrates are not birefringent and thus are suitable for the LCD media. Birefringence is not an issue for the OLED and EPD media.

Surface Smoothness

Surface smoothness and cleanliness are essential to prevent pinpricks in subsequent barrier coatings and to ensure that the defects from the substrate do not deleteriously affect the active matrix TFT manufacturing yield. Industrial grade PEN typically has a rough surface with a large (unacceptable) concentration of peaks (protrusions) of up to 0.1 μm high. By control of recipe and film process optimization, Teonex® Q65 achieves a much smoother surface without any 0.1 μm high peaks and only a small concentration of 0.05 um high peaks. These remaining surface defects are still detrimental to the performance of the thin films deposited on top. These remaining surface defects are then removed by the application of a planarizing layer (Eveson et al. 2008). Figure 2 (Eveson et al. 2008) shows the protrusions in nonplanarized and planarized Q65FA over a 5 cm by 5 cm area. Protrusions greater than 40 nm high are completely removed after planarization. There is a significant decrease in protrusions smaller than 40 nm due to planarization as well. The planarization layer also promotes the adhesion of the subsequent barrier layers deposited on the substrate.

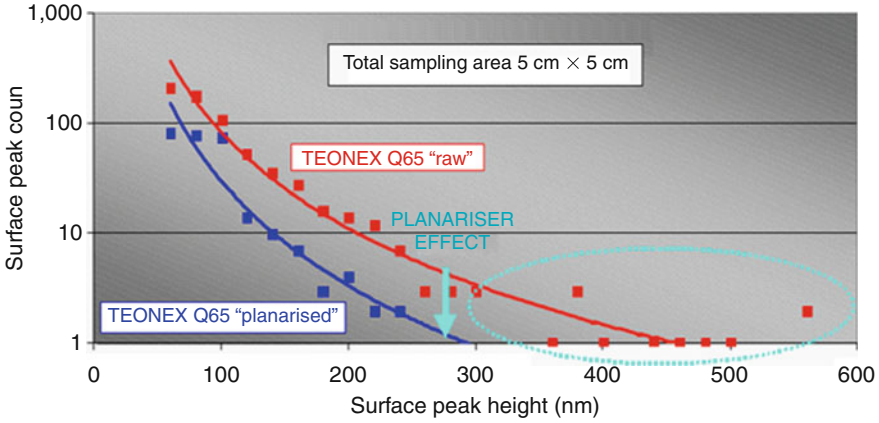

Fig. 2 Reduction of protrusions by surface planarization of Q65FA PEN substrates (Eveson et al. 2008)

Resistance to Solvents and Moisture

The Q65 Teonex® brand has excellent solvent resistance to most acids and organic solvents and will typically withstand the solvents used in AM OLED display fabrication. Indeed no specific issues of significance are observed using the Teonex® Q65 substrate during the fabrication of the a- Si TFT backplanes and AM OLED test displays (Sarma et al. 2003). While the PEN substrate does not react with moisture, it does absorb moisture, which results in a dimensional change. Figure 3 shows the moisture absorption in the PEN substrate as a function of relative humidity (RH) and time (MacDonald et al. 2006). At 40%RH, the equilibrium moisture concentration in the film is expected to be about 957 ppm which is very high, as for every 100 ppm of moisture absorbed, the film is estimated to expand by approximately 45 ppm. This is a very significant dimensional change and can deleteriously affect the TFT backplane process if it is not managed. Moisture absorption is reversible by heating the substrate in vacuum or in an inert atmosphere. Uncontrolled moisture absorption/desorption during the TFT backplane fabrication can potentially have far more impact on the substrate dimensional stability than the dimensional instability due to the inherent PEN substrate shrinkage. It is important to understand the moisture absorption/desorption characteristics of the PEN substrate to control its dimensions during the active matrix backplane fabrication.

Dimensional Stability and Reproducibility

Dimensional stability and reproducibility during TFT array processing (involving temperature cycles between room temperature and the TFT process temperatures) is extremely critical to ensure that the features in each layer of the TFT device structure align properly with the features in the previous layers. Glass substrate does not have this issue as it has excellent dimensional stability during TFT array processing. In addition to dimensional stability, reproducibility is also important for plastic substrates. While dimensional changes (due to moisture absorption etc.) need to be very

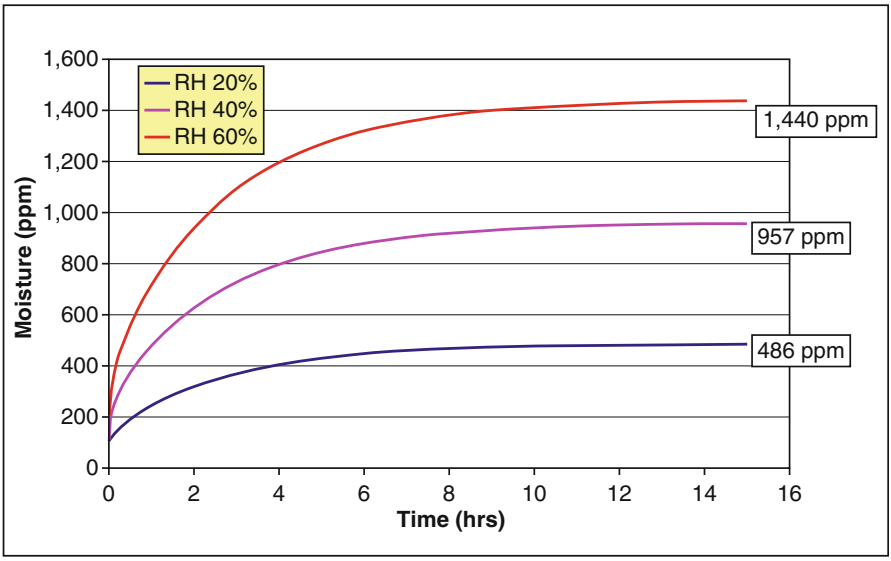

Fig. 3 Moisture absorption in PEN plastic substrates (MacDonald et al. 2006)

small (negligible), at minimum, it needs to be predictable and controllable so that it can be managed during fabrication of each layer of the TFT structure.

Two physical aspects come into play for polymer films during the display fabrication (Eveson et al. 2008): (1) shrinkage of the film and (2) natural expansion of the film. To understand film shrinkage it is important to recognize that PEN films (Teonex®) are produced using a sequential biaxial stretching technology. This process involves stretching film in machine and transverse directions (MD and TD) and heat setting at elevated temperature. As a consequence a complex semi-crystalline microstructure develops in the material, which exhibits remarkable strength, stiffness, and thermal stability. The film comprises a mosaic of crystallites or aggregated crystallites accounting for nearly 50 wt% of its material which align along the directions of stretch. The noncrystalline region also possesses some preferred molecular orientation, which is a consequence of its connectivity to the crystalline phase. Importantly, the molecular chains residing in the noncrystalline region are on average slightly extended and therefore do not exist in their equilibrium Gaussian distribution. Shrinkage is associated with the relaxation of this residual strain, back to equilibrium within the partially oriented parts of the film structure. To counterbalance this effect, PEN films are further exposed to a thermal relaxation process, in which film is transported relatively unconstrained through an additional heating zone. The second factor that impacts dimensional reproducibility as the temperature is cycled is the natural expansion of the film as quantified by the TCE.

Shrinkage at a given temperature is measured by placing the sample in a heated oven for a given period of time. The percentage shrinkage is calculated as the percentage change of dimension of the film in a given direction due to heating.

Table 3 CTE of PEN (Q65) as a function of temperature and orientation

	CTE (ppm/°C)			
	−50–0 °C	0–50 °C	50–100 °C	100–150 °C
Machine direction	13	16	18	25
Transverse direction	8	11	18	29

Heat-stabilized films exhibit shrinkage of the order of <0.1 % and typically <0.05 % when exposed to temperatures of up to 180 °C for 5 min. Once heat stabilized, Teonex® Q65 remains a dimensionally reproducible substrate up to 200 °C. Its improved thermal resistance provides a dimensionally reproducible substrate over this temperature range and permits a continuous use temperature of up to about 180 °C. It should be noted that shrinkage of 0.05 % is not acceptable for fabricating the TFT backplanes. In section "TFT Processing Strategies for Flexible Backplanes," we will discuss this further and describe a prestabilization process to reduce the shrinkage to manageable levels, for direct fabrication of low-temperature a-Si TFT backplanes.

Thermal coefficient of expansion (TCE), and more particularly the difference in the TCE of the plastic substrate and the TFT thin film materials, is an important factor in the backplane fabrication, due to the deleterious effect of the thermally induced strain (in the TFT thin films) during cool down to room temperature from the process temperatures. The TCE in the heat stabilized Teonex films varies with temperature and the orientation (machine direction versus the transverse direction) as shown in Table 3. Excessive strains/stresses result in film cracking, delamination, and substrate curling/buckling problems.

Barrier Properties

The inherent barrier properties of PEN films are typically of the order of ca 1 g/m^2/day for water vapor transmission rate and an equivalent ca of 3 mL/m^2/day for oxygen transmission rates. This is a long way from the levels required for the protection of OLED displays, which require water vapor transmission rates of $<10^{-6}$ g/m^2/day and oxygen transmission rates of $<10^{-5}$ mL/m^2/day. No polymer substrate meets these requirements, and the flexible substrates currently being developed need to use an additional effective barrier film to encapsulate the OLED devices for protection against oxygen and moisture ingression to enhance the OLED life time. Note that the EP displays are far less sensitive to moisture and thus do not impose such stringent requirements on the barrier layer performance.

In Situ Fabricated Flexible Substrates

In some flexible TFT backplane processing strategies (Battersby and Fench 2006; French et al. 2007; French 2009; Pecora et al. 2008), the flexible substrate is fabricated (coated) directly on a rigid temporary substrate. The TFT backplane is then fabricated on this coated thin plastic film (flexible substrate). The display media

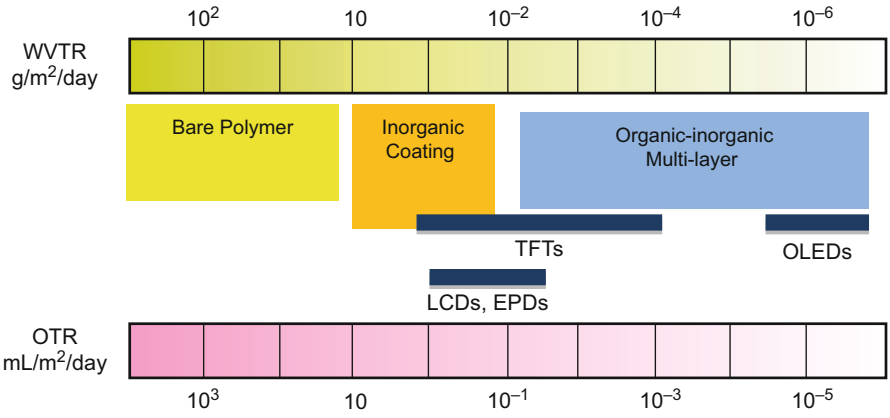

Fig. 4 Oxygen and moisture barrier levels required for various displays

(e.g., EPD, OLED) is then integrated with the backplane while it is still attached to the temporary rigid substrate. Finally, the fabricated active matrix display on the coated flexible substrate is released and separated from the rigid temporary substrate. This approach is discussed in more detail in section "In Situ Plastic Coating on a Temporary Substrate."

Barrier/Encapsulation Films

Lack of impermeability to moisture and oxygen is a serious deficiency of all the available plastic substrates for the flexible display application. All display media including LCDs, EPDs, and OLEDs degrade when exposed to oxygen and moisture in the ambient, even though at different rates with OLED having the most sensitivity to moisture and oxygen, as shown in Fig. 4. Figure 4 shows the oxygen and moisture sensitivity range for the LCD, EPD, and OLED display media and TFTs. For example, for the protection of an OLED display the plastic substrate (barrier layer) must have a permeability of less than 10^{-6} gm/m^2/day for moisture and 10^{-5} mL/m^2/day for oxygen. In comparison, LCD displays have a requirement of less than 10^{-2} gm/m^2 day for oxygen and moisture, which is significantly less stringent compared to OLEDs. The base plastic substrates typically have about 10 gm/m^2 day transmission rates for oxygen and moisture implying the need for incorporating a separate barrier layer.

In principle, a thin layer of an inorganic film such as SiO_2, SiN_x, Al_2O_3, etc., deposited on the flexible plastic substrate can serve as a barrier layer with the required impermeability to oxygen and moisture. However, in practice multilayer barrier film structures are believed to be required to counter the effects of the pinholes/cracks in single layer deposited barrier layers. Several organizations are developing optically transparent multilayer barrier coatings for flexible OLED displays (Graff et al. 2005). Vitex Systems (Moro et al. 2006) uses such kind of an

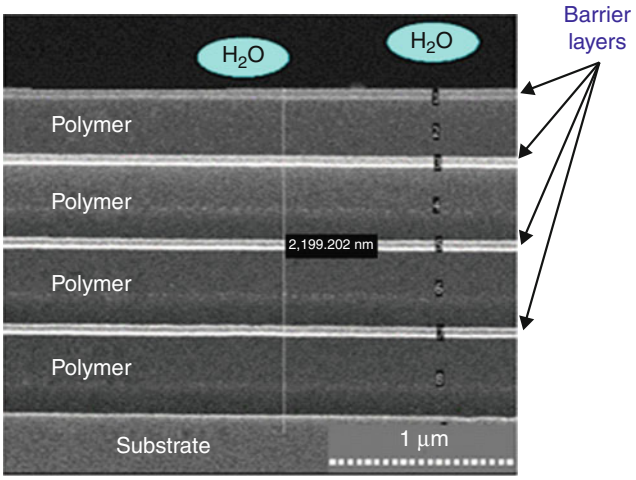

Fig. 5 Vitex barrier comprising a multilayer stack of organic and inorganic films (Moro et al. 2006)

approach for their barrier film called Barix^{TM} which employs alternating layers of a UV curable acrylate polymer and a 500 Å thick ceramic Al_2O_3 deposited in vacuum, as shown in Fig. 5. The inorganic films serve as barrier films for oxygen and moisture, organic layers serve the planarization/smoothing function, and multilayers (diads) provide redundancy against pinhole defects in the barrier films. The Barix^{TM} layer is found to be an effective barrier layer, by minimizing the detrimental effects of pinholes and diffusion at grain boundaries. The Barix^{TM} films typically about 3 um thick were found to have water permeability in the range of 10^{-6} gm m^{-2} day^{-1}.

Note that whether using a plastic substrate or a stainless steel substrate, the top side of the TFT backplane and the display media (e.g., OLED) must be protected with either an impermeable thin film encapsulation (barrier) layer directly or by another substrate coated with an encapsulation (barrier) layer.

TFT Technology Options for Flexible Displays

Flexible substrate compatible TFT backplane technology is a critical item for the development of flexible active matrix displays. Both the well established TFT technologies, namely a-Si TFT and LTPS TFT, are considered for flexible display applications. In addition, newer and emerging TFT technologies, such as organic TFT (OTFT) and oxide semiconductor (OSC-TFT, such as InGaZnO), are also being developed for flexible backplane applications.

Generally, the TFT processes developed and optimized for use with the flat and rigid glass substrates (with an ~600 °C process temperature capability) cannot readily be applied for use with the flexible plastic substrates, due to reasons such as lower process temperature constraints, thermal stress issues resulting from the

CTE mismatch, and dimensional stability issues. Consideration of the characteristics of the available TFT technologies (see Parts 15, "TFTs and Materials for Displays and Touchscreens: Display Glass," 16, "Inorganic Semiconductor TFT Technology," and 17, "Emerging TFT Technologies") can illustrate the issues in adapting them for the fabrication of flexible backplanes. Table 4 shows a comparison of the candidate TFT technologies including device layer transfer (DLT), LTPS, ULTPS, conventional a-Si TFT, low-temperature a-Si TFT, OTFT and OSC-TFT. In the following, we will discuss the advantages and issues with each of these options (except DLT, which is discussed in section "Device Layer Transfer (DLT) Process") for fabricating flexible backplanes.

LTPS TFT

Conventional LTPS process used in the current AM LCD and AM OLED displays uses a typical process temperature in the range of ~450 °C using a polysilicon film produced by excimer laser annealing (ELA) / recrystallization of an a-Si film. Due to the high process temperature requirement, the conventional LTPS TFT approach may be appropriate for use by direct fabrication on stainless steel substrates, but not on available plastic substrates with a process temperature limitation of less than 200 °C. To overcome this problem when using a plastic substrate, ultra low-temperature (<200 °C) polysilicon (ULTPS) TFT processes are being developed (e.g., Kwon et al. 2006; Gosain and Usui 2000). The ULTPS TFT approach has a potential for providing high mobility CMOS TFT devices suitable for driving the OLED pixels, as well as for fabricating the row and column drivers directly on the plastic substrate. Good progress has been reported producing TFTs with high mobility and satisfactory threshold voltages for the n- and p-channel devices. However, the leakage currents need to be reduced, and threshold voltage stability needs to be improved further, for fabricating high quality active matrix displays.

a-Si TFT

Amorphous silicon TFT is currently the workhorse of the well-established AM LCD technology, and thus it would have the advantage of available processes and infrastructure, if it can be adapted for flexible display manufacturing applications. However, for application to OLED display media, a-Si TFT does have some issues that require resolution. These issues include:

(a) The low mobility (μ_{fe} ~ 1 cm^2/Vs) does not allow integration of the row and column drivers on the backplane.
(b) Only NMOS TFTs are available in a-Si, which restricts the choice of pixel circuit designs.
(c) The TFT stability with respect to gate bias is not satisfactory. This has a significant impact as discussed in more detail below.

Table 4 TFT technology options for flexible displays

		Poly-silicon		a-Si			
	Device Layer Transfer (DLT)	LTPS	ULTPS	Conven. a-Si	Low-temp a-Si	Organic TFT	OSC-TFT
Process temp. (°C)	~450 °C	~450 °C	<200 °C	~300 °C	<200 °C	<150 °C	<200 °C
Circuit type	CMOS	CMOS	CMOS	NMOS	NMOS	PMOS	NMOS
Device performance							
Mobility cm^2/Vs)	~100	~100	~100	~1	~1	~1	~10–50
Off-current	Excellent	OK	Issue	Excellent	Excellent	OK	OK
Uniformity	Good	Issue	Issue	Good	Good	OK	OK
Stability	Excellent	OK	Issue	Issue	Issue!	Issue!!	OK ?
Cost	High	Medium	Medium	Low	Low	Very Low ?	Low
Maturity	Low	High	Low	High	Low	Low	Low

The conventional a-Si TFTs used in the current AM LCDs are fabricated at a typical process temperature of 300 °C. Again, for the obvious reason of high process temperature requirement, the conventional a-Si TFT process could not be used with the available plastic substrate with a process temperature limitation of less than 200 °C. Significant advances have been made in the process temperature reduction, and a-Si TFTs have been successfully fabricated using low process temperatures of <200 °C (e.g., Raupp 2007; Sarma et al. 2003; Gleskova and Wagner 1999, 2001; He et al. 2000; Wagner et al. 2010), with a performance comparable to the 300 °C process with respect to mobility, threshold voltage, and leakage current. However, the device stability under gate bias stress remains to be one item that remains to be improved particularly for the low temperature processed a-Si TFTs. a-Si TFTs are known to exhibit threshold voltage shifts, ΔV_t, under prolonged positive gate bias, particularly under higher operating temperature conditions. In AM OLED display operation, the drive TFT is typically subjected to positive gate voltage bias (for an n-channel TFT) for the entire frame time (as opposed to only during the row address time as in an AM LCD). The TFT stability issues become more severe for higher gate drive voltages and higher operating temperatures. With continuing progress in OLED materials and devices towards lower drive voltages and pixel current requirements, the stability of a-Si TFT stability may be expected to become less of an issue.

OTFT

There is much interest in the development of organic electronics utilizing TFTs fabricated using organic semiconductors. OTFTs have the advantage of very low process temperatures (<150 °C), and thus can be fabricated directly on available plastic substrates (Nomoto 2010). Also, they can be fabricated using low-cost solution processing methods (e.g., spin coating, ink jet printing, etc.) instead of the more expensive vacuum based thin film deposition methods. OTFTs fabricated using vacuum deposited Pentacene as the organic semiconductor have shown the good performance (e.g., Gundlach et al.) with a field effect mobility of over 3 cm^2/V s, near zero V_t, and "on" – "off" current ratio of over 10^8. However, the solution processable organic semiconductor based OTFTs have shown lower mobilities (<0.5 cm^2/V s). One major advantage of OTFTs fabricated by compete solution processing (e.g., ink-jet printing) is that it is easier to compensate for dimensional instability of the plastic substrate, if required, during backplane processing (Burns et al. 2006). OTFT backplanes have been used to demonstrate LCD, EPD, and OLED flexible displays (Nomoto 2010). Noda et al. (2010) demonstrated an impressive rollable full color AM OLED display driven by OTFT backplane. This 4.1″ wide rollable display has a resolution of 121 ppi, and a thickness of 80 um, and bending radius of <5 mm. Similarly, Plastic Logic (Burns 2010) has demonstrated the development of a 10.7″ size monochrome flexible electrophoretic display with a resolution of 1280 × 960 (150 ppi) using OTFT backplane fabricated on PET plastic substrate, for commercialization. While, flexible AM EPDs using OTFT backplanes are at commercialization stage, there are some issues to be addressed

including stability for the application of flexible OTFT backplanes for the more demanding AM OLED application. This topic "Organic TFT" is discussed in detail in Part 17, "Emerging TFT Technologies" of this handbook.

OSC-TFT

Transparent oxide semiconductors such as zinc oxide (ZnO) are actively investigated for use in low-temperature TFT backplanes for displays (e.g., Hirao et al. 2006; Carcia et al. 2005). ZnO is a wide band gap (−3.3 eV at 300 K) semiconductor and has the advantage of being deposited directly in a polycrystalline phase even at room temperature (such as by RF magnetron sputtering), and thus is compatible with the currently available flexible plastic substrates. Hirao et al. (2006) achieved a field effect mobility and threshold voltages of 50.3 Cm^2/V s and 1.1 V, respectively, for ZnO TFTs and demonstrated an AM LCD display. Also, an additional feature of the ZnO TFT is its high transmission in the visible range. In recent times there has been much interest, and significant progress in the development of amorphous InGaZnO channel material for fabricating Oxide TFT backplanes and displays (Nomura et al. 2004; Kamiya et al. 2009; Mo et al. 2010), because of their higher mobility (like LTPS) and superior large area uniformity, in terms of the device characteristics (mobility, threshold voltage, leakage current), and large area fabrication capability (like a-Si TFT). In fact, the structure of OSC-TFT is similar to that of the popular a-Si TFT, such as the inverted staggered bottom gate structure. OSC-TFT approach has been used to fabricate and demonstrate flexible backplanes and displays using both stainless steel and plastic substrates and various display media including LCD, EPD, and OLED. OSC-TFT technology is discussed in detail in chapter "► Oxide TFTs" of this Handbook. Carbon nanotubes TFT, which is another emerging TFT technology with a potential for use in fabricating flexible backplanes and displays, is also discussed in chapter "► Carbon Nanotube TFTs" of this Handbook.

In the next section, we will discuss the various TFT process strategies employed in fabricating flexible TFT backplanes using flexible plastic substrates and stainless steel foil substrates.

TFT Processing Strategies for Flexible Backplanes

Various TFT Processing strategies are developed for fabricating flexible TFT backplanes. These include:

1. Direct processing on the flexible substrate
2. Temporary substrate bonding – debonding
3. Device layer transfer (DLT)
4. In situ plastic coating on a temporary substrate

Processing the TFT backplane directly on the flexible substrate is a straight forward approach. Generally, this approach requires low-temperature TFT (<200 °C) processing because of the process temperature limitation for plastic substrates, and due to the stress issues arising from the CTE mismatch between the flexible substrate material and TFT materials. Stainless steel substrates do allow higher process temperatures, but the thermal stress issues (due to CTE mismatch) impose the upper TFT process temperature limit. The other thee strategies are aimed at overcoming the process temperature limitations associated with the direct processing strategy, and the issues in mechanical handling of the thin and flexible substrates during TFT processing.

Constraining the substrate by a frame or some type of fixturing can alleviate the substrate warping and handling issues to some extent. The second strategy extends this concept further by temporary bonding of the flexible substrate to a rigid substrate using a temporary adhesive, prior to the TFT backplane fabrication, and then debonding the flexible substrate with the TFT backplane from the temporary rigid substrate. The third strategy, device layer transfer (DLT), involves transferring the TFT device layer to a flexible substrate. The fourth strategy involves in situ plastic film coating on a temporary rigid substrate, TFT backplane processing, and then release of the coated flexible film/substrate with the TFT backplane from the rigid temporary substrate. In the following, we will discuss each of these process strategies in detail along with advantages and issues.

Direct Processing (on Flexible Plastic and Stainless Steel Substrates)

Direct processing is straightforward and it can be more amenable to roll-to-roll (RTR) processing compared to the alternate TFT process strategies which may be more suitable for batch type implementation. The challenges in direct processing approach when using the available plastic substrates involve development of low-temperature TFT processes, and managing the thermal stress issues arising from the dimensional changes in the plastic substrate (due to shrinkage and moisture absorption), and CTE mismatch during TFT processing. In case of stainless steel substrates, the challenge is primarily managing the issues due to the CTE mismatch that causes thermal stresses leading to film bowing, warping, and cracking.

In the following, we will discuss the direct processing of a-Si TFT, LTPS TFT, OTFT, and OSC-TFT backplanes on flexible PEN plastic substrates, and flexible stainless steel substrates. All these different TFT–flexible substrate combinations have been used with various display media such as LCD, EPD, and OLED.

a-Si TFT on PEN Plastic Substrate

We will discuss the direct fabrication of a-Si TFTs on flexible PEN substrates in detail to discuss to illustrate the issues in fabricating TFT backplanes on flexible substrates in general, and then its status. Dimensional stability issues arising from the substrate shrinkage, moisture absorption/desorption, and CTE mismatch are a major

consideration in the successful fabrication of the a-Si backplanes on PEN substrates. Sarma et al. (2003) utilized a prestabilization process involving annealing of the PEN plastic substrates in vacuum at 160 °C for 4 h to increase the dimensional stability against shrinkage. The need for dimensional stability of the plastic substrate can be illustrated when we consider the typical design rules used in the TFT backplane fabrication. For a typical 3 μm design rule used (for a contact via, as an example), a shrinkage (misalignment) of more than 1.5 μm is problematic. The as-received "heat stabilized PEN substrate" shrinks by about 0.05 % during TFT backplane processing. This translates to a misalignment of 250 μm over a span of 50 mm (for a 2 in. display). Clearly, this level of shrinkage (dimensional instability) is not acceptable. With the developed prestabilization process, the shrinkage during TFT backplane processing is reduced to 1.5 μm over a 60 mm span (~25 ppm or 0.0025 %). Also, as all other plastic materials, Q65 PEN substrate absorbs moisture resulting in a dimensional change (MacDonald et al. 2006). Figure 3 shows the moisture absorption in PEN with time as a function of relative humidity (RH) at 20 °C ambient temperature. Note that every 100 ppm of moisture absorption results in a dimensional change of about 45 ppm, and this level of dimensional change is very inconsistent with the dimensional stability requirements for backplane fabrication. To eliminate or greatly minimize the dimensional changes associated with moisture absorption/desorption during TFT processing, the PEN substrate is coated with 3000 Å thick plasma CVD deposited SiNx moisture barrier on both top and bottom surfaces, after the substrate prestabilization, and prior to the TFT array fabrication. The single layer SiNx film, while it does not eliminate the moisture absorption completely, it greatly minimizes it, thereby enhancing the substrate's dimensional stability during the TFT processing steps. In addition, as an additional precaution, prior to any new film deposition step during the TFT array fabrication, the substrate is prebaked under standard conditions to restore its baseline dimension.

Sarma et al. (2003, 2004, 2007) developed and implemented a 150 °C a-Si TFT process to fabricate backplanes using the PEN plastic substrates that were prestabilized and coated with 3000 Å of SiNx barrier layer on both top and bottom. The process sequence employed was similar to that of conventional high temperature CHP (*Ch*annel *P*assivated) type a-Si TFT process. However, the process recipes for the TFT thin film depositions, particularly for the a-Si and SiNx dielectric layers, are optimized for 150 °C process, to achieve the mobility and leakage current characteristics comparable to the high temperature processed TFTs (Sarma et al. 2003, 2004). Further, the mask and process design details are optimized by taking into consideration the expected level of plastic substrate shrinkage during the TFT process, and thin film stresses due to CTE mismatch. Four-inch diameter, 125 μm thick PEN plastic substrates are utilized for fabricating the backplanes for the test displays. Figure 6a shows a photograph of a fully processed (with three 64 × 64 pixel backplanes) 4-in. diameter PEN plastic substrate. Figure 6b shows the photograph a fabricated pixel in a 64 × 64 pixel array. Figure 7 shows photographs of a 4.8 cm × 4.8 cm, 160 × 160(×3) pixel backplane fabricated on a 4-in. diameter PEN plastic substrate and its flexural capabilities. One of the critical requirements for successful backplane fabrication is maintaining layer-to-layer registration of various

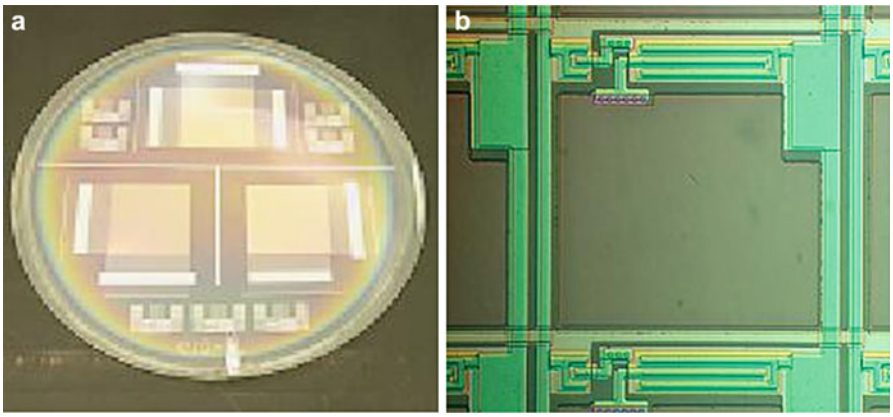

Fig. 6 Photograph of a-Si TFT backplanes processed on a 4″ diameter Teonex® Q65 flexible plastic substrate: (**a**) substrate with three 64 × 64 pixel arrays, (**b**) photograph of a fabricated pixel in the array (Sarma et al. 2003)

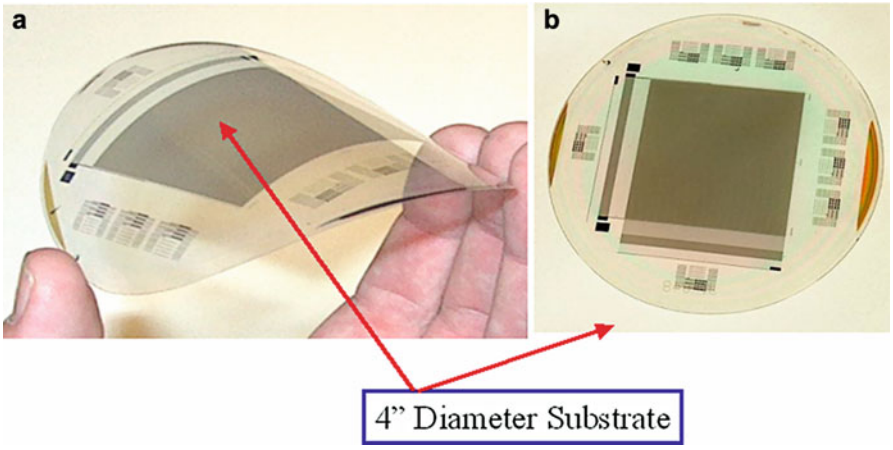

Fig. 7 Photograph of a 160 × 160(×3) pixel backplane fabricated on a flexible PEN plastic substrate illustrating its flexural capability

mask levels during the TFT processing as the substrate dimension changes due to shrinkage and moisture absorption. Using the substrate prestabilization process, and SiN_x barrier layers, acceptable dimensional stability and layer-to-layer alignment accuracy sufficient for fabricating functional backplanes and displays was achieved. Figure 8 illustrates the layer to layer registration achieved at the four corners (UL, upper left; UR, upper right; LL, lower left; and LR, lower right) of a 160(×3)×160 pixel backplane with a pixel pitch of 100 × 300 μm. While the registration was not perfect, the backplanes were found to be functional. The fabricated backplanes are

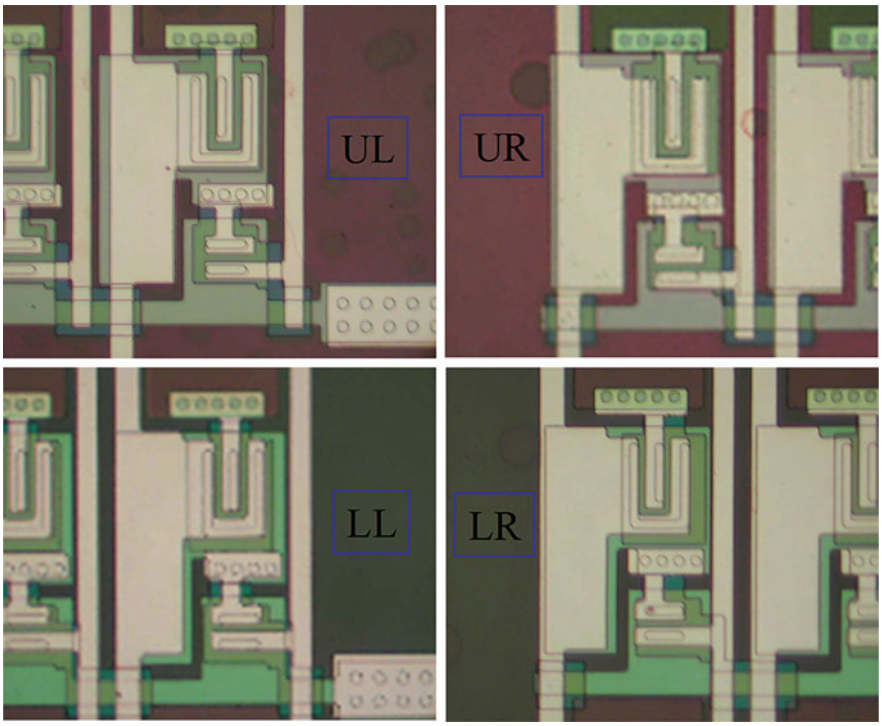

Fig. 8 Photograph illustrating that sufficient alignment accuracy is achieved at the four extreme regions of the fabricated 160 × 160(×3) pixel backplane for proper functioning of the backplane

then integrated with the OLED display media to complete flexible display fabrication.

Figure 9 shows the photographs of test images in the 64 × 64 pixel (Fig. 9a) and the 160 × 3 × 160 pixel (Fig. 9b) monochrome polymer OLED displays fabricated. To protect the OLED media, the display is laminated to a rigid glass substrate on the anode side of the OLED. As seen in Fig. 9, while these displays have some pixel and line defects, they do validate the 150 °C a-Si TFT process, and the backplane design for a flexible AM OLED. The fabricated displays were capable of displaying grayscale images and full motion video. The control displays fabricated using glass substrates were found to perform similarly except for having fewer pixel and line defects. The surface quality of the PEN plastic substrate was found to have a significant impact on the quality of the displays fabricated with respect to pixel and line defects observed. Displays fabricated on PEN substrates with improved surface quality exhibited significantly fewer display defects. To fully demonstrate the flexible display concept, Sarma et al. integrated Barix thin film encapsulation (Sarma et al. 2007; Moro et al. 2006), with the flexible backplanes and a red

Fig. 9 (**a**) Photographs of images being displayed on a 64 × 64 pixel AM OLED and a (**b**)160(×3)×160 pixel AM OLED fabricated using a flexible PEN plastic backplane built with low-temperature a-Si TFTs (Sarma et al. 2004, 2007)

phosphorescent OLED display media. The Barix (barrier film) is of the order of only a few microns. Thus the thickness of the flexible display fabricated is about ~130 μm. Figure 10a and b shows the photographs of a flexible AM OLED test display fabricated along with its flexural capabilities (Sarma et al. 2007). Figure 10c shows a schematic cross-section of the flexible AM OLED display fabricated.

While the concept of flexible AM OLED displays using direct fabrication on flexible PEN plastic displays has been demonstrated for a display size of up to ~5 cm × 5 cm with a resolution of 80 ppi, significant improvements in flexible substrate with respect to reduction of shrinkage and CTE mismatch with the TFT thin films is necessary for extending this approach for larger size and higher resolution flexible displays. In addition, development of methods for mechanical handling of the thin flexible backplanes during the TFT processing are essential for realizing large area backplanes and flexible displays.

ULTPS on Plastic Substrates

Polysilicon TFTs have the advantage of providing high mobility and CMOS option for integrating the row and column drivers in the flexible display. ULTPS approaches where the process temperature is kept under <200 °C (Kwon et al. 2006; Gosain and Usui 2000) for direct fabrication flexible backplanes and displays are attractive. However, several challenges such as achieving good low-temperature gate dielectrics that result in low-leakage currents and stable threshold voltages remain to be resolved to realize the potential of ULTPS TFTs. Because of these challenges in direct fabrication of polysilicon TFTs on plastic substrates, alternate processing strategies are being pursued. These strategies are discussed in sections "Device Layer Transfer (DLT) Process," "Temporary Substrate Bonding and Debonding" and "In Situ Plastic Coating on a Temporary Substrate."

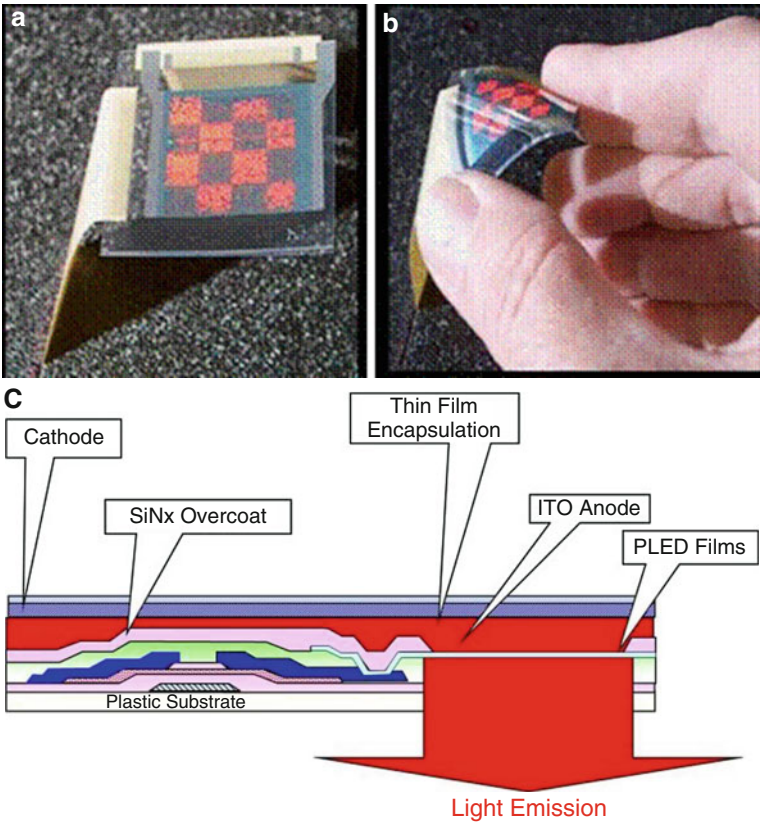

Fig. 10 (**a**) Photograph of a checker board image on a 64 × 64 pixel AM OLED fabricated using a flexible PEN plastic backplane built with low-temperature a-Si TFTs and thin film encapsulation, (**b**) flexural capability of the display, and (**c**) schematic of the display cross-section (Sarma et al. 2007)

OTFT on Plastic Substrate

As OTFTs can be fabricated at low process temperatures (typically <150 °C), they can be processed directly on available flexible plastic substrates. There is much interest in the development of OTFTs for various applications in addition to the backplanes for active matrix displays, such as low-cost RFID tags, and other IoT (Internet of Things) sensor devices. Both small molecule and polymer organic materials are investigated for the OTFT applications. Also, both vacuum evaporation as well as solution processing techniques are considered for depositing the organic semiconductor for the TFT fabrication. OTFT technology is discussed in detail in chapters "► Organic TFTs: Vacuum-Deposited Small-Molecule Semiconductors," "► Organic TFTs: Solution-Processable Small-Molecule Semiconductors," and "► Organic TFTs: Polymers" of this handbook.

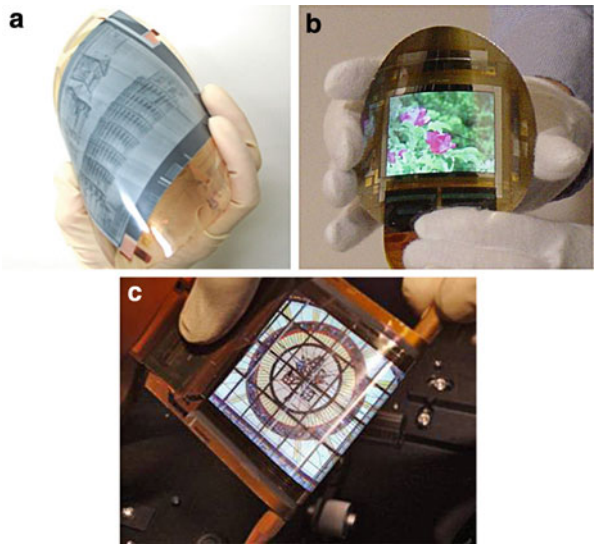

Fig. 11 Printed OTFT driven (**a**) 4.8″ VGA AM FPD, (**b**) 2.5″ QQVGA AM OLED, and (**c**) 4.1″, 80 μm thick, rollable OLED (121 ppi) in a rolled-up condition with a radius of 4 mm (Nomoto 2010; Noda et al. 2010)

OTFT backplanes have been successfully fabricated directly on low-temperature flexible plastic substrates to demonstrate flexible AM LCD, AM EPD, and AM OLED displays (e.g., Nomoto 2010; Burns et al. 2006; Burns 2010; Suzuki et al. 2008; Noda et al. 2010). Suzuki et al. (2008) demonstrated a 5.8-in. diagonal flexible phosphorescent color AM OLED using OTFT backplanes fabricated on flexible PEN plastic substrate. Pentacene used as the organic semiconductor was deposited by thermal evaporation. The OTFT exhibited a current on/off ratio of 10^6, and a mobility of 0.1 cm^2/Vs. The display had a resolution of 213 (RGB) $\times$120 pixel resolution with a pixel pitch of 42 ppi. Sony (Nomoto 2010; Noda et al. 2010) demonstrated very impressive flexible and rollable AM OLED and AM EPD displays driven by OTFTs as shown in Fig. 11. The 4.1″ wide AM OLED display has a resolution of 432 $\times$ RGXB $\times$ 240 pixels with a pitch of 121ppi. The thickness and bending radius of the rollable displays were 80 μm and $<$5 mm, respectively.

Direct Fabrication Using Stainless Steel Substrates

As stainless steel substrates are compatible with high temperature processing, conventional high temperature processes such as thermal oxide growth, thermal dopant activation, and silicide growth that are typically used for achieving superior device performance can be feasible. Stainless steel foil substrates are investigated for fabricating conventional a-Si TFT, LTPS TFT, and OSC-TFT backplanes for flexible EPD and OLED displays (Chuang et al. 2007; Kattamis et al. 2007; Arihara et al. 2009). Kattamis et al. (2007) have demonstrated the feasibility of fabricating a-Si TFT backplanes directly on 125 μm thick, 5 $\times$ 5 cm^2 stainless steel foil substrates after planarizing the surface with 2.5 μm thick siloxane spin-on-glass

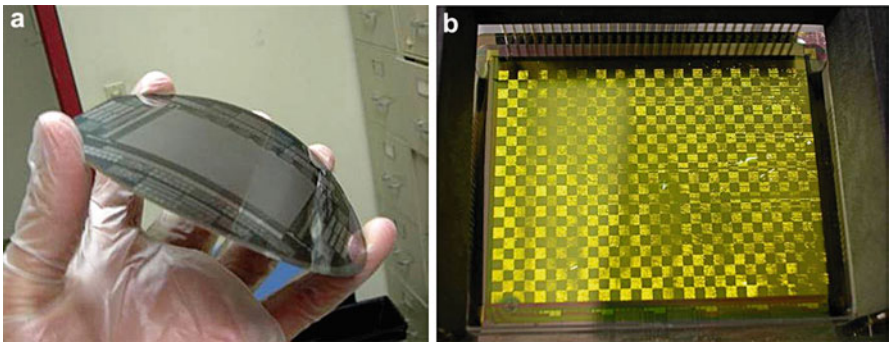

Fig. 12 Flexible stainless steel backplane (**a**) and the 3.3″, 640 × 480 pixel AM OLED display (**b**) fabricated using direct fabrication of LTPS TFT backplane on a stainless steel foil substrates (Kattamis et al. 2007)

dielectric, using a 280 °C a-Si TFT process. They used these backplanes to demonstrate top emission AM OLED displays. Figure 12 shows (Kattamis et al. 2007) the flexible stainless steel backplane and the AM OLED display fabricated using the direct fabrication of LTPS TFT on stainless steel foil substrates.

Chuang et al. (2007) reported fabrication of LTPS TFT backplanes on 100 um thick, type 304 stainless steel substrates. The substrates were first polished to a surface roughness of about 1 nm and then a passivation layer of PE CVD SiO_2 is deposited to isolate the conductive substrate from LTPS TFT backplane fabricated using excimer laser recrystallized LTPS. Process temperatures up to 700 °C were utilized for dopant thermal activation. Arihara et al. (2009) demonstrated fabrication of In-Ga-Zn-Oxide TFT backplanes on stainless-used-steel (SUS) substrates using process temperatures up to 300 °C. These backplanes are then integrated with white OLED display media and a flexible color filter array fabricated on PEN substrates. The 4.7-in. diagonal full color OLED display had a QVGA (320 × RGB × 240) resolution and a panel thickness of 0.4 mm.

Device Layer Transfer (DLT) Process

The DLT process involves standard (high temperature) TFT fabrication on a conventional display glass substrate, followed by transfer of the TFT circuit (backplane) on to a flexible plastic substrate by adhesive bonding at a lower temperature (e.g., less than 150 °C). This approach is pursued by multiple companies (Utsunomiya et al. 2003; Inoue et al. 2002; Miyasaka 2007; Miyasaka et al. 2006; Asano et al. 2003) for flexible display and flexible electronics application. Seiko Epson refers to this process as SUFTLA (surface-free technology by laser annealing) and has made significant advances to this approach in recent years.

More specifically, the SUFTLA technology involves transferring high-performance, LTPS TFT backplane (circuits) fabricated on a conventional display

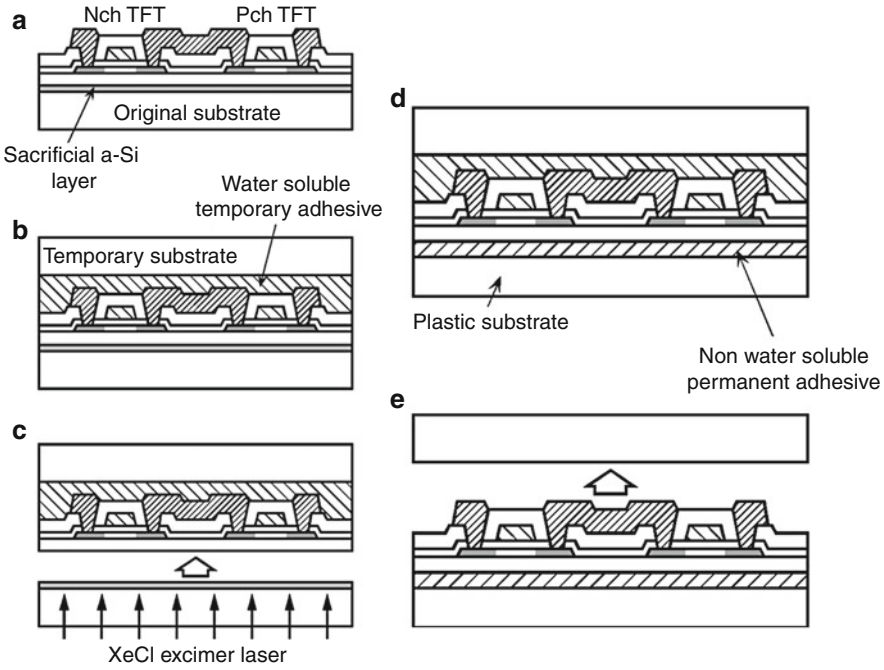

Fig. 13 Device Layer Transfer (*DLT*) process by SUFTLA approach (Miyasaka 2007)

glass substrate with an exfoliation layer (sacrificial a-Si layer), to a flexible plastic sheet as shown in Fig. 13. The SUFTLA process consists of two transfer steps. First, a sacrificial amorphous silicon (a-Si) layer is formed on an original glass substrate (Fig. 13a), followed by conventional CMOS LTPS TFT backplane fabrication. This substrate is then attached to a temporary substrate with a water soluble adhesive as shown in Fig. 13b on the device / top side. Next, Xe Cl excimer laser light is irradiated onto the amorphous silicon layer from the back of the original glass substrate to trigger release of the TFT backplane circuitry from the glass substrate as shown in Fig. 13c. The amorphous silicon layer absorbs the laser light to weaken the adhesion between TFT devices and the original glass substrate. Thus, polysilicon TFT devices are transferred onto the temporary substrate. The second transfer step starts with laminating the back side of the TFT devices onto the final plastic substrate, using a permanent adhesive that is not water soluble as shown in Fig. 13d. The substrate is then submerged in water to separate from the temporary substrate as the temporary adhesive dissolves, thereby transferring the high performance LTPS CMOS backplane on the flexible plastic substrate as shown in Fig. 13e. These high performance backplanes are then used to fabricate and demonstrate a variety of flexible displays including AM LCD, AM EPD, and AM OLED and other flexible electronics devices such as finger print sensors as shown in Fig. 14, with the Y-axis showing the number of TFTs on plastic, and the Y-axis showing the year the device was demonstrated. The paperback-sized displays up to 131 × 98 mm with

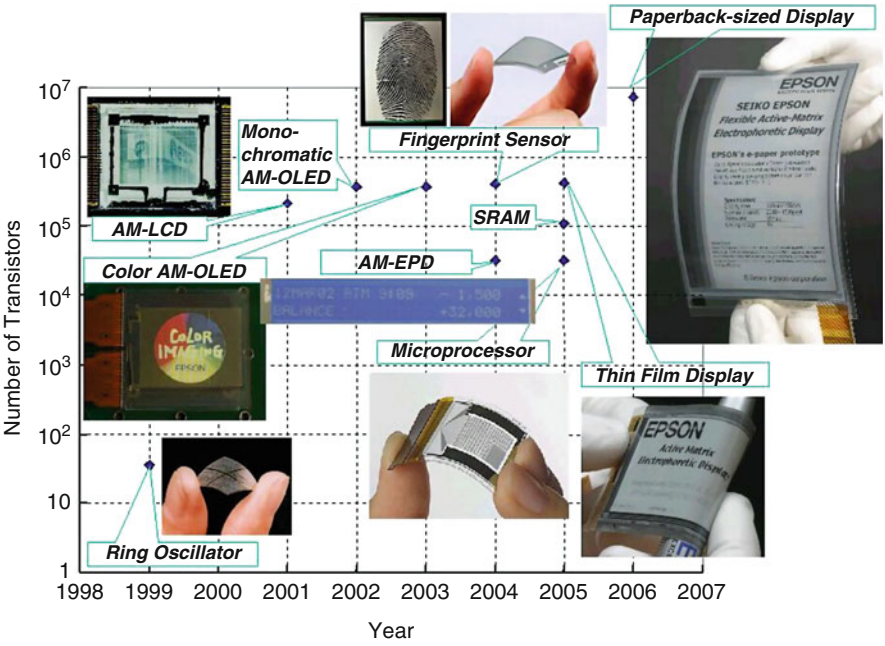

Fig. 14 SUFTLA technology progression (Miyasaka 2007)

the scan and data drivers integrated with over seven million TFTs have been successfully demonstrated on plastic substrates. SUFTLA has the potential to fabricate very high quality flexible displays, using high mobility and stable LTPS TFT technology.

Practical considerations for this approach include cost and yield. The extra cost associated with the a-Si sacrificial layer deposition and the two transfer steps in the fabrication of the flexible TFT backplane need to be minimized. However, the main issues that remain to be resolved for this approach particularly for large size flexible displays include defect control and yield. The transfer yield can have a major impact on the cost of the SUFTLA process. Defects such as air bubbles, dust, and particles in the water-soluble adhesive that prevent adhesion to the temporary substrate can create defects that impact the yield. While small size displays will have less of an issue with yield, large size displays can have significant yield issue to resolve, as the yield decreases exponentially with the display size.

Temporary Substrate Bonding and Debonding

The temporary substrate bonding and debonding approach (Paek et al. 2006; Hwang et al. 2007; Raupp et al. 2007; O'Rourke et al. 2008; Loy et al. 2009; Ma et al. 2010) involves laminating the flexible substrate to a rigid temporary substrate such as a

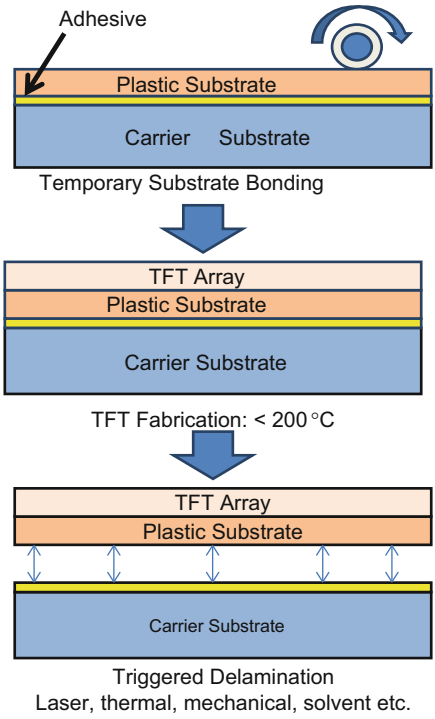

Fig. 15 Bond–debond approach

glass or a ceramic substrate (for example by using a temporary adhesive), fabricating the TFT backplane and debonding/separating the flexible substrate with the TFT backplane from the temporary substrate, as illustrated in Fig. 15. Bonding to a rigid temporary substrate greatly improves the ease of handling the flexible substrate and facilitates using conventional TFT processing equipment to fabricate the backplane. The issues in this approach include: (1) temperature constraints imposed by the temporary adhesive, (2) potential for chemical contamination by the temporary adhesive during the TFT processing, (3) yield of the bonding and debonding (of the flexible substrate / backplane from the rigid carrier substrate) operations with complete removal of the temporary adhesive, (4) cost of the bonding and debonding operations, and (5) cost of the temporary substrate if it is not reuseable, or has limited reuseability.

Flexible backplanes and displays using flexible plastic as well metal foil substrates and display media such as EPD and OLED have been fabricated. Paek et al. (2006) demonstrated a 10.1″ SVGA flexible monochrome AM EPD, with a thickness of 0.3 mm, using this approach with a metal foil substrate as shown in Fig. 16. Hwang et al. (2007) demonstrated a flexible AM FPD display using this approach with a 120 °C a-Si TFT backplane on a flexible PEN plastic substrate as shown in Fig. 17. This is a 14.3-in. (A4 size) display with a 1280 × 900 pixel resolution with a +/− 15 V drive. FDC has demonstrated (Raupp et al. 2007;

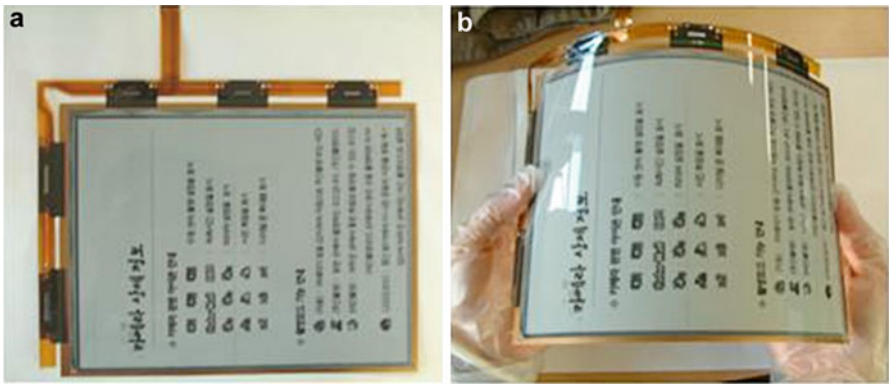

Fig. 16 Photographs of a (**a**) functioning 10.1 in. SVGA flexible AM EPD (e-book display) using an a-Si TFT backplane on a stainless steel substrate, in a flat condition and (**b**) under flexure (Paek et al. 2006)

Fig. 17 Photograph of an AM EPD display fabricated using low-temperature a-Si TFTs backplane on a flexible PEN plastic backplane (Hwang et al. 2007)

O'Rourke et al. 2008; Loy et al. 2009) flexible AM EPDs and AM OLEDs using PEN plastic substrates as well as flexible metal foil substrates and a-Si TFT backplanes processed at 180 °C. Ma et al. (2010) demonstrated fabrication of a-Si TFT backplanes on flexible stainless steel substrates at 200 °C using this approach. These backplanes have been integrated with phosphorescent OLED media to demonstrate full color 4-in. diagonal QVGA displays with a thickness of 0.3 mm as shown in Fig. 18, for a rugged wrist display application.

Fig. 18 Photographs of a 4-in. flexible AMOLED panel fabricated using low-temperature a-Si TFT backplane on a stainless steel substrate, under inward and outward bending (Ma et al. 2010)

In Situ Plastic Coating on a Temporary Substrate

Figure 19 illustrates the in situ plastic coating backplane process strategy (Battersby and Fench 2006; French et al. 2007; French 2009; Pecora et al. 2008). This strategy involves coating a low-TCE polyimide (PI) film on a glass substrate with a sacrificial layer. This coated PI film serves as a flexible substrate. The backplane circuit is then processed on the PI surface using conventional TFT processes and equipment. The fabricated backplane on the flexible PI film (substrate) is then released (separated) from the temporary rigid substrate, by a proprietary trigger release mechanism involving a thermal, optical, or mechanical process. Philips (Battersby and Fench 2006; French et al. 2007; French 2009) has developed this approach initially for flexible a-Si TFT backplanes for e-paper type displays and has named it EPLAR (Electronics on Plastic by *La*ser Release) process. This process involves two extra process steps compared to a conventional a-Si TFT process on a rigid glass substrate. The first is an additive process of spin-coating a 10 μm thick polyimide layer (which subsequently becomes the self-supporting flexible substrate / backplane). The temperature capability of this polyimide layer exceeds the requirements of the conventional a-Si TFT process, thus it can be processed in conventional a-Si TFT backplane fabrication facilities using standard processes. Electrophoretic display media is then laminated to the TFT backplane, and the resulting display on the polyimide foil is then separated from the rigid carrier glass substrate by a laser release process which relies on the appropriate glass surface treatments prior to the polyimide spin coating, and use of the appropriate type of polyimide. Flexible electrophoretic displays have been demonstrated using this process. This process can be adapted for the fabrication of LTPS-TFT or OSC-TFT backplanes, and other display media such as an OLED.

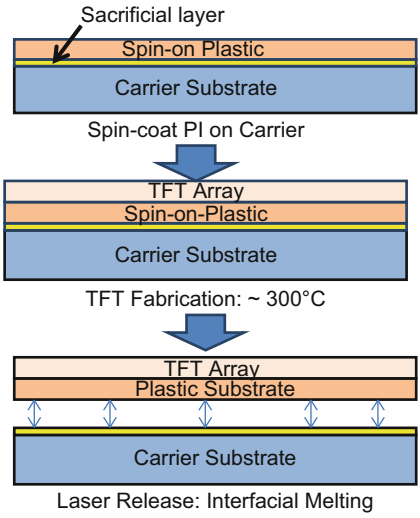

Fig. 19 In situ coating of plastic

Figure 20 shows a photo of a 9.7″ flexible e-paper display (French 2009) using a-Si TFT backplane on a thin PI substrate and EPD display media.

ITRI (Cheng-Chung et al. 2010; Cheng et al. 2009) demonstrated this process using a separate debonding layer (DBL), unlike the EPLaR process. In the ITRI process, the PI material is custom synthesized. The PI solution is coated after depositing a DBL on a glass temporary substrate. The area covered by PI is intentionally made larger than of DBL's. The glass substrate was then subjected to the TFT backplane fabrication process on Gen 2 glass line. Top gate a-Si:H and μc-Si TFTs were fabricated by a 6-mask process at 200 °C. Since PI's edges extend over the underlying DBL and are in direct contact with the glass, it adheres securely to the glass carrier during the entire TFT process. As a result, alignment of TFT layers on the PI substrate can be maintained throughout the process. In other words, the thermally induced misalignment issue can be largely avoided here. Due to the DBL's weak adhesion with PI film, the PI layer with TFT device can be easily separated from glass by simply cutting the circumference of the PI layer where the cutting line is within the edges of the DBL. Figure 21 shows examples of a flexible AM OLED (a) and flexible AM EPD (b) demonstrated (Cheng-Chung et al. 2010) by this process. Jang et al. (2010) developed this process using an ultra-thin buffer layer coating prior to the PI spin coating. They utilized this structure to fabricate amorphous IGZO backplanes at 200 °C for driving AM OLED displays.

Samsung (Jin et al. 2009, 2010; An et al.) developed this process using a plastic film coating with attractive manufacturable properties such as very low CTE (~3 ppm/K) and high temperature processing capability (up to 350 °C), and a room temperature delamination process that makes no electrical and mechanical damage to TFTs. This approach is used to fabricate flexible backplanes using OSC-TFTs, LTPS-TFTs, and AM OLED displays using these backplanes. The top emission mode was used for organic light emitting diode (OLED) structure, and thin

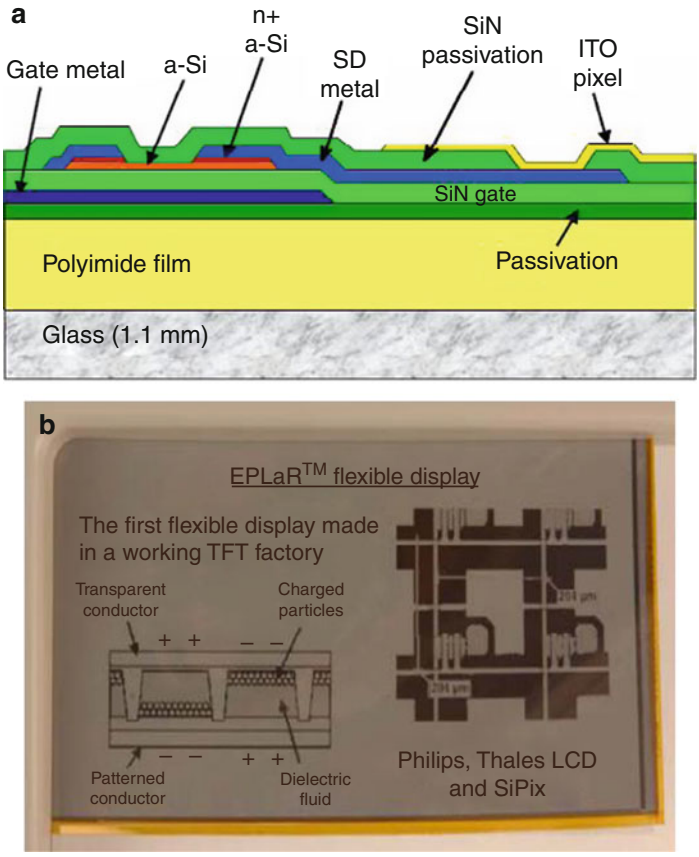

Fig. 20 Cross-section of an EPLAR a-Si TFT array while it is still anchored to a glass substrate (**a**), and photograph of a laser released EPLAR display (**b**) (French et al. 2007)

film encapsulation was applied for flexible encapsulation. Figure 22 shows (An et al.) a 2.8-in., QVGA, full color top emission AM OLED display demonstrated using this approach.

TFT Backplane Fabrication by Direct Printing

Direct pattern printing is a very attractive approach for fabricating each layer of the TFT structure for the flexible backplane and display fabrication. Compared to the conventional thin film deposition and photolithographic processes, direct pattern printing process can be more compatible with use of flexible plastic substrates, and low-cost roll-to-roll processing. Printing is also expected to have a low environmental impact because of small number of process steps, small amount of materials used, and high throughput. Direct pattern printing method requires both printing materials

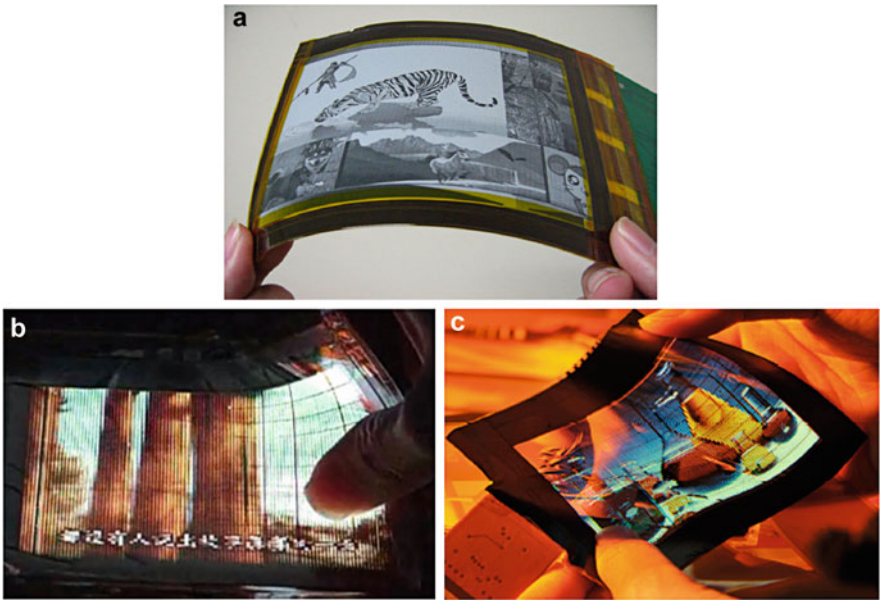

Fig. 21 Photographs of flexible displays fabricated by the in situ plastic coating method using a separate debonding layer: (**a**) 6″ SVGA AM EPD, (**b**) 4.1″ a-Si TFT AM OLED, and (**c**) 4.1″ μc-Si TFT AM OLED (Cheng-Chung et al. 2010)

Fig. 22 Photograph of a flexible 2.8″ QVGA AM OLED fabricated by the in situ plastic coating method involving a plastic film with a CTE of 3 ppm/K and process temperature capability of 350 °C, and LTPS TFTs (An et al. 2010)

(semiconductor ink for the transistor active layer, conductor inks for the bus lines and pixel electrode, and dielectric ink for the dielectric and passivation layers) and printing methods. All inks must meet the full set of requirements to serve their respective functions for the desired TFT device operation. Silver ink is an example candidate for the bus lines. Candidate inks for the transparent pixel electrode include ITO nanoparticles, CNTs, and metal nanowires. Candidate printing methods include ink-jet printing, offset printing, micro-contact printing, imprinting, gravure printing,

flexo-printing, and screen printing. Each printing method has its own advantages and limitations, and different printing methods are better suited for each layer of the TFT structure.

Ink-jet printing of OTFTs is an important topic in large area, printable, and flexible displays and electronics due to its low-temperature processing being compatible with low-thermal budget of the available plastic substrates (Sujuki et al. 2009; Hong and Chung 2010). Since, at this stage of development it is generally difficult to optimize printing conditions of materials for all different TFT functional layers, especially for organic dielectric and semiconductor layers, the inkjet printing process has been used in combination with other solution or vacuum based fabrication methods to demonstrate solution-processable OTFTs. Suzuki et al. (2009) demonstrated a 200 ppi all-printed organic TFT backplane and a flexible EPD display. The bottom gate OTFT structure used surface energy controlled silver nanoparticle ink jet deposition for the gate and source-drain layers, and ink jet printing of organic semiconductor. A spin coated novel polyimide was used as a gate dielectric. The insulator and pixel electrodes were fabricated by screen printing. All these layers were printed under ambient conditions with a maximum process temperature of 180 °C to fabricate OTFTs with a channel length of 5 μm and a mobility of 0.1 cm^2/Vs. This backplane is used to demonstrate a 3.2-in. diagonal, 540 × 360 pixel electrophoretic displays.

While progress is made on printable OTFTs and backplanes, several technical issues still remain to be resolved (Hong and Chung 2010). Although printed OTFTs with a reasonable performance have been demonstrated, there are still several remaining technical challenges in materials and device structures for developing high performance all-inkjet printed organic thin-film transistors. The issues that remain to be resolved include: formation of narrow, high aspect ratio, metal lines with low sheet resistance, optimum processing and curing conditions for a printed, defect free, high-quality organic gate dielectric layer, surface energy and wetting issues for the printed organic semiconducting layer, and contact resistance between source/drain electrodes and the organic semiconducting layer, especially for the bottom-contact organic thin film transistor structure.

Roll-to-Roll (RTR) Processing

Currently the popular approaches for fabricating flexible backplanes and displays are based on a plate-to-plate type approach involving TFT fabrication on a flexible substrate attached (laminated) to a rigid carrier substrate as discussed in sections "Temporary Substrate Bonding and Debonding" and "In Situ Plastic Coating on a Temporary Substrate." These are batch type processes and use conventional vacuum deposition and lithographic patterning technologies. On the other hand, RTR process is a well-known technology that is commonly used in cost-effective manufacturing of some thin film devices on flexible substrates in a continuous fashion. RTR processing offers significant advantages compared to the conventional batch process, as it increases throughput by allowing greater levels of automation and by

eliminating the overhead time involved in loading and unloading panels into lithographic tools and chemical processing stations. However, there are many challenges in fabricating flexible TFT devices and backplanes, requiring multiple layers with small design rules and precise alignment between various layers, using an RTR process. The vacuum and the photolithographic processes which constitute the bulk of the current TFT fabrication are not compatible with true RTR processing, because the roll needs to stay stationary during the photolith exposure time.

The current efforts in the application of RTR processes for flexible backplanes and displays are directed towards realizing the benefit of integrating RTR process steps where feasible in to predominantly plate to plate processes. As an example, NEC (Takechi et al. 2010) reported on the development of a rollable flexible silicon TFT backplane utilizing a RTR continuous lamination process. The roll-to-roll TFT-backplane technology involves a glass-etching TFT transfer process and a roll-to-roll continuous lamination process. The transfer process includes high-rate, uniform glass-etching to transfer TFT arrays fabricated on a glass substrate to a flexible plastic film. In the roll-to-roll process, thinned TFT-glass sheets (0.1 mm) and a base-film roll are continuously laminated using a permanent adhesive. Choosing both an appropriate elastic modulus for the adhesive and appropriate tension strength to be used in the process is key to suppressing deformation of the TFT-backplane rolls caused by thermal stress. TFT backplanes that can be wound without any major physical damage such as cracking on a roll whose core diameter is approximately 300 mm have been demonstrated. In this case, while the actual TFT fabrication is conducted in a plate to plate process, RTR process is utilized for transferring/laminating the backplanes to a flexible plastic roll at a high rate and low cost.

HP Labs reported on their SAIL (self-aligned imprint lithography) technology (Taussig et al. 2010) that utilizes an imprinting process for the manufacture of TFT backplanes on plastic films. The SAIL process would eliminate the need for many photolithographic/resist etch steps which are expensive and have a low throughput. While the SAIL process still uses vacuum deposition and dry etching for the TFT layers, its cost advantage comes from completing all the layer deposition steps prior to any of the patterning steps, and using a monolithic 3D masking structure. The multiple patterns required to create the backplane are encoded in the different heights of a 3D masking structure that is molded on top of the thin film stack, before any of the etching steps. By alternately etching the masking structure and the thin film stack, the multiple patterns required for the backplane are transferred to the device layers. Because the mask distorts with the substrate perfect alignment is maintained regardless of process induced distortion. These backplanes have been used to demonstrate AM EPDs. While the SAIL process is not a true and complete RTR process, it still benefits from the RTR imprint patterning process.

Active-matrix TFT devices and backplanes fabricated completely by printing procedures, without use of any vacuum deposition steps and photolithographic patterning procedures, have the potential for full roll-to-roll fabrication and the associated ultimate low-cost benefits. At present, printable inks for the semiconductor and gate insulator materials are not available particularly for inorganic (a-Si,

LTPS and OSC) TFTs. At this time, OTFT technology appears to be closest to having the printable semiconductor and gate insulator materials and the potential for developing a more complete RTR process for backplane fabrication. Development of fine pattern printing technologies is also essential for realizing RTR technologies capable of fabricating high resolution flexible displays.

Other Technical Challenges for Flexible Displays

Throughout this chapter, up to now, we have discussed various barriers and technical challenges in the fabrication of flexible active matrix TFT backplanes and displays due to the characteristics of the available thin flexible metal and plastic foils. When we consider the actual operational aspects of the flexible electronics and displays based on plastic substrates, there are two other challenges that need to be addressed and resolved, namely self-heating effects and mechanical durability (Miyasaka et al. 2008; Fortunato et al. 2009). It is important to consider the mechanical durability during the flexible display operation, due to the very thin and fragile nature of flexible displays when they are bent with a very small radius or when folded. The characteristics of the flexible substrate selected (such as the TCE, young's modulus, thickness of the film, and its viscosity) can have an impact on the thermo-mechanical stresses generated during operation of the display (Miyasaka et al. 2008), and thus its durability. Mechanical durability issues during use need to be addressed by proper packaging/support for the flexible display during storage and during use that ensures that the backplane/display does not experience stains beyond the elastic limit.

Self-Heating Effects

Self-heating effects in TFTs on glass substrates are well known (Fortunato et al. 2009). When the TFT is in the on-state, the source–drain current results in Joule heating, which raises the temperature of the TFT and this effect is known as self-heating. This effect can present a significant challenge to flexible electronics and displays built on plastic substrates that have a very low thermal conductivity in comparison to the thermal conductivity of glass substrates. Table 5 shows the thermal conductivity of plastic substrates in relation to the typical TFT thin film materials and glass. The low thermal conductivity of plastic film prevents heat from dissipating from the semiconductor channel layer of the TFT, leading to the device temperature rise. Thus, for TFTs with identical performance, flexible plastic backplanes and displays exhibit greater susceptibility to self-heating than the backplanes and displays on glass substrates. Excessive temperature raise can lead to deformation of the plastic material or the delamination of the TFT devices from the substrate in addition to affecting the TFT device performance and consequently the display performance.

Table 5 Thermal conductivity of various TFT and substrate materials

Solid	Thermal conductivity ($WM^{-1}K^{-1}$)
Aluminum	2.39
Stainless steel	0.162
Polysilicon	1.55
Silicon	1.48
Amorphous silicon	0.018
SiO_2 glass	0.014
Polyimide	0.0052
Plastic films	~0.002

The display media used can also have an impact the severity of the self-heating problem. For, example, self-heating is expected to be bigger issue for flexible AM OLED displays that involve continuous current flow and heat generation through the OLED pixel compared to an AM EPD display that does not generate any light (or heat); EPD merely modulates the reflected ambient light.

Self-heating effects can be minimized by: (1) optimizing the shape of the TFT for effective heat dissipation; (2) improving the TFT electrical performance characteristics such as by improving the mobility and reducing the threshold voltage; (3) scaling the TFT dimensions such as channel length and dielectric thickness; and (4) utilizing energy-efficient drive circuits. With respect to optimizing the shape of the TFT, heat dissipation can be improved by utilizing several TFTs with a smaller channel width, W, connected in parallel as opposed to using a single TFT device with a large channel width, while maintaining the desired source-drain current. Self-heating effects can be greatly minimized by metal foil substrates with high thermal conductivity.

Summary, Recent Results, and Conclusions

During recent years, significant progress has been made on the development of flexible substrates and the compatible TFT processing methods for fabricating flexible backplanes and displays. Commercialization of some flexible display technologies has also commenced. While direct fabrication of TFT backplanes on available flexible substrates has been demonstrated for small size displays, this approach is not believed to be practical for large size displays, particularly when using inorganic TFTs requiring higher processing temperatures. The barriers for the direct fabrication approach for large size displays include issues of mechanical handling of thin, flexible, and self-supporting substrates through the current plate-to-plate, batch-type TFT process equipment, and dimensional stability issues due to shrinkage and CTE mismatch. While the direct processing strategy may be more amenable for low-cost RTR processing, significant advances are required in technologies required for direct TFT processing as well as RTR processing, for realizing a viable overall approach.

While the Device Layer Transfer (DLT) strategy can be practical for fabricating high quality flexible displays, yield and cost are the barriers to be overcome for use of this technology, particularly for large area flexible displays. Both bond–debond and in situ plastic coating methods have a significant potential for providing a viable path for fabricating flexible displays with various display media and a broad range of sizes. Flexible displays using both OLED and EPD are being developed very actively, while there are some efforts in the flexible LCD development as well. Very impressive flexible electrophoretic displays have been demonstrated using a-Si TFT, LTPS TFT, and OTFT backplanes, using plastic as well as metal foil substrates. Commercialization efforts are also under way for flexible AM EPDs for e-book and other very low-power display applications.

Because a flexible OLED is considered an ultimate display, the display industry is investing significant resources to further develop various technology elements to enable manufacturing of these displays. Development of a cost effective multilayer barrier film and its integration with the backplane and OLED display fabrication processes is an important enabling element to realize flexible AM OLED displays. Major progress has been made in developing high performance multilayer barrier films suitable for flexible AM OLEDs utilizing atomic layer deposition (ALD), for example as discussed in (http://www.lg.com/us/mobile-phones/gflex2). Important progress continues to be made in LTPS TFT, and OSC-TFT technologies for application to glass substrate based as well as flexible polymer substrate based AM OLED displays. Also, important advances continue to be made in the OLED media itself with respect to improved luminous efficiency, lower drive voltages, and longer life time. These advances relax the requirements of the active matrix TFT devices with respect to drive currents and TFT gate bias stress stability requirements to accelerate the flexible AM OLED development. Commercial production of flexible polymer substrate based AM OLEDs has already commenced with the introduction of LG's G-Flex (http://www.lg.com/us/mobile-phones/gflex2) and Samsung's Galaxy Round (http://www.gsmarena.com/samsung_galaxy_round_g910s-5766.php) smart phones. Similarly, AM OLEDs fabricated using a flexible polymer substrates have been used in the Samsung Galaxy S6 Edge smart phone (http://www.samsung.com/global/galaxy/galaxys6/galaxy-s6-edge) and Apple Watch (http://appleinsider.com/articles/14/09/29/apple-watchs-advanced-amoled-display-far-more-costly-than-traditional-screens—report). While these early commercial products benefit from the light weight and ruggedness (unbreakability) attributes of the flexible displays in small sizes, recent efforts such as LG Display's development and demonstration of a 18-in. flexible OLED display (Jonggeun et al. 2015) and SEL's manufacturing technology development and demonstration of a 13.3-in. 8 K $\times$ 4 K flexible AM OLED (Satoru et al. 2015) are targeted towards realizing expanded benefits of flexible displays.

Development of science and technology required for manufacturing of flexible displays, particularly flexible AM OLED display, is a tough technical challenge. While significant progress has been made in this endeavor, many technical issues still remain to be resolved as discussed in this chapter. However, the potential for successful development and broad commercialization of flexible AM OLEDs is high

because of the significant value proposition of the flexible display products and systems, high probability of the current approaches being pursued to resolving the current technical issues, and high levels of the industry investment in this technology.

Further Reading

An S, Lee J, Kim Y, Kim T, Jin D, Min H, Chung HK, Kim SS (2010) 2.8-inch WQVGA FLexible AMOLED using high performance low temperature polysilicon TFT on plastic substrates. SID 41:706–709

Arihara K, Kano M, Motai K, Naitou Y, Kadowaki M, Nakajima H, Tsuboi T, Kato C, Kishimoto Y, Maeda H (2009) Fabrication of flexible 4.7-inch QVGA AM-OLED panel driven by In-Ga-Zn-Oxide TFTs with flexible color filter. IDW'09, p 1613

Asano A, Kinoshita T, Otani N (2003) A plastic 3.8-in low-temperature polycrystalline silicon TFT color LCD panel. SID 03 Digest: 34:988–991

Battersby S, Fench I (2006) Plastic displays made by standard a-Si TFT technology. IMID/IDMC'06, Daegu, South Korea, p 1546

Burns S (2010) QUE: an e-reader built using flexible display technology. SID 10 Digest: 41:477

Burns SE et al (2006) A flexible plastic SVGA e-paper display. SID'06 Digest: 74

Carcia PF, McLean RS, Reilly MH (2005) Oxide engineering of ZnO thin-film transistors for flexible electronics. JSID 13:547

Cheng HC, Huang YS, Liu CJ, Li CW, Ho KY, Cheng CH, Peng SY, Chen YP, Lin HC, Kung BC, Lee PF, Huang JJ, Jiang LY, Lee CC (2009) Plastic substrate and backplane for flexible AM OLED by sheet to sheet process. IDW'09, Miyazaki, Japan, p 1601

Cheng-Chung Lee, Yu-Yang Chang, Hua-Chi Cheng, Jia-Chong Ho, Janglin Chen (2010) A novel approach to make flexible active matrix displays. SID 10 Digest: 41:810

Chuang TK, Troccoli M, Hatalis M, Voutsas A (2007) Polysilicon TFT technology on flexible metal foil for AM PLED displays. JSID 15(7):455

Chwang A, Hewitt R, Urbanik K, Silvernail J, Rajan K, Hack M, Brown J, Lu J P, Shih C, Ho J, Street R, Ramos T, Moro L, Rutherford N, Tognoni K, Anderson B, Huffman D (2006) Full color 100 dpi AM OLED displays on flexible stainless steel substrates. SID 06 Digest: 37:1858

Erlat AG, Yan M, Duggal AR (2009) Substrates and thin film barrier technology for flexible electronics. In: Wong WS, Sallelo A (eds) Flexible electronics. Springer. New York, NY

Eveson R, MacDonald WA, MacKerron D, Hadgson A, Adam R, Rakos K, Rollins K, Rustin R, Looney, Stewart J, Asai M, Hashimoto K (2008) Optimizing polyester films for flexible electronics applications. SID 08 Digest: 39:1431

Fortunato G, Cuscuna M, Gaucci P, Maiolo L, Mariucci L, Pecora A, Valletta A, Templier F (2009) Self-heating effects in p-channel polysilicon TFTs fabricated on different substrates. J Kor Phys Soc 54(1):455

French I (2009) Flexible E-books. SID 09 Digest: 40:100

French I, George D, Kretz T, Templier F, Lifka F (2007) Flexible displays and electronics made in AM-LCD facilities by the EPLaRTM process. SID 07 Digest: 38:1680

Gleskova H, Wagner S (1999) Amorphous silicon thin-film transistors on compliant polyimide foil substrates. IEEE Electron Dev Lett 20(9):473

Gleskova H, Wagner S (2001) DC-Gate Bias stressing of a-Si:H TFTs fabricated at 150° C on polyimide foil. IEEE Trans Electron Dev 48(8):1667

Gosain DP, Usui TNS (2000) High mobility thin film transistors fabricated on plastic substrates as process temperature of 110°C. Jpn J Appl Phys 39L:179

Graff G, Burrows PE, Williford RE, Praino RF (2005) Barrier layer technology for flexible displays. In Crawford GP (ed) Flexible flat panel displays. Wiley, Chichester, England

Gundlach DJ, Kuo DJ, Nelson CC, Jackson TN (1999) Organic thin film transistors with field effect mobility > $2Cm^2$/V-sec. IEEE Electron Device Lett pp 164–165

He S, Nishiki H, Hartzell, J, Nakata Y (2000) Low temperature PECVD a-Si TFT for plastic substrate. SID Digest 2000: 278–281

Hirao T, Furuta M, Furuta H, Matsuda T, Hiramatsu T, Hokari H, Yoshida M (2006) High mobility top-gate zinc oxide thin film transistors (ZnO-TFTs) for active matrix liquid crystal displays. SID 06 Digest 37:18–21

Hong Y, Chung S (2010) Technical issues towards all inkjet-printed organic thin-film transistors. SID 10 Digest 41:1147

Hwang TH, Lee W, Hong WS, Kim SJ, Kim SI, Roh NS, Nikulin I, Choi JY, Jeon HI, Hong S J, Lee JK, Han MJ, Baek SJ, Meonghee Kim, Son Uk Lee, Shin SS (2007) 14.3 inch active matrix-based plastic electrophoretic display using low temperature processes. SID 07 Digest 38:1684

Inoue S, Utsunomiya S, Saeki T, Shimoda T (2002) Surface-free technology by laser annealing (SUFTLA) and its application to poly-Si TFT-LCDs on plastic film with integrated drivers. IEEE Trans Electron Devices 49(8):1353

Jang J, Choi MH, Cheon JY (2010) TFT Technologies for flexible displays. SID 10 Digest 41:1143

Jin DU, Jeong JK, Kim TW, Lee JS, Ahn TK, Mo YK, Chung HK (2006a) Flexible AM OLED display on stainless steel foil. JSID 14(2):1083

Jin DU, Jeong JK, Shin HS, Kim MK, Ahn TK, Kwon SY, Kwack JHo, Kim TW, Mo YG, Chung HK (2006b) 5.6-inch Flexible full color top emission AM OLED display on stainless steel foil. SID 06 Digest 37:1855

Jin DU, Lee JS, Kim TW, An SG, Straykhilev D, Pyo YS, Kim HS, Lee DB, Mo YG, Kim HD, Chung HK (2009) World-largest (6.5") flexible full color top emission AMOLED display on plastic film and its bending properties. SID 09 Digest 40:983

Jin DU, Kim TW, Koo HW, Stryakhilev D, Kim HS, Seo SJ, Kim MJ, Min HK, Chung HK, Kim SS (2010) Highly robust flexible AM OLED display on plastic substrate with new structure. SID 10 Digest 41:703

Jonggeun Y, Hoiyong Kn, Mireum L, Youn-yeol Y, Nuri C, Min S, Choi J e I, Kwonhyung L, Jungsik J, Hojin K, Hyunmin C, Yongbaek L, Choongkeun Y, Seunghee K, Mingu C, Seyeoul K, Weonseo P, Sooyoung Y, Inbyeong K, Sangdeog Y (2015) World 1st large size 18-inch flexible OLED display, and the Key technologies. SID'15 Digest 46:962

Kamiya T, Nomura K, Hosono H (2009) Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping. J Disp Technol 5(7):273

Kattamis AZ, Giebink N, Cheng CC, Wagner S, Forrest SR, Hong Y, Cannella V (2007) Active-matrix organic light-emitting displays employing two thin-film-transistor a-Si:H pixels on flexible stainless-steel foil. JSID 15(7):433

Kwon JY, Jung JS, Park KB, Kim JM, Lim H, Lee SY, Kim JM, Noguchi T, Hur JH, Jang J (2006) 2.2 inch qqVGA AM OLED driven by Ultra Low Temperature Poly Silicon (ULTPS) TFT direct fabricated below 200 °C. SID'06 Digest 37:1358–1361

Long K, KattamiA Z, Chen IC, Gleskova H, Wagner S, Sturm J (2006) Stability of amorphous silicon TFTs deposited on clear plastic substrates at 250 °C to 280 °C. IEEE Electron Dev Lett 27(2):111

Loy D, Lee YK, Bell C, Richards M, Bawolek E, Ageno S, Moyer C, Marrs M, Venugopal SM, Kaminski J, Colaneri N, O'Rourke SM (2009) Active matrix PHOLED displays on temporary bonded polyethylene naphthalate substrates with 180 °C a-Si:H TFTs. SID 09 Digest 40:988

Ma R, Rajan K, Silvernail J, Urbanik K, Paynter J, Mandlik P, Hack M, Brown JJ, Yoo JS, Jung SH, Kim YC, YoonS Y, Kim CD, Kang IB, Hwang YK, Chung IJ, Tognoni K, Anderson R, Huffman D (2010) Wearable 4-in. QVGA full-color-video flexible AMOLEDs for rugged applications. JSID 18(1):50

MacDonald WA (2004) Engineered films for display technologies. J Mater Chem 14:4–10

MacDonald WA, Mace JM, Polack NP (2002) In: 45th annual technical conference proceedings of the Society of Vacuum Coaters, Lake Buena Vista, FL, USA p 482

MacDonald WA, Eveson R, MacKerron D, Adam R, Rollins K, Rustin R, Looney MK, Hashimoto K (2006) The impact of environment on dimensional reproducibility of polyester film during flexible electronics processing. SID 06 Digest 37:414

Miyasaka M (2007) Suftla flexible microelectronics on their way to business. SID 07 Digest 38:1673

Miyasaka M, Nebashi S, Shimoda T (2006) Suftla flexible active-matrix electrophoretic displays. IMID/IDMC '06 DIGEST, Daegu, South Korea, p 466

Miyasaka M, Hara H, Karaki N, Inoue S, Kawai K, Nebashi S (2008) Technical obstacles to thin film transistor circuits on plastic. Jpn JAP 47(6):4430

Mo YG, Kim M, Kang CK, Jeong JH, Park YS, Choi CG, Kim HD, Kim SS (2010) Amorphous oxide TFT backplane for large size AM OLED TV. SID 10 Digest 41(1):1037–1040

Moro M, Chu X, Hirayama H, Krajewski T, Visser RJ (2006) A mass manufacturing process for Barix encapsulation of OLED displays. IMID/IDMC 23 Aug. Daegu, South Korea

Noda M, Kobayashi N, Katsuhara M, Yumoto A, Ushikura SI, Yasuda RI, Hirai N, Yukawa G, Yagi I, Nomoto K, Urabe T (2010) A rollable AM-OLED display driven by OTFTs. SID 10 Digest 41:710

Nomoto K (2010) Development of flexible displays driven by organic TFTs. SID 10 Digest 41:1155

Nomura K, Ohta H, Takagi A, Kamiya T, Hirano M, Hosono H (2004) Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. Nature 41:432:488

O'Rourke SM, Venugopal SM, Raupp GB, Allee DR, Ageno S, Bawolek EJ, Loy DE, Kaminski JP, Moyer C, O'Brien B, Long K, Marrs M, Bottesch D, Dailey J, Trujillo J, Cordova R, Richards M, Toy D, Colaneri N (2008) Active matrix electrophoretic displays on temporary bonded stainless steel substrates with 180 °C a-Si:H TFTs. SID 08 Digest 39:422

Paek SH, Kim KL, Seo HS, Jeong YS, Yi SY, Lee SY, Choi NB, Kim SH, Kim CD, Chung IJ (2006) 10.1 inch SVGA Ultra thin and flexible active matrix electrophoretic display. SID 06 Digest 37:1834

Paek SH, Park YI, Park CH, Lim YS, Shin SI, Kim CD, Hwang YK (2010) Flexible display technology for a mass production using the improved etching technology. SID 10 Digest: 1047

Pecora A, Maiolo L, Cuscuna M, Simeone D, Minotti A, Mariucci L, Fortunato G (2008) Low-temperature polysilicon thin film transistors on polyimide substrates for electronics on plastic. Solid-State Electron 52:348–352

Raupp G (2007) Active matrix TFT technology development and pilot line manufacturing for reflective and emissive flexible displays. In: Proceedings of USDC flexible displays & micro-electronics conference & exhibit, Phoenix, AZ, USA, 5–8 Feb 2007

Raupp GB, Colaneri N, O'Rourke SM, Kaminski J, Allee DR, Venugopal SM, Bawolek EJ, Loy DE, Moye C, Angeno SK, O'Brien BP, Bottesch D, Rednour S, Blanchard R, Marrs M, Dailey J, Long K (2006) Flexible display technology in a pilot line manufacturing environment. Army science conference, Orlando, 27–30 Nov 2006

Raupp GB, O'Rourke SM, Moyer C, O'Brien BP, Ageno SK, Loy DE, Bawolek EJ, Allee DR, Venugopal SM, Kaminski JP, Bottesch D, Dailey J, Long K, Marrs M, Munizza MR, Haverinen H, Colaneri N (2007) Low-temperature amorphous-silicon backplane technology development for flexible displays in a manufacturing pilot-line environment. JSID 15(7):445

Sarma KR, Chanley C, Dodd S, Roush J, Schmidt J, Srdanov G, Stevenson M, Yu G, Wessel R, Innocenzo J, O'Regan M, MacDonald WA, Eveson R, Long K, Gleskova H, Wagner S, Sturm JC (2003) Flexible Active matrix OLED using 150 °C a-Si TFT Backplane. Cockpit Displays X, Proceedings of the SPIE 2003, pp 180–191

Sarma KR, Schmidt J, Roush J, Dodd S, Chanley C (2004) Active matrix OLED displays using a-Si TFT backplanes fabricated on flexible plastic substrates. In: Proceedings of the SPIE defence displays conference, Orlando, FL, USA, Apr 2004

Sarma KR et al (2007) Flexible OLED displays. In: Proceedings of AM FPD'07, Hugo, 2007

Satoru I, Masakatsu O, Koichi T, Seiji Y, Masataka S, Naoya S, Kenichi O, Kohei Y, Shingo E, Yoshiharu H, Shunpei Y (2015) Apparatus for manufacturing flexible OLED displays: adoption of transfer technology. SID'15 Digest 46:8

Sujuki S, Yutani K, Nakashima M, Onodera A, Mizukami S, Kato M, Tano T, Tomono H, Yanagisawa M, Kameyama K (2009) A 200 ppi all-printed organic TFT backplane for flexible electrophoretic displays. IDW'09, Miyazaki, Japan, p 1581

Suzuki M, Fukagawa H, Nakajima Y, Suzuki T, Yamamoto T, Tokito S (2008) 5.8-inch Phosphorescent color AM-OLED display driven by OTFTs on plastic substgrate. IDW'08, Nigata, Japan, p 1515

Takechi K, Yamaguchi S, Tanabe H, Kaneko S (2010) Development of rollable silicon thin-film-transistor backplanes utilizing a roll-to-roll continuous lamination process. JSID 18(6):391

Taussig C, Cobene R, Elder R, Jackson W, Jam M, Jeans A, Luo H, Maltabes J, Mei P, Smith M, Perlov C, Zhao L (2010) Roll-to-roll manufacturing of backplanes for paper-like displays. SID 10 Digest: 41:1151

Utsunomiya S et al (2003) Flexible color AM OLED display fabricated using surface free technology by laser ablation / annealing (SUFTLA^{TM}). SID 03 Digest 34:864–867

Wagner S, Han L, Hekmatshoar B, Song K, Mandlik P, Cherenack KH, Sturm J (2010) Amorphous silicon TFT technology for rollable OLED displays. SID 10 Digest 41(1):917

Suggestions for Further Reading on Poly-Si TFTs

Wong WS, Salleo A (eds) (2009) Flexible electronics: materials and applications. Springer, Chichester, England