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# Oxide TFTs

Toshio Kamiya and Hideo Hosono

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## Abstract

Research on oxide semiconductor has advanced significantly in the last decade. In particular, transparent amorphous oxide semiconductor (TAOS) was proposed as a novel class of amorphous semiconductors having large electron mobility comparable to those in the corresponding crystals. Since the application of

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T. Kamiya (✉)

Materials and Structures Laboratory, and Materials Research Center for Element Strategy, Tokyo Institute of Technology, Yokohama, Kanagawa, Japan  
e-mail: [kamiya.t.aa@m.titech.ac.jp](mailto:kamiya.t.aa@m.titech.ac.jp)

H. Hosono

Materials and Structures Laboratory, Materials Research Center for Element Strategy and Frontier Research Center, Tokyo Institute of Technology, Yokohama, Kanagawa, Japan  
e-mail: [hosono@msl.titech.ac.jp](mailto:hosono@msl.titech.ac.jp)

TAOS to an active layer in thin-film transistors (TFTs) was reported in late 2004, extensive research on application of TAOS TFT, in particular In–Ga–Zn–O (IGZO)-based TAOS, to the backplanes of state-of-the-art flat-panel displays has been performed, and many displays driven by oxide backplanes have been commercialized. This chapter first gives a review on the history and present status of oxide semiconductors, then explains the unique nature of TAOS and advantages of TAOS over other semiconductors, and finally describes the fabrication process and condition suitable for TAOS TFTs.

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**Keywords**

Oxide TFT • Oxide semiconductor • Transparent amorphous oxide semiconductor (TAOS) • In–Ga–Zn–O (IGZO) • Electronic structure • Doping • Defect • Annealing

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## Brief History of Oxide Semiconductor TFTs

In this chapter, we try to minimize the number of the references due to the page limitation. Please see references Kamiya and Hosono (2010, 2012) and Kamiya et al. (2009a, 2010a) for details and respective references where not provided. References Hosono (2006), Ginley and Paine (2010), Facchetti and Marks (2010), Wager and Keszler (2007), Wager et al. (2014), Fortunato et al. (2012), Park et al. (2012), Kwon et al. (2011), and Jeong (2011) would also help further understanding of the oxide TFT technology.

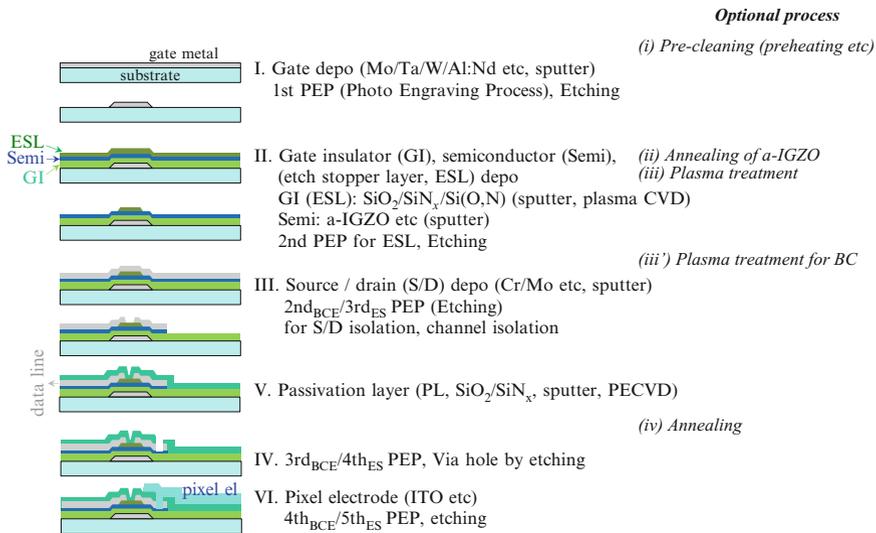
Transparent amorphous oxide semiconductor (TAOS) is an alternative of crystalline oxide semiconductor and now expected to be most promising for channel materials of thin-film transistors (TFTs) in state-of-the-art flat-panel displays (FPDs). Research of oxide TFTs started in the mid-1960s from crystalline ZnO, In<sub>2</sub>O<sub>3</sub>, and SnO<sub>2</sub> field-effect transistors (FETs) and TFTs (Kamiya and Hosono 2012) but had almost disappeared in open-accessible literatures after that until the 1990s. The next oxide TFT reappeared in 1996 with an epitaxial SnO<sub>2</sub> channel combined with a ferroelectric gate memory. Oxide TFT research became active in the 2000s due to the expectation that polycrystalline ZnO (poly-ZnO) can produce TFTs at low temperatures on large-size glass substrates comparable to the already-commercialized hydrogenated amorphous silicon (a-Si:H) TFT technology (see also the “► [Hydrogenated Amorphous Silicon Thin-Film Transistors \(a-Si:H TFTs\)](#)” chapter) but with much larger field-effect (FE) mobilities ( $\mu_{FE}$ ) > 10 cm<sup>2</sup>(Vs)<sup>-1</sup>. However, the initial poly-ZnO TFTs suffered from low  $\mu_{FE}$  up to 3 cm<sup>2</sup>(Vs)<sup>-1</sup> and normally on characteristics caused by high-density residual electron carriers (Hoffman et al. 2003). It was also expected that polycrystalline TFTs would suffer from nonuniformity issues arising from the grain boundaries (GBs) similar to poly-Si TFTs (Fossum and Ortiz-Conde 1983; Higashi et al. 2002; Kamiya et al. 2003), and instability from adsorption/desorption of oxygen-/water-related molecules to GBs is also expected for polycrystalline oxide semiconductors, whose characteristics are actually utilized, e. g., in SnO<sub>2</sub> gas sensors, but cause instability issues.

The first TAOS TFT appeared in late 2004 with an amorphous In–Ga–Zn–O (a-IGZO) channel deposited by pulsed laser deposition (PLD) (Nomura et al. 2004), which followed single-crystalline  $\text{InGaO}_3(\text{ZnO})_5$  TFT (Nomura et al. 2003). Due to the amorphous structure without GBs, it overcomes the above deficiencies of polycrystalline oxide TFTs. Actually, later researches have revealed that a-IGZO and TAOS TFTs have good uniformity similar to a-Si:H TFTs (Hayashi et al. 2008; Lee et al. 2008), and now oxide TFTs are mass produced on G8.5 glass substrates. Although the TAOS TFTs employed in the commercial products and prototype displays require post-deposition thermal annealing at 300–450 °C, the first paper (Nomura et al. 2004) demonstrated the ability of room-temperature (RT) production of flexible, transparent, and high-mobility ( $\sim 10 \text{ cm}^2(\text{Vs})^{-1}$ ) TFTs on polyethylene terephthalate (PET) sheets. Then, many prototype displays have been demonstrated, which include active-matrix (AM) flexible black & white (BW) e-papers (Ito et al. 2005, 2009), full-color e-papers (Ito et al. 2006), organic light-emitting diode (OLED) displays (Lee et al. 2006), flexible OLEDs (Sung et al. 2007; Park et al. 2007), transparent OLEDs (Jeong et al. 2007), and jumbo-size/fast/high-resolution (70", 4 K, 240 Hz, 3D) liquid-crystal displays (LCDs) (SID 2011).

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## Commercialization of Oxide Semiconductor TFTs

Although the first TAOS TFT was fabricated by PLD at RT without thermal annealing, most of current AOS TFTs are fabricated by RF/AC/DC sputtering combined with post-deposition thermal annealing (Ito et al. 2005, 2006, 2009; Lee et al. 2006; Sung et al. 2007; Park et al. 2007; Jeong et al. 2007). It has been demonstrated that the production line of TAOS TFT can be similar to the current a-Si:H TFT ones except for the sputtering process of the TAOS channels; therefore, the number of photolithography masks for LCD backplanes can be as low as 4 or 5 similar to the a-Si:H ones (Fig. 1, details will be described in section “Fabrication Process of TAOS TFTs”), where one mask step can be reduced by using a gray (half-tone) mask. For the sputtering systems, ULVAC (Matsuda et al. 2013) and AKT (Kloppel et al. 2013) provide G8 or larger-size sputtering systems as shown in Fig. 2. ULVAC employs in-plane cathode and anode AC (20–50 kHz) plasma with a moving cathode system to improve uniformity and a shadow skirt to limit the impinging direction of the deposition precursors almost normal to the substrate. AKT employs AC (20–70 kHz) plasma with rotary targets and moving magnets in the targets to control the impinging direction of the precursors and to improve uniformity (Hayashi et al. 2014). On the other hand, preexisting sputtering systems, which would have been used, e.g., for ITO deposition, would also be used with modifications. It is also important to note that selection of the sputtering target would be important. A large-size sputtering target is, usually, made from several pieces of ceramic bodies jointed by bonding, but it would transfer the target joint pattern to the sputtered film and cause uniformity issue. To eliminate this issue, ULVAC supplies a monolithic IGZO target for G8.5 mother glass.



**Fig. 1** Typical fabrication process of a-IGZO TFT. Subscripts “BCE” and “ES” indicate typical PEP steps for BCE and ES structures, respectively



**Fig. 2** Large-size (G8/8.5) sputtering systems provided by (a) ULVAC (Matsuda et al. 2013) and (b) AKT (Kloepfel et al. 2013) for IGZO sputtering

**Table 1** Resolutions and sizes of recent FPDs. “Oxide TFT” in iMac 5 K Retina LCD is speculated also to be IGZO but not disclosed

Company	Product	Type	TFT	Diag. size (inch)	Resolution		ppi (cal)
					Width	Height	
Samsung	Galaxy S5 LTE-A	OLED Pentile	LTPS	5	2,560	1,440	587
Motorola	Nexus 6	OLED Pentile	LTPS	5.96	2,560	1,440	493
Samsung	Galaxy Tab S 8.4	OLED Pentile	LTPS	8.4	2,560	1,600	305
Samsung	Galaxy Tab S 10.5	OLED	LTPS	10.5	2,560	1,600	288
Apple	New iPad (2012)	LCD	LTPS/IGZO	9.7	2,048	1,536	264
Apple	iPad mini (retina)	LCD	LTPS/IGZO	7.9	2,048	1,536	324
Sharp	AQUOS Phone SH-02E	LCD	IGZO	4.9	1,280	720	300
Sharp	AQUOS Phone SH-06E	LCD	IGZO	4.8	1,920	1,080	460
Sharp	AQUOS Pad SH-08E	LCD	IGZO	7	1,920	1,200	323
Fujitsu	UH90/L	LCD	IGZO	14	3,200	1,800	262
Toshiba	Dynabook T95/89 L	LCD	IGZO	15.6	3,840	2,160	282
Sharp	Mebius Pad	LCD	IGZO	10.1	2,560	1,600	299
Apple	iMac 5 K Retina	LCD	Oxide	27	5,120	2,880	218
Sharp	PN-K321	LCD	IGZO	32	3,840	2,160	138
LG	55EA9800	OLED	IGZO	55	1,920	1,080	40
LG	77EC980V	OLED	IGZO	77	3,840	2,160	57

The first commercialization of oxide TFT was done by Sharp in March 2012 for TFT backplane in retina LCD in Apple’s new iPad. Then, Sharp has released Sharp-brand smartphones, tablets, and PC monitors and now also provides OEM displays to other PC/smartphone suppliers. As seen in Table 1, IGZO (or oxide) TFTs are already used in many commercial FPDs, which cover the size from 5 to 77”, the resolution up to 5 K, and are used both in LCDs and OLEDs. Although the highest pixel density in products is given by LTPS OLED in Samsung Galaxy S5 LTE-A (as of the end of 2014), this high resolution is achieved by the pentile matrix pattern for small-size smartphones and tablets (8.4” or smaller, as of 2014), and the real resolution corresponding to the stripe RGB matrix is lower. The largest size and resolution in stripe RGB matrix FPDs are commercialized using oxide TFTs. As for the large-size OLED TV, Samsung commercialized 55” FHD (1,920 × 1,080) curved OLED TV using poly-Si TFT and RGB side-by-side OLED in June 2013;

**Table 2** Comparison among representative TFTs. This table is modified from that taken from J. K. Jeong (Jeong 2007)

	a-Si:H TFT	Poly-Si TFT	TAOS TFT
<b>Generation</b>	> <b>10G</b>	6.5G(LTPS)/8G (HTPS)?	8.5G
<b>Channel</b>	a-Si:H	ELA LTPS/SPC HTPS	a-InGaZnO <sub>4</sub>
<b>TFT mask steps (LCD/OLED)</b>	<b>4–6/6–7</b>	5–9	<b>4–6</b>
<b>Mobility (cm<sup>2</sup>/Vs)</b>	<1	30–100 (or larger)	<b>1–30 (100?)</b>
<b>TFT uniformity</b>	<b>Good</b>	Poor/better	<b>Good</b>
<b>Pixel TFT</b>	NMOS	PMOS, CMOS	NMOS
<b>Pixel circuit (OLED)</b>	Complex (e.g., 4 T + 2C)	Complex (e.g., 5T + 2C)	Simple ( <b>2 T + 1C</b> ) in prototypes <b>Several T in products</b>
<b>Cost/yield</b>	Low/high	High/low	Low/high
<b>TFT reliability</b>	Poor	<b>Good</b>	<b>Good</b>
<b>V<sub>th</sub> shift</b>	>30 V	< <b>0.5 V</b>	< <b>1 V</b>
<b>Stability</b>	Poor	<b>Good</b>	<b>Better than a-Si</b> <b>Large negative ΔV<sub>th</sub> by light illumination</b>
<b>Circuit integration</b>	No	<b>Yes</b>	<b>Yes</b>
<b>Process T</b>	150–350 °C	250–550 °C	<b>RT – 450 (600) °C</b>
<b>Display mode</b>	LCD, e-paper	LCD, OLED	<b>LCD, OLED, e-paper</b>
<b>Substrate</b>	<b>Glass, metal, plastic</b>	<b>Glass, metal, plastic</b>	<b>Glass, metal, plastic</b>

however, in the absence of further updates and product releases, the Samsung position in the OLED TV business remains proprietary (Oled-display.net 2014; OLED-Info 2014). Besides, LG firstly commercialized flat 55" FHD OLED TV using a-IGZO TFT and white OLED backlight improved by a yellowish-green emissive layer with white/RGB color filters in January 2013, then curved 55" OLED TV in June 2013, and curved 65/77" 4 K OLED TV in 2014. LG's products in 2013 were expensive at the prices of US\$11,000–15,000 and suffered from the yield issue in particular for the a-IGZO TFT backplane; the nonuniformity and the instability of the a-IGZO TFTs are compensated by an external circuit and a several-TFT compensation circuit in each pixel (Yoon et al. 2014; Han et al. 2014a). This issue would be now improved significantly (the number of TFTs in pixel was reduced to 3 as presented at IDW 2014 (Han et al. 2014b)), and the selling price is down to ~US\$3,000 as of late 2014.

As for the pixel compensation circuit, it would be important to note that the simplest two-transistor–one-capacitor (2T1C) circuits were employed in a-IGZO OLED prototype displays (Table 2; Jeong 2007) (Park et al. 2007; Kwon et al. 2007; Ohara et al. 2009; Saito et al. 2013; Zhang et al. 2014), but complex

compensation circuits such as 6T1C–3T2C have been used for more practical, higher-resolution prototypes (Tanabe et al. 2012; Suzuki et al. 2013; Chen et al. 2013; Shi et al. 2014) and commercial products (Yoon et al. 2014; Han et al. 2014a, b). Also for light illumination instability issues, the TFTs in LG's OLED TVs are covered with a top metal layer.

Only Sharp (G3.5–8.5) and LG (G4.5–8.5) started mass production as of 2014. LG was launching a new G8.5 production line for the OLED TVs at Paju in 2014. Other companies such as Samsung, AUO, CEC Panda, and BOE are expected to follow soon.

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## New Technologies Realized by Oxide TFTs

As explained in the previous section, many FPDs using oxide TFTs are already in the market. Including the commercial products and prototype displays, the highest resolution and pixel density would be achieved as 13.3" 8K4K (7,680 × 4,320, 664 ppi) AM-OLED (Yamazaki 2014) and 4.1" 2,560 × 1,600 736 ppi LCD (presented at IDW'14 (Ueda et al. 2014)) by Semiconductor Energy Laboratory (SEL) and Sharp. These products benefit from the intrinsic features of TAOS TFTs such as process compatibility to the existing a-Si:H TFT lines, good uniformity owing to the amorphous structure free from GBs, high  $\mu_{FE}$  ( $10 \text{ cm}^2(\text{Vs})^{-1}$  or higher), and low process temperature owing to the strong ionicity of TAOS as will be explained later.

## Flexible Displays

Facilitating the transparency of TAOS and as demonstrated by the first paper (Nomura et al. 2004), TAOS TFTs can be fabricated on plastic substrates such as PET, polyethersulfone (PES), polyethylene naphthalate (PEN), polyetheretherketone (PEEK), and polyimide (PI). As reviewed in Kamiya and Hosono (2012) and Kamiya et al. (2010a), flexible BW e-papers (Ito et al. 2005, 2009) and flexible full-color AM-OLEDs (Sung et al. 2007; Park et al. 2007) have been demonstrated. Very flexible 6.5" WQVGA AM-OLED was reported by Samsung Mobile Display (SMD), which is bendable at a curvature radius of 2 cm (Park et al. 2007). Using much thinner plastic foil substrates, much flexible TFT sheets have also been demonstrated (Rockel  et al. 2011). The highest-resolution flexible AM-OLED (13.5" 4 K) would be demonstrated by SEL, which was fabricated using transfer technology (Uesaka et al. 2014).

LG released a curved smartphone in 2013, which uses LTPS TFT backplane OLED fabricated on plastic by transfer technology (Hong et al. 2014a). Also, Samsung's curved smartphones use LTPS TFT OLEDs (see also the "► Flexible Displays: Attributes, Technologies Compatible with Flexible Substrates, and Applications" chapter). That is, oxide TFTs are not used in the small-size high-resolution OLEDs. One reason would be that the LTPS technology is already matured for

small-to-medium-size OLED displays. However, as pointed out for LG's 55" OLED TV (Yoon et al. 2014; Han et al. 2014a, b), oxide TFT backplane still needs several TFTs compensation pixel circuits, which would be serious for the aperture ratio issue in small-size OLEDs.

## Transparent Display

Another interesting feature of TAOS TFTs is that they can be highly transparent to human eyes if transparent electrodes such as ITO and transparent substrates are employed. As in Kamiya and Hosono (2012), TDK Microdevices started mass production of semitransparent OLED display for mobile phones and Samsung Electronics that of 22" transparent LCD. These transparent displays do not employ TAOS TFTs and their aperture ratios are low, e.g., ~35 %. It is expected that employing transparent TAOS TFTs will improve the aperture ratio. To date, Samsung SDI reported 4.1" transparent dual-emission QCIF AM-OLED using a-IGZO TFTs, but transparency was ~20 % (Jeong et al. 2007). LG Electronics (LGE) and Electronics and Telecommunications Research Institute (ETRI) have developed 2.5" QCIF+ transparent OLED displays using ZnO TFT backplanes with the panel transmittance of 60 % (Park et al. 2006, 2009) and displayed 1.5" QQVGA transparent AM-OLED driven by TAOS TFTs with transparency of 45 % at IMID 2009. AUO displayed a 2.4" transparent OLED driven by a-IGZO TFTs with an integrated touch panel (Hsieh et al. 2010).

Facilitating the high transmittance of TAOS TFTs, Toppa proposed a novel idea of front-drive structure (Ito et al. 2006, 2007). In conventional color AM e-papers and displays, a color filter array is formed on a frontplane and a TFT array on a backplane; therefore, fine alignment between these planes through LC or E-Ink microcapsules is necessary to avoid color misfit. However, as the thickness of the E-Ink microcapsules (40–50  $\mu\text{m}$ ) is much larger than that of LC (4–6  $\mu\text{m}$ ), the alignment is much difficult for e-papers. This problem will be more critical for flexible displays because bending the display inevitably causes horizontal misalignment between the front- and backplanes. This issue would be solved by integrating the TFT array on the color filter frontplane, where the high transparency of TAOS TFTs is beneficial.

## System Integration

AOS TFTs are also expected for integrating driving and other peripheral circuits in display panels (system-on-display) because of their large  $\mu_{\text{FE}}$ . a-IGZO TFTs usually have  $\mu_{\text{FE}} \sim 10 \text{ cm}^2(\text{Vs})^{-1}$ , which is enough for 410 kHz oscillation of a 5-stage ring oscillator (Ofuji et al. 2007). This mobility is enough for gate/source driver circuits. The first oxide-based integrated FPD was presented by Samsung Electronics (SEC) as a gate driver-integrated 15" AM-LCD, and SEL integrated gate and source drivers in 4" QVGA AM-LCD and AM-OLED (see references in Kamiya et al. (2010a)).

Sharp actually integrates the driving peripheral circuits in their FHD ( $1,920 \times 1,080$ – $1,200$ ) smartphones in the market. A faster TAOS ring oscillator was reported by Samsung Advanced Institute of Technology (SAIT) with the delay time of 0.94 ns per stage (Kim et al. 2008).

Ultraminiaturization of oxide TFTs has also been examined for faster operation and integrated high-density memory devices. SAIT reported that a-IGZO TFTs are downscalable to the channel length of 50 nm and their TFT did not exhibit the short-channel effect (Song et al. 2008). SEL explains that an accumulation mode TFT is more immune to short-channel effect (Kobayashi et al. 2014). High-frequency operation up to 180 MHz is reported for 1- $\mu$ m-long a-In–Zn–O (a-IZO) TFTs (Wang et al. 2008).

Hitachi, Ltd. reported very low-voltage (1.5 V) operation of AOS TFTs (Kawamura et al. 2008) and develops 13.56 MHz RFID tag operating with 1 nA of driving current (Ozaki et al. 2011). Facilitating the wide operation voltage from 1.5 to  $\sim 100$  V of TAOS TFTs, Renesas Electronics proposes integration of oxide (n-type IGZO and p-type SnO (see Ogo et al. (2008a, 2009) for SnO TFTs)) TFTs in Si MOS ULSI, where the oxide TFTs bridge the low operation voltage ULSI circuit to an external high voltage load (Kaneko et al. 2011). Further, TAOSs are expected also for memories as in Kamiya and Hosono (2012). SAIT reported nonvolatile memories using an a-IGZO floating gate. Resistive switching memory (ReRAM) using a NiO memory node layer and a IGZO memory node layer controlled by a-IGZO TFTs are also reported. Ferroelectric memory (FeRAM) using an organic ferroelectric memory node is also demonstrated. Novel material amorphous GaO<sub>x</sub> is also proposed for ReRAM (Aoki et al. 2014).

TAOS TFTs also have another advantage over Si FETs/TFTs. FETs/TFTs are used to keep the voltage states in switching TFTs in FPDs and memories; therefore, their retention time is limited by off-state current ( $I_{\text{off}}$ ) of the FETs/TFTs, which are typically  $< 1$  nA for Si MOSFET,  $\sim 1$  pA for poly-Si TFTs, and  $\sim 0.1$  pA for a-Si:H TFTs. Display pixel and driving circuits are designed so that we cannot recognize image blinking at the 60 Hz refresh rate. On the other hand, IGZO TFTs have much smaller  $I_{\text{off}}$ , which can be as low as  $3 \times 10^{-26}$  A per  $\mu\text{m}$  in gate width at 27 °C (Tanabe) and  $2.8 \times 10^{-20}$  A per  $\mu\text{m}$  at 60 °C (Yamauchi et al. 2013). Sharp's smartphones and tablets in the market utilize this very low  $I_{\text{off}}$  and vary the refresh rate down to 1 Hz while a still image is displayed ("LCD idling stop technology"). The low  $I_{\text{off}}$  is effective in particular for reflective displays because only TFT backplanes consume electric power. Qualcomm already released reflective displays based on MEMS ("Mirasol") in smart watches. Mirasol products as of 2014 are driven by a-Si:H TFTs, but the next-generation Mirasol driven by IGZO TFTs was demonstrated (Hong et al. 2014b). Qualcomm Pixtronix has also developed a different type of MEMS display, which uses field sequential color control with RGB LEDs and digital microshutters (Hagood et al. 2008). As the microshutter requires operation voltages as high as 20 V and higher speed than 0.1 ms, IGZO TFTs are used as the backplane (exhibited at SID Display Week 2014). Low  $I_{\text{off}}$  of IGZO TFTs also enables to realize nonvolatile DRAM/NOSRAM and normally off CPU (Nishijima et al. 2012).

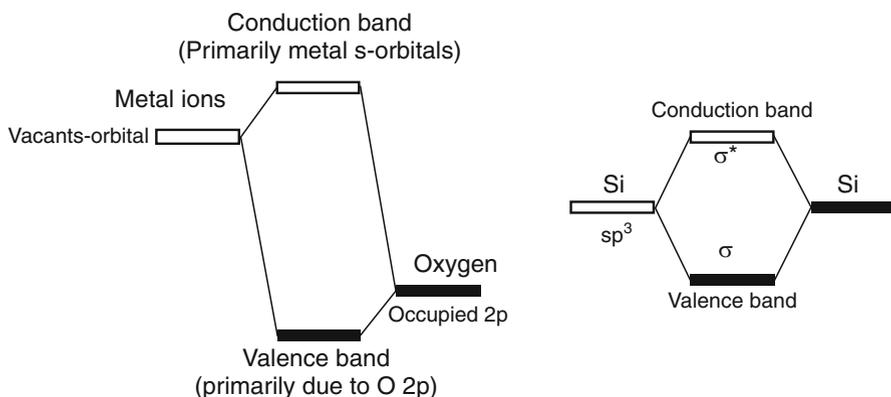
Of course, larger  $\mu_{FE}$  are favorable and required for higher resolution, faster FPDs, and other microelectronic applications. New materials will be reviewed later on.

## TAOS and Related Materials

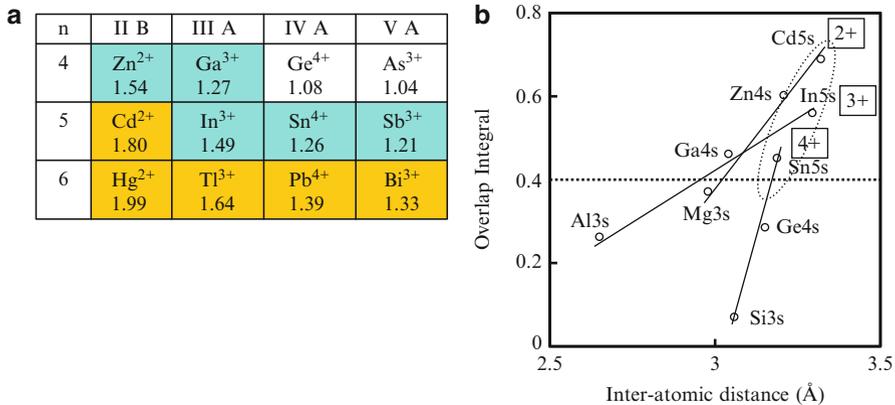
### Electronic Structures of Oxide Semiconductors

Oxide semiconductors made of typical metals are, in general, N-type except several materials. This is a natural consequence of chemical bonding nature in oxides. Figure 3 shows schematic energy diagrams of ionic oxides and silicon. In ionic oxides, the nature of conduction band minimum (CBM), which works as an electron pathway, totally differs from that of the valence band maximum (VBM), which works as a hole pathway. The CBM in ionic oxides is primarily composed of unoccupied s orbitals of cations, and the contribution of oxygen 2p orbitals is limited. The spatial spread of this unoccupied s orbital is so large that direct overlap between the s orbitals of the neighboring cations is possible in post-transition metal (PTM) oxides; therefore, an effective mass of electron is small in these oxides. In fact, some ionic oxides satisfy such situation with large electron mobilities  $\sim 200 \text{ cm}^2(\text{Vs})^{-1}$  and are called transparent conductive oxides (TCOs) represented by  $\text{In}_2\text{O}_3$ ,  $\text{SnO}_2$ , and  $\text{ZnO}$  (see Fig. 4a, b; Orita et al. 2001).

What happens if these TCO materials become amorphous? In an amorphous state, structural disorder concentrates on an energetically weak structural unit. In most amorphous materials, structural disorder appears prominently as the bond angle distribution. When the bond angle has a large distribution, how is the effective mass (in other words, the transfer rate between neighboring cation s orbitals or transfer integrals) modified for carrier electrons? We considered two cases:



**Fig. 3** Schematic energy diagram. (Left) Ionic non-transition metal oxides and (right) covalent compounds like Si

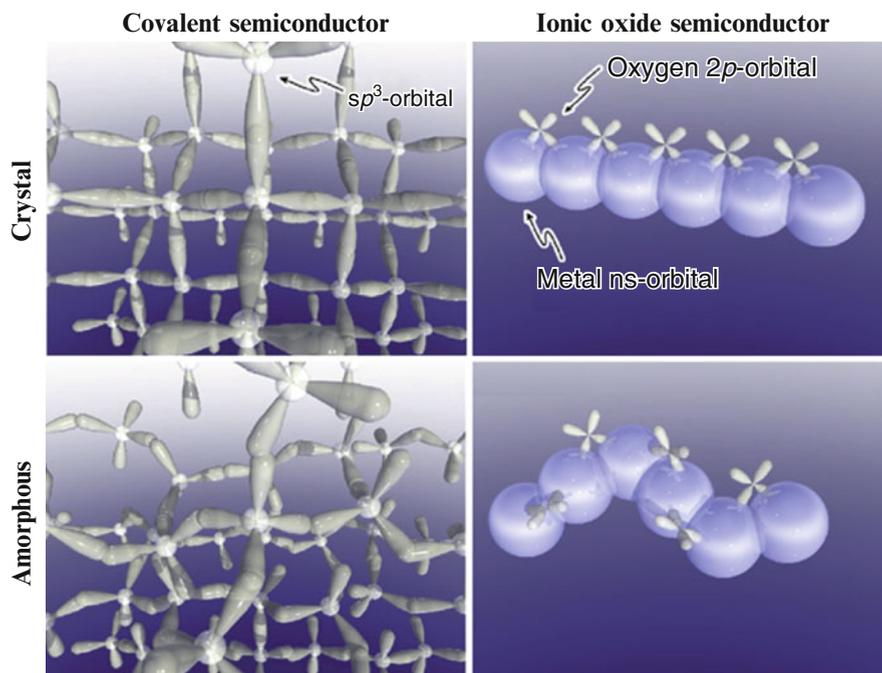


**Fig. 4** (a) Radii and (b) overlap integrals calculated by Slater-type orbitals

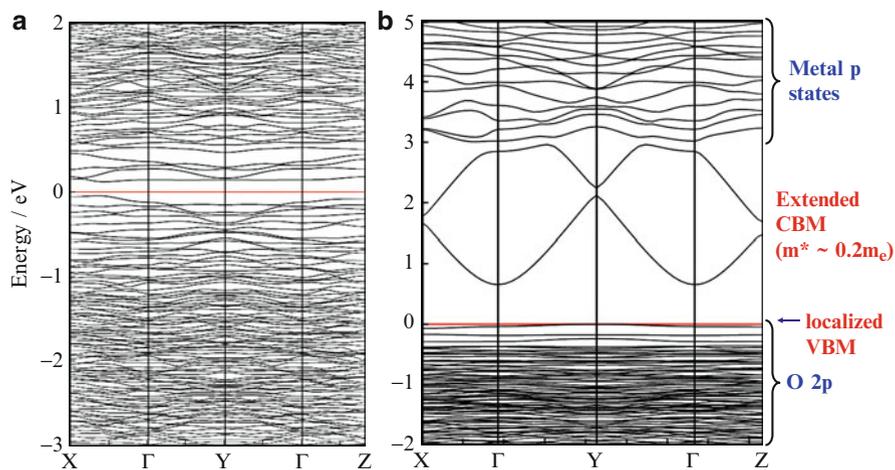
(i) covalent semiconductors and (ii) ionic semiconductors. In the former case, the magnitude of the overlap between the unoccupied orbitals of the neighboring atoms is very sensitive to the variation in bond angle. As a consequence, rather deep localized states would be created at somewhat high concentrations; thereby, the drift mobility would be largely degraded.

On the other hand, the magnitude of the overlap in the latter case is critically different depending on the choice of metal cations (Fig. 4a, b; Orita et al. 2001); when the spatial spread of the s orbital is larger than the inter-cation distance, the magnitude should be insensitive to the bond angle distribution because the s orbitals are isotropic in shape. As a consequence, we may anticipate that these ionic amorphous materials have large electron mobility comparable to that in the corresponding crystalline phase. In the case that the spatial spread of the metal s orbital is small, such favorable situation cannot be expected. The spatial spread of the s orbital of a metal cation is primarily determined by the principal quantum number ( $n$ ) and is modified by the charge state of the cation as discussed for the crystalline TCOs in Fig. 4. Thus candidates for high-mobility TAOSs are found in oxides of PTM cations with an electronic configuration  $(n-1)d^{10}ns^0$ , where  $n \geq 5$  (for crystalline oxide semiconductors, this requirement is relaxed to  $n \geq 4$  as exemplified by ZnO with the  $(3d)^{10}(4s)^0$  configuration).

Figure 5 draws the difference in orbitals between Si and a PTM oxide and between crystalline and amorphous states. The drastic reduction of the electron mobility in the amorphous state from c-Si may be understood intuitively from the figure, whereas medium mobility in c-PTM oxides is reserved even in the amorphous state. In a sense, the situation of CBM in PTM oxides is similar to that in amorphous metal alloys in the aspect that metal orbitals dominantly constitute the electron pathways. This is quantitatively explained by first-principles density functional theory (DFT) calculations in Fig. 6, where all the bands are very flat and carriers are localized in a-Si, while the CBM band is very dispersive and has a small



**Fig. 5** Schematic orbital drawings of electron pathways (conduction band bottom) in covalent semiconductors and ionic oxide semiconductors



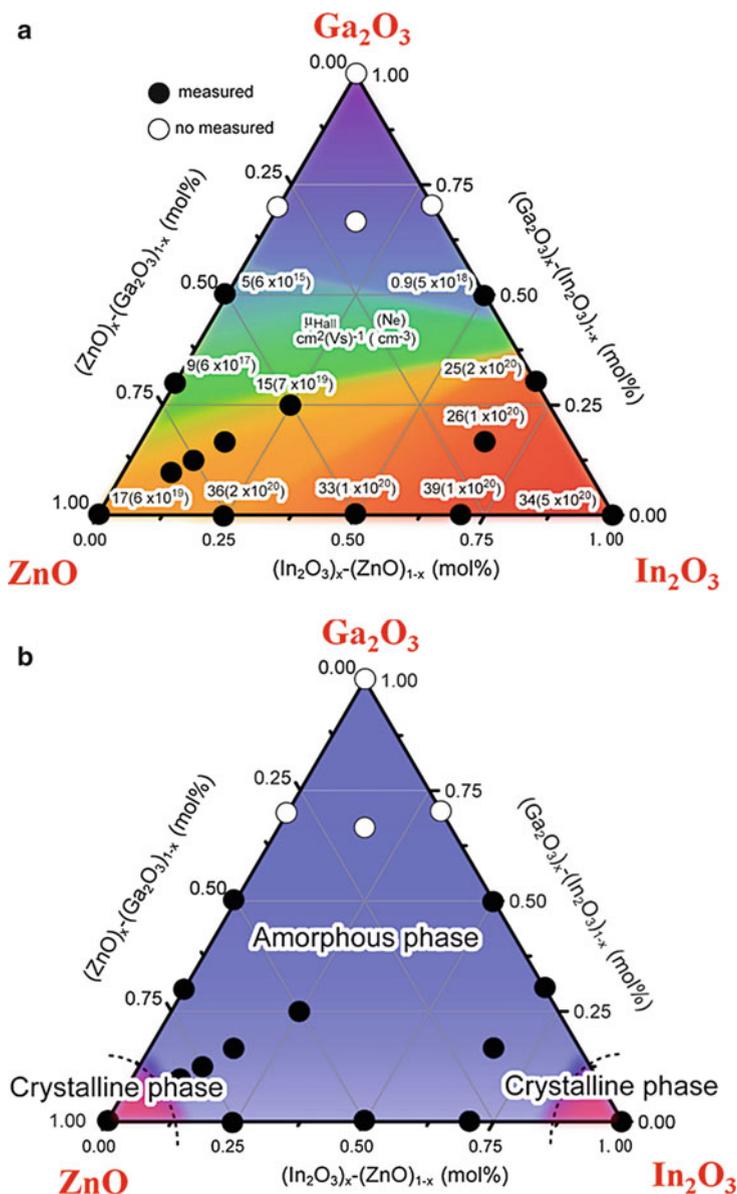
**Fig. 6** Pseudo-band structures of (a) a-Si and (b) a-InGaZnO<sub>4</sub> calculated by DFT

electron effective mass similar to that in crystalline  $\text{InGaZnO}_4$  (c-IGZO) (Kamiya et al. 2009b).

## TAOS Materials

Due to the above electronic structures and the requirement for high-mobility oxides, major TAOS materials have been found in oxides of In–Ga–Zn–Sn multicomponent metal systems. Further, it has been understood that TAOS materials would be composed of several metal cations that have different roles. That is, in a-IGZO, the In ions contribute to a large electron mobility and thus called “mobility enhancer.” Ga forms stronger chemical bond with oxygen (Kamiya et al. 2010b) and would suppress the formation of oxygen deficiency and the generation of conduction electrons and thus called “stabilizer” or “suppressor.” The role of Zn is not clear but expected to stabilize amorphous structure, as known in glass science as network modifier. Therefore, there is a clear trend (Fig. 7) that increasing the In content increases the electron mobility but also increases residual electron density and tends to cause negative threshold voltage ( $V_{\text{th}}$ ) in TFTs. Addition of a suppressor like Ga reduces the electron density ( $N_e$ ) if the same deposition condition is employed but decreases the electron mobility. The decrease in mobility is caused by two factors: (i) reduction of the In content and (ii) reduction of electron mobility due to the small  $N_e$  as will be explained later. Figure 7b shows that pure  $\text{In}_2\text{O}_3$  and ZnO do not take amorphous structures even if deposited at RT without substrate heating; therefore, mixing of two or more kinds of metal cations are necessary to stabilize the amorphous structure.

Therefore, the exploration of TAOS materials has been carried out by examining different combinations of mobility enhancers and suppressors. The first material is a-IGZO with the nominal atomic ratio of In:Ga:Zn = 1:1:1 (called “111” composition) (Nomura et al. 2004), and also the other composition of In:Ga:Zn = 2:2:1 (“221” composition) (Jeong et al. 2007) has been examined intensively. The Oregon State University (OSU) and Hewlett-Packard (HP) group proposed Zn–Sn–O (ZTO) and Zn–In–O (ZIO) TFTs just after the first report of a-IGZO TFT (see references in Kamiya et al. (2010a)), which exhibited high  $\mu_{\text{FE}} > 50 \text{ cm}^2(\text{Vs})$  by annealing at 600 °C. As explained above, an In-rich composition can enhance electron mobility; e.g., 10 wt% ZnO-doped  $\text{In}_2\text{O}_3$  (IZO), developed by Idemitsu (Kaijou et al. 1993), is a stable amorphous TCO with high mobilities (Hall mobilities,  $\mu_{\text{Hall}} > 50 \text{ cm}^2(\text{Vs})^{-1}$ ), and IZO TFTs actually exhibit high  $\mu_{\text{FE}}$  (Itagaki et al. 2008). a-In–Ga–O (a-IGO) TFT was firstly reported by the OSU and HP group in 2006, while nanocrystalline In-rich nc-IGO TFTs and AM-OLED display were reported by Sony (Terai et al. 2011). Tokyo Tech and Canon reported Sn–Ga–Zn–O (Ogo et al. 2008b) and In–X–O ( $X = \text{B, Mg, Al, Si, Ti, Zn, Ga, Ge, Mo, and Sn}$ ) (Kumomi et al. 2009; Goyal et al. 2009). ETRI, Idemitsu, Sony, AUO, etc., have also developed In-rich In–Sn–Zn–O (ITZO) as high-mobility materials (Ryu



**Fig. 7** TAOS materials. (a) Hall mobility and electron density and (b) structure of In–Ga–Zn–O films deposited at RT

et al. 2009; Fukumoto et al. 2010; Arai and Shiratani 2012; Shih et al. 2014). A similar material, Al–Zn–Sn–O (AZTO) and Al–Sn–Zn–In–O (ATZIO) have been developed by ETRI (Cho et al. 2014). By employing different suppressors, Hf–In–Zn–O was reported by SAIT and polycrystalline Zr–In–Zn–O was reported

by Samsung SDI. SAIT also reported a different class of TAOS, ZnON (Ryu et al. 2012). The ZnON TFTs exhibit very high mobilities even exceeding  $100 \text{ cm}^2(\text{Vs})^{-1}$ ; however, the appropriate O:N ratio and the optimum deposition condition window are very narrow and photosensitive to visible light due to a small band gap as evidenced by its brown color. CBRITE has announced that their materials produce very stable, high-mobility TFTs but the chemical compositions and other details have not been revealed; they disclosed that the composition is In–Al–Zn–O (IAZO) with “pinpoint chemical composition” at the presentation of SID’14 (Yu et al. 2014).

Most of the above materials have faded out from development research of FPDs, while practical displays have been developed using IGZO and ITZO TFTs. Sharp and SEL employ C-axis-aligned crystalline (CAAC) IGZO for the small-to-medium-size LCDs and their prototype displays. The specific fabrication conditions have not been disclosed, but some information is available in Yamazaki et al. (2014a, b) and their conference presentations. As also reported in Lynch et al. (2014), IGZO starts to crystallize during sputtering growth if the substrate temperature is raised to 170–190 °C or higher. Post-deposition thermal annealing/crystal growth, e.g., at 450 °C, combined with DC/RF sputtering is also examined in Yamazaki et al. (2014a, b), which forms CAAC IGZO dominantly crystallized in the channel surface region with crystallites a few nanometers in size. They claim that the advantages of CAAC IGZO are as follows: (i) smaller density of subgap states compared to a-IGZO, (ii) etching toughness and better processability for back-channel-etch (BCE)-type TFTs, (iii) better robustness against Cu diffusion, and (iv) good uniformity for short-channel BCE TFTs. ITZO TFTs and displays have been demonstrated by Idemitsu, Sony, AUO, etc. (Arai and Shiratani 2012; Shih et al. 2014). The advantages of ITZO TFTs are high  $\mu_{\text{FE}} > 30 \text{ cm}^2(\text{Vs})^{-1}$  and good robustness/selectivity against wet etching for BCE TFTs (Fukumoto et al. 2010; Shih et al. 2014). While ITZO requires high oxygen partial pressure ( $P_{\text{O}_2}$ ) during sputtering to suppress the electron density so as to fit to normally off TFTs (Tomai et al. 2012), the high  $P_{\text{O}_2}$  condition deteriorates the deposition rate seriously. It is proposed that addition of water to the sputtering atmosphere improves this issue (Kawashima et al. 2013).

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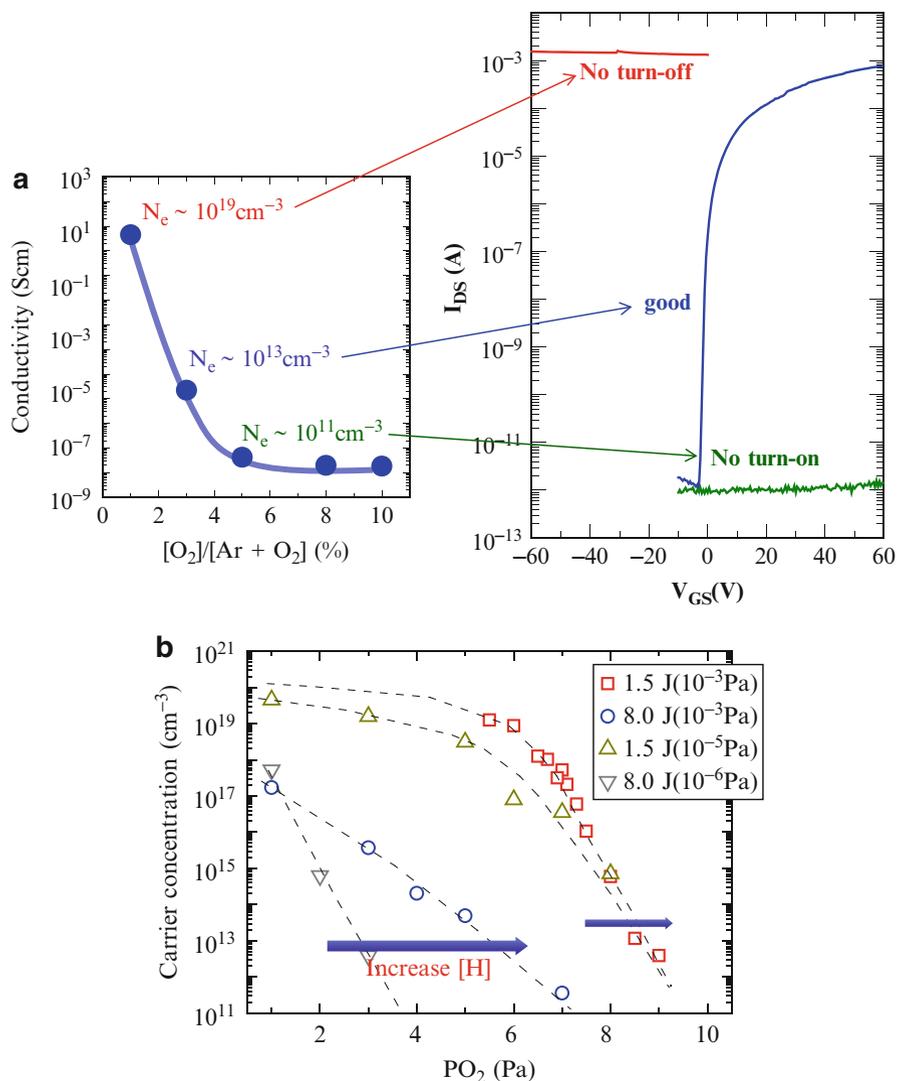
## Electron Transport and Subgap Defects in TAOS

TAOS has several common properties which are not seen in conventional amorphous semiconductors. First is their large electron mobilities  $>10 \text{ cm}^2(\text{Vs})^{-1}$ , which is higher by 1–2 orders of magnitude than that in a-Si:H. Second is that a degenerate state can be realized by doping. This is totally different from the other amorphous semiconductors. For instance, c-Si is easily changed to the degenerate state by carrier doping ( $\sim 10^{18} \text{ cm}^{-3}$ ), but no such a state has been attained in a-Si:H (Joannopoulos and Luicovsky 1984) to date. That is, carrier conduction takes place by hopping through localized tail states in conventional amorphous semiconductors. This is the reason why drift mobility in the amorphous state is so small compared with that in

the crystalline state. On the other hand, in TAOS, the Fermi level ( $E_F$ ) can exceed the mobility gap easily by carrier doping, leading to band conduction. It is considered that this striking difference originates from that in chemical bonding nature between the materials, i.e., strong ionic bonding with spherical potential is much favorable to form a shallow tail state having small density of states.

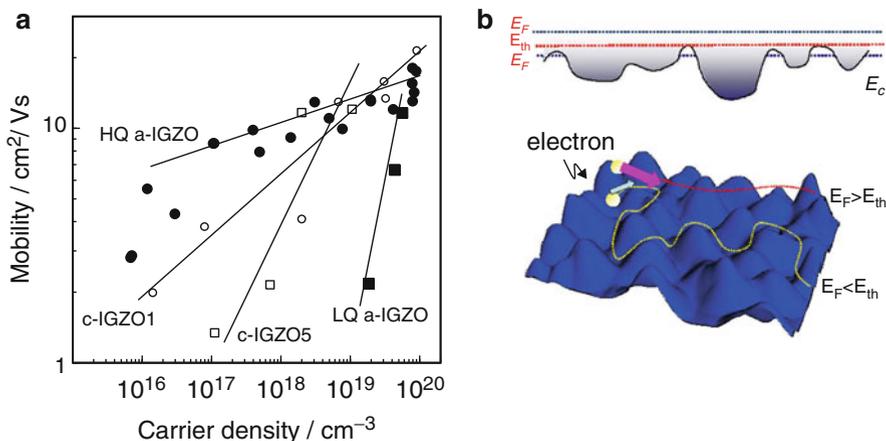
Doping mechanism of TAOS is also different from a-Si:H. In a-Si:H, aliovalent dopants such as P and B replace the Si site in the tetrahedral coordination polyhedral; therefore, aliovalent doping works properly. On the other hand, such clear coordination structure has not been established in TAOS, and DFT calculations for a-IGZO suggest that the coordination numbers around a metal ion have a large distribution (Kamiya et al. 2009b, 2010b; Nomura et al. 2007). Recent researches have revealed that the cation to oxygen ratio in TAOS is very flexible. It is known that a-IGZO deposited by PLD and conventional sputtering contains high-density impurity hydrogens at  $10^{20}$ – $10^{21}$  cm<sup>-3</sup> (Nomura et al. 2013). These hydrogens are considered to work as donors and generate mobile electrons but are compensated by excess oxygens (Fig. 8b) (Orui et al. 2014; Grochowski et al. 2014). This situation would be understood by a simple counting rule summarized in Kamiya et al. (2010a); i.e., the total charge neutrality of the constituent ions determines the electron density. Therefore, aliovalent ion doping (e.g., Ga<sup>3+</sup> doping to Zn<sup>2+</sup> site) is expected to donate one mobile electron, but it is compensated by introducing excess 1/2 O atom, which will be ionized to 1/2 O<sup>2-</sup> ion upon trapping the mobile electron if appropriate deposition condition ( $P_{O_2}$  etc) or post-deposition thermal annealing is applied. A similar situation also happens if more impurity hydrogens are incorporated from a dirty deposition chamber; the mobile electrons generated from the hydrogens can be compensated by higher  $P_{O_2}$  deposition or annealing conditions (Fig. 8b) (Orui et al. 2014). Finally, the doping in TAOS would be determined by off-stoichiometry of the cation to anion ratio and only possible by choosing  $P_{O_2}$  during deposition or annealing or post-deposition H annealing (or metal ion implantation), whose doping mode may be regarded as a kind of chemical (interstitial) doping. Therefore, usually  $N_e$  in TAOS is primary controlled by oxygen partial pressure during deposition ( $P_{O_2}$ ) as summarized in Fig. 8a.

It is important to notice that Hall mobility ( $\mu_{Hall}$ ) in TAOS largely depends on  $N_e$  due to the presence of potential barriers arising from structural disorder. As seen in Fig. 9a,  $\mu_{Hall}$  increases with increasing  $N_e$  and finally exceeds  $10$  cm<sup>2</sup>(Vs)<sup>-1</sup> if  $N_e$  exceeds  $\sim 10^{18}$  cm<sup>-3</sup> (Nomura et al. 2004; Kamiya et al. 2010c). The slope of  $d\mu_{Hall}/dN_e$  and the threshold  $N_e$  ( $N_{e,th}$ ) depend on the local structure of IGZO; i.e., PLD-deposited a-IGZO has a larger slope and  $N_{e,th}$  compared to sputtered a-IGZO even if the nominal chemical compositions are the same. Crystalline IGZO (c-IGZO1 for InGaZnO<sub>4</sub> and c-IGZO5 for InGaO<sub>3</sub>(ZnO)<sub>5</sub>) have larger slopes, which would be explained that the structural disorders are concentrated in the (Zn, Ga)O<sub>3</sub> layers except for the ordered InO<sub>2</sub> layers in crystalline IGZO. Low-quality (LQ) a-IGZO also has larger slope and  $N_{e,th}$  than the optimally deposited high-quality (HQ) a-IGZO, which would be explained also by a more disordered structure. This  $\mu_{Hall}$  vs  $N_e$  behavior is explained by the percolation conduction model, in which electron transport is controlled by distributed potential barriers above CBM (Fig. 9b; Kamiya et al. 2010c). That is, electrons take long winding paths and

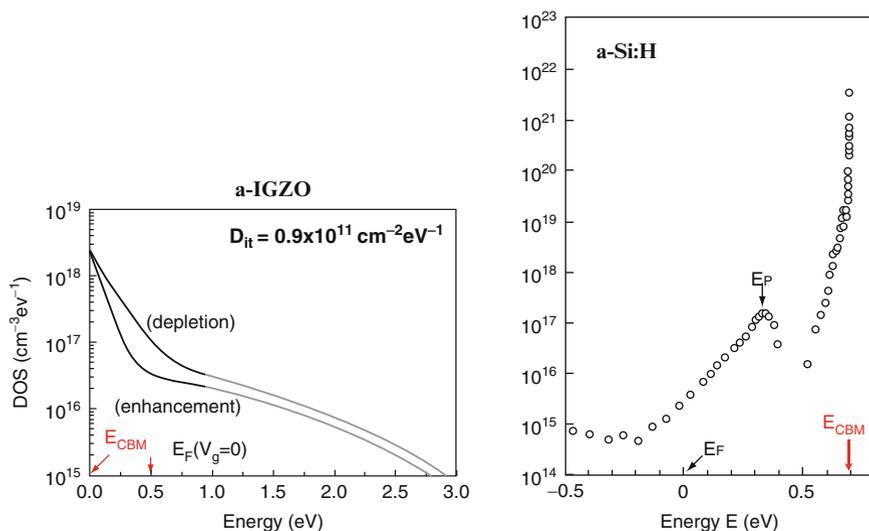


**Fig. 8** Electron doping to a-IGZO by oxygen partial pressure. **(a)** Relationship among  $P_{\text{O}_2}$ , conductivity (carrier concentration), and TFT characteristics. **(b)** Electron density in a-IGZO films deposited by PLD with different back pressures ( $10^{-3}$  and  $10^{-5}$  Pa) in the deposition chamber. Two series of laser energies (1.5 and 8.0 J) are also compared

mobility is low if they do not have enough energy (i.e., at low temperature or with low  $N_e$ /deep  $E_F$ ), while they can take more direct shorter paths at higher temperature or with higher  $N_e$  because the electron kinetic energy/ $E_F$  overcomes the potential barriers. If the TAOS is very defective or at a very low temperature with very low  $N_e$ , hopping conduction would be dominant.

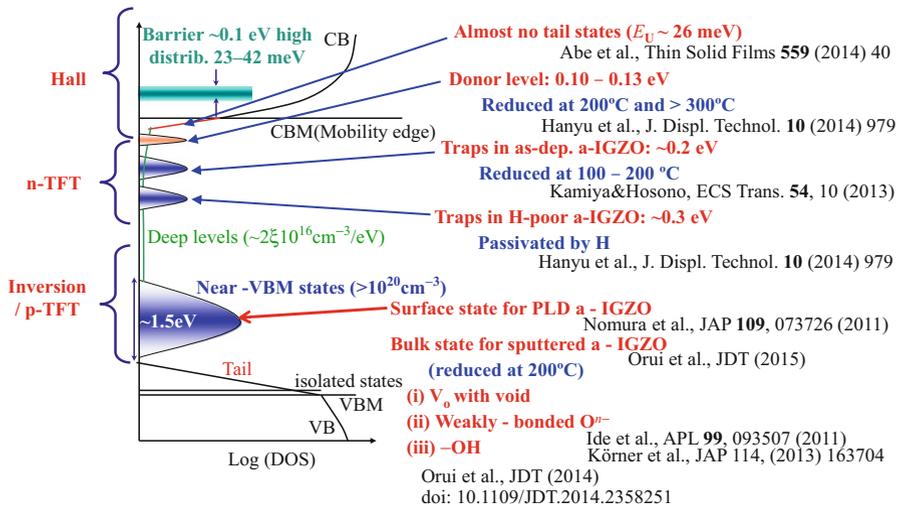


**Fig. 9** Electron transport properties of a-IGZO and c-IGZO. (a) Hall mobility vs electron density. (b) Schematic illustration of potential barriers above CBM causing percolation conduction



**Fig. 10** Tail state density in a-IGZO estimated from TFT characteristics. Estimation is valid in the energy region ~1 eV from the CBM. That of a-Si:H is shown for comparison

The dominant factor of  $\mu_{FE}$  is partly different from that of  $\mu_{Hall}$  because  $\mu_{FE}$  is expressed roughly by  $\mu_{Hall} (N_{ind} - N_{trap})/N_{ind}$ , where  $N_{ind}$  is the total electron density induced by the gate voltage and  $N_{trap}$  is the density of the induced electrons trapped by subgap defects (Kamiya et al. 2010a). Therefore, low  $N_{trap}$  is important to obtain high  $\mu_{FE}$ , and the low  $N_{trap}$  is confirmed by TFT analyses (Hsieh et al. 2008), C-V analyses (Kimura et al. 2008, 2010), etc., as shown in Fig. 10. These studies have



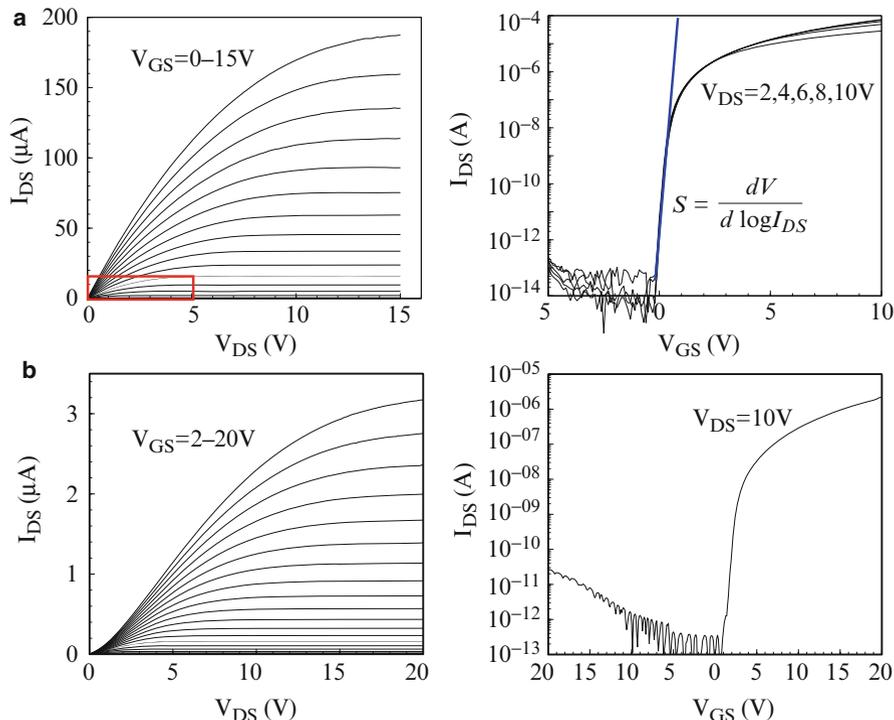
**Fig. 11** Schematic electronic structure around the band gap of a-IGZO

revealed that the subgap trap densities in TAOSs are 2–3 orders of magnitude smaller than that of a-Si:H where  $E_F$  is close to CBM. The low trap density is explained also by the electronic structure specific to the strong ionicity of TAOS similar to Fig. 3 (see Kamiya et al. 2009a); i.e., a Si dangling bond generates an electron and hole trap around the mid band gap in Si, but an oxygen deficiency and resulting non-bonding metal state do not work as an electron trap.

Figure 11 illustrates these electronic structures, which also shows reported defect states in the band gap of a-IGZO (Kamiya et al. 2010a, 2014).

## Deposition Condition to Obtain Good TAOS TFT

Figure 12 shows a typical (left) drain–source current ( $I_{DS}$ )–voltage ( $V_{DS}$ ) characteristics at various gate biases ( $V_{GS}$ ) (output characteristic) and (right)  $I_{DS}$ – $V_{GS}$  characteristics at various  $V_{DS}$  (transfer characteristic) in comparison with those of a-Si:H TFT (see also the “► Hydrogenated Amorphous Silicon Thin-Film Transistors (a-Si:H TFTs)” chapter). It is seen that the on current ( $I_{on}$ ) of a-IGZO TFT is two orders of magnitude larger than that of the a-Si:H TFT. In general, an OLED pixel requires several  $\mu\text{A}$  of driving current, indicating that only 5 V is enough for a-IGZO TFTs but 20 V is not satisfactory for a-Si:H TFTs. This is the reason why a-Si:H and organic TFT backplanes are not considered for practical OLED displays and only oxide and poly-Si TFT backplanes are used. As explained in the previous sections, a-IGZO TFTs easily attain high  $\mu_{FE} > 10 \text{cm}^2(\text{Vs})^{-1}$ , and  $I_{off}$  already reaches the usual measurement limit of  $\sim 10^{-14}$  A and actually much lower than this value. In addition, the low operation voltage of a-IGZO TFT benefits also from the small

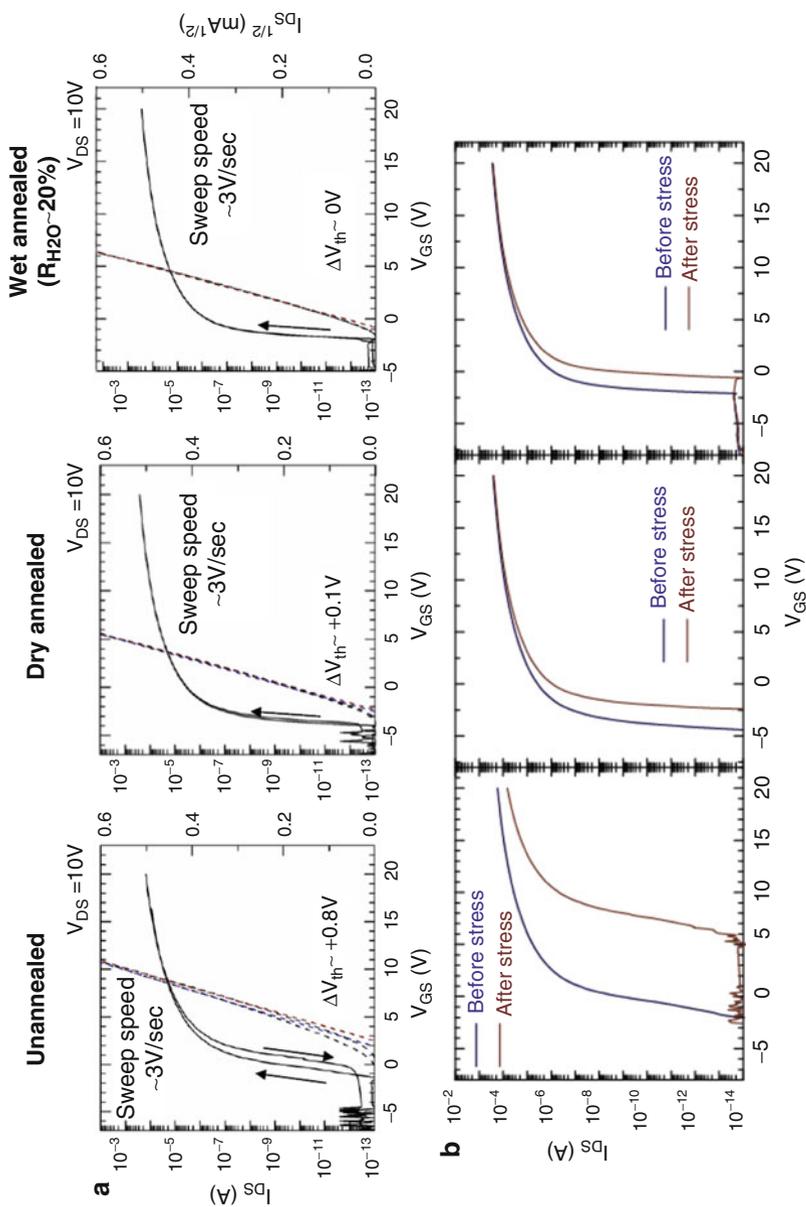


**Fig. 12** Typical TFT characteristics of (a) a-IGZO and (b) a-Si:H TFTs. (Left) Output and (right) transfer characteristics

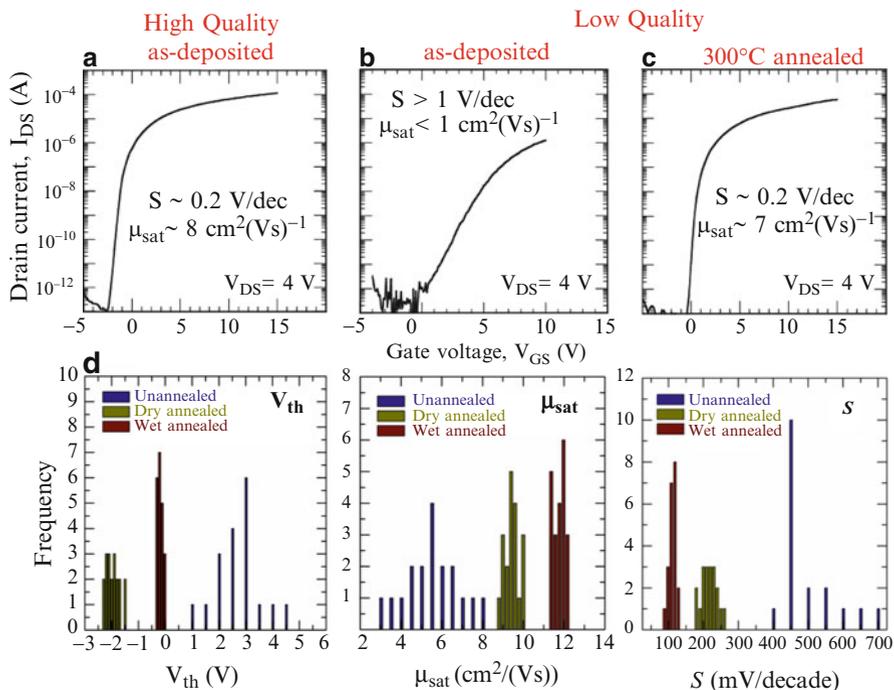
subthreshold voltage swing (S value). These features of TAOS TFTs are compared with those of a-Si:H and poly-Si TFTs in Table 2 (Jeong 2007).

To obtain such good TFTs,  $\text{PO}_2$  during film deposition is very important as seen in Fig. 8a. It has been recognized that good TFTs are obtained with a-IGZO channels having the electrical conductivities  $10^{-6}$ – $10^{-3} \text{ Scm}^{-1}$ , which corresponding to  $N_c = 10^{12}$ – $10^{15} \text{ cm}^{-3}$  upon supposition of  $\mu_{\text{Hall}} = 10 \text{ cm}^2(\text{Vs})^{-1}$ .

A key technology for producing practical TFTs is post-deposition thermal annealing. Although TAOS TFTs operate with large  $\mu_{\text{FE}} > 10 \text{ cm}^2(\text{Vs})^{-1}$  even without substrate heating or thermal annealing, as seen in Fig. 13, unannealed TFTs exhibit serious hysteresis and instability ( $V_{\text{th}}$  shift,  $\Delta V_{\text{th}}$ ). Typically, clockwise hystereses are observed (both for unannealed and annealed TFTs), suggesting effects of, e.g., shallow electron traps in the channel. For typical instability modes without light illumination, positive  $\Delta V_{\text{th}}$  are observed for positive  $V_{\text{GS}}$  bias tests (Nomura et al. 2009) but negative  $\Delta V_{\text{th}}$  for negative  $V_{\text{GS}}$  (usually the negative  $\Delta V_{\text{th}}$  is small or even zero). On the other hand,  $\Delta V_{\text{th}}$  during stress tests sometimes exhibit systematic variation from negative to positive  $\Delta V_{\text{th}}$  as reported, e.g., in Görm et al. (2007) and Cheong et al. (2009), suggesting that there are competing origins of  $\Delta V_{\text{th}}$  that depend on chemical composition, stress condition, etc. Under light illumination,



**Fig. 13** Effects of post-deposition thermal annealing on (a) hysteresis and (b)  $V_{th}$  shift of a-IGZO TFTs. Two thermal annealing, dry  $O_2$  annealing and wet  $O_2$  annealing, are compared



**Fig. 14** Effects of post-deposition thermal annealing on (a–c) the performance and (d) uniformity of a-IGZO TFTs. For (d), two thermal annealing, dry O<sub>2</sub> annealing and wet O<sub>2</sub> annealing, are compared

typically large negative  $\Delta V_{th}$  and increase in  $I_{off}$  are observed even if the illuminated photon energy is smaller than the band gap of the TAOS layer (3.0–3.2 eV for a-IGZO) (Nomura et al. 2010a) (see also section “Fabrication Process of TAOS TFTs” and Conley (2010) for a review).

Post-deposition thermal annealing at 300–400 °C in air or O<sub>2</sub> improves these issues. Thermal annealing is also effective to homogenize the TFT characteristics and improves uniformity as shown in Fig. 14 (Hosono et al. 2008; Nomura et al. 2008a). As explained above, a-IGZO TFTs deposited with the optimum condition (high-quality, HQ a-IGZO) operate with good  $\mu_{FE}$ . On the other hand, that fabricated with off-optimized condition often causes poor operation characteristics as shown in Fig. 14b, but the poor characteristic is recovered to a good one comparable to Fig. 14a by the thermal annealing (Fig. 14c). However, although the resulting TFT characteristics appear similar, the annealed LQ a-IGZO still have high-density deep defects just above the VBM (near-VBM states) (Nomura et al. 2008b); therefore, it is important to use the optimum condition so as to obtain high  $\mu_{FE}$ , small  $S$  value, and  $V_{th}$  close to 0 V with minimum subgap optical absorption (corresponding to the density of the near-VBM states).

For depositing TAOS films, other parameters should also be considered. It has been clarified that low total pressure ( $P_{tot}$ ) produces higher-density a-IGZO films and

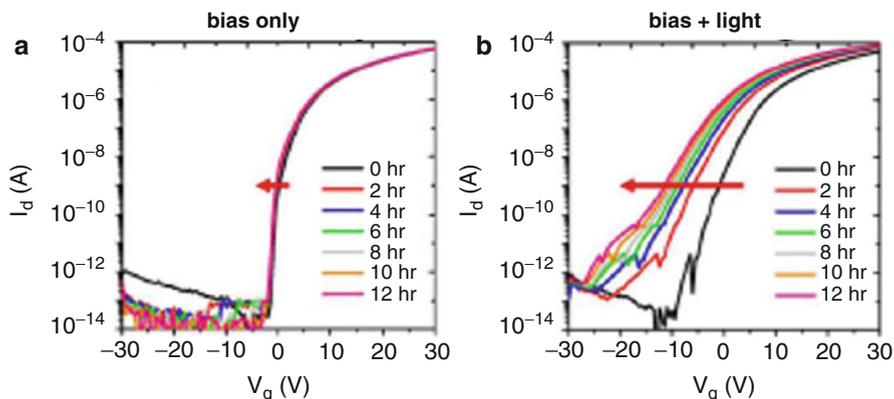
less-defective a-IGZO TFTs (Grochowski et al. 2014; Jeong et al. 2008). For a plasma process, it is known that  $P_{\text{tot}}$ -electrode distance ( $D$ ) product ( $P_{\text{tot}}D$ ) is a universal parameter as seen, e.g., in the Paschen glow curve (Paschen 1889) because it determines the frequency of molecule/electron collisions in plasma, suggesting that a shorter substrate-target distance would also be better to obtain dense, better TAOS films. There is also a trend that higher RF/AC/DC power is better (Kikuchi et al. 2010). These conditions, higher power and smaller  $P_{\text{tot}}D$ , appear to contradict with a common sense of plasma depositions because these increase kinetic energy of deposition precursors and  $\text{Ar}^+$  ions and thus increase ion bombardment damage to the film. However, on the other hand, higher kinetic energy would be better to form denser films by enhancing surface migration and structural relaxation at the growing surface, and the bombardment damage would be recovered by post-deposition thermal annealing for TAOS films. Recent works have revealed that higher  $P_{\text{tot}}$  incorporates excess oxygen and Ar into a-IGZO films and causes low density (Grochowski et al. 2014). As for  $P_{\text{O}_2}$ , too high  $P_{\text{O}_2}$  also incorporate excess/weakly bonded oxygen and create extra defects (Kamiya and Hosono 2013; Ide et al. 2011); therefore,  $P_{\text{O}_2}$  should be tuned finely.

Another important issue to be considered is cleanness of deposition chamber and annealing system. As explained in section “[Electron Transport and Subgap Defects in TAOS](#)” and for Fig. 8b, impurity hydrogen affects  $N_e$  and optimum  $P_{\text{O}_2}$  very seriously. Further, the impurity hydrogen increases the near-VBM defects as  $-\text{OH}$  bonds (Terai et al. 2011). For our conventional sputtering system, the optimum  $R_{\text{O}_2} = [\text{O}_2]/([\text{O}_2] + [\text{Ar}])$  is  $\sim 3\%$  but is significantly reduced if ultrahigh-vacuum (UHV) sputtering system is employed (Miyase et al. 2014) while increased if a dirty condition (poorer base pressure) is employed as seen in Fig. 8b. This indicates that the optimum  $R_{\text{O}_2}$  may be used as a measure of cleanness of deposition chamber and impurity hydrogen concentration. To date, it has been revealed that some hydrogens have good roles to reduce defects (Miyase et al. 2014; Hanyu et al. 2013), but too much hydrogen causes extra instability (Domen et al. 2014).

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## Fabrication Process of TAOS TFTs

Fabrication processes of TAOS TFTs for practical displays are similar to those of the current a-Si:H TFTs because most of TAOS TFTs employ the inverted staggered structure like a-Si:H TFTs. For practical TFTs, passivation technology should be considered to improve the instability issues. For driving LCDs, biases are applied under light illumination during most of operation time. Thus, the instability under positive/negative bias under light illumination (P/NBIS) is important, and NBIS is much serious for TAOS TFTs. Figure 15 shows changes in transfer curves of a-Hf-In-Zn-O TFT subjected to negative-bias stress at  $V_{\text{GS}} = -20$  V without (NBS) and with light illumination (NBIS) (Park et al. 2010a; Kwon et al. 2010). Large negative  $\Delta V_{\text{th}}$  and increase in  $I_{\text{off}}$  are conspicuous for the TFTs subjected to the NBIS condition. Such observation was commonly reported for oxide TFTs including a-IGZO and polycrystalline ZnO. Recent researches have clarified that



**Fig. 15** Changes in transfer curves of a-Hf-In-Zn-O TFT with voltage bias and light illumination

these changes can be largely reduced by applying passivation of back channel such as dense  $\text{Al}_2\text{O}_3$  (Park et al. 2010b, 2013), implying that photo-induced desorption of atmospheric components such as  $\text{O}_2$  and  $\text{H}_2\text{O}$  plays an important role in these phenomena.

The typical fabrication process of TAOS TFT was already shown in Fig. 1. This structure, bottom-gate and top-contact inverted staggered structure, is similar to that of a-Si:H TFTs. It is known that the channel thickness should be less than 100 nm for a-IGZO TFTs; otherwise,  $V_{\text{th}}$  shifts to negative with increasing the channel thickness. Therefore, a-IGZO TFTs employ 30–50 nm thick channels for research purposes, while thicker channels  $\sim 70$  nm would be employed for mass production probably due to better controllability and yield for mass production over a large area.

Exposure of the back channel of the TAOS layer to hydrogen-bearing plasma must be strictly avoided because hydrogen impregnated in the TAOS serves as donor by releasing an electron as explained in section “[Electron Transport and Subgap Defects in TAOS.](#)” For example, direct deposition of SiN/SiON by PE-CVD with  $\text{SiH}_4$  makes the TAOS layer conducting (Sato et al. 2009). This result originates from the ionization of  $\text{H}^0$  in the TAOS (this is also true for most transparent conductive oxides such as ZnO); i.e., the reaction  $-\text{M}-\text{O} + \text{H}^0 = > -\text{M}-\text{O}-\text{H}^+ + \text{e}^-$  (Nomura et al. 2013). It should also be noticed that H impurity would also cause instability issues because  $\text{H}^+$  is expected to easily migrate under electric field (Domen et al. 2014).

The electrode materials should be robust against oxidation, diffusion, and intermixing with the TAOS channel so as not to form a resistive oxide layer; e.g., Al is easily oxidized and forms very insulating  $\text{Al}_2\text{O}_3$ , while W, Mo, and Ta, their alloys, etc., are tough for oxidation at the processing temperatures up to 400 °C. ITO and Ti are good in forming ohmic contact because their work functions are close to those of TAOS (Shimura et al. 2008). Ti easily forms  $\text{TiO}_x$  ( $x \ll 2.0$ )  $\leftarrow$  ( $x \ll 2.0$ );

however, the suboxide  $\text{TiO}_x$  is still conducting and not so bad for source/drain contacts. On the other hand, it is considered that such  $\text{TiO}_x$  would cause  $V_{\text{DS}}$ -bias instability due to oxygen migration. To obtain better ohmic contact with smaller contact resistance, it would be better to form a heavily doped interfacial layer between the TAOS channel and the electrode metal (similar to the  $n^+$  layer in a-Si:H TFTs). This can be carried out by reduction of the TAOS contact areas by Ar sputtering, H doping from H plasma, or H-containing deposition of an upper layer such as SiN and SiON. Formation of heavily doped a-TCO such as IZO has also been examined.

Figure 1 illustrates mainly for etch-stopper (ES)-type TFTs but can be red for back-channel-etch (BCE)-type ones if the ES layer (ESL) is removed from step II and the later steps. The upper metal electrode layer is isolated to source and drain regions by wet etching at step III. In the BCE case, etching penetrates inside to the TAOS channel layer; therefore, it is important to control the etching depth very precisely. This is a reason why a-Si:H TFT employs a very thick channel ( $\sim 250$  nm), but as explained above, it is difficult for TAOS TFTs to employ such very thick channel due to the electrical property change and the increased tact time for the channel layer formation. In addition, it is not easy to get high selectivity for etching between the TAOS and the metal materials. Usually, PAN (phosphoric acid – acetic acid – nitric acid) etchant is used for metal etching, but the etching selectivity between IGZO and Mo is very small. SACHEM Europe develops a new chemical (SACHEM's proprietary formulations, details not disclosed) that etches Mo but IGZO very slowly (Vermeulen et al. 2013). Another approach to overcome this issue is to employ more robust channel materials. As explained above, SEL claims that CAAC IGZO is easy to make BCE-type TFTs. Kobe Steel, Ltd. and Idemitsu propose a new oxide material, which would be ITZO or its relatives (Ochi et al. 2013). BCE-type TFTs have another issue because the etched back channels have high-density defects and would cause deterioration and instability issues. This may be improved by employing appropriate annealing, plasma treatment, or forming appropriate passivation layers (see “Optional process” in Fig. 1).

Another way to avoid the BCE issue is to employ an ESL structure, where an ESL is formed by  $\text{SiO}_2$  or else before formation of the upper metal layer. This process is free from the back-channel etching damage and the etching selectivity issue, but the channel length becomes larger than those of BCE TFTs if the same design rule is employed. In addition, an additional lithography mask and step are required (compare the PEP steps for BCE and ES), causing extra production cost. Therefore, it is important to employ the BCE process for lower cost and higher resolution/miniaturation.

For the ESL and passivation layers, hydrogen issues should be considered because their process temperatures are in general lower than that of the bottom-gate insulators and contain much hydrogens (Nag et al. 2014; Templier et al. 2014); therefore, deposition temperature, post-thermal annealing temperature, and gas conditions should be finely tuned to obtain desired TFT characteristics and better stability.

## Perspective

Fundamental research on TAOS TFTs has progressed very rapidly in the last decade. This is particularly true for a-IGZO TFTs. The main advantages of a-IGZO TFTs are scalability, uniformity, availability of low temperature process, and a wide range of material choice for gate insulators. As a result, the major instability issues appear resolved for practical applications, and mass production of TAOS TFT-based FPDs started in 2012.

The next technical challenge in TAOS TFTs will be the development of non-vacuum process (Kamiya and Hosono 2012; Lee et al. 2007). Although research on this subject is rapidly increasing, examination of device reliability has not been performed satisfactory. The ultimate goal of this research is to fabricate high performance TFTs on plastics or polymer-coated papers leading to flexible/paper displays. Recently, Evonik provides several sets of solution chemicals for TFTs (iXsenic S material platform), which has been examined by several groups (Cobb et al. 2014). As such, inventions of innovative material and processing beyond the traditional sol-gel or solution process would be needed.

Another technical challenge in oxide TFTs is to realize CMOS. Transparent oxide semiconductors (TOS) were born from TCO. The requirements for TOS rather differ from those for the latter. Control of carrier concentration and carrier type is essentially important for TOS. The current status of TOS is far from this ideal situation in particular for carrier polarity control. Although many papers have reported p-type TOSs including p-type ZnO, Cu<sub>2</sub>O, and p-SnO and some p-SnO TFTs have large mobilities, these are still at the research stage and not considered for practical devices. This is due to high-density hole traps (Matsuzaki et al. 2008) and narrow process window probably arising from the instability of the multivalent cations such as Sn (Sn<sup>0</sup>, Sn<sup>2+</sup>, and Sn<sup>4+</sup>) and Cu (Cu<sup>0</sup>, Cu<sup>+</sup>, and Cu<sup>2+</sup>). For example, Cu<sub>2</sub>O is a well-known p-type semiconductor and has attracted attention as the active layer since the first TFT parent proposed by Heil in 1935. Matsuzaki et al. fabricated epitaxial thin films and obtained Hall mobility of  $\sim 100 \text{ cm}^2(\text{Vs})^{-1}$  at the hole concentration of  $\sim 10^{13} \text{ cm}^{-3}$ , which is comparable to that in single-crystalline Cu<sub>2</sub>O. However, Cu<sub>2</sub>O-based TFT did not operate satisfactory and the estimated field-effect mobility remained  $\sim 0.1 \text{ cm}^2(\text{Vs})^{-1}$  (Matsuzaki et al. 2008). This striking difference comes from large hole trap densities. Such a situation appears to be similar to other p-type oxide semiconductors. In 2008, Ogo et al. (2008a, 2009) reported a p-channel TFT with the mobility of  $1.4 \text{ cm}^2(\text{Vs})^{-1}$  employing SnO (not SnO<sub>2</sub>) as the active layer. This is a first demonstration of p-channel oxide TFT with a mobility  $> 1 \text{ cm}^2(\text{Vs})^{-1}$ , which was a long-standing target in this area.

The next goal is fabrication of CMOS by combining p-channel and n-channel oxide TFTs. Although the monopolar channel is enough for pixel TFTs in FPDs, CMOS is better used for peripheral and other logic circuits. Exploiting bipolar semiconductive oxides with low tail state densities that can be fabricated at low temperatures is ahead as the most essential work for this goal. Oxide semiconductors are easily fabricated by conventional sputtering and are robust to oxygen and

radiation, in general. If oxide-based CMOS circuits can be fabricated on various types of substrates including plastics, flexible electronic circuits would be promising. Ambipolar TFT utilizing an n-type TOS/p-type organic semiconductor heterojunction channel and oxide–organic TFT hybrid CMOS circuits (Nomura et al. 2010b) are a practical and promising approach to realize active device applications such as photo-sensors, CMOS circuits, and solar cells.

The coming challenge of TAOS TFTs is the application to the backplane of OLEDs. In particular, large-size OLEDs are expected to be driven by oxide TFTs because the fabrication of large-size LTPS TFT backplane is costly and technically difficult. There are several obstacles to overcome for practical applications, i.e., higher stability, higher mobility, and compatibility with the OLED structure (the inverted stacking OLED structure is favorable for n-channel TFTs like TAOS TFTs). We expect that a breakthrough in TAOS TFTs based on a novel idea will resolve these issues.

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