Towards Self-Powered Systems: Using Nanostructures to Harvest Ambient Energy

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Abstract In this chapter, we present the advantages of semiconducting nanostructures (nanowires) for energy harvesting applications. Three sources of energy are considered: mechanical inputs, light and thermal energy. Different simulation approaches are used to discuss the prospects of these energy transduction solutions at nanoscale. Some guidelines are brought out for the improvement of energy conversion efficiency by nanowires, when integrated into functional devices.

1 Introduction

The combination of new materials integration, 3D processing and low-power circuits enable the development of autonomous systems. These systems are typically used on Wireless Sensors Networks (WSN) applications, with the objective to monitor human health, environment, or structures such as airplanes or buildings [1]. Three main issues need to be addressed to improve the performance of the autonomous systems: (i) the reduction of the overall energy consumption to ideally

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less than about 100 μW [2], (ii) the reduction of the general size and/or surface for easier integration and (iii) the augmentation of the power autonomy or battery lifetime. To solve this last issue, ambient energy harvesting is a promising solution. In addition, this solution allows the maintenance cost associated to battery replacement and/or charging to be cut down or even suppressed.

An autonomous system is composed of several subsystems [2] for computing, communication, sensing, energy management and energy harvesting, respectively. Basically, the energy from the harvester must be processed before been stored in a capacitor or a rechargeable battery, and later used in the system. This chapter will only deal with the strictly speaking energy harvesting subsystem.

To date, several approaches have been proposed to harvest energy from different energy sources, such as thermal, solar, RF, or mechanical sources [3], using thin films and MEMS technologies. With the advent of ultra-low power circuits, the energy needed for autonomous systems can be harvested by even smaller structures and, eventually, nanostructures. Most importantly, some properties of nanostructures can be controlled and improved compared to bulk [4, 5].

In this paper we present the advantages and prospects of using semiconducting nanostructures (nanowires) for energy harvesting applications from three different sources: mechanical inputs, solar and thermal energy sources. The chapter is divided in three main sections focalized on each energy conversion. Each section provides first a brief review of the concepts at the macro and micro scales, before discussing the main advantages at the nano scale from a theoretical point of view, supported by simulation and modeling results. The chapter ends by the conclusions and perspectives.

2 Mechanical Energy Harvesting Using Piezoelectric Nanostructures

Many approaches have been proposed to harvest ambient mechanical energy: using the variation of electromagnetic or electrostatic fields and using piezoelectric materials [3]. All these approaches have been largely studied at the macro and micro scale leading to some commercial devices. This section is focalized on piezoelectric materials, where electrical charges are generated when a mechanical load is applied (direct effect), or which get strained when an electric field is applied (reverse effect). This property is quantified by the piezoelectric coefficients (d), measured in C/N or pm/V, respectively. In what follows, we will firstly sum up briefly the approach used at the macro scale to harvest energy from mechanical inputs, before introducing the different approaches that can be used with nanoscale piezoelectric materials.

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Chapter No.: 11 | Date: 22-7-2014 Time: 6:26 pm | Page: 225/240

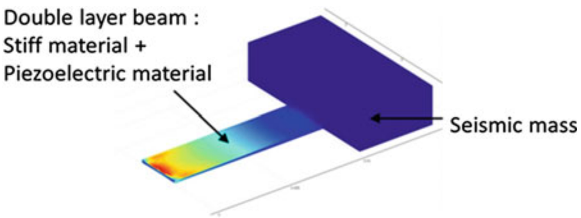

Fig. 1 Schematic structure of a resonant piezoelectric cantilever illustrating the location of the maximum stress (fixed end). The dimension of the cantilever and the weight of the seismic mass are adjusted to match a resonance frequency driven by the application

2.1 The MEMS Approach

At the macroscale, the most widely used structure to harvest mechanical inputs with piezoelectric materials is a resonant cantilever composed of a stiff material (Si or plastic), a piezoelectric layer (typically PZT or AlN, between others), and a seismic mass (Fig. 1). The whole structure is tuned to resonate at a specific frequency driven by the application (typically between a few Hz and several 100 Hz). The aim is to increase the quality factor (*Q*) of the resonator, at the expense however of bandwidth narrowing [6]. Many devices have been reported using this structure, with generated energy density values ranging from 0.1 to 40 mW/cm^3 [3], for input accelerations between 1 and 10 m/s^2, corresponding to a force in the range of 30 µN–40 mN. Commercial devices can also be found from companies such as Midé (USA) proposing devices generating 9 mW/cm^3 at 15 V using a PZT film integrated into a plastic beam.

Several strategies have been proposed to increase the bandwidth of cantilever based devices, including bi-stables structures, coupled oscillators, arrays of cantilevers featuring different resonance frequencies, or the addition of amplitude limiters, between others [7].

2.2 Piezoelectricity at the Nanoscale

The reduction of beam size down to the nanoscale has been proven to improve the elastic properties, such as flexibility compared to bulk materials. Fracture strain is also increased [8]. It has also been shown that size reduction resulted in improvements of the piezoelectric coefficients (in particular d_{33}, longitudinal, along the c-axis) of semiconducting materials such as GaN and ZnO in form of nanowires (NWs) with diameters wider than 150 nm [9] or nanoribbons thicker than 500 nm [10] (see Table 1) leading to a higher voltage generated (i.e. more power and better energy conversion efficiency) for given deformation [11].

Table 1 Piezoelectric coefficient d_{33} in ZnO and GaN nanostructured materials compared to bulk (adapted from [16])

d_{33} [pm/V]			
Material	Experimental (bulk)	Experimental (nanoscale)	Theoretical (nanoscale)
ZnO	9.93 [10]	14-26.7 [10]	168.2 [12]
GaN	1.86 [12]	12.8 [9]	65.8 [12]

The experimental trends of these piezoelectric coefficients have been confirmed by theoretical studies on semiconducting NWs (GaN, ZnO and more recently AlN NWs), although at lower diameters (a few nm) (see Table 1). These calculations have used different approaches such as first principles-based density functional theory (DFT) [12] or continuum models including surface effects from ab initio calculations [13]. More recent calculations using the finite element method (FEM) have included the semiconducting properties of individual ZnO NWs (i.e. doping level and free charges) showing their impact on the reduction of the generated piezo-potential (screening effect) [14, 15] and thus on the effective piezoelectric coefficients. These results altogether show that there is still a gap between theoretical predictions and experimental measurements.

2.3 Integrated Piezoelectric Nanowires into Functional Devices

As dimensions decrease, the resonant approach becomes less appropriate for energy harvesting since most mechanical sources present in the environment are at low frequency or frequency-less, and solutions that exploit real-time deformations and impacts are thus better suited [17]. In addition, one single NW will not give enough energy for typical autonomous systems, so that practical harvesting devices must integrate large arrays of piezoelectric NWs. Several integration techniques have been reported in the literature, including lateral [18–22], vertical [20, 23, 24] and radial integration [25, 26] of ZnO, PZT, $NaNbO_3$ and PVDF NWs. To date, the most performing device integrates vertically grown ZnO NWs. It produces 0.78 W/cm^3 (estimated from output voltage and output current, measured in open and short circuit conditions, with values of 58 V and 134 µA, respectively) when a non-quantified mechanical input is applied on the device (palm impact) [27]. While most of the effort has been invested on proof of concept demonstrations and device fabrication, fewer references can be found in the literature about the theoretical analysis of the performances of such devices and the identification of optimization guidelines.

Analytical modeling is an effective way to predict general trends for device performance evolution and, especially, the influence of dimensions downscaling. Such approach has been used for vertically integrated ZnO NWs deformed by lateral or compressive forces. One example of device designed to use lateral forces to bend

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Chapter No.: 11 Date: 22-7-2014 Time: 6:26 pm Page: 227/240

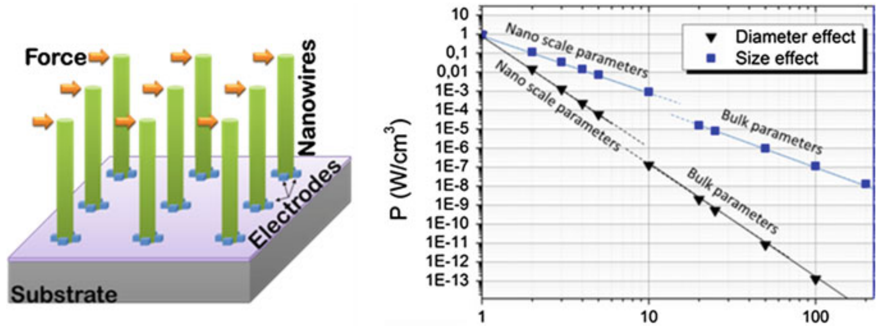

Fig. 2 Structure of a mechanical energy harvester using lateral forces applied on ZnO NWs (*left*). Effect of the NWs diameter and size (fixed aspect ratio of 20) on the power density generated from the device. The smallest scaling factor $\alpha = 1$ represents 50 nm-wide and 600 nm-long NWs (*right*) (adapted from [11])

vertically grown NWs is schematically presented in Fig. 2 (left) [11]. An analytical model has been used to study the power density harvested as a function of NWs geometrical parameters (Fig. 2 right panel) under the assumption of a constant peak lateral force (10 nN) and an average of 50 mechanical deformations per second (not necessarily periodic). Downscaling of NW size (diameter and length scaled together with fixed aspect ratio) or diameter (diameter scaled alone with fixed length) results in a large power density increase, with a maximum of 1 W/cm^3 at the minimal geometry considered (scaling factor $\alpha = 1$ representing 50 nm-wide, 600 nm-long NWs), which is compatible with the requirements of autonomous systems. Although promising, the main issue of this device would be the placement of the metallic contacts at the bottom of the device (see Fig. 2 left panel) that would be technologically challenging. These contacts could be fabricated using E-beam lithography or nanoimprint for instance, before the selective growth of the NWs.

Vertically grown ZnO NWs integrated into devices operating in compression mode have been modeled by several groups using different approaches. In 2012, Graton et al. developed a lumped circuit model of one million of NWs connected in parallel with bottom (Ohmic) and top (Schottky) metallic contacts (Fig. 3a). A maximum of 2.9 W_{rms}/cm^3 (19.4 V and 1.86 nA with an optimal load of 10 GΩ) has been reported when a compressive force of 1.2 μN at 50 Hz is applied to the device. Simulation results have shown that the reduction of NWs diameter should increase power density [15]. In 2011, Hu et al. have modeled two layers of vertical NWs integrated on a flexible polymer substrate as a continuous medium using FEM [28], predicting 80 V output voltage under bending. The fabricated devices delivered 10 V, which is quite high, even if still one step behind theoretical predictions. In 2012, Hinchet et al. have determined preliminary design guidelines for the VING (Vertically Integrated Nano Generator) architecture (Fig. 3b). This device includes a bottom electrode, a layer of ZnO NWs immersed in a polymer matrix (around and over the NWs) and a top electrode. The whole structure is fabricated typically on a Si substrate. FEM models (Fig. 4a) were developed

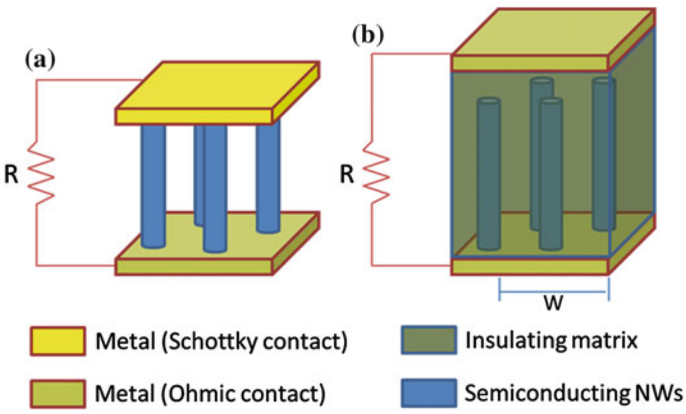

Fig. 3 **a** Structure of a device integrating vertical NWs between two metallic contacts. **b** Structure of a VING device (adapted from [16])

showing that Poly(methyl methacrylate) (PMMA) was a good matrix material and that an optimum in generated energy density was obtained for: (i) NWs separated by distances similar to their diameter (Fig. 4b) and (ii) a thinner PMMA layer over the NWs [29]. The range of parameters explored corresponded to typical experimental values for grown NWs, with 50–200 nm-wide NWs, separated by distances of 50 nm–1 μm. The maximal reported energy density was close to 10 pJ/cm^2 (65 mV) for a given peak pressure of 1 MPa. This corresponds to 20 nW/cm^3 after 50 compressions (and decompressions) per second, considering a 500 μm thick device (substrate). These results still need to be validated by experiments.

2.4 Further Improvements at the Nanoscale

Piezoelectric properties can still be further improved at the nanoscale. Recent near field (AFM) experiments on GaN NWs (25 nm-wide, 500 nm-long) including a thin AlN (8 nm) barrier along their c-axis, have shown an estimated piezoelectric coefficient 9 times higher compared to intrinsic GaN NWs with the same dimensions [30]. This would increase the efficiency of the energy conversion and the power density generated by harvesting devices [11].

3 Solar Energy Harvesting Using Semiconducting Nanostructures

Most of the world solar cell production is based on bulk (thick) silicon wafers. These solar cells are called first generation solar cells. Their main drawback is the cost of the material mainly induced by silicon purification, crystallisation and in-got and wafers

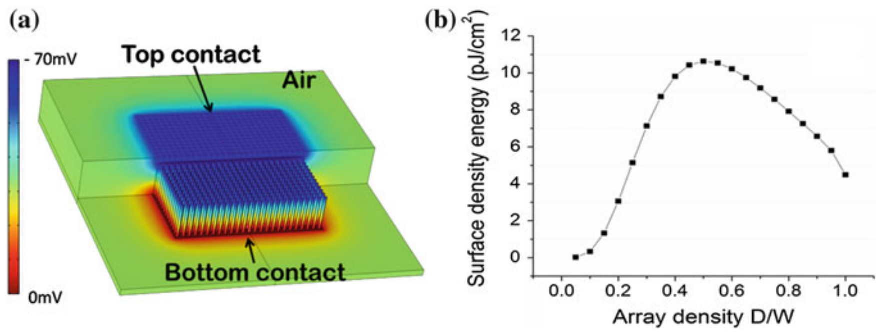

Fig. 4 **a** FEM simulation of the potential generated in a VING device surrounded by air and integrating 625 ZnO NWs in a PMMA matrix, for a pitch (defined as the ratio D/W between NW diameter and cell width) of 0.5, which corresponds to NWs separated by a distance equal to their diameter. **b** Surface density of mechanical energy stored in the VING as a function of D/W

sawing. One way to lower photovoltaic cost is therefore to reduce material consumption. However, it is then necessary to improve light trapping scheme in order to keep high absorption in the material. Silicon nanowires (NWs) based solar cells are an attractive approach to realize solar cells with an efficient light trapping scheme, potentially combined with high collection efficiency in the case of radial junctions. Indeed, the high-aspect-ratio of nanowires permits to reduce significantly solar cell thickness without loss of optical absorption while simultaneously providing effective carrier collection in the case of radial junction [31]. This structure benefits from the long optical path within the NW length and by exploiting a radial junction, a shorter path for carrier collection corresponding to the NW radius, leading to a smaller carrier recombination rate. Efficiencies similar or higher than the ones obtained with first generation solar cells (about 14–18 %) are expected for single junction nanowire solar cells with a cost reduction thanks to reduced material consumption and to low-cost growth methods.

There are two main approaches to elaborate the NWs arrays: a bottom-up approach based on the growth of the NWs and a top-down approach based on etching methods. Top-down approach has the disadvantage of wasting large quantity of matter, thus increasing the device cost. In contrast, the bottom-up approach is low-cost, technologically competitive and promising for photovoltaic energy.

Therefore, Si NWs arrays for photovoltaic applications are usually grown by Chemical Vapor Deposition (CVD) on top of silicon wafer, glass substrate or metal [31–35]. In the framework of the CVD method, the most used technique is the vapor liquid solid method which uses a metal catalyst to form a liquid eutectic with the desired NW material. Radial pn junction can be realized by diffusion of doping species from the NW surface. However, due to the small diameter of the NW, if the diffusion time is too long, there might be a complete doping resulting in a suppression of the pn junction. Another way to create the radial pn junction is to deposit a conformal and doped polysilicon layer on the NW. However, in the latter case, the interface is usually highly recombinant and should be passivated.

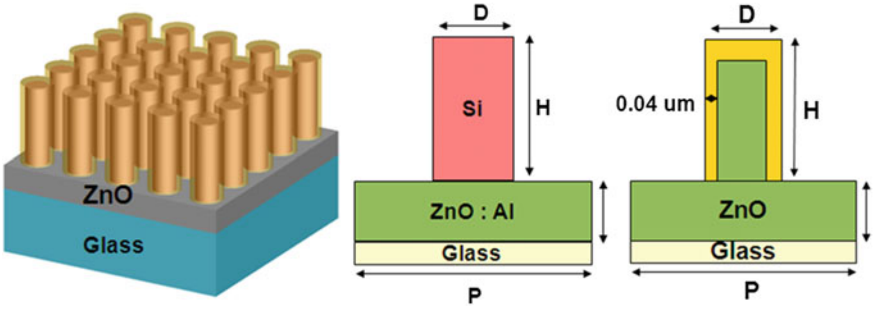

Fig. 5 NW based solar cell on ZnO on glass substrate (*left*); Si NW (*middle*); CdTe/ZnO NW (*right*), yellow shell is CdTe (adapted from Ref. [46])

The amorphous silicon / crystalline silicon (a-Si/c-Si) heterostructure is a good candidate for NW based solar cells since the heterostructure is able to efficiently separate the carriers while a-Si acts as a good surface passivation. The a-Si/c-Si heterojunction has already demonstrated high efficiency for first generation solar cells [36].

Increasing efforts have also been dedicated to the development of nanostructures based on ZnO thanks to its ability to grow within the NW morphology by a wide variety of growth methods such as CVD [37], chemical bath deposition [38] or electro-deposition [39]. Such NWs can be covered with CdSe [40], ZnS [41], ZnSe [42], or CdTe [38, 43] in order to create a type II band alignment heterojunction. The latter is a very efficient absorbing material with a bandgap energy of 1.5 eV at room temperature and will be also studied in this work in order to perform a comparison with Si NWs which are less absorbent due to the Si indirect band gap.

The relatively low experimental efficiencies obtained up to now (experimental power conversion efficiency of 7.9 and 4.74 % has already been reported for grown Si NW arrays [44] and ZnO/CdSe [45], respectively) are mainly due to high surface recombination velocity and to series and shunt resistance. There are still technological improvements needed to grow high quality NWs and to reduce surface recombination.

To optimize the absorption, it is necessary to define the best geometry by using optical simulations. Two types of materials have been compared: silicon NWs as the reference material with indirect band gap; ZnO NWs with CdTe radial heterojunction as the absorbing direct band gap material [46].

Simulation activities were performed using a Rigourous Coupled Wave Analysis (RCWA) 3D software for the optical simulations. For each structure (Fig. 5), the solar cells based on Si and ZnO/CdTe NWs have been simulated and an optimized geometry from an optical point of view has been defined [46]. The absorption versus wavelength of the incident light was deduced from the simulations of each structure (defined period and diameter) and the ideal short circuit current density (all generated electron/hole pairs are collected) corresponding to

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Chapter No.: 11 Date: 22-7-2014 Time: 6:26 pm Page: 231/240

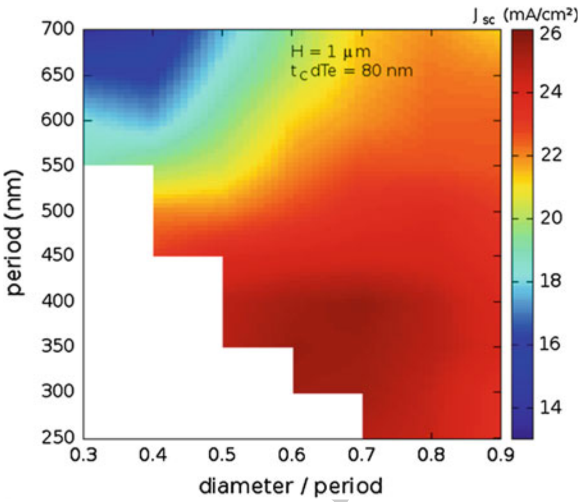

Fig. 6 Ideal short circuit current density computed with the RCWA tool for ZnO/CdTe core/shell NW arrays for different values of period and ratio between diameter and period. NW length is 1 µm. CdTe thickness is 80 nm

the standard AM1.5 incident light was then calculated [46]. An example of short circuit current density map versus period and diameter to period ratio is presented in Fig. 6 for ZnO/CdTe structure.

It was found that the NW structure significantly increases photons absorption compared to a planar structure with the same amount of material, especially in the case of indirect band gap semiconductor.

Compared to Si NW arrays, ZnO/CdTe NW array provided higher absorption with a less compact structure resulting in a smaller amount of material used thanks to the higher absorption of CdTe.

4 Thermal Energy Harvesting Using Semiconducting Nanostructures

In most of electronic and mechanical systems, a significant amount of power is wasted into heat. This power could be partially harvested by converting the resulting temperature gradients into electric power thanks to thermoelectric (TE) materials.

The efficiency of the thermoelectric devices is related to the dimensionless figure of merit $ZT = \sigma S^2 T/\kappa$, where σ is the carrier conductivity, S is the Seebeck coefficient, T is the temperature, κ is the thermal conductivity and Z is called the power factor. In order to attain large values of ZT, it is required a device/material with high carrier conductivity, large Seebeck coefficient and, at the same time, low thermal conductivity. For ordinary bulk semiconductors, ZT is far below 1. In 1990s, the thermoelectric materials regained attention as the low-dimensional systems were proposed to potentially have high thermoelectric figure of merit due to the presence of interfaces and the consequent thermal conductivity reduction below the alloy limit [47]. A largely investigated possibility to increase *ZT* is to consider bulk nanostructured materials. By using this approach, an enhancement of the figure of merit of BiTe was obtained [48] from 1 to 1.4. An alternative strategy to improve the thermoelectric efficiency is using energy filtering at the interfaces [49, 50]. In the energy-filtering technique, energy barriers are used to block the low-energy electrons and, therefore, increase the average heat transported per carrier. Hence, the Seebeck coefficient increases and could result in an enhanced power factor [51]. However, the same interfaces can also substantially reduce the mobility and, therefore, such an approach requires careful design of the nanostructures. Alternatively, the introduction of resonant impurity levels inside the conduction or valance band was proposed to create sharp features in the density of states and increase the Seebeck coefficient [52]. Another possibility is to increase the electron conductivity via modulation doping. In such an approach, charge carriers are spatially separated from their parent impurity atoms and consequently the impurity scattering is reduced [53].

Finally, much attention has been devoted to semiconductor NWs, which are particularly promising structures due to their low density of states and the high surface/volume ratio. Although this interest was initially motivated by hopes of taking advantage of electron confinement in the structures, it soon became clear that another advantage of NWs was their potentially strongly reduced thermal conductivity [54]. A large reduction in Si NW lattice thermal conductivity was experimentally reported in 2003, further stimulating research activities in this area [55]. An astonishingly low thermal conductivity has also been claimed on Si NWs due to the effect of surface roughness [56]. Recent works show that the interplay between alloy scattering and scattering by the nanostructured features can lead to interesting qualitative differences between the behavior of the thermal conductivity of alloy and non-alloy structures [57].

From a theoretical point of view, accurate models free of adjustable parameters are the most reliable way of computing fundamental phonon transport properties [58, 59]. Thermal conductivity in NWs in the presence of roughness or other spatial defects is addressed either within the semi-classical Boltzmann transport [60], which cannot take into account phase-coherent phenomena, or within non-equilibrium Green's function techniques, which usually consider only elastic transport [61, 62].

4.1 Simulation of Thermoelectric Properties of Rough Si NWs

The understanding of phonon confinement and phonon scattering effects in nanostructures is a key to any thermal transport engineering for the improvement of the thermoelectric performances. Here, we present 3D simulations of phonon properties in confined structures as semiconductor NWs in the presence of spatial

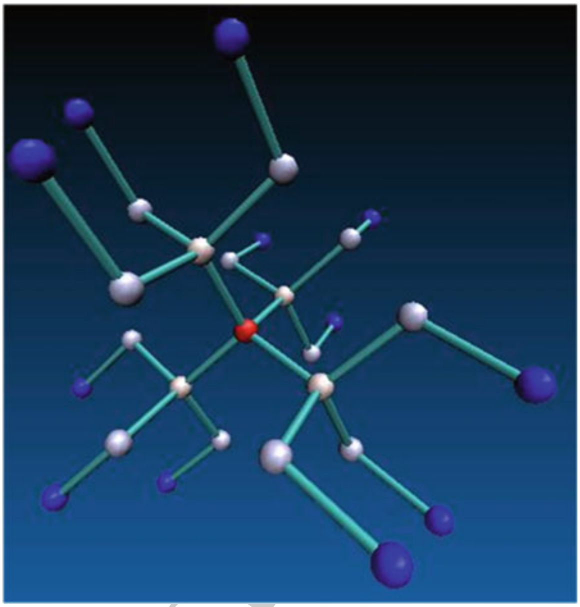

Fig. 7 Sketch of the extended valence force model showing the coupling of a single Si atom with its 28 first neighbor atoms

fluctuations. We address phonon band structures and heat flux within a full-quantum mechanical theory and further couple these results with self-consistent electron transport calculations in order to extract relevant factors of merit of thermoelectric devices.

The phonon band structure calculations were obtained by implementing an extended Keating model including four terms (bond-stretching, bond-bending, angle-angle and bond-bond interactions) for the determination of the dynamical matrices of nanosystems [63]. A scheme of the coupling of a single atom with its neighbors is shown in Fig. 7.

This model uses material constants that are chosen to reproduce the bulk phonon dispersion and then it is extended to compute the confined modes of NWs, which are assumed to be infinite and composed of identical unit cells. The NWs simulated with such an atomistic description can be naturally generalized to any crystallographic orientation and include the presence of random disorder (e.g. roughness, crystal defects). From the dynamical matrices, the NW basic phonon properties, as band structure and density of states, can be extracted. For example, Fig. 8 shows the phonon band structure and the corresponding density of states (DOS) of a square <100> oriented Si NW with a lateral cross section of $2 \times 2\ \mathrm{nm}^2$.

Hence, starting from the dynamical matrices computed with the extended Keating model, we were able to implement a recursive algorithm based on the Sancho-Rubio iterative scheme [64] to compute the surface and bulk Green's function of Si NWs. The first application of this code was to evaluate in an alternative way the DOS of the NW in Fig. 8(left), previously computed via a

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Chapter No.: 11 | Date: 22-7-2014 | Time: 6:26 pm | Page: 234/240

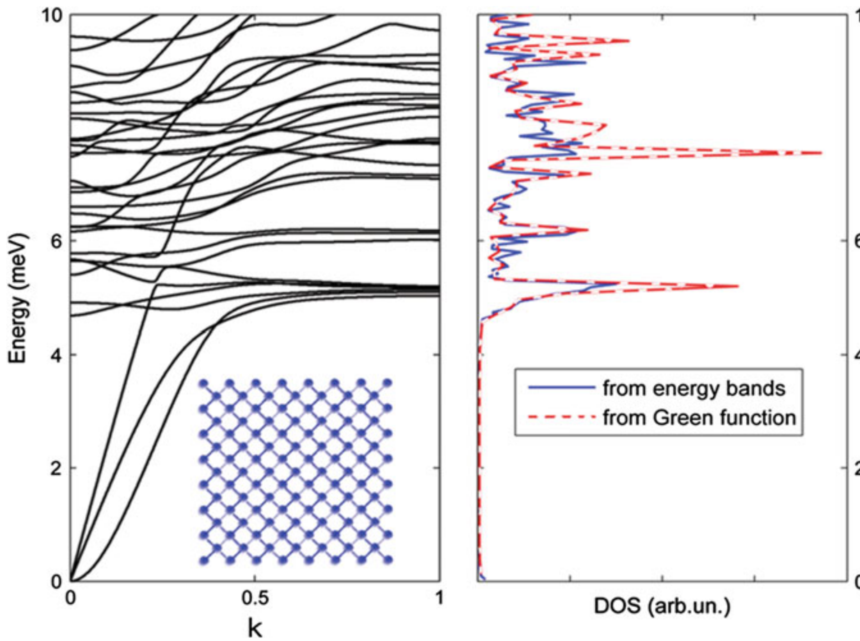

Fig. 8 Phonon band structure of a <100> Si NW with a squared cross section of 2 × 2 nm2 (*left*) and the corresponding density of states (*right*) obtained from the direct counting of energy eigenvalues in the band structure (*solid line*) and from the retarded Green's function (*dotted line*)

direct counting of the energy bands. The DOS computed via the two alternative methods presented the same features validating the methodology.

Based on the non-equilibrium Green's function formalism [65], we computed the phonon transport properties as thermal conductivity at different temperatures of silicon NWs in the presence of surface roughness. Importantly, such a kind of calculation can be easily extended to other geometries as superlattices and quantum dots and other semiconductor materials as Ge and III-V compounds.

We considered a square <100> oriented NW with an edge of 5 nm and different roughness root mean square (r.m.s.) values [66]. Surface roughness was geometrically generated with a random algorithm as described in [67]. Our results reported in Fig. 9 clearly show that surface roughness induces a strong decrease of the thermal conductance. Even a small value of roughness *r.m.s.* is able to considerably reduce the transmission in the whole frequency spectrum (left panel) and consequently strongly suppresses the thermal conductivity (right panel).

Finally, 3D atomistic simulations within the Keldysh-Green's function formalism were exploited to evaluate the increase of the factor of merit *ZT* due to the presence of surface roughness in silicon NWs. The Seebeck coefficient *S*, the electrical conductance *G* and the corresponding power factor S^2G have been computed for rectangular NWs with cross sections of 5 × 5 nm^2 and 3 × 3 nm^2 and for surface roughness *r.m.s.* 0.2 and 0.4 nm. The evolution of these parameters

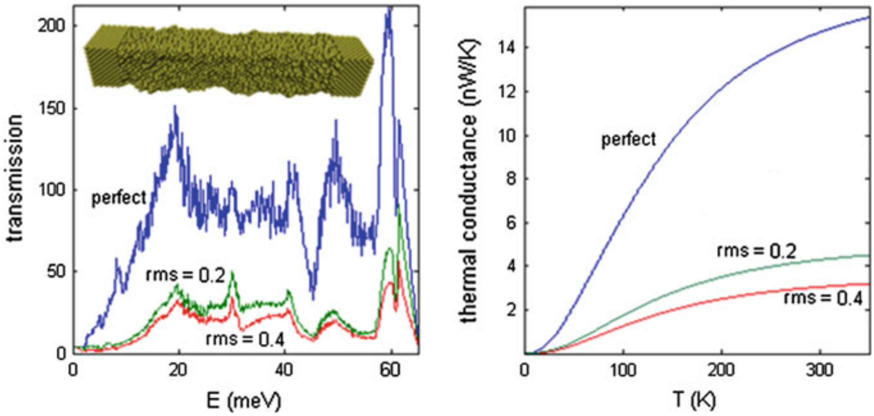

Fig. 9 Phonon transmission (*left panel*) and thermal conductivity (*right panel*) of a Si NW (*inset*) with square section of 5 × 5 nm^2 and in the absence (*blue lines*) and in the presence of surface roughness with *r.m.s.* 0.2 nm (green lines) and 0.4 nm (*red lines*)

as a function of the surface roughness *r.m.s.* is shown in Fig. 10a, where we can observe the opposite behavior of the Seebeck coefficient and of the electrical conductance as the roughness increases. The increase of the Seebeck coefficient due to surface roughness can be explained by analyzing the shape of the spectral density of the transmission probability. This implies that, as shown in Fig. 10b, the power factor, which expresses the electrical performance of the thermoelectric materials, monotonically decreases with increasing the roughness.

However, such decrease of the factor S^2G has to be compared with the corresponding decrease of the thermal conductance shown in Fig. 11a. For this, we can remark that the phonon conductance is strongly suppressed by both the lateral confinement and by the surface roughness. Phonon transmission is therefore decreased when the surface/volume ratio is as small as possible. As shown in Fig. 11b, this behavior results in an increase of the factor of merit *ZT* up to about 0.7 for very thin NWs with a 3 × 3 nm^2 lateral section and 0.2 nm of surface roughness *r.m.s.* In this configuration, *ZT* turns out to be increased, because phonon thermal conductance decreases faster than the power factor with decreasing the wire cross sections.

5 Conclusions and Perspectives

Several properties can be improved at the nanoscale compared to bulk materials: higher piezoelectric coefficients and flexibility, higher photon absorption, lower thermal conduction between others. These improvements make nanostructures promising for mechanical, solar and thermal energy harvesting but also for sensing

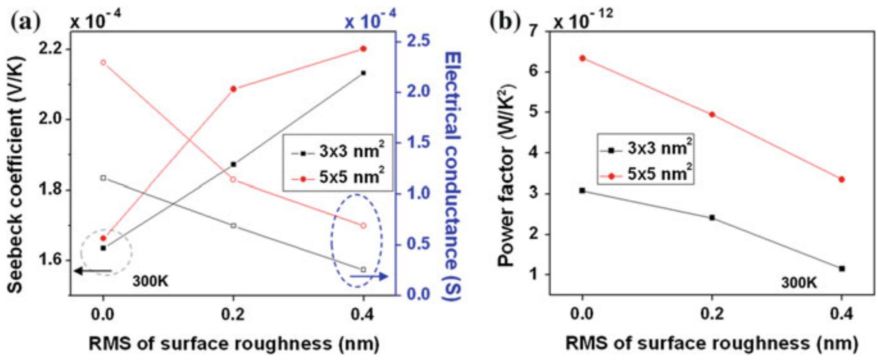

Fig. 10 **a** Seebeck coefficient and electrical conductance and **b** power factor as a function of the surface roughness rms of Si NWs with different cross sections of 3 × 3 and 5 × 5 nm^2

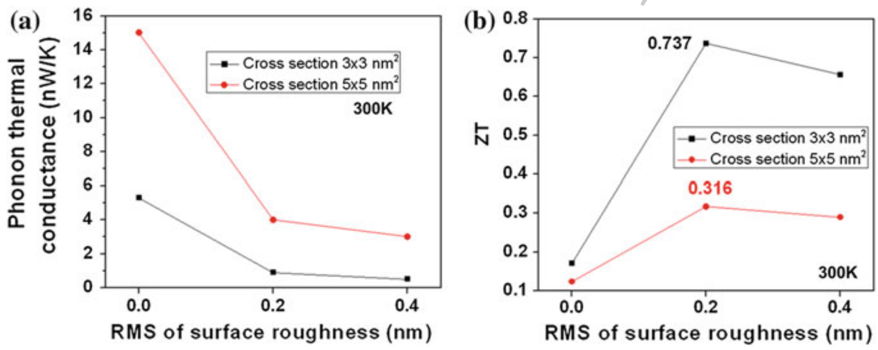

Fig. 11 **a** Phonon thermal conductance and **b** the ZT factor of merit as a function of the surface roughness rms of Si NWs with different cross sections of 3 × 3 and 5 × 5 nm^2

applications, although multiple technical issues concerning their integration into functional devices need to be solved to improve the global efficiency.

Very few models can be found in the literature concerning the performances optimization of devices based on NWs for energy conversion applications. The models reviewed in this work proposed optimization guideline rules on the choice of materials, NWs geometries (diameter, length) and roughness to improve the energy conversion efficiency for the three mentioned harvesting applications, although experimental validation is still required.

The energy conversion efficiency can be further improved at the nanoscale using axial or radial (core-shell) heterostructured NWs depending of the application. For instance, GaN NWs with thin AlN axial barriers can increase the mechanical harvesting efficiency, while ZnO (core)/CdTe (Shell) NWs can increase the optical absorption efficiency for photovoltaic applications.

Finally, the integration of several energy conversions into one single device could be a solution to increase the harvested energy density and to build truly autonomous systems working in any ambient condition.

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