Constructive Reversible Logic Synthesis for Boolean Functions with Special Properties

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Abstract. Reversible computation is gaining increasing relevance in the context of several post-CMOS technologies, the most prominent of those being quantum computing. The problem of implementing a given Boolean function using a set of elementary reversible logic gates is known as reversible logic synthesis. Though several generic reversible logic synthesis methods have been proposed so far, yet the scalability and implementation efficiency of these methods pose a difficult challenge. Compared to these generic synthesis methods, few reversible logic synthesis approaches for restricted classes of Boolean functions demonstrated better implementation efficiency and scalability. In this paper, we propose a novel constructive reversible lo[gic](#page-14-0) synthesis technique for Boolean functions with special properties. The proposed techniques are scalable, fast and outperforms state-of-the-art [ge](#page-14-1)neric rever[sib](#page-14-2)le synthesis methods in terms of quantum cost, gate count and the number of lines.

1 Introduction

From thermodynamic principles of computing, Landauer [11] pointed out that for every bit of information lost, $kT \cdot \ln 2$ Joules of heat is generated in an irreversible computation, which is recently verified experimentally [3]. Bennett [2] proposed that the computation can be done in reversible manner to achieve theoretically zero power dissipation by building upon Landauer's observations. This concept helped to form the field of reversible computation, which also dictates that the physical reversibility must be accompanied at higher abstraction by logical reversibility. This is a cornerstone for serveral post-CMOS technologies including quantum computing. Reversible logic synthesis accepts an (in)completely specified reversible Boolean function as input and generates a logical representation of the function, where reversible logic gates are used.

Boolean functions serve as pr[ime](#page-15-0) building block of symmetric-key cryptosystems and error-correcting codes, for which several properties are highly desirable such as nonlinearity, symmetry, correlation immunity and balancedness. The main motivation behind this work is to show that the combinatorial construction of the reversible Boolean functions with specific properties can be done in order to improve the circuit efficiency compared to automated logic synthesis method. In this paper, we focus to two properties namely, *symmetry* and *nonlinearity* of Boolean functions.

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2 Preliminaries

A Boolean function f is of the form $f : \{0,1\}^n \rightarrow \{0,1\}$ (or equivalently f : $\mathbb{V}_2^n \to \mathbb{V}_2$). The output of the Boolean function f can be represented as a string s
of ones and zeros. It can also be represented as a multivariate polynomial over $CF(2)$ of ones and zeros. It can also be represented as a multivariate polynomial over $GF(2)$. This polynomial can be expressed as a exclusive disjunction (EXOR) of a constant a_0 and one or more conjunctions of the function argument. This is called the Exclusive Sum-Of-Product (ESOP) representation. A less general representation of the ESOP form is known as the Algebraic Normal Form (ANF). The general ANF for a function $f(x_1, \ldots, x_n)$ over *n*-variables can be written as,

$$
f(x_1, ..., x_n) = a_0 \oplus a_1 x_1 \oplus \cdots \oplus a_i x_i \oplus \cdots \oplus a_n x_n
$$

$$
\oplus \cdots \oplus a_{1,2,...,n} x_1 x_2 \cdots x_n
$$
 (1)

Reversible and Irreversible Boolean Functions. An *n*-variable vectorial Boolean function is *reversible* if all its output patterns map uniquely to an input pattern and vice-versa. It can be expressed as an n -input, n -output bijection or alternatively, as a Boolean permutation function over the truth value set $\{0, 1, \ldots 2^{n-1}\}\$. An *irreversible* Boolean function $f_{irr}: \{0,1\}^n \to \{0,1\}^m$ with $n \neq m$ can also be made reversible with the help of extra input lines (ancilla) and/or output lines (garbage lines) such that, $input + ancilla = output + garbage.$

Nonlinearity. The nonlinearity of a Boolean function f on *n*-variables, denoted by N_f is the minimal Hamming Distance between f and all the affine functions on \mathbb{V}_2^n .
The class of Boolean functions having the highest poplinearity are known as

The class of Boolean functions having the highest nonlinearity are known as *Bent functions*. They are defined only on $\mathbb{V}_2^{2\bar{k}}$, i.e. Boolean functions of even number of veriables and their poplinearity is given by $2^{2k-1} - 2^{k-1}$. In contrast, the maximum variables and their nonlinearity is given by $2^{2k-1} - 2^{k-1}$. In contrast, the maximum
poplinearity attainable for a Boolean function ∇^{2k+1} with odd number of variables still nonlinearity attainable for a Boolean function \mathbb{V}_2^{2k+1} with odd number of variables still
remains an open problem remains an open problem.

Symmetry. A Boolean function $f : \{0, 1\}^n \to \{0, 1\}$ is called symmetric if its output is invariant under any permutation of its input bits. Equivalently we can say that the value of $f(x)$ is constant for all x's having the same weight.

Direct Sum. The direct sum of two strings x and y, of lengths n and m respectively, de[note](#page-14-3)d b[y](#page-15-1) x $\aleph y$ is given by $x\aleph y = (x \otimes y^c) \oplus (x^c \otimes y)$, where $x \otimes y = (x_0 \text{ AND})$ y)...(x_{n−1} AND y) denotes the Kronecker product of two strings producing a string of length nm. y*^c* denotes complement of y.

Reversible Logic Synthesis. Reversible Boolean logic synthesis is achieved with the help of reversible logic gates. The gates are characterized by their implementation cost in quantum technologies, which is dubbed as Quantum Cost (QC). We use the standard QC values from [13] along with the latest improvements reported in [30] for QC computation. Few prominent reversible logic gates are as following.

- **CNOT gate**: $CNOT(a, b) = (a, a \oplus b).$
- **CCNOT gate (Toffoli gate):** CCNOT $(a, b, c) = (a, b, ab \oplus c)$. This gate can be generalized with $T \circ f_n$ gate, where first $n - 1$ variables are used as control lines. NOT and CNOT gates are denoted as $T \circ f_1$ and $T \circ f_2$ respectively.
- **Controlled Swap gate (Fredkin gate)**: Fred $(a, b, c) = (a, \overline{a}b \oplus ac, \overline{a}c \oplus ab)$. This is generalized with $Fred_n$ gate $(n > 1)$, where [first](#page-15-2) $n - 2$ variables are used as control lines.
- **Peres gate**: $Per(a, b, c) = (a, a \oplus b, ab \oplus c)$. This gate can be generalized with Per_n gate $(n > 2)$ [30], where first $n - 1$ variables are used as control lines.

2.1 Related Work and Motivation

A Boolean function should possess certain properties for its use in cryptographic applications such as symmetry, balancedness and high nonlinearity. Matsui in [17] showed that Boolean functions of low nonlinearity can be approximated and hence can be consequently attacked using linear cryptanalysis attacks, which makes high nonlinearity a desirable property of cryptographically stro[ng](#page-15-3) Boolean function. To this effect, researchers came up with multiple construction methods for highly nonlinear Boolean [f](#page-15-4)unctions with large number of variables. These constructive methods could be adopted for reversible circ[uit](#page-14-4) construction, which has not been attempted before this work. This constructive approach not only provides a scalable reversible logic synthesis method for hi[ghly](#page-15-5) nonlinear Boolean functions but also, demonstrates increased efficiency of implementation compared to generic reversible logic synthesis te[chn](#page-15-6)iques. Symmetry of Boolean functions, while a desirable property for cryptographic applications, has also been shown to be important for general reversible logi[c syn](#page-15-7)thesis [23].

[E](#page-14-5)xisting reversible logic synthesis methods can be broadly classified in two categories - generic [26] and property-specific. In the area of property-specific reversible logi[c sy](#page-15-7)nthesis, Beth and Rötteler [4] suggested synthesis approach for linear reversible circuits using Gaussian Elimination and LU-Decomposition to yield circuits with $O(n^2)$ gates. In [21], an improved algorithm with better speed and asymptotically optimal performance for synthesis of linear reversible circuits is proposed. Younes [34] proposed a factorization algorithm for synthesis [of](#page-14-6) homogeneous Boolean functions. For Symmetric Boolean functions, a synthesis technique is proposed at [15]. This is improved further at [8], where a cascade of Peres gates is utilized to obtain reversible circuits with improved QC.

It has been noted at [15] that the constructive reversible logic synthesis procedures for Boolean functions with special pr[ope](#page-15-8)[rtie](#page-15-4)s are scalable and can outperform, in many cases, the generic synthesis techniques. This forms the key motivation of this work. Besides, it has been shown in a recent work that several Quantum algorithms do require efficient reversible circuits for specific classes of Boolean functions [7]. In this work, we make two contributions. First, we propose a constructive reversible logic synthesis technique for highly nonlinear Boolean functions. Second, we propose a constructive reversible logic synthesis technique for symmetric Boolean functions. For both the cases, we report improved results compared to the current literature.

In contrast to the state-of-the-art synthesis techniques [28,26] for Boolean functions with special propertes, we explore deeper and draw from the classical Boolean function

construction techniques from the literature. *The constructive approach presented in this paper have multiple advantages, e.g., scalability, low synthesis runtime and significant implementation efficiency, as we demonstrate via benchmarking with state-of-the-art generic and property-specific reversible synthesis flows.*

3 Synth[esis](#page-15-9) of Highly Nonlinear Functions

In this section, several construction techniques for highly nonlinear Boolean functions and Bent functions are [disc](#page-15-9)ussed. Those are followed by their reversible circuit synthesis approaches, corresponding theoretical results on the upper bounds of gate count (GC), QC and the total number of lines (L) and comparison with state-of-the-art generic synthesis techniques.

3.1 Construction Method I: [27]

Here, we follow the [co](#page-15-9)ncatenation-based construction of *n*-variable, *m*-resilient Boolean functions. (following Theorem 4,[27]). The idea is to utilize Boolean functions with smaller number of variables to construct a highly nonlinear Boolean function of large variable count. Before the concatenation, *direct sum* function is used. An optimized reversible circuit construction for the direct sum function (denoted as \aleph) is developed for the same. We illustrate with the help of a construction of a 14-variable Boolean function with 2nd order resiliency. The values of k and r , which are defined as two parameters for the construction in [27] are chosen as 6. Following the theorem, we concatenate 4 Boolean functions f_i 's on \mathbb{V}_2^{12} as $f_i = g_i \aleph \lambda_i$, where g_i is maximum
poplinear function on 6-variables. We choose 4 Bent functions on \mathbb{V}^6 which are as folnonlinear function on 6-variables. We choose $\overline{4}$ Bent functions on \mathbb{V}_2^6 which are as following lowing.

$$
g_1 = x_1 x_2 \oplus x_3 x_4 \oplus x_5 x_6, g_2 = x_1 x_2 \oplus x_3 x_4 \oplus x_5 x_6 \oplus x_2, g_3 = x_1 x_2 \oplus x_3 x_4 \oplus x_5 x_6 \oplus x_2 \oplus x_3, g_4 = x_1 x_2 \oplus x_3 x_4 \oplus x_5 x_6 \oplus x_2 \oplus x_3 \oplus x_4
$$
 (2)

The λ_i 's belong to $UL_k(m + 1)$ where, $UL_k(m + 1) = L_k(m + 1) \cup \cdots L_k(k)$ (i.e., $L_k(3)$ ∪ ··· $L_k(6)$) The individual sets $L_k(i)$ denote the set of all k-variable linear Boolean functions which are non-degenerate on exactly j -variables. The choices for the λ_i 's are,

$$
\lambda_1 = L_6(3) = x_7 \oplus x_8 \oplus x_9,\n\lambda_2 = L_6(4) = x_7 \oplus x_8 \oplus x_9 \oplus x_{10},\n\lambda_3 = L_6(5) = x_7 \oplus x_8 \oplus x_9 \oplus x_{10} \oplus x_{11},\n\lambda_4 = L_6(6) = x_7 \oplus x_8 \oplus x_9 \oplus x_{10} \oplus x_{11} \oplus x_{12}
$$
\n(3)

For reversible circuit implementation, constructions of g_i and λ_i s are straightforward. It is noted that, the reversible logic implementation of *direct sum* is nothing but the \oplus operation of the two functions g_i and λ_i . This allows efficient implementation of this method also via ESOP-based approach. However, the constructive approach considerably reduced the QC of the individual functions, resulting in overall improvement (Table 1). In the table, the shaded cells represent equal or improved performance in comparison with state-of-the-art synthesis methods.

Comparison with the state-of-the-art synthesis methods: We compare the proposed synthesis technique with state-of-the-art reversible logic synthesis methods. The functions are represent[ed b](#page-15-10)y the choi[ce o](#page-15-11)[f th](#page-14-7)e paramet[ers -](#page-15-12) n, k, r and m . The nonlinearity of the functions are denoted by N_f and the maximum achievable nonlinearity (in the case of Bent functions) by $nlmax$. It can be observed that, with the proper choice of r and k, the method can easily scale to large Boolean functions. On the other hand, the choice of a large k and/or r , requires one to first synthesize a large Boolean function.

Table 1. Benchmarking Construction Method I

Function			ESOP[20,10] MMD[18] BDD[32] $N_f/nlmax$ $\frac{2KL[36]}{\text{Lines Gates QC}}$ Lines Gates QC Lines Gates QC Lines Gates QC					This work					
	$(14, 6, 6, 1)$ 7836/8028	26				17	157 ¹	14	40	886			-88
	$(14, 6, 6, 2)$ 7836/8028	31		86 238			16 148	14	39	660 l	18		-91
	$(16, 6, 8, 1)$ 31856/32368	- 31	80	208	17	22	262	16		168 5670	20		87
	$(1\overline{6, 8, 6, 2})$ 31344/32368 36			93 241		16	136	16		172 5850	-20		$\overline{0}1$

3.2 Construction Method II: Recursive Construction[22]

A construction method presented in [22] generates large Boolean functions of high nonlinearity and resilience recursively like the previous one. A 10-variable, 4-resilient Boolean function of degree 4 and of nonlinearity 480 is constructed using a 7-variable, 2-resilient Boolean function of degree 4 and nonlinearity 56 as described in Theorem 7 [22]. The 7-variable function is first presented below. Note that this function was again found using a constructive method based on 6-variable functions.

$$
f(x_1,...,x_7) = (1 \oplus x_7)(1 \oplus x_6)h_1() \oplus (1 \oplus x_7)x_6h_2() \oplus (1 \oplus x_6)x_7h_3() \oplus x_6x_7h_4(),
$$
\n(4)

where

 $h_1(x_1,...,x_5) = x_1 \oplus x_2 \oplus x_1x_4 \oplus x_3x_4 \oplus x_2x_5 \oplus x_3x_5 \oplus x_4x_5 \oplus x_1x_4x_5 \oplus x_2x_4x_5 \oplus x_3x_4x_5$ $h_2(x_1,...,x_5) = 1 \oplus x_1 \oplus x_2 \oplus x_4 \oplus x_3x_4 \oplus x_2x_5 \oplus x_3x_5 \oplus x_4x_5 \oplus x_1x_4x_5 \oplus x_2x_4x_5 \oplus x_3x_4x_5$ $h_3(x_1,...,x_5) = x_3 \oplus x_1x_3 \oplus x_1x_2x_3 \oplus x_1x_4 \oplus x_2x_4 \oplus x_1x_2x_4 \oplus x_3x_4 \oplus x_1x_3x_4 \oplus x_5 \oplus x_1x_5$ [⊕] *^x*1*x*2*x*⁵ [⊕] *^x*1*x*3*x*⁵ $h_4(x_1,...,x_5)=1\oplus x_2\oplus x_1x_2\oplus x_1x_2x_3\oplus x_4\oplus x_1x_4\oplus x_1x_2x_4\oplus x_1x_3x_4\oplus x_1x_5\oplus x_2x_5\oplus x_1x_2x_5$ [⊕] *^x*3*x*⁵ [⊕] *^x*1*x*3*x*⁵

(5)

In [22], an n-variable Boolean function F*^d* is defined to be in *desired form* if it follows the construction

$$
F_d = (1 \oplus x_n) f_1 \oplus x_n f_2, \tag{6}
$$

where f_1 and f_2 [are](#page-5-0) $(n - 1)$ -variable functions with their degree being 1 less than F_d . The aforementioned 7-variable function is in *desired form* since, those are constructed recursively using 6-variable functions. Based on the 7-variable function $f(x_1,...,x_7)$, ^a 10-variable, 4-resilient Boolean function of degree 4 and of nonlinearity 480 is construct[ed](#page-5-1) as following. Let $F = x_{n+2} \oplus x_{n+1} \oplus f$ and $G = (1 \oplus x_{n+2} \oplus x_{n+1})f_1 \oplus f$ $(x_{n+2} \oplus x_{n+1})f_2 \oplus x_{n+2} \oplus x_n$. Then the target 10-variable function F_1 of specified properties is constructed as $F_1 = (1 \oplus x_{n+3})F \oplus x_{n+3}G$. The construction of the 10variable function from the 7-variable function can be easily achieved with Toffoli and Fredkin gates, as shown in the Figure 1. The detailed implementation of the constituent functions h_1 , h_2 , h_3 and h_4 are not shown. These functions were synthesized using an ESOP-based flow including common cube sharing.

The proposed synthesis technique is compared with the existing state-of-the-art synthesis techniques in Table 2. It is interesting to note that, even though the recursive construction allows direct implementation via simple reversible gates, none of the synthesis methods had matching QC or gate count that could be achieved from our constructive technique. The additional 6 lines, compared to the MMD method is contributed due to the fact that the constituent functions were synthesized using ESOP, thereby requiring 4 lines for the constituent functions h_1 , h_2 , h_3 and h_4 . Furthermore, 2 were required for 6-variable functions f_1 and f_2 , which were used for constructing $f(x_1,...,x_7)$ as well as for constructing F_1 . The improvement in constructive method is due to the following facts

- **–** The *desired form* of a function directly translates to controlled swap gate
- **–** Recursive construction method is based on basic CNOT gates

Evidently, these properties are not utilized by generic synthesis methods.

Table 2. Comparison of Construction Method II with existing synthesis methods

3.3 Construction Method III: [9]

An early construction method for Bent functions on \mathbb{V}_2^{2k} was originally proposed in [9].
This construction, known as Majorana McFarland construction, has been further gen This construction, known as Maiorana-McFarland construction, has been further generalized in [5]. Numerous developments on Bent function construction followed the basic Maiorana-McFarland technique, such as in [12], authors obtained Bent functions with high resiliency. In this work, we focus on the basic construction as outlined in [9] and [35]. The idea of the construction is to concatenate the linear functions on \mathbb{V}_2^k , thereby generating Bent functio[ns](#page-7-0) on \mathbb{V}_2^{2k} .

$$
f(y,x) = \pi(y) \cdot x \oplus g(y), x, y \in \mathbb{V}_2^k \tag{7}
$$

[w](#page-15-5)here f is the resultant Bent function, π represents a permutation on \mathbb{V}_2^k and g is any
Declare function on \mathbb{V}_k^k . There are $\mathbb{R}^{2^k}(\mathbb{R}^k)$ such Bent functions, where the possible Boolean function on \mathbb{V}_2^k . There are $2^{2^k}(2^k!)$ such Bent functions, where the possible permutations are covered by the factor $(2^k!)$. For our study, we restricted π to all possipermutations are covered by the factor $(2^k!)$. For our study, we restricted π to all possible linear functions, and assumed q to be 0, thereby generating $2^k(2^k!)$ Bent functions. The general implementation is as shown in the Fig. 2.

Mapping to Reversible Circuits and Implementation Cost Determination: The aforementioned construction can be realized by applying psuedo-optimal linear reversible circuit synthesis [21] followed by a set of Fredkin gates. This construction has high L , GC and QC due to the multiplexer type functionality where k lines act as control lines and select one from all possible 2^k linear functions on \mathbb{V}_2^k . This construction method
suffers from scalability issues since with increasing variable count, the number of linsuffers from scalability issues since, with increasing variable count, the number of linear functions increases exponentially.

Comparison with state-of-the-art synthesis methods: The benchmarking results are presented in Tabl[e 3.](#page-8-0) Note that due to the size constraint, the complete functions are not presented for the studied 8-variable Boolean functions. Instead, only the permutation of the 16 linear functions for the sub-space \mathbb{V}_2^4 are given, where $1 \to 0, 2 \to x_1, 3 \to x_2,$
 \ldots 16 $\to x_1 \oplus x_2 \oplus x_3 \oplus x_4$. The total number of lines required remain upper-bounded \cdots , $16 \rightarrow x_1 \oplus x_2 \oplus x_3 \oplus x_4$. The total number of lines required remain upper-bounded by 20, which is due to 4 control inputs, 4 inputs for the linear functions, which are reused as part of the total 16 linear functions. Thereby, the upper bound of lines can be generalized as $k + 2^k$ for a bent function construction on \mathbb{V}_{2k}^k . In this case, however, the line counts could be further reduced by applying algebraic optimization based on the ESOP formulation (see subsection 3.5). In the same manner, it is possible to determine the generalized costs for the linear function generator part. However, the identification of minimum swap count for a given permutation is non-trivial. Thankfully, the construction method as shown in [35] includes the swaps. Except for the count of lines, the constructive method outperformed ESOP and BDD-based methods both in gate count and QC for most of the permutations. We did not benchmark against MMD as it typically reports even higher gate count and QC compared to ESOP and BDD-based methods.

Fig. 2. Construction Method III: Bent Function

Fig. 3. Construction Method IV: Bent Function

Table 3. Benchmarking Construction Method III

Permutation of Linear Functions	Variable ¹	BDD[32]			ESOP[20,10]			This work		
			Lines Gates OC						Lines Gates OC Lines Gates OC	
$\{11, 15, 10, 16, 4, 5, 2, 13, 8, 14, 6, 12, 9, 3, 7, 1\}$	8	22	71	219	9	32	488	18	33	97
$\{7, 14, 5, 13, 1, 16, 6, 3, 10, 12, 9, 2, 4, 11, 8, 15\}$	8	22	68	196	9	35	479	14	30	90
$\{15, 9, 14, 7, 5, 1, 16, 12, 6, 2, 11, 10, 4, 8, 3, 13\}$	8	22	62	174	9	25	353	13	23	71
$\{6, 14, 9, 4, 7, 13, 11, 1, 8, 15, 12, 5, 10, 3, 16, 2\}$	8	22	70	202	9	33	509	19	34	86
$\{11, 13, 16, 15, 8, 7, 2, 14, 10, 5, 4, 9, 3, 12, 1, 6\}$	8	20	62	174	9	36	516	16	35	99
$\{4, 7, 10, 9, 15, 16, 3, 8, 12, 11, 13, 6, 1, 5, 14, 2\}$	8	24	65	169	9	29	461	15	31	87
$\{9, 4, 2, 15, 6, 10, 7, 11, 12, 3, 16, 14, 5, 1, 13, 8\}$	8	22	72	208	9	34	506	15	29	81
$\{16, 9, 10, 7, 15, 4, 5, 12, 2, 1, 6, 13, 11, 8, 14, 3\}$	8	23	68	200	9	33	461	15	30	86
$\{16, 4, 15, 8, 9, 1, 14, 5, 10, 13, 2, 3, 12, 6, 7, 11\}$	8	22	73	201	9	34	490	18	34	98
$\{2, 7, 5, 6, 12, 3, 1, 4, 16, 10, 13, 11, 9, 14, 8, 15\}$	8	22	68	196	9	37	597	16	30	86

3.4 Construction Method IV: [33]

The authors in [33] proposed two theorems for construction of new Bent functions using existing Bent functions. This is particularly interesting for Boolean functions with odd number of variables, where direct construction[s](#page-7-1) [m](#page-7-1)ethods cannot be used [25].

Theorem 1: Let f and g be Boolean functions on \mathbb{V}_2^m and \mathbb{V}_2^n respectively. Then the Boolean function $h: \mathbb{V}^{m+n} \to \mathbb{V}_2$ defined by $h(\mathbf{x}, \mathbf{v}) = f(\mathbf{x}) \oplus g(\mathbf{v})$ is bent iff f and Boolean function $h : \mathbb{V}_2^{m+n} \to \mathbb{V}_2$ defined by $h(\mathbf{x}, \mathbf{y}) = f(\mathbf{x}) \oplus g(\mathbf{y})$ is bent iff f and g are bent.

Theorem 2: If f is a Bent function on \mathbb{V}_2^n , then $f \oplus l$ is a Bent function for any affine function l on \mathbb{V}_2^n function *l* on \mathbb{V}_2^n .

Mapping to Reversible Circuits and Implementation Cost Determination: The basic idea of this construction according to theorem 1 is given by Fig. 3. The second construction method can be achieved similarly by performing a CNOT operation between the Bent function and the linear function. The QC of the resulting circuit using this method of construction is simply the sum of QCs of the constituent functions added

with 1, which is due to the CNOT gate. The total number of lines for the resulting circuit is $L(f_1) + L(f_2) + m + n$, where f_1 denotes a Bent function on *n*-variables and f_2 is a Bent function on m-variables for Theorem 1. Here, an ESOP-based implementation of the constituent Bent functions is assumed. f_2 is a linear function on *n*-variables for Theorem 2 (hence, $m = 0$ for the second construction).

The QC, GC and L for this construction are enlisted in Table 4.

Table 4. Implementation Costs for Construction Method IV

	Gate Count $\left GC(f_1) + GC(f_2) + 1 \right $
	Quantum Cost $ QC(f_1) + QC(f_2) + 1 $
Lines	$L(f_1) + L(f_2) + m + n$

Comparison with state-of-the-art synthesis methods: This simple construction of Bent function is compared with BDD-based and ESOP-based methods, when the final Boolean function is subjected to synthesis. We observed an improved performance in most of the cases. The constructive method is scalable to large number of variables, in contrast to the generic methods. An 1-hour timeout set to the benchmarked synthesis methods failed to return a valid circuit in one case (indicated by '-').

3.5 Post-sy[nth](#page-8-2)esis Optimization

Aforementioned construction techniques show strong algebraic structure and hence there is a wide scope for optimizing the synthesis by using *common cube sharing*. Common cube sharing is a well-studied problem in classical logic synthesis as it helps in minimization of cost and size by identifying the sub-circuits which form the basis for larger functional blocks. This optimization is applied on the Boolean functions obtained following the construction techniques[. T](#page-15-10)he impl[em](#page-15-11)[en](#page-14-7)tation costs of these functions, as presented in the following Table 5, is computed after application of the cube sharing algorithm [20]. Note that, such optimizations are present also for the ESOP-based synthesis flows that we compared against and hence, do not provide any undue advantage to the proposed constructive synthesis flow.

Function			BDD[32]			ESOP[20,10]			This work		
		Variable Lines Gates QC Lines Gates QC Lines Gates QC									
Ĵх	$= x_1 x_2$										
$g_{\rm v}$	$= y_1 y_2 \oplus y_3 y_4 \oplus y_5 y_6$	6	9	11	31			15			15
$h_{\mathbf{x},\mathbf{y}}$	$= f_{\mathbf{x}} \oplus g_{\mathbf{y}}$	8	12	17	45	9	4	20	10		21
Ĵх	$= x_1 x_2 \oplus x_3 x_4$	4	h		19						10
$g_{\rm v}$	$= y_1 y_2 \oplus y_3 y_4 \oplus y_5 y_6 \oplus y_7 y_8 \oplus y_9 y_{10} \oplus y_{11} y_{12}$	12	19	30	78	13	12	88	13	6	30
$h_{\mathbf{x},\mathbf{y}}$	$= f_{\mathbf{x}} \oplus q_{\mathbf{v}}$	16	22	40	92	17	24	112	18	$\mathbf Q$	41
$f_{\bf x}$	$x_1x_2 \oplus x_3x_4 \oplus x_5x_6 \oplus x_7x_8 \oplus x_9x_{10} \oplus x_{11}x_{12}$	16	22	40	92	17	26	214	17	12	44
	$\oplus x_{13}x_{14}\oplus x_{15}x_{16}$										
$g_{\rm v}$	$= y_1 y_2 \oplus y_3 y_4 \oplus y_5 y_6 \oplus y_1 \oplus y_2 \oplus y_6$	6	9	12	28		6	18		6	18
$h_{\mathbf{x},\mathbf{v}}$	$= f_{\mathbf{x}} \oplus g_{\mathbf{y}}$	22							24	19	53

Table 5. Benchmarking Construction Method IV

4 Synthesis of Symmetric Functions

In contrast to nonlinear Bo[olea](#page-15-1)n functions, constructive approach for synthesizing symmetric Boolean functions have been studied in the past [15,8], possibly due to their usage in efficient synthesis of general reversible Boolean functions [23]. Before proceeding further, we present some recent results on generalized Peres gates as well as show how cascaded multi-control Peres gates can be realized with lower Quantum costs.

4.1 Quantum Cost of Cascaded, Generalized Peres Gates

G[en](#page-9-0)eralization of Peres gates is introduced in [30] with the following definition,

$$
Per_n(x_0, x_1, \dots, x_n) = (x_0, x_0 \oplus x_1, x_0 x_1 \oplus x_2, \dots, x_0 x_1 \dots x_{n-1} \oplus x_n), \ n \ge 2
$$
\n(8)

[Su](#page-15-1)ch gates are implemented in an optimized manner with controlled k*th*-root-of-NOT gates. In the following Fig. 4, Per_3 and its corresponding reversible circuit realization is shown. Here, controlled-V, controlled-V⁺ represents controlled k^{th} -root-of-NOT for $k = 2$ and controlled-W, controlled-W⁺ represents the same for $k = 4$. In the lower part of the same Fig. 4 an alternative reversible circuit is presented, which locally reorders the controlled k*th*-root-of-NOT gates. Since the control lines are exclusive, the resultant Boolean function remains the same.

In lemma 1 of [30], the number of elementary gates for Per_n is proved to be n^2 , which is same as its QC since the elementary gates have a QC of 1. We explore this further considering cascaded, generalized Peres gates. The re-ordering of controlled

Fig. 4. Generalized Peres Gate Implementation

k*th*-root-of-NOT gates provides an opportunity to reduce a few adjacent gates. This has been explored in the context of basic Peres gate [19] and for multi-control Toffoli gates [29].

Lemma 1. *Cascading* 2 *Per_n gates require* $n^2 + n$ *gates.*

Proof. From lemma 1 of [30], 2 cascaded Per_n gates require $2n^2$ elementary gates. An *n*-controlled Peres gate, i.e., Per_n consists of three parts. The part in middle implements a Per_{n-1} gate. The first and the last part of the circuit consists of n and $n-1$ controlled Quantum gates respectively. For two adjacent Per_n gates, by re-ordering, $(n - 1)$ controlled Quantum gates can be cancelled out with their corresponding inverses. This leads to a reduction of $2(n - 1)$ elementary gates. Every Per_n contains a Per_{n-1} inside it, which, in the same manner allows a reduction of $2(n-2)$ gates. This continues till there is a Per_2 gate, for which a reduction of $2(n - (n - 1))$ gates are possible. Hence, by summing the reductions, we obtain the elementary gate count as following.

$$
2n2 - \sum_{i=1}^{n-1} 2(n-i)
$$

= 2n² - n(n - 1)
= n² + n

Corollary 1. *Cascading* t *Per_n gates require* $n^2 + (t - 1)n$ *gates.*

Proof. For each pair of Per_n gates, a reduction of $n(n-1)$ is obtained. For t number of [c](#page-11-0)ascaded Per_n gates, the total reduction from a basic tn^2 gate count is $(t-1)n(n-1)$. Hence, the final gate count is,

$$
tn2 - (t - 1)n(n - 1)
$$

= $tn2 - (t - 1)n2 + (t - 1)n$
= $n2 + (t - 1)n$

Evidently, the above results also lead to the QC values as we are only considering gates with 1 QC. An application of the above lemma is shown graphically for 2 cascaded Per_3 gates in Fig. 5. It is clear that by cascading as much as possible Peres gates with same control lines, one can obtain a significant reduction in gate count and QC. In the constructive synthesis of symmetric Boolean functions, this property is exploited.

4.2 Constructive Synthesis for [Sy](#page-12-0)mmetric Functions

Since the symmetric Boolea[n](#page-14-3) [fu](#page-14-3)nctions have unique output for a given Hamming weight of the input *n*-variable Boolean vector \mathbb{V}_2^n , we propose an approach based on two
phases. First, the Hamming weight computation in ($\lfloor \log n \rfloor + 1$) lines followed by phases. First, the Hamming weight computation in $(|\log_2 n| + 1)$ lines followed by an evaluation of the function on those lines. Note that, due to the sharing of one target Hamming weight line with one input line, $(\lfloor \log_2 n \rfloor)$ ancilla lines are needed. The circuit complexity largely depends on the Hamming weight computation, which is done using a ripple-carry adder approach as shown in Fig. 6. This approach is earlier used for Hidden Weighted Bit (HWB) functions in [13]. It can be observed that the Hamming weight computation circuitry is nothing but a series of cascaded, generalized Peres gates. In case of $rd73$, the Hamming weight computation is done with 2 cascaded Per_2

Fig. 5. Cascaded Generalized Peres Gate Implementation

gates and 4 cascaded Per_3 gates, resulting into a total QC of 24. Please note, that to reduce garbage c[ou](#page-14-5)nt, an input line is [re-](#page-15-7)used for storing the LSB of the Hamming weight value. The Hamming weight values directly result into the output. Hence, no further gate is required. In providing the gate count, we report the number of mixed-control Tof_n gates for ease of comparison with previous results.

	Function I/O			$[8]$ (Low Garbage) $[8]$ (Low QC)			[15]			This work	
			Garbage	ОC	Garbage QC Garbage Gates QC Garbage Gates QC						
	2of5	5/1		$\overline{}$			12	32	O		
	rd53	5/3		28		20	12	36	4^*	10	18
	rd73	7/3	┑	46	10	32	20	64	6^*	16	24
	rd84	8/4		66	13	44	28	98	7	20	27
	6sym	6/1					20	62	8	16	32
	9sym	9/1	14	88	19	59	28	94	10	22	30

Table 6. Benchmarking with Property-specific Synthesis Techniques

The computation of Hamming weight is further optimized by taking the desired output into consideration. For example, the benchmark function $2of5$ produces an output of 1 when the Hamming weight is 2 or 010. However, 110 is not a valid Hamming weight for 5-variable circuit. Therefore, the Hamming weight computation can optimize the carry propagation circuitry and an additional line used for the most significant

Constructive Reversible Log

Fig. 6. Generation of Hamming Weight for *rd*73 **Fig. 7.** Reversible Ciruit: 2*of*5

bit. Similarly for $rd84$, the Per_4 gate can be avoided by putting an inverted-control Toffoli gate at the end, which sets the output line indicating Hamming weight of 1000 to true if none of the les[s H](#page-11-1)am[m](#page-14-5)ing weight values are true. This allows cascading of 5 Per_3 gates. For $9sym$, computing the final two Hamming weights 1000 and 1001 can be avoided, since those do not influence the output. Neither of the Hamming weight values influencing the output, i.e. 3, 4, 5 a[nd](#page-14-3) 6, has any overlapping bit-pattern in the 3 least significant bits. The complete reversible circuit for $2of5$ is shown in Fig. 7.

Comparison with state-of-the-art synthesis methods: This construction technique easily outperforms both the previous property-specific synthesis flows for symmetric functions in *all the efficiency metrics* as shown in Table 6. In [8], a cascade of 2-control Peres gates are used followed by an extraction-elimination module. In contrast, we do not require any follow-up module and obtain the individual Hamming weight values directly. The values with [∗] in the garbage count are shown to be minimal [13]. Further, it is likely that any approach based on adder circuit and generalized Peres gates may benefit from the result[s pr](#page-15-1)esented in this paper.

4.3 Upper Bounds of Symmetric Functions

In this subsection, we establish novel upper bounds for the gate count and QC for symmetric Boolean fu[nctio](#page-15-17)ns based on the proposed constructive approach. To the best of our knowledge, no such upper bound for symmetric Boolean functions exist.

Based on a recent result [30], we have an expression of the QC of Tof_n gate as following.

$$
2(n-1)^2 - 2(n-1) + 1 \tag{9}
$$

While this result is for positive-control Tof_n gates, we use it also for mixed-polarity Tof_n gates. It has been showed in the case of mixed-polarity Tof_n gates, a realization with equivalent QC can be obtained [16]. The only case, where the QC for mixedpolarity is higher, is when all the control inputs are negated. In that case, the QC is

$$
2(n-1)^2 - 2(n-1) + 3\tag{10}
$$

Using the proposed constructive approach, we explore the following upper bound calculation based on the circuit for Hamming weight computation using cascaded Per_n gates.

Lemma 2. *The upper bound of QC for an* n*-variable Hamming weight computation circuit is* $(\lfloor \log_2 n \rfloor)^2 + n(\lfloor \log_2 n \rfloor) + n - 1$.

Proof. For an *n*-variable Boolean function, the Hamming weight computation requires $(n-1)$ cascaded Per_k gates, where the maximum value of k can be $\log_2 n + 1$. Considering the worst-case scenario, total $(n-1)$ cascaded $Per_{\lfloor \log_2 n \rfloor + 1}$ gates are needed. By using the result from Corollary 1, the upper bound on QC is $(\log_2 n + 1)^2 + (n 2)(\lfloor \log_2 n \rfloor + 1)$. Simplification of this leads to the result. \Box

Theorem 1. *The upper bound of QC for an* n*-variable Symmetric Boolean function is* $(2n+1)(\lfloor \log_2 n \rfloor)^2 - n(\lfloor \log_2 n \rfloor) + 4n - 1.$

Proof. The computation of Symmetric function is composed of Hamming weight calculation followed by a set of comparators. Each comparator is due to one Hamming weight value. There can be $(n+1)$ different Hamming weights for an *n*-variable Boolean function. However, at most n H[am](#page-13-0)ming weights can contribute to the generation of the Symmetric function, as otherwise, it will become a co[ns](#page-14-9)tant function. The Hamming weights are stored in $(\log_2 n + 1)$ lines. Each comparator for a specific Hamming weight value require a mixed-polarity $T \circ f_k$ gate, where k is at most $(\lfloor \log_2 n \rfloor + 1)$ $(\lfloor \log_2 n \rfloor + 1)$. This leads to the worst-case QC value from the comparator circui[t a](#page-13-0)s $n(2(\lfloor \log_2 n \rfloor)^2 - 2(\lfloor \log_2 n \rfloor) + 3)$. By adding the upper bound of QC from the Hamming weight circuit with the comparator circuit, we obtain the result. Ч

Clearly, the upper bound derived in Theorem 1 based on the constructive approach is tighter compared to the generic upper bounds presented recently in [1].

It can be also noted that the QC values obtained for benchmark circuits, presented in Table 6 is significantly less than the upper bound presented in Theorem 1. To predict a tighter bound of QC for individual circuits compared to theorem 1, we need to enumerate the number of $Per_1, Per_2 \cdots Per_{\lfloor \log_2 n \rfloor + 1}$ gates, which follows a piecewise function. Let us define the number of Per_k gates for an *n*-variable Hamming weight computation circuit as $C_n(Per_k)$. It can be easily shown that,

$$
C_n(Per_k) = \begin{cases} 0 & \text{if } n < 2^{k-1} \\ (n+1) - 2^{\lfloor \log_2 n \rfloor} & \text{if } 2^{k-1} \le n \le 2^k - 1 \\ 2^{k-1} & \text{if } n \ge 2^k \end{cases}
$$

5 Summary and Future Work

In this paper, a novel, constuctive reversible logic synthesis method is presented for Boolean functions with special properties. It has been shown that this synthesis methods outperforms state-of-the-art, general reversible logic synthesis methods. Detailed experimental studies are presented to support the claim.

Due to the desirability of Boolean functions with specific properties, new constructions are continuously being proposed. The presented techniques can be extended to cover further Boolean function construction methods. The interdependence between the Boolean function properties and the implementation efficiency is an interesting open research problem. Further, we will like to explore the usage of efficient reversible circuits for symmetric Boolean functions in the context of reversible logic synthesis and adder circuit realizations.

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