Stability Analysis of Continuous Time Sigma Delta Modulators

Kyung Kang and Peter Stubberud

1 Introduction

Many electronic systems, including instrumentation, signal processing systems and portable communication systems, digitize analog signals using analog to digital converters (ADCs). Both continuous time (CT) and discrete time (DT) sigma delta modulator (ΣΔM) ADCs are often used for such applications because they use relatively simple, low power, analog circuitry and a low order quantizer in a feedback loop to achieve high speed, high resolution and low power signal conversion. Although CT ΣΔMs and DT ΣΔMs have many similarities such as the ability to increase their resolution by increasing their quantizer's sampling rate, increasing the number of bits in their ΣΔM's quantizers and increasing the orders of their loop filters, CT ΣΔMs have some advantages which include having inherent antialiasing filtering in the CT ΣΔM's signal transfer function (STF) and operating at higher frequencies than DT ΣΔMs because CT ΣΔMs don't have settling time requirements in their loop filters [1]; however, because DT ΣΔMs are entirely implemented using discrete time, or clocked, components while CT ΣΔMs are implemented using both analog and discrete components, DT ΣΔMs are simpler to analyze and simulate than CT ΣΔMs. Stability analysis in particular is more difficult to perform for CT ΣΔMs than it is for DT ΣΔMs.

Because a ΣΔM's output is typically the output of the ΣΔM's quantizer, ΣΔMs cannot be unstable in the bounded input bounded output (BIBO) sense. Instead, a ΣΔM is considered to have become unstable when the amplitude of a ΣΔM's input is increased over a value which causes the ΣΔM's output signal to quantization noise ratio (SQNR) to decrease dramatically and the ΣΔM's output SQNR cannot be restored to its previous values even when the ΣΔM's input is decreased to its previous amplitudes. Other phenomenon, such as input overload, can also cause a ΣΔM's output SQNR to decreased dramatically when the ΣΔM's input is increased over a certain value; however, in these cases, the ΣΔM's output SQNR can be restored to its previous values when the ΣΔM's input is decreased to its previous amplitudes.

In a general, a CT ΣΔM can be modeled by the canonical feedback loop shown in Fig. 1 where $X(s)$ and $Y(s)$ are the Laplace transforms of the input signal and the output signal, respectively, and $F(s)$, $G(s)$ and $H(s)$ are the system functions of the pre-filter stage, the feedforward path and the feedback path, respectively. The quantizer block represents a clocked quantizer, and the DAC block represents a digital to analog converter (DAC). The quantizer delay and DAC delay are often represented by a single delay block as they are in Fig. 1, and the combination of these two delays is often referred to as the excess loop delay.

Fig. 2 shows a linear model of the CT ΣΔM shown in Fig. 1 where the quantizer has been modeled by a variable gain, K, for the ΣΔM's STF, $Y(s)/X(s)$, and by an additive quantization noise, $E(s)$ for the ΣΔM's noise transfer function (NTF), $Y(s)/E(s)$. The ΣΔM's STF can be written as

$$STF(s) = \frac{K \cdot F(s) \cdot G(s)}{1 + K \cdot e^{-sD} \cdot G(s) \cdot H(s) \cdot DAC(s)} \quad (1)$$

and the ΣΔM's NTF can be written as

$$NTF(s) = \frac{1}{1 + e^{-sD} \cdot G(s) \cdot H(s) \cdot DAC(s)} \quad (2)$$

where the exponential function, e^{-sD} is the Laplace transform of the excess loop delay, D. Although the DAC is not explicitly modeled, a typical zero order hold (ZOH) DAC would have the system function

K. Kang (✉) • P. Stubberud
Department of Electrical and Computer Engineering, University of Nevada, Las Vegas, USA
e-mail: kangk3@unlv.nevada.edu; peter.stubberud@unlv.edu

H. Selvaraj et al. (eds.), *Progress in Systems Engineering: Proceedings of the Twenty-Third International Conference on Systems Engineering*, Advances in Intelligent Systems and Computing 1089,
DOI 10.1007/978-3-319-08422-0_71, © Springer International Publishing Switzerland 2015

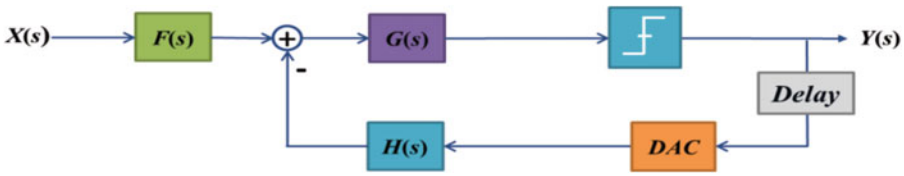

Fig. 1 The canonical form of the feedback system

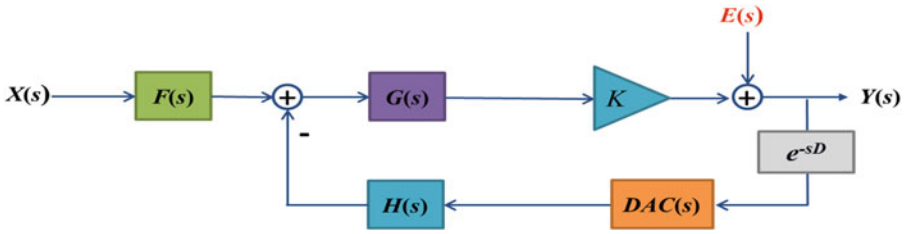

Fig. 2 A linear model of the CT ΣΔM

$$DAC(s) = \frac{1 - e^{-sT}}{sT} \tag{3}$$

where T is the ΣΔM's sampling period. Most other DACs are also typically modeled using exponential functions.

Root locus methods have been successfully used to determine the stability of DT ΣΔMs; however, because the denominator terms of both the STF and NTF contain exponential functions, traditional root locus methods cannot be used for determining the stability of CT ΣΔMs. Instead, several other methods have been developed for predicting the stability of CT ΣΔMs. One such method models the nonlinear quantizer using two linear gains, one for the signal gain and one for quantization noise gain [2]. This approach has not received much attention because of its complexity and because it cannot predict stability for several classes of ΣΔMs. Other approaches predict CT ΣΔM stability by assuming that the ΣΔM's has a DC input and then by performing a simple stability analysis. These methods are effective for predicting stability for lower order ΣΔMs but not for higher order ΣΔMs [3–9]. Another method attempts to determine ΣΔM's stability by using a one-norm of the ΣΔM's NTF to determine stability in a BIBO sense. It has been shown that the one-norm condition is available only for second order lowpass modulators [10]. Therefore, a mixture of one-norm, two-norm and infinity-norm constraints have been proposed to predict the stability of higher order modulators [11]. Lee's rule is another method used to determine the stability of ΣΔMs [12]. Lee's rule states that a ΣΔM will be stable if the gain of the ΣΔM's NTF is less than two for all frequencies. It has been shown that Lee's rule is neither a necessary nor a sufficient condition to ensure stability in ΣΔMs [13].

In this paper, an analytical root locus method is used to determine the stability criteria for CT ΣΔMs that include exponential functions in their characteristic equations. This root locus method determines the range of quantizer gains for which a CT ΣΔM is stable. These values can then be used to determine input signal and internal signal ranges that prevent ΣΔM from becoming unstable. A circuit designer can then take measures to prevent the ΣΔM from becoming unstable. Examples of 3rd order CT ΣΔMs illustrate this method.

2 ΣΔM Stability Analysis using an Analytical Root Locus Method

Root locus analysis is a method for examining how the poles of a system change as function of a certain system parameter. This method is commonly used to determine the stable region of feedback systems as a function of open loop gain by plotting the poles of the system's closed loop transfer function as a function of the system's open loop gain. As shown in (1), CT ΣΔMs typically have characteristic equations of the form

$$1 + K \cdot e^{-sD} \cdot G(s) \cdot H(s) \cdot DAC(s) = 0 \tag{4}$$

where D is the ΣΔM's excess loop delay and $DAC(s)$ contains at least one exponential function.

When $D = 0$ and $DAC(s) = 1$, root locus analysis of the characteristic equation in (4) can be performed using standard graphical analysis methods [14] or using an analytical method [15,16]. When $D \neq 0$ and $DAC(s)$ contains at least one exponential function, root locus analysis of the

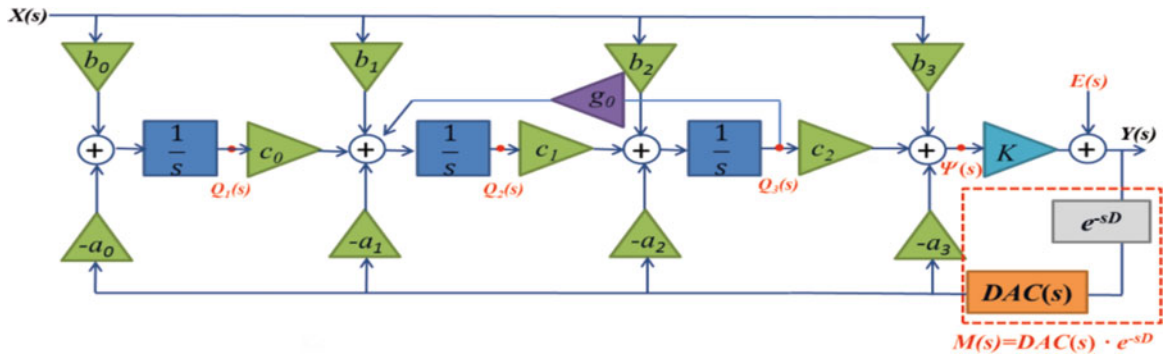

Fig. 3 3rd order low pass CT ΣΔ block diagram

characteristic equation in (4) can be performed using an extended graphical analysis method [17–19] or using the analytical method in [20]. In this paper, the analytical method in [20] is used to determine the quantizer gains that allow CT ΣΔM to remain stable.

To illustrate this method, the term $e^{-sD}\cdot G(s)\cdot H(s)\cdot DAC(s)$ in (4) is written as

$$e^{-sD}\cdot G(s)\cdot H(s)\cdot DAC(s)=\frac{N(s)}{D(s)} \tag{5}$$

which implies that (4) can be written as

$$D(s)+K\cdot N(s)=0\,. \tag{6}$$

Solving (6) for K,

$$K=-\frac{D(s)}{N(s)}=-\frac{\mathrm{Re}\{D(s)\}+j\mathrm{Im}\{D(s)\}}{\mathrm{Re}\{N(s)\}+j\mathrm{Im}\{N(s)\}}\,. \tag{7}$$

In standard form, (7) can be written as

$$K=\frac{-\mathrm{Re}\{D(s)\}\cdot\mathrm{Re}\{N(s)\}-\mathrm{Im}\{D(s)\}\cdot\mathrm{Im}\{N(s)\}}{(\mathrm{Re}\{N(s)\})^2+(\mathrm{Im}\{N(s)\})^2} +j\frac{\mathrm{Re}\{D(s)\}\cdot\mathrm{Im}\{N(s)\}-\mathrm{Im}\{D(s)\}\cdot\mathrm{Re}\{N(s)\}}{(\mathrm{Re}\{N(s)\})^2+(\mathrm{Im}\{N(s)\})^2} \tag{8}$$

Because the quantizer's variable gain, K, is real, (8) implies that

$$K=\frac{-\mathrm{Re}\{D(s)\}\cdot\mathrm{Re}\{N(s)\}-\mathrm{Im}\{D(s)\}\cdot\mathrm{Im}\{N(s)\}}{(\mathrm{Re}\{N(s)\})^2+(\mathrm{Im}\{N(s)\})^2} \tag{9}$$

and that

$$\mathrm{Re}\{D(s)\}\cdot\mathrm{Im}\{N(s)\}-\mathrm{Im}\{D(s)\}\cdot\mathrm{Re}\{N(s)\}=0\,. \tag{10}$$

Plotting (10) in the s-plane renders the root locus of (4) for $-\infty<K<\infty$.

3 Examples

ΣΔMs achieve high resolution by using a feedback loop to attenuate quantization noise in the frequency band of interest while passing the input signal to the output. Because of the importance of attenuating the quantization noise over the frequency band of interest, the ΣΔM's NTF is designed before the STF. After determining an NTF and STF, the NTF and STF coefficients need to be implemented in a hardware structure, such as a cascade of resonators feedback (CRFB), cascade of resonators feedforward (CRFF), cascade of integrator feedback (CIFB), and cascade of integrator feedforward (CIFF) implementations. In the following example, 3rd order Chebyshev Type 2 NTFs are implemented using a CIFB implementation.

Fig. 3 shows the linear model of a 3rd order lowpass CT ΣΔM using a CIFB implementation. In Fig. 3, the signals, $X(s)$, $E(s)$ and $Y(s)$, are the Laplace transforms of the input signal, the quantization noise signal and the output signal, respectively. The quantizer has been modeled by a variable gain, K, an additive quantization noise, $E(s)$, and a delay. The DAC block represents a digital to analog converter (DAC), and the excess loop delay is represented by the *Delay* block as it is in Fig. 2. The blocks with the symbols, a_0, a_1, a_2, a_3, b_0, b_1, b_2, b_3, c_0, c_1, c_2 and g_0 represent scalar multiplication with gains associated by the blocks' respective symbols.

The STF and NTF of the ΣΔM shown in Fig. 3 can be calculated from the block diagram by calculating the states and the output as

$$Q_1(s)=\{b_0X(s)-a_0\cdot M(s)\cdot Y(s)\}\frac{1}{s} \tag{11}$$

$$Q_2(s)=\{b_1X(s)-a_1\cdot M(s)\cdot Y(s)+c_0Q_1(s)+g_0Q_3(s)\}\frac{1}{s} \tag{12}$$

$$Q_3(s)=\{b_2X(s)-a_2\cdot M(s)\cdot Y(s)+c_1Q_2(s)\}\frac{1}{s} \tag{13}$$

$$\Psi(s) = b_3X(s) - a_3 \cdot M(s) \cdot Y(s) + c_2Q_3(s) \tag{14}$$

$$Y(s) = K \cdot \Psi(s) + E(s) \tag{15}$$

where $M(s)=DAC(s)\cdot e^{-sD}$. Substituting (11) into (12), (12) into (13), (13) into (1414) and (14) into (15), the STF and the NTF can be written as

$$STF(s) = \frac{\frac{K\cdot\left\{b_3s^3+b_2c_2s^2+(b_1c_1c_2-g_0b_3c_1)s+b_0c_0c_1c_2\right\}}{s(s^2-g_0c_1)}}{1 + \frac{K\cdot M(s)\cdot\left\{a_3s^3+a_2c_2s^2+(a_1c_1c_2-g_0a_3c_1)s+a_0c_0c_1c_2\right\}}{s(s^2-g_0c_1)}} \tag{16}$$

and

$$NTF(s) = \frac{1}{1 + \frac{M(s)\cdot\left\{a_3s^3+a_2c_2s^2+(a_1c_1c_2-g_0a_3c_1)s+a_0c_0c_1c_2\right\}}{s(s^2-g_0c_1)}} \cdot \tag{17}$$

Comparing (1) with (16) and (2) with (17), it can be seen that

$$F(s) = b_3s^3 + b_2c_2s + (b_1c_1c_2 - g_0b_3c_1)s + b_0c_0c_1c_2 \tag{18}$$

$$G(s) = \frac{1}{s(s^2 - g_0c_1)} \tag{19}$$

$$H(s) = a_3s^3 + a_2c_2s^2 + (a_1c_1c_2 - g_0a_3c_1)s + a_0c_0c_1c_2\ . \tag{20}$$

Assuming that the DAC is implemented using a ZOH, $DAC(s)$ can be written as shown in (3). The gains, a_0, a_1, a_2, a_3, b_0, b_1, b_2, b_3, c_0, c_1, c_2 and g_0 can be determined by equating the STF coefficients in (16) and the NTF coefficients in (17) with the desired STF and NTF coefficients, respectively. For example, if the NTF is a high pass Chebyshev Type 2 filter and the STF has a lowpass characteristic, then the rational function describing the Chebyshev Type 2 filter is set equal to the rational NTF in (17) and the rational function describing the lowpass STF is set equal to the rational STF in (16).

Using (5), (19), (20) and (3), $N(s)$ and $D(s)$ can be determined to be

$$N(s) = \left\{a_3s^3 + a_2c_2s^2 + (a_1c_1c_2 - g_0a_3c_1)s + a_0c_0c_1c_2\right\} \cdot \left(1 - e^{-sT}\right) \cdot e^{-sD} \tag{21}$$

and

$$D(s) = \left(s^2 - g_0c_1\right) \cdot s^2 \cdot T\ . \tag{22}$$

Substituting $\sigma + j\omega$ for s where $\sigma = \mathrm{Re}\{s\}$ and $\omega = \mathrm{Im}\{s\}$,

$$\mathrm{Re}\{D(s)\} = T \cdot \sigma\left(\sigma^3 + a\sigma - 3\sigma\omega^2\right) - T \cdot \omega\left(-\omega^3 + a\omega + 3\sigma^2\omega\right) \tag{23}$$

$$\mathrm{Im}\{D(s)\} = T \cdot \omega\left(\sigma^3 + a\sigma - 3\sigma\omega^2\right) + T \cdot \sigma\left(-\omega^3 + a\omega + 3\sigma^2\omega\right) \tag{24}$$

$$\mathrm{Re}\{N(s)\} = (b\sigma^2 - b\omega^2 + c\sigma + d)\left\{e^{-D\sigma}\cos(D\omega) - e^{-(T+D)\sigma}\cos((T+D)\omega)\right\} - (2b\sigma\omega + c\omega)\left\{-e^{-D\sigma}\sin(D\omega) + e^{-(T+D)\sigma}\sin((T+D)\omega)\right\} \tag{25}$$

and

$$\mathrm{Im}\{N(s)\} = (b\sigma^2 - b\omega^2 + c\sigma + d)\left\{-e^{-D\sigma}\sin(D\omega) + e^{-(T+D)\sigma}\sin((T+D)\omega)\right\} + (2b\sigma\omega + c\omega)\left\{e^{-D\sigma}\cos(D\omega) - e^{-(T+D)\sigma}\cos((T+D)\omega)\right\}\ . \tag{26}$$

Substituting (23), (24), (25) and (26) into (10), the root locus of the 3rd order CT ΣΔM shown in Fig. 3 can be plotted for $-\infty < K < \infty$.

Fig. 4 (*a*), (*b*) and (*c*) show the plot of (10), or the root locus, for 3rd order CT ΣΔMs with a sampling frequency, f_s where $f_s=1/T$, of 1GHz and Chebyshev Type 2 NTF with 47dB, 37dB, and 30dB attenuation in the stopband for $D = 0$, $D = T/2$, and $D = T$, respectively. The plots in Fig. 4 include both the positive gain ($K > 0$) root locus and the negative gain ($K < 0$) root locus. According to the plots, the CT ΣΔMs with $D = 0$, $D = T/2$, and $D = T$ are stable for $0.326 < K < 3.734$, $0.359 < K < 2.001$, and $0.376 < K < 1.648$, respectively. Although the root locus plots show that the CT ΣΔMs with $D = 0$, $D = T/2$, and $D = T$ are unstable for $K > 3.734$, $K > 2.001$, and $K > 1.648$, respectively, none of the modulators show a degradation in SQNR when K enters those ranges because when the modulator enters unstable regions for large values of quantizer gain, K, the feedback signal increases which reduces the quantizer gain, K, and moves the poles back into a stable region. However, when $K < 0.326$, $K < 0.359$, and $K < 0.376$ for the CT ΣΔMs with $D = 0$, $D = T/2$, and $D = T$, respectively, the modulator shows a degradation in SQNR because when the modulator enters those unstable regions the feedback signal increases which further reduces the quantizer gain, K, and consequently moves the poles further from the stable region. Therefore, a CT ΣΔM will remain stable if its quantizer gain, K, remains above its minimum value, $K_{\min}$, as determined from its CT ΣΔMs root locus plot.

Using this stability criterion, the maximum quantizer input, $\psi_{\max}$, that prevents the modulator from becoming

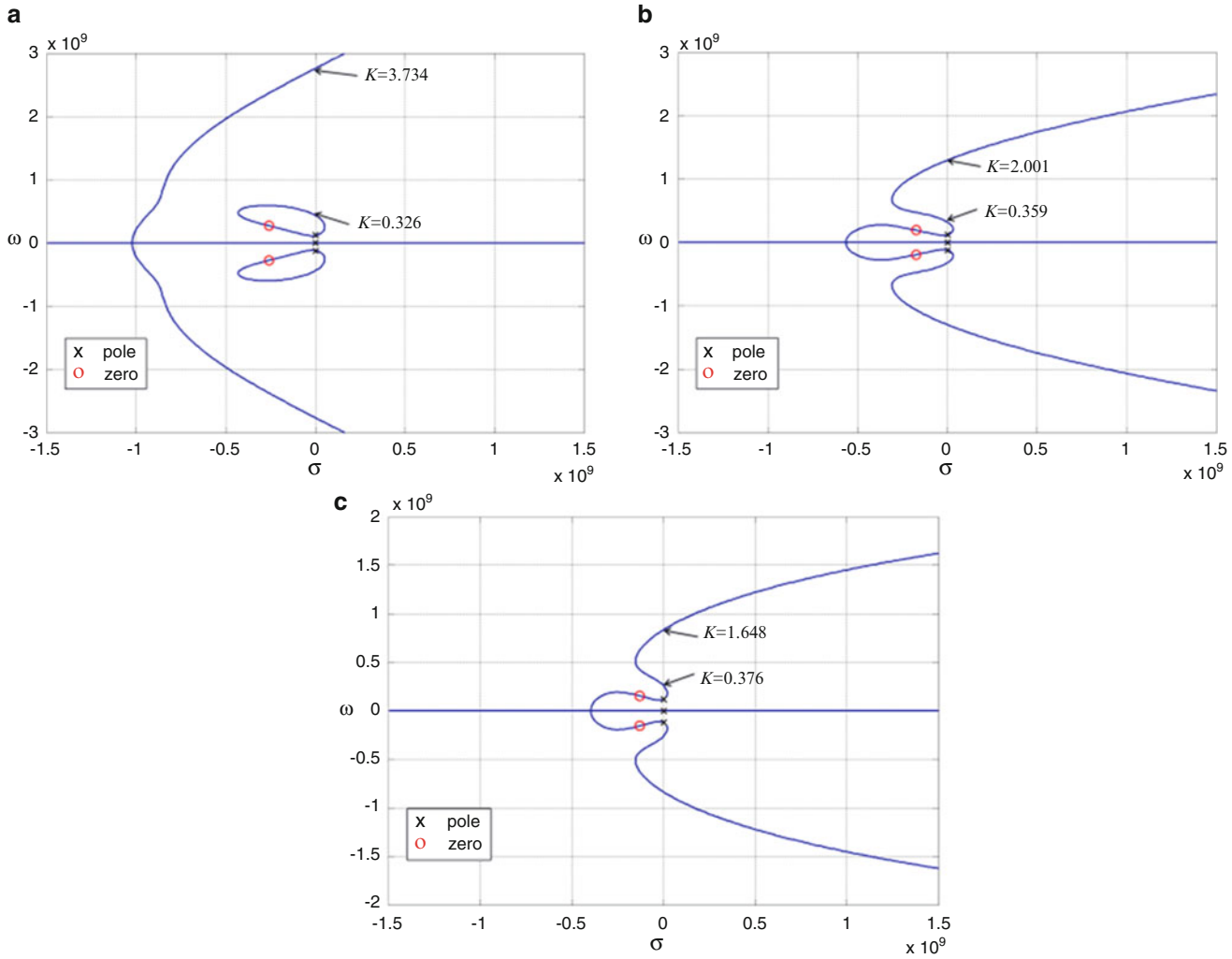

Fig. 4 The root locus of 3rd order CT ΣΔMs that uses Chebyshev Type 2 NTFs and a sampling frequency of 1GHz for (*a*) $D = 0$ (*b*) $D = T/2$ (*c*) $D = T$.

unstable is $1/K_{\min}$. Therefore, the CT ΣΔMs with $D = 0, D = T/2$, and $D = T$ are unstable when $\psi_{\max} > 3.07$, $\psi_{\max} > 2.78$, and $\psi_{\max} > 2.66$, respectively.

Assuming that the ΣΔM's input, output and quantization noise signals have means of zero, the maximum power, σ^2_x, of the ΣΔM's input signal can be calculated from

$$\sigma_y^2 = \sigma_x^2 \int_{-fs/2}^{fs/2} |STF(f)|^2 df + \frac{\sigma_e^2}{f_s} \int_{-fs/2}^{fs/2} |NTF(f)|^2 df \quad (27)$$

where σ^2_e is the quantization noise power when the maximum input signal power is applied to the input and σ^2_y is the output signal power which equals one. If the input signal is sinusoidal, then $\sigma^2_x = x_{\max}{}^2/2$ where $x_{\max}$ is the ΣΔM's maximum input amplitude. Assuming a sinusoidal input, the maximum input values are 0.432 (-7.2 dB), 0.447 (-7.0 dB), and 0.376 (-8.5 dB) for the CT ΣΔMs with $D = 0, D = T/2$, and $D = T$, respectively.

All three CT ΣΔMs were simulated using the method described in [21]. Fig. 5(*a*) shows SQNR and the minimum gain, $K_{\min}$, as a function of input signal amplitude for the ΣΔMs with $D = 0$. As shown in the Fig. 5(a), the ΣΔM's SQNR increases linearly until the input signal's amplitude is less than -8 dB, or $K_{\min} = 0.391$. As the input signal's amplitude is increased above -8 dB, the ΣΔM's SQNR no longer increases linearly. As the input signal's amplitude is increased above -6 dB, the ΣΔM's SQNR degrades dramatically and the ΣΔM's SQNR cannot be restored to its previous values even when the ΣΔM's input is decreased to its previous amplitudes. Fig. 5 (*b*) and (*c*) show the SQNR and the minimum gain, $K_{\min}$, as a function of input signal amplitude for the ΣΔMs with $D = T/2$ and $D = T$, respectively. From Fig. 5 (*b*), when the input signal's amplitude is increased above -7 dB, or $K_{\min}$ is less than 0.359, the ΣΔM's SQNR begins to degrade. Similarly, the ΣΔM's SQNR with $D =$

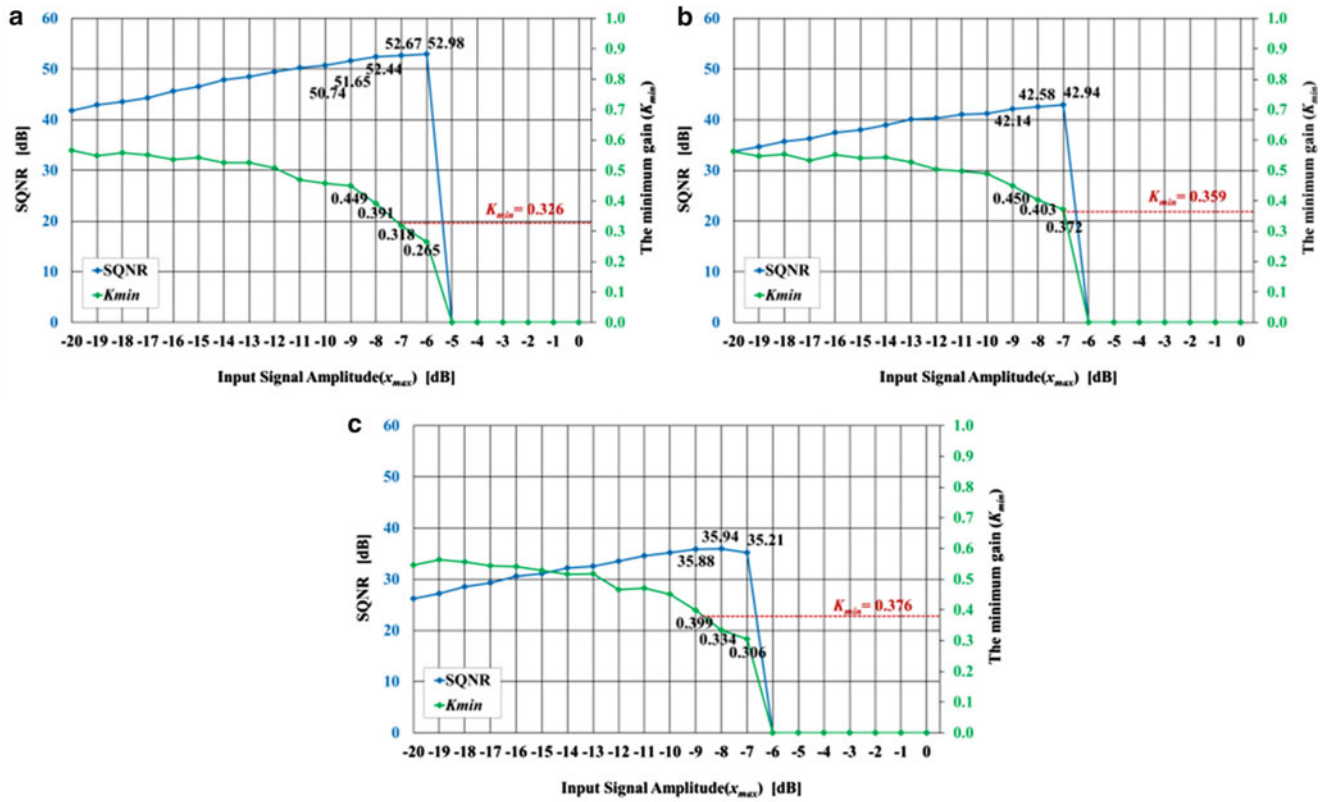

Fig. 5 Simulated SQNR and the minimum gain ($K_{\min}$) for the 3rd order CT ΣΔM for (*a*) $D = 0$ (*b*) $D = T/2$ (*c*) $D = T$

T is degraded when the ΣΔM's input is greater than -9 dB, or $K_{\min}$ is less than 0.376 as shown in Fig. 5 (*c*).

4 Conclusion

In this paper, an analytical root locus method was used to determine the minimum quantizer gains that keep a CT ΣΔM stable. It was then shown how to use the minimum quantizer gain to determine the maximum quantizer input amplitude and ΣΔM maximum input amplitude value that prevent ΣΔM from becoming unstable. Using these values, a circuit designer can then take measures to prevent the ΣΔM from becoming unstable. Examples of 3rd order CT ΣΔM illustrate this method.

References

1. J. A. Cherry and W. M. Snelgrove.: Continuous-Time Delta-Sigma Modulators for High Speed A/D Conversion Theory, Practice and Fundamental Performance Limits: Kluwer Academic, New York, NY, USA (2002)
2. S. H. Ardalan, and J.J. Paulos.: An analysis of non-linear behaviour in Σ-Δ modulators. In: IEEE Trans. on Circuits and Syst., vol. CAS-34, no. 6, pp.1157-1162 (1987)
3. N. Wong, and N.G. Tung-Sang.: DC stability analysis of higher-order, lowpass sigma-delta modulators with distinct unit circle NTF zeroes. In: IEEE Trans. on Circuits & Syst.-II, vol. 50, issue 1, pp. 12-30 (2003)
4. J. Zhang, P.V. Brennan, D. Juang, D, E. Vinogradova, and P.D. Smith.: Stable analysis of a sigma-delta modulator. In: Proc. IEEE Int. Symp. Circuits Syst., vol.1, pp.1-961-1-964 (2003)
5. P, Steiner, and W. Yang.: Stability analysis of the second-order sigma-delta modulator. In: Proc. IEEE Int. Symp. Circuits Syst., vol. 5, pp. 365-368 (1994)
6. J. Zhang, P.V. Brennan, D. Juang, E. Vinogradova, and P.D. Smith.: Stable boundaries of a 2nd-order sigma-delta modulator. In: Proc. South. Symp.Mixed Signal Design (2003)
7. N. A. Fraser, and B. Nowrouzian.: A novel technique to estimate the statistical properties of sigma-delta A/D converters for the investigation of DC stability. In: Proc. IEEE Int. Symp. Circuits Syst., vol.3, pp.111-289-111-292 (2002)
8. D. Reefman, J.D. Reiss, E. Janssen, and M.B. Sandler.: Description of limit cycles in sigma-delta modulators. In: IEEE Trans. on Circuits and Syst-I., vol. 52, issue 6, pp.1211 – 1223 (2005)
9. S. Hein, and A. Zakhor.: On the stability of sigma-delta modulators. In: IEEE Trans. on Signal Processing, vol. 41, no.7, pp. 2322-2348 (1993)
10. 10 R. Schreier and W. M. Snelgrove.: Bandpass Sigma-Delta modulator. In: Electronics letters, vol. 25, no. 23, pp. 1560-1561 (1989)
11. Lars Risbo.: FPGA Based 32 Times Oversampling 8th-order Sigma-Delta Audio DAC. In: Proc. 96th AES Convention, Preprint # 3808 (1994)
12. W. L. Lee and C. G. Sodini.: A topology for higher interpolative coders. In: Proceedings of ISCAS, pp. 459-462 (1987)

13. R. Schreier and G.C. Temes.: Understanding delta sigma data converters: Wiley-IEEE express (2004)
14. John, B.: Essentials of control techniques and theory, CRC pressInc (2009)
15. Bendrukov,G.A, Teodorchik,K,F: The analytic theory of constructing root loci. In: automation and remote control, vol. 20, pp. 340-344 (1959)
16. Cogan,B.:Use of the analytic method and computer algebra to plot root loci. In: International journal of electrical engineering education. vol. 35, pp. 350-356 (1998)
17. D'azzo, J.J, Houpis, C.H.: Linear control system analysis and design conventional and modern, Mc Graw Hill, New York (1988)
18. Ogata, K.: Modern control engineering, Prentice Hall (2002)
19. Palm,W.J.:Control system engineering, John Wiley & Sons (1986)
20. Cogan.B, Paor.A.M.: Analytic root locus and LAMBERT W function in control of a process with time delay. In: Journal of electrical engineering, vol. 62, pp. 327-334 (2011)
21. K.Kang, P.Stubberud: A comparison of continuous time sigma delta modulator simulation methods. In: IEEE International Midwest Symposium on Circuits and Systems (2014)