

# Digital Enhanced Transmitter Concepts for Nanometer-CMOS Technologies

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**Abstract** This chapter shows novel digital enhanced transmitter concepts based on RF-D/A converters as example for innovative circuit solutions mitigating the technology scaling related drawbacks for analog and RF design. Moving analog requirements from voltage to time domain allows to fully benefit from high switching speed in scaled CMOS. RFDACs are key building blocks for digital TX architectures and have to provide very high dynamic range at high clock frequencies and high power efficiency. Innovative digital RFDAC concepts are presented based on current mode and capacitive operation. Pre-distortion, calibration, distributed mixers and novel decoding schemes are employed to fulfill tough cellular and co-existence specifications and to allow multi-mode operation in future digital TX architectures.

## 1 Introduction

The increasing demand for global mobile computing and internet access (any standard, any place, any time) drives the continuous integration of analog and RF functionality into deeply scaled digital CMOS technologies. Highly integrated system-on-chip solutions enable lower cost and reduced power consumption. However, the classical analog device performance like  $g_m$ ,  $g_{ds}$  or noise tends to suffer from technology scaling, e.g. due to pronounced short channel effects and reduced supply headroom.

This work shows kind of a top down approach for RF IC design in scaled technologies. A digital transmitter concept serves as example for scaling friendly system partitioning and scaling friendly architectures that are combined with

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circuit techniques like calibration or pre-distortion to deal with analog imperfections in scaled CMOS technologies. The focus is on the design of the RFDAC as typical mixed-signal circuit suffering from analog imperfections and benefiting from higher switching speed.

The chapter is organized as follows: Sect. 2 describes some key system considerations for the digital transmitter and derives specifications for the RFDAC. In Sect. 3 the design of a current-mode RFDAC in 28 nm CMOS is shown in detail with special focus on technology related design issues. Besides implementation aspects also measurement results from a test IC are presented. Section 4 shows an even more digital and scaling friendly concept for a capacitive RFDAC which may be suited for transceiver solutions in technologies beyond 28 nm.

The focus in this work is on cellular applications; however, the concepts could be easily extended to other radio access technologies (RAT) like WLAN or Bluetooth.

## 2 System Level Aspects of Digital TX

To derive the specifications for the RFDAC some system level requirements for the digital TX need to be discussed. Flexibility is one of the key aspects in today's cellular transceiver solutions. The support of multiple standards and modes like 2G (GSM/EDGE), 3G (WCDMA/HSPA+) and 4G (LTE/LTE-CA) is mandatory. In addition a variety of frequency bands (>40 actually defined in 3GPP) needs to be covered and co-existence with other connectivity technologies like WLAN, Bluetooth or GNSS needs to be supported.

Obviously low cost and low power consumption are key requirements. Low cost translates typically in small chip area, high level of integration, low pin count and low amount of external components. Small chip area and high level of integration can be achieved by moving RF functionality as much as possible in the digital domain. Here technology scaling also helps to reduce power consumption. However, the remaining RF building blocks need to be suitable for deep submicron CMOS. Avoiding the use of external TX filters is another measure reducing costs but increasing the requirements on the dynamic range of the transmitter. The need for very high dynamic range at the TX output is caused by today's frequency division duplex systems and co-existence scenarios. TX and RX (same or different RAT) are active at the same time but on different frequencies. Consequently the TX noise that falls into the RX frequency band needs to be very low. The following example illustrates this: in order to not de-sensitize the RX the injected noise from TX should be much less than the thermal noise from the  $50\ \Omega$  input impedance, e.g.  $-180\ \text{dBm/Hz}$ . Assuming a duplexer attenuation of about 47 dB and a maximum output power of 24 dBm the total TX noise in the RX band should not exceed  $-157\ \text{dBc/Hz}$  at maximum power.

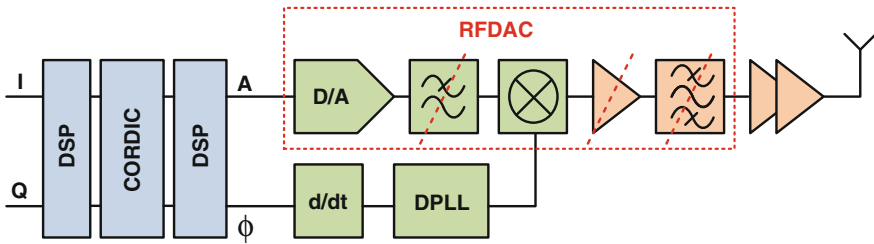


Fig. 1 High-level overview of digital polar TX showing functionality of RFDAC

The digital polar transmitter concept based on RFDAC [1] as shown in Fig. 1 addresses these tough requirements. The digital IQ data from baseband is converted into polar data (amplitude and phase) in the digital front-end using a CORDIC algorithm and digital filtering/interpolation. The derivative of the phase signal (=modulation frequency) is fed to a digital PLL producing the phase-modulated LO signal. The RFDAC block combines almost all the remaining analog functionality in the amplitude path of the transmitter.

Instead of an analog reconstruction filter a D/A converter with very high sample rate is used. The D/A converter is combined/stacked with the up-conversion mixer (fed by phase modulated LO signal) to re-use the DAC current and to avoid a dedicated  $g_m$  cell. The RFDAC is providing enough output power to directly drive the external power amplifier, i.e. no additional analog/RF sensitive driver is needed. Finally the external SAW filter can be removed if the RFDAC provides very high dynamic range. Apart from the external power amplifier and the digital controlled oscillator core in the DPLL the RFDAC is the only remaining analog/RF block in the signal chain.

Obviously the combination of different analog/RF functions in one block yields very tough requirements for the RFDAC:

- High-speed ( $\sim 1\text{--}2$  GHz): to avoid an analog reconstruction filter the sample rate of the DAC needs to be high enough to shift the repetition images far away from RX bands which can mean up to 1 GHz. Additional co-existence restrictions may enforce even higher sample rates up to 2 GHz. Thus, timing is very critical in the decoding logic and the control of the DAC switches. However, scaled technologies and high switching speed help in this case.
- High-power ( $\sim 12$  dBm): without dedicated PA driver the RFDAC needs to provide about 12 dBm peak power which translates into signal currents of up to 100 mA. Therefore power efficient structures are mandatory, e.g. class-B operation, where the DAC current consumption follows the output signal. Class-B operation is equivalent to a single-ended DAC (for current mode).
- High-resolution ( $\sim 100$  dB/17 bit): since the digital TX chain does not provide additional filtering the DAC needs very high resolution and dynamic range. The sum of quantization and thermal noise contributed by the DAC should not exceed  $-166$  dBc/Hz in a 4 MHz bandwidth (RX band) in worst case which translates into approximately 17bit effective resolution.

### 3 Current Mode RFDAC Concept

The basic concept addressing all the requirements mentioned above is shown in Fig. 2. The RFDAC consists of a single-ended current mode DAC stacked with a simple current commuting mixer. The current mode DAC converts the digital input word into a (baseband) current signal with a sample rate of about 1 GHz. It comprises basically just a current source fix connected to the bias voltage and a switch controlled by the digital amplitude information. To avoid spur generation the clock signal for the DAC is directly derived from the LO signal (e.g. LO/2). Since the baseband frequency is typically much lower a significant oversampling ratio is guaranteed. The bias voltage of the DAC is generated via a current mirror that is fed by another (slow) D/A converter. In this way the DAC gain can be controlled over wide range in digital way. The signal current is fed to a single-balanced mixer pair doing the up-conversion to LO rate. To isolate the thin oxide devices of mixer and DAC from the high voltage swing at the output an additional cascode stage is inserted (not shown). Finally a LC balun (trafo) converts the differential current signal into a single-ended voltage signal and filters out the high-order LO components.

In order to achieve the required resolution a segmented approach for the 14bit DAC is chosen [2]. Since the far-off noise/resolution requirements are determined by the differential non-linearity (DNL) of the DAC the thermometer coded segment comprises 10 MSBs resulting in 1024 unit cells. The 4 LSBs in the binary coded part add another 4 binary scaled cells. To avoid the digital complexity of a 10bit binary-to-thermometer decoder, the decoding scheme is split into two parts. The 1024 cells are arranged in an array of  $32 \times 32$  cells controlled by 32 thermometer coded line and 32 thermometer coded column signals derived from 5 binary bits each. To select the active cells a local decoder in each unit cell is added.

#### 3.1 Current Mode RFDAC Design Details

The sizing of the current source transistor is mainly determined by impedance, noise and matching requirements.

- Impedance: the finite output impedance of the current source yields a certain deterministic integral non-linearity (INL) according to [3]. This kind of deterministic, low-order INL shape only affects the in-band resolution or signal quality (system level spec = error vector magnitude, EVM) and the close to carrier harmonics (system level spec = adjacent channel leakage ratio, ACLR). Typical values for EVM ( $\sim 3\%$ ) and ACLR (45 dB) result in quite relaxed numbers for INL and current source impedance. Moreover the switch in series helps to get sufficient impedance.

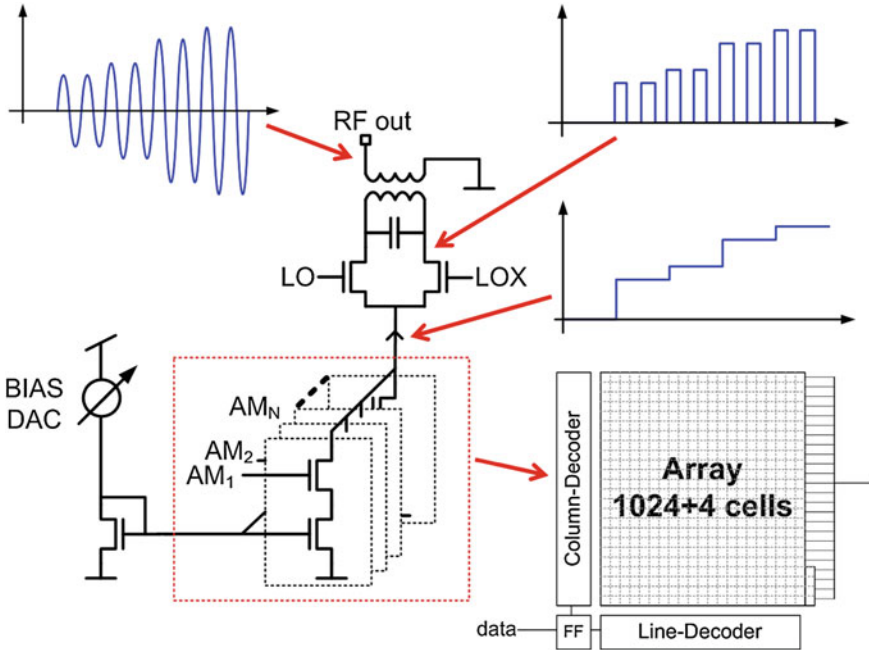


Fig. 2 Basic concept of stacked current mode RFDAC and mixer

- Noise: the thermal noise contribution of the current source is given by

$$\bar{I}_n^2 = 4kT\gamma g_m. \tag{1}$$

The tolerable thermal noise level can be calculated from the total noise budget of  $-166$  dBc/Hz for the DAC comprising thermal and quantization noise. To achieve low thermal noise a low  $g_m/I_d$  ratio is desirable which translates into high overdrive voltage and large channel length of the current source transistor. Flicker noise (which is typically pronounced in scaled CMOS technologies) is no concern here since the frequency offset of the RX bands is in most cases several tens of MHz and thus much higher than the  $1/f$  noise corner frequency.

- Matching: the requirements for the current source mismatch  $\sigma(I)/I$  can be calculated out of the DNL specifications of the DAC. The DNL is dominating the high-order harmonics and the “far from carrier” quantization noise behavior and needs to fulfill the above mentioned 100 dB of SNR. The DNL of a N bit segmented DAC with B binary and N-B thermometer coded bits can be approximated with [4]

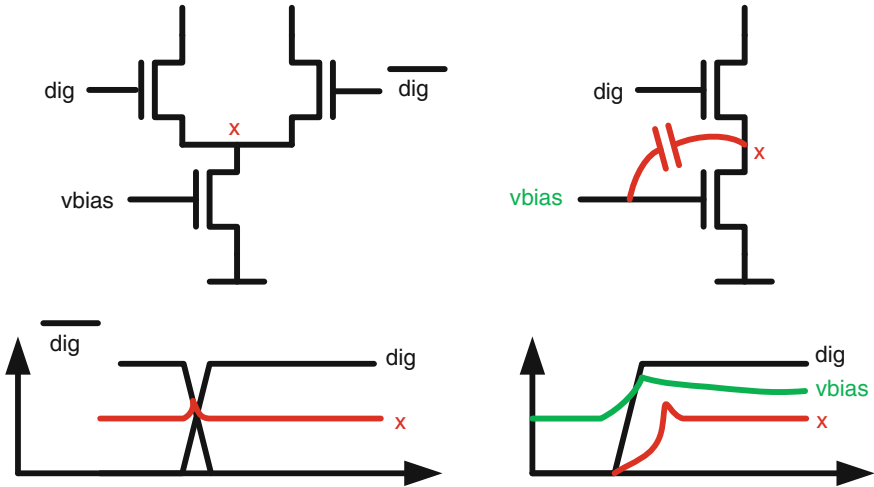


Fig. 3 Differential (left) and single-ended (right) DAC cells

$$DNL \approx \sqrt{2^{B+1} - 1} \frac{\sigma(I)}{I} LSB. \tag{2}$$

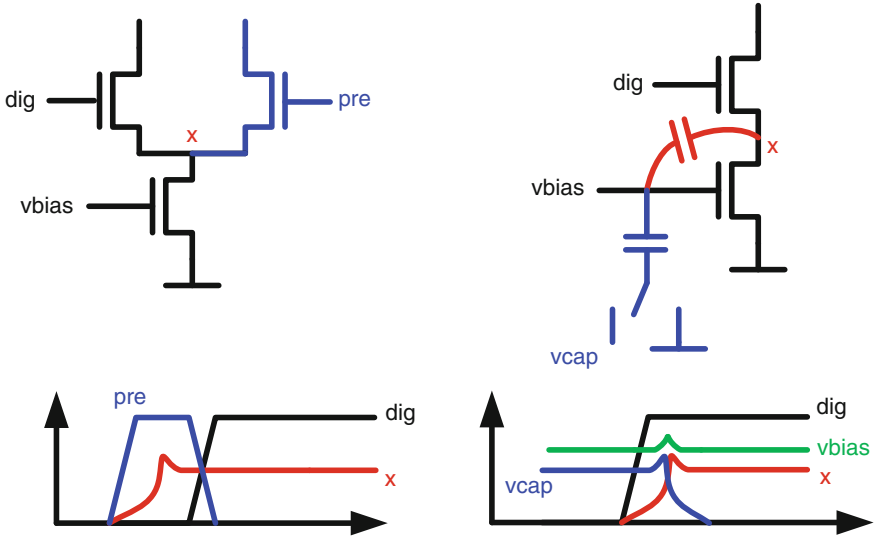
The current source mismatch  $\sigma(I)/I$  finally yields the minimum transistor dimensions according to [5]

$$(WL_{\min}) = \frac{1}{2} \left[ A_{\beta}^2 + \frac{4A_{VT}^2}{(V_{GS} - V_T)^2} \right] \bigg/ \left( \frac{\sigma_I}{I} \right)^2 \tag{3}$$

where  $A_{VT}$  and  $A_{\beta}$  are technology related mismatch parameters. Interestingly these parameters improve with technology scaling down to 45 nm and at least do not worsen even in nanometer scaled CMOS [6].

Besides the static design considerations discussed above the single-ended current mode DAC has some critical drawbacks compared to its differential counterpart as shown in Fig. 3. In contrast to the differential version where the current source is always on and the current is just steered between positive and negative branch the on/off switching in the single-ended version really means a complete charging/discharging of the current source drain node  $x$  since the bias of the current source is not disconnected. This charging/discharging affects especially the dynamic DAC performance:

- To charge the parasitic capacitances at node  $x$  first some current is needed which is missing in the actual signal current. This effect is quite non-linear and leads to harmonic distortion in the output current.



**Fig. 4** Single ended DAC cell with pre-charge (*left*) and H2 compensation (*right*)

- Switching on/off the cells yields large voltage jumps at node  $x$  causing a significant feedback on the bias voltage via the gate-drain capacitor of the current source. This so-called H2 effect is also non-linear and degrades the dynamic performance of the DAC.

To achieve sufficient dynamic performance also in the single-ended DAC two additional compensation schemes are introduced here.

To compensate for the missing signal current during cell activation a pre-charge switch is added, see Fig. 4. The pre-charge switch is closed for half a clock-cycle before the cell is actually switched on. During this half clock cycle node  $x$  is charged to approximately the desired value, so no current is missing when it's really needed. Of course the current flowing through the pre-charge switch results in some current consumption overhead. However, as long as the oversampling ratio is high enough, there is no significant power penalty.

To compensate the H2 effect a dummy capacitor and two further switches are added. In off-state this capacitor is charged to  $V_{cap}$ . When the current cell is activated the capacitor is switched to ground at the same time and charge is subtracted from the bias node. This charge is intended to compensate for the unwanted charge coupled on  $V_{bias}$  via the gate-drain capacitor in order to keep the voltage flat and avoid the H2 effect as shown in Fig. 4.

The effectiveness of the proposed techniques is shown in Fig. 5.

The simulation compares the spectral performance of a single-ended DAC output current with and without pre-charge and H2 compensation for a 1 MHz sine-wave digital input. Especially the critical second harmonic is significantly improved. However, the additional switching activity increases the noise floor slightly.

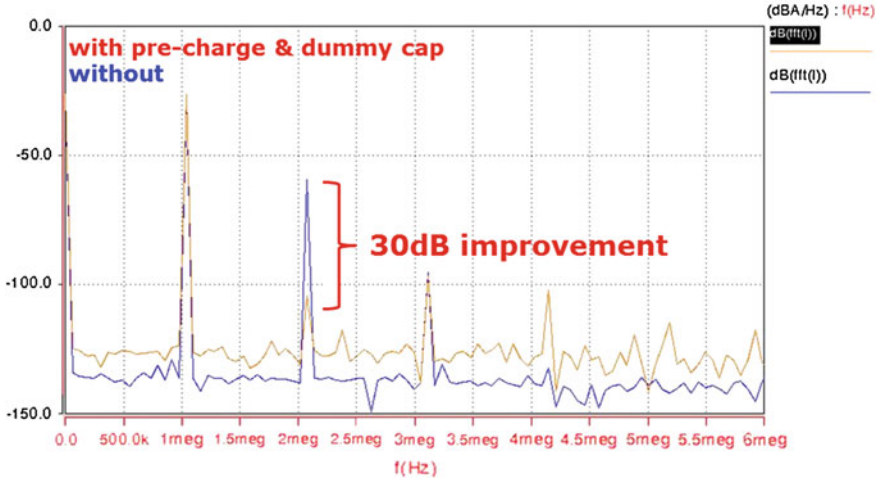


Fig. 5 Simulation result of single-ended DAC with and without pre-charge and H2 compensation for 1 MHz sine-wave input

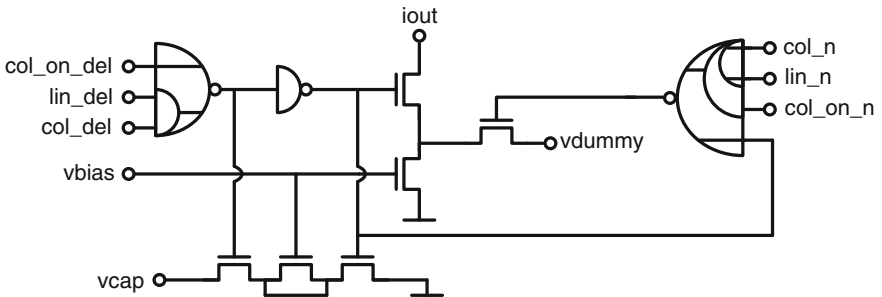
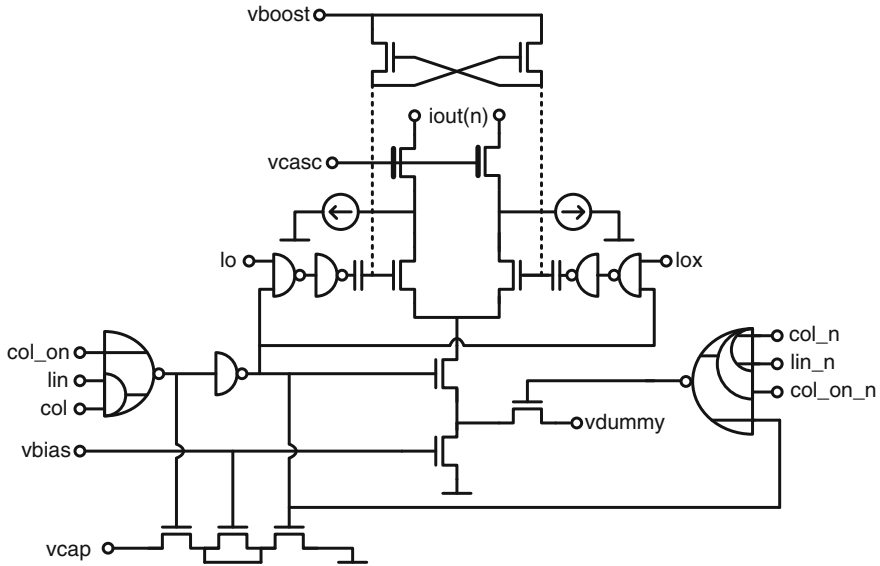


Fig. 6 Schematic of DAC unit cell including pre-charge and H2 compensation

The complete schematic of the current source including pre-charge and H2 compensation capacitor is shown in Fig. 6. The actual switch of the current source is controlled by the local decoder processing the line/column information and is driven by full-swing logic signals. These “cell on/off” logic signals also control the charging and discharging of the dummy capacitor for the H2 compensation that is realized as MOS-cap.

The pre-charge switch is connected to an additional bias voltage  $V_{dummy}$  (approximately set to the desired voltage for node  $x$ ) and controlled by a second local decoder. This additional decoder is controlled by the inverted logic signals for columns and lines which are triggered half a clock cycle before the non-inverted logic signals to generate the pre-charge pulse.

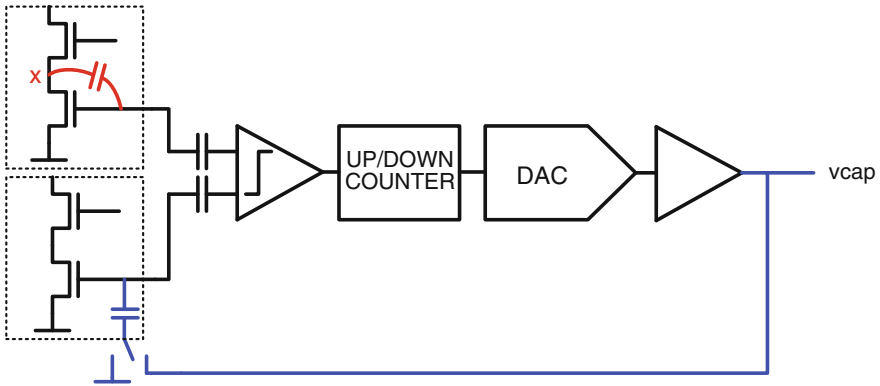




**Fig. 7** Schematic of DAC unit cell including distributed mixer, LO boosting, cascode, pre-charge and H2 compensation

To better deal with the analog limitations in scaled technologies it has been decided to distribute the mixer and include it in the DAC unit cell. This has several advantages: there is no voltage swing at the mixer tail node (=DAC output) so the supply headroom limitations are relaxed. This is quite important since the current source is operated with high overdrive and needs to be kept in saturation. Furthermore the big wiring parasitics at the DAC output that degrade the mixer performance are minimized when the mixer is distributed and placed locally in the cell. Also the sizing of the mixer devices is relaxed since the current density no longer changing so drastically. On the other hand some additional functionality needs to be included in the cell. The LO is gated locally by the “cell-on” signal with a NAND gate to reduce the LO leakage to the output. A local LO signal boosting circuitry is introduced. Thus the mixer devices still can be driven with full swing signals and the bias voltage for the mixer tail node can be selected independently. The boosting consists of an AC coupling (MOS-cap) and a cross-coupled NMOS pair that is setting the DC point. The schematic of the complete DAC unit cell including cascode and mixer is shown in Fig. 7.

Another problem is related to the H2 compensation. The H2 compensation circuit only works only effectively if the charges cancel each other. The main issue here is to select an appropriate voltage for the dummy capacitor. Unfortunately a direct replica of the current source gate-drain capacitor cannot be used for area reasons. Instead a MOS-cap is used. Consequently the capacitor values will not match especially over process, voltage and temperature variations. In order to select the correct voltage for the dummy capacitor a calibration circuit is



**Fig. 8** Simplified schematic of H2 voltage calibration circuit

introduced as shown simplified in Fig. 8. In this concept two kinds of dummy DAC cells are used. One part is always coupling on a virtual bias node via the current source gate-drain capacitor whereas the other part is always coupling on another virtual bias node via the dummy capacitor. The amount of coupling on both nodes is now compared via an offset compensated comparator. The comparator result controls an up–down counter which again sets a simple very slow D/A converter generating the voltage for the dummy capacitor. The voltage is changed via the control loop until the coupling on both nodes is the same. As soon as the coupling is equal the correct H2 compensation voltage is found and used in the array. The calibration can be operated in the background from time to time since typical PVT variations occur quite slowly.

### 3.2 Measurement Results

The digital polar TX based on current-mode RFDAC has been implemented on a test IC in 65 and 28 nm digital CMOS. Supply voltages are 1.1 and 2.5 V for digital & DAC-array and balun center-tap, respectively. The active chip area for the DAC including balun, biasing and LDO is about 0.2 mm<sup>2</sup> in 28 nm.

Since the RFDAC is covering almost all functionality in the amplitude chain a stand-alone characterization does not make much sense. Instead the measured performance of the complete TX is briefly discussed here.

The measured spectra for 3G modes in 65 nm are shown in Fig. 9. The linearity and in-band signal quality is reflected in the ACLR. In both cases very good linearity is achieved due to DAC pre-charge and H2 compensation even without digital pre-distortion.

As mentioned above the far-off noise is considered as much more critical than linearity. One example from 65 nm test IC for 3G high-band operation at

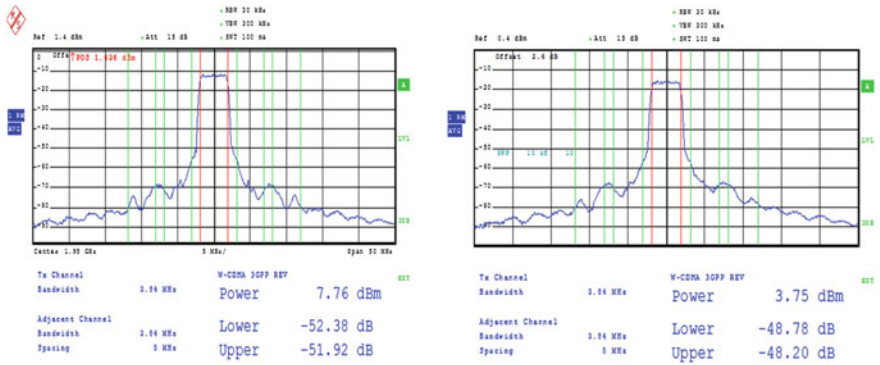


Fig. 9 Measured 3G spectra for WCDMA at 8 dBm (left) and HSUPA at 4 dBm (right)

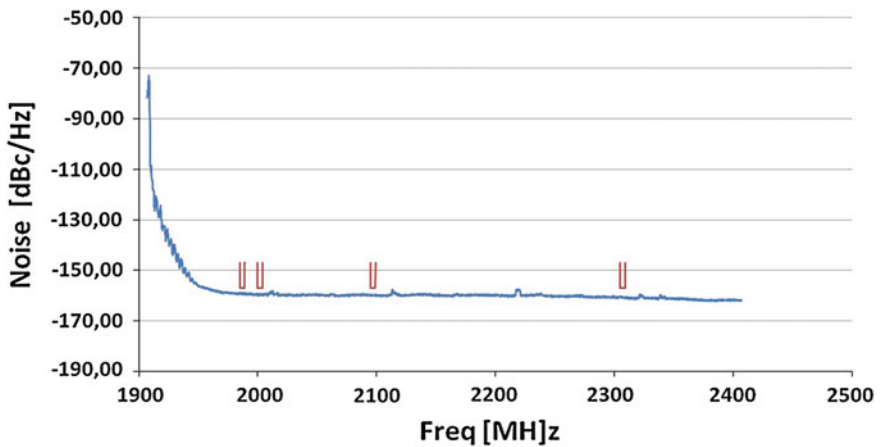


Fig. 10 Measured far-off noise in 3G with different duplex requirements

1907 MHz and 6 dBm output power is given in Fig. 10 where also the different RX frequency bands are indicated. The noise floor is quite flat and achieves the required values of  $-157$  dBc/Hz (at chip level) with sufficient margin. It's worth mentioning that the actual TX signal is only partly visible in the measurement. The reason is the limited dynamic range of the measurement equipment. As mentioned above about 100 dB dynamic range is required. The dynamic range of commercially available spectrum analyzers does not reach these values. To circumvent this limitation a second chain with tuneable notch and LNA is used. The notch filters out the carrier signal and the LNA amplifies the remaining noise floor. Of course careful calibration is needed for this signal chain.

## 4 Capacitive RFDAC

Although the digital transmitter concept shown above is already technology scaling friendly there are some limitations, mostly related to the current mode RFDAC. The limited supply voltage headroom is the biggest concern since a current source is used as linear/matching element. The required saturation voltage limits the down-scaling of the supply voltage but also the achievable efficiency. The need for a thick oxide cascode device complicates the design and especially the layout of the complex DAC unit cell. Finally the actual signal bandwidth is limited by the bandwidth of the auxiliary circuitry for compensation, calibration and biasing. To show a possible path for further technology scaling a novel RFDAC concept is briefly introduced here. Based on the idea of switched-capacitor power amplifiers [7] a capacitive RFDAC has been developed and tested in 28 nm CMOS. The basic concept is shown in Fig. 11. The DAC comprises an array of matched capacitors that are driven by the phase modulated LO signal. The amplitude modulation is added by a digital mixer which is just a NAND gate. Based on the amplitude information the amount of cells contributing to the output signal is controlled, the off-cells form a capacitive divider. Similar to the current mode approach a matching network is required to filter out higher order components. The capacitive RFDAC concept has several advantages: the structure behaves like a class-D amplifier where high power efficiency is achievable. Instead of a current source a capacitor acts a linear/matching element. So no headroom for saturation is wasted and the resolution is given only by capacitor matching which tends to improve by technology scaling. The capacitors are driven by inverters which are by definition the most scaling friendly elements in CMOS technologies: supply voltage can be reduced well below 1 V and active area is very small. Another advantage is that no high voltage domain is needed anymore for the balun since the matching is not stacked but connected in parallel.

Despite of the clear benefits in terms of scaling the C-RFDAC obviously suffers from some imperfections. The main challenge is related to the supply of the inverters which is now acting also as DAC reference. The current consumption follows the amplitude, so any response of the supply voltage on signal current e.g. via IR drop or imperfect load regulation in the LDO creates non-linear effects. Also the thermal noise of the supply needs to be very low. The non-ideal behavior of the inverters furthermore degrades the performance of the DAC. The AM information ( $=n$ ) modulates the effective load and the rise-fall time of the inverters, see Fig. 12. This effect creates some amplitude dependent phase shift (AM-PM) resulting in harmonic distortion. Interestingly the phase-shift follows the amplitude in an almost linear manner. So a simple digital pre-distortion can be used to compensate for the effect. The finite, non-linear MOS resistance is also modulating the actual current flowing into the load (AM-AM). Further non-ideal effects can be found in [7].

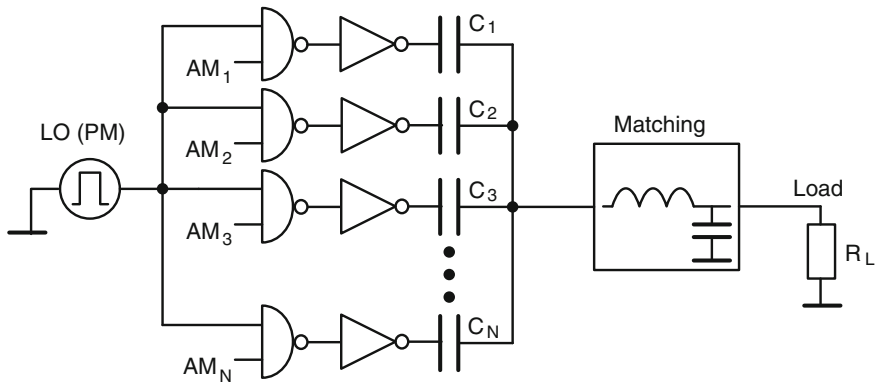


Fig. 11 Basic concept of capacitive RFDAC

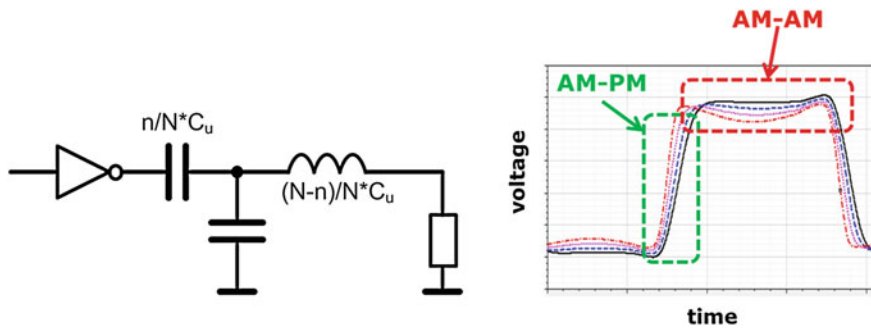
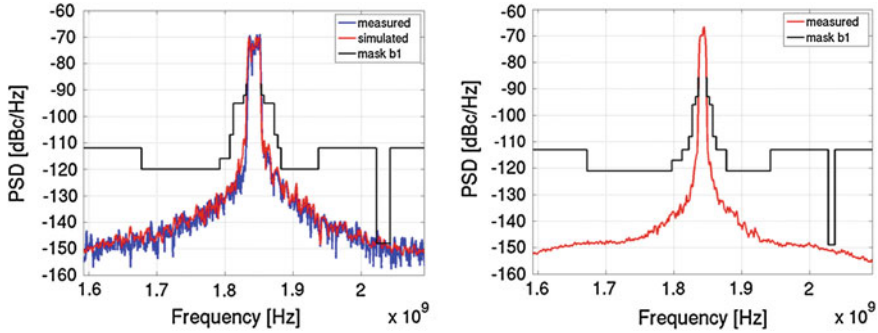


Fig. 12 Load modulation of inverters and resulting non-ideal switching wave-form

Finally the LO signal distribution and the timing alignment is very critical to achieve the tough far-off noise specifications. However this shift from voltage to time domain requirements enables to benefit from faster switching in scaled CMOS. The sizing of inverter and capacitors is not discussed in detail but can be derived in a similar way as shown in Sect. 3 from linearity, output power and resolution requirements.

Also the capacitive RFDAC has been implemented as part of a digital TX chain in 28 nm CMOS. To achieve similar resolution the DAC structure and segmentation is identical to the current mode approach, just the unit cell is replaced and the decoder adapted. A LUT based digital pre-distortion is included. The supply voltage is 1.1 V for digital and analog, no high-voltage domain is needed. The active chip area for the DAC including matching network and LDO is about 0.14 mm<sup>2</sup>.

Some key measurement results are shown in Fig. 13.



**Fig. 13** Measured and simulated spectrum for LTE20 (*left*) and measured spectrum for LTE10 (*right*) at 0 dBm output power

The measured linearity and effective resolution are very promising since the tough out-of-band emission mask is fulfilled even for wideband standards like LTE20 and LTE10. The measured performance proves the feasibility of this RFDAC concept for future digital TX applications.

## 5 Conclusions

It has been shown by two concrete design examples that technology scaling is no road block for integration of analog/RF functionality. Appropriate system partitioning and scaling friendly architectures combined with innovative circuit techniques enable high resolution analog circuitry even in nanometer CMOS. Moving analog functionality in the digital domain and moving voltage resolution requirements into time resolution requirements further supports scaling and integration.

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