Chapter 10
Space Vector Modulation in Three-Phase Three-Level Flying Capacitor Converter-Fed Adjustable Speed Drive

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Abstract This Chapter is devoted to the Space Vector Modulation (SVM) in three-phase three-level Flying Capacitor Converter (FCC) fed adjustable speed drive (ADS). First, the classical and adaptive SVM are described. The adaptive SVM provides reduction of number of switching in the whole linear range of the converter operation because minimal number of vectors is used in each modulation region. As result, switching losses in FCC are reduced in comparison to the classical SVM and thus, the converter efficiency is increased. Next, elimination of DC sources unbalance in full range of operation of the FCC is presented. The minimization of the flying capacitors voltages pulsation is obtained by the compensation of flying capacitors voltages balancing delay based on prediction of those voltages values in next modulation period. Finally, taking to account the requirements of the demanding ASD application: low speed operation without phase current distortion and the high speed operation over the linear range of the converter with reference output voltage amplitude, the additional features for both modulation techniques: the dead-time effect and semiconductor devices voltage drop compensation as well as the overmodulation algorithm are shown.

1 Introduction

Recent advances in the energy conversion area (e.g. Distributed Power Generation systems, traction and Adjustable Speed Drives (ASD)) show a focus trend in the Voltage Source Converters (VSC) [1–5]. Generally we can distinguish two groups

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of VSC: two-level and multilevel. Two-level converter is well known topology used for a long time by industry. Multilevel converter is also not new topology, some of converters are known since 1960s, but they were not used by industry until recently by some of technological barrier. Two technology breakthroughs of the electronic industry have enabled this remarkable development:

- the introduction of modern IGBTs on the market enabled the manufacturing of reliable, robust and low cost VSC modules which allow to construct VSC working with increased voltage and current ratings,
- the introduction of low cost digital signal microprocessors and FPGA for real time applications allowed the successful implementation of complex vector control schemes for VSC.

The idea of multilevel VSC is based on series connection of semiconductor devices with more than one DC voltage source. The multilevel VSC operation above typical semiconductor voltage limits with reduced voltage stress, lower common mode voltages, reduced harmonics distortion and lower filter requirements are some of the well known advantages that have made this topologies popular for research and industry. Lately, the multilevel VSC topologies fed three-phase ASD have become attractive for the medium and high power conversion [6, 7]. Especially two three-level topologies are now used in the three-phase ASD industrial applications: the Diode Clamped Converter (DCC), proposed in 1981 by Nabae and Takahashi [8] and the Flying Capacitor Converter (FCC), proposed in 1991 by T. A. Meynard and A. Foch [9].

The three-phase three-level DCC is most popular in the ASD industrial application. In the DCC, the DC-link capacitors voltage balancing depends on the switching states in all phases. However, many DC voltage sources causes problem of capacitors utilization in full range of the converter operation. For example, in three-phase three-level DCC for high modulation index and for higher number of levels, even with sophisticated Pulse Width Modulation (PWM) techniques, bringing DC-link capacitors voltage difference to zero is difficult [10–15]. Hardware solutions (such as passive voltage balancing with parallel resistors) or introducing additional virtual switching states may have detrimental effects on the ASD efficiency [12, 13, 16]. To solve this problem, for higher number of levels, the Active DCC topology was introduced by ABB [17, 18]. This five-level hybrid topology combines flexibility of the FCC with the robustness of the industrial DCC to generate multilevel voltages. However, it cannot be used for commonly three-level applications.

From other hand FCC topology typically is used in active filtering [19, 20] because the flying capacitors (FCs) voltage balancing in one phase is independent of switching states in other phases [9, 21–24]. It means, that each phase can be considered separately and in that case the FC's voltage balancing does not depend on the value of modulation index, only on the current flow direction. In comparison to the DCC this is an advantage of the FCC topology, because the FC's are used for output voltage generation in full converter operation range, except six step operation. Thus, the three-phase three-level FCC can be an important alternative to

the three-phase three-level DCC in ASD application especially in aspect of capacitors utilization in full range of operation.

In the typical active power filter application of the FCC, usually for each phase Carrier-Based PWM (CB-PWM) is applied [25–28]. Therefore, the SVM techniques where not developed for the FCC as widely as for the DCC, and only several works describing this issue in classical approach can be found [24, 29–33]. However it should be noted that various SVM strategies of selecting the vectors order exist for multilevel converters. Strategy selection will affect the harmonic content and the switching losses [34–36]. Especially, SVM techniques which minimize number of switching and as consequence, the switching losses were not published for the FCC—only a few works exist in this subject [24, 33].

This chapter is devoted to SVM in three-phase three-level FCC fed ASD. First, the classical and adaptive SVM, which minimizes number of switching and as consequence, reduces the switching losses in FCC are described. Next, elimination of DC sources unbalance in full range of operation of the VSC and minimization of the FCs voltages pulsation is presented. Finally, taking to account the requirements of the demanding ASD application: low speed operation without phase current distortion and the high speed operation over the linear range of the converter with reference output voltage amplitude, the additional features for both modulation techniques: the dead-time effect and semiconductor devices voltage drop compensation as well as the Overmodulation algorithm are shown.

2 Space Vector Modulation in Flying Capacitor Converter

2.1 Introduction

Modulation techniques for VSC are responsible for generation of average output (represented by different width of short voltage pulses) voltage with proper balancing of the additional DC voltage sources for multilevel converters. Depending on VSC topologies and switching frequency numerous PWM techniques can be listed [26]. Among them two kinds of PWM are used for FCC: CB–PWM [25–28, 37] and SVM [29–33].

The operation principle of CB-PWM bases for each phase on comparison of reference sinusoidal output phase voltage signal $u_{x,ref}$, where x is the phase of the system with the triangular carrier signals. As result, the width of output pulses is proportional to the reference signal and the output voltage harmonics are concentrated around doubled carrier signal frequency and their multiplication. The multilevel converter needs n–1 triangular carrier signals, where n is number of levels. Thus, two carrier signals are used for the three-level converter. Depending on mutual location of carrier signals two general groups of the CB-PWM can be listed: Phase Shifted [27, 38] and Level Shifted PWM [28]. The Phase Shifted PWM carrier signals are shifted in phase by $360°/(n-1)$. The Level Shifted PWM

carrier signals are level shifted in mean of average voltage level value. Phase Shifted PWM is widely used in FCC due to automatic self-balancing of FC capacitors [39]. For Level Shifted PWM three modifications based on carrier signals phase shifting are known, however they do not provide automatic self-balancing of FC capacitors.

The three-phase VSC output phase voltage maximum instantaneous value is 2/3 of DC-link voltage in so-called six step or square wave mode operation [21]. The maximum possible modulation index for six step operation is $M = n-1$. However, the linear modulation range of the VSC for CB-PWM with sinusoidal reference output phase voltage signal $u_{x,ref}$ is limited to $M < 0.785(n-1)$. To extend converter linear range of operation in the CB-PWM up to $M = 0.907(n-1)$, the Zero Sequence Signal (ZSS) of 3rd harmonics frequency is added to sinusoidal reference output phase voltage signal $u_{x,ref}$ [21, 40]. If neutral point of ASD is not connected to the DC-link midpoint, the phase current depends only on phase-to-phase voltage. In such case, the ZSS does not produce phase voltage distortion, however current harmonics are changed. The most known ZSS bases on sinusoidal signal with 1/4 and 1/6 amplitude of the fundamental harmonics. The 1/4 amplitude provides minimum phase current harmonics [41] while the 1/6 amplitude provides maximal converter linear range of [42]. It should be noticed that the triangular ZSS with 1/4 amplitude generates the same output voltage as the SVM with symmetrical vector placement.

The second kind of mostly used PWM is SVM [21, 43]. The three-phase circuit—due to space vector theory—can be described in stationary rectangular coordinate system. Thus, the three-phase VSC can be described in $\alpha\beta$ plane as switching state representation of Space Vector. As it was mentioned before, the SVM techniques where not widely developed for the FCC, usually in the typical active power filter application for each phase CB-PWM is applied [25–28]. Thus, only several works describing this SVM issue in classical approach can be found [24, 29–33]. However, recent advances and constant development of the digital signal processing systems (allowing high precision digital implementation of complex control algorithms) contributed to this, that the SVM gained superior position for research and industry. The digital implementation of SVM is characterized by its simplicity. Therefore, the SVM is a good alternative for the CB-PWM in the modern three-phase FCC fed ASD application.

For multilevel converters various SVM strategies of selecting the vectors order exist. Strategy selection can affect—in the same way as the CB-PWM—the harmonic content and the switching losses [34–36]. The SVM FC voltage balancing mostly depend on selection of redundant vectors [22, 23, 43]. Thus, to reduce switching losses with proper FC voltages balancing, only minimal number of vectors in each modulation region—typically three—can be applied to the FCC [13, 35]. The vectors selection is made adaptively to the changes of the FCC electrical parameters (currents sign and amplitude, FC voltages amplitude etc.) [13]. In this section the classical and adaptive SVM (CSVM and ASVM, respectively), which minimizes number of switching and as consequence, reduces the switching losses in FCC are described.

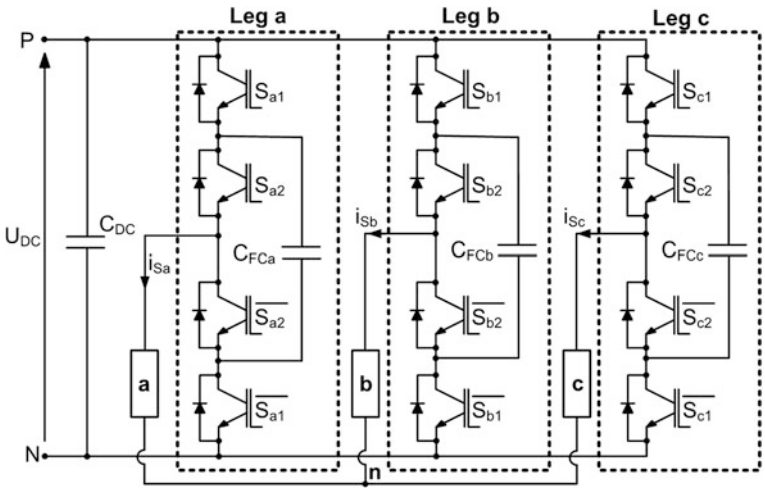

Fig. 1 Three-level three-phase FCC converter

2.2 General Description of Space Vector Modulation for Flying Capacitor Converter

Figure 1 shows the three-level three-phase FCC converter. Each leg consist of four switches and a Flying Capacitor C_{FCx}.

As far as the FCC three-phase system is assumed to be symmetric, the simplified Clarke transformation from natural *abc* into stationary $\alpha\beta$ coordinate system can be used. Figure 2 shows graphic representation of the Space Vector $\alpha\beta$ voltage plane with possible output voltage vectors of the three-level converter. All voltage vectors are described by three numbers, corresponding to switching states in leg *a*, *b* and *c*, respectively. Table 1 presents possible switching states for single inverter leg. Typically, the FC voltage for the FCC operation should be equal half of the DC-link voltage. With this condition switching state **1** can be divided into two redundant states **1A** and **1B** (highlighted in the Fig. 3) which generates the same output voltage $U_{FCx} = U_{DC}/2$. As the output voltage does not depend on the type of selected state (**1A** or **1B**), they can be used for independent control of U_{FCx}. To decrease number of commutations only one state for each phase is chosen in sampling period. Table 2 shows selection between redundant states **1A** or **1B** based on the stator current i_{Sx} sign.

For the three-phase three-level FCC the twenty-seven voltage vectors **V** can be specified, as follows:

- 3 zero vectors (**000**, **111** and **222**),
- 12 internal small amplitude vectors (**100**, **211**, **110**, **221**, **010**, **121**, **011**, **122**, **001**, **112**, **101** and **212**),
- 6 middle medium amplitude vectors (**210**, **120**, **021**, **012**, **102** and **201**),

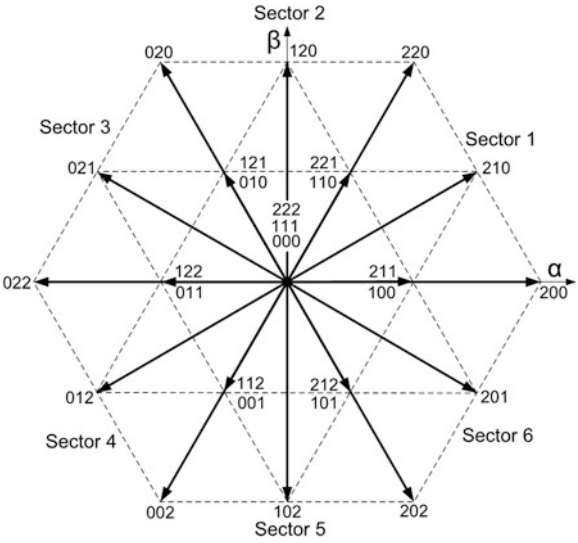

Fig. 2 The $\alpha\beta$ voltage plane for three-level three-phase converter

Table 1 Switching states for the three-level FCC leg

Switching states	S_{x1}	S_{x2}	$U_{a,UdcN}$
0	OFF	OFF	0
1A	ON	OFF	$U_{DC} - U_{FCx}$
1B	OFF	ON	U_{FCx}
2	ON	ON	U_{DC}

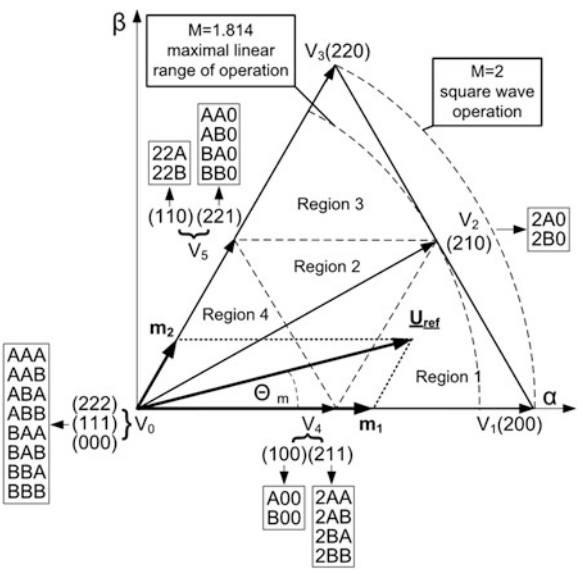

Fig. 3 Sector 1 with division into four regions and all possible switching states

Table 2 Redundant switching state selection

Conditions	$i_{Sx} < 0$	$i_{Sx} > 0$
$U_{FCx} < U_{DC}/2$	**1B**	**1A**
$U_{FCx} > U_{DC}/2$	**1A**	**1B**

- 6 external large amplitude vectors (**200**, **220**, **020**, **022**, **002** and **022**).

External vectors divide vector plane into six sectors: 1–6 (see Fig. 2). Each sector is divided into four triangular regions. Figure 3 shows sector 1 divided into four regions with all possible switching states.

The reference Space Vector $\boldsymbol{U_{ref}}$ is described by length and its angle:

$$U_{ref} = \sqrt{u_{\alpha,ref}^2 + u_{\beta,ref}^2}, \quad \Theta_m = \arctan\frac{u_{\alpha,ref}}{u_{\beta,ref}} \tag{1}$$

Since each sector encloses in 60°, the Space Vector angle Θ_m is used to determine reference Space Vector $\boldsymbol{U_{ref}}$ sector location. To calculate region number and duration of switching states, a value of modulation index is indispensable. Modulation index M determines proportion of reference Space Vector $\boldsymbol{U_{ref}}$ length in respect to the DC-link voltage. There are a few definitions of modulation index:

$$M = \frac{\sqrt{3}U_{ref}}{U_{DC}}(n-1) \tag{2}$$

where $M = 2$ when $\boldsymbol{U_{ref}}$ trajectory lies on circumscribed circle in the hexagon,

$$M = \frac{3U_{ref}}{U_{DC}}(n-1) \tag{3}$$

where $M = 2$ when $\boldsymbol{U_{ref}}$ trajectory lies on inscribed circle in the hexagon,

$$M = \frac{\pi U_{ref}}{2U_{DC}}(n-1) \tag{4}$$

where $M = 2$ for the square wave operation (six step mode) of the VSC. In further considerations the (4) definition will be used.

Calculation of the region number of the Space Vector location and duration of switching states is based on two additional factors, so-called *small modulation indexes*. The m_1 and the m_2 are projection of the reference Space Vector $\boldsymbol{U_{ref}}$ on the sector sides, limited by external vectors (see Fig. 3) According to the trigonometric dependence, *small modulation indexes* are calculated as follows:

$$m_1 = M(\cos\Theta_m - \frac{\sin\Theta_m}{\sqrt{3}}) \tag{5}$$

$$m_2 = 2M\frac{\Theta}{\sqrt{3}} \tag{6}$$

Table 3 Region number and duty cycles calculation

Conditions	Region	Switching times
$m_1 > 1$	1st	$T_1 = (m_1 - 1)T_S$, $T_2 = m_2 T_S$
		$T_4 = (2 - m_1 - m_2)T_S$, $T_0 = T_3 = T_5 = 0$
$m_1 < 1$, $m_2 < 1$	2nd	$T_2 = (m_1 + m_2 - 1)T_S$, $T_4 = (1 - m_2)T_S$
$m_1 + m_2 > 1$		$T_5 = (1 - m_1)T_S$, $T_0 = T_1 = T_3 = 0$
$m_2 > 1$	3rd	$T_1 = m_1 T_S$, $T_3 = (m_2 - 1)T_S$
		$T_5 = (2 - m_1 - m_2)T_S$, $T_0 = T_1 = T_4 = 0$
$m_1 < 1$, $m_2 < 1$	4th	$T_4 = m_1 T_S$, $T_5 = m_2 T_S$
$m_1 + m_2 < 1$		$T_0 = (1 - m_1 - m_2)T_S$, $T_1 = T_2 = T_3 = 0$

In each sector calculations carried out to achieve vectors switching times are the same and the difference is only in power switch selection for the gating signal. Thus, the reference vector is normalized to the first sector and after evaluation of vectors switching times a proper transistor switching sequence, for reference position, is created. Table 3 presents calculation of region number and switching times in respect to the m_1 and the m_2.

Depending on placement of zero and internal vectors, the CSVM and their modifications, like ASVM, can be distinguished.

2.3 Compensation of Flying Capacitor Voltage Balancing Delays

Regardless of used SVM, control algorithm introduces one period delay between switching states calculation and its hardware realization. One period delay has a significant impact on FC voltages balancing through the PWM modulator, which is based on actual measured values. When the FC balancing is delayed, the FC voltage ripples are doubled. Therefore, for compensation of the delay effect, the estimation of the FC voltages instantaneous value was introduced. In the first step, the U_{FCx} instantaneous value at the end of sampling period is calculated as:

$$U_{FCx}(t+1) = U_{FCx}(t) + \frac{i_{Sx}(t+0.5)dT_{Sx}}{C_{FC}} \tag{7}$$

where $U_{FCx}(t)$ is measured FC voltage and dT_{Sx} is pulse time duration influencing C_{FCx} voltage. Moreover, the $i_{Sx}(t+0.5)$ is estimated amplitude of measured stator current $i_{Sx}(t)$ in the middle of sampling period:

$$i_{Sx}(t+0.5) = i_{Sx}(t) + \frac{i_{Sx}(t) - i_{Sx}(t-1)}{T_S} \tag{8}$$

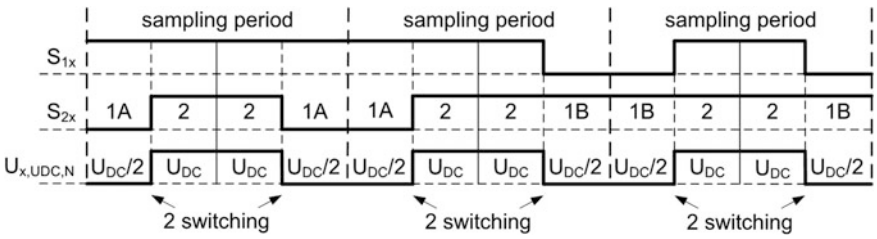

Fig. 4 Modification of switching pattern

where: $i_{Sx}(t-1)$ measured stator current in previous sampling period. In the next step estimated $U_{FCx}(t+1)$ instantaneous value of U_{FCx} is used for the FC voltages balancing selection. This eliminates the delay effect.

2.4 Classical Space Vector Modulation

The CSVM modulation for the FCC uses all possible nearest vectors including their redundant states (e.g. in sector 1: $\mathbf{V_1}$, $\mathbf{V_2}$ and $\mathbf{V_4}$ in 1st, $\mathbf{V_2}$, $\mathbf{V_4}$ and $\mathbf{V_5}$ in 2nd, $\mathbf{V_2}$, $\mathbf{V_3}$ and $\mathbf{V_5}$ in 3rd and $\mathbf{V_0}$, $\mathbf{V_4}$ and $\mathbf{V_5}$ in 4th region) for output voltage generation with symmetrical placement of zero and internal vectors [29–33]. It means that time T_0 dedicated for zero vector is divided by three and each of zero vectors $\mathbf{V_0}$ (**000**, **111** and 2**22**) are selected for one-third of the T_0. Also times T_4 and T_5 are divided by two and each of $\mathbf{V_4}$ (e.g. in sector 1: **100** and **211**) and $\mathbf{V_5}$ (e.g. in sector 1: **110** and **221**) vectors are selected for half of proper calculated time. The CSVM provides low phase current distortion due to high number of switching states used for the output voltage generation (all 7 possible vectors in 4th region and 5 vectors in regions 1st, 2nd and 3rd are used). The FC capacitors voltages U_{FCx} ripples are also limited—both redundant states **1A** and **1B** uses the FC for output voltage generation. However, high phase current quality results in switching losses.

When the selected redundant state **1A** or **1B** is changed, the next modulation period can contain additional switching between sampling periods: two in 2nd and four in region 1st and 3rd region. These additional switching can damage the converter—all switches are changing their state what can generate overvoltage. To eliminate this undesired effect and to provide better switching distribution between particular switches a modification of switching pattern was introduced (see Fig. 4). Modified switching patterns of the CSVM always provide 6 switching in 1st and 3rd, 8 switching in 2nd and 12 switching in 4th region.

Figures 5, 6, 7 and 8 presents switching patterns in 1st, 2nd, 3rd and 4th region in sector 1 for different switching states selected **1A** or **1B** for all phases, respectively.

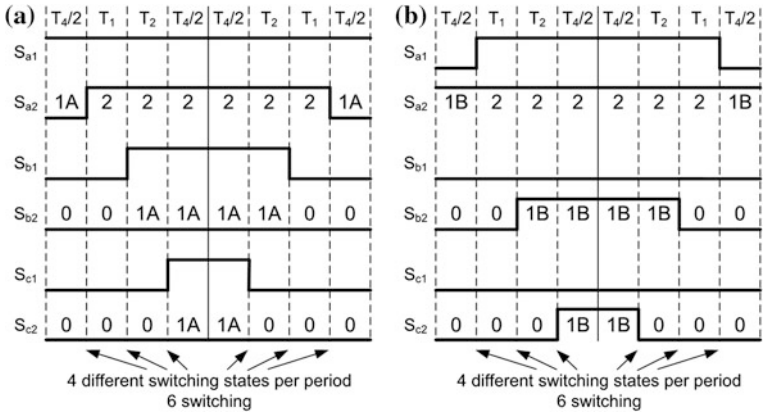

Fig. 5 Duty cycles for the 1st region in sector 1: **a** for **1A** state selection in each phase, **b** for **1B** state selection in each phase

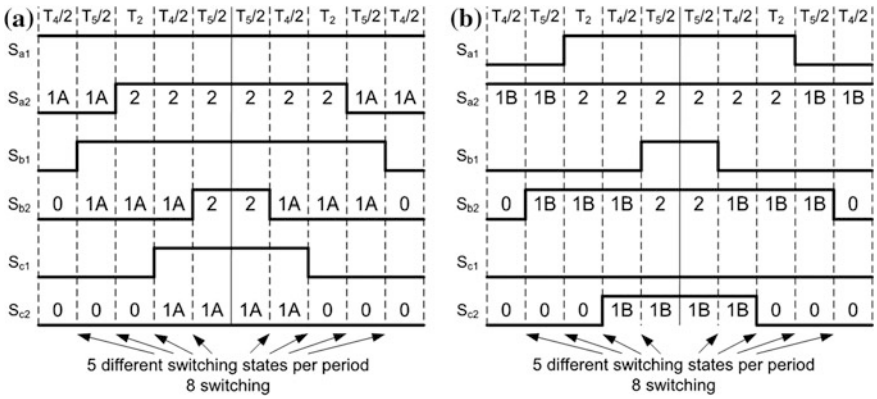

Fig. 6 Duty cycles for the 2nd region in sector 1: **a** for **1A** state selection in each phase, **b** for **1B** state selection in each phase

2.5 Adaptive Space Vector Modulation with Reduced Number of Switching

To reduce switching losses only three selected vectors in each operation region are applied in modulation period adaptively to the electrical parameters [13, 21, 24, 44, 45]. To achieve this goal two solutions have been used in the ASVM.

The first one—used in all regions—bases on assumption that only one instead of two states of internal vectors $\mathbf{V_4}$ and $\mathbf{V_5}$ is applied in each sampling period. Table 4 shows pairs of internal vectors that should be chosen in each sector.

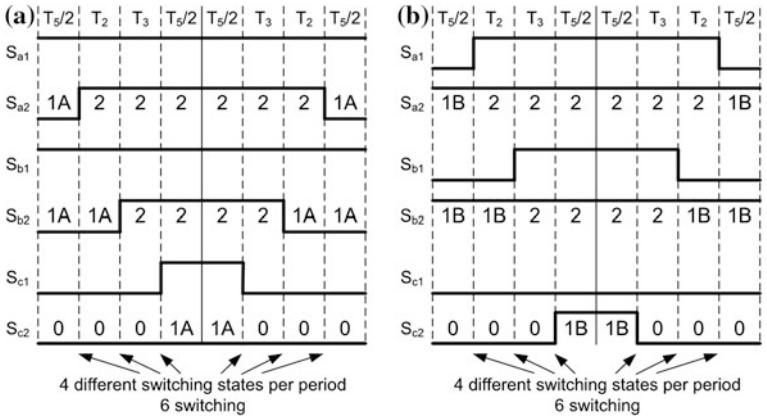

Fig. 7 Duty cycles for the 3rd region in sector 1: **a** for **1A** state selection in each phase, **b** for **1B** state selection in each phase

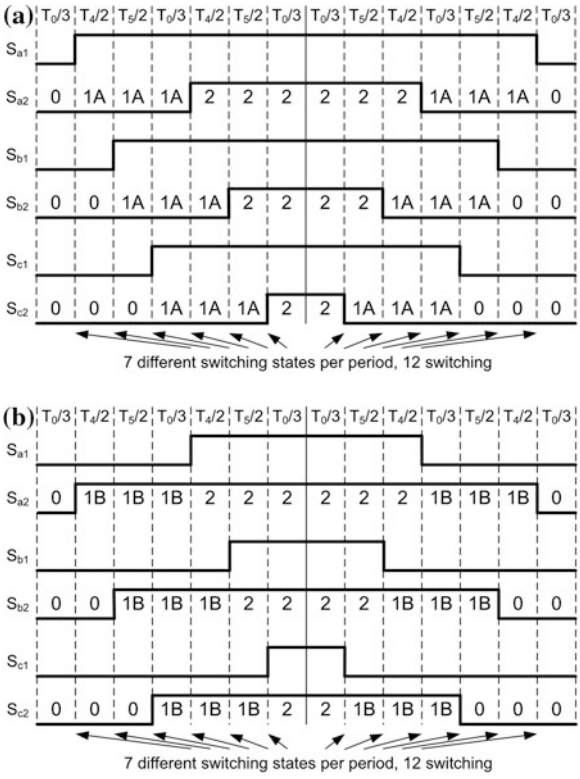

Fig. 8 Duty cycles for the 4th region in sector 1: **a** for **1A** state selection in each phase, **b** for **1B** state selection in each phase

Table 4 Internal vectors $\mathbf{V_4}$ and $\mathbf{V_5}$ pairs selection

Sector	Pair $P1$	Pair $P2$
1	**100** and **110**	**211 and 221**
2	**110** and **010**	**221** and **121**
3	**010** and **011**	**121** and **122**
4	**011** and **001**	**122** and **112**
5	**001** and **101**	**112** and **212**
6	**101** and **100**	**212** and **211**

Those pairs combined with middle and external vectors provide switching losses reduction. Which pair should be selected depends on their influence on U_{FCx} values at the end of sampling period. The pair which provide smallest maximum difference between reference $U_{DC}/2$ and estimated voltage at the end of sampling period $U_{FCx}(t+1)$ for all FCs will be used. The pair selection algorithm is realized as follows:

1. For each phase the redundant state **1A** or **1B** is chosen.
2. For each pair, according to the (9) and (10) all FCs voltages at the end of sampling period are estimated:

$$U_{FCx,P1}(t+1) = U_{FCx}(t) + \frac{i_{Sx}(t+0.5)dT_{Sx,P1}}{C_{FC}} \tag{9}$$

$$U_{FCx,P2}(t+1) = U_{FCx}(t) + \frac{i_{Sx}(t+0.5)dT_{Sx,P2}}{C_{FC}} \tag{10}$$

where: $dT_{Sx,P1}$ and $dT_{Sx,P2}$ are pulse time duration respectively of pair $P1$ and $P2$ influencing C_{FCx} voltage and the $i_{Sx}(t+0.5)$ is estimated amplitude of measured stator current $i_{Sx}(t)$ in the middle of sampling period:

$$i_{Sx}(t+0.5) = i_{Sx}(t) + \frac{i_{Sx}(t) - i_{Sx}(t-1)}{T_S} \tag{11}$$

3. For each pair the modulus of the difference between estimated $U_{FCx}(t+1)$ and reference $U_{DC}/2$ voltage is calculated:

$$\Delta U_{FCx,P1} = \left| \frac{U_{DC}}{2} - U_{FCx,P1}(t+1) \right| \tag{12}$$

$$\Delta U_{FCx,P2} = \left| \frac{U_{DC}}{2} - U_{FCx,P2}(t+1) \right| \tag{13}$$

4. For each pair the maximum of above modulus for each FC is calculated:

$$U_{FC,P1,MAX} = maximum\left(\Delta U_{FCa,P1}, \Delta U_{FCb,P1}, \Delta U_{FCc,P1}\right) \tag{14}$$

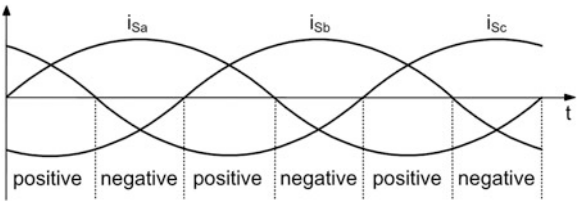

Fig. 9 Peak of the current polarity

$$U_{FC,P2,MAX} = maximum\left(\Delta U_{FCa,P2}, \Delta U_{FCb,P2}, \Delta U_{FCc,P2}\right) \tag{15}$$

5. The pair for which maximum of above modulus has smaller value is chosen for better global FC voltages balancing.

In comparison to the CSVM the above solution slightly increases ripples of the FC voltages.

The second solution is used only in 4th region, where zero vectors are applied. It bases on assumption that only two phases are modulated and third phase is clamped in one of switching states: **0**, **1** or **2** during whole modulation period. As result only one zero vector is used in sampling period. This minimize switching losses, however they strongly depend on load power factor [44]. Therefore maximal reduction can be obtained, when peak of the phase current is located in the centre of clamped regions. It is necessary to observe the peak current position and select proper zero vector for this purpose. The peak current observer according to the Fig. 9 is realized by simple relation describing positive or negative peak of current polarity in each phase:

$$peak\ of\ current \begin{cases} positive\ when\ i_{Sa}i_{Sb}i_{Sc} > 0 \\ negative\ when\ i_{Sa}i_{Sb}i_{Sc} < 0 \end{cases} \tag{16}$$

If the peak of current is positive for pair $P1$ or $P2$, the zero vector **111** or **222** should be selected. If the peak of current is negative, the zero vector **000** or **111** should be selected, respectively. However, for low speed operation selection of **111** is associated with the FC's voltages change during almost whole sampling period as far as zero vector will be applied mainly. Regardless to the switching losses minimization, quality of the output voltage and as a consequence phase current is priority. Therefore, if the state **111** should be selected according to the peak current observer, the same calculation of zero vectors influence U_{FCx} values at the end of sampling period should be carried out as for the internal vectors pairs. The **111** zero vector with proper $P1$ or $P2$ pair can be chosen only if give smaller error between estimated and commanded FC voltage. In practice for low speed operation **111** is chosen only for high FC voltages unbalance. Final vectors selection in respect to peak of current and pair selection in sector 1 is shown in Table 5.

Figure 10 presents example of switching patterns in 2nd region for different switching states selected **1A** or **1B** as well as different pair selection $P1$ or $P2$ for all phases, respectively. Note that—the same as for the CSVM—next modulation

Table 5 Final vectors selection in sector 1

Selected pair	Peak of current	Region			
		1st	2nd	3rd	4th
$P1$	$i_{Sa}i_{Sb}i_{Sc} > 0$	**100**	**100**	**110**	**100**
		200	**110**	**210**	**110**
		210	**210**	**220**	**111**
	$i_{Sa}i_{Sb}i_{Sc} < 0$				**000**
					100
					110
$P2$	$i_{Sa}i_{Sb}i_{Sc} > 0$	**200**	**210**	**210**	**211**
		210	**211**	**220**	**221**
		221	**221**	**221**	**222**
	$i_{Sa}i_{Sb}i_{Sc} < 0$				**111**
					211
					221

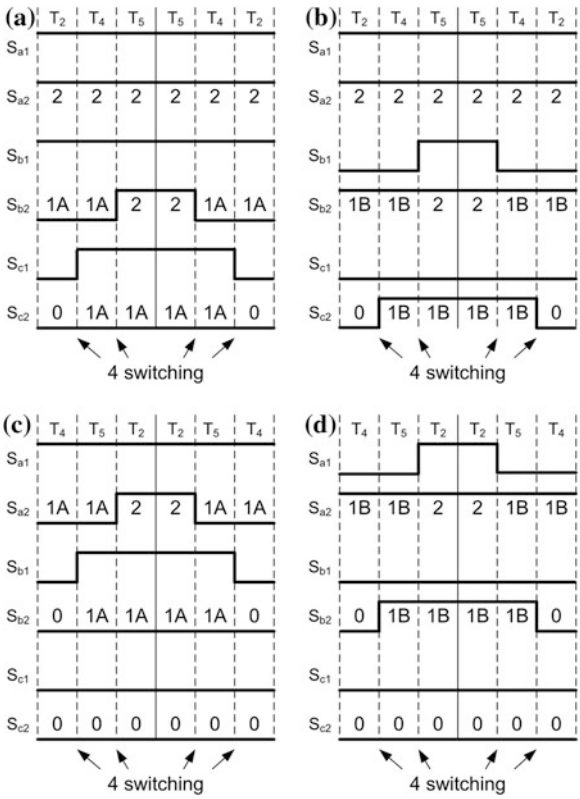

Fig. 10 Duty cycles for the 2nd region in sector 1: **a**, **c** for **1A** state selection in each phase, **b**, **d** for **1B** state selection in each phase, **a**, **b** for $P1$ pair selection, **c**, **d** for $P2$ pair selection

period can contain additional switching between sampling periods, when selected redundant state **1A** or **1B** is changed. Those additional switching can be divided into two groups:

Table 6 Theroretical number of switching in modulation period

Region number	CSVM	ASVM		Switching reduction		
		Typical	Maximum	Maximum (%)	Average (%)	Minimum (%)
1st	6	4	6	33.33	16.66	0.00
2nd	8	4	6	50.00	37.50	25.00
3rd	6	4	6	33.33	16.66	0.00
4th	12	4	6	66.66	58.33	50.00

- related with different switching states selection **1A** or **1B**, that can damage the converter—all switches are changing their state what can generate overvoltage,
- related with different pair selection $P1$ or $P2$, that mean normal operation of the converter—only two of four switches are changing their state.

To eliminate additional switching that can damage the converter and to provide better switching distribution between particular switches a modification of switching pattern introduced for the CSVM is used (see Fig. 4).

The ASVM provide number of switching reduction to 4 in all regions, however with additional switching as result different pair selection $P1$ or $P2$ number of switching can be increased to 7.

2.6 Space Vector Modulation Comparative Study

Table 6 shows theoretical comparison between the CSVM and the ASVM in respect to number or switching in modulation period. As it can be observed, highest reduction can be obtained in 4th region, which corresponds to low values of modulation index $M < 0.866$. For higher values of modulation index $M > 1$, reduction depends on the value of M due to different switching number reduction in region 2nd and regions 1st and 3rd. Thus, according to reference Space Vector $\boldsymbol{U}_{\boldsymbol{ref}}$ trajectory, in upper regions greater value of the M provides smaller total reduction of switching number. For modulation index $0.866 < M < 1$, reference Space Vector $\boldsymbol{U}_{\boldsymbol{ref}}$ crosses between 2nd and 4th region. Thus, in this operation region—the same as for $M > 1$—total reduction of switching number depends on M value—greater value of the M provides smaller total reduction. However, it can be assumed, that the ASD in traction application operates mainly in the low and high speed region. Thus, the further comparative study present operation of FCC for two different values of modulation index: $M < 0.866$ and $M > 1$.

Tables 7 and 8 shows THD factor of phase a stator current $THD(i_{Sa})$ and switching number reduction in simulation and experiment, respectively. In simulation, the calculation of switching number reduction is based on real, counted number of switching. In experiment, the calculation of switching number reduction is based on assumption that the changes of stator current THD (i_{Sa}) depends only on number of switching, and therefore shows how much the THD (i_{Sa}) is increased.

Table 7 Switching number reduction and stator current i_{Sa} THD factor $THD(i_{Sa})$ in CSVM and ASVM—simulation results

Modulation index	CSVM		ASVM		Switching reduction (%)
	$THD(i_{Sa})$ (%)	Switching	$THD(i_{Sa})$ (%)	Switching	
$M = 0.51$	0.96	3,000	2.08	1238	58.73
$M = 1.55$	1.28	507	1.93	336	33.73

Table 8 Switching number reduction and stator current i_{Sa} THD factor $THD(i_{Sa})$ in CSVM and ASVM—experimental results

Modulation index	CSVM $THD(i_{Sa})$ (%)	ASVM $THD(i_{Sa})$ (%)	Switching reduction (%)
$M = 0.51$	0.85	1.69	49.70
$M = 1.55$	1.45	2.15	32.56

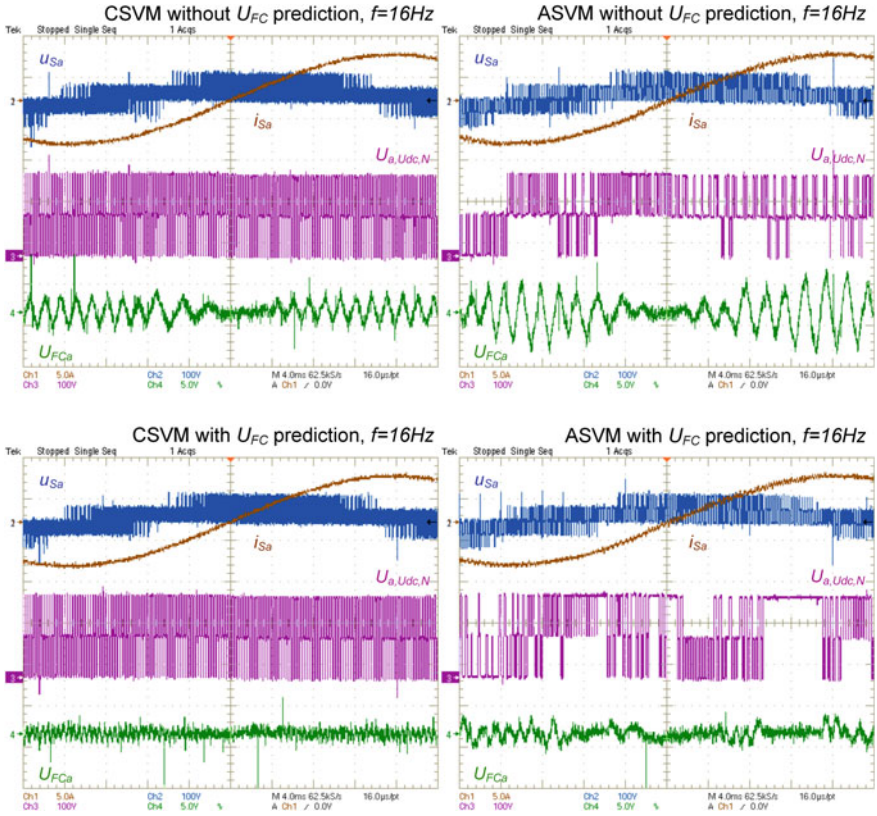

Fig. 11 Operation of the FCC (phase *a*) without and with the FC voltage prediction for the CSVM and the ASVM, output frequency $f = 16$ Hz (modulation index $M = 0.51$, 4th region): stator voltage u_{Sa} and current i_{Sa}, pole voltage $U_{a,UdcN}$ and AC component of FC voltage U_{FCa}

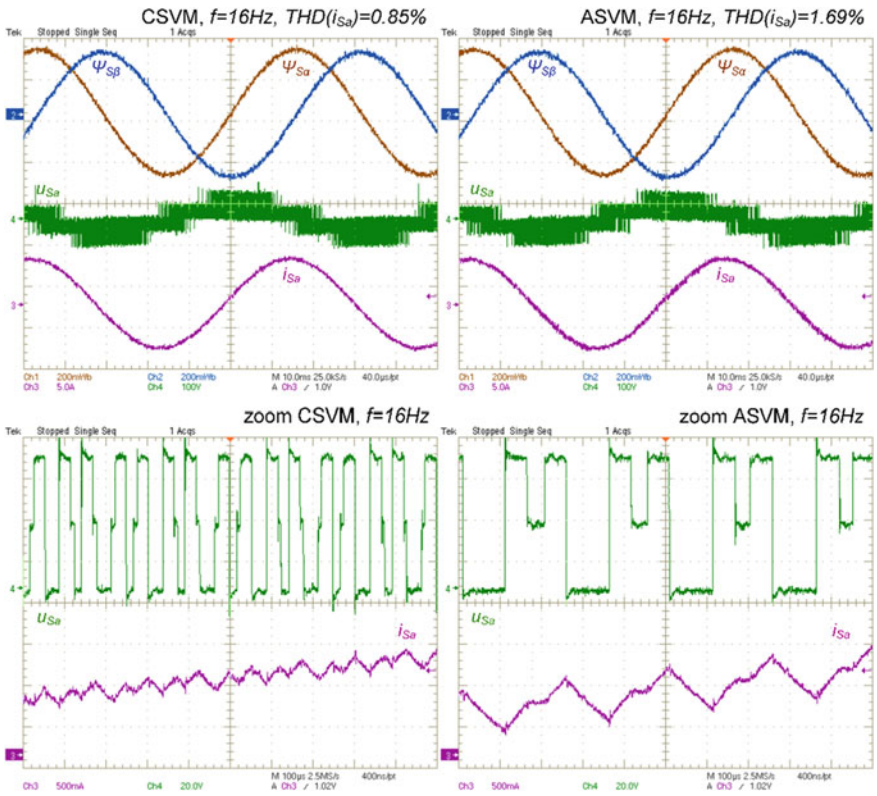

Fig. 12 Operation of the FCC (phase *a*) for the CSVM and the ASVM, output frequency $f = 16$ Hz (modulation index $M = 0.51$, 4th region): stator fluxes $\Psi_{S\alpha}$ and $\Psi_{S\beta}$, stator voltage u_{Sa} and current i_{Sa}, zoom of stator voltage u_{Sa} and current i_{Sa}

Average theoretical (58.33 %, Table 6) and simulation (58.33 %, Table 7) values of switching number reduction are the same for $M = 0.51$. The experimental value of switching number reduction (49.70 %, Table 8) is lower than the average theoretical however is equal minimum value of reduction in 4th region—50 %—what corresponds to the maximum number of 6 switching in ASVM. For $M = 1.51$, average theoretical value of switching number reduction depends on the reference Space Vector $\boldsymbol{U_{ref}}$ trajectory in 1st, 2nd and 3rd region. Therefore, the similar results for simulation (33.73 %, Table 7) and experimental (32.56 %, Table 8) are not equal to average theoretical value. However, for typical switching number values the maximum theoretical switching number reduction is 33.33 % in 1st and 3rd and 50.00 % in 2nd region, respectively. Thus, the simulation and experimental values of switching number reduction stays in possible range and are similar to the typical theoretical value (for $M = 1.51$ reference Space Vector $\boldsymbol{U_{ref}}$ trajectory largely lies in 1st and 3rd region).

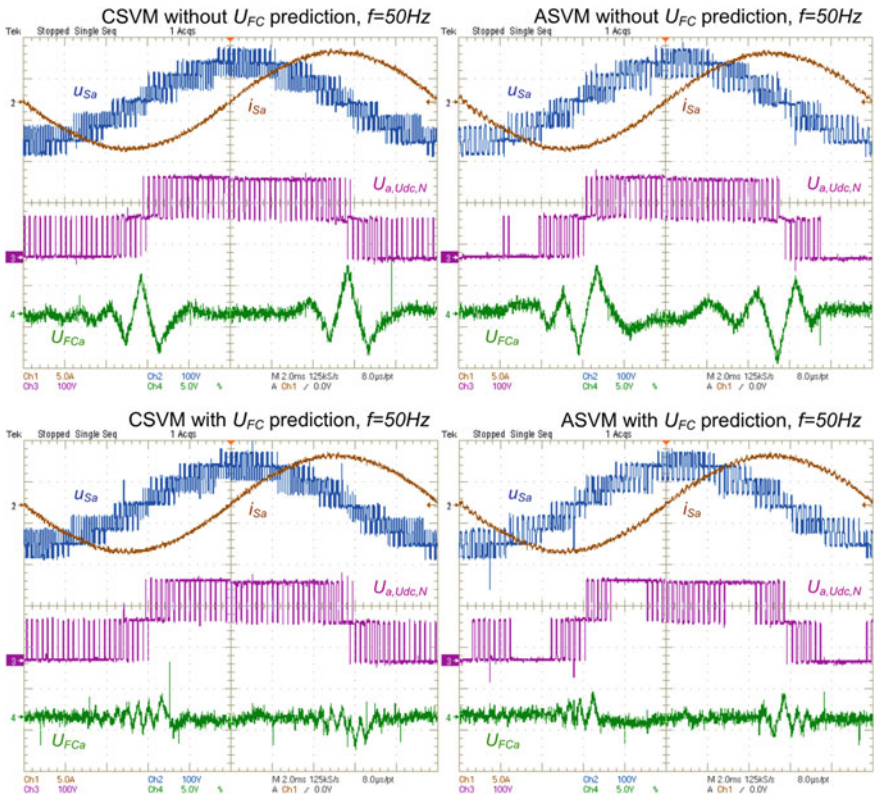

Fig. 13 Operation of the FCC (phase *a*) without and with the FC voltage prediction for the CSVM and the ASVM, output frequency $f = 50$ Hz (modulation index $M = 1.55$, 1st, 2nd and 3rd region): stator voltage u_{Sa} and current i_{Sa}, pole voltage $U_{a,UdcN}$ and AC component of FC voltage U_{FCa}

Figures 11 and 12 shows steady state operation of the FCC with CSVM and ASVM for the output frequency $f = 16$ Hz (modulation index $M = 0.51$, operation in 4th region).

Figure 11 presents the FCC operation without and with the FC voltage prediction U_{FCx}. As it can be observed on the AC component of FC voltage U_{FCa}, the FC voltage prediction provides significant ripples reduction. Also, Fig. 11 shows high reduction of the number of switching at the ASVM, which is visible on the pole voltage $U_{a,UdcN}$. However, this can be seen better on the zoom of stator voltage u_{Sa} and stator current i_{Sa} presented in Fig. 12. Figure 12 shows also that the modified SVM does not affect the estimated stator fluxes $\Psi_{S\alpha}$ and $\Psi_{S\beta}$.

Figures 13 and 14 shows—similarly to the previous one—steady state operation of the FCC with the CSVM and the ASVM for the output frequency $f = 50$ Hz (modulation index $M = 1.55$, operation in 1st, 2nd and 3rd region). In such conditions the reduction of the number of switching, which is visible on the

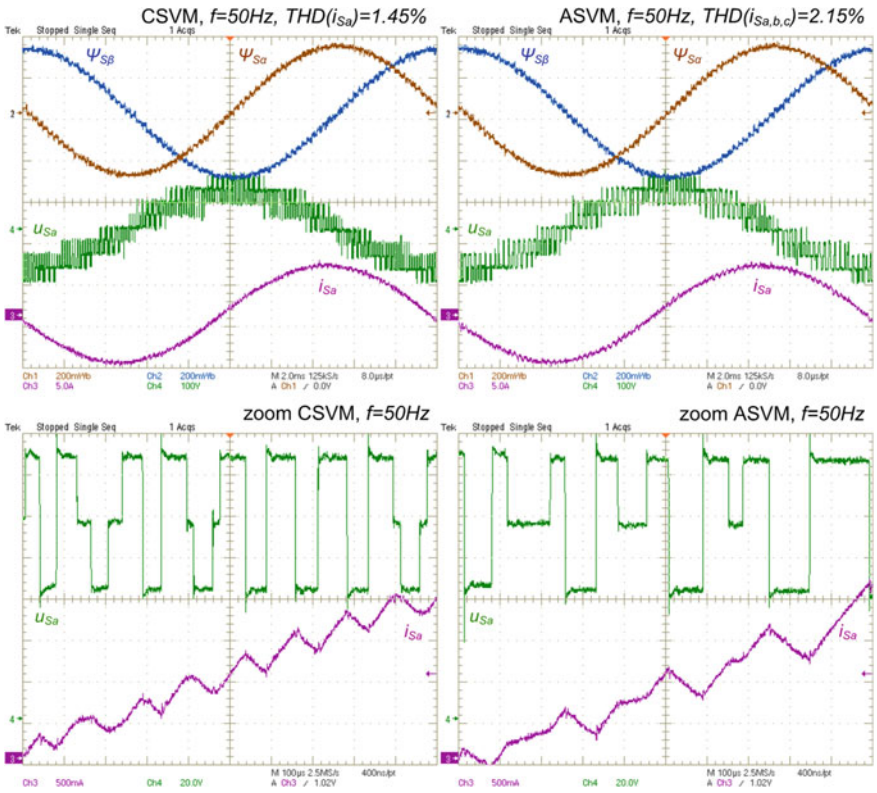

Fig. 14 Operation of the FCC (phase a) for the CSVM and the ASVM, output frequency $f = 50$ Hz (modulation index $M = 1.55$, 1st, 2nd and 3rd region): stator fluxes $\Psi_{S\alpha}$ and $\Psi_{S\beta}$, stator voltage u_{Sa} and current i_{Sa}, zoom of stator voltage u_{Sa} and current i_{Sa}

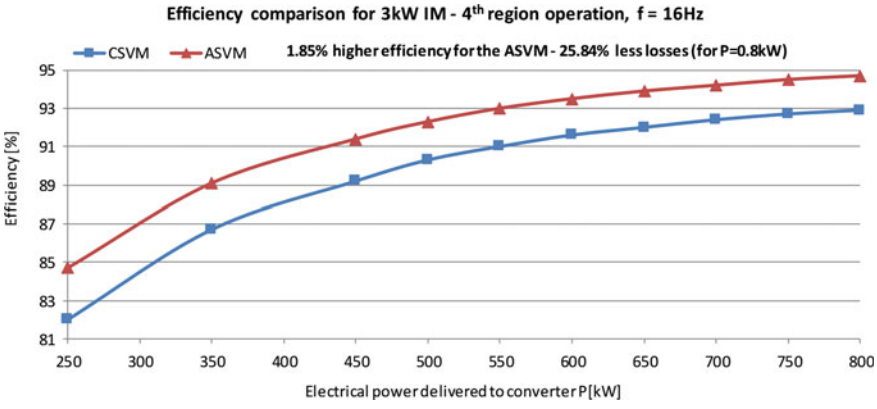

Fig. 15 The FCC efficiency comparison for the CSVM and the ASVM for 3 kW IM, output frequency $f = 16$ Hz (modulation index $M = 0.51$, 4th region)

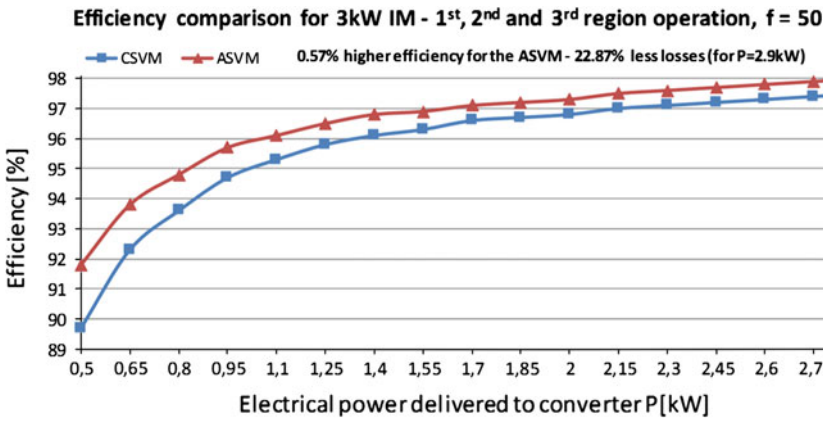

Fig. 16 The FCC efficiency comparison for the CSVM and the ASVM for 3 kW IM, output frequency $f = 50$ Hz (modulation index $M = 1.55$, 1st, 2nd and 3rd region)

pole voltage $U_{a,UdcN}$ is lower. However, similarly to previous case, the FC voltage prediction provides significant ripples reduction as well as the ASVM does not affect the estimated stator fluxes $\Psi_{S\alpha}$ and $\Psi_{S\beta}$.

Figure 15 presents the FCC efficiency comparison for the CSVM and the ASVM modulation with the 3 kW IM drive. For the FCC operation in 4th region, total efficiency of the converter (including not only switching losses) with the ASVM is 1.85 % higher than for the CSVM. It means that the FCC losses for the nominal load are reduced approximately 26 %.

Figure 16 presents the FCC efficiency comparison for the CSVM and the ASVM modulation with the 3 kW IM drive. For the operation in regions 1st, 2nd and 3rd profit of the ASVM is lower. The total efficiency of the converter with the ASVM is 0.57 % higher than for the CSVM, with the FCC losses lower for the nominal load approximately 23 %.

3 Compensation of Dead-Time Effect and Semiconductor Devices Voltage Drop

3.1 Introduction

The IGBT devices has finite switching time and they are turning off much more slower than turning on, therefore there is needed a delay in control signals between

complementary switching devices (so-called dead-time t_{DT}) in order to prevent a short-circuit across the converter voltage sources. Depending on the sign of stator current i_{Sx}, dead-time can increase or decrease the amplitude of the output voltage amplitude applied to the converter in comparison to the reference Space Vector $\boldsymbol{U}_{ref}$, and in result stator current i_{Sx} is distorted.

The voltage drop on semiconductor devices is second nonlinearity that has significant impact on the amplitude of output voltage applied to the converter. Similarly to the dead-time effect, it can increase or decrease the amplitude of reference output voltage applied to the converter, depending on the sign of stator current i_{Sx} and in result distorts the stator current i_{Sx}. However, contrary to the dead-time depends not only on the ratio of the dead-time t_{DT} of the sampling time T_S, but also on the amplitude of the stator current i_{Sx}.

It is obvious, that frequency and amplitude of reference Space Vector $\boldsymbol{U}_{ref}$ significantly depend on reference speed of the drive. Thus, for the low speed operation the amplitude of reference Space Vector U_{ref} is also low. Therefore, in low speed operation the dead-time as well as the voltage drop on semiconductor devices has significant impact on stator current i_{Sx} on the output voltage amplitude applied to the converter due to the distortion introduced by the them is relative large to the amplitude of reference Space Vector U_{ref}. For high speed operation the distortion introduced by the them is relative small and their impact on stator current i_{Sx} is negligible. To avoid that, the dead-time effect as well as the voltage drop on semiconductor devices compensation algorithms are used. The semiconductor devices voltage drop and dead-time impact on phase current distortion have been well investigated for the two-level as well multilevel converters. These methods can be divided into two groups:

- modification of amplitude (length) of reference Space Vector $\boldsymbol{U}_{ref}$ [33, 46, 47, 50],
- modification of the duty cycles at the output of the PWM modulator [33, 46, 48, 49].

3.2 Compensation of Dead-Time Effect

Figure 17 presents the dead-time t_{DT} impact on the pole voltage $U_{x,UdcN}$ applied to the converter, depending on the stator current i_{Sx} polarity. The dead-time effect does not depend on the amplitude of the stator current i_{Sx}, only on the sampling time T_S and the amplitude of the DC-link voltage U_{DC}. However, it should be noticed, that for multilevel converter the dead-time effect on the output voltage amplitude applied to the converter is increased in comparison to the two-level converter due to increased number of switching. However, the impact of dead-time in multilevel converter depends on type of applied modulation technique. In case of three-level VSC with the CSVM in comparison to the two-level VSC is doubled. For the ASVM, where the number of switching is reduced the dead-time effect is similar to the two-level VSC.

Thus, in first step the stator voltage error δu_{Sx} should be calculated for single switching device of the n-level converter [50]:

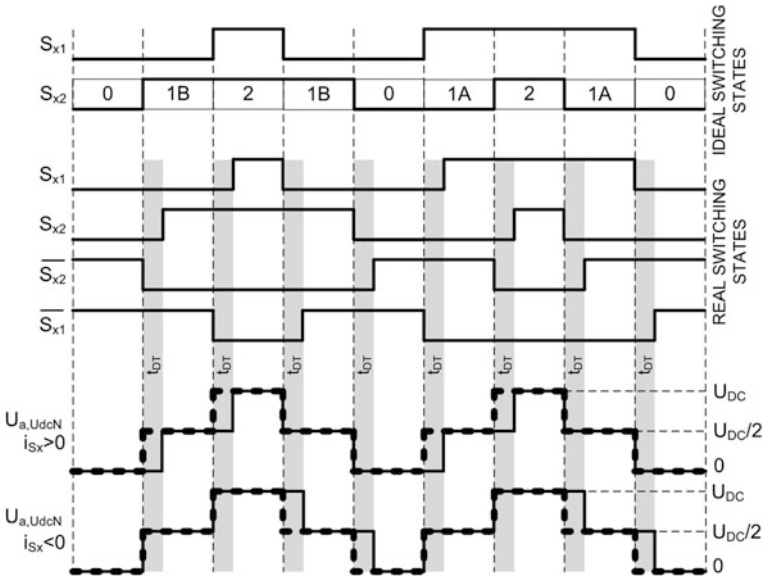

Fig. 17 Dead-time effect impact on the pole voltage $U_{a,UdcN}$ applied to the converter depending on the stator current i_{Sx} polarity—ideal (*solid line*) and real (*dotted line*) output pole voltage $U_{a,UdcN}$

$$\delta u_{Sx} = \frac{U_{DC} t_{DT}}{(n-1)T_S} sgn(i_{Sx}) \tag{17}$$

where sign of stator current i_{Sx} is defined as:

$$sgn(i_{Sx}) \begin{cases} 1 \ \ for \ i_{Sx} > 0 \\ -1 \ for \ \ i_{Sx} < 0 \end{cases} \tag{18}$$

In next step, depending on the type of applied modulation, the total stator voltage error $\Sigma \delta u_{Sx}$ should be calculated for each leg:

$$\sum \delta u_{Sx} = k \delta u_{Sx} \tag{19}$$

where k factor denotes number of switching per phase, e.g. typically for CSVM $k = 2$ and for ASVM $k = 1$. From (17) it can be noticed that changes of the sampling time T_S has significant influence on the dead-time effect, as far as the DC-link voltage U_{DC} and dead-time t_{DT} is assumed to be constant. Dead-time effect—understood as ratio of the phase voltage error to the reference output voltage—increases linearly with increasing of the switching frequency.

One of important aspects related to the dead-time effect compensation is proper calculation of stator current i_{Sx} zero crossing. If stator current i_{Sx} polarity is not calculated properly, inadequate compensation can worse the shape of i_{Sx}. Quality of the stator current i_{Sx} polarity calculation depends on the measurement noise level as well as on the control delays. To improve $sgn(i_{Sx})$ calculation two solutions can be

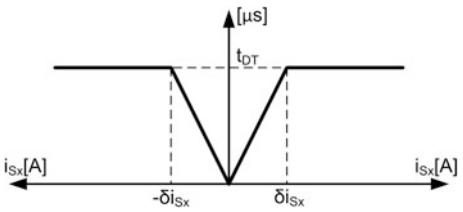

Fig. 18 Dead-time t_{DT} value limiting in assumed range δi_{Sx} of stator current i_{Sx}

used. First uses simple current estimation based on current difference which allow to eliminate one sampling control delay. Second solution uses hysteresis regulator on the estimated current to obtain $sgn(i_{Sx})$ with hysteresis width equal to measurement noise level. Taking into account that both solutions does not provide exact phase current zero crossing, total stator voltage error $\Sigma\delta u_{Sx}$ or dead-time t_{DT} should be linearly limited in assumed range of phase current i_{Sx} (Fig. 18). In industrial applications the value of δi_{Sx} is set experimentally, as far as it depends on the measurement noise level as well as on the control delays.

As it was aforementioned, the compensation of the dead-time can be realized by modification of amplitude (length) of reference Space Vector $\boldsymbol{U_{ref}}$ or by modification of the duty cycles at the output of the PWM modulator. For the dead-time effect it is recommended to use second solution. Such approach allows to decrease number of calculations due to omitting the precalculation, which switches will be modulated in sampling period. Only for each switch the switching time is increased or decreased according to Fig. 18.

3.3 Compensation of Semiconductor Devices Voltage Drop

Figure 19 presents the stator current i_{Sx} flow (bold line) in single leg of the FCC for different switching states. As it can be observed, semiconductors devices voltage drop does not only depend on the selected switching state, but also on the phase current polarity. Table 9 shows the desired $U_{x,UdcN,ref}$ and the real pole voltage $U_{x,UdcN}$ produced for all possible switching states and different direction of the current flow. The $u_{fD,x}$ denotes the voltage drop on the freewheling diodes and $u_{CEon,x}$ denotes the voltage drop on the conducting IGBT during ON state.

Contrary to the dead-time effect, the voltage drop on semiconductor devices depends not only on the changes of the sampling time but also on the amplitude of the phase currents. Figure 20 presents example of voltage drop characteristics of the IRG4BC20UDPBF IGBT transistor, according to the International Rectifier datasheet [51]. As it can be observed on the $u_{fD,x}$ and the $u_{CEon,x}$ characteristics are strongly nonlinear functions of stator current i_{Sx}. Thus, contrary to the dead-time effect, the voltage drop on semiconductor devices depends not only on the changes of the sampling time but also on the amplitude of the phase currents. Therefore, two-straight-line approximation for each characteristic should be used (see Fig. 21). The first approximation is assumed as a linear resistance for relatively

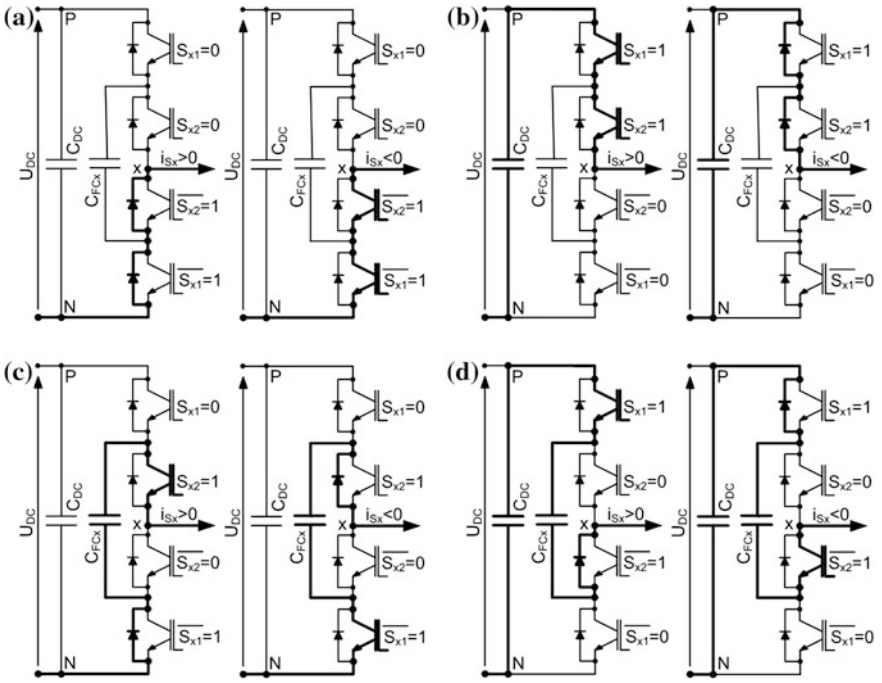

Fig. 19 Stator current i_{Sx} flow (bold line) in single leg of the FCC for different switching states: **a 0** switching state, **b 2** switching state, **c 1A** switching state, **d 1B** switching state

Table 9 The desired $U_{x,UdcN,ref}$ and real pole voltage $U_{x,UdcN}$ for different conditions

Switching states	Pole voltage		
	$U_{x,UdcN,ref}$	$U_{x,UdcN}$ for $i_{Sx} > 0$	$U_{x,UdcN}$ for $i_{Sx} < 0$
0	0	$U_{x,UdcN,ref} - 2u_{fD,x}$	$U_{x,UdcN,ref} + 2u_{CEon,x}$
1A	U_{FCx}	$U_{x,UdcN,ref} - u_{fD,x} - u_{CEon,x}$	$U_{x,UdcN,ref} + u_{fD,x} + u_{CEon,x}$
1B	$U_{DC} - U_{FCx}$	$U_{x,UdcN,ref} - u_{fD,x} - u_{CEon,x}$	$U_{x,UdcN,ref} + u_{fD,x} + u_{CEon,x}$
2	U_{DC}	$U_{x,UdcN,ref} - 2u_{CEon,x}$	$U_{x,UdcN,ref} + 2u_{fD,x}$

low stator currents. The second approximation is assumed as a constant voltage drop with an incremental resistance for higher stator currents.

Similarly to presented dead-time t_{DT} value limitation in assumed range δi_{Sx} of stator current (see Fig. 18), the dual slope of approximated characteristics reduces the amount of voltage drop to be compensated around the current zero crossing. Thus, voltage drop on switching devices compensation is prevented against overcompensation.

Figure 22 shows example of sector 1 with the ideal and real vectors location. For each vector and six different current directions, six different voltage drop errors can be specified (white dots). Note that single current polarity shifts all

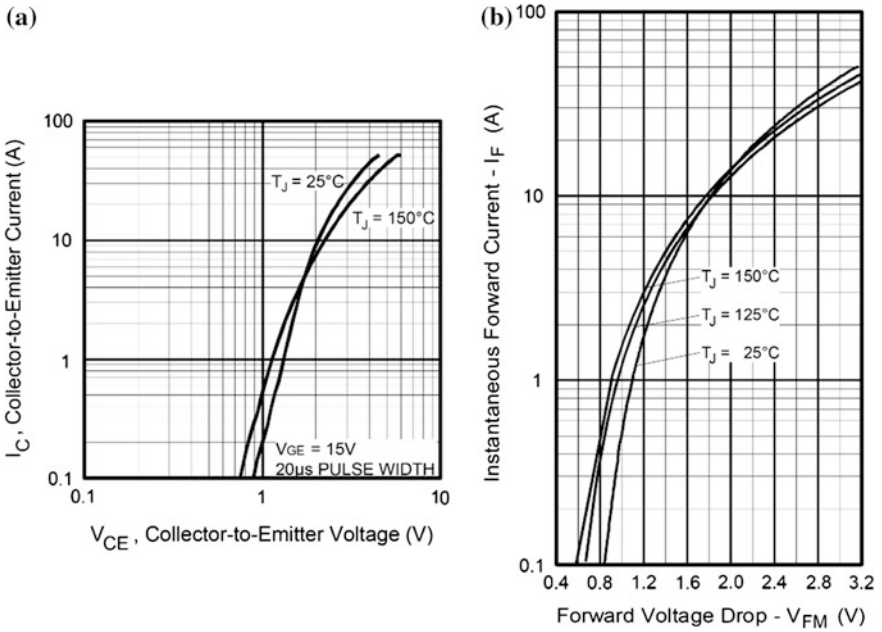

Fig. 20 Voltage drop characteristics of the IRG4BC20UDPBF IGBT [51]: **a** on the IGBT during ON state, **b** on the freewheeling diode

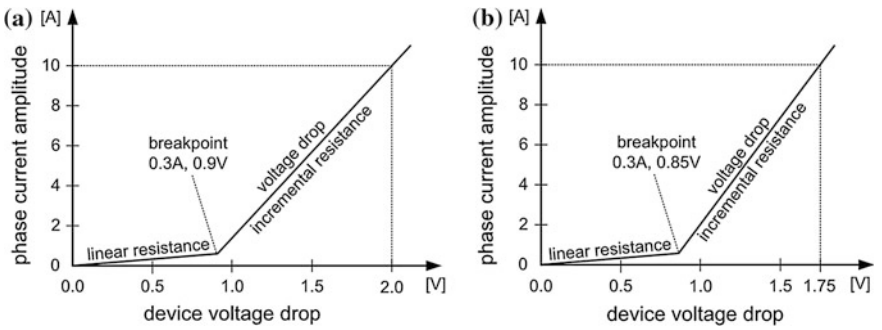

Fig. 21 Linearized voltage drop characteristics of the IRG4BC20UDPBF IGBT: **a** on the IGBT during ON state, **b** on the freewheeling diode

vectors location in the same direction, regardless of the voltage drop error amplitude [51]. It means also that redundant vectors $\mathbf{V_4}$ and $\mathbf{V_5}$ can generate two different semiconductor devices voltage drop values as well as zero vector $\mathbf{V_0}$ can generate three different values of voltage drop (in the one of six positions of voltage drop two or three white dots, respectively). For example, for each of $\mathbf{V_5}$ redundant states **110** and **221** the amplitude of the ideal pole voltage $U_{x,UdcN,ref}$ is the same, but for each of them currents flow through different semiconductor

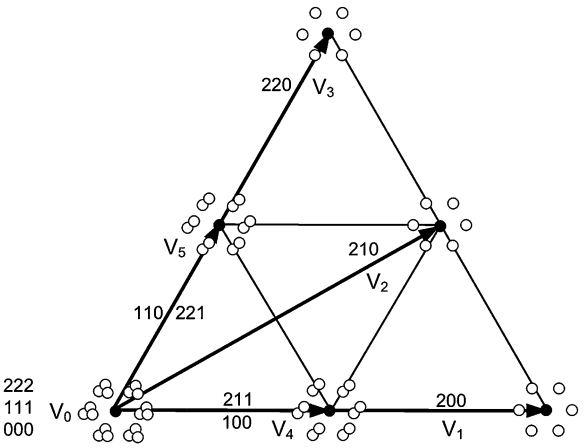

Fig. 22 Ideal and real (taking into account semiconductor devices voltage drop) vectors location in sector 1—*black* and *white dots*, respectively

devices and as consequence, for each summary voltage drop is different. Therefore, to compensate voltage drop on semiconductor devices, the calculated value of voltage drop should be added to the reference stator voltages.

According to the Clarke transformation, three-phase system without neutral wire can be transformed from natural *abc* to stationary $\alpha\beta$ coordinates. As far as the voltage drop on semiconductor devices introduced by all legs of the VSC is nonlinear, it does not fulfil following condition:

$$u_{VDa} + u_{VDb} + u_{VDc} = 0 \tag{20}$$

where u_{VDx} denotes summary voltage drop in leg x. Therefore, to obtain reference converter output voltages in stationary $\alpha\beta$ coordinates: $u_{\alpha,ref}$ and $u_{\beta,ref}$, respectively, with voltage drop compensation, the full Clarke transformation has to be used:

$$\begin{bmatrix} u_{\alpha,ref} \\ u_{\beta,ref} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} u_{a,ref} + u_{VDa} \\ u_{b,ref} + u_{VDb} \\ u_{c,ref} + u_{VDc} \end{bmatrix} \tag{21}$$

Thanks to that, vector plane will be shifted to the position, where the real vectors location coincides with ideal position [51].

3.4 Results of Low Speed Operation of Adjustable Speed Drive

Figures 23 and 24 presents compensation of dead-time effect and voltage drop on semiconductor devices for the CSVM and the ASVM modulation in leg *a* for a low speed operation.

Reference output frequency is 3 Hz. Without compensations, for both CSVM and ASVM stator current i_{Sa} is strongly distorted (see Figs. 23a and 24a).

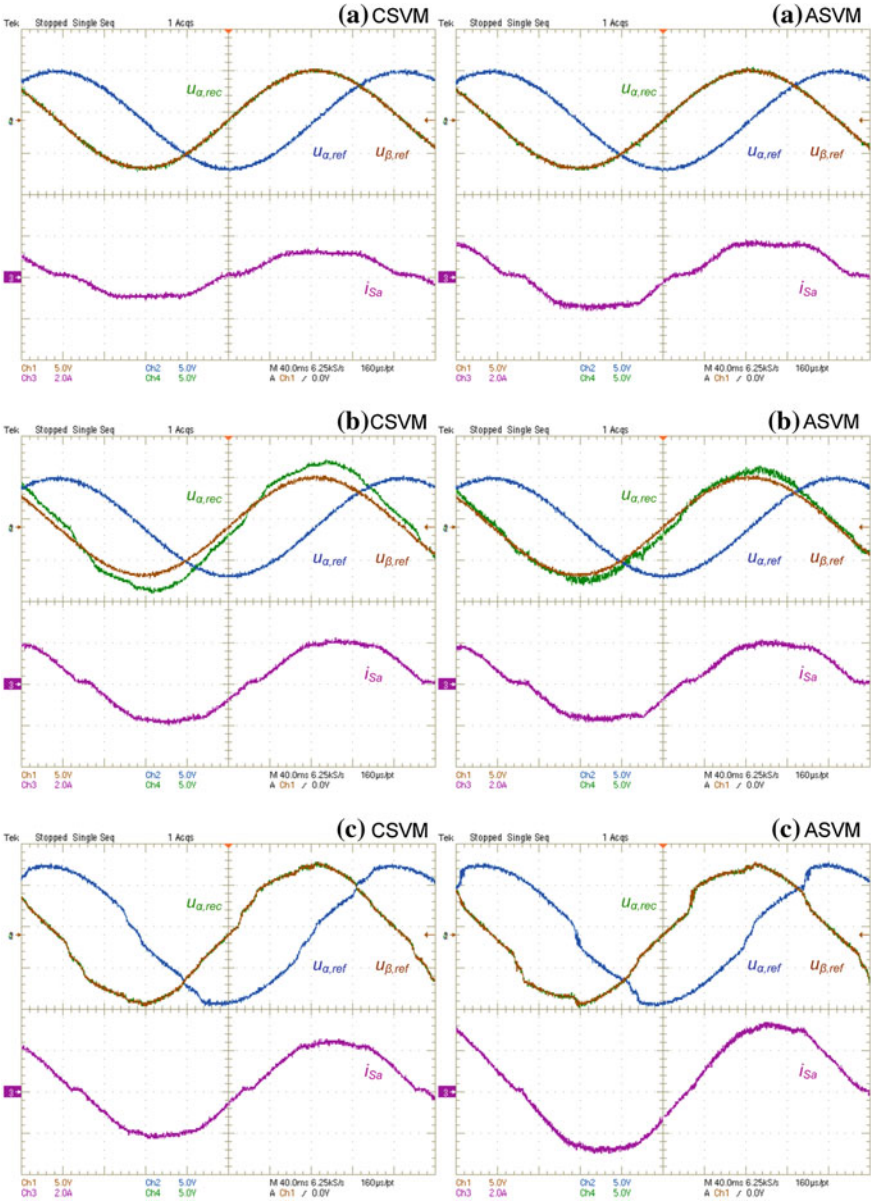

Fig. 23 Dead-time effect compensation for the CSVM and the ASVM, output frequency $f = 3$ Hz: **a** no compensation, **b** dead-time effect compensation, **c** voltage drop effect compensation. From the *top*: converter reference voltage $u_{\alpha,ref}$ and $u_{\beta,ref}$ in $\alpha\beta$ coordinates, $u_{\alpha,rec}$ which is reconstructed from switching states $u_{\alpha,ref}$ and phase a stator current i_{Sa}

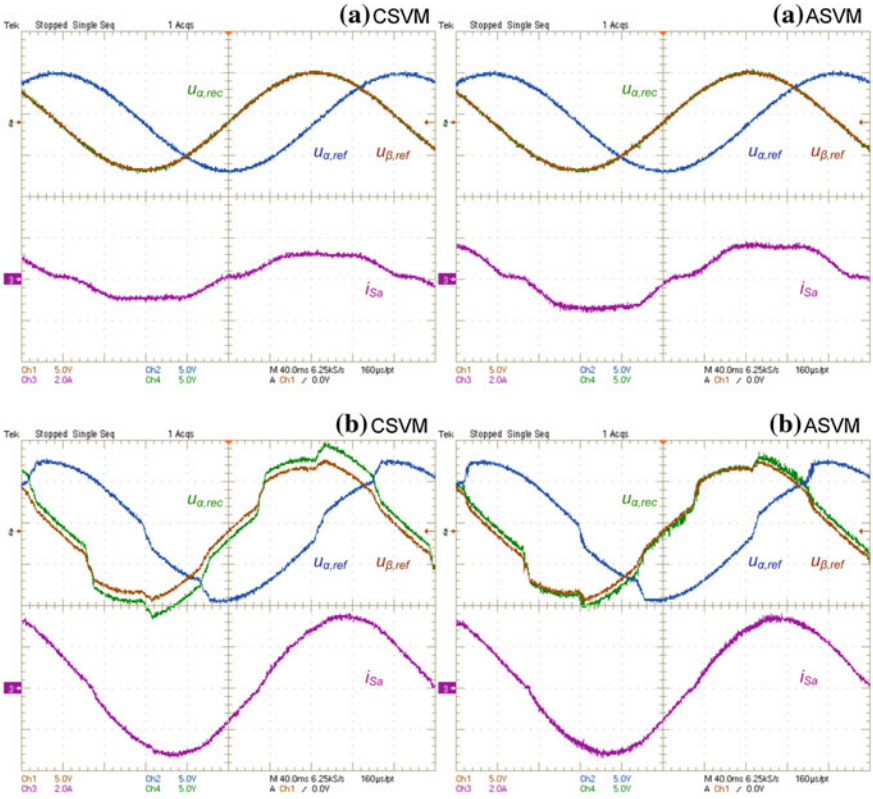

Fig. 24 Dead-time effect compensation for the CSVM and the ASVM, output frequency $f = 3$ Hz: **a** no compensation, **b** dead time and voltage drop effect compensation. From the *top*: converter reference voltage $u_{\alpha,ref}$ and $u_{\beta,ref}$ in $\alpha\beta$ coordinates, $u_{\alpha,rec}$ which is reconstructed from switching states $u_{\alpha,ref}$ and phase a stator current i_{Sa}

However, for the CSVM amplitude of i_{Sa} is lower. It is caused by increased dead-time effect for the CSVM, due to higher number of switching.

The dead-time compensation is realized on the output of the modulator—thus, converter reference voltages in $\alpha\beta$ coordinates $u_{\alpha,ref}$ and $u_{\beta,ref}$ are not modified. The influence of the Dead Time effect compensation can be observed on Fig. 23b, where the $u_{\alpha,rec}$ voltage is shown. The $u_{\alpha,rec}$ is the output converter voltage reconstructed from the switching states of $u_{\alpha,ref}$, and contains the dead-time effect compensation signal. As it can be observed on Fig. 23b, for the CSVM, the amplitude of the $u_{\alpha,rec}$ is higher than for the ASVM modulation. It means that the higher number of switching must be compensated.

From other hand, the voltage drop on semiconductor devices compensation signal is added directly to the $u_{\alpha,ref}$ and $u_{\beta,ref}$ reference voltages (see Fig. 23c), where for both modulation techniques voltage drop effect is similar. It manifests itself in the same amplitude of $u_{\alpha,ref}$ and $u_{\beta,ref}$ reference voltages, regardless of the type of SVM.

Figures 23c and 24b shows operation of the both compensation algorithms applied to the converter.

4 Space Vector Overmodulation in Flying Capacitor Converter

The SVM generates sinusoidal output voltages, when the trajectory of the reference Space Vector $\boldsymbol{U_{ref}}$ traces a circle inscribed into the hexagon. According to the modulation index definition (4) for the three-level VSC:

$$M = \frac{\pi U_{ref}}{U_{DC}} \tag{22}$$

where $M = 2$ for the square wave operation (six step mode) of the VSC. Thus, the trajectory of the reference Space Vector $\boldsymbol{U_{ref}}$ traces a circle inscribed into the hexagon when $M = \sqrt{3}$, which corresponds to the height of an equilateral triangle with the length of the side equal 2. As far as the external vectors generates output voltage amplitude equal $2/3U_{DC}$ for the sinusoidal output voltage generation the maximum length of the Space Vector is:

$$U_{ref,max} = \frac{\sqrt{3}U_{ref}}{3} \tag{23}$$

Therefore, for linear operation the modulation index value is limited to:

$$M = \frac{\pi U_{ref,max}}{U_{DC}} = \frac{\sqrt{3}\pi}{3} \cong 1.814 \tag{24}$$

Above $M = 1.814$ the inverter output voltage is distorted, and the magnitude of output voltage becomes smaller than the reference output voltage. For demanding ASD high speed operation over the linear range ($M > 1.814$) of the converter is very often required. However, when output voltage does not correspond to the reference value, drive cannot work properly due to decreased stator flux amplitude. The SVM high speed operation over the linear range of the converter is possible thanks to the Space Vector Overmodulation algorithm. For the Space Vector Overmodulation output voltage and phase current is distorted, however the amplitude of first harmonic of the output voltage is equal to the reference output voltage. Thus, the Space Vector Overmodulation make possible to maximize stator flux. However, it should be noticed that for the six step operation, Flying Capacitor voltages cannot be controlled because switching states **1A** and **1B** are not used.

The Space Vector Overmodulation bases on the proper modification of the Space Vector length and angle, when the trajectory of the reference Space Vector lies partly outside a circle inscribed into the hexagon. Based upon the degree of

output voltage distortion, for the Space Vector Overmodulation two modes can be defined [13, 21, 24, 53–55]:

- Space Vector Overmodulation mode I—where the output voltage is distorted continuous reference output voltage,
- Space Vector Overmodulation mode II—where the output voltage is distorted discontinuous reference output voltage.

4.1 Space Vector Overmodulation Mode I

In the Space Vector Overmodulation mode I, the SVM algorithm changes the magnitude of the reference Space Vector $\boldsymbol{U_{ref}}$, while the angle of Space Vector Θ_m is not changed. Figure 25 presents the trajectory of the reference and compensated (boosted) Space Vector $\boldsymbol{U^*_{ref}}$ in stationary $\alpha\beta$ coordinates.

For a given $\boldsymbol{U_{ref}}$ the output phase voltage waveform can be divided into four segments, depending on the Θ_r angle [54] The Θ_r angle denotes a reference angle of the insertion of the compensated Space Vector $\boldsymbol{U^*_{ref}}$ trajectory. The output voltage equations in each segment are expressed as:

$$f_1 = \frac{U_{DC}}{\sqrt{3}} \tan \Theta_m \text{for } 0 \lesssim \Theta_m < \left(\frac{\pi}{6} - \Theta_r\right) \tag{25}$$

$$f_2 = \frac{U_{DC}}{\sqrt{3}\cos\left(\frac{\pi}{6} - \Theta_r\right)} \sin \Theta_m \quad \text{for} \quad \left(\frac{\pi}{6} - \Theta_r\right) \lesssim \Theta_m < \left(\frac{\pi}{6} + \Theta_r\right) \tag{26}$$

$$f_3 = \frac{U_{DC}}{\sqrt{3}\cos\left(\frac{\pi}{3} - \Theta_r\right)} \sin \Theta_m \quad \text{for} \quad \left(\frac{\pi}{6} + \Theta_r\right) \lesssim \Theta_m < \left(\frac{\pi}{2} - \Theta_r\right) \tag{27}$$

$$f_4 = \frac{U_{DC}}{\sqrt{3}\cos\left(\frac{\pi}{6} - \Theta_r\right)} \sin \Theta_m \quad \text{for} \quad \left(\frac{\pi}{2} - \Theta_r\right) \lesssim \Theta_m < \frac{\pi}{2} \tag{28}$$

Expanding (25, 26, 27 and 28) in a Fourier series and taking only the fundamental component into consideration, the resultant equation can be expressed as [54]:

$$F(\Theta_r) = \frac{\pi}{4}\left[\int_A f_1 \sin \Theta d\Theta + \int_B f_2 \sin \Theta d\Theta + \int_C f_3 \sin \Theta d\Theta + \int_D f_4 \sin \Theta d\Theta\right] \tag{29}$$

where A, B, C and D denote integral ranges of each voltage function f_1, f_2, f_3, and f_4, respectively. Since $F(\Theta_r)$ represents the peak value of the fundamental component, the $F(\Theta_r)$ according to the definition of the modulation index (4) can be expressed as:

$$F(\Theta_r) = \frac{2}{\pi} U_{DC} M \tag{30}$$

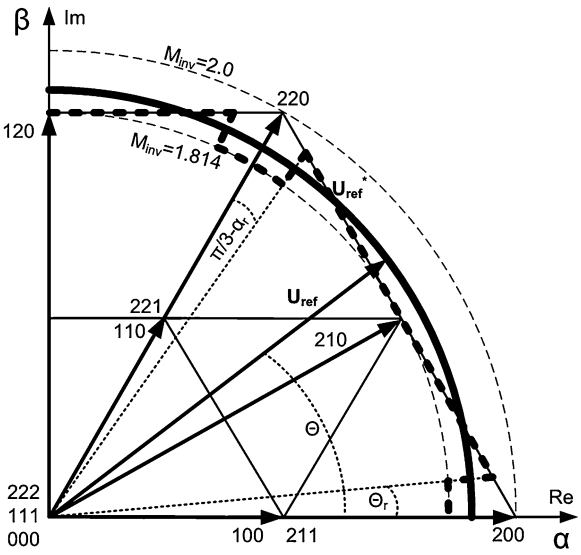

Fig. 25 Reference $\boldsymbol{U_{ref}}$ (*solid bold line*) and compensated $\boldsymbol{U_{ref}^*}$ (*dotted bold line*) trajectory of Space Vector in the Space Vector Overmodulation mode I

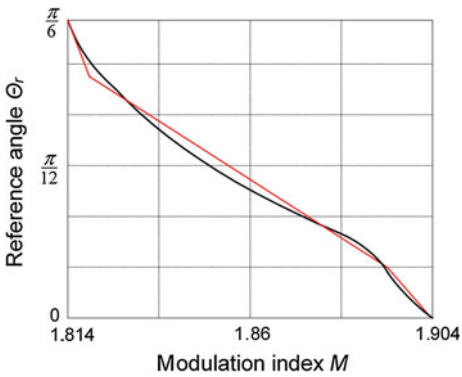

Fig. 26 Reference angle Θ_r versus modulation index M and linearization of $\Theta_r = f(M)$

Thus, combining the (22) with the (29) a relationship between modulation index and the angle can be determined, which gives a linearity of the reference output voltage. Because of strong nonlinearity, the linearization of (30) function was proposed [53, 54]:

$$\Theta_r \begin{cases} 30^\circ \div 24.5^\circ & \Leftrightarrow \quad M \in \langle 1.814, 1.818 \rangle \\ 24.5^\circ \div 5.5^\circ & \Leftrightarrow \quad M \in \langle 1.818, 1.896 \rangle \\ 5.5^\circ \div 0^\circ & \Leftrightarrow \quad M \in \langle 1.896, 1.904 \rangle \end{cases} \tag{31}$$

Figure 26 presents the Θ_r angle versus the modulation index.
For a given angle of the reference Space Vector $\boldsymbol{U_{ref}}$:

$$\Theta_m \in \langle \Theta_r, \frac{\pi}{3} - \Theta_r \rangle \tag{32}$$

only two vectors are used: external and middle vector. For the (22) magnitude of the reference Space Vector it changed. Thus, small modulation indexes have to be calculated as follows, where the sum of the m_1 and m_2 is always equal 2:

$$m_1 = 2\frac{\sqrt{3}\cos\Theta_m - \sin\Theta_m}{\sqrt{3}\cos\Theta_m + \sin\Theta_m} \tag{33}$$

$$m_2 = 2 - m_1 \tag{34}$$

Outside of the region (32) the magnitude of the reference Space Vector it not changed. Thus, the CSVM or ASVM modulation is applied. From the Fig. 26 it is obvious, that for the Space Vector Overmodulation mode I, modulation index M limit is 1.904. When $M > 1.904$, the Space Vector Overmodulation mode II should be applied.

4.2 Space Vector Overmodulation Mode II

In the Space Vector Overmodulation mode II, the SVM algorithm changes the magnitude and the angle of the reference Space Vector $\boldsymbol{U_{ref}}$. When the $\boldsymbol{U_{ref}}$ enters to the sector, the compensated Space Vector $\boldsymbol{U^*_{ref}}$ is held at a vertex for particular time. The time, in which compensated Space vector $\boldsymbol{U^*_{ref}}$ remains at the vertices is determined by the holding angle Θ_h. When the reference $\boldsymbol{U_{ref}}$ crosses the holding angle Θ_h, compensated Space Vector $\boldsymbol{U^*_{ref}}$ speeds up and moves along the side of hexagon. For the angle of the reference Space Vector $\Theta_m = \pi/6$, accelerated compensated Space Vector $\boldsymbol{U^*_{ref}}$ catches up reference $\boldsymbol{U_{ref}}$. When the reference Space Vector $\boldsymbol{U_{ref}}$ crosses the holding angle $\Theta_m = \pi/6 - \Theta_h$, the compensated Space Vector $\boldsymbol{U^*_{ref}}$arrives to the next vertex. Figure 27 presents the trajectory of the reference $\boldsymbol{U_{ref}}$ and compensated Space Vector $\boldsymbol{U^*_{ref}}$ in stationary $\alpha\beta$ coordinates.

Similarly to the Space Vector Overmodulation mode I, for a given reference Space Vector, the output phase voltage waveform can be divided into four segments, depending on the Θ_h angle [54]. The output voltage equations in each segment are expressed as:

$$f_1 = \frac{U_{DC}}{\sqrt{3}}\tan\Theta_p \quad \text{for} \quad 0 \lesssim \Theta_m < \left(\frac{\pi}{6} - \Theta_h\right) \tag{35}$$

$$f_2 = \frac{U_{DC}}{3} \quad \text{for} \quad \left(\frac{\pi}{6} - \Theta_h\right) \lesssim \Theta_m < \left(\frac{\pi}{6} + \Theta_h\right) \tag{36}$$

$$f_3 = \frac{U_{DC}}{\sqrt{3}\cos\left(\frac{\pi}{3} - \Theta'_p\right)}\sin\Theta'_p \text{for} \left(\frac{\pi}{6} + \Theta_h\right) \lesssim \Theta_m < \left(\frac{\pi}{2} - \Theta_h\right) \tag{37}$$

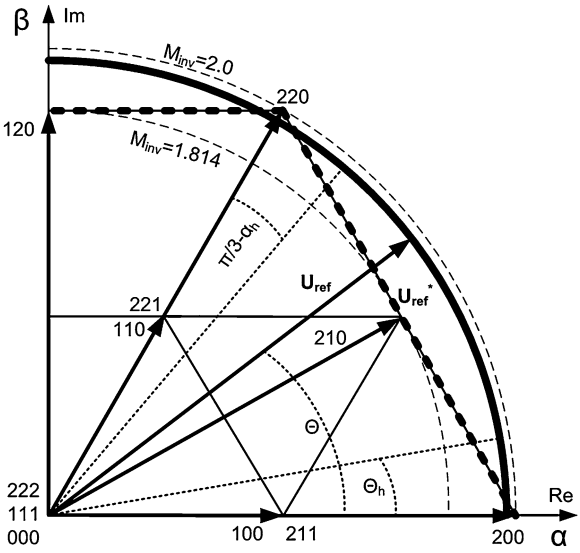

Fig. 27 Reference $\boldsymbol{U_{ref}}$ (*solid bold line*) and compensated $\boldsymbol{U_{ref}^*}$ (*dotted bold line*) trajectory of space vector in the space vector overmodulation mode II

$$f_4 = \frac{2U_{DC}}{3} \text{for} \left(\frac{\pi}{2} - \Theta_h\right) \lesssim \Theta_m < \frac{\pi}{2} \tag{38}$$

where:

$$\Theta_p = \frac{\Theta_m}{1 - \frac{\pi}{6}\Theta_h} \tag{39}$$

$$\Theta_p^{'} = \Theta_p - \frac{\pi}{6} \tag{40}$$

are angles of compensated Space Vector $\boldsymbol{U_{ref}^*}$ for $0 \leq \Theta_m < (\pi/6 - \Theta_h)$ and $(\pi/6 - \Theta_h) \leq \Theta_m < (\pi/3)$, respectively.

Similarly to the Space Vector Overmodulation mode I, substituting (35, 36, 37 and 38) into (29), the $F(\Theta_h)$ according to (22) can be expressed as:

$$F(\Theta_h) = \frac{2}{\pi} U_{DC} M \tag{41}$$

Figure 28 presents the Θ_h angle versus the modulation index. Because of strong nonlinearity, the linearization of (41) function was proposed [52, 53]:

$$\Theta_h \begin{cases} 0^\circ \div 17.2^\circ & \Leftrightarrow \quad M \in (1.814, 1.818\rangle \\ 17.2^\circ \div 19.5^\circ & \Leftrightarrow \quad M \in (1.818, 1.896\rangle \\ 19.5^\circ \div 30^\circ & \Leftrightarrow \quad M \in (1.896, 1.904\rangle \end{cases} \tag{42}$$

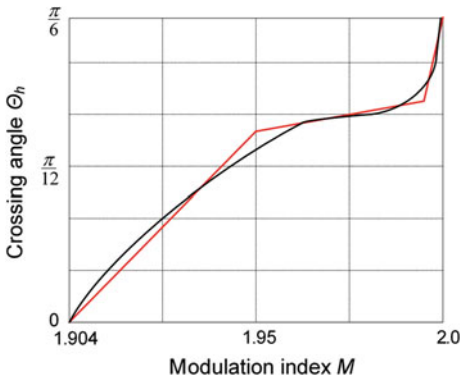

Fig. 28 Crossing angle Θ_h versus modulation index M and linearization of $\Theta_h = f(M)$

As far as compensated Space Vector $\boldsymbol{U}^*_{\boldsymbol{ref}}$ trajectory lies on the side of hexagon, only external vectors are used in the Space Vector Overmodulation mode II. Thus, small modulation indexes are evaluated similarly like in the Space Vector Overmodulation mode I, when Space Vector magnitude is changed, where the sum of the m_1 and m_2 is always equal 2:

$$m_1 = 2\frac{\sqrt{3}\cos\Theta_p - \sin\Theta_p}{\sqrt{3}\cos\Theta_p + \Theta_p} \tag{43}$$

$$m_2 = 2 - m_1 \tag{44}$$

4.3 Results of High Speed Operation of Adjustable Speed Drive over the Linear Range of Operation

Figure 29 presents steady state operation of the FCC in the Space Vector Overmodulation mode I ($M = 1.85$) and mode II ($M = 1.94$ and $M = 1.98$) for the CSVM and the ASVM modulation. In spite of the stator current i_{Sa} distortion, the FC voltages are properly balanced. Figure 30 shows the FCC operation in six step mode. As can be observed, in six step mode the FC voltage balancing is not possible. Thus, depending on the FCC parameters (such as dead-time value t_{DT}) modulation index should be limited.

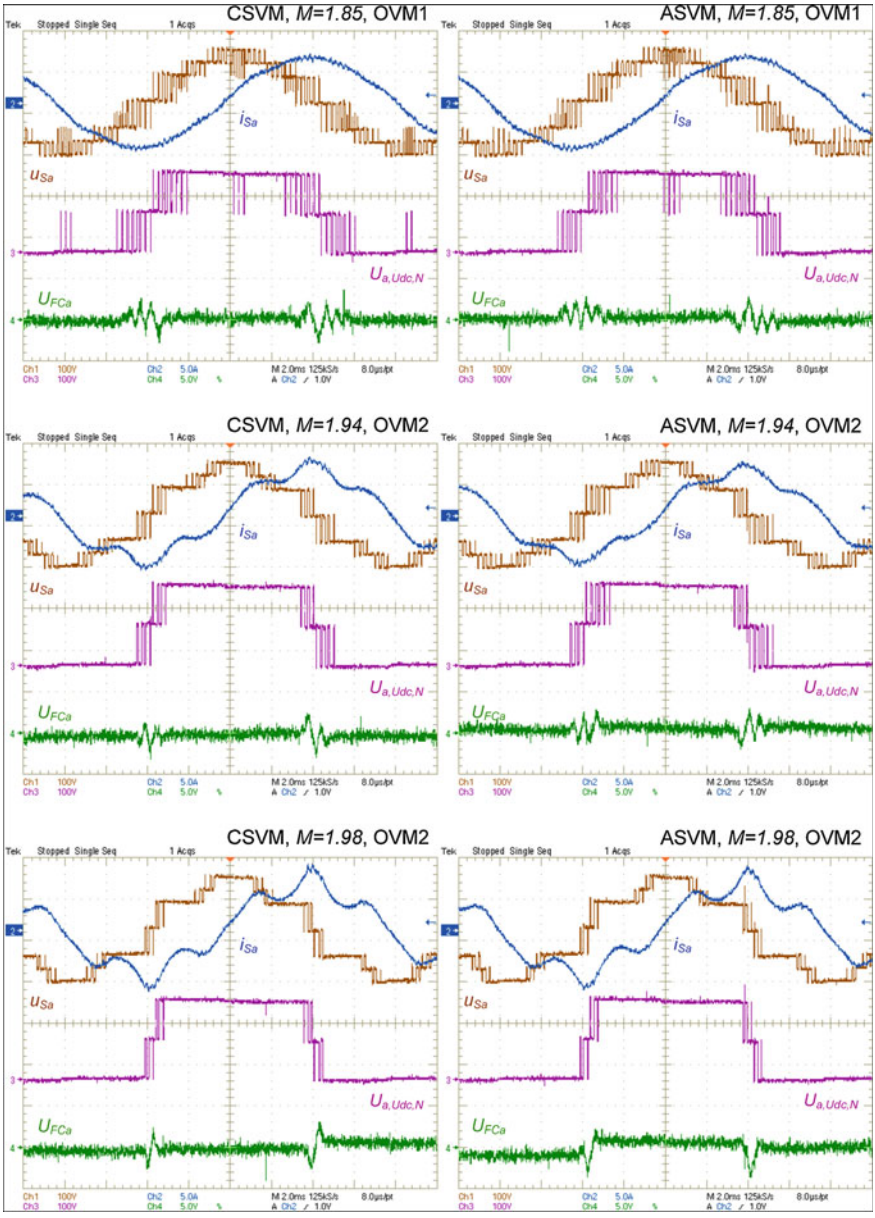

Fig. 29 Operation of the FCC in the space vector overmodulation mode I ($M = 1.85$) and mode II ($M = 1.94$ and $M = 1.98$) for the CSVM and the ASVM: stator voltage u_{Sa} and current i_{Sa}, pole voltage $U_{a,UdcN}$ and AC component of FC voltage U_{FCa}

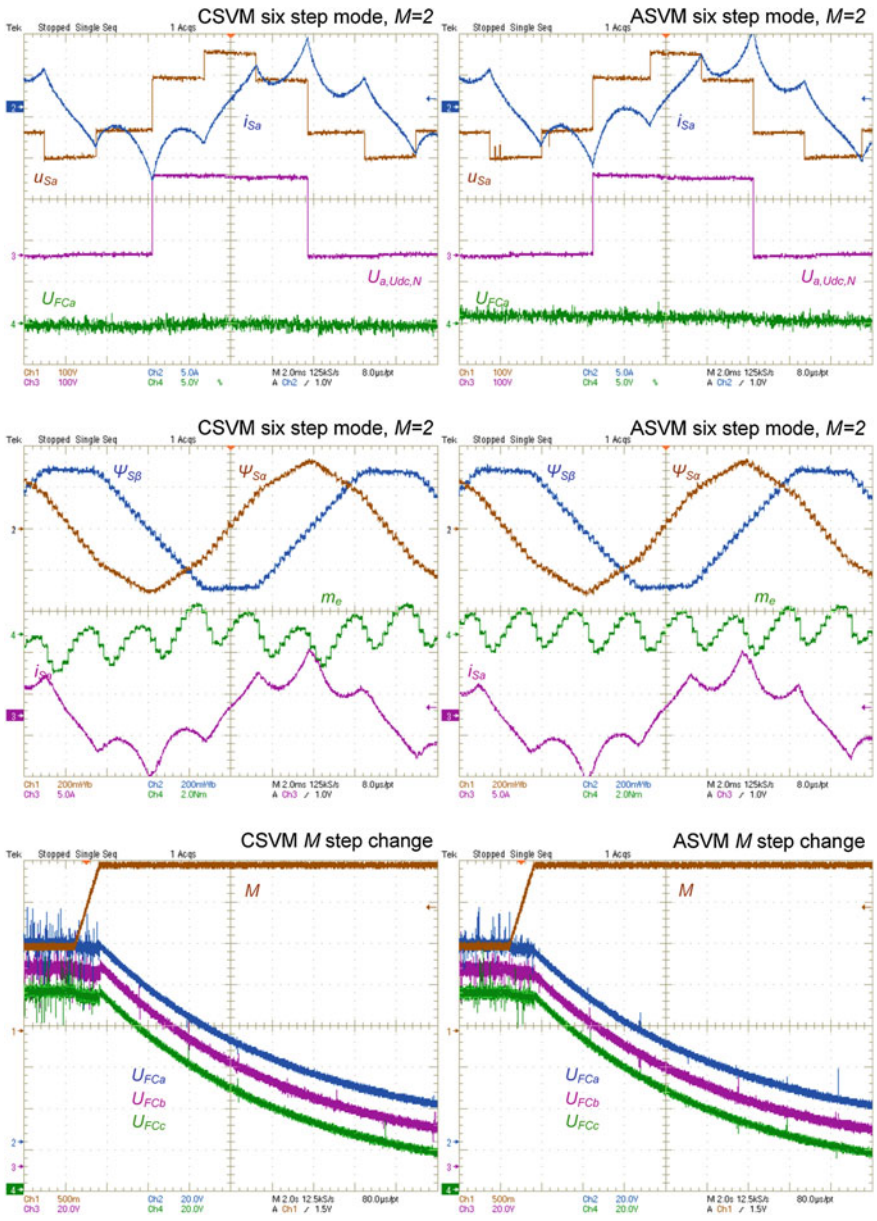

Fig. 30 Operation of the FCC in six step mode for the CSVM and the ASVM. From the top: **a** stator voltage u_{Sa} and current i_{Sa}, pole voltage $U_{a,UdcN}$ and AC component of FC voltage U_{FCa}, **b** stator fluxes $\Psi_{S\alpha}$ and $\Psi_{S\beta}$, electromagnetic torque m_e and stator current i_{Sa}. Step change of modulation index M from 1 to 2 for CSVM and ASVM: modulation index M, FC voltages U_{FCa}, U_{FCb} and U_{FCc}

5 Summary

In this Chapter the classical (CSVM) and adaptive (ASVM) Space Vector modulation for the Flying Capacitor Converter (FCC) was shown. The ASVM provides reduction of number of switching and the switching losses (more than 20 %) in the whole linear range of the converter operation because minimal number of vectors is used in each modulation region.

Also, additional features for both the CSVM and the ASVM was shown:

- elimination of DC sources voltage unbalance in full range of the converter operation (except square wave operation—six step mode),
- compensation of the Dead Time and the effect of semiconductor devices voltage drop—possible low speed operation, without phase currents distortion,
- the non-linear Overmodulation algorithm extending the operation range of the converter—possible high speed operation over the linear voltage control range of the converter,
- compensation of FC voltages balancing delay based on prediction of the FC voltages at the end of each sampling period, which provides minimization of the FC voltages pulsations.

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