Category: Device Modeling and Simulation

Surface Potential Based Analytical Model for Hetero-Dielectric p-n-i-n Double-Gate Tunnel-FET

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***Abstract*— In this work a piecewise Surface Potential based analytical model for a Hetero-Dielectric p-n-i-n Double Gate Tunnel FET has been developed which captures the device performance in all regions of operation i.e. Accumulation, Depletion and Inversion Region. Moreover, a comparative study among single High-k dielectric, single Low-k dielectric and Hetero-Dielectric TFET has been done. Here V_{gs} and V_{ds} dependent explicit equations for surface potential have been derived which are subsequently been made to be channel length dependent. Furthermore, the electrostatic behavior of the device is studied in terms of Lateral Electric Field and Energy Band Diagram. The efficacy of the model has been validated through simulated results obtained using ATLAS device simulation software.**

***Index Terms*— Tunnel FET (T-FET), Accumulation Region and Explicit Equation.**

I. INTRODUCTION

Steep sub threshold slope is a major requirement for energy efficient digital ICs. Continuous downscaling of MOSFETs has resulted in severe Short Channel Effects (SCEs) which have an adverse effect on device performance. In order to suppress these short channel effects and to improve the current driving capability a few other device architectures such as Double Gate (DG) architecture, Gate All Around (GAA) architecture have been proposed. Although, device scaling results in improvement of switching speed, density of circuits per chip, functionality and cost but it has also increased the difficulty of further reducing the supply voltage and rising leakage current(I_{on}/I_{off}). Thus, in response to the enormous challenges associated with scaled MOSFET several novel devices have been proposed. Among all these devices, Tunnel FET (TFET) is one such candidate which has sub threshold slope of less than 60 mV/decade [1].

TFET is a gated p-i-n diode with heavily doped source and drain regions ($1x10^{20}$ /cm^3). Unlike MOSFET, the current conduction phenomenon in TFET is quantum mechanical band to band tunneling (BTBT). For n-type TFET there is a reduction in barrier width at the Source/Channel junction with increasing gate voltage. The order of this tunnel barrier width is so small (a few nanometers) that it allows electrons to tunnel across the source/channel junction. Although, Tunnel FETs have shown better and improved characteristics than MOSFETs in terms of low I_{off}, high I_{on}/I_{off} and low subthreshold slope but they have some major shortcomings i.e. low I_{on} current, high ambipolar current and high gate to drain capacitance C_{gd} (miller capacitance). In order to enhance the tunneling current i.e. I_{on}, an improved architecture of TFET (p-n-i-n) has been reported with a heavily doped pocket region in between source and channel [2]. A Hetero-Dielectric TFET has also been proposed having higher I_{on} with suppressed ambipolar current [3]. Although there have been many experimental and simulation studies exploring different aspects of TFET but a very few analytical models regarding TFET have been reported [4]. Moreover, the existing T-FET models lack in capturing the complete device behavior. In this direction, a surface potential based model (Accumulation to Strong Inversion Region) for a Hetero-Dielectric p-n-i-n Double Gate Tunnel FET (DG-TFET) has been developed and reported in present paper. The basic idea behind the choice of Hetero-Dielectric p-n-i-n TFET was to integrate both the device performance boosters i.e. p-n-i-n TFET and Hetero-Dielectric TFET in a single architecture so as to attain higher I_{on}, low sub threshold slope with suppressed ambipolar current.

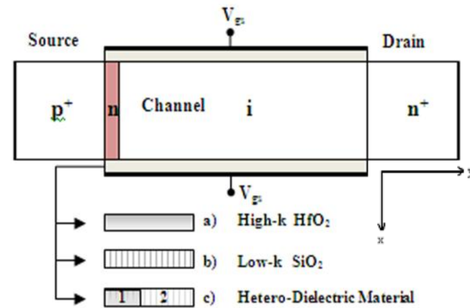

FIG.1. Schematic for a p-n-i-n Double-Gate Tunnel FET (L_{ch}=45nm, L_{pocket}=5nm, t_s=10nm, t_{ox}=3 nm, N_s=N_d=10^{20}/cm^3, N_{halo}=$3x10^{19}$/cm^3, N_{ch}=$1.45x10^{10}$/cm^3, Φ_m=4.5eV) for different-dielectric materials (a) High-k, HfO_2 ($\varepsilon_1=21\varepsilon_0$) (b) Low-k, SiO_2 ($\varepsilon_2=3.9\varepsilon_0$), (c) Hetero-Dielectric material.

II. DEVICE ARCHITECHTURE AND SIMULATION

Fig.1 represents a p-n-i-n Double-Gate Tunnel FET for three different dielectric materials i.e. (a) High-k dielectric (b) Low-k dielectric and (c) Hetero-dielectric (which includes a high-k material near source end and a low-k material near drain end) respectively. In this modeling scheme the channel is considered to be intrinsic or undoped. The model has been validated through simulation results obtained using ATLAS [5]. Standard models such as CONMOB, FLDMOB, SRH, FERMI and nonlocal BTBT have been used.

III. MODEL FORMULATION

Surface potential has been derived by using Two Dimensional (2-D) Poisson's equation as given below:

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$$\frac{\partial^2 \phi_k(x,y,V_{gs},\mathrm{V}_{ds})}{\partial x^2}+\frac{\partial^2 \phi_k(x,y,V_{gs},\mathrm{V}_{ds})}{\partial y^2}=\frac{qN_k}{\varepsilon_{si}} \quad (1)$$

where, $\phi_k(x,y,V_{gs},\mathrm{V}_{ds})$ is the two dimensional electrostatic potential, N_k denotes the doping concentration with k =1 and 2 for pocket and channel region respectively. ε_{si} is the silicon channel permittivity. The solution of Poisson's equation (1) has been approximated as a second order polynomial.

$$\phi_k(x,y,V_{gs},\mathrm{V}_{ds})=\phi_{sk}(y,V_{gs},\mathrm{V}_{ds})+C_{1k}\cdot x+C_{2k}\cdot x^2 \quad (2)$$

where, $\phi_{sk}(y,V_{gs},\mathrm{V}_{ds})$ is 1-D potential i.e. the potential at the surface of the silicon channel. C_{1k} and C_{2k} are the constants obtained by using appropriate boundary conditions:

$$\left.\begin{aligned}
&\phi_k(0,y,V_{gs},\mathrm{V}_{ds})=\phi_{sk}(y,V_{gs},\mathrm{V}_{ds})\\
&\phi_k(t_s,y,V_{gs},\mathrm{V}_{ds})=\phi_{sk}(y,V_{gs},\mathrm{V}_{ds})\\
&\frac{\partial\phi_k(0,y,V_{gs},\mathrm{V}_{ds})}{dx}=\frac{-C_{ox}\cdot(V_{gs}-V_{fb}-\phi_{sk}(y,V_{gs},\mathrm{V}_{ds}))}{C_s\cdot t_{si}}\\
&\frac{\partial\phi_k(t_s,y,V_{gs},\mathrm{V}_{ds})}{dx}=\frac{-C_{ox}\cdot(-V_{gs}+V_{fb}+\phi_{sk}(y,V_{gs},\mathrm{V}_{ds}))}{C_s\cdot t_{si}}
\end{aligned}\right\} \quad (3)$$

with channel thickness t_{si}, channel capacitance $C_s=\frac{\varepsilon_{si}}{t_{si}}$ gate dielectric capacitance $C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}$, gate to source voltage V_{gs} and flat band voltage $V_{fb}=\phi_m-\phi_{si}$ where ϕ_m and ϕ_{si} are the metal gate and silicon channel work functions respectively. Important point to be noted here is that while modeling channel region has been divided into two parts because Hetero-Dielectric TFET consists of both High-k and Low-k dielectric materials near source and drain ends respectively. Using equations (1) and (2) 1-D differential equation for $\phi_{sk}(y,V_{gs},\mathrm{V}_{ds})$ is obtained as below:

$$\frac{\partial^2\phi_{sk}(y,V_{gs},\mathrm{V}_{ds})}{dy^2}-\frac{1}{\lambda^2}\cdot\phi_{sk}(y,V_{gs},\mathrm{V}_{ds})=-\frac{1}{\lambda^2}\cdot\varphi_{dk}(V_{gs}) \quad (4)$$

Where, $\lambda=\sqrt{\frac{t_s^2\cdot C_s}{2\cdot C_{ox}}}$ is the characteristic length and

$$\varphi_{dk}(V_{gs})=-\frac{t_s^2\cdot C_s}{2\cdot C_{ox}}\cdot\left[\frac{qN_k}{\varepsilon_{si}}-\frac{2\cdot C_{ox}}{t_s^2\cdot C_s}\cdot\psi_G\right] \quad (5)$$

Equation (5) is the solution of 1-D approximation of the Poisson equation for long channels [6]. ψ_G is the effective gate voltage at the top and bottom of the channel at $y=\frac{L_{ch}}{2}$.The ψ_G value for different regions of operation is defined as below:

$\psi_G=V_{gs}-V_{fb}$ in **Depletion Region** where, $V_{fb}<V_{gs}\le V_{bi}+V_{ds}$. $V_{bi}+V_{ds}$ is the potential at Drain/Channel junction. In **Inversion Region,** $V_{gs}>V_{bi}+V_{ds}$ where V_{gs} and V_{ds} dependent explicit equation for ψ_G has been derived using Gradual Channel Approximation (**GCA**) considering the mobile charges.

$$\psi_G(V_{gs},V_c,V_{ds})=V_{gs}-V_{fb}-\frac{2\cdot k\cdot T}{q}\times W(S(V_{gs},V_c)) \quad (6)$$

$\frac{k\cdot T}{q}$ is the thermal voltage, W is the Lambert function which is a very rare function used for the conversion of implicit equations into closed explicit equations. Here, $S(V_{gs},V_c)$ can be determined using [7]. In similar way, explicit equation for **Accumulation Region** ($V_{gs}\le V_{fb}$) has been derived [8]. The only difference is that the majority charge carrier type has changed (holes).

Solution of equation (4) is given as:

$$\phi_{sk}(y,V_{gs},\mathrm{V}_{ds})=U_k\cdot\exp\left(\frac{y}{\lambda}\right)+V_k\cdot\exp\left(\frac{-y}{\lambda}\right)+\varphi_{dk}(V_{gs}) \quad (7)$$

U_k and V_k can be calculated by using the continuity equation for potential and electric field. The analytical expressions for lateral electric field, valence band energy and conduction band energy are given by equations (8), (9) and (10) respectively.

$$E_{sy}(y,V_{gs},V_{ds})=-\frac{\partial}{\partial y}\phi_{sk}(y,V_{gs},\mathrm{V}_{ds}) \quad (8)$$

$$\mathit{Valance\ Band\ Energy}=-\phi_k(\mathrm{x},y,V_{gs},\mathrm{V}_{ds})-\frac{E_g}{2} \quad (9)$$

$$\mathit{Conduction\ Band\ Energy}=-\phi_k(\mathrm{x},y,V_{gs},\mathrm{V}_{ds})+\frac{E_g}{2} \quad (10)$$

IV. RESULTS & DISCUSSIONS

Fig. 2(a), 2(b) and 2(c) represents the surface potential along the channel length for p-n-i-n DG TFET using High-k and Low-k dielectric materials in Off-State, Inversion Region and Accumulation Region respectively. From Fig. 2(a) it can be seen that there is a steep rise in surface potential in case where High-k dielectric is at drain end as compared to Low-k dielectric which results higher drain current leakage. However, the same steep rise in surface potential of High-k dielectric TFET near source end seems beneficial for better device performance in terms of low threshold voltage and switching as shown in Fig. 2(b) i.e. Inversion Region. In Fig. 2(c), it can be noticed that because of High-k dielectric TFET the surface potential is varying with a much higher rate than Low-k dielectric TFET at drain end. Therefore, it can be stated that this steep rise in potential at drain end may result in faster switching of the device in accumulation state. Fig. 2(d) represents surface potential for Hetero-Dielectric p-n-i-n DG TFET for V_{gs} = 0V, V_{gs}= 1.0V and V_{gs}= -0.4 V at V_{ds} = 0.5 V. Hetero-Dielectric TFET exhibits the advantage of both High-k and Low-k at source and drain ends respectively thereby yielding low leakage current, low threshold voltage and suppressed ambipolar behavior.

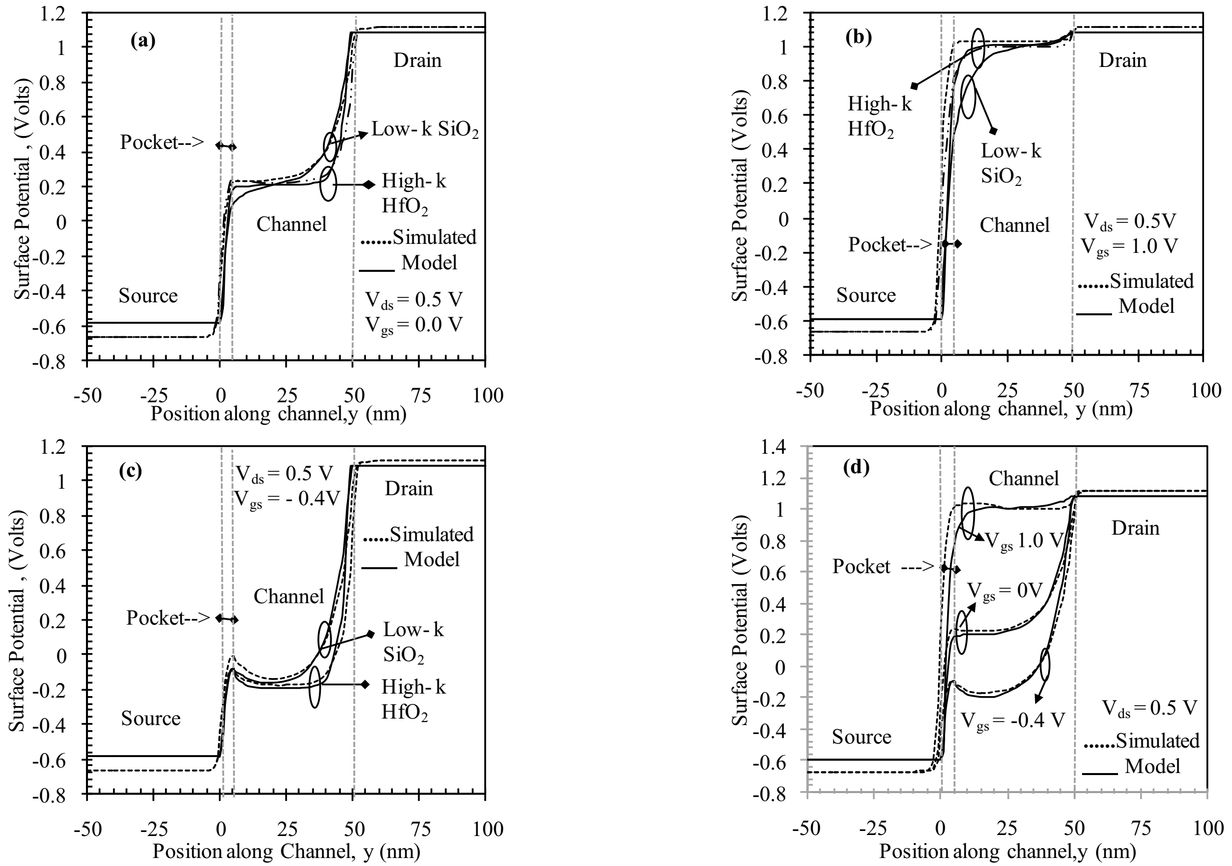

FIG.2. Surface potential along the channel length for p-n-i-n DG TFET using high-k and low-k dielectric materials at a constant drain voltage (V_{ds}= 0.5 V) and different gate voltages (a) V_{gs} = 0.0V (b) V_{gs} = 1.0V and (c) V_{gs} = -0.4 V (d) Surface Potential for Hetero-Dielectric p-n-i-n DG TFET in all regions of operation i.e Inversion Region (V_{gs}= 1.0 V), Off-State (V_{gs} = 0.0 V) and Accumulation Region (V_{gs} = -0.4 V) respectively.

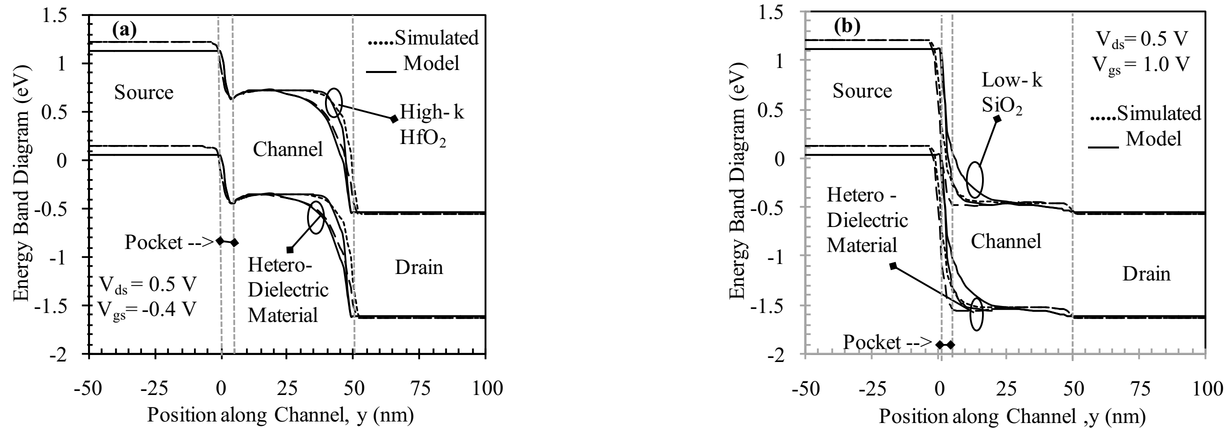

FIG.3. Energy band diagram along the channel length for (a) High-k and Hetero-Dielectric TFET in accumulation Region i.e. at V_{gs} = -0.4 V and V_{ds} = 0.5 V(b) Low-k and Hetero-Dielectric TFET in Inversion Region i.e. at V_{gs} = 1.0 V and V_{ds} = 0.5 V

In Fig. 3(a), energy band profiles for Hetero-Dielectric and High-k dielectric TFETs have been compared. It has been observed that the barrier width near drain/channel junction for Hetero-Dielectric TFET is much wider as compared to the barrier width of High-k dielectric TFET. This wider barrier width resists the tunneling of electrons across the junction and helps in suppressing the ambipolar current flow in Accumulation Region. Similarly, in Fig. 3(b) High-k dielectric TFET near source end causes an abrupt change in energy bands at source/channel junction in On-State thereby yielding a higher On-State current because of thinner tunneling barrier width at source channel junction in comparison with Low-k dielectric TFET. Fig. 4(a), (b) and (c) represents the lateral electric field along the channel length for

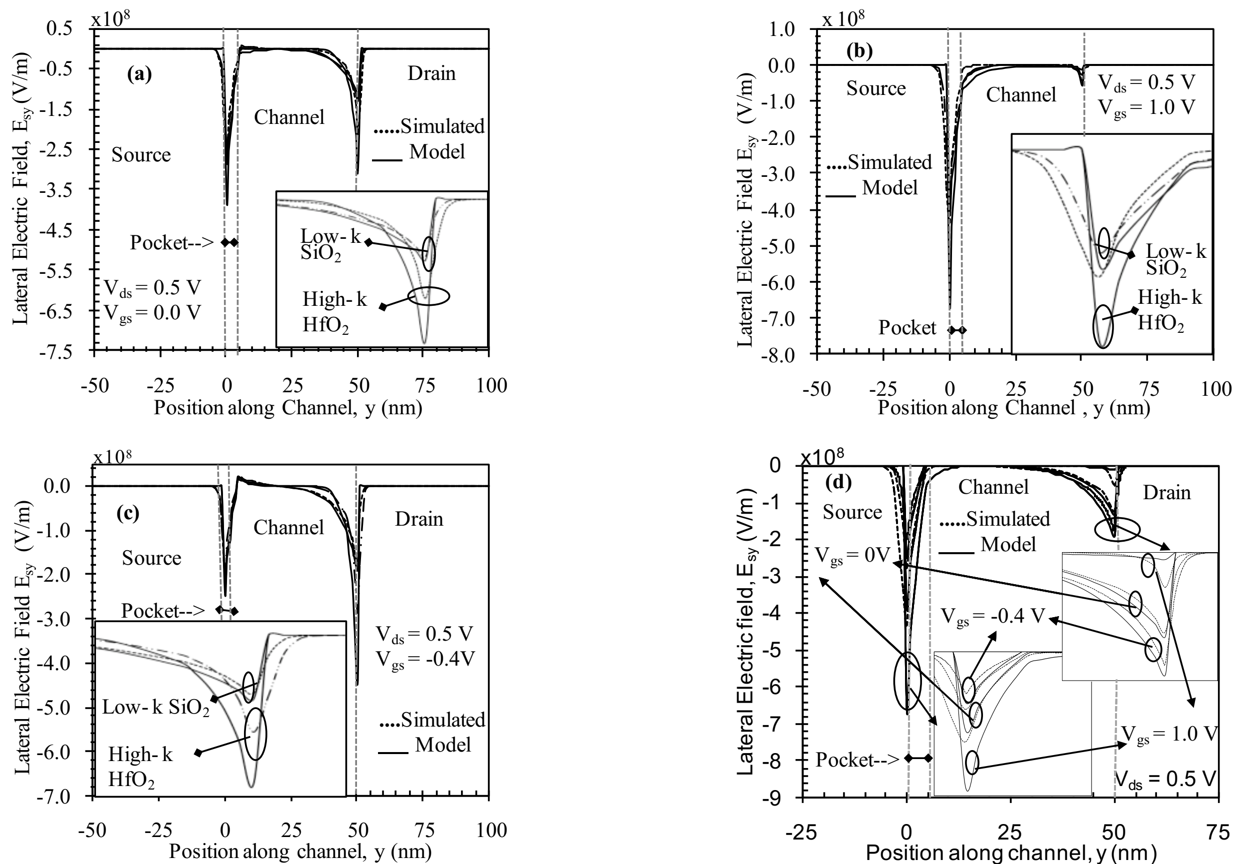

FIG. 4 Lateral electric field along the channel length for high-k and low-k gate dielectric TFET at a constant drain voltage (V_{ds}= 0.5 V) and different gate voltages (a) V_{gs} = 0.0V (b) V_{gs} = 1.0V and (c) V_{gs} = -0.4 V V (d) Lateral electric field for Hetero-Dielectric TFET in all regions of operation i.e Inversion Region (V_{gs}= 1.0 V), Off-State (V_{gs} = 0.0 V) and Accumulation Region (V_{gs} = -0.4 V) respectively.

High-k and Low-k dielectric TFETs in Off-State, Inversion Region and Accumulation Region respectively. High-k dielectric TFET results in an electric field enhancement at drain junction in Off-State and Accumulation Region i.e. Fig. 4(a) and 4(c). This causes more leakage current and also enhances the ambipolar behavior of the device. Moreover, a Low-k dielectric TFET helps in suppressing the ambipolar behavior as shown in Fig. 4(c). In Fig. 4(b), electric field of High-k dielectric TFET at Source/Channel junction is higher than Low-k dielectric TFET thereby resulting in improved tunneling current. Hetero-dielectric TFET combines the advantage of high-k and low-k dielectric TFETs in a single device as shown by inset of Fig. 4(d).

V. CONCLUSION

A surface potential based analytical model for a p-n-i-n Double-Gate Tunnel FET has been developed for all regions of device operation i.e. depletion, inversion and accumulation region. The derived model includes analytical expressions for surface potential, lateral electric field and energy band profile.Here, the advantage of using Hetero-dielectric material over single high-k and single low-k dielectric material has been shown and the model also captures the ambipolar behavior of the device. All the derived results are in good agreement with the simulated data.

VI. ACKNOWLEDGEMENT

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