Chapter 1
Introduction

Abstract This chapter presents a brief introduction to analog integrated circuits (ICs) design and to the area of analog IC design automation. First, the analog IC design problem is presented, that led to the research in this area, then, the traditional analog design flow is sketched and, finally, the features of the proposed methodology to enhance the circuit-sizing task are outlined.

Keywords Analog IC design · Circuit sizing · Gradient rules · Electronic design automation · Computer-aided-design

1.1 Analog IC Design

In the last decades, Very Large Scale Integration (VLSI) technologies have been widely improved, allowing the proliferation of consumer electronics and enabling the growth of integrated circuits (IC) market from $10 billion in 1980 to over $300 billion in 2013 [1]. IC designers are building systems that are increasingly more complex and integrated. The need of new functionalities, smaller devices, longer battery life, e.g., more power efficiency, less production and integration costs, and less design cost makes the design of electronic systems a truly challenging task, which must be completed within strict time-to-market constraints.

Although most of the functionalities in a modern electronic system are implemented using digital and digital signal processing (DSP) circuitry, analog and radio frequency (RF) circuitry, being essentially the link between digital circuitry and the continuous-valued external world, is integrated in the same chip. In such systems on a chip (SoC), the analog part occupies only about 10 % of the circuit area, however, the development time of analog blocks is considerably higher when compared to the development time of the digital part. The three main reasons identified for the larger development time of analog blocks are: the lack of effective Computer Aided Design (CAD) tools for Electronic Design Automation (EDA); analog circuits are being integrated using technologies optimized for

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digital circuits; and, analog blocks are difficult to reuse because they are more sensitive to environmental and process variations than its digital counterpart [2].

In digital IC design, several EDA tools and design methodologies are available that help the designers keeping up with the new capabilities offered by the technology processes. By its part, electrical simulators are the only analog design automation tool really established, despite the algorithms and techniques introduced in the last 25 years [3]. Due to the lack of automation, designers keep exploring the solution space almost manually. This method causes long design cycles, and allied to the non-reusable nature of analog IC, makes analog IC design a cumbersome task.

Designers have been replacing functions of analog circuits for digital processing whenever possible; however, there are some typical blocks that are appointed as remaining forever analog, such as [4]:

- On the input side of a system, the signals of a sensor, microphone or antenna have to be detected or received, amplified and filtered, to enable digitalization with good signal-to-noise and distortion ratio. Typical applications of these circuits are in sensor interfaces, telecommunication receivers or sound recording;
- Mixed-signal circuits like sample-and-hold, analog-to-digital converters, phase-locked loops and frequency synthesizers. These blocks provide the interface between the input/output of a system and digital processing parts of a SoC;
- On the output side of a system, the signal from digital processing must be converted and strengthened to analog so that the signal achieves the output with low distortion;
- Voltage/current reference circuits and crystal oscillators offer stable and absolute references for the sample-and-hold, analog-to-digital converters, phase-locked loops and frequency synthesizers;

The developments on the IC industry enabled the design of extremely complex Analog and Mixed-Signal (AMS) systems, which are established in telecommunications, medical and multimedia applications. To increase the performance of the ICs, i.e., enhance the functionalities but with lower power consumption, there is an exponential increase in the number of devices contained in a IC, as described by Moore's law. This means that the designers deal with the IC projects containing billions of transistors, under extreme competitive market conditions.

Despite the developments in the recent years, analog design automation tools and methodologies are still far from achieving a mature state, as there is no automation tool really established to support the analog design flow. Today's analog design is supported by circuit simulators, layout editing environments and verification tools, however the design cycle for AMS ICs is still long and error-prone.

In order to understand the automation of analog IC design, the steps in the design flow must be clear. After this brief introduction to the analog IC design problem, the systematic approach to the analog design automation flow [4], which intends to ease design automation, is covered in the next section.

1.2 The Analog IC Design Automation Flow

A typical and well accepted design flow for AMS ICs is presented in Fig. 1.1. This design flow consists of a series of top-down topology selection and specification translation steps, repeated from system level to the device level, and bottom-up layout generation, extraction and verification steps. Adopting a hierarchical top-down design methodology is possible to perform system architectural exploration, obtaining a better overall system optimization at a higher abstraction level before starting more detailed implementations at the device level. Thus, problems are found early in the design flow and, as a result, design have a higher chance of first-time success, with fewer or no overall time consuming redesign iterations.

On the top-down path, the topology selection is the process where a set of blocks and the connections between them in defined in order to implement the input specifications of the current hierarchy level. In the specification translation task, the higher-level specifications are translated in the specifications for each of the blocks. Block specifications may be the definition of the Gain and bandwidth for an amplifier, or the sizes of the transistors, depending of the models used in that abstraction level. The sizing is then verified to ensure the fulfillment of the input specifications.

At this point, the bottom-up flow is executed. Layout generation consists of creating the geometrical layout of the block under design at the lowest level in the

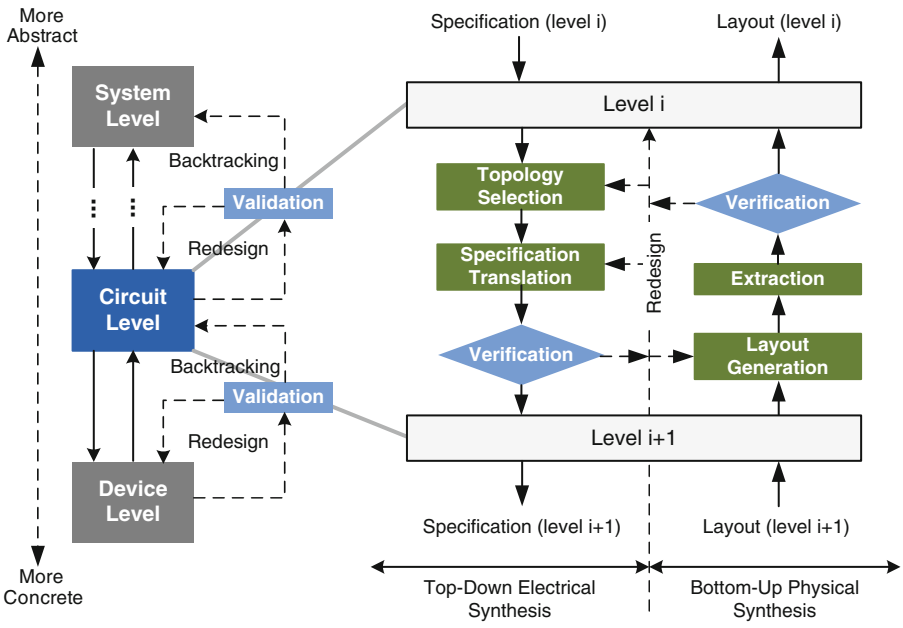

Fig. 1.1 System-level to device-level tasks of the analog IC design flow [4]

design hierarchy, or place and route the layouts of the sub-blocks at higher levels. Typically, the desired layout for a circuit is the one that minimizes the total area, while reducing the parasitic effects in the circuit performance. Then, the layout needs to be verified, which is done with design rule checkers and the layout-versus-schematic tools. Finally, the layout parasitics are extracted and simulated to verify its impact on the overall performance of the circuit.

The ascension to higher hierarchical levels is done when no potential problems are detected at the lowest levels and the layout meet the target requirements. When the topmost level verification is complete, the system is designed and ready for fabrication.

1.3 Research Contributions

This work addresses the problem of automatic specification translation at circuit level, also known as circuit sizing, where from the set of specifications, the designer finds out the sizes for the components, e.g., widths and lengths of the transistors, resistors, capacitors, etc. In the industry, this task is commonly done manually. The designers start by finding an approximate solution using simplified analytical expressions, and then, iteratively, adjust the solution until it meets all specifications, which sometimes can be very time consuming. The verification is done using circuit simulations that provide extra accuracy to the simplified (but treatable) equations used to derive the initial solution. The analog designer is aided by CAD frameworks comprised by many tools such as electrical simulators (e.g., Spectre® [5], HSPICE® [6]), layout editors (e.g., Virtuoso Layout Editor [5]), or tools for layout verification (e.g., CALIBRE [7], DIVA [5]). Despite its functionalities to support the manual IC design, these tools have limited automation options, and the ones available are usually overlooked by the majority of the designers. The time required to manually implement an analog project is usually of weeks or months, which is in opposition to the market pressure to accelerate the release of new and high performance ICs.

The designer's experience and knowledge are of the utmost importance, as they allow simplifications that speed up the design process, without compromising the quality of the solution, particularly, in the specification translation at the circuit-level, i.e., circuit sizing, the designer interacts manually with the available tools in order to achieve the project objectives, e.g., achieve the best set of device sizes, such that the circuit will meet the desired performance specifications (DC Gain, power, area, etc.). However, the search space of the objective function, which relates the design variables and the performance specifications of the circuit, is characterized by a complex multidimensional and irregular space, turning the manual search for the best solution into a cumbersome task.

In this research, GENOM-POF [8], which is a tool that performs a layout-aware circuit-level optimization that stems from Barros et al. GENOM [9–11], is enhanced by adding circuit specific knowledge that is automatically extracted using

machine learning techniques. The circuit sizing is done using the Nondominated Sorting Genetic Algorithm (NSGA-II) [12] for multi-objective multi-constraint optimization, which addresses robust design requirements by considering Process Voltage Temperature (PVT) corner analysis, where Mentor Graphics® ELDO™ and Synopsys® HSPICE® circuit simulators are used for accurate evaluation of the circuit performance. This work aims to demonstrate the advantage of embedding simple statistical models, representing design knowledge, into the optimization kernel in order to improve the performance of the sizing optimization. The main objectives for this work are detailed below:

- Create a simple model that is capable of extracting a set of gradients rules, automated and autonomously, i.e., without any human knowledge. This set of gradients rules extracted should contain knowledge about any analog circuit in study;
- Create a model of rules and integrate it with the mutation operator of the (NSGA-II), in order to improve its efficiency during the optimization of the analog circuit. Compare the performance of reference NSGA-II with the modified NSGA-II with the model of gradients, created in the previous paragraph, and verify potential benefits of this modification;
- Evaluate and analyze the robustness of the models created previously, through its application in highly complex analog circuits;
- Improve the quality of the achieved sizing solutions.

The designer provides the chosen topology for the project, the variables for optimization and their ranges, the specifications to be met and the objective functions, e.g., minimize area/power, maximize DC Gain, etc., the tool instantiates the components to size, ensures that specifications are met and performs the search objectives space for the optimum solutions. The modified GENOM-POF, produced within this work, aims at helping the designer in his/her circuits sizing task, not only by generating solutions faster but also by achieving better Pareto optimal solutions.

1.4 Conclusions

The complexity of electronic systems imposes the use of CAD tools to support the design process. In digital IC design, several EDA tools and design methodologies are available that help the designers keeping up with the new capabilities offered by the technology, however the analog design automation tools strive to close the gap created due to the large investment made in the digital domain. This cause the manual exploration of the solution space, that in its turn creates expensively long designs that are difficult to reuse. In this context, the contributions of this research were presented, that aim to ease the efforts of analog designers to successfully complete this time-consuming task.

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