Chapter 4
Quantum Mechanical Potential Modeling of FinFET

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Abstract This chapter focus on a full Two-Dimensional (2D) Quantum Mechanical (QM) analytical modeling in order to evaluate the 2D potential profile within the active area of FinFET structure. Various potential profiles such as surface, back to front gate, and source to drain potential have been presented in order to appreciate the usefulness of the device for circuit simulation purposes. As we move from source end of the gate to the drain end of the gate, there is substantial increase in the potential at any point in the channel. This is attributed to the increased value of longitudinal electric field at the drain end on application of a drain to source voltage. Further, in this chapter, the detailed study of threshold voltage and its variation with the process parameters is presented. A threshold voltage roll-off with fin thickness is observed for both theoretical and experimental results. The fin thickness is varied from 10 to 60 nm. From the analysis of S/D resistance, it is observed that for a fixed fin width, as the channel length increases, there is an enhancement in the parasitic S/D resistance. This can be inferred from the fact as the channel length decreases, quantum confinement along the S/D direction becomes more extensive. For our proposed devices a close match is obtained with the results through analytical model and reported experimental results, thereby validating our proposed QM analytical model for DG FinFET device.

4.1 Introduction

The scaling of CMOS structure is approaching its limits; multiple gate architecture such as Double Gate FinFET structure presents significant advantages to fulfill long range International Technology Roadmap for Semiconductors (ITRS) [1] requirements. The Poisson's equation-based numerical modeling of Double Gate

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FinFET device has been carried out by many workers [2–6] which presents generic implicit surface potential solution for FinFET device. For nanoscale multi-gate devices, two-dimensional analytical approach would be required which will be valid under Quantum Mechanical (QM) domain of FinFET device under study. For this purpose, we present a fully quantum mechanical surface potential model for the channel region of FinFET device using analytical modeling.

For a CMOS technology to keep pace with downscaling, improved carrier transport and low parasitic source/drain resistance are required. Pei et al. [7] investigated FinFET simulation and analytical modeling. Double gate FinFET has been considered as one of the most promising candidate for sub-50 nm designs. But double gate structure suffers from possible misalignment between source/drain with gate region, thereby increasing the overlap capacitances as well as source to drain series resistance. This would result in a slower device, and hence high frequency operation of the device would be restricted. Fin height and Fin thickness are modified in order to achieve optimized operation of the device. Potential in the active area of FinFET device and threshold voltage have also been evaluated. Dixit et al. [8] used a 45 nm FinFET structure to understand the implication of source/drain resistance on the device characteristics. Sub-20 nm FinFET using SiGe as a gate material was developed by Hisamoto et al. [9]; they showed the ease of fabrication using planer MOSFET process technology. Double Gate FinFET structure offers higher driving capabilities and reduces SCE [10, 11]. To develop sub-50 nm MOSFETs, double gate FinFET structure has been widely studied [12–14]. For the double gate MOSFETs, the gate controls the energy barrier between source and drain effectively [1, 12, 15–17]. Further studies have shown [18–22] that controlling threshold voltage and parasitic for ultrathin body is a difficult task.

The threshold voltage of a transistor is one of the key parameters in the design of FinFET circuits. Katti et al. [23] have modeled fully depleted SOI MOSFETs using the solution of three-dimensional (3-D) Poisson's equation. As the device dimensions continue to scale down to deep sub-micrometer regime to obtain better performance, analytical modeling of these devices becomes even more challenging. Although Kedzierski et al. [24] have addressed this issue and proposed a technology solution, an analytical understanding of parasitic series resistance in the FinFET device is desirable. In this chapter, a full quantum mechanical analytical modeling for FinFET structure has been carried out. The subsequent section deals with 3D FinFET structure followed by quantum mechanical potential modeling, threshold voltage modeling, and source/drain (S/D) resistance modeling. The results obtained based on our model are compared and contrasted with reported, experimental, and simulated results for the purpose of validation and verification of our proposed analytical model.

4.2 FinFET Structure

Figure 4.1 shows 3D view of FinFET. The gate "wraps" over the thin Si Fin, yielding a quasi-planar symmetrical double-gate FinFET structure with two inversion channels that are charge coupled. Both the front and back gates might have the

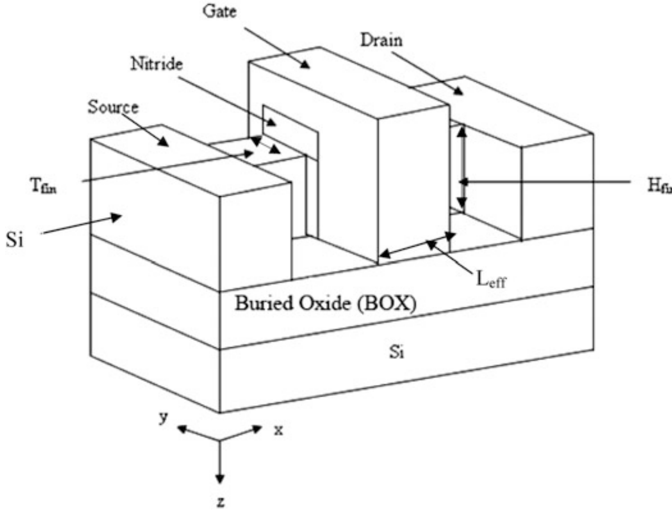

Fig. 4.1 Structure of FinFET

same work function. They are further tied to same applied potential. The key challenges in the fabrication of Double Gate FinFET devices are [25–28] self-alignment of the two gates and formation of an ultrathin silicon film. In FinFET device, the fin is a narrow channel of silicon patterned on an SOI wafer. The gate wraps around the fin on three faces. The top insulator is usually thicker than the side insulators; hence, the device has effectively two channels. The top insulator may be reduced in thickness in order to control the channel as well.

4.2.1 FinFET Design Parameters

FinFET parameters are indicated in the Fig. 4.1. The definitions of the various parameters are: L_{eff}: effective channel length of FinFET, which is the actual distance between source and drain region, H_{fin}: height of silicon fin defined by the distance between top gate and buried oxide, T_{fin}: thickness of silicon fin defined as the distance between front and back gate oxides, W_{fin}: geometrical channel width defined as: $W_{\text{fin}} = (2 \times H_{\text{fin}}) + T_{\text{fin}}$. When the thickness of silicon film (T_{fin}) is much larger than its height (H_{fin}) or when top gate oxide is much thinner than the front and back oxides, FinFET can be approximately treated as single-gate fully depleted (FD) SOI MOSFET [7, 29, 30].

On the other hand, when height of the silicon film (H_{fin}) is much larger than its thickness (T_{fin}) or top gate oxide is much thicker than the front and back oxides, FinFET can be approximately treated as Double Gate FET device. The two limits of FinFET, namely, FD-FET and DG-FET have been widely studied and well understood [3, 20, 21, 31, 32]. To our understanding in the regime where both fin height and thickness have control over short channel effects (SCE), the dependence

of SCE on device dimensions is not well extracted or known. For the purpose of understanding the dependence of output characteristics of FinFET with respect to various device/process parameters, a full quantum mechanical analytical potential modeling is carried out in the next section.

4.3 Quantum Mechanical Potential Modeling

In order to extract full two-dimensional potential profile within the active area of the device, QM solution is carried out. For this purpose, several methods have been proposed [33–36], where the potential function is divided into two parts, the first one being the long channel solution and the second one, a short channel evaluation. But the evaluation of short channel term takes into account the functional dependence of device parameters, which is a complicated issue and takes large computational time. For the purpose of simplification and also to have a reduced complexity in time, we have assumed the following dependence of potential, where two-dimensional potential is broken down into 1D surface potential and a 2D function [37] as given below:

$$\psi(x,y) = \psi_s(x) \times A(x,y) \tag{4.1}$$

where $\psi_s(x)$ is the surface potential and $A(x,y)$ is the vertical distribution of the envelop function.

$A(x, y)$ as given in (4.1) can be written as [37]:

$$A(x,y) = \frac{Z(x,y)}{Z(x,y=1)} \tag{4.2}$$

where $Z(x, y)$ can be written as [37]

$$Z(x,y) = \psi_0(x) - \frac{2}{\beta}\ln\left\{\cos\left[\sqrt{\frac{q^2 n_i}{2kT\varepsilon_{\mathrm{Si}}}e^{\frac{\beta(\psi_0(x)-V_{\mathrm{F}}(x))}{2}}}\left(y-\frac{T_{\mathrm{fin}}}{2}\right)\right]\right\} \tag{4.3}$$

The behavior of center potential $\psi_0(x)$ as a function of effective gate voltage is given as [3]:

$$\psi_0(x) = U - \sqrt{U^2 - \left(V_{\mathrm{gs}} - V_{\mathrm{FB}}\right)\psi_{0\max}(x)} \tag{4.4}$$

where $\psi_{0\max}(x)$ is the maximum potential that can be obtained at the center of the channel under a given bias at the terminal and U is given as

$$U = \frac{1}{2}\left[\left(V_{\mathrm{gs}} - V_{\mathrm{FB}}\right) + (1+r)\psi_{0\max}(x)\right] \tag{4.5}$$

$\psi_{0\max}(x)$ can be evaluated as:

$$\psi_{0\max}(x) = V_{\mathrm{F}}(x) + \frac{1}{\beta}\ln\left(\frac{2\pi^2\varepsilon_{\mathrm{Si}}kT}{q^2 n_i T_{\mathrm{fin}}^2}\right) \tag{4.6}$$

where r in (4.5) is defined as smoothing parameter which weakly depends on oxide and silicon thickness and quasi-Fermi potential which is given by [37]:

$$r = (At_{\mathrm{ox}} + B)\left(\frac{C}{T_{\mathrm{fin}}} + D\right)e^{-EV_{\mathrm{F}}(x)} \tag{4.7}$$

The optimized value of A, B, C, D, and E are given as 0.0267 nm^{-1}, 0.0270, 0.4526 nm, 0.0650, and 3.2823 V^{-1} respectively. The optimized values obtained are for the device dimensions of $t_{\mathrm{ox}} < 10$ nm and $T_{\mathrm{fin}} > 5$ nm [37]. Extensive numerical simulations show that quasi-Fermi potential also depends on gate voltage, effective channel length, and fin thickness and is given by a semiempirical relationship as

$$V_{\mathrm{F}}(x) = \frac{2kT}{q}\frac{m}{n}\ln\left[\left(\exp\left(-\frac{V_{\mathrm{ds}}(m/n)^{-1}}{kT/q}\right) - 1\right)\left(\frac{x}{L_{\mathrm{eff}}}\right)^{\frac{c}{V_{\mathrm{gs}}-V_{\mathrm{FB}}}} + 1\right]^{-1} \times (a \times T_{\mathrm{fin}})^{\frac{V_{\mathrm{ds}}}{3c}} \tag{4.8}$$

where $m/n = 2 + b(V_{\mathrm{gs}} - V_{\mathrm{FB}})$, $a = 0.2\ \mathrm{nm}^{-1}$, $b = 7.5\ \mathrm{V}^{-1}$, $c = 1$ V, and V_{ds} is the applied drain voltage. The quasi-Fermi potential given in (4.8) is a function of position along the channel length and drain voltage V_{ds}. Substituting the value of $\psi_0(x)$ from (4.4) and $V_{\mathrm{F}}(x)$ from (4.8) in (4.3), we obtain $Z(x, y)$ as:

$$Z(x,y) = \left(U - \sqrt{U^2 - (V_{\mathrm{gs}} - V_{\mathrm{FB}})\psi_{0\max}(x)}\right) - \frac{2}{\beta}\ln\left\{\cos\left[\sqrt{\frac{q^2 n_i}{2kT\varepsilon_{\mathrm{Si}}}e^{\frac{\beta\left(\left(U - \sqrt{U^2 - (V_{\mathrm{gs}} - V_{\mathrm{FB}})\psi_{0\max}(x)}\right) - \left(\frac{2kT}{q}\frac{m}{n}\ln\left[\left(\exp\left(-\frac{V_{\mathrm{ds}}(m/n)^{-1}}{kT/q}\right) - 1\right)\left(\frac{x}{L_{\mathrm{eff}}}\right)^{\frac{c}{V_{\mathrm{gs}}-V_{\mathrm{FB}}}} + 1\right]^{-1} \times (a \times T_{\mathrm{fin}})^{\frac{V_{\mathrm{ds}}}{3c}}\right)\right)}{2}}}\left(y - \frac{T_{\mathrm{fin}}}{2}\right)\right]\right\} \tag{4.9}$$

An expression of $Z(x, y)$ is used to obtain the analytical solution of the function $A(x, y)$. The solution of one-dimensional Poisson equation is:

$$\psi_{\mathrm{s}}(x) = C_1\exp(m_1 x) + C_2\exp(-m_1 x) - \frac{R}{m_1^2} \tag{4.10}$$

where C_1, C_2, m_1, and R are calculated by putting the following boundary conditions based on the physics of the device as:

$$\psi_{\mathrm{s}}(x = 0) = \phi_s \quad \text{and} \quad \psi_{\mathrm{s}}(x = L_{\mathrm{eff}}) = \phi_s + V_{\mathrm{ds}}$$

We obtained the values of the parameters as:

$$C_1 = \frac{\phi_S[1 - \exp(-m_1 L_{\text{eff}})] + V_{\text{ds}} + \frac{R[1-\exp(-m_1 L_{\text{eff}})]}{m_1^2}}{2\sinh(m_1 L_{\text{eff}})} \tag{4.11}$$

$$C_2 = -\frac{\phi_S[1 - \exp(+m_1 L_{\text{eff}})] + V_{\text{ds}} + \frac{R[1-\exp(+m_1 L_{\text{eff}})]}{m_1^2}}{2\sinh(m_1 L_{\text{eff}})} \tag{4.12}$$

$$R = \frac{\eta}{\varepsilon_{\text{Si}} T_{\text{fin}}} \left[qN_a T_{\text{fin}} - 2C_{\text{ox}}\left(V_{\text{gs}} - V_{\text{FB}} - \phi_F\right)\right] \tag{4.13}$$

$$m_1 = \sqrt{\frac{2\eta C_{\text{ox}}}{\varepsilon_{\text{Si}} T_{\text{fin}}}}$$

where η is a fitting parameter which incorporates the effects of the variation of the lateral field on the depleted film under the channel. As demonstrated by Harrison et al. [38], η is lower than 1 for $V_{\text{gs}} \leq V_{\text{th}}$ and depends on the channel doping concentration and thickness. Therefore, this parameter has to be calibrated for each technology. $C_{\text{ox}} = \varepsilon_{\text{ox}}/t_{\text{ox}}$ is the oxide capacitance per unit area, and N_a is the channel doping. Substituting the value of C_1, C_2, and R in (4.10), surface potential, $\psi_{\text{s}}(x)$, is obtained as:

$$\begin{aligned}\psi_{\text{s}}(x) = &\left(\frac{\phi_S[1 - \exp(-m_1 L_{\text{eff}})] + V_{\text{ds}} + \frac{R[1-\exp(-m_1 L_{\text{eff}})]}{m_1^2}}{2\sinh(m_1 L_{\text{eff}})}\right)[\exp(m_1 x)] \\ &+ \left(\frac{\phi_S[1 - \exp(+m_1 L_{\text{eff}})] + V_{\text{ds}} + \frac{R[1-\exp(+m_1 L_{\text{eff}})]}{m_1^2}}{2\sinh(m_1 L_{\text{eff}})}\right)[\exp(-m_1 x)] \\ &- \frac{\left(\frac{\eta}{\varepsilon_{\text{Si}} T_{\text{fin}}} \left[qN_a T_{\text{fin}} - 2C_{\text{ox}}\left(V_{\text{gs}} - V_{\text{FB}} - \phi_F\right)\right]\right)}{m_1^2}\end{aligned} \tag{4.14}$$

From (4.2) and (4.14), we obtained the full QM two-dimensional surface potential as:

$$\begin{aligned}\psi(x,y) = &\Bigg[\left(\frac{\phi_S[1 - \exp(-m_1 L_{\text{eff}})] + V_{\text{ds}} + \frac{R[1-\exp(-m_1 L_{\text{eff}})]}{m_1^2}}{2\sinh(m_1 L_{\text{eff}})}\right)[\exp(m_1 x)] \\ &+ \left(\frac{\phi_S[1 - \exp(+m_1 L_{\text{eff}})] + V_{\text{ds}} + \frac{R[1-\exp(+m_1 L_{\text{eff}})]}{m_1^2}}{2\sinh(m_1 L_{\text{eff}})}\right)[\exp(-m_1 x)] \\ &- \frac{\left(\frac{\eta}{\varepsilon_{\text{Si}} T_{\text{fin}}} \left[qN_a T_{\text{fin}} - 2C_{\text{ox}}\left(V_{\text{gs}} - V_{\text{FB}} - \phi_F\right)\right]\right)}{m_1^2}\Bigg] \times \frac{Z(x,y)}{Z(x,y=1)}.\end{aligned} \tag{4.15}$$

4.4 Threshold Voltage Modeling

The threshold voltage of a FinFET can be defined as that voltage (gate) which would be able to invert all the channels within the Fin structure simultaneously. We can derive the QM threshold voltage, $V_{\text{th,QM}}$, of the DG FinFET as [39]:

$$V_{\text{th,QM}} = V_{\text{FB}} + \psi_{\text{s(inv)}} - \frac{Q_{\text{b}}}{2C_{\text{ox}}} + \Delta V_{\text{th,QM}} \tag{4.16}$$

where $\psi_{\text{s(inv)}}$ is the surface potential at threshold, and $\Delta V_{\text{th,QM}}$ is the threshold voltage change due to QME's, which can be approximated as a function of the ratio of the carrier effective mass in the direction of confinement to the free electron mass and silicon film thickness which is given as [40]:

$$\Delta V_{\text{th,QM}} \cong \frac{S}{(kT/q)\ln(10)} \times \frac{0.3763}{(m_x/m_o)T_{\text{fin}}^2} \tag{4.17}$$

where S is the subthreshold slope, T_{fin} is fin thickness, and m_x/m_o is the ratio of the carrier effective mass in the direction of confinement to the free electron mass (e.g., 0.92 for electrons and 0.29 for holes).

The bulk charge Q_{b} is given as:

$$Q_{\text{b}} = -qN_a T_{\text{fin}} \tag{4.18}$$

When considering the quantum-mechanical confinement of inversion-layer carriers, $V_{\text{th,QM}}$ of (4.16) should be augmented with $\Delta V_{\text{th,QM}}$. The surface potential at threshold is given by:

$$\psi_{\text{s(inv)}} = 2\psi_b \tag{4.19}$$

$$\psi_b = \frac{kT}{q}\ln\left(\frac{N_a}{N_i}\right) \tag{4.20}$$

Substituting the value of ψ_b from (4.20) into (4.19), we obtained:

$$\psi_{\text{s(inv)}} = 2\left(\frac{kT}{q}\ln\left(\frac{N_a}{N_i}\right)\right) \tag{4.21}$$

Substituting the value of Q_{b} from (4.18), $\psi_{\text{s(inv)}}$ from (4.21) and $\Delta V_{\text{th,QM}}$ from (4.17) into threshold expression (4.16), the final expression for the threshold voltage with QM corrections is obtained as:

$$V_{\text{th,QM}} = V_{\text{FB}} + 2\left(\frac{kT}{q}\ln\left(\frac{N_a}{N_i}\right)\right) - \frac{(-qN_a T_{\text{fin}})}{2C_{\text{ox}}} + \frac{S}{(kT/q)\ln(10)} \times \frac{0.3763}{(m_x/m_o)T_{\text{fin}}^2} \tag{4.22}$$

4.5 Source/Drain Resistance Modeling

The quasi-nonplanar devices suffer from a high parasitic resistance due to narrow width of their source/drain (S/D) regions. The series resistance in the S/D regions of a FinFET has contributions from its components arising from different parts of the S/D geometry. The enhanced total resistance of FinFET reduces the driving capability of the device at all applied biases. We analyzed the parasitic S/D resistance and the total resistance of FinFET device using analytical model. The sheet resistance R_{sh} in the S/D extension is given by [8]:

$$R_{sh} = \rho_{ext}\left(\frac{W_{sp}}{H_{fin} \times W_{fin}}\right) \tag{4.23}$$

where ρ_{ext} is the resistivity of the S/D extension, and W_{sp} is the length of S/D extension.

Spread resistance (R_{sp1}) is due to the spread of current from the thin accumulation layer into the S/D extension which can be written as [8]:

$$R_{sp1} = \frac{1}{2} \times \left[\frac{2\rho_{ext}}{\pi H_{fin}} \ln\left(0.75\frac{\left(\frac{W_{fin}}{2}\right)}{x_c}\right)\right] \tag{4.24}$$

where x_c is the channel thickness. R_{sp2} is the resistance due to the spread of current from S/D extensions into the wider Heavily Doped S/D (HDD) region and is given as [8].

$$R_{sp2} = \frac{\rho_{hdd} \times [\ln(0.75) + \ln(W_{sd}) - \ln(W_{fin})]}{\pi(H_{fin} + T_{SEG} - T_{SIL})} \tag{4.25}$$

where T_{SIL} is the thickness of the S/D silicide and T_{SEG} is S/D SEG thickness.

R_{sd} has been modeled as series combination of two resistances, R_1 and R_2, and is given as:

$$R_{sd} = 2 \times (R_1 + R_2) \tag{4.26}$$

R_1 is the resistance between the gate and S/D spacer edge.

$$R_1 = R_{sp1} + R_{sh} \tag{4.27}$$

Substituting the value of R_{sh} and R_{sp1} from (4.23) and (4.24) in (4.27), we get the value of R_1 as:

$$R_1 = \left(\frac{1}{2} \times \left[\frac{2\rho_{ext}}{\pi H_{fin}} \ln\left(0.75\frac{\left(\frac{W_{fin}}{2}\right)}{x_c}\right)\right]\right) + \left(\rho_{ext}\left(\frac{W_{sp}}{H_{fin} \times W_{fin}}\right)\right) \tag{4.28}$$

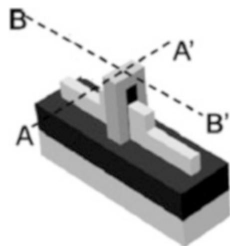

Fig. 4.2 Geometry of the FinFET device [8]

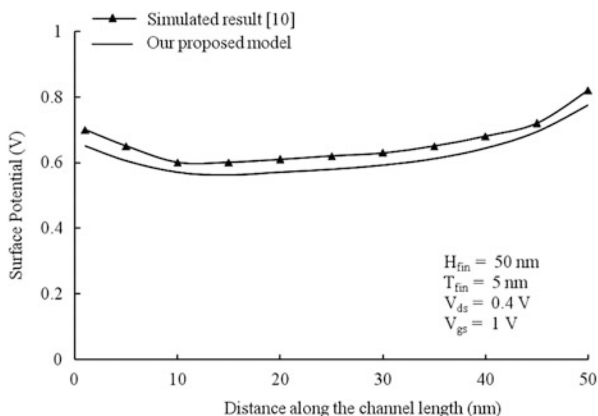

Fig. 4.3 Surface potential variations along the channel length for comparing our quantum result and through reported simulation result [37]

Also R_2 is the parallel combination of resistance of plane A–A′ and plane B–B′ (Fig. 4.2) and is given by

$$R_2 = \frac{R_a \times R_b}{R_a + R_b} \tag{4.29}$$

$R_a = R_{\text{conA}}$ and $R_b = R_{\text{sp2}} + R_{\text{conB}}$; R_{conA} is contact resistance of plane A–A′ and R_{conB} is contact resistance of plane B–B′.

Contact resistance in plane A–A′ (Fig. 4.2) is given:

$$R_{\text{conA}} = \frac{\rho_{\text{int}}}{W_{\text{fin}} \times T_{\text{SIL}}} \tag{4.30}$$

where ρ_{int} is the contact resistivity. Contact resistance in plane B–B′ (Fig. 4.3) is given by:

$$R_{\text{conB}} = \frac{\rho_{\text{int}}}{(L_{\text{transfer}} \times W_{\text{sd}})} \coth\left(\frac{L_{\text{con}}}{L_{\text{transfer}}}\right) \tag{4.31}$$

where L_{con} is the physical length and W_{sd} is the width of HDD region. In case of the current conduction parallel to a semiconductor–metal interface, a minimum contact length exists before this conduction current is actually transferred from the semiconductor to the metal. This length is known as transfer length (L_{transfer}).

Substituting the value of R_1 and R_2 from (4.28) and (4.29) in (4.26), we get the S/D resistance (R_{sd}) as:

$$R_{\mathrm{sd}} = 2 \times \left(\left(\left(\frac{1}{2} \times \left[\frac{2\rho_{\mathrm{ext}}}{\pi H_{\mathrm{fin}}} \ln \left(0.75 \frac{\left(\frac{W_{\mathrm{fin}}}{2}\right)}{x_{\mathrm{c}}} \right) \right] \right) + \left(\rho_{\mathrm{ext}} \left(\frac{W_{\mathrm{sp}}}{H_{\mathrm{fin}} \times W_{\mathrm{fin}}} \right) \right) \right) + \left(\frac{R_a \times R_b}{R_a + R_b} \right) \right) \quad (4.32)$$

The total resistance is obtained as:

$$R_{\mathrm{total}} = \frac{V_{\mathrm{ds}}}{I_{\mathrm{s}}} = R_{\mathrm{ch}} + R_{\mathrm{sd}} \quad (4.33)$$

where R_{ch} is the resistance of channel region. From (4.32), substitute the value of R_{sd} in (4.33). The final expression for the total resistance is obtained as given below:

$$R_{\mathrm{total}} = R_{\mathrm{ch}} + \left(2 \times \left(\left(R_{\mathrm{sp1}} + R_{\mathrm{sh}} \right) + \left(\frac{R_a \times R_b}{R_a + R_b} \right) \right) \right) \quad (4.34)$$

4.6 Results and Discussion

A full two-dimensional potential analytical modeling scheme taking into consideration various quantum mechanical effects has been presented for FinFET structure for a channel length of 30 nm, fin thickness of 10 nm, and fin height of 30 nm. For the purpose of validation of our analytical model, the results obtained have been compared and contrasted with reported simulated results as well as experimental results.

Figure 4.3 shows the variation of surface potential with distance along the channel length obtained on basis of our model and reported simulation results. The device parameters used for the analysis are shown within the figure. It can be seen from the figure that there is a good match between the reported result and result obtained through our modeling at any point along the channel length from source to drain. It can be observed that the potential initially falls to a minimum value at around the center of channel length and then monotonically increases at the drain end. At any point along the channel length, our model predicts a lower value of surface potential as compared to the simulated results. The small deviation seen in the results might be due to variation of carrier mass due to quantum confinement at an applied drain and gate voltage of 0.4 V and 1 V, respectively.

Figure 4.4 shows the variation of three-dimensional surface potential profile in the active region of the device. It can be seen from the figure that there is an increase in the potential along the channel length toward the drain end. It can be also be

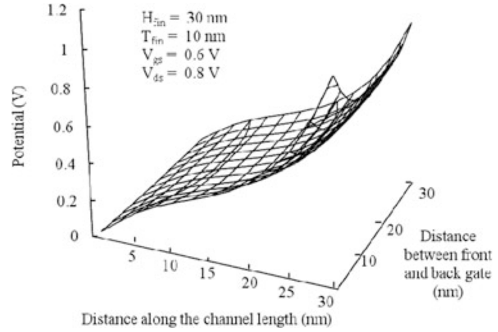

Fig. 4.4 3D potential plot of FinFET for 30 nm channel length

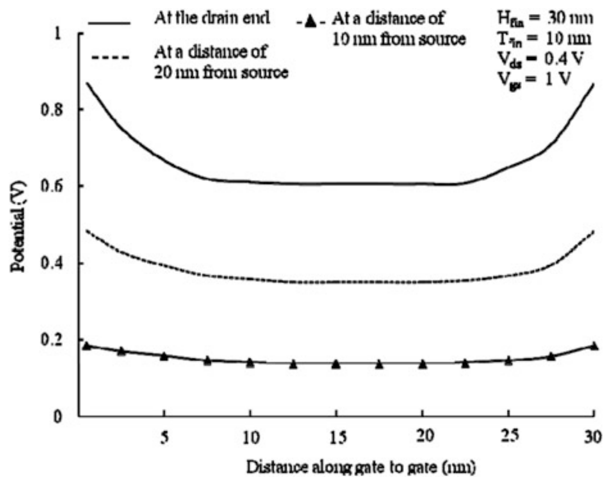

Fig. 4.5 Potential variations from front gate to back gate at various positions along the channel length

observed that the potential variation from the gate to gate at drain is more pronounced as compared to the variation at the source end. This is due to a large transverse as well as longitudinal direction electric field within the channel near the drain end as compared to source end.

The variation of channel potential from front gate to back gate at various distances from source side for fixed drain and gate bias is shown in Fig. 4.5. The gate length, fin height, and thickness have been taken as 30 nm, 30 nm, and 10 nm, respectively. It can be seen from the figure that as we move from source end of the gate to the drain end of the gate, there is substantial increase in the potential at any point in the channel. This is attributed to the increased value of longitudinal electric field at the drain end on application of a drain to source voltage. It can be further observed that near the source end, the potential is almost constant as one moves from front to back gate. But near the drain end, the variation of potential near either of the gates is very drastic. This is because of larger effective gate voltage at the drain end of the device as compared to the source end. This also implies that the

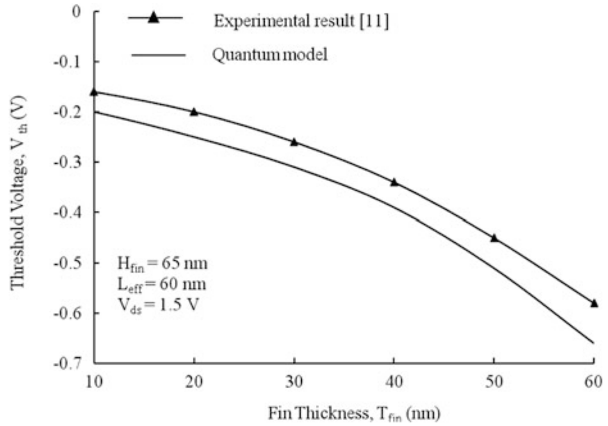

Fig. 4.6 Variation of threshold voltage with Fin thickness for our proposed QM model, classical model, and experimental reported result [7]

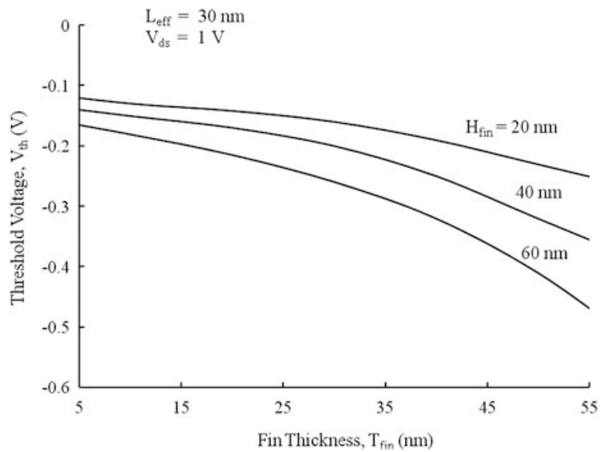

Fig. 4.7 Variation of threshold voltage with fin thickness for various fin height

longitudinal electric field is enhanced near the Si–SiO_2 interface due to its proximity to metal gates.

Variation of threshold voltage with fin thickness for our quantum mechanical model, classical model, and experimental results has been shown in Fig. 4.6 for the purpose of comparison. A threshold voltage roll-off with fin thickness is observed for both theoretical and experimental results. The fin thickness is varied from 5 to 55 nm. The percentage roll-off for our model is 77 % and that for experimental result it is 75 %. It can be inferred, therefore, that there is a close match of percentage variation between our results and experimental measurement, given the fact that the device process parameters undergo fluctuations at such low dimensions.

Figure 4.7 shows the variation of threshold voltage with fin thickness for varying fin height. It can be seen from the figure that as the fin height increases, the rate of reduction of threshold voltage with fin thickness also increases. Moreover, the

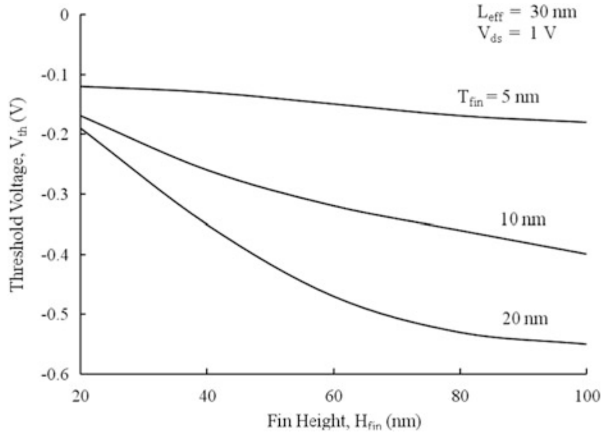

Fig. 4.8 Variation of threshold voltage with fin height for various fin thickness

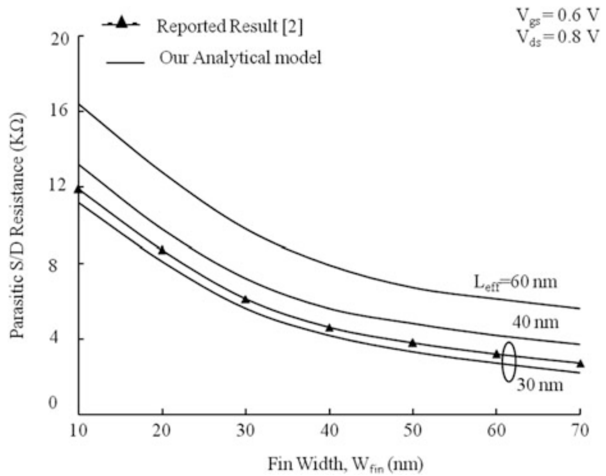

Fig. 4.9 Variation of parasitic S/D resistance with varying fin width for proposed analytical model and reported result [8]

absolute value of threshold shows an enhancement with larger fin thickness. This is because at larger fin thickness, the top gate of the fin is able to control the channel charge to a lesser amount. Hence, there is an increase in threshold voltage. It can be further seen that as fin thickness increases, the transverse electric field reduces and hence a larger gate voltage is reduced in order to form channel, thereby increasing threshold voltage.

The Variation of threshold voltage with fin height for varying fin thickness is shown in Fig. 4.8. From this figure, it may be seen that as the fin thickness increases, the rate of reduction of threshold voltage with fin height also increases. This is because as the fin thickness increases, the effective area under the gate also increases, thus increasing threshold voltage.

Figure 4.9 shows the variation of parasitic S/D resistance with varying fin width for our proposed analytical model and reported numerical result [8] for the purpose

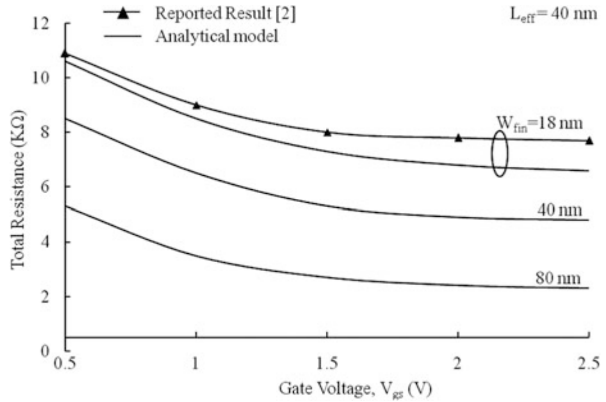

Fig. 4.10 Variation of total resistance with variation of gate voltage for varying fin width

of validation for all fin width. A close match is found between the two results for channel length of 30 nm.

It can be seen from the figure that as the fin width increases, there is a decrease in the parasitic resistance for all values of channel length. As the fin width increases, the total area through which drain current flows also increases. This results in a decrease in the parasitic resistance. Further it is observed that for a fixed fin width, as the channel length increases, there is an enhancement in the parasitic S/D resistance. This can be inferred from the fact as the channel length decreases, quantum confinement along the S/D direction becomes more extensive. This results in an enhancement in the mobility of charge carriers which in turn increase the drain current and hence the parasitic S/D resistance decrease.

Figure 4.10 shows the variation of total resistance between S and D with variation of gate voltage. The results obtained by our analytical model have been compared with the reported numerical result [8] for $W_{\text{fin}} = 18$ nm. The variation is also shown for fin width of $W_{\text{fin}} = 40$ and 80 nm. It is observed that as the fin width increases, there is almost linear decrease in the total resistance for a fixed applied gate voltage. Further for large gate voltage, the total resistance becomes almost independent of applied gate voltage.

4.7 Conclusion

In this chapter, a full 2D quantum mechanical analytical modeling has been presented in order to evaluate the 2D potential profile within the active area of FinFET structure. The key issues related to device parameters and structures are also shown in the chapter. The variation of potential from gate to gate is also reported in this chapter. For potential profile, there is close match between our results and reported experimental results. The results obtained would be useful to design device and for fabricating future nanoscale devices. Various potential

profiles such as surface, back to front gate, and source to drain potential have been presented in order to appreciate the usefulness of the device for circuit simulation purposes. Further, in this chapter, the detailed study of threshold voltage and its variation with the process parameters is presented for our proposed devices and a close match is obtained with the results through analytical model and reported experimental results.

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