Chapter 13
Single-Electron Tunneling Transistors Utilizing Individual Dopant Potentials

Daniel Moraru and Michiharu Tabe

Abstract For many decades since the invention of the transistor in 1947, the dimensions of transistor channels have been continuously downscaled so that more and more functionality can be incorporated into one chip. However, nowadays, critical dimensions of transistors enter into the real nanoscale and fundamental limitations, in physics and technology, raise serious challenges in front of further miniaturization. A conceptually different operation mechanism for the next-generation transistors must be considered. In this framework, we focus on transport characteristics arising from single-electron tunneling via individual dopant atoms, the basic operation mode of *single-dopant transistors*. Single-dopant transistors are devices that make use of individual dopant potentials as natural, ultrasmall quantum dots. In this chapter, we outline basic results related to our research on single-dopant transistors, after briefly introducing the concept and fundamental physics of their operation. First, Kelvin probe force microscopy is used for direct observation of individual dopants in the channel of transistors under normal operation. Next, focus falls on the electrical characteristics indicating single-electron tunneling via individual donor atoms in different temperature ranges. Finally, a domain of dopant-based applications is outlined at the end of the chapter, opening the door for the development of atomic-level electronics.

13.1 Introduction

Since the invention of the transistor in 1947, fundamental research on silicon-based transistors allowed a continuous reduction of their critical dimensions, closely following the trend predicted by the famous Moore's law [1]. In spite of predictions

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of the end of the downscaling trend at different stages of the transistor's evolution, the limitations were overcome by technological innovation and focused research. However, nowadays, commercial transistors reached channel dimensions on the order of only several tens of nanometers. It becomes obvious that fundamental and technological limits of the transistors will soon become an insurmountable barrier in front of further miniaturization.

One of the main problems that nanoscale transistors are facing is related to the discrete distribution of dopant (impurity) atoms in the channel. Together with the reduction of channel dimensions, the number of dopant atoms existing in the channel is also strongly reduced [2]. One important research direction is oriented toward understanding [3–5] and improving the impact of the discreteness of the dopant distribution [6, 7] by advancing the doping processes and fabrication technology. This research provides valuable information on the basic physics that could be dominant in nanoscale and could allow several more generations of downscaling. Nevertheless, it is obvious that a radically new transport mechanism must be considered for the later generations of electronics. Alternative technologies, such as FinFETs [8] or a variety of other new approaches [9], have been studied as viable alternatives for conventional silicon transistors, but these new technologies still require more study and other alternatives may be available.

As a significantly different approach, our group, along with several other groups around the world, focused on a different research direction. This approach continues on the basis of devices still built on the well-developed silicon platform and using knowledge accumulated through decades of experience for this material. The transport mechanism, however, is significantly different than for the conventional silicon devices, i.e., *single-electron tunneling mediated by individual dopant atom potential wells*, working as tiny quantum dots (QDs). Over the past few years, several papers have been published on the topic of *single-dopant transistors*, revealing various fundamental aspects of these basic devices [10–16].

The basic principle of single-dopant transistor operation is illustrated in Fig. 13.1 in an ideal design. We can imagine that, in a nanoscale silicon channel, between well-defined source and drain leads, one dopant atom can be introduced. For instance, let's consider the situation of a phosphorus (P) donor atom between *n*-type source and drain leads. When such a system is formed in a field-effect transistor (FET) structure, a gate can control the potential of the channel and, implicitly, the potential at the donor location. In particular, for negatively large gate voltages, V_G, the channel will be depleted of electrons, which means that the donor atom will also be positively ionized by removing its extra electron. Under these conditions, the ionized donor atom (P^+) introduces a Coulomb potential well in the channel, which can be treated as a natural, really atomic QD. When V_G is swept gradually in the positive direction, the donor's ground state is aligned with the lead's Fermi level, and electrons can be transported from source to drain by tunneling. In particular at low temperatures, where thermally activated carriers are limited, this tunneling mechanism will allow the observation of electrical characteristics ($I_D - V_G$ characteristics) containing a current peak. This mechanism is basically similar to the case of conventional single-electron transistors

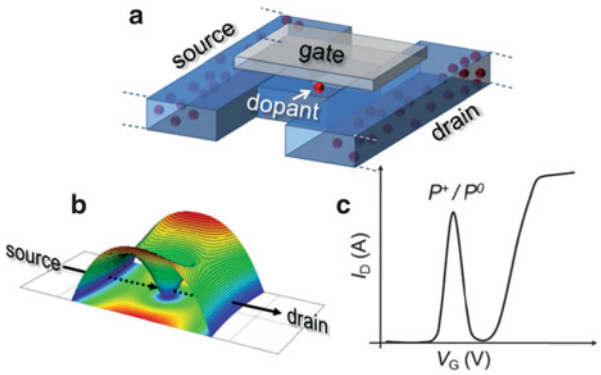

Fig. 13.1 (**a**) An ideal structure of a single-dopant transistor, with one dopant (e.g., a P donor) located between *n*-type source and drain leads. (**b**) Electron potential landscape induced by an ionized donor in the channel. The donor potential well works as a quantum dot. (**c**) Expected $I_D - V_G$ characteristics, exhibiting one peak corresponding to the one-electron occupancy of a regular donor atom at usual temperatures

(SETs) with QDs artificially designed, but in *single-dopant transistors* the QD is induced by a single dopant.

Considering typical dopants for silicon, such as phosphorus (P) and arsenic (As) as donors or boron (B) as acceptor, it is known that such dopants can basically accommodate only one extra carrier (electron or hole) at usual temperatures [17, 18]. A second electron/hole may be introduced in a so-called shallow dopant, but its binding energy is so small (only a few meV) [19] that it is not expected to be observable in usual transport measurements, unless the temperature is maintained within the cryogenic range. Hence, in the $I_D - V_G$ characteristics, a single current peak is expected to be seen, corresponding to tunneling transport via a single donor in the channel before the regular FET characteristics set in. This single peak can be considered as a basic feature to identify single-dopant transistor tunneling operation.

In realistic devices, however, it is still quite challenging to precisely position one dopant atom in the channel. Therefore, most devices investigated so far in terms of individual dopants contain dopants in the channel which either randomly diffuse from the highly-doped source and drain electrodes [10, 12, 14, 15] or are intentionally (randomly) doped with a relatively low doping concentration [11, 13]. In both situations, individual dopants can be addressed by electrical measurements and single-dopant transistors can be identified, albeit not necessarily in all devices studied. These multiple-dopant channels are the systems that will be mainly treated here.

In this chapter, we focus on three main points essential to elucidate for a complete and smooth further progress of single-dopant devices. *First*, in Sect. 13.2, we address the issue of *dopant observation in devices under normal operation*. We employ a nondestructive method, low-temperature Kelvin probe force microscope (LT-KFM), which offers improved capabilities for dopant characterization in devices under normal operation conditions. A *second* issue,

described in Sect. 13.3, is the *identification of single-electron transport via individual dopant atoms* even in transistor nano-channels containing more than just one dopant. We demonstrated that, in spite of the presence of a large number of dopants, i.e., in dopant-rich environments, it is still possible to electrically address one or only a few dopant atoms, which allows some flexibility in designing single-dopant devices. Section 13.4 presents our approach to push the operation temperature of single-dopant transistors toward room temperature, for practical applications. We proposed a specific channel nano-design that allows an enhancement of the dopant's tunnel barrier and, implicitly, higher tunneling-operation temperatures. *Finally*, in an attempt to outline a new world of *atom-level applications starting from individual dopants*, we briefly present in Sect. 13.5 some recent results of our research on several functionalities of dopant-based devices, originating either from dopant–dopant or dopant–photon interactions.

13.2 Charging in Individual Dopants Observed by Low-Temperature Kelvin Probe Force Microscopy

As outlined so far, the individuality of dopants becomes more significant in the electrical characteristics of nanoscale transistors and it even gives rise to a new family of devices, *single-dopant devices*. In this background, it is crucial to observe directly the spatial distribution of ionized dopant potentials in the device channel in order to, eventually, correlate it with the electrical characteristics. Several reports on shallow-dopant profile or carrier concentration measurements by different techniques are available in literature, but they usually require special preparation of the samples and/or cannot perform accurate measurements on dopants located in the channel of devices under operation. Scanning tunneling microscopy (STM) was used to identify and characterize individual dopants in the top atomic layers from the surface [20–22]. Scanning capacitance microscopy (SCM) [23], for instance, is another interesting technique that provided information about capacitive coupling between a tip and the charges in a sample, but it does not yet have the required accuracy. Atom probe tomography [24–26], another promising technique for eventually resolving the three-dimensional distribution of dopant atoms in nano-channels, is a destructive technique and does not yet allow high-precision measurements of all dopants in the structures.

One attractive technique that could overcome most fundamental limitations is Kelvin probe force microscopy (KFM) [27], which allows, in principle, measurements with higher spatial resolution and higher sensitivity to charges located deeper in the device structure. We already demonstrated the possibility of observing individual dopants (both donors and acceptors) in the channel of devices under normal operation, by using our own designed low-temperature Kelvin probe

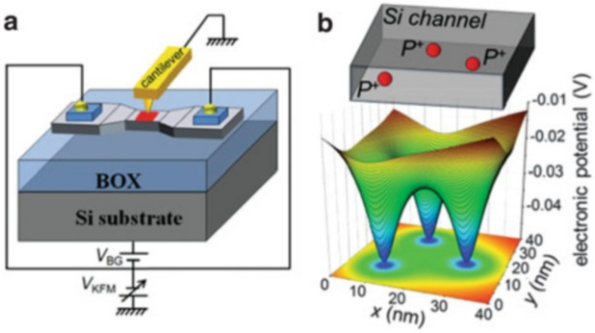

Fig. 13.2 (**a**) Schematic representation of the KFM measurement setup. SOI-FET (without top gate) is biased from an external circuit as a regular transistor, while a cantilever scans over the channel surface and measures the electron potential. The device and measurement system are included in an ultrahigh vacuum chamber, and measurements can be performed at variable temperatures. (**b**) Calculated electronic potential landscape expected to be induced by an arrangement of a few ionized P donors in the device channel (after [31])

force microscopy technique (LT-KFM) [28–30]. Our LT-KFM technique allows KFM measurements in ultrahigh vacuum chamber, at temperatures from 13 to 300 K, with the possibility of biasing the devices with regular FET external biasing circuit [28]. More recently, we analyzed the effect of a gate voltage (substrate voltage for the KFM devices) on the charge occupancy of individual donors in a nanoscale channel [31]. By comparing results at 13 and 300 K, we could observe not only electronic potential wells induced by the phosphorus (P) donors but also distinct effects of electron injection in P donors, reflecting different electron transport mechanisms.

For the purpose of KFM measurements, we fabricated silicon-on-insulator (SOI) FETs without top gate, with the *p*-type Si substrate ($N_A \cong 1 \times 10^{15}$ cm^{-3}) working as back gate, as schematically shown in Fig. 13.2a. Channel thickness is about 15 nm, with length and width of about 500 and 200 nm, respectively. Top Si layer was uniformly doped with phosphorus, in a structure similar to that of a junctionless transistor, at the concentration $N_D \cong 1 \times 10^{18}$ cm^{-3}, which corresponds to an average inter-donor distance of ~10 nm. The sample was inserted in the KFM measurement chamber in ultrahigh vacuum ($<5 \times 10^{-7}$ Pa), and the electrodes were connected to external voltage sources. We measured the KFM surface potential images in the channel region of the device. Source and drain electrodes were grounded in this experiment, which allows us to study the static charge distribution in the channel in the absence of current flow. When several ionized P donors exist in the scan area, as shown in Fig. 13.2b, it is expected that the potential landscape will contain Coulomb wells induced by individual donors.

A KFM potential image for the back gate voltage $V_{BG} = -3$ V, taken at 13 K, is shown in Fig. 13.3a. The applied V_{BG} works to ionize the donors and deplete electrons from the SOI channel [28–30]. Hence, the channel potential contrast is

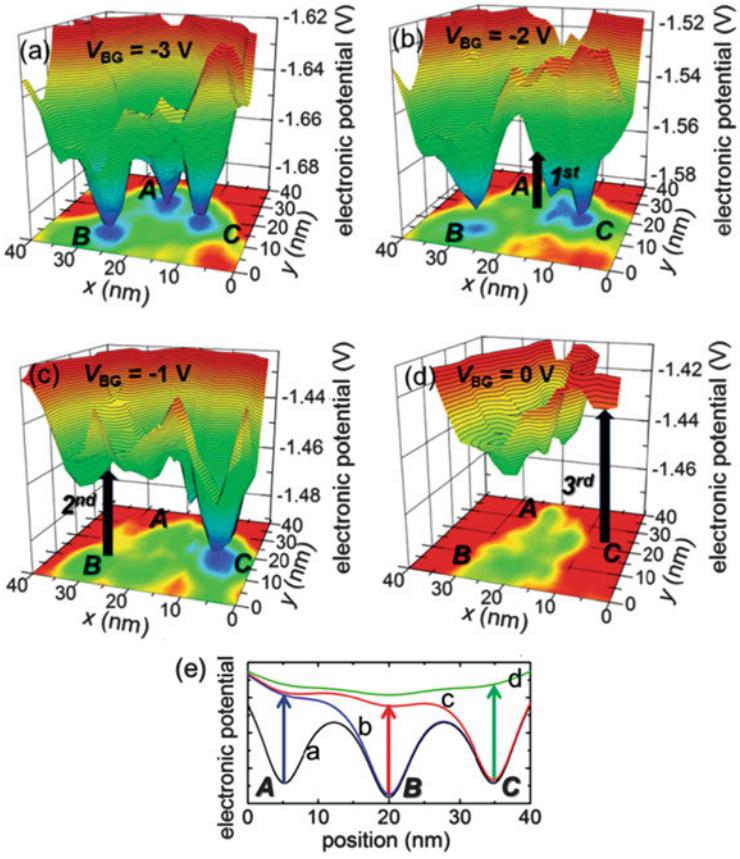

Fig. 13.3 (**a**–**d**) Electronic potential landscape measured by LT-KFM at low temperature ($T = 13$ K), with back gate voltage, V_{BG}, increasing from -3 to 0 V in 1 V steps. Successively, the potential wells of individual P donors vanish one by one, as also illustrated schematically in (**e**) (after [31])

primarily formed by the ionized P donors. In the shown area, three potential wells can be seen. Each well has a spatial extension of ~10 nm and an electronic potential depth of 10–40 mV. These features suggest that each potential well is created by a different ionized P donor. In order to allow injection of electrons from grounded source and drain electrodes into the channel, V_{BG} is increased from -3 to 0 V in 1 V steps. As a result, significant changes in the potential landscape can be seen. First, at $V_{BG} = -2$ V (Fig. 13.3b), one of the potential wells, A, disappears, while, at $V_{BG} = -1$ V, a second potential well, B, successively disappears (Fig. 13.3c). The last remaining potential well, C, disappears at $V_{BG} = 0$ V (Fig. 13.3d). These potential changes are illustrated schematically in Fig. 13.3e as successive flattening of neighboring dopant-induced potential wells. These localized modifications are ascribed to successive single-electron filling in donors, since it is expected that each

P donor potential is almost neutralized and compensated by the capture of one electron.

This situation is significantly different at higher temperatures [31]. For a temperature of 300 K, it was found that, regardless of the V_{BG} values, all donors are thermally activated, i.e., ionized. Therefore, spatially extended free electrons screen the dopant potentials and electron charging was observed only as delocalized potential increase by successively-injected electrons.

The results shown here illustrate the fact that LT-KFM is able to detect not only the potential of individual dopant atoms but also the electron injection, one by one, into dopants in a strongly localized manner. It also reveals the important effect of increasing temperature on the localization of the electrons at the level of individual dopants. These are the grounds on which the operation of single-dopant devices is established, since this operation consists of single-electron tunneling via individual dopant atoms, i.e., the current is formed by successive single-electron tunneling via a dopant atom. Based on this knowledge, we proceed to the electrical characterization of doped-channel nanoscale transistors with the purpose of revealing the features of tunneling transport mediated by individual dopant atoms.

13.3 Single-Electron Tunneling via an Individual Dopant Atom in Nanoscale Silicon Transistors

As revealed by the direct measurements using LT-KFM and presented in the previous section and our previous work [31], it is now possible to directly observe the fact that an ionized dopant atom works as a quantum dot (QD). When one dopant is coupled to electrodes in a transistor structure, electrons should be transported between source and drain via the donor-QD by successive injection into and extraction from the dopant well. Ideally, precise placement of one dopant in the channel is desirable and it has been recently demonstrated even experimentally by an STM atomic manipulation technique [16], but it remains quite complex for full CMOS compatibility. Nanostructures containing many dopant atoms can be, on the other hand, fabricated with conventional doping techniques. Under these conditions, it is essential to understand whether electron transport can be controlled by individual dopants even in such many-dopant environments.

In these structures, the overall potential landscape is not modulated by only one dopant atom but by the superposed potentials of many dopants [13, 28–30, 32]. For nano-channels doped with phosphorus (P) donors in a random process, the lowest electronic potential is most likely formed close to the channel center as a consequence of the entire set of dopants and the superposition of their long-range potentials [13]. When the channel minimum conduction band energy is shifted close to the source Fermi level by the gate voltage, transport occurs through the dopant-induced QDs. We demonstrated, by experiments and simple simulations, that even in such dopant-rich environments, individual P donors can be addressed

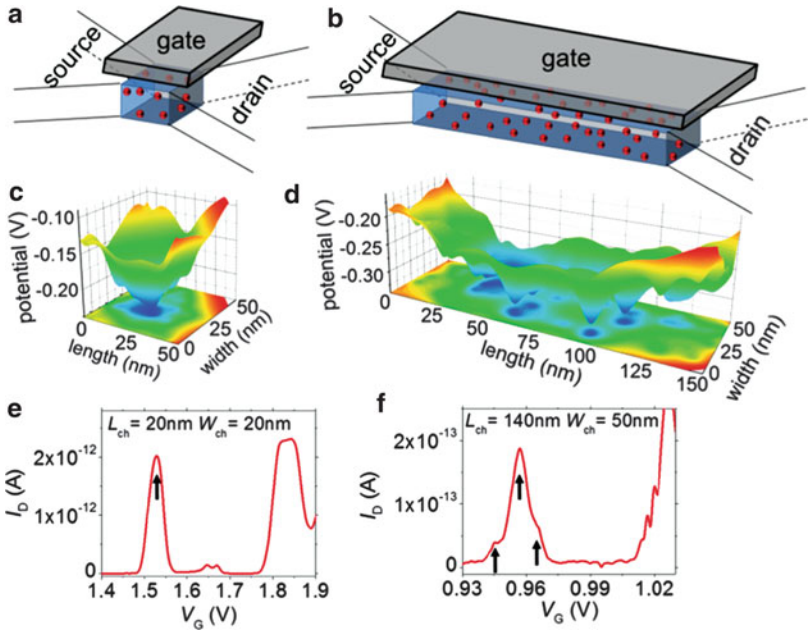

Fig. 13.4 (**a**, **b**) Schematic representation of the P-doped channel of two devices, with short and, respectively, long channel length. (**c**, **d**) Channel electronic potential landscapes calculated by the superposition of randomly located P donors in the channels shown in (**a**) and (**b**), respectively. (**e**, **f**) $I_D - V_G$ characteristics measured at low temperature ($T = 17$ K) and for small source-drain bias ($V_D = 10$ mV). *Arrows* indicate inflections (sub-peaks) seen on the first observable current peak (above the noise level) (after [16])

electrically by monitoring the electrical characteristics, i.e., the $I_D - V_G$ characteristics, in particular at low temperatures and small source-drain biases.

For understanding single-electron transport properties of P-doped nano-channel FETs, we fabricated devices using similar processes as for the ones used for KFM observation. However, channel constrictions of smaller lengths (20–150 nm) were defined between the two wider fan-shaped pads of Si for source and drain (as illustrated in Fig. 13.4a, b). After gate oxidation for a 10 nm-thick SiO_2, a wide Al front gate was formed on top of the nanoscale-doped channel. Doping concentration was estimated to be $N_D \cong 1–5 \times 10^{18}$ cm^{-3}, which means that, in the device channel, there are many dopants, not only one, that modulate the channel potential.

Figure 13.4c, d shows typical examples of dopant-induced potential landscapes simulated for random arrangements of dopant atoms with Coulomb potentials (all calculated [32] for doping concentration $N_D = 1 \times 10^{18}$ cm^{-3}) in a short nanostructure (Fig. 13.4c) and a long nanostructure (Fig. 13.4d). In certain locations of the channel, potential minima will be formed and conduction starts when the channel minimum potential is shifted close to the source Fermi level by applying a positive V_G to the gate. It is expected that one dopant or an array of a few dopants

with comparable potentials will control the initial stages of transport. The $I_D - V_G$ characteristics contain non-periodic current oscillations, which can be ascribed to transport by single-electron tunneling through dopant-induced QDs. The two lower panels in Fig. 13.4 (e, f) show the first peaks (first observable current peaks above 10 fA, when V_G is increased) of $I_D - V_G$ characteristics measured at 17 K for FETs with constriction lengths of 20 nm and 140 nm, respectively. As a statistical tendency, while the short-channel FETs exhibit smooth single-peak (or double-split peak) current oscillations, longer-channel FETs typically exhibit multiple-split peak features (or inflections). The observed inflections are marked by arrows in the $I_D - V_G$ characteristics. The splitting of a current peak may be treated as an indication of the formation of a multiple-QD array in the channel, while the number of sub-peaks can be considered an indication of the number of QDs [33]. These results suggest, thus, that in the shortest channels, containing a small number of donors, it is usual to observe transport mediated by single P donors. The situation becomes more complex in longer channels, in which it is likely that arrays of several P donors control the transport at the initial stages.

To provide a statistical image of our results, we counted the number of sub-peaks in the first measured current peak for 5–10 devices for each channel length (L_{ch}) value (L_{ch} was changed in 11 steps from 20 to 150 nm). Figure 13.5a contains the statistical results of the average number of sub-peaks (dot symbols) and the standard deviation from the average (error bars), extracted from the experiments. Although the dispersion of the data is considerable, it is obvious that there is an increasing trend of the number of sub-peaks (i.e., the number of dopant-induced QDs) with L_{ch}. In order to further confirm this point, we performed simulations of dopant-induced potential landscapes for a statistical number of cases. For simplicity, we studied the behavior of isolated channels in the absence of the influence from source/drain doping. We considered nanostructures of different lengths (20–150 nm) but same width (50 nm) and thickness (10 nm). In these structures, we randomly introduced dopants with Coulomb potentials to a concentration $N_D = 1 \times 10^{18}\,cm^{-3}$. The potential at each point is the result of the superposition of all dopant potentials. For monitoring the QD array structure, we choose a potential window of 30 mV from the bottom of the channel potential. This value is close to our approximate estimation of the charging energy from the experimental characteristics. Figure 13.5b plots the average number of QDs (dot symbols) obtained from 50 different dopant arrangements for each L_{ch} value, together with the error bars. The results indicate that the number of QDs exhibits, indeed, an increasing trend as a function of L_{ch}. The trend is in good agreement with the experimental results, which confirms that the number of dopant QDs is statistically controllable by the channel length. More detailed analysis is required for providing more definite conclusions on the quantitative trends.

Based on the simulations, it is also possible to evaluate how many P donors create the estimated QDs. For this purpose, we defined a potential window with the lower level fixed at the bottom of the potential in the channel. We gradually increased the higher level of the potential window and monitored the number of dopants and the number of QD inside the window, as illustrated in Fig. 13.5c.

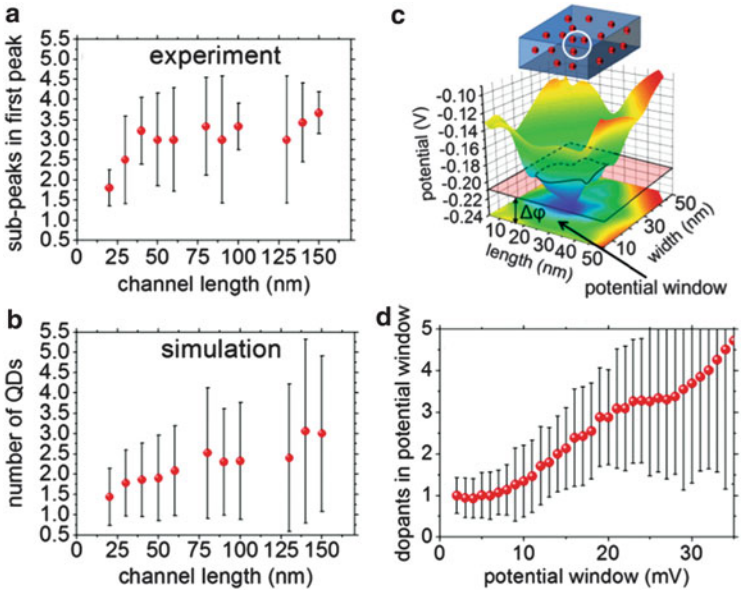

Fig. 13.5 (**a**) Number of sub-peaks (inflections) observed within the envelope of the first current peak (observed at lowest V_G's above the noise level) as a function of channel length, extracted from 5 to 10 devices for each value of the channel length. (**b**) Number of QDs observed within a potential window of 30 mV, starting from the minimum channel potential, as a function of channel length. The data was extracted from a statistical number of simulated dopant-induced potentials for a $50 \times 50\ \text{nm}^2$ channel area. *Error bars* are also indicated on both graphs. (**c**) An illustration of the basic procedure for evaluating the number of donors responsible for transport. (**d**) Number of dopants within a variable potential window, defined with the lowest level corresponding to the bottom of the channel potential

Figure 13.5d shows the number of dopants per QD statistically estimated from simulations for $50 \times 50\ \text{nm}^2$ nanostructures, as shown above, for a doping concentration, $N_D = 1 \times 10^{18}\ \text{cm}^{-3}$. It can be observed that, within a window of ~10 mV, each QD contains on average one dopant, i.e., the observed QDs are formed by individual P donors. Above ~30 mV, the average number of dopants in each QD is ~3. These findings indicate that, for the first observable current peaks, when the source Fermi level most likely "scans" the bottom of the channel potential, the QDs responsible for tunneling transport are mostly induced by individual donors. Hence, even in such donor-rich environments, single-electron tunneling via single P donors can be identified as the main transport mechanism, allowing us to develop and study *single-donor transistors* with the transport donors coupled (surrounded) by other donor atoms.

At this stage, we demonstrated that single-electron transport through single-dopant dots can be achieved even in randomly doped dopant-rich environments. This is due to the effect of the large number of dopant atoms that create a potential landscape favorable for accessing even a single dopant atom. From these preliminary

results it was also suggested that individual dopants can be identified easier in channels which are significantly isolated from source/drain electrodes [13]. This point was examined in more detail in our next work, in which we also took fully into consideration the quantum effects that should be observable in nanostructured channels.

13.4 Specially Patterned Single-Dopant Transistors with Tunneling Operation at Elevated Temperatures

Recent progress in silicon nanotechnology allowed electrical measurements of electron or hole tunneling through individual dopants located in the channel of silicon transistors. Results reported so far have been mostly obtained for transistors having channels without any special patterns. In these studies, dopants maintain their shallow ground states, and tunneling transport is reported only at low temperatures ($T < 15$ K). In addition, for most reports on single-dopant devices, the final target application is quantum computing [34–36], for which low temperatures are suitable because of longer coherence time. Until recently, there were no reports focused on tunneling operation via dopants at elevated temperatures, despite the fact that, for applications toward CMOS-based electronics, higher tunneling-operation temperature is crucial. Several conditions must be met in order to be able to observe clear signatures of single-electron tunneling via dopants at high temperatures. One important requirement is for the charging energy to be significantly larger than k_BT, which is a first limiting factor for shallow dopants (charging energy is known to be on the order of several tens of meV only). Furthermore, at high temperatures, thermally activated transport, i.e., transport over the tunnel barrier of electrons found in the high-energy tail of the Fermi–Dirac distribution, may become quickly dominant. For practical applications, considering this last limiting condition, we focus on developing a channel design that would allow not only identification of single-electron tunneling transport via individual P donors but also operation at elevated temperatures [37].

In order to enhance the tunnel barrier height and, implicitly, increase the temperature up to which purely tunneling operation can be maintained, we attempted to take advantage in device design of phenomena that are specific for dopants in nanostructures. For single dopants embedded in silicon nanowires, it was recently found by simulation studies [38, 39] that dielectric confinement (and, in extremely small nanostructures, even quantum confinement) leads to a significant modification of the electronic properties of dopants as compared with the bulk Si case. In particular, it was reported that the ionization energy of dopants in nanowires is drastically increased, leading to an effective deactivation of the dopants and to a loss in conductivity, as observed also experimentally [40]. The significant impact of the dielectric confinement is due, basically, to the fact that dopants embedded in silicon nanostructures are mostly surrounded by dielectric material, and not by a large silicon matrix, as is the case for bulk. Due to this

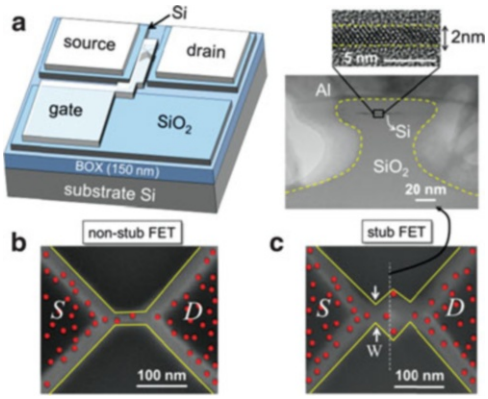

Fig. 13.6 (**a**) Bird's eye view of SOI-FETs studied in this work. As shown on the *right* by the cross-section TEM image, top Si layer is extremely thin (only ~2 nm). (**b**, **c**) Two types of channel patterns (non-stub-channel and stub-channel) were studied, as shown by the SEM top-view images. The boundaries of the channel region are delineated, and P donors are illustrated as red spheres according to some random distribution. In the case of stub-channel FETs, it is possible to find P donors located in the edge of the stub region, where dielectric confinement should be strongest (after [37])

configuration, screening of the dopant's extra charge by the silicon matrix is strongly reduced, leading to a modification of the dopant's ground state, i.e., a further deepening of the ground state below the conduction band edge for the case of a donor. Effectively, such enhanced ionization energy means that the donor's tunnel barrier is also enhanced, which is our main objective for the device design.

Based on the above reports and on our own *ab initio* simulations [13], we focused on specific channel design which could provide optimal conditions for the observation of dielectric confinement effect in P donors randomly introduced in the channels of nanoscale SOI-FETs (as shown in Fig. 13.6a). We found that a promising design consists of a stub-channel, as illustrated in Fig. 13.6c using a scanning electron microscope (SEM) image of one of the smallest devices; a random P donor arrangement is also illustrated for suggesting the possible favorable location of individual donors. For reference, we also fabricated devices without any special pattern of the channel, as shown in Fig. 13.6b. It should be mentioned that, in the vertical direction, donors are embedded in an ultrathin (~2-nm-thick) Si layer (as seen from the cross-sectional transmission electron microscope (TEM) image as inset). For both structures, donors located in the channel should experience significant dielectric confinement effect in the vertical direction. However, only when a donor is located within the edge of the stub region, dielectric confinement effect becomes strong in the lateral direction as well, because it is mostly surrounded by SiO_2, which is quite different than for the case of non-stub FETs.

For non-stub- and stub-channel FETs, $I_D - V_G$ characteristics were measured at a small source–drain voltage, $V_D = 5$ mV. Temperature was changed as a parameter from ~15 to ~300 K. Figure 13.7a, b shows representative sets of $I_D - V_G$

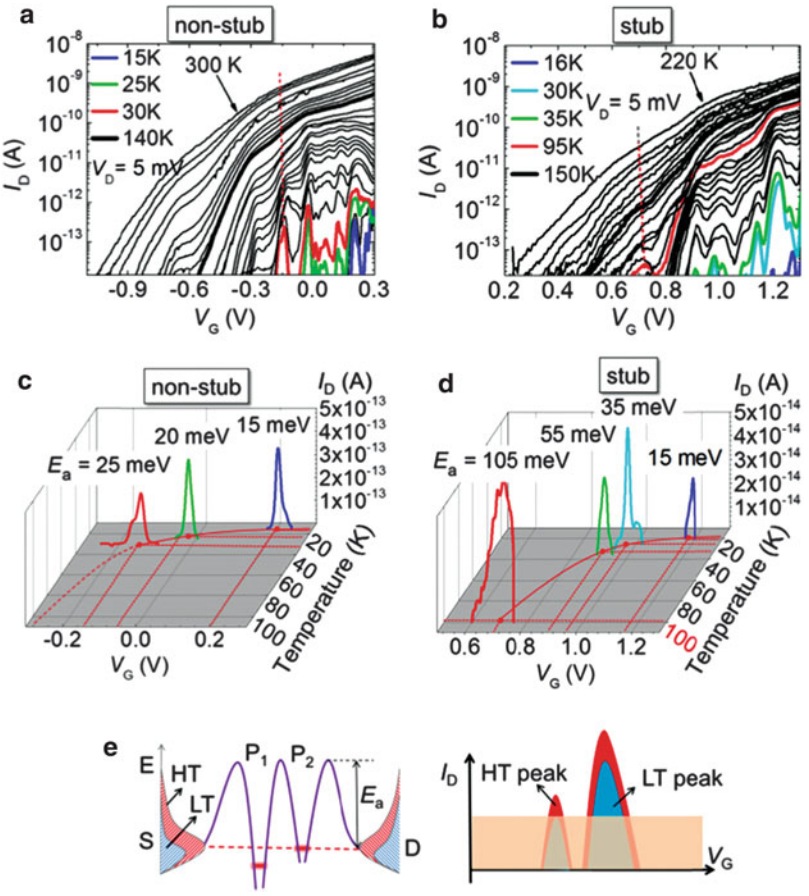

Fig. 13.7 (**a**, **b**) Temperature-dependent $I_D - V_G$ characteristics measured for smallest devices with different channel patterns: non-stub channel [(**a**)] and stub channel [(**b**)]. (**c**, **d**) The last observable current peak (for different temperatures) as a function of both V_G and T. For stub-channel FETs, the final peak emerges at elevated temperatures ($T = 100$ K), the highest temperature reported so far for single-dopant transistors. (**e**) Schematic model of the reason why higher temperature allows the observation of current peaks (after [37])

characteristics for two smallest devices with different channel patterns. At lowest temperatures (~15 K), the $I_D - V_G$ characteristics exhibit a number of isolated current peaks, as seen both in Fig. 13.7a, b. As argued up to this point, these peaks are due to electron tunneling transport through donor-induced QDs formed in the channel. By raising the temperature in the range of 20–100 K, several new current peaks successively emerge at smaller V_G's for both types of devices.

In Fig. 13.7c, d, for clarity, only the temperature-associated lowest-V_G current peaks are extracted from the full $I_D - V_G$ characteristics and are plotted in the V_G-temperature plane. These peaks successively appear with increasing temperature and are ascribed to tunneling via P donors with deeper ground-state energies.

We cannot observe the current peaks of these deep donors at low temperatures (~15 K), since the tunneling rate is too small due to the high potential barriers. (The detectable current level in the present system is around ~1×10^{-14} A.) With increasing temperature, however, due to broadening of the Fermi–Dirac electron distribution in the reservoir and other thermal effects [41], as illustrated in Fig. 13.7e, the tunneling rate is enhanced and current peaks successively emerge, exceeding the detectable current level. It is found that, for the stub-channel FET, the last emerging current peak appears at $T \cong 100$ K (Fig. 13.7d), which is the highest temperature reported so far for single-dopant transistors operating in single-electron tunneling (SET) mode. Moreover, the SET feature survives as a prominent hump up to ~150 K, as shown by the thick $I_D - V_G$ curve in Fig. 13.7b. At high temperatures, above ~100 K, a number of SET peaks are significantly broadened and overlap each other, indicating a change from the Coulomb blockade mechanism to the resonant tunneling mechanism, primarily due to the reduction of the tunnel resistance.

From the temperature dependence of the electrical characteristics, such as data shown in Fig. 13.7a, b, it is possible to extract the barrier height at different V_G's based on the analysis of Arrhenius plots. In particular, these values are most reliable as extracted from the data taken at highest temperatures, where it is certain that the thermally activated transport is the dominant transport mechanism [10]. Details of this extraction procedure and the results as a function of device dimensions can be found in our work [37]. Here, for simplicity, the values extracted for the barrier height for V_G's corresponding to the last observable current peaks are indicated in Fig. 13.7c, d. It can be seen that, for the peak emerging at the highest temperature of ~100 K, the barrier height is large (~100 meV), much larger than the value known for the ionization energy for P donors in bulk Si (~44 meV). These findings strongly suggest that, in stub-channel FETs, P donors, most likely located in the edge of the stub region, are exposed to a strong dielectric confinement which, as predicted by theory, leads to the detectable enhancement of their ionization energy (barrier height).

The findings described above and insights provided by *ab initio* simulations [37] suggest that the nano-channel's specific design is the critical factor in enhancing the tunneling operation temperature of single-dopant devices toward room temperature. If such operation can be realized by further optimization of the channel design or another innovative technique, single-dopant devices can be considered in the future for more practical applications. In this sense, it is necessary to investigate and clarify what kind of applications are suitable or achievable using dopant atoms in silicon nanodevices. The preliminary research that we carried out on this wide topic [42] and more recent progress will be briefly outlined in the following section.

13.5 Extended Applications of Dopant-Based Devices

In the previous sections of this chapter, we focused mainly on the characterization of individual dopants, either by KFM observations or by electrical characteristics. However, it is natural to expect that more complex functionality can be obtained

when dealing with systems of more than one dopant, because of the interactions between dopants, as well as interactions with external factors, such as absorbed photons and phonons. In order to propose single-dopant or multiple-dopant devices as viable candidates for future generations of electronics, it is essential to study possible functions involving a few dopants in silicon nanostructures.

In recent years, we addressed several topics dealing with functionalities arising from multiple-dopant systems and dopant–photon interactions [42]. However, it is beyond the scope of this chapter to enter deeply into the details of each topic, and more information can be found in our relevant publications. Here, we would like to offer only an overview of the wide range of possibilities that this field can provide, not only in terms of innovative applications, built from the fundamental level of atoms, but also regarding new physics possible to be revealed by utilizing these systems.

A single dopant, either a donor or an acceptor, can be indeed the building block of an atomic-level transistor. As we presented earlier, it is important to make efforts in research toward improving their fabrication and their operation so that they can be realized in a reproducible, reliable, and efficient manner. But, if in the vicinity of such a transport donor, for instance, another donor can be found, then we have the core unit for a dopant-atom-based memory device. The satellite donor atom can store an electron as a single-electron memory node and its charge state can be detected using the single-electron tunneling current flowing through the transport donor. We demonstrated such operation by carefully examining the charging effects detectable in nanoscale transistors containing more than one donor [43]. We found that the interaction of donors with nearby Si/SiO_2 interface plays also a key role in the transfer of one electron between donors. This kind of operation basically takes us one step further, now into atomic scale, following previous demonstrations of single-electron memories using semiconductor QDs [44, 45].

A similar observation of single-electron trapping and detrapping in a dopant atom was done under light illumination, in devices with basically the same structure, but only lacking the metallic top gate. We found that, by the absorption of individual visible-light photons into an ultrathin SOI channel and subsequent generation of an electron-hole pair, the elementary charges, separated in the electric field, can be captured by the ionized donors (in an *n*-doped channel). The electron is released after some time, leading to the observation of random telegraph signals (RTS) that depend strongly on light intensity [46]. This is a fundamental demonstration of single-photon detection using an array of QDs induced by individual donor atoms [47], similar in principle to previous works on photon detectors using semiconductor QDs [48, 49]. The impact of photogenerated carriers can also be detected in nanoscale *pn* junctions, where both donors and acceptors interact in creating appropriate conditions for the capture of elementary charges in individual dopant atoms [50]. In such nanoscale *pn* junctions, we also found that the dopant properties drastically change, most likely as a result of significant dielectric confinement and interdiffusion of donors and acceptors. This was understood from direct measurements of LT-KFM on nanoscale *pn* junctions, which revealed special properties of dopants in the depletion layer [51].

By considering systems with three or more dopants, e.g., P donors, we demonstrated also single-electron turnstile operation, both by experiments [52, 53] and by simulations [54, 55]. Such single-electron turnstile function was originally proposed using metallic QDs [56], then demonstrated also with semiconductor QDs [57]. These devices were considered attractive because of their ability to control electron transfer not only in space, through a specific array of QDs, but also in time, thus overcoming, to some extent, the stochastic nature of the single-electron tunneling phenomenon. Once realized with donor-atom arrays, it becomes possible to design and implement dopant-atom switches which could work as fundamental building blocks for the integrated circuits of future atomic-level electronics.

It is, thus, possible to design and couple a wide variety of applications starting from the fundamental structure of a dopant atom working as a QD, then involving interaction with neighboring dopants and with individual photons. All the functionalities that could be extracted from the analysis of single-dopant or multiple-dopant transistors will definitely provide the solid foundation necessary for building up the field of *dopant-atom-based electronics*. Exciting physics phenomena at atomic scale in these silicon nanodevices have been already revealed, while others are still expecting to be revealed, making this field a rapidly growing one, with chances to become a viable candidate for future generations of electronics.

13.6 Conclusions

In this chapter, we introduced our basic approach for moving beyond the present limitations that the device miniaturization trend is facing. We suggest that atomic-level electronics can be taken into consideration as an important candidate because it still builds upon the well-developed platform created for silicon nanodevices but focuses on a significantly different transport mechanism as compared to conventional devices: *single-electron tunneling via individual dopant atoms*. Based on this concept, a new family of electronic devices, *single-dopant devices*, can be developed and used to study fundamental physics related to the interaction between elementary charge carriers, single dopant atoms, and single photons.

After briefly outlining the essential points of this conceptual change, we present the direct observation of discrete dopants in operating devices using low-temperature Kelvin probe force microscopy. Then, our research on single-dopant transistors was introduced, starting from our demonstration of tunneling transport via an individual donor even in dopant-rich environments. Channel design can be considered for obtaining improved properties of dopants in nanostructured channels, properties completely different than in bulk silicon and which are promising for allowing eventually room-temperature operation of single-dopant devices. Finally, a range of applications can be designed, and we took a few basic steps by preliminary demonstrations of the feasibility of several dopant-based devices. The findings

included in this chapter, together with a rich and fast-paced development of the field in recent literature, guarantee an exciting future for atom-level electronics, with a smooth transition from present-day silicon-based electronics entering deeper and deeper into nanoscale.

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