Chapter 14
Silicon Nanostructures for Thermoelectric Applications

Massimo Totaro and Giovanni Pennelli

Abstract In this chapter, an overview on silicon nanostructures for thermoelectric applications is presented. After an introduction on the key concepts of thermoelectricity, we show that nanostructuring is one of the most promising solutions for making high efficient thermoelectric devices. In particular, we discuss the use of nanostructured silicon as a good thermoelectric material, due to its abundance, its nontoxicity, and its technological pervasiveness in the society, compared to other materials often proposed in the literature. Furthermore, a top-down process for the reliable fabrication of very complex and large area arrays of silicon nanowires (SiNWs) is shown and discussed. Finally, we show that these networks can be employed for the fabrication of high efficiency thermoelectric generators, and the high reliability and the high tolerance with respect to SiNW width dispersion are demonstrated by means of numerical simulations.

14.1 Introduction

Increasing energy demand and global warming have in recent years generated a burgeoning activity dedicated to the development of low-CO_2 and sustainable energy production technologies [1–3]. Nowadays, electrical power is mainly

M. Totaro (✉)
Center for Micro-BioRobotics @SSSA, Istituto Italiano di Tecnologia,
Viale Rinaldo Piaggio 34, I-56025 Pontedera (PI), Italy

Dipartimento di Ingegneria dell'Informazione, Università di Pisa, Via Caruso 16,
I-56122 Pisa, Italy
e-mail: massimo.totaro@iit.it

G. Pennelli
Dipartimento di Ingegneria dell'Informazione, Università di Pisa, Via Caruso 16,
I-56122 Pisa, Italy
e-mail: g.pennelli@iet.unipi.it

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obtained from fossil fuels and nuclear energy, while the electricity produced by renewable sources (sun, wind, etc.) is only a very small fraction. The transformation of almost all energy sources into mechanical or electrical energy, such as means of transport, industrial processes, or electric power transmission lines, produces always a substantial waste heat, which is in average about the 60 % of the input energy.

Moreover, a significant portion of this waste heat is produced by relatively low energy heat sources ($T < 300$ °C) [4], and there is not yet a technology available to convert this energy into electricity with high efficiency. In the last 10 years, thermoelectric (TE) generation is being more and more considered one of the most promising solutions. The thermoelectric conversion is based on the Seebeck effect [5]. Carriers in metals and in semiconductors transport electrical charge as well as heat. When a temperature gradient is applied to the extremities of a conductor, the mobile charge carriers at the HOT side flow through the device to the COLD contact. At the equilibrium, this temperature gradient generates an electrostatic voltage difference V , and this effect is the basis of thermoelectric energy conversion. Thermoelectrics has several advantages even over photovoltaics [6, 7], always indicated as the best and leading sustainable energy source, because of the endless possibilities to recover waste heat from a huge variety of industrial processes [8–10], and because of the potentially higher efficiency, both vs.conventional Si-based cells and vs. thin-film large-area devices. Furthermore, waste heat can also be recovered from several distributed sources, such as residential heating and automotive exhaust, making TE conversion the ideal solution for localized energy harvesting, without any need of centralized systems and energy transport lines, usually expensive and with several maintenance required.

One of the most limiting factors of thermoelectric generators is the significant portion of the thermal energy lost by Joule effect, due to the finite electrical conductivity of the material, and by direct heat conduction from the hot to the cold region of the device, due to the thermal conductivity of the materials. For this reason, a device with high electrical but low thermal conductivity should be developed. Regrettably, this is hard to achieve with metals, since the two parameters are directly correlated, thus giving very poor TE performances.

As far as now, lead and bismuth telluride compounds present the best TE properties [11], being the most widely used material for TE energy conversion, with an efficiency about 6–8 %. However, such compounds as material for energy generation in very large-scale applications have several disadvantages. First of all, some of these materials are unstable above 1,000 K, due to melting or vaporization, thus they are not suitable for high temperature processes. In addition, the abundance on the Earth's surface of these materials is another factor which limits the development of large-scale applications. Indeed, in an industrial context, the price of a material, due to market request and to its extraction and transformation costs, influences largely the whole device cost, making very unlikely the widespread

use of current thermoelectric systems for waste energy harvesting. Furthermore, low natural abundance is often accompanied by a certain level of toxicity for the environment, and health hazard for people. In particular, tellurium and thallium, which appears in a large number of the high performance thermoelectric compounds presently used, are considered to be highly toxic metals, and this also affects the cost of material packaging and recycling to minimize the environmental contamination. In addition, these materials should particularly be avoided for high temperature processes since they tend to vaporize and release harmful pollutants to the environment.

Finally, in last years the sustainability is commanding ever-increasing attention. It can be viewed as the use of a material in the future without worrying about its availability or its degradation. Sustainability mainly depends on the resource availability, which is the total amount of the material on the Earth's crust, and on the reserve availability, defined as the quantity of the element that is currently possible to extract. From both these points of view, high performance thermoelectric alloys present critical concerns.

On the other hand, silicon would satisfy all the above requirements, since, after oxygen, it is the most abundant element on the Earth's surface, it is not toxic, it is stable even at very high temperatures, and it is sustainable for very large-scale applications [11], as demonstrated by its pervasiveness in the society. Moreover, due to its large employment as leading element in modern microelectronics, and to the impressive technological development of microchip fabrication, the costs related to the material processing, to the system fabrication, and to the distribution into the market are much lower if compared to any other material or compound. Finally, silicon-based thermoelectric modules can be easily integrated in existing electronic systems, giving a significant breakthrough to energy harvesting applications.

Unfortunately, bulk silicon, due to its quite high thermal conductivity, presents very poor thermoelectric performances [12]. Interestingly, in recent years, it has been demonstrated, as we discuss below, that in silicon nanostructures, and in particular in silicon nanowires, nanoscale dimensions can enhance the surface scattering of phonons that can be viewed as lattice vibrations which act as heat carriers, without degrading electronic transport. In this way, the conversion efficiency of silicon-based thermoelectric generators (TEGs) can become competitive with now available commercial thermal engines.

In this chapter, after a description of thermoelectric effects in bulk materials, we discuss which are the key parameters to optimize the thermoelectric efficiency, and we clarify the proper use of different thermoelectric figures of merit commonly found in the literature. Then, we show how nanostructuring can allow silicon to be used as high efficiency thermoelectric material, and we present a top-down process for the fabrication of large area silicon nanowire arrays for thermoelectric applications. Finally, we discuss their reliability with respect to the random nanowire breakdown, and we demonstrate by means of numerical simulation their high tolerance with respect to the nanowire width dispersion.

14.2 Thermoelectric Effect in Bulk Materials

In the case of thermoelectric systems, we have a device, as shown in Fig. 14.1, with a temperature gradient $\Delta T = T_H - T_C$ at its extremities where T_H are T_C are HOT and COLD side temperatures, respectively. This gradient induces a voltage drop V, related to ΔT through the Seebeck coefficient, defined as the ratio of the voltage drop and the temperature difference at the extremities of the device:

$$S = \frac{V}{\Delta T}, \tag{14.1}$$

However, in the case of the device depicted in Fig. 14.1, if we suppose to measure the voltage drop V by means of a voltmeter, the result will be zero. Indeed, in a closed circuit the total temperature gradient is zero, and the only way to obtain a non-null V is to put two materials with different Seebeck coefficients S_1 and S_2 between T_H and T_C, as sketched in the upper panel of Fig. 14.2. In this way, we obtain

$$V = (S_2 - S_1)(T_H - T_C). \tag{14.2}$$

Thus, the output voltage depends on the product of the Seebeck coefficient difference and the temperature gradient. If the two materials are metals, both Seebeck coefficients will have the same sign, since carriers are always electron which diffuses from the HOT to the COLD side, and the total $S = S_2 - S_1$ coefficient will be very low, with a consequent low voltage V. On the other hand, if we have

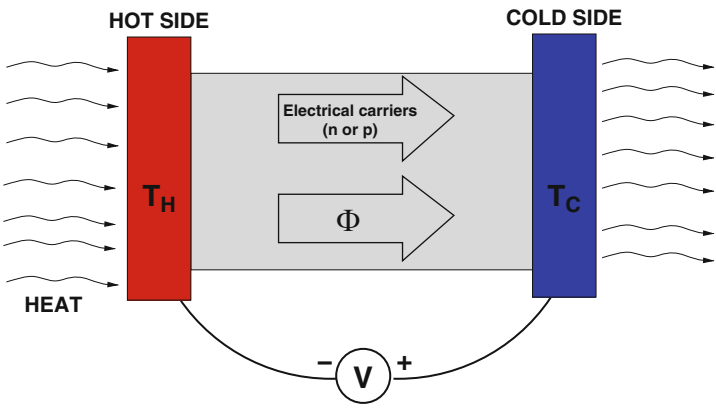

Fig. 14.1 Sketch of a thermoelectric device, where a temperature gradient $\Delta T = T_H - T_C$ between the HOT and the COLD side induces a voltage drop V at its extremities

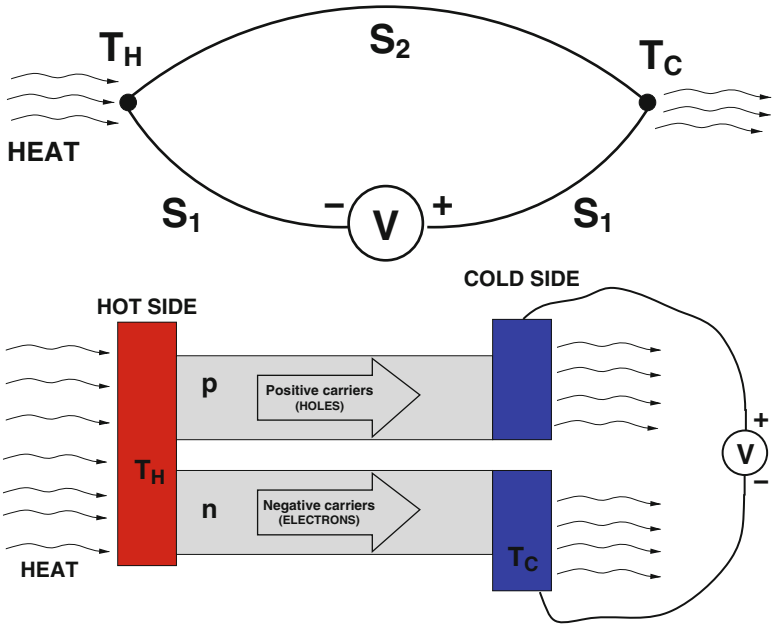

Fig. 14.2 *Upper panel*: Schematic sketch of a thermocouple, composed of two materials with different Seebeck coefficient. When a temperature gradient T_H–T_C occurs at the contacts between the two materials, a non-null voltage V can be observed. *Lower panel*: schematic sketch of a thermoelectric generator, composed of two n and p-type semiconductors, connected thermally in parallel and electrically in series

semiconductors, since charge carriers will always diffuse from the hot side to the cold one, in the case of n doped materials electrons will charge the cold side *negatively*, with $S_n < O$, meanwhile in the case of p doped the cold side will be charged *positively* by holes, with $S_p > 0$. Thus, if we connect n-type and p-type modules thermally in parallel and electrically in series, as shown schematically in the lower panel of Fig. 14.2, we obtain

$$V = (S_p - S_n)(T_H - T_C) \tag{14.3}$$

$$V = (S_p + |S_n|)(T_H - T_C) \tag{14.4}$$

In this way, the total Seebeck coefficient is the sum of absolute values of the two Seebeck coefficients, giving a higher output voltage V.

14.3 Thermoelectric Power Factor and Efficiency

The aim of any energy conversion system is to have the highest efficiency, that is defined as

$$\eta = \frac{P_L}{P_{IN}}, \tag{14.5}$$

where P_L and P_{IN} are the power supplied to the load and the input power, respectively.

In this context, we should identify which quantities are involved in the thermoelectric power conversion picture.

First of all, let us suppose that the device extremities can be maintained at fixed temperatures T_H and T_C. This means that the HOT side can be considered as an infinite heat source, while the COLD side an infinite heat sink. In this case, we can ignore the heat flux Φ through the device, and it is sufficient to optimize the maximum output electrical power

$$P_{el} = \frac{V^2}{4R} = S^2 \Delta T^2 \sigma \frac{A}{4L}, \tag{14.6}$$

where

$$R = \frac{L}{\sigma A} \tag{14.7}$$

is the internal device resistance (remembering that the maximum power transfer is obtained if the load and the internal resistances are equal), σ its electrical conductivity, L and A the length and the cross-section surface of the conductor, respectively. Considering that L and A are two geometrical factors, so not related to material properties, and the temperature gradient ΔT is kept constant, to maximize the output power, we should optimize the factor $S^2\sigma$, which for this reason is commonly known as *thermoelectric power factor*. In this context, we should find a material with S and σ as high as possible. For this kind of applications, due to its properties (both huge electrical conductance and Seebeck coefficient), graphene seems to be the ideal material, which lead to predict a *giant thermoelectric effect in graphene* [13].

Unfortunately, in almost all real applications, the assumption of infinite heat source and/or sink is not satisfied. Indeed, the heat flux through the device, due to its finite thermal conductivity k, reduces ΔT unavoidably, or by raising T_C up if the heat flux from the HOT side is larger than the heat that the COLD side can dissipate, or by lowering T_H down when the heat source is not able to supply enough thermal energy to balance the heat flowing to the COLD side. In many cases, both phenomena can occur simultaneously. Then, a new dynamic thermal equilibrium, with lower ΔT and with a significant efficiency loss, can be obtained, or both sides will

reach the same temperature, with a consequent null thermoelectric conversion. Thus, we should take into account also the thermal conductivity k, and, in particular, to optimize thermoelectric performances we would like to have a material with the highest σ and the lowest k. Briefly, our aim is to find an unusual phonon-glass and electron-crystal material [14]. The phonon-glass behavior is needed for as low a thermal conductivity as possible, while the electron-crystal requirement hails from the fact that crystalline materials (in particular semiconductors) are the best compromise for the electronic properties (Seebeck coefficient and electrical conductivity).

To evaluate the quality of a thermoelectric material we can introduce the factor of merit [5]

$$Z = \frac{S^2\sigma}{k}. \tag{14.8}$$

This factor, which depends only on the physical properties of a material, is useful since it appears in the thermoelectric maximum efficiency expression [5]:

$$\eta_{\mathrm{TOT}} = \eta_C \cdot \eta_{\mathrm{TH}} = \frac{T_H - T_C}{T_H} \frac{\sqrt{1 + Z\overline{T}} - 1}{\sqrt{1 + Z\overline{T}} + T_C/T_H}, \tag{14.9}$$

where $\overline{T} = (T_H + T_C)/2$ is the average absolute temperature. We have to note that this expression is only a first order approximation and, while it is almost always used in the literature for evaluating thermoelectric performances, it is strictly correct only if S, σ and k, and therefore Z, can be considered constant with respect to the temperature between T_C and T_H [15]. Of course, this is only a rough approximation, since, as well known, all the above parameters vary with the temperature, both in metals and in semiconductors. In this case, an averaged Z is often used [15].

Moreover, we can observe that η_{TOT} is composed of two terms. The first one, $\eta_C = (T_H - T_C)/T_C$ is the Carnot efficiency, which is the maximum efficiency for any thermal cycle operating between T_C and T_H [5]. The second term, η_{TH}, can be ascribed to the thermoelectric conversion process, and it depends only on the material chosen for the device.

As well known, due to the second law of thermodynamics, the Carnot limit is unavoidable. Thus, for example, any thermal machine working between room temperature (300 K) and 800 K cannot reach a total efficiency over than 62.5 %. However, commonly available internal combustion engines (such as diesel or gasoline-based ones) have a typical efficiency around 20 %. Aware of this fact, thermoelectrics can be a valid option for competitive energy conversion if a total efficiency approaching the 20 % can be reached. In Fig. 14.3, we can see the theoretical maximum efficiency of a thermoelectric device, as a function of T_H and assuming the COLD side at room temperature (300 K), for different values of the Z factor. While for Z less than 10^{-3} the efficiency is well below the 20 % target

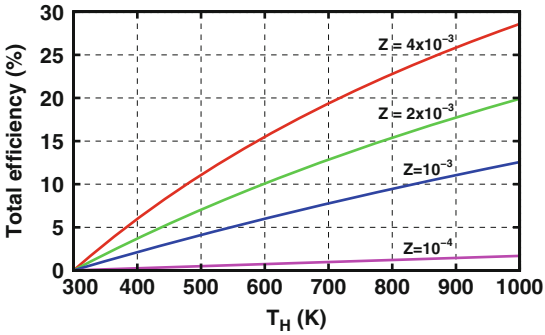

Fig. 14.3 Maximum thermoelectric total efficiency as a function of T_H, assuming $T_C = 300$ K, for different values of Z

even at quite high temperatures, we can see that an increase to $Z = 4\times10^{-3}$ rises the efficiency up to more than the 20 % for temperatures above 700 K. Furthermore, even for $Z = 2\times10^{-3}$ the efficiency starts to be competitive, with a value of 15 % at 800 K, easily obtainable, for example, with solar concentration systems, and 20 % at 1,000 K, that can be reached in several industrial processes. Thus, it is apparent to understand the big effort in the scientific community to improve thermoelectric performances by fabricating complex alloys [16] or, in recent years, by nanostructuring [17], and the significant interest of the industrial sector in these kinds of applications.

Thermoelectric efficiency and figure of merit, which is the right factor?

Instead of Z, in the literature, we can often find as figure of merit the parameter ZT, with T the *average* absolute temperature. The product ZT appears explicitly in Eq. (14.9); moreover, it is a dimensionless parameter, with typical values around 1. Thus, it is "easy" to remember, to cite, and to compare. Also for these reasons, it is often used as the "unit of measurement" for thermoelectric performances. However, as we explain below, this factor should be handled carefully, and, unfortunately, sometimes its misuse can give incomplete or even incorrect indications on thermoelectric materials. From this point of view, we could state, as often found in the literature, that a material whose ZT is higher than 1 can be considered a good thermoelectric material. However, this statement is incomplete if we do not specify the operating temperatures (T_H and T_C) of the thermoelectric device.

First of all, the T value in ZT is the *average* absolute temperature, and according to Eq. (14.9) we should write $\overline{T}$. Observing again the curves of Fig. 14.3, we can obtain a 20 % total efficiency (which is, more or less, our goal) with a material whose $ZT = 2$ at $T_H = 700$ K (Z = 0.004 K^{-1} and $\overline{T} = 500$ K), and, for such a material, we can often find $ZT = 1.2$ at room temperature (300 K). The latter value is often cited as the threshold for a good thermoelectric material. Unfortunately, this statement, if incomplete, could

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have some critical points. First of all, saying $ZT = 1.2$ at 300 K should mean that $\overline{T} = 300$ K. For this reason, it is an indicative factor if we suppose that the conversion process is operating with $\overline{T}$ around the room temperature, as for example in domestic heating or air conditioning systems. In this case, if ΔT is less than 100 K, the variation of Z with respect to the temperature is not very relevant. Indeed, both S and σ do not vary too much, especially in heavily doped semiconductors, where the carrier mobility is limited by the scattering with lattice impurities. Thus, comparing different materials or compounds with ZT at room temperature is indicative only for quite low temperature processes. Otherwise, in applications where the conversion occurs between 300 K and T_H about 500 K or more, the approximation of constant Z in the whole temperature range is not satisfied, and the ZT parameter at room temperature could give incorrect information.

In addition, it is obvious that if $T_C = 300$ K is supposed, considering ZT at room temperature means that the device would operate between 300 K and. . .300 K, giving, for the Carnot law, an efficiency of 0! Briefly, without paying attention to previous facts, we could measure the thermoelectric performances with an almost fictitious value; in addition, we should be careful to avoid confusion between the average temperature $\overline{T}$ that should be considered in ZT and the absolute temperature T_H.

Another critical point is that giving a ZT value can be, sometimes, a bit misleading. Indeed, the same value can be obtained with another (worse) material just by varying the operating temperature, so it is not an absolute "unit of measurement," as Z alone could be. In this context, the main strategy to obtain the best thermoelectric efficiency is to maximize the ZT of a material. Even if we handle correctly this parameter, we could achieve incomplete results. If, for example, we find a material whose maximum ZT is 3 at 500 K (which means $T_H = 700$ K if $T_C = 300$ K), according to the ZT optimizing strategy, we will try to use the thermoelectric device at that temperature, with an efficiency, from expression (14.9) with $T_C = 300$ K, $\eta_{\mathrm{TOT}} = 0.1538$ (15.38 %). On the other hand, if the same material had $ZT = 2.5$ at 700 K ($T_H = 1,100$ K with $T_C = 300$ K), we would obtain $\eta_{\mathrm{TOT}} = 0.2164$ (21.64 %), with a significant improvement, due to the much higher T_H, at a lower ZT.

Furthermore, the operating temperature T_H is often imposed by the process that we want to exploit, or it can be tuned only slightly. Thus, the strategy to optimize the ZT factor should consider in any case at which temperature we want to operate, and, if T_H cannot be varied, it actually means to optimize Z at a given temperature. For example, if our aim is to recover waste energy from domestic heating, it would be unlikely to exploit successfully a system which

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has the best efficiency at 800 K (and, thus a commonly indicated ZT value around 1 *at room temperature*). This indicates that the best strategy should be to consider both Z and T, but separately, if we want to optimize the whole thermoelectric efficiency.

Finally, regarding the ZT misuse, in few cases, we can find graphics for the theoretical maximum efficiency where different curves, as a function of the temperature, equivalent to those in Fig. 14.3, are shown taking ZT as parameter, instead of Z. In this way, we impose implicitly that, for a certain curve, the whole factor ZT should be independent to the temperature $\overline{T}$, that would be true only if the factor Z was proportional to $1/\overline{T}$. Unfortunately, as already shown above, the expression is valid only if Z is constant with the temperature, and we run into an inconsistency.

In conclusion, the widespread use of ZT as thermoelectric figure of merit, without any wisdom, can lead to wrong conclusions about thermoelectric performances. Indeed, it should sound strange to use as 'unit of measurement' a parameter which does not give absolute indications and, most importantly, with values that, according to the application, can be fictitious. For these reasons, in our exposition we prefer to use Z as much as possible, and we will always keep in mind the previous considerations when referring to ZT.

14.4 Nanostructuring Strategy for Thermoelectric Applications

Nanostructuring is one of the most powerful strategies to increase the thermoelectric figure of merit of materials [18]

$$Z = \frac{S^2\sigma}{k}, \tag{14.10}$$

Through nanofabrication, the device active elements become comparable in size to the phonon mean free path (m.f.p.), and thus benefit from a reduced k via enhanced surface scattering of the acoustic phonons that provide the most significant contribution to the overall thermal conductivity. Electrical conductivity σ however, remains essentially unaltered owing to a much smaller electron m.f.p., thereby yielding a real advantage for thermoelectrics. To this end, current research concentrates on the search for novel nanostructured materials, characterized by high σ but low k to enhance the thermoelectric conversion figure of merit Z (or the alternative dimensionless parameter ZT, as discussed previously). As mentioned earlier, there

are encouraging prospects for limiting the value of the overall thermal conductivity k via nano-engineering of the materials. k can be expressed in general as the sum of two contributions due to the charge carriers (k_e), and the lattice (namely due to heat transmission by crystalline lattice vibrations or phonons) k_{ph} [19],

$$k = k_e + k_{\mathrm{ph}}. \tag{14.11}$$

For bulk elemental metals k_e provides a dominant contribution to k and is related to σ by the Wiedemann–Franz law [19]:

$$\frac{k_e}{\sigma} = \frac{\pi^2}{3}\left(\frac{k_B}{e}\right)^2 T, \tag{14.12}$$

where k_B is the Boltzmann constant, e the electron charge, and T the absolute temperature. This means that k_e cannot be decreased without altering σ, thereby making metals poor TE materials. Interestingly, however, there are significant deviations from these behaviors in both alloyed semiconductor superlattices, and nanostructured semiconductors.

14.5 The Choice of Silicon as Thermoelectric Material

The case of silicon is worth mentioning explicitly, given its nontoxic nature, versatility, abundance, and its pervasiveness in society as the elective semiconductor for microelectronics. In silicon the main contribution to k is given by $k_{\mathrm{ph}} = 148\,\mathrm{W/mK}$, whereas k_e, that depends on doping, is less than 1 W/mK. Most importantly, theoretical studies [20, 21] confirmed by experiments [22, 23] have shown the possibility to suppress k by up to 2 orders of magnitude, to 1 W/mK, thereby yielding $Z = 0.002\ \mathrm{K}^{-1}$ (with an equivalent $ZT = 0.6$ at 300 K). This is possible because the phonon mean free path (m.f.p.) is much longer than the electron m.f.p., i.e. of the order of 20–50 nm compared to 2–10 nm for electrons. When the lateral dimensions of the nanowires become comparable with the phonon m.f.p, conduction of the latter results limited by surface scattering, thus leading to a decrease in k, and determining an increase in Z. A further thermal conductivity reduction can be obtained by suitable surface treatments [18, 24, 25], aimed, for example, at increasing the surface roughness, and thus again the phonon m.f.p. owing to enhanced phonon scattering. Interestingly, this can be done in such a way that the electrical properties are almost perfectly preserved. Overall, by the combined effect of reduced dimensions and enhanced surface roughness, an increase of Z of more than 2 orders of magnitude can be expected. Obviously, once k_{ph} is minimized and reduced to values below or comparable to k_e, it is important again to consider the factors affecting both k_e and k_{ph} (such as effective mass, electronegativity and atomic weight of the component elements, charge mobility and energy gap) as already discussed a decade ago in the

excellent review by Disalvo [26]. While significant work has been done since then, especially in terms of materials nanostructuring [27], there are still ample margins for improvement in the engineering of TEGs with *ZT* at high temperatures (800–1,000 K) of 4 or greater, for example by seeking further reduction of the NWs diameter, their uniformity, density, and the control of their doping level. Importantly, in considering the best results obtained to date, it is also useful to distinguish, as already stated previously, between nontoxic, up-scalable, and essentially "sustainable" materials such as nanostructured-Si (for which *ZT* at room temperature is essentially still limited to 1 or less), and "high-*Z*" materials (e.g., based on Pb, Te, Sb, Bi, and their nanostructured alloys), which while attaining *ZT* values at 300 K of 3 or more [11, 26] raise significant concerns in terms of scalability, toxicity, and eventually sustainability, a property that is commanding ever increasing attention.

In any case, a single SiNW can convert into a negligible energy. For this reason, the research should be focused on the fabrication of large SiNW arrays [28], in order to exploit the TE nanoscale properties in macroscopic devices. By putting in parallel *n* and *p* doped SiNW arrays, high efficiency TEGs can be fabricated.

14.6 Fabrication of Silicon Nanowire Networks

The reduced SiNW thermal conductivity gives interesting possibilities for the fabrication of devices to be used for thermoelectric generation with high heat to electrical power conversion efficiency. These devices could be usefully employed for energy harvesting purposes. However, for the development of usable SiNW-based thermoelectric generators a technique for a massive and reliable production of well-organized, very long, SiNWs must be available. Such a technology could also be employed for the fabrication of several electronic devices, such as solid-state memories [29], or sensors based on large arrays of very sensitive nanowires [30].

Here we present a top-down technique for the fabrication of a well-organized and very reliable network based on a large amount (order of 10^5 SiNWs per mm^2) of narrow (< 50 nm) silicon nanowires. In ideal conditions (i.e., no defects are present) these very large area SiNW arrays are equivalent to the parallel of many very long (order of millimeters) and small SiNW. On the other hand, the arrays are much more tolerant to unavoidable random defects of single, very long, nanowires.

Figure 14.4 shows SEM photos of a typical top down fabricated SiNW net. In the upper panel, a low magnification image showing the 1×0.6 mm^2 area of the SiNW network (dark zone of the image) is shown; clear areas are silicon, and a trench (dark) runs at the borders of the net to provide electrical insulation. Conduction is measured (see the next sections) between crystalline silicon areas (top and bottom terminals) which are accessed through aluminum contacts (not visible). In the lower panel, the texture of the net, made of SiNWs 3 μm long, is shown; the SEM image of the inset shows the 50 nm wide Si core, embedded in silicon dioxide. The implemented fabrication technique is an advancement of a previously

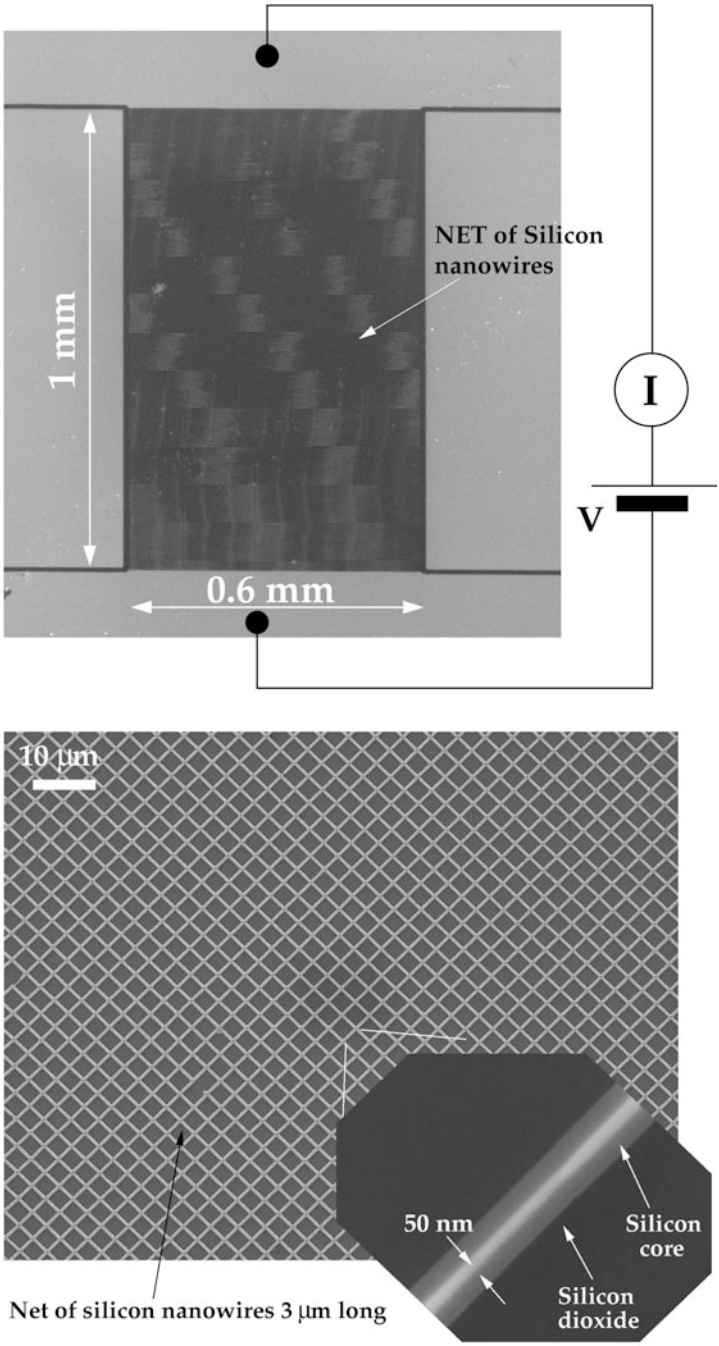

Fig. 14.4 SEM images of a silicon nanowire network. *Upper panel*: a low magnification image showing the overall dimension of the network. *Lower panel*: the texture made of 3 μm long SiNW is shown; the *inset* shows a detail of the SiNW with a core width of 50 nm. (Reprinted with permission of Elsevier, from [28])

developed top-down process [31, 32] that allows the reliable fabrication of devices based on narrow (down to 10 nm), micrometers long, single SiNWs, whose both mechanical [33] and electrical properties [34, 35] have been fully investigated in our recent works. The process is developed on Silicon On Insulator (SOI) substrates, with a top silicon layer 260 nm thick. The doping of the top silicon layer has been adjusted by means of a solid source doping technique based on Filmtronics ceramic wafer for phosphorus (*n*-type) or boron (*p*-type), already employed for the selective doping of a silicon nanowire [36]. The doping process consists in the pre-deposition and the drive-in steps. The ceramic wafer is brought into contact with the SOI substrate, and a rapid thermal annealing (RTA) cycle in N_2 atmosphere is performed. Varying the temperature and the time of pre-deposition process the top layer can be doped as needed. After the ceramic wafer removal, an RTA cycle at 1, 150 °C for 10 min, with 1 min in O_2 atmosphere and 9 min in N_2 atmosphere, is applied to the SOI sample. Afterwards, a 50 nm thick top dioxide layer, used as a mask for the following silicon anisotropic etching, is grown by means of a dry oxidation step at 1, 150 °C for 5 min. The final doping, and carrier mobility, of silicon nanowires is still and open problem, because they depend on many factors as interfacial states density, surface segregation of doping species, and so on.

A silicon dioxide layer is grown on top by dry thermal oxidation. A suitable SiO_2 mask is then obtained by a high resolution electron beam lithography step [37], through standard PMMA resist and calibrated chemical wet etching. It is important to underline that electron beam lithography is not mandatory for this step. Indeed, SiNWs with a cross-section smaller than 30 nm can be fabricated starting from 150 nm masks, easily obtainable with advanced optical lithography, making this process suitable for massive and very large-scale production.

The most critical point of the lithographic step is to optimize the electron beam process in order to achieve the lowest dispersion in the SiNW widths. As known, in a large structure defined by means of electron-beam lithography, the effective dose in different region of the device is not uniform, due to proximity effects. In fact, the forward and the back-scattering of electrons hitting the target broaden the exposed area of a single spot. The result is that highly dense patterned regions can be over exposed easily, while portions with very few surrounding patterns are often under exposed. In a very high-resolution process (with several thousands of dense different structures) this will affect the lithographic step with no chance to fabricate the desired device. In order to overcome this limitation, a very big effort has been made and several correction techniques have been developed. The common point of all techniques is to lower the dose in dense patterned regions, while at the boundaries it is raised. Unfortunately, the exact solution of the problem is computationally very demanding, since it has an exponential growth with the exposed area. For this reason, often only approximated techniques can be performed. Regarding the large area and high density of the devices here proposed, an ad hoc procedure for the correction of electron beam lithography intra proximity effects has been developed in order to obtain a more uniform exposure on large areas. As shown in Fig. 14.5 the SiNW network is defined by writing several rows of boxes, starting from the one

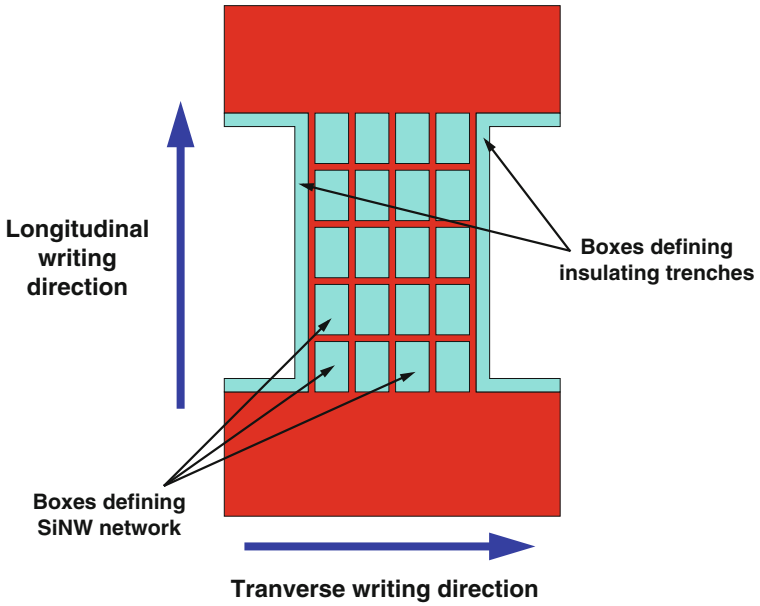

Fig. 14.5 A sketch of the adopted e-beam writing strategy and of the intra proximity effect correction. (Reprinted with permission of Elsevier, from [28])

corner of the structure that we want to fabricate. Moreover, the device is isolated from the whole Si chip by means of lateral trenches. The dose is partially compensated along the transverse writing direction by tuning the exposure dose of the insulating trenches. On the other hand, the compensation in the longitudinal writing direction is obtained by varying the exposure dose of each box, that is larger at the boundaries and it is reduced toward the center of the device. In Fig. 14.6 we show a comparison between the boundary regions of some arrays without (in a and b) and with the proximity effect correction applied. As we can note, in the first case we have under-exposition and poor pattern definition, while, if the correction is applied, we obtain very uniform and well-patterned networks.

Silicon anisotropic wet etching has been used in order to obtain very uniform wires with trapezoidal cross section, laterally delimited by [111] silicon crystalline planes. Stress controlled oxidation [32] is then used for defining the SiNWs and reducing their width in a well-controlled and reliable way. At the end of the oxidation-reduction process, each silicon nanowire has a triangular cross section. As it has been demonstrated [38], by using this technique it is possible to obtain very narrow SiNW even starting by not very small initial structures (over 100–150 nm of initial width) that could be obtained even with advanced optical lithography, in order to reduce fabrication costs. The initial width of the structures is limited only by the maximum nanowire density that has to be obtained in the final device.

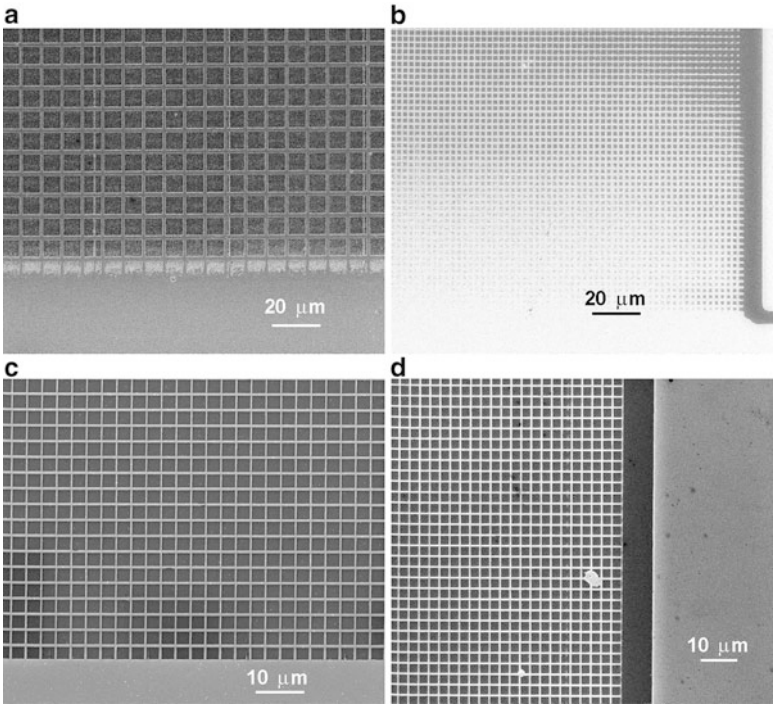

Fig. 14.6 (**a**) and (**b**) SEM images of SiNW array boundary regions without any proximity effect correction applied. (**c**) and (**d**) Similar boundary regions with the proximity effect correction

14.7 Random Failures in SiNW Networks

As schematically represented in the sketches of Fig. 14.7a and b, a silicon nanowire network is equivalent to many parallel silicon nanowires, each of the same width of the SiNWs forming the texture and of the same length of the whole net (1 mm in the case of the net shown in Fig. 14.4). In particular, important properties connected to the low nanowire width, such as large electrical to thermal conductivity ratio, are preserved; in Fig. 14.7c a sketch of the electrical equivalent resistor network is shown. Each of the $N \times M$ (row by column) resistors of the network models a SiNW of the net texture with a resistance value R_0 (conductance value $G_0 = 1/R_0$). It is trivial to demonstrate that this resistor network is equivalent to M parallel resistors, each given by the series of N elementary resistor of the network that are the vertical branches in the sketch of Fig. 14.7c. In the case of a perfect network, horizontal branches are ineffective both for the electrical and for the thermal conduction. The key point in using a silicon nanowire network is that this structure is much more tolerant to nanowire failures (as breaking) that can occur during the fabrication process for the presence of defects or other.

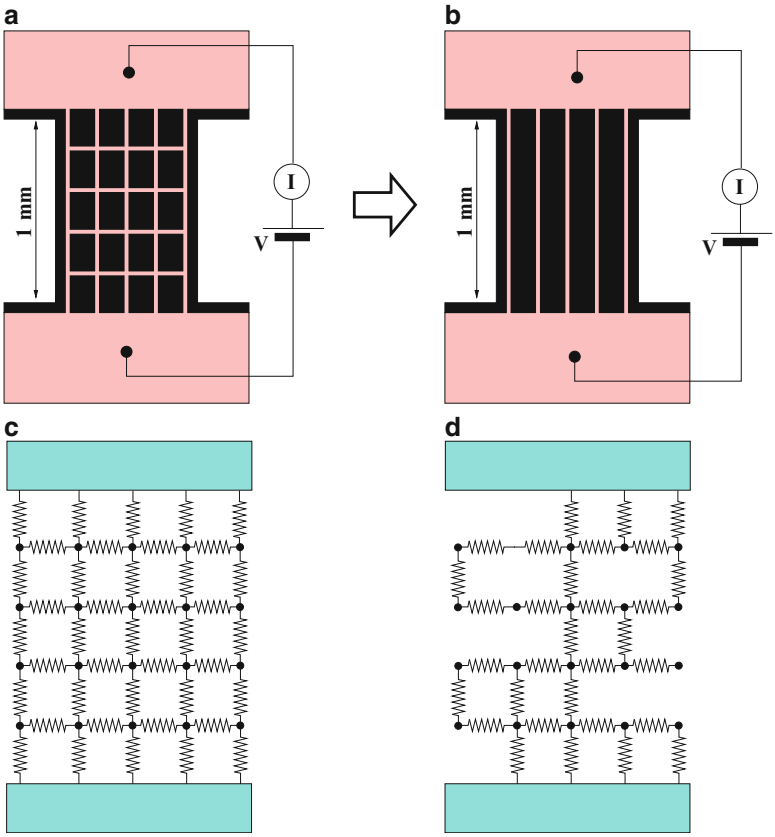

Fig. 14.7 Sketch of a SiNW network (**a**), electrically and thermally equivalent to many very long SiNWs in parallel (**b**). In (**c**) the equivalent electrical resistor network is shown and in (**d**) it is shown how random nanowire failures can be schematized by removing resistors from the net. (Reprinted with permission of Elsevier, from [28])

This allows the fabrication of very large areas SiNW networks (equivalent to millimeters long SiNWs in parallel) with high reliability and repeatability of the total thermal and electrical resistance of the net.

In order to give theoretical support to these considerations, a Monte Carlo technique has been implemented and applied to resistor networks. An ad hoc program for the resolution of electrical networks with a great number of resistance, based on a recursive optimized $Y-\Delta$ transformations [39], has been developed in order to optimize computational times. The program has been tested on a complete network of $N\times M$ resistors of resistivity R_0, confirming that it is equivalent to M parallel resistors, each of value $N\times R_0$. If, for example, $N\times M = 291\times 190$ resistors with $R_0 = 1$ kΩ are considered, the total resistance of the net resulted exactly $1\times 291/190 = 1.53$ kΩ. Nanowire failures, due to defects in the fabrication

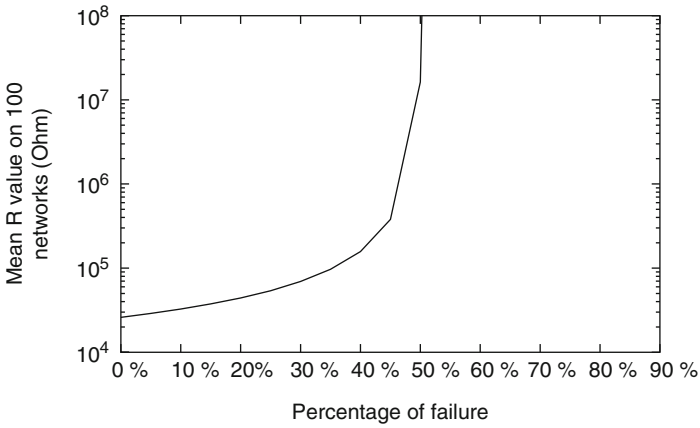

Fig. 14.8 The average value of resistance, evaluated on 100 networks with 291 ×190 initial number of resistors, is reported as a function of percentage of randomly removed resistors that simulated the nanowire failure. (Reprinted with permission of Elsevier, from [28])

process, have been modeled by randomly removing resistors from the net, as schematically shown in Fig. 14.7d. For each resistor a random number with an uniform distribution between 0 and 1 has been generated [40] and compared with a threshold P that established the probability (percentage) of failures: the resistor is removed if the random number is below the threshold P. The random removal of resistors has been repeated a suitable number n of times (population), stating from the same initial resistor network. Figure 14.8 shows the evaluated resistance of a network with $N \times M$ 291×190 resistors, each with a resistance of 17 kΩ, as a function of percentage of failure. A population of $n = 100$ networks has been considered for each percentage, and the average value of resistance is reported as a function of percentage of randomly removed resistors (threshold value). It can be seen that the net total resistance value shows a reduced variation even for high percentage of failure (10–20 %). For example, the resistance increases from 26 kΩ (no failures) to 33 kΩ in the case of 10 % of failures. According to the bond percolation theory [41, 42], a full failure (disconnection between top and bottom contacts) occurs only for very high nanowire failure percentages; in the case of Fig. 14.8 only failure percentages greater than 40 % give a complete disconnection between the top and the bottom contacts of the network.

In the case of M parallel resistors, each representing a millimeter long nanowire (no horizontal branches), the reliability of the top to down connection with respect to nanowire failure is much more small. The same defect density can be considered by assuming that a millimeter long nanowire is outlined as the series of N elementary resistors R_0 (conductivity G_0), representing a nanowire of the texture 3 μm long, with a probability failure P. The failure of one elementary resistor of the series brings to the failure of the millimeter long nanowire. The probability that an

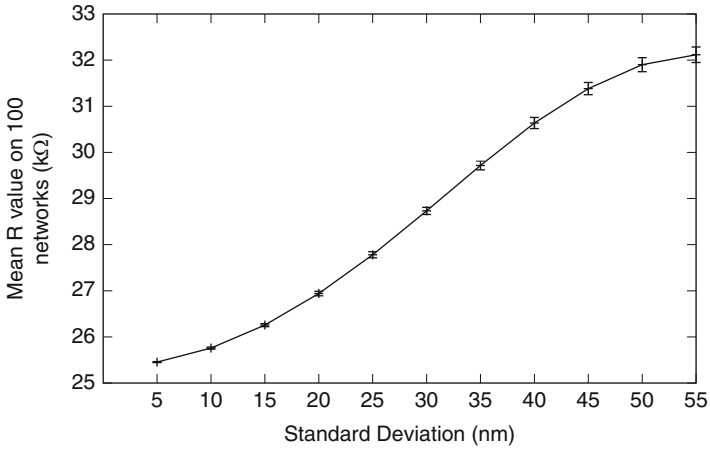

Fig. 14.9 The average value of resistance, evaluated on 100 networks with 291×190 random resistors, is reported as a function of the silicon nanowire width dispersion (standard deviation). (Reprinted with permission of Elsevier, from [28])

elementary resistor R_0 does not fail is $1-P$; making the reasonable hypothesis that failure events are uncorrelated, the probability that the series (the sum) of N resistors does not fail is the product of each single probability. This means that the probability of conduction for a millimeter long nanowire is $1-P^N$, and it results to be very small even with low P because it depends on N that in the case of long nanowires is of the order of several hundreds. If M long nanowires are placed in parallel, the total conductance can be evaluated as $G = M \times G_0/N$ in the case of no failures (no defects); in the case of failures with probability P, the expression for the total conductance can be evaluated as

$$G = M \times G_0 \frac{(1-P)^N}{N}. \tag{14.13}$$

For example, by considering again $R_0 = 17$ kΩ, ($G_0 = 5.88 \times 10^{-5}\ \Omega^{-1}$), the total conductance in the case of 10 % of failures ($P = 0.1$) is $G = 1.2 \times 10^{-15}\ \Omega^{-1}$ and the total resistance is $1/G = 8.2 \times 10^{14}$, i.e. top and bottom are practically disconnected.

Tolerance of the total net electrical resistance with respect to nanowire width dispersion has been investigated. Random resistance networks have been generated; each resistor has been evaluated by considering an ohmic behavior of nanowires. Each one has a length of 3 μm and a random width generated by means of a gaussian random generator [40] with a given average width of 80 μm and standard deviation σ. Figure 14.9 shows the average total network resistance, evaluated on 100 random nets (generated by different seeds), as a function of the nanowire width standard deviation σ. The errorbars show the standard deviations of

the total net resistance that resulted to be well reduced with respect to the dispersion of the nanowire width. For example, given a $\sigma = \pm$ 50 nm (more than 60 % of the average width of 80 nm), the total average resistance is 31,900 Ω with a standard deviation of ±152 Ω that is less than 5 %. This demonstrates the robustness of the total electrical resistance of the net with respect to the nanowire width dispersion. However, as far as the thermal conductivity is concerned, its reduction seems not to be linear with the nanowire width [18, 22]; in this case the average nanowire width and dispersion must be low enough for maintaining the thermal conductivity below a suitable value.

14.8 Network Reliability and Electrical Characterization

An estimation of nanowire failure percentage in fabricated networks, as the one shown in Fig. 14.4, can be performed by means of SEM inspection. For example, SEM photo of Fig. 14.10a shows a portion of a typical SiNW network, and interruptions (broken nanowires) in the network are enlightened. By inspecting several samples of fabricated SiNW networks, we can conclude that the mean value of failures is between 10 and 15 %. This value is well below the threshold failure percentage for which the whole resistance grows up noticeably. Figure 14.10b shows a typical $I-V$ characteristic measured for an SiNW network. The dispersion of the SiNW width W in a very large portion of the device is between 50 and 90 nm, and the proximity effect correction strategy previously described has been applied. The ohmic behavior shows that nonlinear effects in the conduction are negligible, and the value of about 66.7 kΩ is consistent to the above considerations about the electrical equivalence of the whole network with a large number of 1 mm long single nanowires in parallel. Indeed, from previous electrical measurements of a single SiNW the conductivity can be estimated of $40\times10^3\ \Omega^{-1}\ \mathrm{m}^{-1}$ (heavily doped). The measured resistance value of the network is comparable to the one of 190 SiNWs in parallel, with a length of 1 mm and a width mean value $W \simeq 72$ nm, which is very close to the W mean value observed by SEM inspection in a very large region of the device. Moreover, as it has been previously demonstrated, even a large dispersion in the width at the boundaries of the device does not affect the electrical characteristics of the network significantly, since the whole behavior of such devices is dominated by the large number of SiNWs smaller than 90 nm observed inside the structure.

14.9 Conclusions

In this chapter, after an introduction on the key concepts of thermoelectricity and a discussion of the different figures of merit used in the literature, we showed which are, nowadays, the limiting factors of a widespread diffusion of thermoelectric

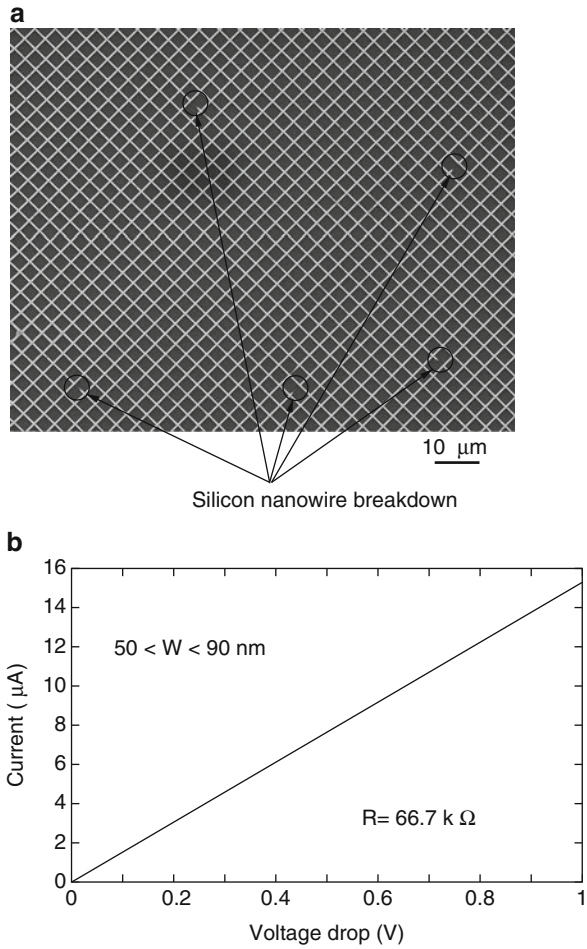

Fig. 14.10 In (**a**) an SEM image of a portion of SiNW network is shown; nanowire failures are enlightened. In (**b**) the $I-V$ characteristics of the SiNW network shown in (**a**), measured between the top and bottom contacts, are reported. The conduction is linear and the resistance is very similar to the one of many small and long silicon nanowires. (Reprinted with permission of Elsevier, from [28])

generators. In particular, currently available high efficient materials present several concerns in terms of abundance, toxicity, technological development, market distribution, and, ultimately, sustainability, which in last years is acquiring ever-increasing impact in the worldwide economy. Silicon could overcome all these aspects, since it is the most abundant element on the Earth's surface, it is not toxic, and, definitely, it is sustainable. Moreover, its technology and its market are impressively advanced, due to the leading role of silicon in the modern microelectronics. The main problem of bulk silicon for thermoelectric applications is its quite

high thermal conductivity k (about 148 W/mK), which does not allow relevant conversion efficiencies. We showed how nanostructuring can reduce k up to two order of magnitude, mainly due to the surface scattering of acoustic phonons, without any degradation of electrical properties, thus obtaining a significant improvement of thermoelectric performances.

Then, we presented a CMOS-compatible top-down process exploited for the fabrication of silicon nanowire arrays. We showed that these very large area networks are very reliable with respect to the failure of single SiNWs (the whole resistance variation is less than one order of magnitude up to 40 % of SiNW failures). Furthermore, the average value is very robust with respect to the SiNW width dispersion (even with a standard deviation about the 60 % of the average width value, the whole resistance standard deviation is less than 5 %).

These results are very promising for the fabrication of large area silicon nanowire networks that could allow practical applications of the interesting properties of SiNWs. In particular, the equivalence of reliable networks to the parallel of many, millimeters long, SiNWs makes this technique suitable for the fabrication of high efficiency thermoelectric devices. Finally, the possible implementation of this technique with advanced optical lithography is very promising for the fabrication of even larger area SiNW networks to be applied to energy harvesting.

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