

Chapter 18

Architectures for Digital Intensive Transmitters in Nanoscale CMOS

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Abstract Thanks to nanoscale CMOS, the computational power of digital integrated circuits has increased tremendously. For wireless communication systems, this resulted in increased transmission speeds using complex modulation schemes. The speed of nanoscale CMOS allowed to integrate the analog RF transmitter together with the digital baseband and brought high bitrate wireless communication to the consumer. Complex modulation schemes have to be supported by performant RF transceivers though. The design complexity of the analog transceivers has increased while their scalability is poor. Furthermore, many transistor parameters are degrading for traditional analog techniques. Calibration is therefore essential to achieve the required performance in traditional transmitters, but this increased tunability also offers new opportunities. Concurrently, the speed of nanoscale CMOS brought the digital closer to the antenna and enabled a new transmitter architecture: the direct digital modulator, which comes with its own set of challenges and solutions.

18.1 Introduction

The evolution of CMOS technology is mainly driven by the need to decrease the cost of computing power. This results in ever decreasing device sizes combined with increasing operating speed. Powerful baseband processors handle complex modulation schemes and bring ever increasing communication bitrates to the consumer market. This created a new family of handheld wireless devices, the smartphone, that combines a multitude of communication standards. As these phones are targeting the consumer market, cost and form factor are important

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parameters. The analog functions are therefore best integrated together with the processor, in the digital technology.

Unfortunately, while the CMOS technology is continuously optimized for digital circuits, many of its analog performances are degrading. As an example the supply voltage is reducing much faster than the transistors' threshold voltage. The output impedance and the intrinsic gain of the transistors are also decreasing with their lengths. Analog functions need new circuits to provide the required performances, as they can no longer rely on stacking of transistors with their relatively large threshold in a limited supply voltage. New architectures have to leverage on the strength of the new technologies, whose main assets are their small feature size and high speed. A multitude of small devices can be added to support and improve the main analog function, while the available computing power can be used to *program* the complex analog circuit in its optimal operating point. The intrinsic speed of nanoscale CMOS also enabled completely new architectures, such as direct digital RF modulation.

This paper focuses on how nanoscale CMOS can be used to the designer's advantage in wireless transmitters. First, it will be demonstrated how transmitters based on traditional analog architectures can take advantage of nanoscale CMOS. In a Software Defined Radio transmitter, the tunability of the transmitter is increased tremendously compared with more traditional realizations, without concession on performance. The second part of this paper presents a new family of transmitters: the Direct Digital RF Modulators. These leverage on the high speed and low size of nanoscale CMOS to bring the digital domain closer to the antenna. This architecture comes with specific challenges. Several realizations will be presented to address some of these challenges.

18.2 Digitally Assisted Analog Transmitter

Today's dominant wireless communication device is a smartphone that gives its user ubiquitous access to a multitude of services provided through an even wider range of wireless standards, covering short and long range communication combined with small or wide data rates. Depending on the use case, a link is set up on the most appropriate channel, but several links may also be active in parallel. To accommodate the various standards, flexibility of the transmitter is a must. Indeed, adding every new wireless feature by hardware multiplication is no longer possible. Instead, a transmitter that is capable of transforming itself satisfying the requirements of any desired communication protocol while still providing competitive power consumption, is required. This is even enhanced with the recent introduction of LTE that combines variable baseband bandwidths with variable RF frequencies. A Software Defined Radio (SDR) Transmitter, provides this functionality. Such a transmitter can be designed despite but mainly thanks to nanoscale CMOS.

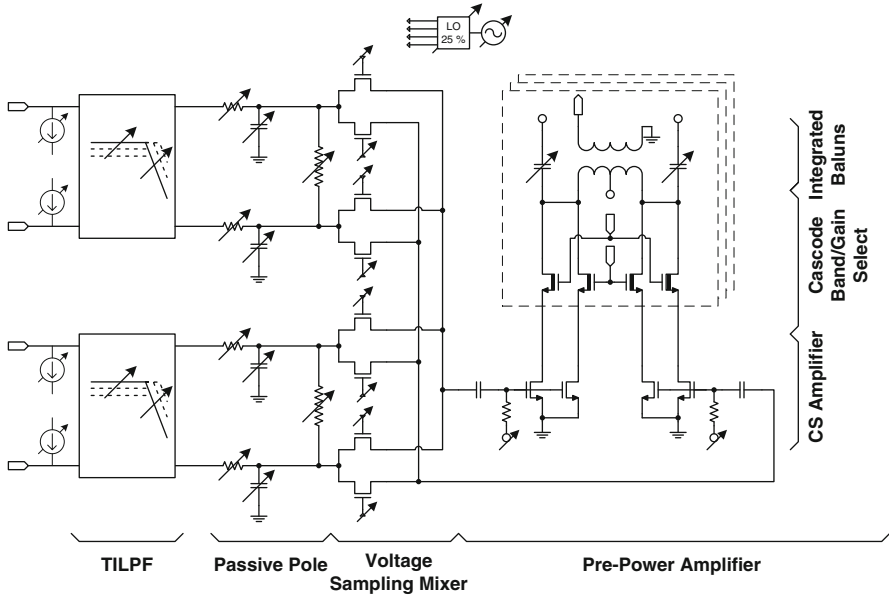


Fig. 18.1 40 nm CMOS SDR transmitter circuit diagram

18.2.1 A 40 nm CMOS Software Defined Radio Transmitter

Figure 18.1 shows the schematic diagram of a SDR transmitter realized in 40 nm CMOS. The transmitter is based on a direct up-conversion architecture which is the most suitable to build a SDR radio [1]. Besides its powerful performance, it has the potential to allow flexible operation by including reconfigurability into the circuit blocks. The transmitter consists of a low-pass filter followed by a passive mixer and a pre-power amplifier. While these are traditional building blocks, they benefit from nanoscale integration which provides programmability to improve the overall performance by calibration and tuning.

The baseband section consists of an active transimpedance low-pass filter (TILPF) based on a flexible Tow-Thomas architecture (Fig. 18.2) that offers independent programming of the transimpedance gain, the bandwidth and the quality factor [1]. The active filter is followed by a programmable passive filter to further reduce the out-of-band noise. All resistors and capacitors are split in small units that can be added or removed from the circuit as needed. This results in a programmable bandwidth from 400 kHz up to 20 MHz. The transimpedance gain of the filter can be programmed from 1 to 8 K Ω . This accommodates the various standards targeted. But the tunability reaches further. Both amplifiers in the active filter consist of several small opamps connected in parallel. They can be turned on or off individually to adjust the amplifier's gain-bandwidth product in eight steps from 60 to 480 MHz. The current consumption of the amplifier is now linearly

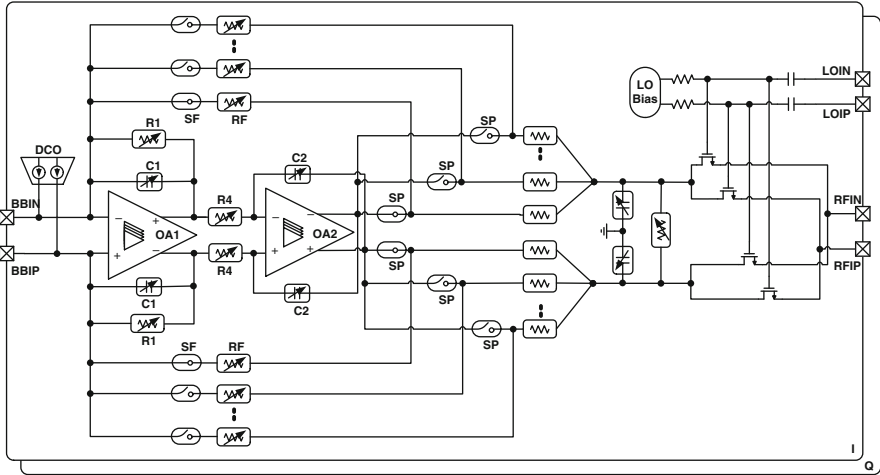


Fig. 18.2 SDR baseband followed by the passive voltage sampling mixer

proportional to its gain-bandwidth. This allows to trade power for performance and vice versa. Maximal performance is achieved at maximal power, but when the requirements are less stringent, power can be saved. The programmability is achieved thanks to nanoscale CMOS, that offers good, small switches and little parasitic overhead.

The DC offset of the TILPF can be compensated by injecting a small DC current at its input through integrated calibration current DACs. DC offset has thus not to be guaranteed over PVT at design time, which would result in the need for larger, better matching transistors and would require more design effort and consume more power. Instead, nanoscale CMOS allows the compact integration of simple DACs, and offers the possibility for automatic integrated tuning at run-time with little overhead.

The output of the active low pass filter is further filtered by a programmable passive RC filter before being up-converted in the subsequent quadrature voltage sampling mixer. Passive mixers require good switches and are widely used in nanoscale CMOS. In the presented implementation, a passive voltage sampling mixer is chosen for its good out-of-band noise performance as required for FDD operation.

The final block in the transmitter is the pre-power amplifier. Its circuit schematic is included in Fig. 18.1. It consists of a cascaded differential Common-Source amplifier loaded with two on-chip baluns with programmable center frequency. A wideband differential output is also provided. The amplifier transistor is split in multiple units that can be turned on or off by one of the three the thick-oxide cascode transistors topping each amplifier branch. These cascode transistors also determine to which of the three outputs the amplifier's output is derived. Here again, nanometer CMOS enables to split the main amplifier into small parts with little overhead, to obtain the extra functionality.

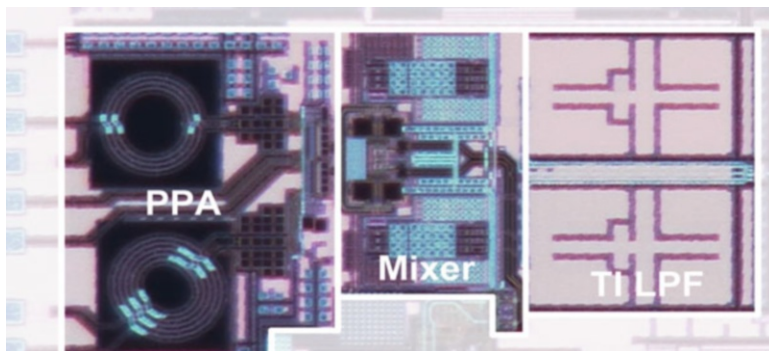


Fig. 18.3 40 nm LP CMOS SDR transmitter chip photograph

The 25 % duty cycle LO generator benefits from the speed of the technology and is based on conventional CMOS logic. This eases the implementation and lowers the power consumption. It is proportional to the LO frequency as the generator does not consume static power. The phase noise is low thanks to the large LO voltage swing, which is also beneficial to drive the passive mixer's switches. Note that the sizing of the devices has to be performed in an analog way, to achieve the extremely low phase noise required for SAW-less FDD.

The presented Software Defined Radio transmitter was implemented in 40 nm LP CMOS. Its core area is $1.4 \times 0.7 \text{ mm}^2$ (Fig. 18.3) and is mainly dominated by the baseband capacitors and the on-chip baluns. The transmitter consumes 13–44 mA from the 1.1 V supply (TILPF + LO generation) depending on the selected bandwidth and the LO frequency. The PPA consumes less than 43 mA from the 2.5 V. This is proportional to the required output power and linearity. The SDR concept is demonstrated in the modulator's performance summary of Fig. 18.4. A single transmitter achieves SOA performance comparable to dedicated solutions for a multitude of standards, including the toughest WCDMA/LTE bands as well as GSM, WLAN and WiMAX. The output P1dB is better than 10 dBm in all modes except GSM, where lower PPA linearity is traded for current consumption. An EVM better than 2.5 % is measured in WCDMA, LTE GSM and WiMAX while the CNR in the RX band is better than -160 dBc/Hz, which is sufficient for SAW-less operation in all WCDMA/LTE FDD bands.

The SDR concept may also be used to further reduce the transmitter's average power consumption in two ways. First, the user's communication is not limited to a single protocol as in a dedicated terminal. Instead, the most optimal link can be chosen in any given situation. What's more, when the optimal link has been selected, the power budget can be further optimized by programming the hardware for the best trade-off for noise, filter order, linearity, etc. for the actual channel conditions. Traditionally, these trade-offs were fixed at design time but are now performed at run-time, allowing for the best compromise possible between user experience and battery life.

<i>Band #</i> <i>Fcarrier</i> Δ TX-RX	<i>Mode</i>	<i>BW</i> [MHz]	<i>OP1dB</i> [dBm]	<i>Pout</i> [dBm]	<i>EVM</i> [%]	<i>ACLR1/2</i> [dBc]	<i>CNR</i> [dBc/Hz]	<i>I_{max}</i> [mA] 1.1V/2.5V	<i>DG.09</i> [mW]
Band I 1.92GHz 190MHz	UMTS	4	10.4	3.79	2.0	-40.2/67	-162	21/41	30.9
	LTE	20	10.4	2.1	2.5	-39/-58	-160	25/40	
Band II 1.85GHz 80MHz	UMTS	4	10.4	4.39	2.3	-40.2/-63	-164	20/40	30.2
	LTE	20	10.4	2.6	2.4	-40.1/-59	-162.5	24/40	
Band V 0.82GHz 45MHz	UMTS	4	10.9	4.45	1.7	-41/-68	-161.7	14/37	24.8
	LTE	10	10.9	2.45	1.7	-41.4/-63	-160.5	17/37	
Band VII 2.5GHz 120MHz	UMTS	4	13.5	7.1	1.5	-46/-72	-159	24/40	38.5
	LTE	20	13.5	5.1	2	-42/-58	-158	28/40	
Band XI 1.42GHz 48MHz	UMTS	4	11.7	5.2	1.5	-41/-67	-162.6	18/37	27.8
	LTE	20	11.7	3.4	2.0	-42/-58	-160.4	21/36	
Band XII 0.7GHz 30MHz	UMTS	4	10.5	2.41	2.1	-39.5/-65	-160	13/34	24.8
	LTE	10	10.5	0.4	1.8	-41/-67	-159	17/33	
0.9GHz 20MHz	GSM	0.2	8.1	4.5	1.7	-54/-67	-160	18/25	
2.4GHz 100MHz	WLAN	40	13.6	4.6	3.3	-41/-54	-159	27/40	
3.5GHz 100MHz	WiMAX	20	12.6	3	1.8	-41/-54	-155	38/43	
4.8GHz 100MHz	WLAN	20	10.47	1	8.1	-42/-48	-156	44/39	

Fig. 18.4 SDR TX performance summary (Measurements with on-chip balun, except Band VII, WiFi and WiMAX where the wideband output is used)

18.3 Direct Digital RF Modulator

Switching amplifiers have the potential to realize high efficiency. They eliminate internal device dissipation by avoiding the simultaneous occurrence of current through and voltage over the switch. Switching amplifiers typically feature a constant output amplitude and rely on a polar architecture in non-constant envelope modulation schemes. Figure 18.5 presents a basic polar transmitter. The Cartesian I and Q components are first converted into phase and amplitude. The phase modulated LO is applied to the amplifier, while the amplitude is modulated through the supply voltage. While this architecture aims for the high efficiency of the switching amplifier, it suffers from several implementation issues. As the Cartesian to polar conversion is non-linear, the bandwidth of both the phase and the amplitude are increased by at least a factor 4. This impacts the implementation of both the phase and amplitude modulator.

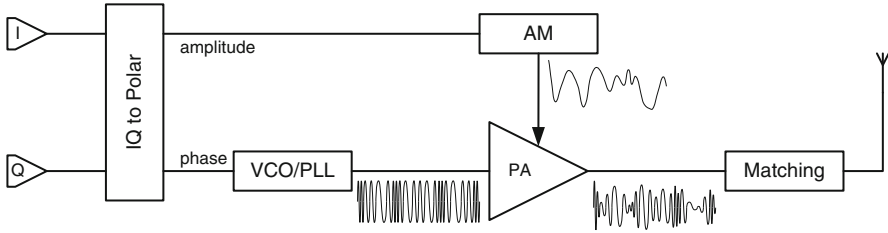


Fig. 18.5 Polar modulator architecture

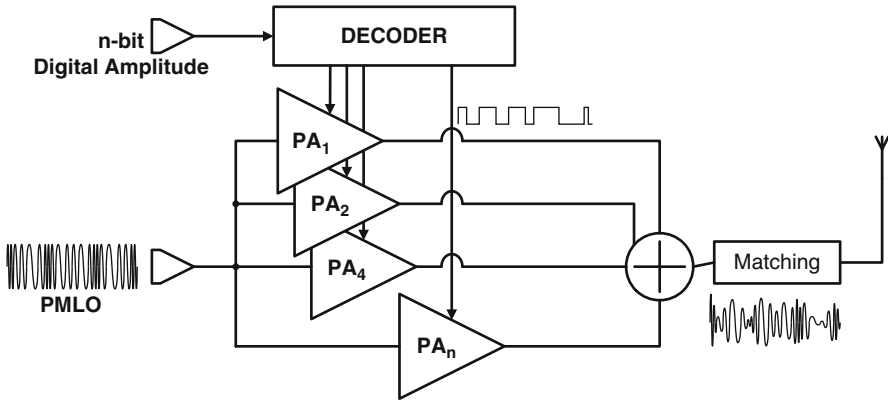
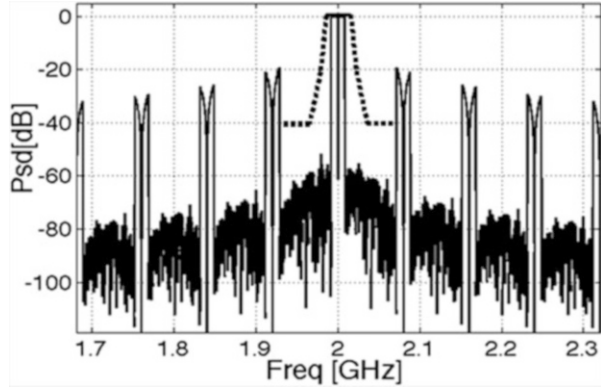


Fig. 18.6 Polar modulator with digital amplitude modulation

Phase modulators based on a digital PLL have been presented [2], but their bandwidths are still not sufficient to deal with modern, high bandwidth communication schemes. Alternatively, a phase modulated LO can be generated with a constant amplitude Cartesian up-converter, but this obviously creates quite some overhead. The AM modulator has to deliver modulated power to the amplifier, but high efficiency is difficult to combine with high bandwidth. A modulated DC-DC converter can be used for high efficiency, but its bandwidth is very limited. It may be combined with a linear regulator, which offers wide bandwidth, but bad efficiency. As a result, the combination of the switching PA with its amplitude modulator results in average efficiency and RF bandwidth.

Nanometer CMOS enables a new, digital architecture for the amplitude modulator. The switching amplifier is split up in a multitude of smaller parallel amplifiers whose outputs are summed. The amplitude of the output signal is modulated by turning on or off more or less unit amplifiers as needed (Fig. 18.6) [3, 4]. The transmitter's DAC has thus effectively been moved to the antenna. Amplitude modulation speed is no longer a bottleneck. It is now a transfer of information rather than power. The digital modulator is the base for Direct Digital RF Modulators (DDRM), a new family of RF transmitters which are likely to gain in importance, as they are extremely suited for integration in scaled CMOS.

Fig. 18.7 DDRM spectral response



Obviously, as the DDRM is in essence a DAC at the antenna, it lacks an anti-aliasing filter. As a result, both aliases and quantization noise reach the RF output un-attenuated (Fig. 18.7). They can be reduced by increasing the resolution and the baseband sampling rate though, which is more likely in the newest technologies. Furthermore, new architectures can specifically address the DDRM drawbacks. As technology scaling improves the DDRM's performance and as porting the DDRM to any new technological node is relatively easy thanks to its digital nature, its importance will continue to grow.

18.3.1 A Compact 90 nm CMOS Polar Amplitude Modulator

A compact 90 nm CMOS polar amplitude modulator is presented in this paragraph [5]. It is based on a cascoded common source amplifier that is divided in multiple unit amplifiers. All units are driven by a common RF phase-modulated signal. Each unit amplifier has a dedicated cascode transistor which is also used as a switch that turns the unit amplifier on and off based on a digital control bit (Fig. 18.8). The output currents of all units are summed to shape the RF envelope. As the bias current is switched off in the unused branches, a good efficiency is obtained. Furthermore, the open loop structure and the absence of high impedance nodes give this amplitude modulator a wide bandwidth.

An 8 bit prototype has been implemented. This gives 2 bit margin to transmit a WLAN-like 64 QAM modulated OFDM signal [4]. Monotonicity of the DAC may be obtained by using thermometric coding. However this would result in a complex decoding scheme, and a large area overhead. Binary and thermometric coding are therefore combined to get the advantages of both schemes, while limiting the disadvantages [6] (Fig. 18.8). In the prototype, 4 LSBs are addressed binary while four MSBs are thermometric coded. The size of the unit CS transistor is a compromise between loading of the phase modulated LO and mismatch. It is scaled to obtain monotonicity of the amplitude response in presence of device mismatch.

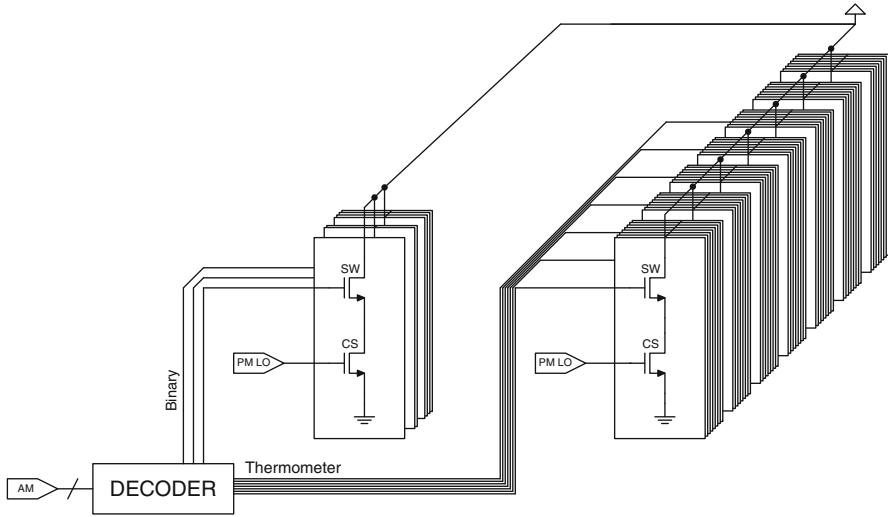


Fig. 18.8 Polar DDRM based on CS amplifier units and segmented digital control

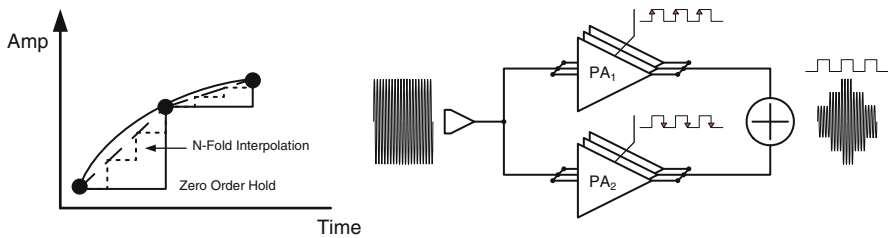


Fig. 18.9 N-fold interpolation principle & twofold DDRM schematic

As discussed before, a DDRM behaves as a DAC without anti-alias filter and the aliases of the transmitted signal are present at multiples of the clock frequency around the LO frequency. They may thus violate the out-of-band emission requirements. The aliases can be spread and attenuated by increasing the baseband sampling frequency. However, the required oversampling may be too high. The aliases can also be reduced by applying linear interpolation between two consecutive samples. This adds a supplemental sinc filter to the DAC output spectrum [7]. In practice, linear interpolation can be approached in discrete steps, resulting in an intermediate filtering (Fig. 18.9). The presented prototype features twofold interpolation by clocking two parallel DDRM arrays at opposite baseband clock edges.

The layout of the DDRM matrix is primordial for its performance. As the DDRM is a DAC, matching is important. Both the phase modulated LO and the output RF are distributed to the various cells. Coupling between both should be minimized to limit LO feed-through. Digital baseband data is distributed throughout the matrix as well and coupling to the RF lines may result in spurs at the output. Finally, long RF

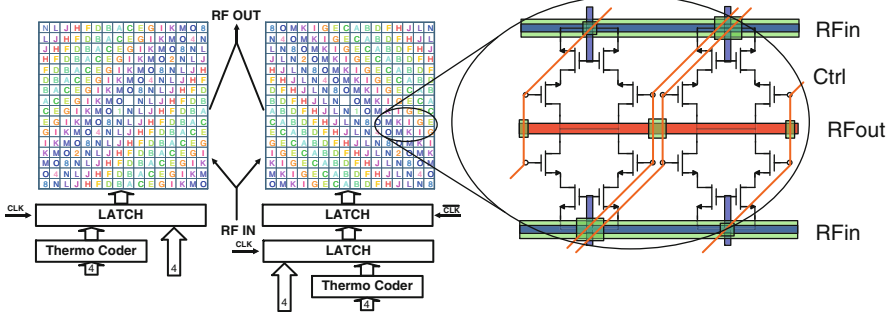


Fig. 18.10 (Double) DDRM matrix & Compact DDRM basic cell

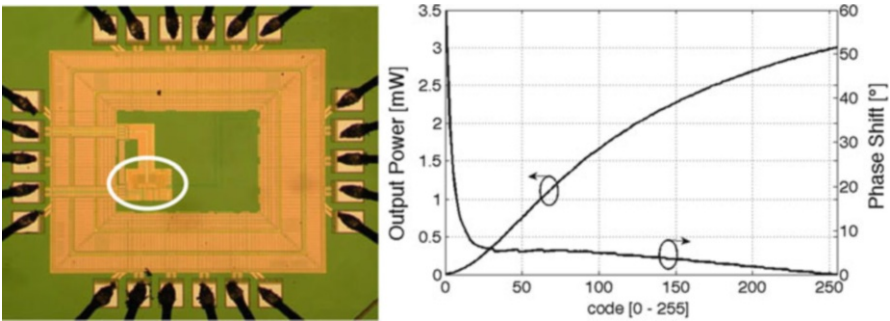


Fig. 18.11 (a): Compact DDRM chip photo with $110 \times 65\mu\text{m}$ circuit highlighted. (b): DDRM AM/AM and AM/PM response

lines increase the losses and reduce the global efficiency of the transmitter. All these points have to be considered carefully to layout the DDRM matrix.

The 8 bits amplitude modulator is segmented into four binary coded LSBs and four thermometric coded MSBs. The thermometric unit cell consists of 16 LSB units. To reduce errors due to process gradients, these are distributed along the central diagonal resulting in a matrix of 16×16 LSBs. An extra border of dummy cells is added. The binary units are placed on the central diagonal and distributed with their center of gravity in the middle. The thermometric unit cells are flipped both vertically and horizontally to share the horizontally routed RF and supply lines. RF input and output are routed on alternating horizontal lines to avoid their crossing. The digital control lines are routed along the diagonals. This strategy results in a compact structure as presented in Fig. 18.10. The complete modulator consists of two identical flipped DDRM arrays. The digital amplitude words are applied through latches clocked on opposite clock phases to obtain the twofold interpolation.

The chip has been realized in 90 nm CMOS [5]. The microphotograph of the chip is presented in Fig. 18.11a. The effective area of the polar amplitude modulator is an extremely compact $110 \times 65 \mu\text{m}^2$.

To measure the prototype, it was bonded directly on a printed circuit board (PCB). Figure 18.11b shows the measured static AM/AM and AM/PM responses of the modulator. The non-linear AM/AM curve is mainly due to the varying output impedance of the amplifier with the digital code. This is a common problem with DDRM, as the number of active cells varies with the output amplitude. The AM/PM curve is flat at the highest codes, but changes rapidly at the lowest codes due to a higher contribution of LO feed-through. Fortunately, the digital nature of the transmitter makes it easy to compensate both curves through pre-distortion, be it that this reduces the effective number of bits.

The modulator is tested with a WLAN-like 64 QAM OFDM signal. The amplitude data is pre-distorted based on a static look-up table and applied at a rate of 40 MHz to the modulator. Note that this baseband clock speed was limited by the available equipment, rather than by the modulator. With a phase modulated LO at 2.45 GHz, an EVM better than -26 dB is obtained for -2.5 dBm output power. The maximal drain efficiency is 23 % at 5 dBm Pmax.

18.3.2 A Class E Impedance Modulated DDRM

Previous paragraph described a digital amplitude modulator which is the base for many polar DDRMs. In this paragraph an amplitude modulator that acts on the amplifier's load through a digitally programmable impedance matching network is presented. This architecture is demonstrated with a class-E based polar amplifier.

The class-E amplifier is a switching amplifier that achieves high efficiency by avoiding any overlap of voltage over and current through the switch [8]. As a result, no power is dissipated and a theoretical efficiency of 100 % is achievable. In a class-E amplifier, the output power is inversionally proportional to the load impedance. Depending on the supply voltage and the required output power an impedance transformation network is placed between the amplifier and the antenna. Its parameters are traditionally fixed at design time, but in this work, the matching network is used for the dynamic amplitude modulation of the polar amplifier. As the network is controlled directly from the digital data stream, the achievable modulation bandwidth is large. Furthermore, the efficiency of the presented scheme is only limited by second order effects, mainly the deviation from the optimal class-E operating point during operation and in less extend the parasitics in the matching network. The choice of the transformation network is a compromise between tunability, efficiency and practical realization. The ratio between minimal and maximal transformed load impedance determines the dynamic range of the resulting amplifier. It is limited, as the losses in the matching network increase with its complexity and reduce the efficiency. For 10 dB dynamic range, the ratio between the maximal and the minimal transformed load impedance should be a factor 10. To keep the matching network realizable, tuning of inductors is not considered. Figure 18.12 shows the simulated real impedance and phase of the chosen π -type matching network at 2.4 GHz when sweeping the digitally controlled

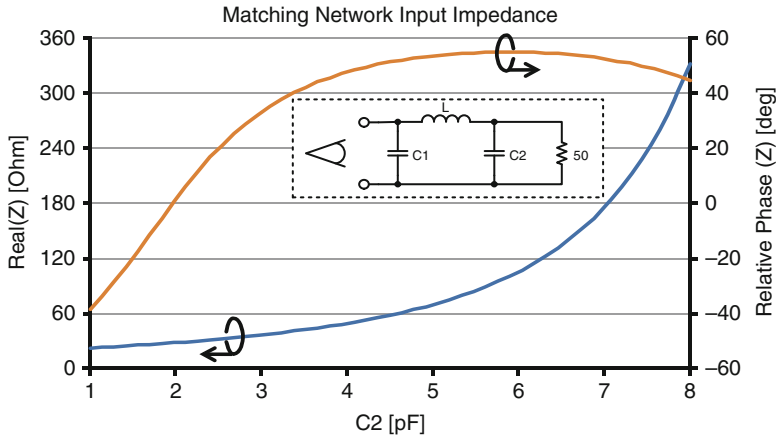


Fig. 18.12 Pi type impedance transformation network response

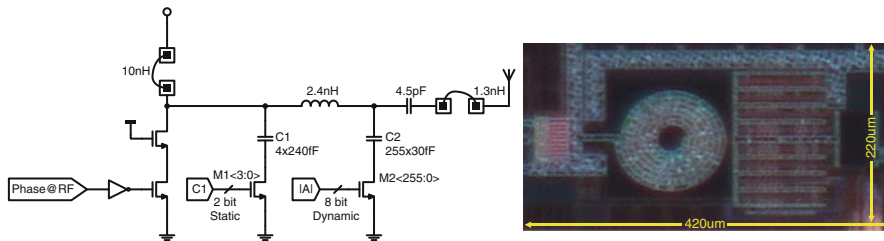


Fig. 18.13 Impedance modulated class-E amplifier circuit diagram and photograph

capacitor C2. The real impedance seen by the amplifier varies from approximately 20Ω up to 300Ω. The non-linear shape implies that pre-distortion is needed, both for amplitude and phase.

The impedance modulation concept is demonstrated with a 90 nm CMOS polar amplifier prototype [9]. Its circuit diagram and microphotograph are presented in Fig. 18.13. The main amplifier is protected from the high voltage swing which may reach above the supply voltage due to the class-E operation, by a thick-oxide cascode transistor. A 1 cm bondwire to the PCB is used as a 10 nH load inductor. The total active area of 420 μm × 220 μm is dominated by the tunable impedance transformation network.

For the dynamic measurements, amplitude and phase are generated with Matlab and pre-distorted based on static measurements. The eight bits wide amplitude information is sent to the digital impedance modulator at a rate of 100MS/s, while the LO is phase-modulated with the pre-distorted phase information.

A dynamic range of 11dBm is measured. Figure 18.14 shows a measured vector diagram after the receive filter for a π/4 DQPSK modulated Bluetooth-like signal

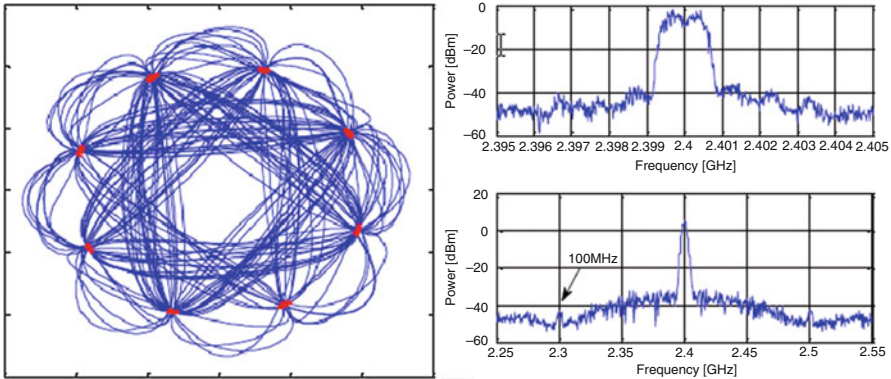


Fig. 18.14 Pi/4 DQPSK diagram & spectral plots

with a symbol rate of 1MS/s (bitrate of 2 Mb/s) at 2.4 GHz. The transmitter features an EVM of 2.6 % at 6 dBm RMS power. Both the narrow and the wide band spectral plots of the modulated output are shown in the same figure. Some alias power is visible at 100 MHz offset due to the direct digital modulation.

18.3.3 An IQ DDRM with RF FIR-Based Quantization Noise Filter

The previous paragraphs introduced direct digital modulation for a polar modulator. However, due to the bandwidth increase introduced by the Cartesian to polar conversion and the complexity of a digital LO phase modulator, the polar architecture is less suited for modern wide bandwidth communication standards. Two digital amplitude modulators can be combined into a Cartesian digital modulator to solve this problem. One of both is modulated with a fixed LO to up-convert the I baseband data, while the other has a fixed 90° LO for the Q data. Differential modulators accommodate the sign change of I and Q. A compact IQ DDRM cell that combines all phases into a single unit is presented in Fig. 18.15. It consists of 4 RF switches (RF0, RF90, RF180, RF270) modulated with fixed 25 % duty cycle LO phases in series with the digitally controlled baseband switches (EN0, EN90, EN180, EN270). The latter determine whether a certain LO phase is active in a given cell. The eight thin oxide switches are cascaded with a thick-oxide current source that determines the gain of the cell and protects the low voltage switches from the large output swing. The output currents of all DDRM units are summed at their outputs and dumped into the load. To transmit the quantized code $a + jb$ for example, an equivalent of a EN0 and b EN90 switches are closed. The resulting drain current is depicted in Fig. 18.15.

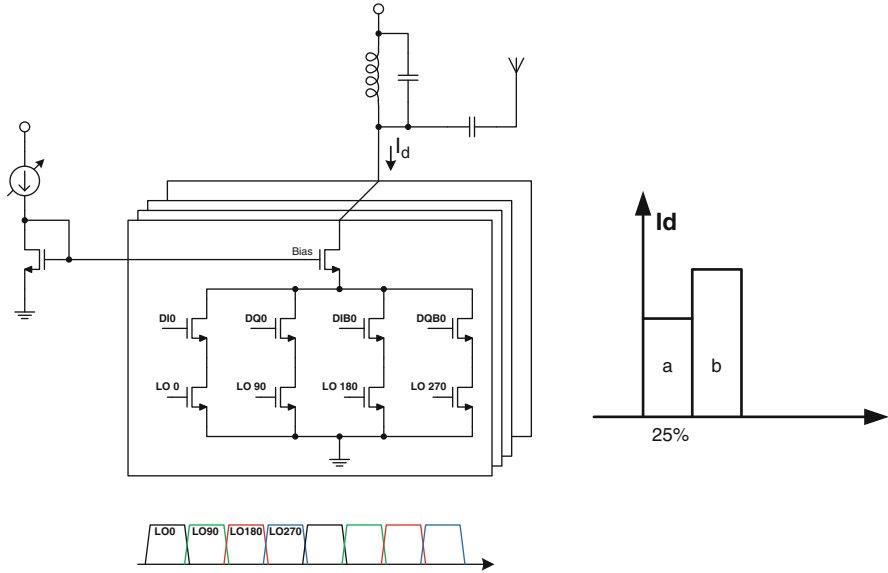


Fig. 18.15 Compact 25 % duty cycle IQ DDRM

The presented cell is compact as it combines all thin oxide switches under a single thick oxide current source, the latter consuming the largest area in the unit. Its bias voltage can be used to control the average output power.

As the architecture is based on Cartesian modulation, it has potentially a wide bandwidth. However, besides the benefits, this architecture obviously shares the main disadvantages of Direct Digital RF Modulation, being quantization noise and aliases. Both can be reduced by increasing the baseband oversampling [10] and increasing the number of bits [11]. For saw-less FDD operation the quantization noise requirements are very stringent though. The noise floor should be reduced below -160 dBc/Hz [12] in the RX band. In FDD, the most stringent noise requirements are localized in the RX band associated with the TX band. Instead of aiming to reduce the global out-of-band quantization noise, it is sufficient to filter the quantization noise specifically at the RX frequency. This can be achieved by combining a number of correctly sized DDRMs to implement a FIR filter that acts directly at RF (Fig. 18.16). The bias of the DDRMs' current sources determine the FIR filter coefficients and can be tuned to adjust the filter's shape and notch position. Note that the depth of the notch will be limited by the thermal noise of the current sources and the LO phase noise.

A digital transmitter prototype was realized in 130 nm CMOS and contains four 8 bit DDRM matrices [13]. They are fed from a 2.7 V supply. The digital data between each matrix is delayed by flip-flops (FFs) to form a fourth-order RF FIR filter. The 4 LO phases with 25 % duty cycle are generated on chip by a digital frequency divider. The digital circuits, the LO generator and the switches in the

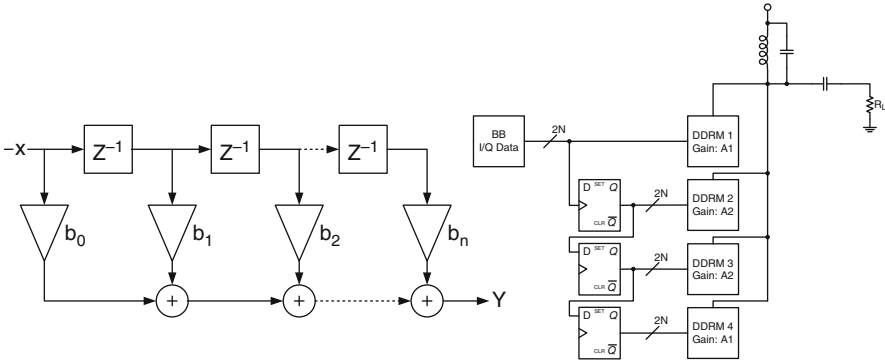


Fig. 18.16 FIR and its implementation in an IQ DDRM

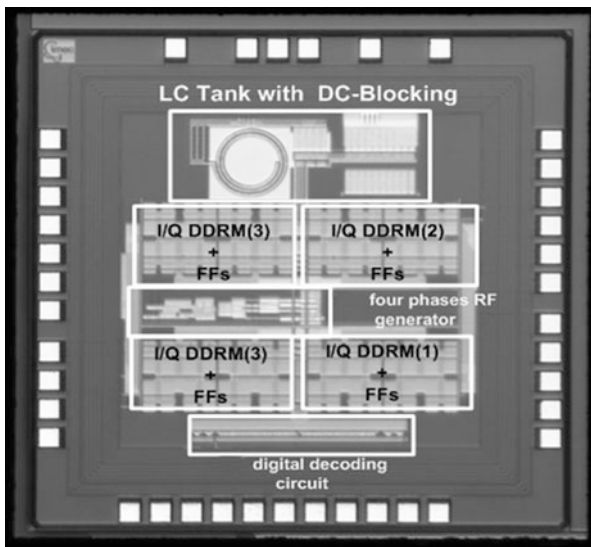
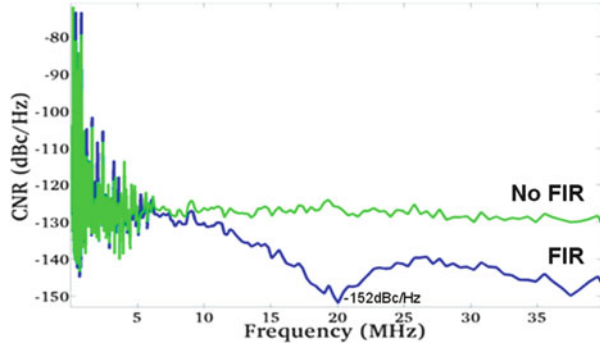


Fig. 18.17 Compact 25 % duty cycle IQ DDRM

DDRM are all powered from 1.2 V The resulting chip occupies an area of $1.5 \times 1.5 \text{ mm}^2$ (Fig. 18.17).

The transmitter achieves a peak power of 15.4 dBm with a drain efficiency of 13 %. The power consumption of the drivers and the digital part (the flip-flops and the digital decoding) is 55 mW. Pre-distortion is applied to compensate the non-linear AM/AM behavior of the IQ DDRM. This pre-distortion is more complicated than for the polar DDRM where AM/AM and AM/PM can be considered independently. In the IQ DDRM, I and Q are linked, and a pre-distortion matrix is used rather than a vector.

Fig. 18.18 Quantization noise notch with FIR DDRM



The effect of the FIR notch is demonstrated in Fig. 18.18. For a 200 kHz baseband tone transmitted at 900 MHz, the noise floor reaches -152 dBc/Hz @ 20 MHz offset, an improvement of 22 dB compared with a FIR-less modulator. When applying a 64 QAM signal with 10 MHz RF BW to the transmitter, an EVM of -27.2 dB is measured at 4.1 dBm RMS output power. The transmitter then consumes 48 mW from the 2.7 V supply

18.3.4 A CMOS IQ Doherty DDRM with Modulated Tuning Capacitors

Many challenges that exist for traditional transmitters still hold for DDRM based transmitters and some of the solutions for these challenges can take advantage of the DDRM architecture. Modern communication systems use complex modulation schemes with a high peak to average power ratio (PAPR). For a good average transmitter efficiency, its drain efficiency should be preserved at lower power levels such as at 6 dB back-off or lower. The regular DDRM typically has a Class-B like efficiency curve [13]. In traditional power amplifiers, the Doherty architecture can be used to increase the efficiency at back-off [14]. It combines a main amplifier with a peaking amplifier which is turned on when the main amplifier is at maximal output swing and efficiency (Fig. 18.19a). The main amplifier still works at maximal efficiency at higher power and the power for the peaks is provided by the auxiliary amplifier.

A major design challenge of this architecture is the accurate biasing and modulation of the auxiliary amplifier. In a DDRM, the transmitted amplitude is exactly controlled at any moment in time, so it makes sense to apply the Doherty scheme on the DDRM transmitter. Indeed, the digital modulation of both the main and the peaking DDRM allow a perfect control of the cooperation between them.

A Doherty transmitter requires a power combining impedance transformation network, which is traditionally realized using an off-chip $\lambda/4$ Transmission Line.

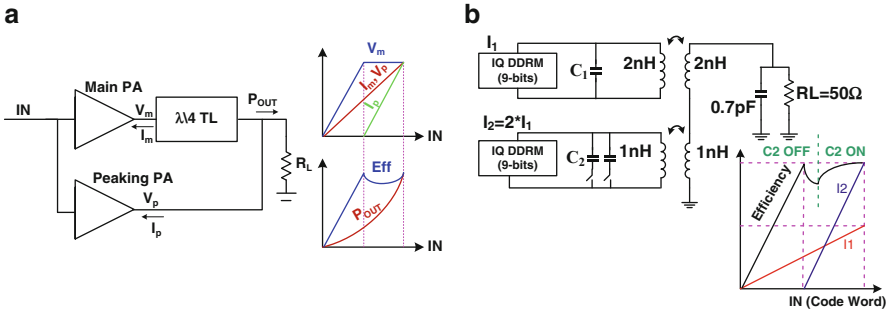


Fig. 18.19 (a): Doherty principle. (b): Doherty DDRM with transformer based power combiner

However, an on-chip impedance transformation network using integrated transformers can be used for power combining and impedance transformation [15, 16]. Two transformers are combined to create a fully integrated Doherty amplifier [17]. The analog amplifiers can be replaced by DDRMs though [18] (Fig. 18.19b). For output powers below 6 dB back-off, the peaking amplifier is turned off and ideally the peaking transformer is shorted. The transformed output impedance is seen as a load by the main amplifier. At 6 dB back-off the main amplifier has maximal swing, and the transformed load is optimal. Beyond this power, the peaking amplifier gradually increases its contribution, and feeds part of the output load. As a result, the load seen by the main amplifier decreases gradually. The latter delivers more output power at maximal voltage swing and stays optimally loaded. The power delivered by the peaking amplifier continues to increase until both amplifiers deliver their power at full swing on the output impedance, which is then divided between both.

In practice, it is impossible to short the second transformer completely when it is not used. A low impedance would require very large switches that would introduce too large parasitics. An alternative is to open the primary of the second transformer. When no current flows through one transformer winding, the other acts as a single inductor. However, the tuning capacitor on the primary of the second transformer then still creates a high impedance in the signal path. This can be solved by disabling this capacitor with a series switch when the auxiliary amplifier is not in use. Again, this is easily achievable in a DDRM based amplifier, as it is exactly known when the auxiliary amplifier is in use.

A 9 bit prototype of the IQ digital Doherty transmitter is realized in 90 nm CMOS [18]. Its microphotograph is shown in Fig. 18.20. The chip measures $1.9 \times 1.9 \text{ mm}^2$. The main and auxiliary DDRMs are fed from 2.4 V while the digital circuits, including the LO are powered from 1.2 V. At 2.4 GHz, the digital transmitter achieves a peak power of 24.8 dBm with a drain efficiency of 26 %. This efficiency is also achieved at 6 dB back-off. From the measurements in Fig. 18.20 the benefit of the switched transistor in the second transformer is clearly visible.

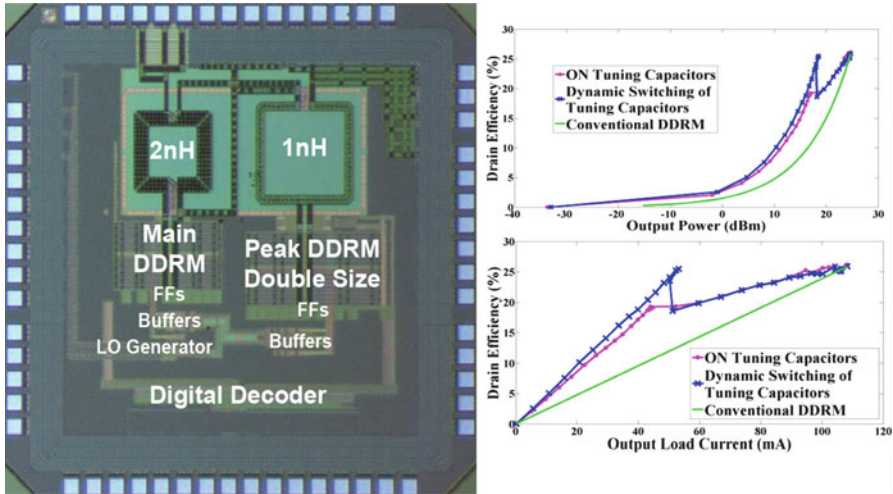


Fig. 18.20 Doherty IQ DDRM chip photo with measured efficiency

18.4 Conclusions

Nanoscale CMOS increased computing power tremendously and introduced complex modulation schemes in wireless communication. The limited analog performances of the technology forced the development of new transceiver architectures to deal with the new parameters and take advantage of the new potentials. The traditional analog transmitters are now supported by more calibration while increased configurability improves both the functionality and the performance. In parallel, the digital domain is moving towards the antenna in the wireless transmitter. This is expected to be a trend as the technology scales further and innovative architectures improve the DDRM even beyond the technological scaling.

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