Chapter 10
Is Digital SMPS Ready to Eliminate Analog Regulators for Portable Applications Power Management?

S. Cliquennois and A. Nagari

Abstract This chapter reviews the challenges which integrated voltage regulators have and will have to tackle for power management of portable applications while focusing on how the Digital Switched-Mode Power Supplies (SMPS) technology, already widely used for medium and high power systems, is able (or not) to challenge the classical analog loops. The study will explore mainly step-down architecture, and analyses the challenges in many aspects of integrated regulators design: efficiency, area, speed, flexibility, current estimation, low-power modes, multi-phases and control sharing, voltage scaling and EMI.

10.1 Introduction

Integrated Switched-Mode Power Supplies have become ubiquitous regulator architectures in portable applications, and have superseded the classical Low-Dropout (LDO) linear regulators for every power hungry (i.e. more than half a watt) supply needed on portable, battery-operated devices. Although LDO provide low-cost, fast and low-noise regulated output voltages, their typically very low efficiency – less than 28 % for a typical output voltage of 1 V supplied by a regular 3.6 V battery – is disqualifying them for the very demanding core of portable applications (processors, modems, memories, I/Os…). More than 85 % peak efficiency can be expected from a noisy and expensive – because using an external coil – well-sized SMPS [1].

The main and specific challenges which SMPS designers have to face when working for portable applications will be reviewed, and discuss if so-called digital SMPS can bring added value with respect to their analog counterparts, a debate open for many years [2].

S. Cliquennois (✉) • A. Nagari
ST Microelectronics, Grenoble, France
e-mail: sebastien.cliquennois@st.com

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While efficiency at high load currents is a critical factor of merit of integrated SMPS, it is not the only one: in order to optimize speed of processors, which can dynamically adapt their speed and power supplies depending on their operating mode, regulators need to be very precise and fast – a trend that is becoming more stringent as the processors supply voltage lowers, and the maximum current capability requirement grows [3]. Reaching this transient speed specification often requires using coil-current sensing techniques which are essential in modern, fast SMPS. The different control techniques will also be discussed.

An often over-looked feature in literature is the capability for switched regulators to keep a very good efficiency figure of merit on their full output load range, which requires dedicated and crafted low-power modes, and on-the-fly efficiency optimization tricks [4].

While the trend in the previous decade was to aim at higher and higher switching frequencies to reduce external component footprint – mainly coil – the recent surge of tablet computers is actually orienting integrated SMPS in another direction: even if integration remains important, the need for higher current capabilities at reasonable efficiency is nowadays driving development of integrated multi-phase DC-DC converters, where digital control architectures can bring some benefits.

10.2 Generic Analog and Digital SMPS Architectures

Figures 10.1 and 10.2 illustrate the core components of "analog" and "digital" buck (i.e. step-down) converters. The power stage is driven by logical signals, hence actually possesses an intrinsic digital control, although design of integrated power MOSFETs is a purely analog task, where robustness, channel on-resistance, efficiency of driving buffers are the main aspects to be controlled. This important part of switched-mode power supplies is exactly the same whatever the type of control chosen.

An essential differentiation lies on the control loop. 'Pure Analog' SMPS rely on a number of electrical signals to perform feedback for regulation. Output voltage is generally sensed, and most of fast control structures, may they be current-control [1] or sliding-mode controllers [5] use either directly a current sensing resistor, or better, a lossless current sensing circuitry in order to re-construct the current information. Note that the intermediate LX node can also be sensed, as it provides very relevant information (on current direction in coil for example).

On the other hand, digital SMPS are all characterized by presence of one of several ADC converters which at least convert the error voltage (*Vout-Vref*) into a digital signal (common architectures are windowed flash, delay-lines or SAR ADC), and generally also input voltage (battery voltage in portable applications), an information which is essential to many compensation or current estimator schemes. It must be noted that the coil current bandwidth is much more important that the switching frequency, hence digital estimation of current has to rely on

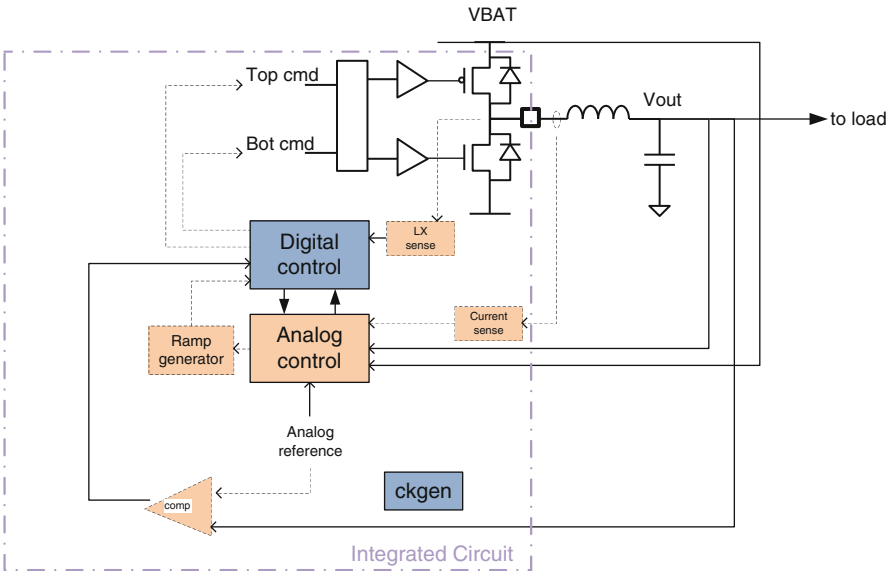

Fig. 10.1 Generic "analog" integrated SMPS block diagram

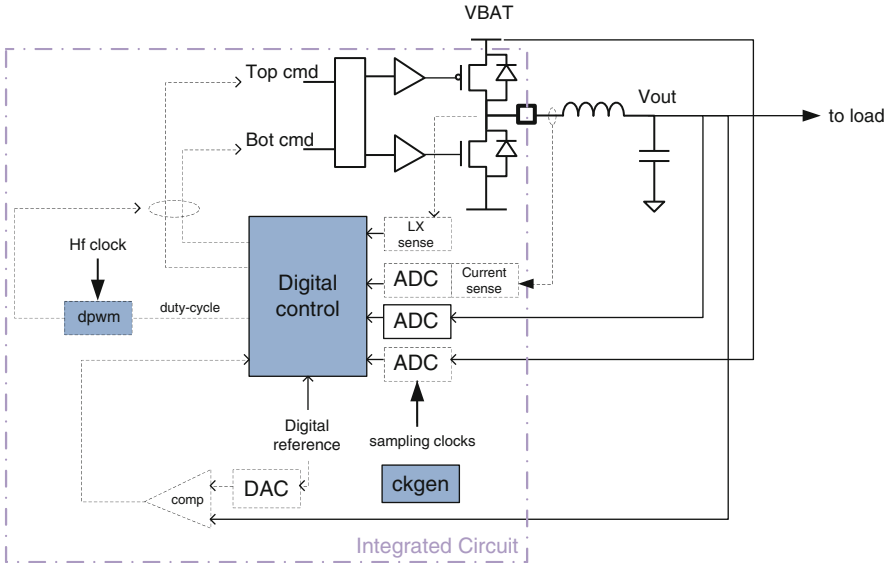

Fig. 10.2 Generic digital SMPS block diagram

sampled information of coil current, one among the challenges that digital control has to face.

The different control strategies will be discussed more in detail, but essential part of control is to generate a two-leveled (i.e. digital) signal which will control

power switches. An historically important family of controller generates Pulse-Width Modulated signal, may it be analogically thanks to a clock-synchronized ramp generator or digitally by the means of a Digital PWM, for which many different implementation details have been proposed [6].

Another important family does not rely on PWM, but directly generates the control signals using for example a sliding mode approach [7]. This approach, which leads to very fast response, has been implemented both in analog and digital world.

10.3 Efficiency

Efficiency is a key parameter of any power management system. It will have a direct impact on system thermal dissipation, as well as on battery life in portable systems.

While theoretical efficiency of SMPS is 100 % [1], losses which affect this figure can be split into three main categories: Ohmic losses, which main components are power FETs on-resistance, coil series resistances and parasitic resistance. Switching losses, which account both for losses due to buffers needed to charge and discharge power mosfets gates, as well has losses due to switching parts of control system. Quiescent losses, which are static DC currents needed in control parts.

Ohmic losses and switching losses are essentially identical in analog and digital SMPS, but they can be minimized by adapting the size of power mosfets to output currents: at low currents, ohmic losses are less important, so reducing the size of power stage has a very beneficial impact on switching losses. An adaptive size selection can be done digitally. Note that discussion is only concerned with synchronous rectification, asynchronous rectification when a simple diode replaces the bottom switch being much less efficient and generally avoided in integrated designs.

Unlike analog parts which in general require to be biased during operation, digitally-controlled SMPS can generally operate at zero-DC bias.

However, because losses are dependent on output load, the efficiency curve has to be optimized in the four areas where buck converters operate:

- The high current area, where ohmic losses are dominant, and proper sizing and choice of MOSFETs (e.g. use dual-Nmos architectures instead of Nmos-Pmos, which reduces gate capacitance for same on-resistance)
- The medium current area, where switching and ohmic losses are dominant. The two previous areas correspond to SMPS supplies circuits in full to medium activity.
- The low current area, where if switching is kept, switching losses become way to dominant, so some pulse-skipping designs, or pulse-frequency modulation scheme have to be devised. This area corresponds generally to load circuits with little activity.

– The no-load area, which is an essential part, and often overlooked feature: SMPS need to supplies circuits which are not working (in retention state) and only compensate for leakage of supplied parts, with no transient load involved.

10.4 Scalability, Flexibility and Partitioning

Integrated SMPS for portable application have to face the tough challenge of area optimization, which has a direct impact on cost of solution. Whereas digitally controlled-SMPS comprises a control part which scale well with process, the area of power mosfets, which does not scale very well with technology – is dominant in most of integrated implementations. Actually, the problem is even getting worse with more advanced technology nodes: below 65 nm, it is rare that native mixed technologies support devices that can stand directly battery voltage (up to 4.35 V) as drain-source voltage, making usage of cascoded power stage compulsory – which added to more area and losses dues to more complex gate drivers.

On the other hand, a very scalable architecture for digital SMPS is shown on Fig. 10.3: the System-In-Package (SiP) approach allows assembling different circuits with different technologies in a single package. Typically, a product like ST-Ericsson's M7350 comprises of an "analog" die dedicated to power management, and a "digital" die – which here includes a modem circuit. Classical SMPS are fully embedded in analog die, but digital SMPS can have their (digital) control

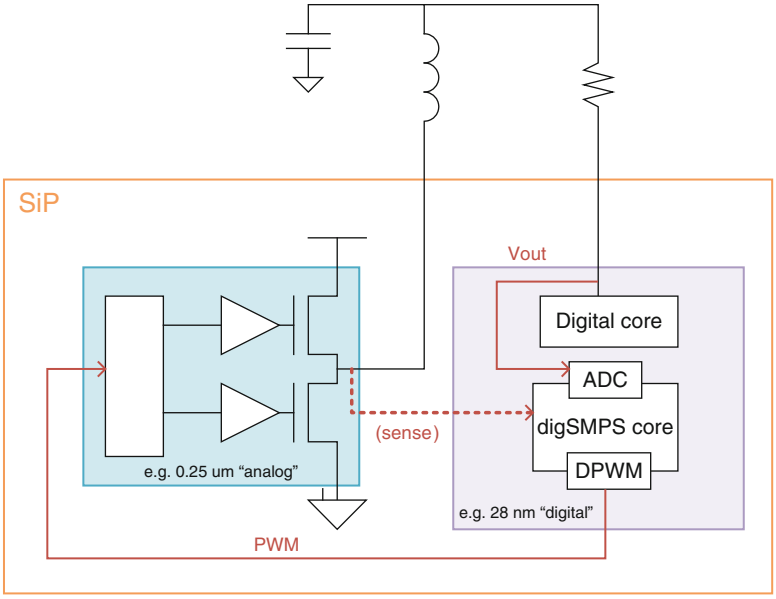

Fig. 10.3 Proposed system-in-package partitioning

part, ADC and DPWM embedded in digital die, while power part remains in analog die. Not only this approach allows a better scalability of SMPS, but is also give more flexibility and control to the digital die, which can directly control its supply internally. Remote sensing, which allows a better voltage stack optimization can be directly done inside digital chip. This approach requires an additional LDO regulator that allows for startup and can be turn-off when SMPS auto-supplies its digital part. The main drawback of this approach is that package thermal characteristics should be able to handle both power FETs and load (i.e. digital IC), which is not the trend for mobile processors.

10.5 Current Estimation Challenges

While voltage-mode (VM) loops have been the first ones to be proposed and are still widely used, the advantages of current-mode (CM) or sliding-mode control in terms of load transient speed, maximum current limitation, and multi-mode optimizations such as automatic power-stage sizing or automatic mode switching are tremendous [1]. Many CM analog implementations are using a discrete sense resistor, which is a solution to be avoided in portable applications, both because of sense resistor cost and additional loss in efficiency.

Several analog solutions without external sense resistor have been proposed:

- Internal current sensing: principle schematic is shown on Fig. 10.4. This solution generally shows a poor precision due to inherent poor matching -between very big power MOS and integrated sense-FETs. Bigger sense-FETs would imply un-acceptable efficiency losses.
- External R-C sense [8]. This type of sensing is lossless and relies on the fact that sensed voltage is equal to

$$V_{sense}(s) = I_L(s) \cdot R_L \cdot \frac{1 + s\frac{L}{R_L}}{1 + sR_fC_f}$$

i.e. $V_{sense}(s) \sim I_L(s)$ if $L/R_L = R_f C_f$. The spread in R,C and R_L are such that this solution requires calibration.

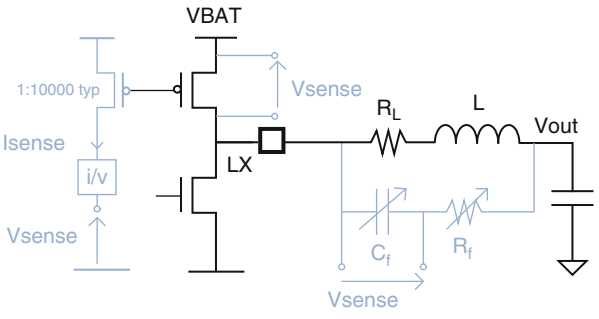

Fig. 10.4 Different current sensing strategies

– Structures based on LX node sensing (Fig. 10.4). This approach generally relies on sensing and amplifying *VBAT-LX* voltage, which is proportional to output current on the top mosfet conducting phase.

On the control digital side, a first approach consists in implementing the above analog solutions, and using an ADC to convert sensed current/voltage. Unlike ADC used for output voltage sensing which is generally windowed around reference, the current sensing ADC should be full range.

Another scheme consists in directly estimating coil current in digital world: a first digital-only first order current estimator has been proposed [9], and relies on the following approximation:

$$V_{OUT} \approx DV_{BAT} - I_L(DR_{ONP} + (1-D)R_{ONN} + R_L)$$

It allows calculating I_L, but requires a precise measurement of *Ronp*, *Ronn* and R_L, requiring extra (analog and digital) circuitry for calibration. What's more, this equation is only valid in CCM.

Another digital-only solution is to implement a digital current estimator [10], which can be based on a state-space representation of system. It provides a robust solution, but comes at a cost of implementing the estimator, requiring real-time complex operations such as matrix multiplications, hence limiting the switching frequency of system.

10.6 Low-Power Modes

While literature concentrates generally on CCM, where the transient and efficiency performance of SMPS are critical, commercial SMPS must keep an acceptable efficiency even on low output current, and particularly when load is such that current in coil in below critical conduction current, hence naturally inverting current in coil if system stays in CCM [22].

10.6.1 CCM Detection

Detecting this threshold is fundamental so that system can switch to a mode where conduction is such that coil current is not inverting anymore, and consequently, the system now passes some time in hi-impedance mode, which can be done for example by skipping pulses when voltage is above a determined thresholds, or changing control scheme to Pulse-Frequency modulation (PFM) where a fixed current pulse is output at a variable frequency.

If a very precise current sensor is implemented, it can be used for this threshold detection, however, it is preferable for precision to use a dedicated circuitry. It must

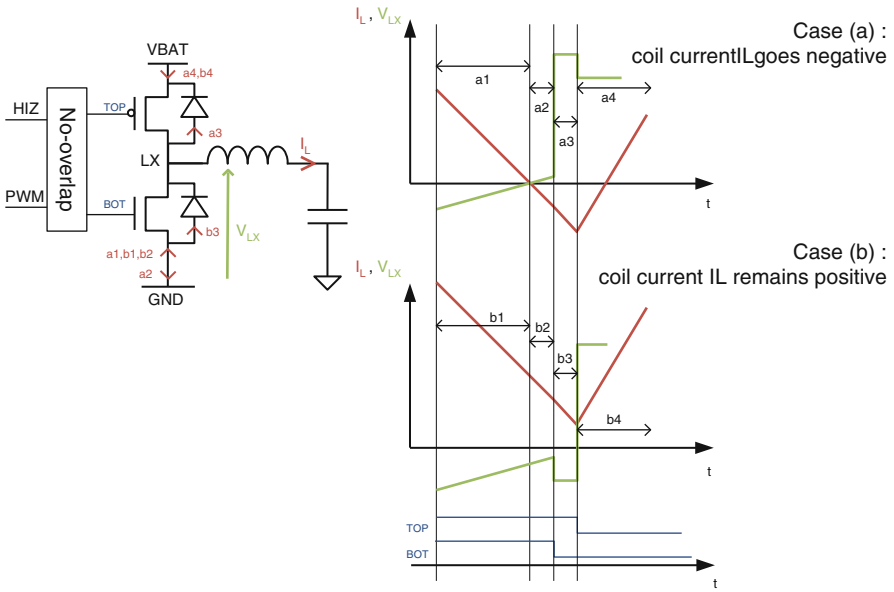

Fig. 10.5 LX node sensing for current inversion detection

be noted that if CCM detection is done with a current actually above the actual critical conduction current, system will oscillate between the full power (CCM) and whatever the low power mode chosen, creating an important ripple on output voltage.

Most CCM detection schemes rely on analog principles, but they output a single-bit digital signal which can be used in digitally controlled SMPS. A common principle for bucks consists in relying on body-diode conduction at the end of conduction period (cf. Fig. 10.5): when current in inverted in coil at end of conduction period, during the dead time, current is evacuated through top mosfet body diode, instead of bottom mosfet body diode when coil current is above critical conduction threshold. This conduction on top MOS can be either detected by a fast sampled comparator on LX node [11], or detecting phase delta on LX node.

10.6.2 PFM Digital Implementation

PFM mode is generally used for ultra-low current modes, where higher ripple is acceptable. Switching losses are reduced to a minimum, because the system is no clocked anymore and only generating constant *Ton* pulse (in classical implementations). Using such a scheme for "digital" SMPS requires to be able to calculate ideal $Ton = Vref/Vbat$, and to generate the needed PWM pulse.

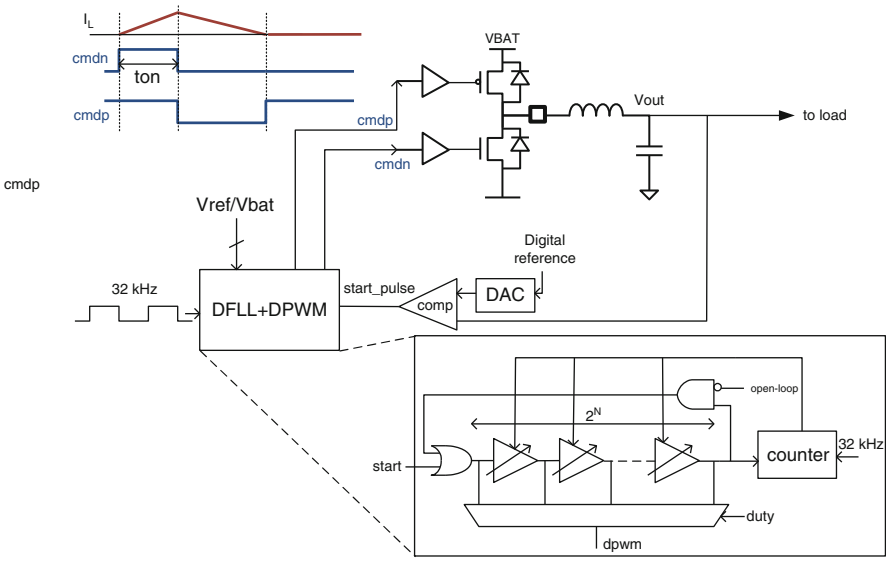

Fig. 10.6 Digital PFM loop with combined DFLL + DPWM (simplified)

However, a proposed digital implementation consists in using an open-loop DFLL/DPWM which internal clock, digitally compensated, is only woken up when output comparator states that system need to be compensated (shown on Fig. 10.6). The DFLL being open-loop can drift if supply or temperature is evolving – and these changes are compensated by running DFLL in closed-loop based on a very low-frequency clock, with a negligible impact on power consumption.

In order not to invert current in coil – which is necessarily the case if duty cycle is taken to be the ideal *Vref*/*Vbat*, and adaptive duty-cycle compensation scheme, using the previously described CCM detectors can be used.

It however appears that in the area of very low power, digital SMPS show little improvement over analog ones, because digital requires clock presence, which implies power consumption well above acceptable thresholds for ultra-low power modes where analog quiescent current can be as low as 15 µA.

10.7 Precision and Voltage Stack

By essence, regulators are designed to maintain output voltage as constant as possible, whatever the load and input voltage variations. Load and line regulation describe the DC variation of output voltage to output current and input voltage on their full range, while load and line transient are concerned with transient response to sudden variation in output current or input voltage.

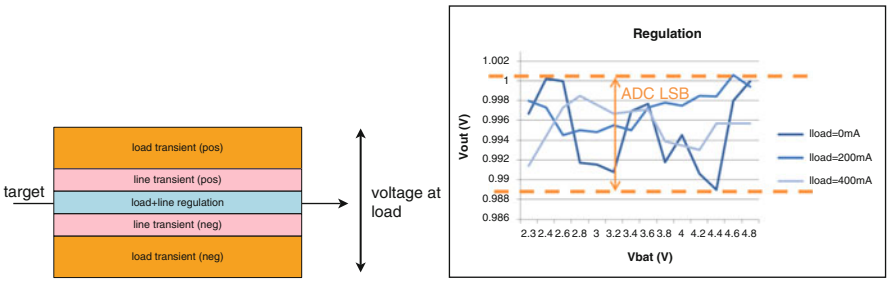

Fig. 10.7 Simplified voltage stack and typical regulation of digital SMPS

10.7.1 Load Transient and Voltage Stack

Load transient performances are of uttermost importance when designing (integrated) power supplies: processors – which supply voltage trend is to lower, while they current consumption is growing because of supplemental cores for example – tend to dynamically update they voltage request in order to set it at the minimum value to be able to work flawlessly at a given frequency.

But actually, the "minimum" value the processor shall require has to take into account the fact that the voltage which effectively reaches the core will have to account for the line and load regulation of SMPS, as well as its line and load transient in the region of operation. All this summed-up constitute the voltage stack (Fig. 10.7) which had to be minimized, and for which load transient represents an important challenge.

Load transient performance is a direct outcome of regulation loop performance, so in this matter, analog or digital implementation show significant differences.

Classical compensation analog compensation loops are voltage-loop PID controllers [1], but there are superseded by many regulation scheme using current sensing (and regulation loop) such as current-programmed control as far as linear controller are concerned.

Digital controllers have first started to implement digital PID, which performance where poorer than their analog counterparts and are now exploring a wide-range of non-linear techniques, ranging from non-linear PID to model-predictive controllers.

All controllers are actually trying to approach the optimal response to load transient, while keeping good line transient and regulation properties.

For a given LC output filter and a given load transient, the optimal transient response is known (Fig. 10.8), and it means, for a positive load transient, to turn on top mosfet on for a time *Ton* than off for time *Toff*, these two times being calculated using output capacitor charge balance approach [13]. This approach requires complex calculations that can only be handled by digital implementation and most certainly offline e.g. using look-up tables (LUT) for fast switching circuitries.

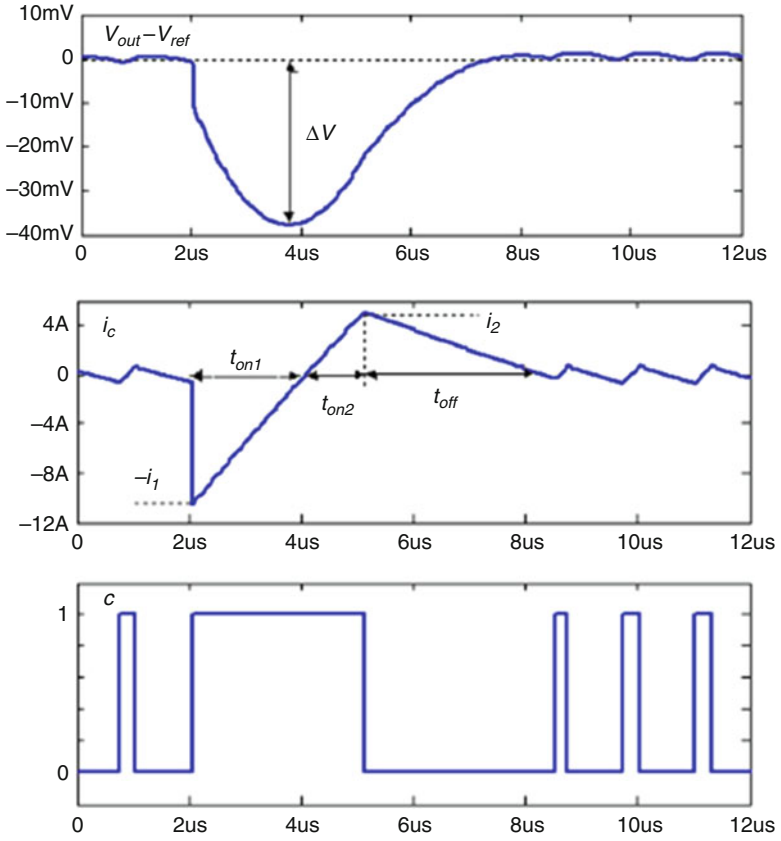

Fig. 10.8 Proximate time-optimal digital control [12]

Several proposed implementation are combining a non-linear implementation for transient response and linear controller for steady-state control.

Digital control can theoretically calculate the ideal or near-ideal response [12], but it will be limited by several factors:

- Lag due to calculation time, which can be minimized using fast processes and fast computing units, or LUT techniques.
- Lag due to ADC conversion times, and A/DC throughput rate, particularly on coil current measurements.
- Imprecision due to ADC resolution (quantization effects)

On the other hand, analog system such as sliding mode controllers, when implementing very precise current sensors, shows a transient response which (at least in theory) can nearly match optimal response [7].

Another solution for digital controllers is to implement digital sliding mode, but the three previous limitation factors will also applied, making transient response worse than its analog counterpart.

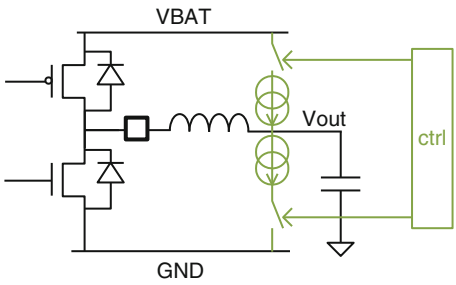

Fig. 10.9 Augmented buck

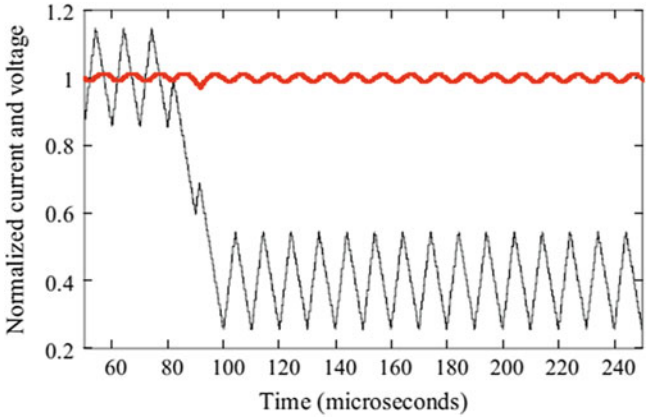

Fig. 10.10 Simulated ideal augmented control [14]

10.7.2 Augmented Systems

Nevertheless, Digital SMPS can show better load transient performance than optimal analog controllers, if they implement augmented systems [14, 20] as showed on Fig. 10.9. When a load transient is detected (on output voltage) digital turns on an extra current source which help to sink or source current in the load, hence reducing the over/undervoltage.

The extra current source is then turned off when output voltage has recovered. Figure 10.10 illustrates the ideal case when output current need is integrally compensated by current source, which is never the case. However, actual (unpublished) silicon implementations have shown that load transient can be reduced by a factor of 2 (this figure depends on size of current source). The silicon area cost depends on the size of the extra current sources which are chosen, but these types of techniques which need to be further studied are good contenders to optimal analog controllers, with an extra area cost.

10.7.3 Digital SMPS Precision and Ripple

A major drawback of most digital SMPS structures is that they use an ADC which LSB limits the resolution of system. A fundamental stability equation [15, 23] states that in order to avoid limit cycles, resolution of DPWM must be high enough to ensure that output voltage can be set to lie into ADC zero-bin. Because of limited feasible resolution of DPWM, this condition greatly limits the precision of digital SMPS, compared to analog SMPS where precision can be only limited by loop gain. A typical precision of reported digital SMPS lies between 5 and 10 mV, whereas analog loop can achieve regulation in the range of less than 1 mV.

What's more, the needed reported DPWM precision required is typically around or more than 10 bits, making direct DPWM implementation impossible, because of required time resolution of such a system. It is hence necessary to use dithering or delta-sigma modulation to achieve an equivalent average resolution with less "physical" bits in DPWM. This technique generates low-frequency spectral content on output voltage, visible as a low frequency ripple.

10.7.4 Line Transient and Feed-Forward

Most analog Bucks use a supply voltage feed-forward, which not only makes the loop gain independent of supply voltage, but also allows to almost reduce line transient (i.e. supply voltage variations) to zero. The classical implementation [1] consists in using a ramp generator with a gain proportional to inverse of input voltage.

Implementation of feed-forward in digital systems imposes more constraints: not only digital image of supply voltage is required, generally through an ADC, but the compensation loop gain has to be multiplied by the invert of this signal. A proposed solution [11] uses a look-up table to implement division as a multiplication, but more efficient techniques have probably to be proposed to improve feed-forward. On top of this problem, quantization of input voltage creates a less than ideal non-linear response to line transient which adds to voltage stack.

10.8 Auto-Tuning

Integrated IC suffer from large process variation effects on both passive and active devices, which make integrated analog control difficult to tune in all process corners, and gives an important advantage to digital implementation of filters (e.g. typically in a PID controller), which are not subject to process variations.

Another important advantage of embedded digital processing capabilities and ADC, which are required for digital control, it that it eases the auto-measurement

and auto-tuning methods, which have been a popular research subject, may it be for regulator performance [16, 17], or current sensor self-tuning. These techniques are somewhat adaptable to analog controllers, but in this case require dedicated logic and converters.

10.9 Multi-phases and Control Sharing

Maximum current loads requirements continue to rise in portable application, and a practical solution to keep with this current while keeping acceptable load transient and ripple without requiring a huge output capacitor consists in using multi-phase SMPS, where several coils in parallel are providing current to a single load (Fig. 10.11) [23]. In order to minimize ripple, the different phases are spread, and this allow for Digital SMPS which are using a unique time-multiplexed ADC to perform all conversions. If control calculation allow for it, the processing unit can also be shared between the phases.

The same ADC sharing technique can be used to share ADC and digital controller among several independent DC-DC converters, as long as their phases are spread, as shown on Fig. 10.12. The sharing can be extended to use the same ADC to sample output voltage and battery voltage [11], hence allowing further area savings.

Sharing techniques are unique to digital controlled SMPS and can provided consistent saving both in area of control part, as well as in power consumption.

An additional point in multi-phases SMPS is that a current-sharing external loop is necessary to balance current in all coils. This requires sensing and processing of very coil current, which can also be done in an analog or a digital way.

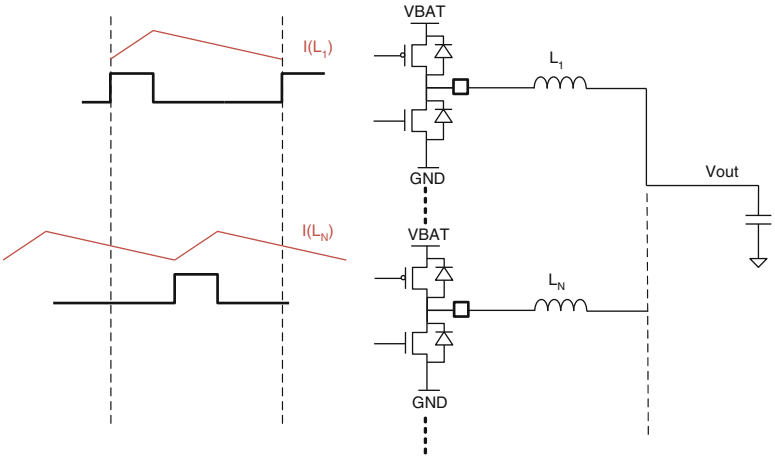

Fig. 10.11 Multi-phase power stage

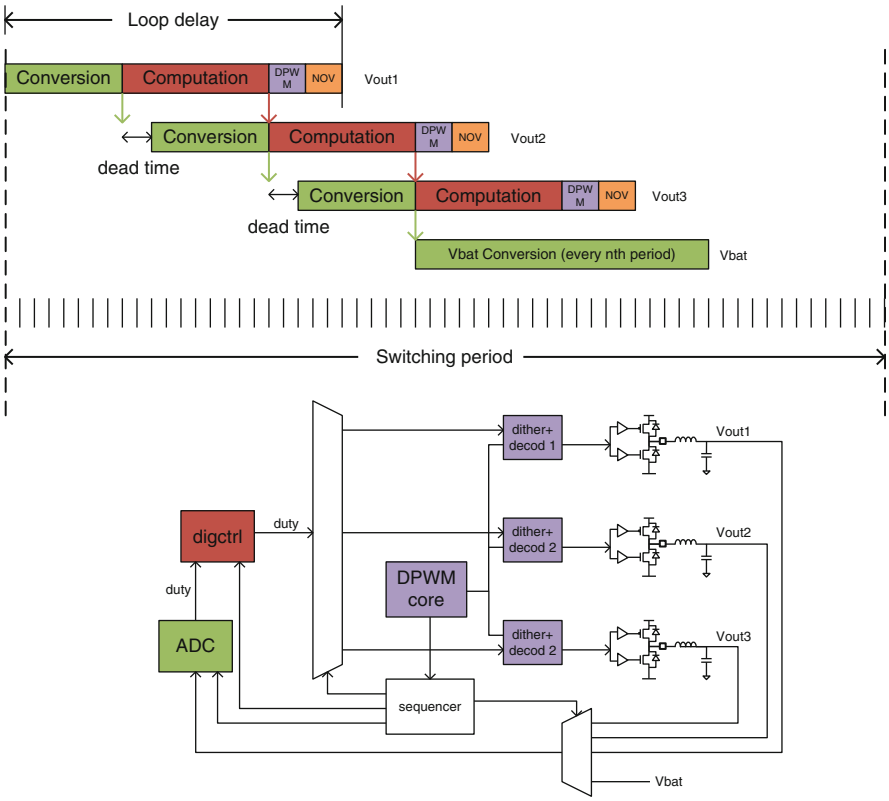

Fig. 10.12 Sharing single ADC and controller with several power stages

10.10 Voltage and Frequency Scaling

A common feature to regulators is ability to allow for Dynamic Voltage Scaling, allowing changing output voltage on the fly. This technique requires a filtering on reference in order to prevent destructive current in-rushes if reference voltage is changed abruptly. Including this as a digital filter inside digital control makes its somehow more flexible than adding an additional control part before a static DAC, which is the main option in analog structures.

Another technique consists in changing on the fly the switching frequency of SMPS at low currents in order to reduce the switching losses which become dominant in this area – at expense of slightly bigger ripple.

However, DPWM is not very flexible concerning frequency control: its resolution is generally frequency related – most architectures are not designed to support multiple switching frequencies. Yet, a digital DCM architecture proposed in [18] shows an efficient way of reducing the switching frequency, while keeping then *Ton* duration between *Vref*/*Vbat* and *Vref*/*Vbat*/*sqrt(2)*.

10.11 EMI Mitigation

Portable applications typically include cellphones where conducted and radiated noise due to switching power supplies can have a dramatic effect on RF part and should be minimized. On top of using expensive ferrites to isolate parts, some important EMI mitigation techniques are used both in analog and digital SMPS:

– Slope on power mosfet controls can be reduced so that current drawn on battery contains less high harmonics, at the expense of efficiency loss
– System clock can use some dithering so that some spectrum spreading occurs. But this technique should be used with care in digital SMPS, because a minimum clock period is generally required to sample and calculate next period duty-cycle.

Yet, the most efficient and programmable spectrum-spreading technique, i.e. random wrapped-around pulse-position modulation (RWAPPM) [19] can only be implemented easily on digital SMPS: while in analog systems duty-cycle value is unknown at the beginning of a conduction period, most DPWM system actually require that is this duty cycle is calculated before conduction period begins. This allows to simply implementing a RWAPPM scheme by randomly position the start of conduction pulse (Figs. 10.13 and 10.14).

10.12 A Conclusion on Analog Versus Digitally-Enabled Versus Digital SMPS

Table 10.1 summarizes the main differences between analog and digital SMPS (assuming that analog SMPS are developed in low-cost, older process, while digital SMPS take advantage of cutting edge digital process – no partitioning involved here). While Digital SMPS is a clear winner for flexibility – which however comes at cost of area and power consumption – for EMI reduction complex schemes and advanced sharing for complex structures, analog structures still keep an advance when pure transient performance is required, because the advances in control which have been reported for discrete medium-to-high power SMPS (up to kW range) are difficult to transpose to integrated high-speed, low-area SMPS.

One could wonder if, with such a picture, “digital SMPS” will ever become an option in integrated SMPS for portable applications.

Yet, digital SMPS is already there, even if not for main loop control: the many different modes, and controls, and calibration today require many, many more gates in an ‘analog’ SMPS. An example from a ST-Ericsson commercial analog SMPS is that the (analog) control part uses six times as many “digital” transistors than analog transistors! So integrated SMPS is already truly a mixed-signal system, which should be designed and architecture as such, and digital control loop will in the long run probably becoming an “option” for this complex system, when, for a given design requirement, its strong assets in configurability and flexibility will justify to sacrifice some of the transient performance.

Modulation Scheme		Peak Spectral Power (dBFS)	Ripple Noise (mV_{rms})#
PWM		0.4	0.9
RPPM		−1.0	1.6
RPWM		−2.0	115.1
RCFM-FD (δ= 15 %)		−16.1	0.9
RCFM-VD (δ= 15 %)		−16.2	39.3
PFM	(δ= 15 %, β= 20)	−12.9	2.1
	(δ= 15 %, β= 10)	−10.2	1.3
CFM	(δ= 5 %)	−16.4	1.0
	(δ= 15 %)	−21.1	1.1
	(δ= 30 %)	−24.2	1.1
Proposed RWAPPM		−26.6	2.0

Fig. 10.13 From [19], analytical peak spectral density and ripple noise of various modulation schemes

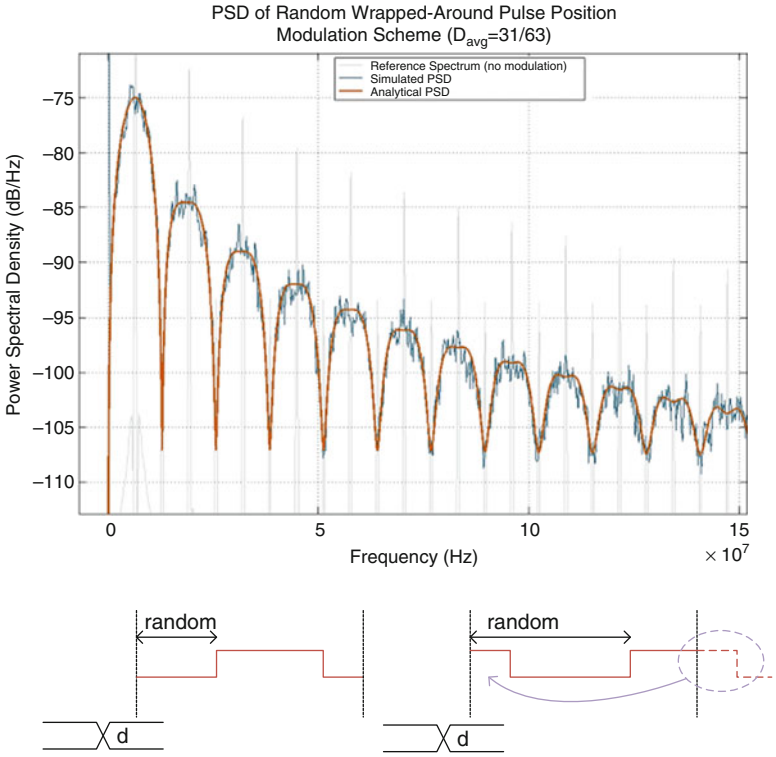

Fig. 10.14 Implemented RWAPPM scheme vs. simulation and theory

Table 10.1 Summary of analog versus digital SMPS

	(Fully) Analog SMPS	(Fully) Digital SMPS
Input voltage range	Low cost 5 V compliant process Low digital integration capability	High cost process. (40, 28 nm) 5 V capability through expensive options
Low profile components	Almost independent of the control type	Almost independent of the control type
Efficiency	Very competitive RDSon/Cg/Area 20 uA Iq achievable with simple PFM control	Cascoding increases design complexity. Transistor area almost equivalent. Requires integrated capacitors for decoupling
	35 uA Iq achievable with Pulse Skipping control	Very low quiescent possible
Fast transient	Current mode sensing can be done in pure passive way. Very simple and cheap	Voltage mode requires at least 1 ADC for feedback. Current mode requires additional sensitive system
Clock synchronization capability	Easy to medium (PLL for hysteretic control)	Easy
EMI	Basic	Easy implementation of complex modulation schemes
Flexibility	Possible (with digital): configurable compensation network, information exchange with digital requires extra ADC/DAC	Possible: parameterized algorithm. Requires additional hardware Possible to take benefit from processor activity status
Control sharing	Impossible	Possible (depending on controller bandwidth)
DVS and reference management	DAC for reference	No conversion required

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