FPGA-Based Single-Phase Photovoltaic Inverter Design

Bin Liang, Jun Shi, and Mingcheng Liu

Abstract Based XC3S500E FPGA chip as its control core, structuring SOPC system through embedding 32-bit MicroBlaze soft core processor, so that 1KW image acquisition system is implemented. Its main circuit topology consists of DC/DC push–pull converters, DC/AC full-bridge inverters and LC filters. Its sampling circuit consists of ADS1115 A/D converters and associated sensors, realizing the sampling of the PV arrays, DC/DC booster circuits, the voltage and current of inverter circuits. It completes the controller loop design, realizing the I^2C interfaces of A/D converters, the PWM generator controlled by MPPT, the SPWM generator controlled by PID and the interactive user interface. The results of the test show that the design of the inverter is reasonable and reliable, and meets the requirements of the power output. Not only its inversion efficiency can be up to 92 %, but also its power factor can be close to 1.

Keywords FPGA • SOPC • PV • Inverter

1 Introduction

In the global background, the environmental pollution is growing more seriously and the energy consumption is becoming more scarcely. The solar, a kind of large-scale developed and available clean energy, has been used widely in the form of photovoltaic power. The PV inverter is the core equipment of photovoltaic power, its performance directly determines the energy efficiency. This article puts forward the design of miniaturization PV inverter which is based on the SOPC system of FPGA chip.

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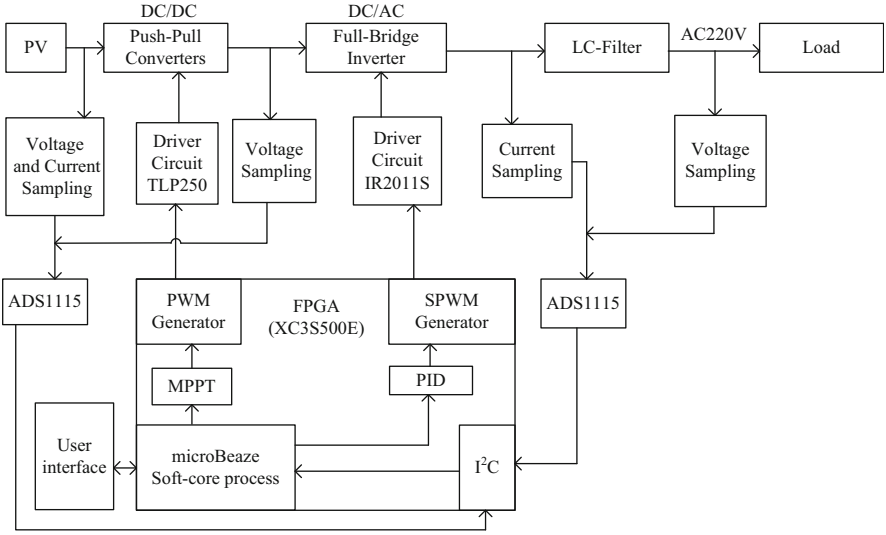

Fig. 1 System architecture diagram

2 Design of System

As Fig. 1 shown, it is the overall framework of the system. The main circuit of this design consists of DC/DC push–pull converter circuit, DC/AC full-bridge inverter circuit and LC filter circuit [1]. Its sampling circuit consists of ADS1115 A/D converters and associated sensors, realizing the sample of the PV arrays, DC/DC booster circuits, the voltage and current of inverter circuits. It completes the controller loop design, realizing the I2C interfaces of A/D converters, the PWM generator controlled by MPPT, the SPWM generator controlled by PID and the interactive user interface.

It's DC/DC push–pull converter circuit can raise the output voltage of the PV arrays to 400 V or so. FPGA takes sample of the voltage-current characteristics of PV and the voltage after rising separately by A/D converters. Also it uses MPPT algorithms to control the duty cycle of the push–pull converter circuit [2], so that it can regulate the maximum power output of the voltage finally. On the other hand, FPGA take sample of the output current of the full-bridge inverter circuit and the output voltage of LC filters by another ADS1115 chip, it uses PID algorithms to control the SPWM generator [3, 4, 5], so that it can realize the closed-loop control of full-bridge inverter circuit.

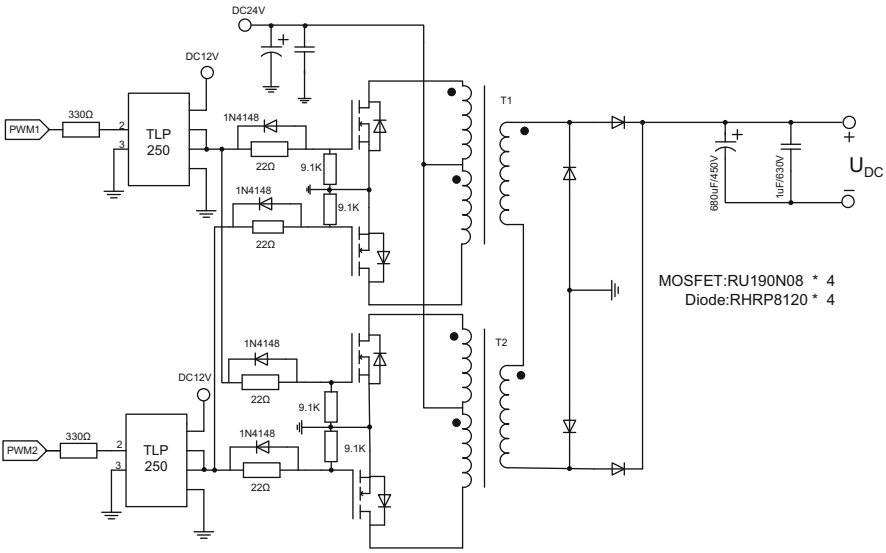

Fig. 2 Push–pull converter circuit schematics

3 The Design of Functional Circuit

3.1 Push–Pull Converter Circuit

Push–pull converter circuit is equivalent to a combination of two forward converter. Complementary work by turns, and two windings with a center tap at one side of the transformer work with each connection of the switch tube conduction by turns. It is particularly suitable for low input voltage DC / DC converter and can power up to 1KW or more.

In actual design, the circuit structure as shown in Fig. 2 is a combination of two sets of push–pull transform circuit. So that each transducer only need for the power of 500 W, which lower the index of volume of a transformer and requirements of the switch tube standards effectively. The transformer choose two EC49 core winding, which are primary parallel and secondary series, and their power is 500 W. The switch tube choose MOSFET and models for RU190N08 with the characteristics of withstand voltage 80 V and maximum current 190A. The switching diode choose RHRP8120 whose reverse voltage is 1,200 V and working current is 8A.

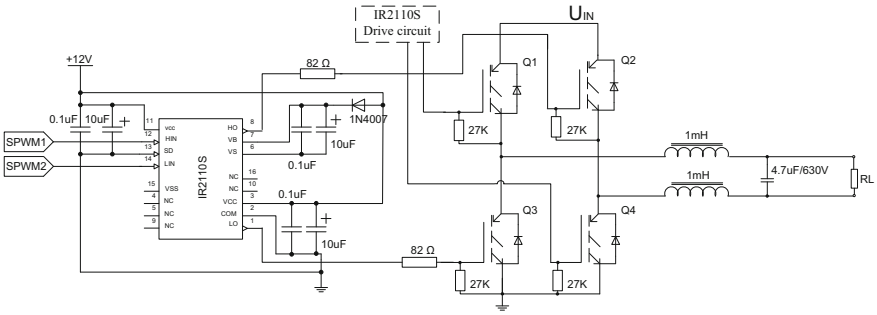

Fig. 3 Full-bridge inverter circuit schematics

3.2 *Full Bridge Inverter Circuit*

Full bridge inverter circuit is shown in Fig. 3,the SPWM1 and SPWM2 driving signal control the power switch Q4, Q1 and the open and shut off of the Q2, Q3 respectively. When the Q4 and Q1 is on and the Q2 and Q3 is off, the voltage of the load on both ends is +UIN. When the Q2 and Q3 is on and the Q4 and Q1 is off, the voltage of the load on both ends is -UIN. The Q1–Q4 as the power switch tube of IGBT, choose GW39NC60VD model. Its withstand voltage is 600 V, maximum current is 40A and the collector to emitter saturation voltage is 1.8 V. Driving circuit with the bootstrap floating power supply selects two IR2110S half bridge driver chips, in which the driving current is 2A.

3.3 *Sampling Circuit*

As is shown in the Fig. 4, the core of sampling circuit adopts two slices of interconnected Analog-digital Converter called ADS1115 based on I^2C-bus. It's a high-speed 16-bit converter, integrated an internal reference voltage source, and can achieve single-ended and difference sampling. It disposes the Voltage and Current Signal converted in the sampling and quantitative main circuit.

The voltage and current signal outputed from PV Cell Array is cut down by Resistance Voltage-division network, and gets converted when flowing through Hall Current Sensor SW4T50C50V6. Just as the output of PV Cell Array, the output voltage of Push–Pull Converter is reduced by Resistance Voltage-division network, and then, enters ADC. The output current of Inverter gets converted through Hall Current Sensor ACS712-30A. Voltage Mutual Inductor takes sample of the output AV filtered via LC Filter, and after this, the signal will flow into ADC.

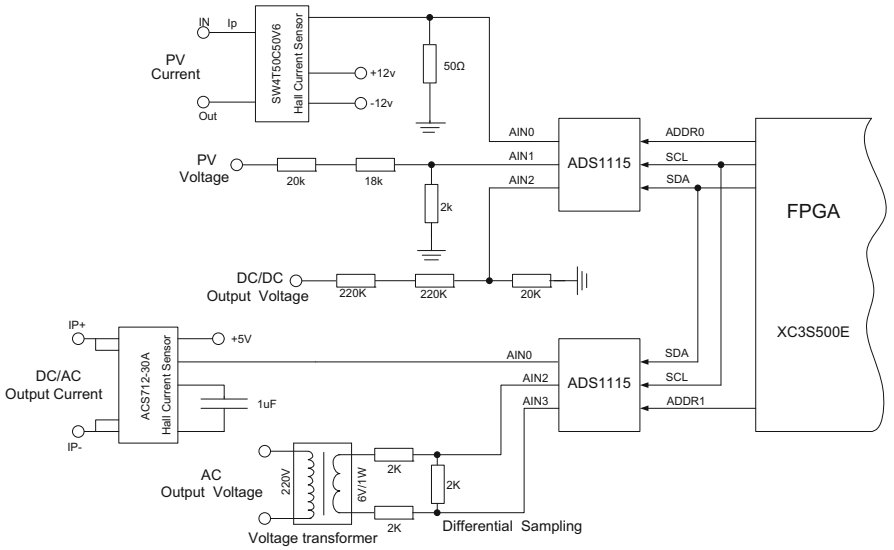

Fig. 4 Sampling circuit schematics

Table 1 With load power test data

Number	Load	Input vottage (v)	Input current (A)	Power input (W)	Bus vottage (V)	Bus current (A)	Power output (W)	Efficiency %
1	100 Ω	24.5	13.4	330.7	369	0.86	318.3	96.3
2	200 Ω	24.4	27.1	660.8	362	1.74	629.4	96.2
3	300 Ω	24.3	40.7	988.2	350	2.63	918.8	93
4	400 Ω	24.3	52.4	1,272.4	339	3.44	1,165.2	91.6

4 Testing Data

In the testing process, it takes use of resistive load to complete the test of power ranged from 300 W to 1KW, and the testing data is depicted in the Table 1. It shows that Inverter works steadily, and that its efficiency is expected to 96 % under the circumstances of low load, to 91 % in a full load condition, which matches the design's requirements.

5 Conclusion

This article takes XC3S500E FPGA chips as the core, embeds 32-bit MicroBlaze soft core processor in it, structures SOPC system, and implements 1KW image acquisition system. It introduces hardware circuit architecture, the working

principles and parts selection of the inverter system. It shows the associated experiments results and data through the practical operation and test. The inverters' efficiency can be up to 92 %, and the power factor can be close to 1. Not only its harmonic content of the inverters is low, but also it has the function of over-current and under-voltage protection.

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