Chapter 9
Transparent Amorphous Oxide Semiconductor TFTs

Abstract Transparent amorphous oxide semiconductors, especially a-InGaZnO, are the most recent TFT materials of interest for driving active matrix displays. The high level of activity on these devices is because, even though the material is amorphous, it can offer a carrier mobility of 10 cm^2/Vs, or more. This is 10–20 times greater than a-Si:H, and the higher mobility is advantageous for driving organic light emitting diode, OLED, displays. Also, due to the amorphous nature of the material, it may have better uniformity than poly-Si, which is the currently preferred TFT technology for commercial, hand-held AMOLED displays. In this chapter, the material and electronic properties of AOS materials are reviewed, paying particular attention to a-InGaZnO TFTs. Other topics include device architecture and fabrication, the DOS and conduction mechanisms within the material, overall device performance, and bias stability issues.

9.1 Introduction

The current interest in transparent amorphous oxide semiconductor, AOS, TFTs was stimulated by the publication, in 2004, of the operation of amorphous indium-gallium-zinc oxide, a-IGZO, TFTs on low temperature, flexible, polymer substrates [1]. Since that time, the work in the AOS area has rapidly developed, with a-IGZO TFT addressed active matrix displays being demonstrated for LCDs [2], OLEDs [3], and electrophoretic e-readers [4]. This interest is due to the particular properties of AOS TFTs, which make them well suited to the FPD application. Firstly, this amorphous material has Hall-effect and field-effect electron mobilities of $\sim$10 cm^2/Vs, or more, which is >10 times higher than a-Si:H [5]. This makes the material more appropriate than a-Si:H for driving AMOLED displays, and it is even relevant for addressing 120 Hz, high resolution AMLCDs, where a carrier mobility of $\sim$2 cm^2/Vs is required for display diagonals >90 inches [5, 6]. Indeed, the mass-production of large size, high resolution AMLCD TVs with AOS pixel TFTs has been forecast to begin in 2012 [7]. In addition, its amorphous nature should mean that it will have better uniformity than poly-crystalline

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materials [5]. Hence, there is interest in AOS TFTs for large diagonal AMOLED TVs, where poly-Si (which is presently used in small diagonal AMOLED displays) is perceived to be too non-uniform for this application [3]. However, this argument is not yet proven, and, as discussed in Sect. 7.2.2.4, advanced crystallisation techniques have improved the uniformity of laser crystallised poly-Si [8].

In addition to the higher electron mobility compared with a-Si:H, a-IGZO TFTs also have a better overall performance, with state-of-the-art devices having a sub-threshold slope of 0.12 V/dec [10], compared with 0.4 V/dec in a high quality a-Si:H TFT [11]. Both these mobility and sub-threshold slope differences are indicative of a lower density of trapping states near the conduction band edge in a-IGZO [5].

From a device fabrication point of view, the material can be deposited by sputtering at temperatures down to room temperature, and a further attractive feature of a-IGZO TFTs is that they can be fabricated with a simple contact metallisation scheme, without doped contacts, and a wide range of gate dielectrics have given acceptable performance [5].

These features of AOS TFTs are discussed in the following sections, starting with the background material properties in Sect. 9.2, and the device architecture and fabrication processes in Sect. 9.3. Device performance, including the DOS assessment, series resistance, and bias stability effects, are discussed in Sect. 9.4. Finally, the issues of complementary p-channel TFTs, and driver circuit integration in demonstrator displays are briefly reviewed in Sect. 9.5.

9.2 Material Properties

One of the key features of the AOS materials is their large carrier mobility, even in the amorphous state, where the mobility may be 50 % or more of the crystalline mobility. This is very different from the a-Si:H/c-Si comparison, and the key to understanding this difference lies in the difference between the covalent bonding of Si and the ionic bonding of the AOS materials [5]. As discussed in Sect. 6.2, the conduction and valence bands of Si are formed from hybridised sp^3 states, and, in the amorphous Si network, strained and broken Si–Si bonds lead to localised band tail states and deep gap states, respectively. The band tail states reduce the field effect mobility by >10 times, compared with the band mobility, which itself is very low due to the carrier scattering distance in the extended states being of the order of the inter-atomic spacing. In the ionic bonding configuration of AOS materials, due to charge exchange between the metal cation and the oxide anion (in, for instance, ZnO), the outer s-states of the metal ion are empty, and the outer p-states of the oxygen ion are filled. The charge exchange results in a Madelung potential, which separates the metal and oxygen ion orbitals, with the empty s-states of the metal cation predominantly forming the conduction band minimum, and the filled p-states of the oxygen anion mainly forming the valence band

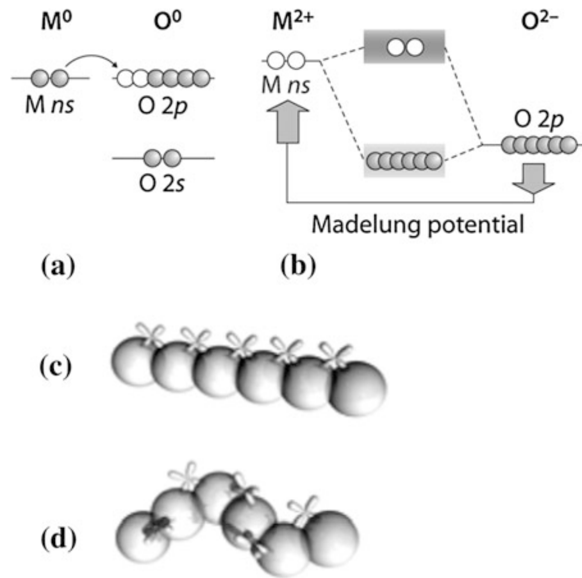


Fig. 9.1 Schematic diagram of (**a**) charge transfer and (**b**) band gap formation process in an ionic oxide semiconductor. Molecular orbital representation of the conduction band bottom, showing carrier conduction pathways in (**c**) crystalline and (**d**) amorphous oxide semiconductor (**a** and **b**: Reprinted by permission from Macmillan Publishers Ltd: NPG Asia Materials [5], copyright (2010); **c** and **d**: Reprinted from [12] with permission of IEEE)

maximum, as shown in Fig. 9.1a, b [5, 12]. The separation between these band edges was ~3 eV in the original pulsed laser deposited a-IGZO material [1] (giving these amorphous oxide materials their optical transparency), although more recent, sputter deposited a-IGZO layers have given Tauc optical gaps up to 3.7 eV [13]. For metal oxides, the spatial spread of the spherically symmetric metal s-state orbital is determined by the principal quantum number, n, of the metal ion [14]. For post-transition metals with $n \geq 5$, such as In, Ga and Sn, it is sufficiently large that there is an overlap between adjacent cations, as shown in Fig. 9.1c [12]. This leads to small electron effective masses and high electron mobilities, as found, for instance, in the transparent conducting oxide ITO. The illustration in Fig. 9.1c shows the s-state overlap for a crystalline lattice, and this overlap is still maintained in the disordered amorphous structure shown in Fig. 9.1d. Hence, these spatially extensive s-state orbitals, in the post-transition metal oxides, explain the relatively high carrier mobilities found in the transparent amorphous oxide semiconductors [5, 12].

The AOS material can be doped, but, due to the flexibility of the ionic bond, this is not achieved by introducing different valence atoms (as is standard with group IV semiconductors), but most commonly occurs via the oxygen vacancy. The vacancy results in a non-bonded metal cation producing a shallow donor level [5]. The vacancy concentration is determined by the oxygen partial pressure during deposition, and, for a low partial pressure, the interrelationship between the composition of the ternary structure In_2O_3-Ga_2O_3-ZnO, the Hall mobility and the as-grown doping level is shown in Fig. 9.2a [5]. Over most of this compositional space, the material is amorphous, although it tends to be crystalline within ~10 % of either pure ZnO or pure In_2O_3. However, as will be seen along the base of the triangle, this structural difference had little effect upon the Hall mobility, whereas increasing the

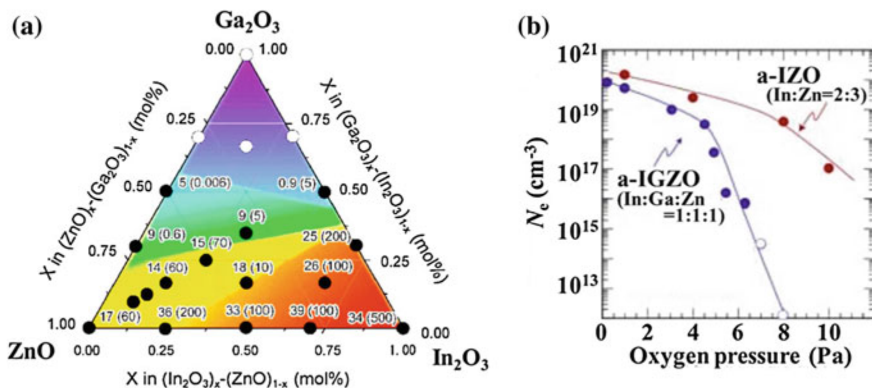


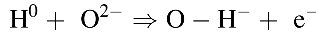
Fig. 9.2 **a** Compositional dependence of Hall effect mobility and free carrier density (in parentheses, with units of 10^{18} cm^{-3}) in the In_2O_3-Ga_2O_3-ZnO system, and **b** dependence of free carrier density on the O_2 partial pressure during deposition of a-IGZO and a-IZO films. (Reprinted from [12] with permission of IEEE)

Ga content reduced both the mobility and the free carrier density. A low free carrier density is required in TFT material to ensure a low off-current, and Ga plays an important role in this respect, because its strong Ga-O bond reduces the O-vacancy density [5]. In addition, the free carrier concentration can be further reduced by increasing the oxygen partial pressure during deposition, as shown in Fig. 9.2b. This also compares a-IGZO with IZO, and demonstrates the importance of Ga incorporation in the material [12]. For this reason, $InGaZnO_4$ (IGZO) is the preferred composition for TFTs, even though it is not the highest mobility material [12].

The oxygen vacancy has been referred to as forming a shallow donor level in IGZO material; however, the vacancy is a negative U-centre, with the fully occupied, neutral level in the lower half of the band-gap [5, 15]. This level occurs within a relatively un-relaxed, 'stoichiometric' lattice, whereas the formation of the charged centre is accompanied by an inward relaxation of the metal ions around the oxygen vacancy location [15, 16]. Given the lattice relaxation necessary to form the ionised donor level, it is more likely to be formed during film growth (under low oxygen partial pressure) [15, 16], although an increased free carrier density has also been found in material subjected to prolonged vacuum exposure [17]. This was attributed to donor formation by effusion of oxygen from the material, and the process was reversible by re-exposing the sample to an oxygen ambient. Both types of oxygen vacancy may be found in a-IGZO films, and the instability caused by negative bias illumination stress, NBIS, discussed in Sect. 9.4.3.2, is believed to be due to photo-ionisation of the deep lying neutral oxygen vacancy [18]. More work is currently required for a fuller understanding of NBIS, and of the conditions determining the relative concentrations of neutral and ionised oxygen vacancies in as-prepared thin films of a-IGZO.

Low temperature annealing in a H_2-N_2 gas mixture has also been found to increase the free electron concentration in a-IGZO [12], and calculations of the electronic properties of various point defects in c-IGZO have shown that

interstitial hydrogen bonds to an oxygen ion, forming a donor level above the conduction band edge [19]. A similar interaction has been found from bonding calculations in a-IGZO [12], with H always forming an O–H bond. It is suggested that the donor activity results from the following reaction [12]:



$$H^0 + O^{2-} \Rightarrow O - H^- + e^-$$

This reaction is believed to underlie the susceptibility of unpassivated a-IGZO TFTs to ambient moisture effects, in which water immersion [20] shifted the TFT threshold voltage in a negative direction. As with the vacuum/oxygen exposure results discussed above, the effect of water immersion was also reversible, in this case by baking the sample in vacuum to break the O–H bonds and to effuse the water molecules [20].

Finally, the Hall mobility was found to increase with increasing carrier density, and was attributed to percolation limited transport around potential barriers within the conduction band [12, 21]. A schematic illustration of the a-IGZO density of states, DOS, is shown in Fig. 9.3, and includes the percolation barriers, which are indicated by their average height, E_{center}, and distribution, ΔE. Also shown in this figure is the location of the shallow donor levels, and a low density band-tail at the conduction band edge. As the valence band edge is composed of p-type states, these do not have the overlapping orbitals of the conduction band states, and there is a large density of localised states, as well as deep states above the valence band mobility edge [12], which inhibit useful p-channel TFT behaviour. The a-IGZO DOS and electron conduction mechanisms are discussed further in Sect. 9.4.2.

9.3 TFT Architecture and Fabrication

Unlike a-Si:H and poly-Si TFTs, AOS TFT technology is still developing, and there is not an established process around which a consensus has emerged,

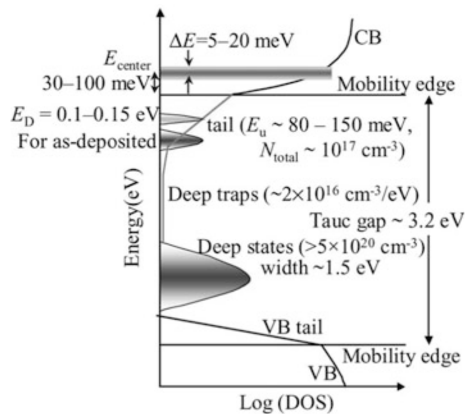


Fig. 9.3 Illustrative a-IGZO density of states distribution, DOS, showing band edges, band-gap states and distribution of percolation potentials in the conduction band. (Reprinted from [12] with permission of IEEE)

leading to a well-defined manufacturing technology. However, there are clearly emerging trends, and these are reviewed below, with a particular focus on the TFT architecture and processes used to fabricate high quality demonstration displays [2, 3, 6, 13].

9.3.1 Architecture

Although the original demonstration a-IGZO TFT was a top-gated, coplanar structure [1], the presently preferred configuration for demonstration displays is bottom gated, with either staggered [3, 13, 22] or coplanar [2, 23] source and drain electrodes, as illustrated in Fig. 9.4a and b, respectively [3, 23]. The inverted staggered structure is more widely used, but, predominantly, with the etch–stop configuration shown in Fig. 9.4a [3]. The two principal inverted staggered TFT architectures, of back-channel etched (BCE) and etch-stop (ES), were discussed in Sect. 5.3, in the context of a-Si:H TFTs, where it was shown that the BCE architecture was preferred for mass production. However, for the a-IGZO TFTs, the preference is for the ES architecture because of the sensitivity of the back channel to ambient effects, and also to damage and donor formation during the deposition and etching of the source and drain metals [24]. This was demonstrated in a direct comparison of BCE and ES TFTs, in which the ES TFTs had an SiO_x etch-stop layer deposited by PECVD, and both device types had sputter deposited and dry etched MoW source and drain metals. With a 200 nm thick PECVD SiN_x gate dielectric, the sub-threshold slopes and electron mobilities of the BCE and ES TFTs were 3.5 V/dec and 0.59 V/dec, and 5.0 cm^2/Vs and 35.8 cm^2/Vs, respectively [24]. Hence, the damage to the unprotected back surface of the a-IGZO film in the BCE TFT resulted in almost an order of magnitude degradation in device performance. The choice of ES layer was also crucial in obtaining high performance. For a-Si:H TFTs, a-SiN_x:H is usually used in the ES structure, but, when PECVD SiN_x was used in the a-IGZO TFTs, the gate modulation of the channel current was lost, and the devices became simple resistors due to a large free carrier concentration of $\sim 4 \times 10^{19}$ cm^{-3} in the material [24]. This was attributed to hydrogen entering the a-IGZO film from the SiN_x layer, and either acting as a donor [25], or reducing the a-IGZO and introducing oxygen donor vacancies. To avoid these effects, SiO_x is the preferred ES/passivation layer in many publications [2, 3, 13, 22–24], with some groups evaluating both PECVD and sputter deposition, given the latter's lower H-content [26]. The SiO_x has also been used as the uppermost film in a double layer passivation process [13, 22], with an alternative material placed in direct contact with the back face of the a-IGZO. For instance, a DC sputter deposited layer of Al_2O_3 gave excellent bias stability results, as well as good passivation [22]. In another case, the lower film of Ti, from a sputtered double layer of Ti and Mo for the source/drain metallisation, was exposed to an oxygen plasma to convert it to an insulating TiO_x passivation layer, as depicted in Fig. 9.5 [13]. After the definition of the metallisation pattern, a final capping layer

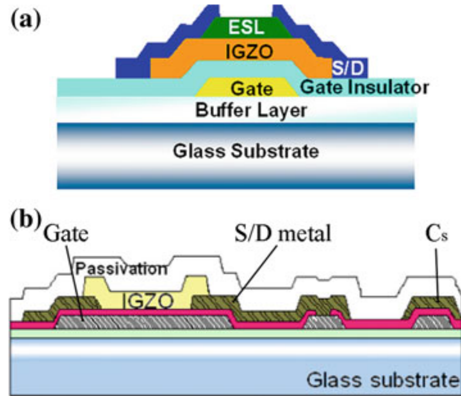


Fig. 9.4 Cross-sections of a-IGZO TFT structures **a** inverted staggered etch-stop (Reprinted from [3] with permission of SID), and **b** inverted coplanar (Reprinted with permission from [23]. Copyright (2010) The Japan Society of Applied Physics)

of PECVD SiO_x was added to this structure. This approach had the additional benefit of a reduced number of deposition stages, as the passivation layer was directly formed from the source/drain metallisation.

As discussed in Sect. 5.3, the inverted staggered, rather than the inverted coplanar structure, is exclusively used with a-Si:H TFTs in order to position the n^+ layer on the top of the device stack, so that it could be selectively etched to form the source and drain contact regions during final patterning. As doped contact regions have not been routinely implemented with the a-IGZO TFTs, this constraint is removed, and the source and drain metal regions, in the coplanar structure, can be deposited, and defined, before the deposition of the a-IGZO layer itself, as illustrated in Fig. 9.4b [23]. This architecture also has the advantage that the a-IGZO layer is not exposed to the deposition and etching processes required for the source/drain metallisation, and requires one less mask than the ES process [6], as discussed further in Sect. 9.3.2.4. However, the structure still incorporated a SiO_x passivation film on top of the completed device structure [6, 23], in order to protect it against moisture in the ambient, and from damage during subsequent display processing.

In addition to these conventional architectures, there is interest in self-aligned structures to reduce the overlap capacitance in pixel TFTs, and also as a route to future channel length reduction [27, 28]. A bottom gated self-aligned structure has been demonstrated, in which the transparency of the a-IGZO layer has been exploited to use the bottom gate as a UV exposure mask for the definition of the etch-stop layer by back-face illumination [27]. This process reduced the total mask

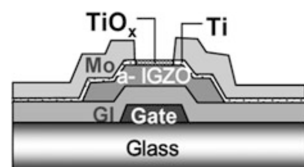


Fig. 9.5 Cross section of inverted staggered etch-stop TFT, showing the local conversion of Ti source/drain metal to a TiO_x passivation/ ES layer. (Reprinted from [13] with permission of SID)

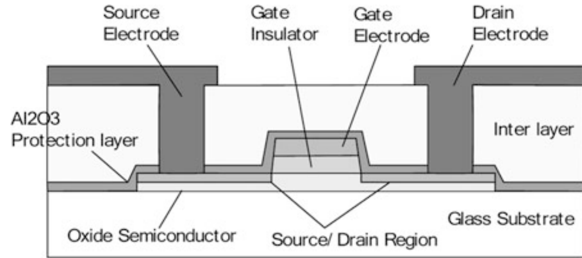


Fig. 9.6 Cross-section of a self-aligned top-gated TFT. (Reprinted from [28] with permission of SID)

count for the ES process by one, as well as reducing the gate/drain overlap to 2μm. A more novel process has been used to produce the self-aligned top-gated TFT, shown in Fig. 9.6 [28], in which the total overlap of the gate and source/drain regions was reduced to 0.8 μm or less. This structure incorporated low resistance contacts to the a-IGZO layer, which were self-aligned to the gate. In order to form them, after the definition of the gate electrode and the removal of the gate dielectric around it, the structure was coated in a thin film of Al, and annealed at 300 °C in oxygen. During this process, the lower surface of the Al reacted with the a-IGZO to form a low resistance contact, whilst the upper surface of the Al was oxidised to form an insulating layer of Al_2O_3. The self-aligned, low resistance source and drain regions were contacted by the top metallisation pattern through windows in the interlayer dielectric. TFTs with a minimum channel length of 4 μm were fabricated by this process, and high quality transfer characteristics, as well as good gate bias stability, were reported [28].

9.3.2 *Fabrication Processes*

9.3.2.1 a-IGZO Layer

The active a-IGZO layer is typically $\sim$30−60 nm thick in the FPD demonstrator TFTs, and is usually deposited at room temperature by DC sputtering [2, 3, 6, 13, 26]. The sputter targets had a compositional ratio of In_2O_3:Ga_2O_3:ZnO in the range 1:1:0.5 to 1:1:1, and the sputtering gas was an Ar/O_2 mixture. Whilst other techniques, including pulsed laser deposition [1] and RF sputtering [24], have also been used, the advantages of DC magnetron sputtering are that it is widely used for ITO deposition in AMLCDs [29], and the equipment is readily available for large area depositions.

9.3.2.2 Gate Dielectric

In the demonstration displays, the gate dielectric was 200 nm thick, and was most commonly SiO_x deposited by PECVD [3, 6, 22], although in some cases PECVD

SiN_x [30] and SiO_xN_y [23] were also used. Where SiN_x was used, there was no apparent effect on threshold voltage, in spite of the high density of positive charge which is customarily found in a-SiN_x:H layers. A fuller discussion of the PECVD deposition of a-SiN_x:H and SiO_x layers can be found in Sects. 5.5.3 and 7.3.1, respectively.

In view of the bottom gate structure, and the absence of Fermi level dependent meta-stability effects (such as seen in a-Si:H), the particular gate dielectric and its deposition procedure have, in principle, little impact upon the subsequently deposited a-IGZO layers, thereby affording a broad choice of gate dielectric. This is apparent from the successful use of a-SiN_x:H, SiO_x and SiO_xN_y as cited above; however, these high quality PECVD dielectrics require a deposition temperature of $\sim$300 °C, or higher, and are more suited to glass than flexible, polymer substrates. Indeed, the original paper reporting a-IGZO TFTs on low temperature, flexible PET films used room temperature deposition of Y_2O_3 as the gate dielectric [1]. Hence, there is continuing interest in alternative gate dielectrics, and in reduced deposition temperatures compared with conventional PECVD depositions. As part of this broad investigation, a range of low temperature, high-k dielectrics has been examined, in which it is agued that the high dielectric constant can compensate for a poorer interface compared with the higher quality PECVD films [31]. Amongst the dielectrics examined have been Ta_2O_5 (k = 29) [32], ZrO_2 (k = 25) [33] and HfLaO (k = 25) [34], all of which were deposited by room temperature sputtering, with a film thickness in the range 200−300 nm (i.e. comparable to the PECVD dielectrics). However, only HfLaO gave a notably low value of sub-threshold slope, S, of 0.076 V/dec, whereas Ta_2O_5 and ZrO_2 were $\sim$0.6 V/dec (compared with 0.29 V/dec for a PECVD SiO_x dielectric [3]), suggesting that these two high-k dielectrics were, indeed, producing a poor quality interface. In addition, the TFT with a Ta_20_5 dielectric had a high gate leakage current, and a channel current on:off ratio of 10^5, compared with $> 10^8$ in the SiO_x device [3]. The other two dielectrics had on:off ratios of 1-5$\times 10^7$, and the particularly low value for Ta_2O_5 [31, 32] has been attributed to its small band gap, and small conduction band offset with respect to the a-IGZO layer [31, 35]. A compromise approach has been a room temperature sputtered composite high-k and SiO_2 dielectric, such as Ta_2O_5–SiO_2, and HfO_2-SiO_2, or even a tri-layer stack of SiO_2/HfO_2-SiO_2/SiO_2, leading, in the first case, to an improved on:off ratio of 3×10^6, and 2×10^7 for the triple stack [31].

From the above discussion, it is clear that there is on-going research to identify the optimum gate dielectric for AOS TFT fabrication on low temperature, flexible substrates. In addition to the impact of the gate dielectric layer on the static TFT characteristics, it also needs to be evaluated in terms of the bias stability of the device, and this topic is reviewed in Sect. 9.4.3.

9.3.2.3 Post Deposition Annealing

Post-deposition annealing of the a-IGZO TFT structure is commonly used, and it has been shown to lead to a major improvement in device performance and uniformity [10]. In that study, the effects of 400 °C annealing, in dry and wet oxygen, were investigated using inverted staggered TFTs fabricated on thermally oxidised n^+ silicon substrates, and the a-IGZO layers were produced by pulsed laser deposition at two different oxygen partial pressures. This difference in deposition conditions led to threshold voltage differences of 6 V, as shown by the transfer characteristics in Fig. 9.7a. However, the dry annealing removed this difference, and gave a common threshold voltage of ~ -1 V, and a reduction in S values from 0.4–0.5 V/dec to a common value of $\sim$0.25 V/dec [10]. Wet oxygen annealing had a similar effect, in terms of removing the built-in differences due to different oxygen partial pressures during deposition, and the overall effect was a function of the water partial pressure, as shown in Fig. 9.7b. At the optimum water partial pressure of $\sim$20 %, the wet annealing was more effective than the dry annealing, and normalised the threshold voltage to $\sim$1 V and S to $\sim$0.12 V/dec [10]. In addition, both dry and wet annealing improved the overall uniformity of a given set of TFTs, and, once again, the wet annealing was the most effective in this respect. Hence, the post-deposition annealing of a-IGZO, especially in a wet

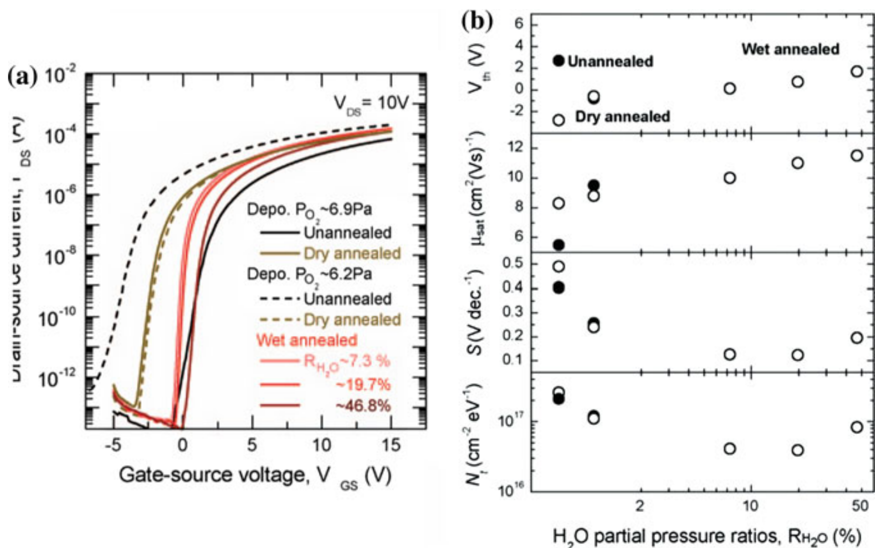


Fig. 9.7 **a** The influence of deposition partial pressure of O_2, and post-deposition annealing on TFT transfer characteristics, and **b** effect of water partial pressure during post-deposition annealing on TFT parameters {open (closed) circles 6.2 Pa (6.9 Pa) O_2 partial pressure during deposition}. (Reprinted with permission from [10]. Copyright (2008) American Institute of Physics)

oxygen ambient, improved device performance, and uniformity, and reduced the dependence of the device characteristics on the initial layer deposition conditions.

To stabilise the a-IGZO film, post-deposition annealing is routinely applied to the TFTs used for demonstrator displays [3, 6, 13, 22, 23], and is typically 1–2 h in the temperature range 250–350 °C, although the ambient is rarely specified.

9.3.2.4 Metallisation

The choice of gate and source/drain metals is determined by considerations of line resistance, processability (to include deposition by sputtering), and experience within the LCD industry. Accordingly, in some instances, Mo [3, 22] or Ti/Mo [13] has been used for the metallisation in inverted staggered devices, and, as discussed in Sect. 9.3.1, the Mo was etched away over the channel region, in the latter case, to selectively expose Ti to an oxygen plasma, which formed a dual-purpose TiO_x passivation and etch-stop layer [13].

A combined Ti/Al/Ti layer was used in some inverted coplanar TFT structures [23], and, as a consequence of the a-IGZO post-deposition anneal, the Ti reduced the a-IGZO adjacent to it to produce a layer of electron-rich, high conductivity material, thereby reducing the contact resistance between the metallisation and the channel [23].

9.3.2.5 Process Flow

The 4-mask process flow for the inverted coplanar TFT is shown in Fig. 9.8 [6], in which the mask definition stages are the definition of the gate metal (M1), the

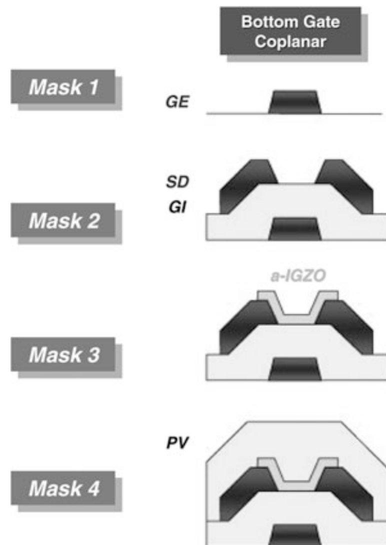


Fig. 9.8 Inverted coplanar TFT process flow. (Reprinted with permission from [6]. Copyright (2011) The Japan Society of Applied Physics)

source/drain metal (M2), the a-IGZO layer (M3) and the contact holes (M4) through the top passivation layer (not shown). For the inverted staggered etch-stop TFT, shown in Fig. 9.4a, the comparable stages are deposition and definition (M1) of the gate metal, deposition of the gate dielectric, deposition of the a-IGZO and etch-stop layers, definition of the etch-stop pad (M2), definition of the a-IGZO layer (M3), deposition and definition of the source/drain metallisation (M4), and deposition of the final capping/passivation layer and contact window opening (M5). Hence, the inverted staggered ES architecture requires one more mask than the inverted coplanar process.

9.4 a-IGZO TFT Performance

9.4.1 n-Channel Characteristics

The transfer characteristics of a high quality, inverted staggered etch-stop a-IGZO TFT, with W = 25 μm and L = 10 μm, are shown in Fig. 9.9a. This device, with a 200 nm thick SiO_x PECVD gate dielectric, had a field effect mobility of 21 cm^2/Vs, a sub-threshold slope of 0.29 V/dec and an on:off ratio of $>10^8$ [3]. Typical output characteristics [12], of an a-IGZO TFT with a saturation mobility of 11.8 cm^2/Vs, are shown in Fig. 9.9b, and the device displayed good current saturation at large V_D, and an absence of current crowding at low V_D.

However, even though current crowding is not an issue in high quality a-IGZO TFTs, the absence of a doped contact to the material has led to the investigation of series resistance effects in these devices [36–38], and its impact upon the field effect mobility as channel length is reduced [24]. If an ohmic resistance, R_s and R_d,

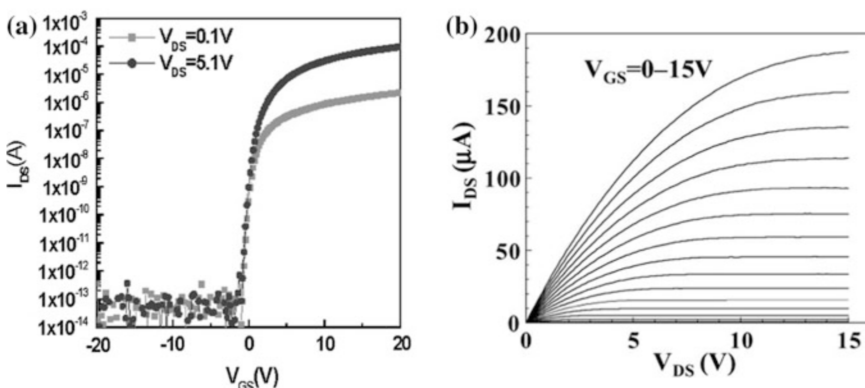


Fig. 9.9 High quality a-IGZO TFT characteristics (**a**) transfer characteristic of ES TFT (Reprinted from [3] with permission of SID, and (**b**) output characteristics (Reprinted from [12] with permission of IEEE)

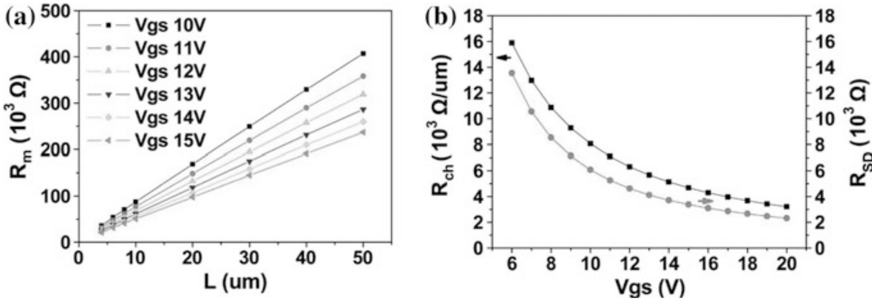


Fig. 9.10 **a** Total TFT resistance measured as a function of L and V_G, and **b** variation of channel resistance, R_{ch}, and series resistance, R_{SD}, with V_G. (Reprinted from [36] with permission of IEEE)

is present at the source and drain terminals, respectively, then the total measured device resistance, R_m, is

$$R_m = R_{ch} + R_s + R_d = R_{ch} + R_{SD} \tag{9.1}$$

where $R_{SD} = R_s + R_d$, and the channel resistance, R_{ch}, in the linear regime, can be obtained from Eq. 3.11 as:

$$R_{ch} = \frac{L}{\mu_n W C_i (V_G - V_T)} \tag{9.2}$$

Hence, for gate-bias-independent R_{SD}, a plot of R_m vs L, for any value of $V_G - V_T$, will give R_{SD} where the line intersects the R_m axis, and its slope will give the channel resistance per unit length at that gate voltage. An example of this measurement is shown for BCE inverted staggered a-IGZO TFTs in Fig. 9.10a, and the two extracted resistance parameters are shown in Fig. 9.10b [36]. There was not a common intersection point of the data sets, and the measurement yielded an approximate evaluation of the series resistance, R_{SD}, which was gate-bias-dependent. The background, and limitations, to this measurement procedure are briefly discussed below.

This resistance technique was originally developed for MOSFETs, and, with different values of $V_G - V_T$, it was found that the individual lines may have a common intersection point at a positive value of L, ΔL, rather than at L = 0 [39]. This was interpreted as channel shortening during processing, such that the effective channel length, L_{eff}, differed from the mask value by ΔL, and the value of R_{SD} was taken at this common intersection point (and not on the R_m axis). The technique has also been used with a-Si:H inverted staggered ES TFTs [40, 41], where a common intersection point was found at negative values of L, indicating an increase in the effective channel length due to current collection spreading along the n^+ doped regions. Using the above procedure, the identification of the common intersection point, and the related evaluation of the effective channel length, relies upon the series resistance being independent of gate bias, whereas,

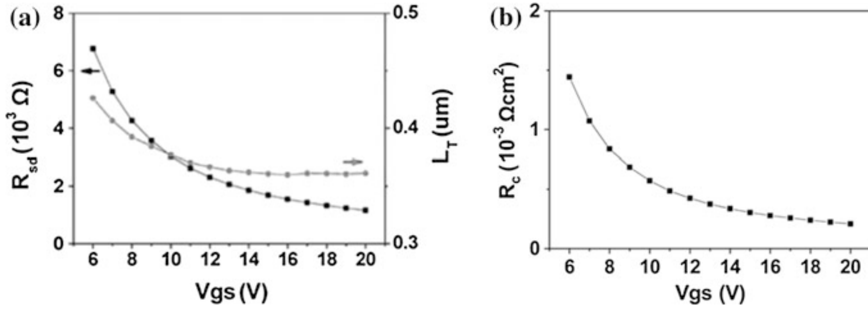


Fig. 9.11 Gate bias dependence of (**a**) change in effective channel length, L_T, and (**b**) specific resistivity of source and drain contacts (Reprinted from [36] with permission of IEEE)

for the a-IGZO TFTs in Fig. 9.10 this was not the case. A modified version of the common intersection measurement procedure was developed to handle this situation for MOSFETs, and, for each value of gate bias, V_G, a common intersection point was measured at closely paired values of V_G at $V_G \pm \Delta V_G$, where ΔV_G may be ~0.25 V. The technique was referred to as the 'paired V_G method' [42]. However, this procedure was not used with the above a-IGZO data set; instead, the intersection of each line with the x-axis in Fig. 9.10a was used as an expedient measure of the change in channel length, ΔL. This is shown as 'L_T' in Fig. 9.11a [36], demonstrating that the effective channel length was weakly gate bias dependent, and ~0.4 μm longer than the mask length. This was attributed to current spreading beneath the metal source and drain contacts.

Figure 9.10b showed that the total series resistance and the normalised channel resistance were comparable, and, therefore, for a device, with a channel length of 5 μm, the series resistance would be ~20 % of the channel resistance, and have an appreciable effect upon the on-current (although its impact would diminish as the channel length increased).

The gate bias dependent values of R_{SD} were attributed to the influence of the gate bias on the semiconductor/Mo contact on the top of the a-IGZO film. The values of R_{SD} in Fig. 9.10b were specific to the technology and geometry of the particular TFTs used, and these values may be corrected to remove the geometric effects either by normalising for the channel width (i.e. $R_{SD}W$ Ωcm), where this makes no assumption about the current distribution in the contact, or by normalising by contact area, A_c, to give the specific contact resistivity, R_c (i.e. $R_{SD}A_c$ Ωcm^2). This requires knowledge of the contact area, and the specific contact resistivity is usually measured in simple vertical contact structures of known area [43], rather than in TFTs. In the measurements here, it was assumed that the channel length extension of ~0.4 μm was an effective measure of the contact length, from which the specific contact resistance at each end of the channel was given by [36]:

$$R_c = \frac{WR_{SD}}{2}\frac{\Delta L}{2} \tag{9.3}$$

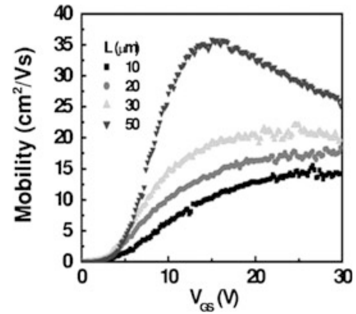


Fig. 9.12 Variation of field effect mobility with gate bias and channel length. (Reprinted with permission from [24]. Copyright (2007) American Institute of Physics)

The two factors of 2 in the denominator account for the measurements of R_{SD} and ΔL being the sum their effects at both ends of the channel. The dependence of R_c on the gate bias is shown in Fig. 9.11b, and, as with R_{SD}, it reduced with increasing gate bias.

In this study [36], the electron mobility was calculated from the slope of the inverse channel resistance/unit length against gate bias, and the intercept with the x-axis gave V_T. Thus, this procedure did not explicitly use the channel length to calculate mobility, but, in contrast, the more widely used field effect mobility calculation does, and, to give an accurate value of mobility, that would require both the use of the effective channel length, and the series resistance. However, by using long channel length TFTs to measure the field effect mobility, both of these corrections are minimised.

It can be assumed that the series resistance effects noted in this paper [36] are common, although the specific values will vary with the detailed processing conditions. A common example of a series resistance artefact is the reduction in field effect mobility with increasing gate bias and reducing channel length, as shown in Fig. 9.12, for an ES inverted staggered a-IGZO TFT [24]. From plots of total resistance as a function of gate length, the series resistance was again shown to be gate bias dependent. The gate width normalised resistance, WR_{SD}, at $V_G = 20$ V was $\sim$250 Ωcm, whereas the comparable figure for the data shown in Fig. 9.10a was $\sim$12.5 Ωcm, illustrating the variability between differently prepared samples. Indeed, some very short channel length TFTs, with L = 50 nm, have been reported with a field effect mobility of 8.2 cm^2/Vs, and good output characteristics, up to a drain bias of 10 V, as seen in Fig. 9.13 [44]. These were BCE inverted staggered TFTs, with a PECVD SiN_x gate dielectric, which was $\sim$40 nm thick, as was the a-IGZO layer. The device displayed very few short channel effects, including minimal drain induced barrier lowering, as is apparent from the tightly clustered transfer characteristics in the sub-threshold regime, and from the high impedance of the output characteristics. No doubt the thin SiN_x layer contributed to the suppression of short channel effects, but the device still had remarkably good characteristics given its channel length. (Short channel effects are discussed in greater detail in Sect. 8.7).

The detailed channel resistance measurements discussed above were for an inverted staggered BCE TFT [36], and a comparable study has been made of ES

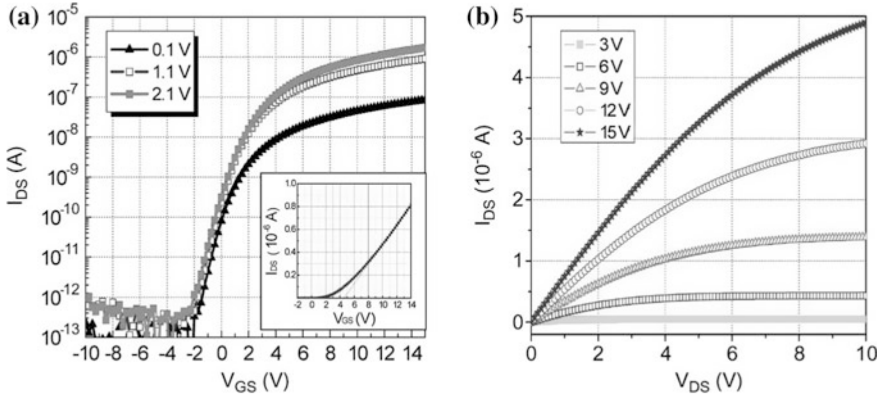


Fig. 9.13 I–V characteristics of short channel TFTs with dimensions W/L = 200/50 nm (**a**) transfer, and (**b**) output characteristics. (Reprinted from [44] with permission of IEEE)

TFTs [37], in which the defined channel length, determined by the width of the ES layer, had less control over the channel current than the separation of the source and drain contacts on top of the ES layer. The device structure is shown in Fig. 9.14a, and the conventional channel length, defined by the width of the etch stop layer, ESL, is given by L_{cnt}, and the separation of the source and drain contacts on ESL is given by L_{mask}. In this structure, the metals were MoW, the 200 nm SiN_x gate dielectric and the SiO_x etch-stop layer were both deposited by PECVD, and the 50 nm thick a-IGZO layer was deposited by RF sputtering [24, 37]. Figure 9.14b shows that the channel current was independent of the width of ESL, L_{cnt}, over the range 10–16 µm, whereas Fig. 9.14c shows that the current varied with the magnitude of L_{mask} over the range 4–10 µm [37]. In broad terms, these results suggest a channel current dominated by contact resistance effects, in which the contact resistance was determined by the magnitude of the overlap of the source and drain pads on ESL. Using the source/drain pad separation, L_{mask}, as the reference channel length, the dependence of R_m and ΔL on V_G were evaluated using the 'paired V_G method' [42], and the results are shown in Fig. 9.15. This demonstrated that, as V_G increased, the effective channel length, L_{eff}, increased beneath the overlap region towards the metal contacts at the edge of ESL (i.e. L_{eff} tended towards L_{cnt}) [37]. At the same time, the total series resistance, R_{ext}, decreased with V_G, where, from Fig. 9.14a:

$$R_{ext} = R_S + R_D + R_{ovS} + R_{ovD} = R_{SD} + R_{ovlp} \tag{9.4}$$

Further analysis of this data, including the separation of R_{SD} and R_{ovlp}, showed that both resistances reduced with increasing V_G, but R_{ovlp} was ~10 times less than R_{SD}, which itself was ~10 times less than the channel resistance. The width normalised series resistance was ~30 Ωcm at V_G-V_T = 10 V [37], which is of the same order as

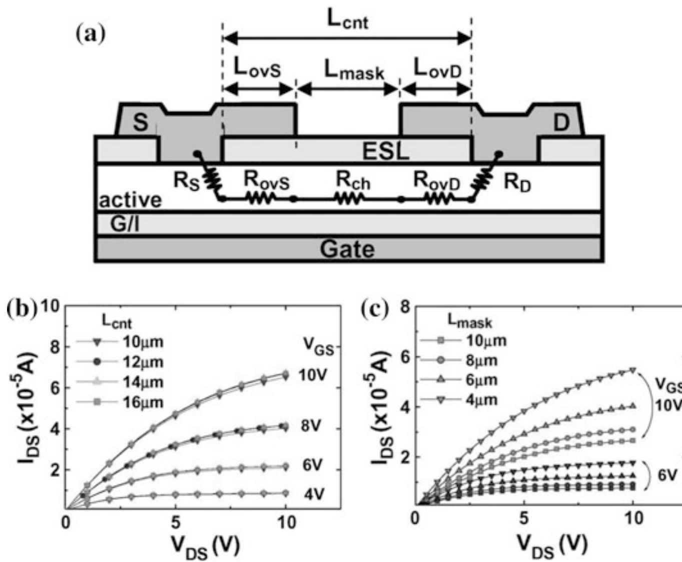


Fig. 9.14 **a** TFT structure, and definition of layout dimensions L_{cnt} and L_{mask}, **b** variation of output characteristics with channel length, L_{cnt}, for $L_{mask} = 4\mu m$, and **c** variation of output characteristics with L_{mask}, with constant channel length, $L_{cnt} = 16\mu m$. (Reprinted from [37] with permission of IEEE)

the value of 12.5 Ωcm measured at 20 V in the BCE device, shown in Fig. 9.10b [36]. A full explanation of these anomalous ES TFT results [37], which are not consistent with conventional MOSFET theory, has not been given, beyond noting that it appeared to be related to the accumulation of electrons beneath the overlap region as the device was turned-on more strongly. However, if this effect is common in a-IGZO TFTs with the ES architecture, then the conventional use of L_{cnt} to calculate the field effect mobility will overestimate its value (because L_{cnt} overestimates the effective channel length).

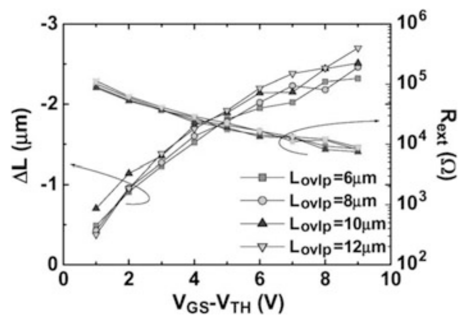


Fig. 9.15 Gate bias dependence of the change in effective channel length, ΔL, and the contact resistance, R_{ext}, for different values of the source/drain metallisation pad overlap on the etch stop layer. (Reprinted from [37] with permission of IEEE)

9.4.2 Conduction Process and Density of States Distribution, DOS

9.4.2.1 Conduction Process

Some of the characteristic features of the conduction process in a-IGZO films have been obtained from Hall effect measurements of doped films [12, 45, 46], such as those shown in Fig. 9.16. Among the key features was the increase in the Hall mobility with the doping density, in Fig. 9.16a. This is opposite to the behaviour seen in c-Si, where the mobility reduces due to increased charged impurity and electron–electron scattering. In Fig. 9.16b, the carrier density was temperature independent for densities above 10^{17}cm^{-3}, indicating that the material was degenerate, with the Fermi level above the conduction band edge [12]. This is also quite different from the behaviour of a-Si:H, where the band tail density was sufficiently great that the Fermi level never entered the conduction band. At the other end of the dopant range in Fig. 9.16b, the lightly doped material displayed a low temperature activation energy of 0.11 eV, as the material 'froze-out' with the electrons trapped on the donor level. Figure 9.16c showed that, in contrast to the temperature independent carrier density at moderate doping levels, the mobility continued to be thermally activated, until much higher carrier concentrations in excess of 2×10^{18}cm^{-3}, when it also became temperature independent [12]. Finally, Fig. 9.16d shows the electrical conductivity, σ, which is the product of the carrier density and mobility, and this was thermally activated at doping levels below 3×10^{19} cm^{-3}, but, only at the lowest carrier concentration was there a unique activation energy. At the intermediate doping levels, where there was not a simple Arrhenius plot, ln(σ) was shown to vary as $T^{-1/4}$ [46]. These results have been interpreted both in terms of a low DOS near the conduction band edge, which permitted the material to become degenerate, and a distribution of potential barriers within the conduction band, which are schematically illustrated in Fig. 9.17a [45, 46]. As indicated, electron transport around these barriers was by percolation, where there was assumed to be a Gaussian distribution of barrier heights, g(E), given by [46]:

$$g(E) = \exp[-(E - \phi_0)^2/(2\sigma_\phi^2)] \tag{9.5}$$

and ϕ_0 is the average barrier height, and σ_ϕ is the energy distribution width, as shown in the simplified diagram in Fig. 9.17b. In this work, the carrier mobility, μ, was related to the band mobility, μ_0, by the following percolation model expression [47]:

$$\mu = \mu_0 \exp\left[-\frac{q\phi_0}{kT} + \frac{(q\sigma_\phi)^2}{2(kT)^2}\right] \tag{9.6}$$

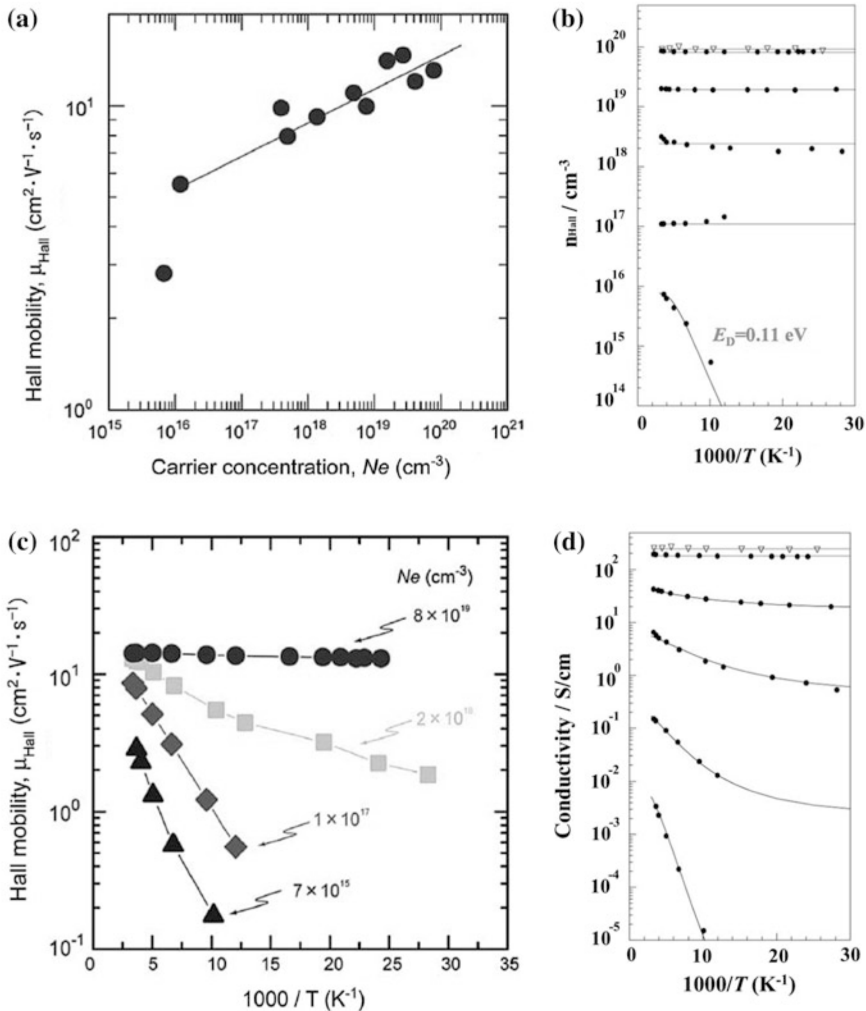


Fig. 9.16 Hall effect data from doped a-IGZO samples (**a**) variation of mobility with electron concentration. Temperature dependence of (**b**) electron density, (**c**) electron Hall mobility, and (**d**) conductivity. (**a** and **c**: Reprinted from [45] Copyright (2006), with permission from Elsevier; **b** and **d**: Reprinted from [12] with permission of IEEE)

The percolation process gave a direct physical explanation for the thermally activated mobility, and its eventual temperature independence at high enough carrier concentrations, when the Fermi level was above the maximum barrier height. The model also gave a good fit to the detailed experimental carrier concentration and conductivity data, as shown by the solid lines in Fig. 9.16b, d respectively [12, 46]. It also followed the $T^{-1/4}$ temperature dependence of the conductivity data (not shown) [46]. In establishing the data fits in Fig. 9.16b, d the

potential barrier height distribution was found to be dependent upon the background doping level, as shown by Fig. 9.17c [46], in which the average barrier height, ϕ_0, was 40–120 meV above the conduction band mobility edge, E_m, and the distribution width, σ_ϕ, was 20–30 meV.

9.4.2.2 Density of States Distribution, DOS

Given the dependence of the Hall mobility on the electron density, some caution is required in using device simulation to establish the DOS in TFTs, particularly when it is done by fitting a calculated transfer characteristic to a measured characteristic [48]. This is because, if the carrier-dependent mobility is ignored, then a field-effect mobility extracted at large V_G will overestimate its value at lower V_G values, with a corresponding overestimate of the DOS [49] (as discussed further below). Equally, the gate-voltage-dependent field-effect mobility itself cannot be

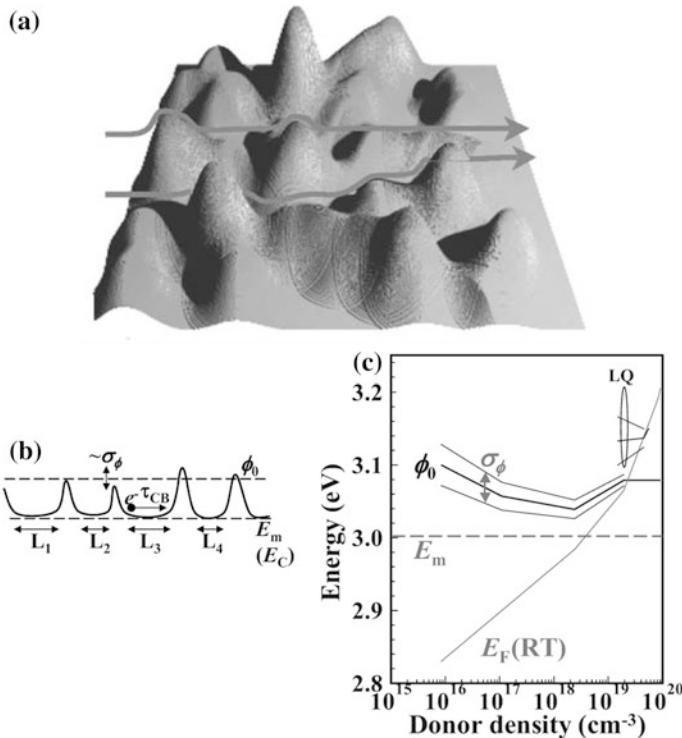


Fig. 9.17 **a** Schematic illustration of potential barriers in the conduction band, and percolation transport of electrons, **b** idealised potential barrier model used in calculations, and **c** variation of fitted barrier parameters with doping density. (**a**: Reprinted from [45] Copyright (2006), with permission from Elsevier; **b** and **c**: Reprinted with permission from [46]. Copyright (2010) American Institute of Physics)

used in the simulation, as this parameter is an artefact of carrier trapping in the DOS, as well as being affected by percolation effects. Indeed, the separation of carrier trapping and percolation phenomena on the field effect mobility should be done by explicitly analysing it for these two effects [21], as discussed below.

In view of these concerns, some authors have used C–V measurements on TFTs [48–50] (rather than I_d-V_G measurements) to determine the trap occupancy as a function of gate bias, because the electron trapping effects will be independent of the electron mobility [48–50]. The DOS thus established was then used to simulate the I_d-V_G characteristics, with the mobility as an adjustable parameter [50]. This yielded an average mobility at each value of gate bias, whereas a more detailed analysis extracted the mobility as a function of free carrier density [49], which could be directly compared with the carrier-dependent Hall-effect mobility.

The C–V measurements [51, 52] made use of the capacitor formed by the gate and the source/drain contact regions in BCE TFTs [48, 49], and the resulting C-V_G and I_d-V_G curves are shown in Fig. 9.18. The C-V_G curve was measured at a low enough frequency that the electrons could follow the frequency of the measuring signal. Using the band bending notation from Chap. 2, the surface potential, V_s, was extracted from the measured C-V_G curve by using [48, 51]:

$$Q_s = C_i(V_G - V_s) \tag{9.7}$$

$$dV_s/dV_G = 1 - (C_i)^{-1} dQ_s/dV_G = 1 - C_m/C_i \tag{9.8}$$

where C_i is the dielectric capacitance (measured at large positive gate bias), C_m is the measured capacitance, and V_s is calculated as a function of V_G by integrating Eq. 9.8:

$$V_s = \int_{V_{FB}}^{V_G} (1 - C_m/C_i) dV_G \tag{9.9}$$

From Gauss Law, the surface field, F_s, is related to the total surface charge, Q_s, by:

$$Q_s = -\varepsilon_0 \varepsilon_s F_s \tag{9.10}$$

Hence, the surface field can be calculated using Eqs. 9.7 and 9.10, together with the numerically calculated values of V_s from Eq. 9.9. The surface field is also related to the space charge density, ρ, by Poisson's equation:

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\varepsilon_0 \varepsilon_s} \tag{9.11}$$

and, for space charge densities dominated by trapped carriers:

$$\rho(x) = -q \int_0^V N dV \tag{9.12}$$

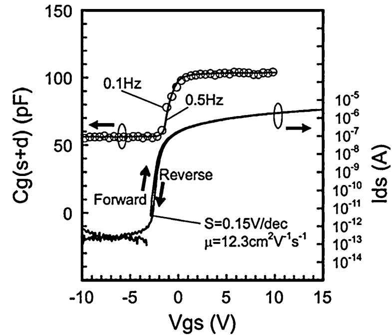


Fig. 9.18 C–V and I-V measurements on a BCE a-IGZO TFT. (Reprinted with permission from [48]. Copyright (2008) American Institute of Physics)

The trap density, N, was used iteratively, as an adjustable parameter, in Eqs. 9.11 and 9.12 to ensure that the values of V_s and F_s from those equations matched those established in Eqs. 9.9 and 9.10. The DOS measured by this procedure is shown by the solid lines in Fig. 9.19a [49], and illustrates the reduction in DOS produced by the post-deposition annealing in wet and dry oxygen, as discussed in Sect. 9.3.2.3. The decrease in the DOS was attributed to the reduction in oxygen deficiencies and structural relaxation as a result of the oxygen annealing procedure [49].

Having established the DOS and the relationship between V_s and V_G, the electron concentration could be calculated through the film at any given value of V_G. This carrier profile was then used in a computational procedure which stratified the a-IGZO film parallel to the dielectric interface, and progressively built up a mobility profile such that the integral of the vertical mobility and carrier concentration profiles accurately simulated the transfer characteristic [49], with the resulting dependence of mobility on electron concentration shown in Fig. 9.19b. This figure showed that the post-deposition annealing treatments primarily affected the DOS rather than the mobility, and also demonstrated that, for a given carrier concentration in the TFT, the electron mobility was lower than the Hall mobility in the doped samples. As indicated, the percolation model was fitted to the field-effect mobility data, and the mobility difference from the Hall samples was attributed to the doping reducing the mean percolation barrier height in the latter, as is apparent in Fig. 9.17c. Hence, this procedure separated the components of electron conduction in the a-IGZO TFTs due to trap limited conduction, determined by the DOS, and percolation conduction in the extended states.

The DOS values represented by the broken lines in Fig. 9.19a were obtained by simply fitting simulated transfer characteristics to measured ones [53], in which the electron mobility, in the simulations, was fixed at the conventionally measured field effect mobility at large gate bias. The overestimate in the DOS, over a substantial fraction of the band-gap, was attributed to the field effect mobility overestimating the correct, carrier-dependent mobility [49].

An alternative C-V_G technique was based upon the use of optical illumination during the measurement to increase the frequency response of the trapped carriers

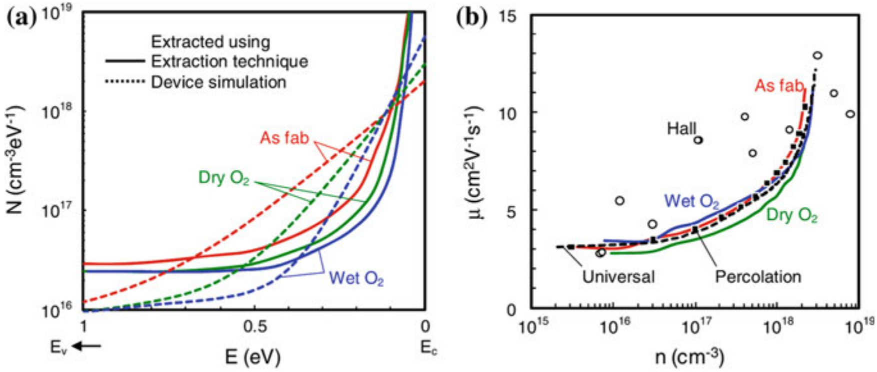


Fig. 9.19 **a** a-IGZO DOS measured by C-V technique (*solid lines*), and DOS measured by conventional TFT simulation (*broken lines*), and **b** extracted electron mobility as a function of the free electron concentration in TFTs (*solid lines*), average mobility (*broken line*), percolation model (*squares*), and Hall mobility in doped films (*open circles*). (Reprinted with permission from [49]. Copyright (2010) American Institute of Physics)

[50], and resulted in a DOS, which was qualitatively similar to that shown in Fig. 9.19a, but with a lower band edge density. The distribution, N(E), was represented by a double exponential of tail and deep states given by:

$$N(E) = 1.2 \times 10^{18}\exp - (E_c - E)/0.125 + 9.5 \times 10^{16}\exp - (E_c - E)/1.4 \tag{9.13}$$

in which the first term represented the tail state density [50].

As mentioned above, the field effect mobility itself has also been analysed in order to separate the DOS responsible for carrier trapping from the potential barrier distribution in the conduction band, controlling the percolation effects [21]. This was done by fitting the data to a model containing percolation-modulated trapping effects when the Fermi level was below the conduction band edge, and percolation transport alone when it was within the band. To account for the effect of the DOS on the mobility, the modified MOSFET equation was used [21, 54]. This was introduced in Chap. 6 (Eq. 6.27) in the discussion of on-state currents in a-Si:H TFTs, and the drain current expression is:

$$I_d = \frac{\mu_0 W C_i^{\alpha-1} \xi}{\alpha L}\left[(V_G - V_T)^{\alpha} - (V_G - V_T - V_d)^{\alpha}\right] \tag{9.14}$$

where μ_0 is the band mobility, and α and ξ are related to the tail state energy width, E_t, and the carrier density trapped in the tail states, N_t, by [54]:

$$\alpha = 2E_t/kT \tag{9.15}$$

$$\xi = \frac{(q\varepsilon_s\varepsilon_0\alpha kTN_t)^{1-\alpha/2}}{\alpha - 1} \tag{9.16}$$

A Taylor expansion of Eq. 9.14 in the linear regime gives [54]:

$$I_d = \frac{\mu_0 W C_i^{\alpha-1} \xi}{L} \left[(V_G - V_T)^{\alpha-1} V_d \right] \tag{9.17}$$

And from Eq. 9.17, the field effect mobility is given by:

$$\mu_{FE} = \mu_0 C_i^{\alpha-2} \xi(\alpha - 1)(V_G - V_T)^{\alpha-2} = \mu_0 A (V_G - V_T)^{2(E_{t/kT}-1)} \tag{9.18}$$

However, the band mobility, μ_0, must be modified to include the influence of percolation, so that, using Eq. 9.6, Eq. 9.18 becomes:

$$\mu_{FE} = \mu_0 \exp\left[-\frac{q\phi_0}{kT} + \frac{(q\sigma_\varphi)^2}{2(kT)^2} \right] A (V_G - V_T)^{2(E_{t/kT}-1)} \tag{9.19}$$

In summary, Eq. 9.19 describes the situation in which the Fermi level is below the conduction band edge, and transport is limited by both carrier trapping and percolation effects.

At a gate bias in excess of V_P, which is the threshold voltage for percolation, and occurs when the Fermi level is positioned at the conduction band edge, the mobility is controlled only by percolation, and the field effect mobility is given by [21]:

$$\mu_{FE} = \mu_0 \exp\left[-\frac{q\phi_0}{kT} + \frac{(q\sigma_\phi)^2}{2(kT)^2} \right] \exp\frac{q\Delta V_s}{kT} \tag{9.20}$$

Equation 9.20 is valid for Fermi level positions between the band edge and the maximum barrier height, ϕ_M, and ΔV_s corresponds to the change in Fermi level position within the band due to a change in band bending ΔV_s. By developing an approximate analytical expression for the free carrier density as a function of V_s, a relationship was established between ΔV_s and ΔV_G, from which the following expression was derived [21]:

$$\mu_{FE} = \mu_0 \exp\left[-\frac{q\phi_0}{kT} + \frac{(q\sigma_\phi)^2}{2(kT)^2} \right] B (V_G - V_P)^{4S} \tag{9.21}$$

where S is the ratio, $(D_B\text{-}W_B)/D_B$, of the percolation barrier width, W_B, and the inter-barrier spacing, D_B. Hence, both equations 9.19 and 9.21 show that the field effect mobility has a power law dependence on V_G of the form:

$$\mu_{FE} = K (V_G - V_{T,P})^\gamma \tag{9.22}$$

The values of K and γ were extracted from the solid line fits of the model to the experimental field effect mobility data shown in Fig. 9.20a (for a bi-layer a-IZO/a-IGZO TFT). These fits yielded a band mobility of 70 cm^2/Vs, values of ϕ_0, and σ_ϕ of 50 meV and 45 meV, respectively, and a band tail DOS given by:

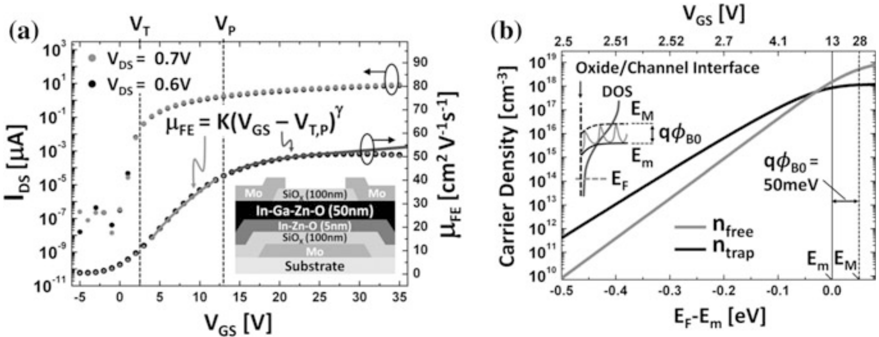


Fig. 9.20 **a** Measured values (data points) of I_{ds}, and μ_{FE} in an a-IZO/a-IGZO TFT, and the fitted expressions (*solid lines*) from equations 9.19 and 9.21, and **b** calculated variation of free and trapped electron densities with Fermi level position. (Reprinted with permission from [21]. Copyright (2011) American Institute of Physics)

$$N(E) = 4 \times 10^{19} \exp - (E_c - E)/0.035 \tag{9.23}$$

Using the extracted DOS parameters, Fig. 9.20b shows the calculated free and trapped carrier densities as a function of Fermi level position, and identifies the threshold voltage, V_P, for percolation limited conduction at 13 V [21]. This figure also illustrates the greater concentration of trapped charge, compared with free charge, when the Fermi level was more than ~0.05 eV below the conduction band edge, and confirms the trap limited conduction within this gate voltage range [21].

It is apparent that accurate DOS and percolation parameter assessment in AOS TFTs present a number of challenges, and different techniques are being explored. Also, whilst the currently published DOS values show some variability with device processing and layer composition, it is equally clear that the field effect mobility and tail state DOS values are consistently superior to those found in a-Si:H TFTs.

9.4.3 Bias Stress Instability

Due to its different bonding configuration, the meta-stable weak bond breaking observed in a-Si:H is predicted not to occur in AOS devices [55], but, even without this mechanism, both positive [53, 56–58] and negative [57, 58] gate bias instabilities have been widely reported in a-IGZO TFTs. The instability is predominantly a positive threshold voltage shift with positive gate bias stress, and is accompanied by minimal changes in mobility or sub-threshold slope. The shift is indicative of electron trapping at/near the AOS/dielectric interface, and is driven by the electron accumulation within the film. For negative bias stress, the threshold voltage shifts negatively, and is consistent with hole trapping. In addition, optical illumination

during bias stress results in a further instability process, which greatly increases the magnitude of the negative bias instability [57, 59], and reduces the positive bias stress shift [60], or even produces a net negative shift [61]. The optically enhanced instability has been attributed to photo-ionisation of the oxygen vacancy [18, 59, 61–63], and has also been correlated with persistent photoconductivity in the a-IGZO layer after the removal of the illumination [61–63]. Similar gate bias instability effects have also been reported in a wide range of other AOS TFT materials (including HfInZnO, AlSnInZnO, ZnInSnO, ZnInO, ZnSnO and ZnO) [62, 64, 65], and the a-IGZO results reviewed below can be taken to be broadly representative of the instabilities observed in other AOS materials of interest.

9.4.3.1 Gate Bias Instability

Typical examples, and artefacts, of positive gate bias instabilities are shown in Fig. 9.21a–d [53, 56]. These results were obtained after constant current stress (with positive gate and drain bias), from differently prepared inverted staggered TFTs. Figure 9.21a and b compare the shift in the transfer characteristics of an unannealed device with one given a post-deposition wet anneal at 400 °C [53]. As discussed in Sect. 9.3.2.3, anneals of this type are essential to improve the basic device characteristics, and they similarly reduce the magnitude of the gate bias instability, resulting in a small parallel shift of the transfer characteristics. From simulations [53], and a-IGZO film thickness dependent stability results [57], it was concluded that the defects were electron traps at the a-IGZO/dielectric interface in the annealed TFTs. A further aspect of device processing was identified by the results in Fig. 9.21c and d, in which an organic photoacryl and an inorganic, PECVD SiO_x passivation layer were compared in etch-stop TFTs [56]. The SiO_x layer was found to result in a smaller and more parallel shift of the transfer characteristics, and, indeed, the magnitude of the instability was found to be critically dependent upon the type of passivation layer used. The best results were obtained with a dense SiO_x layer, which suppressed the gate bias instability, and this was attributed to it providing an impervious barrier to the ingress of ambient oxygen and moisture into the top surface of the a-IGZO film, where these impurities led to trap generation within the film. Further work has directly correlated the instability of unpassivated, bottom gate devices with the relative humidity of the ambient during bias stressing [66], and also to water vapour exposure prior to the stress measurement [58]. A high quality passivation layer is, therefore, needed to minimise this contribution to positive gate bias instability, where the residual instability is associated with trapping at the dielectric/semiconductor interface.

A high quality dielectric layer is also necessary to reduce trapping within the layer itself [58, 67], and, for top-gate TFTs, the dielectric deposition process itself needs careful control to avoid damage to the underlying AOS layer [64]. For bottom gate TFTs, superior stability was obtained with a PECVD SiO_x gate dielectric compared with PECVD SiN_x [67], and the difference was attributed to a higher hydrogen content in the latter giving a larger trap state density.

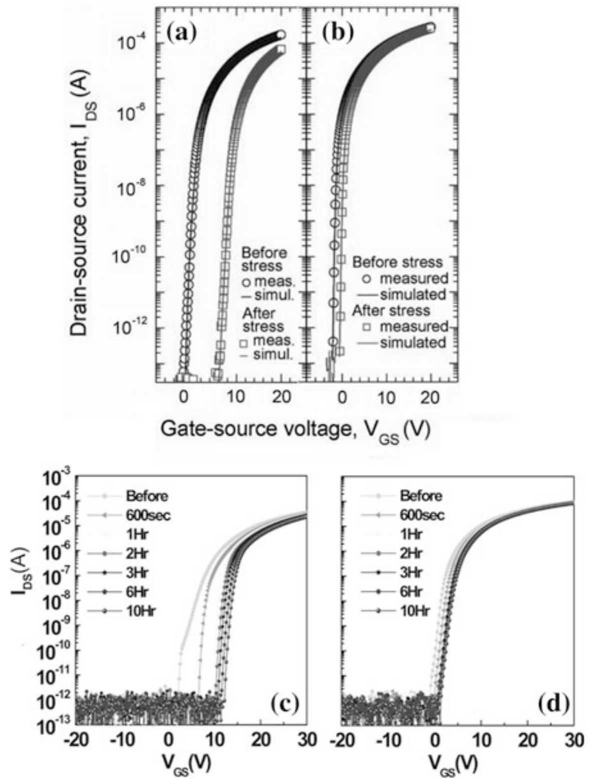


Fig. 9.21 Positive gate bias instabilities induced by constant current stress in a-IGZO TFTs (**a**) unannealed, and (**b**) with post-deposition wet anneal of a-IGZO at 400 °C (50 h stress at 5μA) (Reprinted with permission from [53]. Copyright (2009) American Institute of Physics). Time dependent stress at 10μA with (**c**) organic photo-acryl, and (**d**) inorganic PECVD SiO_x passivation layers. (Reprinted with permission from [56]. Copyright (2008) American Institute of Physics)

The time dependence of the positive gate bias instability was thermally activated, and followed a stretched exponential [57, 58, 60, 65] of the form:

$$\Delta V_T = (V_{GSt} - V_{T0})\left\{1 - \exp -\left(\frac{t}{\tau}\right)^{\beta}\right\} \tag{9.24}$$

where V_{GSt} is the stress bias, V_{T0} is the pre-stress threshold voltage, $\beta = T/T_0$, and the thermally activated time constant, τ, is given by:

$$\tau = \nu \exp\left(\frac{E_A}{kT}\right) \tag{9.25}$$

This process describes time dependent trapping into an exponential distribution of trapping states, with a characteristic width T_0. It is apparent that the kinetics of the instability process can be empirically modelled using the same formalism as used to describe gate bias instabilities in a-Si:H TFTs (see Sect. 6.4.1), although the physical mechanisms underlying the instabilities are quite different. Depending upon the details of sample fabrication, and the measurement conditions, activation energies, E_A, have been reported over the range 0.4 eV [60] to 0.7 eV [58].

The bias stress induced threshold voltage shifts were reversible after the removal of the gate bias, and the recovery characteristics also displayed a stretched exponential time dependence, but with a different activation energy compared with the initial instability results [58, 60].

As is apparent from the above discussion, careful device processing is required to minimise the positive gate bias instability, where important details include the choice of gate dielectric, defect removal in the AOS film by post-deposition annealing, and the implementation of a suitable passivation process over the device structure. With such processing, the negative gate bias instability is usually smaller than any residual positive gate bias instability. However, if negative gate bias stressing occurs under conditions of optical illumination, large negative threshold voltage shifts can occur [57, 59], even for devices showing good negative bias stability in the dark, as discussed in the following section.

9.4.3.2 Negative Bias Illumination Stress (NBIS)

Due to the transparency of the AOS materials, and the frequent use of transparent gate metals, there may be no natural light screening of the TFT when it is used for active matrix addressing of LCDs and OLEDs. As this will be a photon rich environment, the optical response of the TFTs, and the impact of optical illumination on their bias stability, have been widely studied [18, 57, 59, 61–63]. The NBIS instability is a negative shift in threshold voltage, and this occurs for both band-gap illumination ($E > 3.0$ eV), as well as for sub-band-gap illumination, as shown by the representative results in Fig. 9.22 [57]. These results were obtained from wet-annealed inverted staggered a-IGZO TFTs, and similar results have been obtained from top-gated TFTs [59], as well as from bottom-gated a-HfInZnO [62], and bi-layer a-InZnO/a-IGZO [61] TFTs passivated with SiO_x. The results in Fig. 9.22a showed that the devices were stable with negative gate bias stress in the

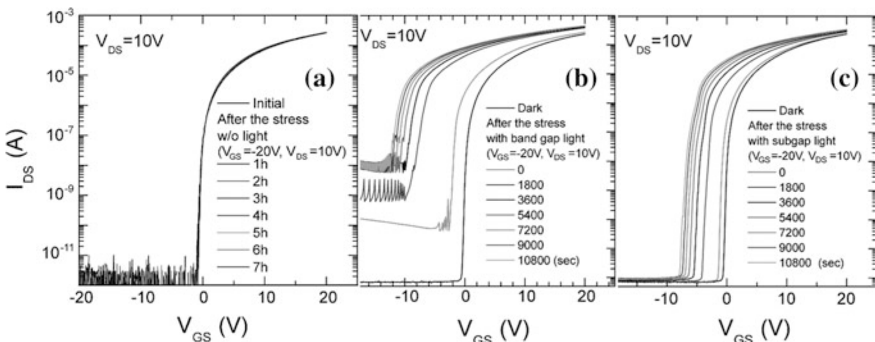


Fig. 9.22 Time dependent negative bias stress effects ($V_G = -20$ V) on TFT transfer characteristics (**a**) dark, (**b**) illumination at $E = 3.4$ eV, and (**c**) illumination at $E = 2.7$ eV. (Reprinted from [57] with permission of SID)

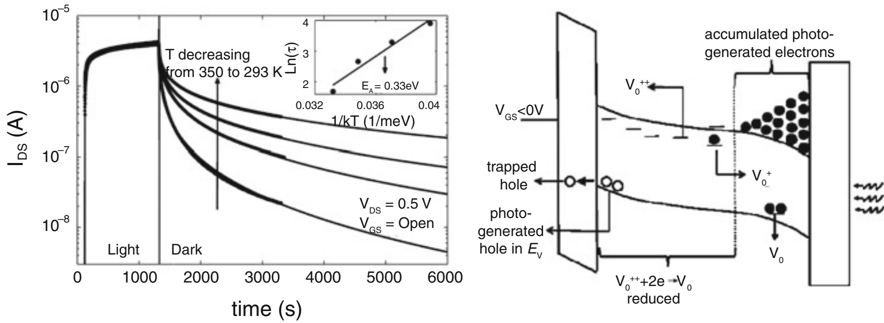


Fig. 9.23 **a** Time and temperature dependent dark relaxation of channel current after illumination (Reprinted with permission from [62]. Copyright (2010) American Institute of Physics), and **b** TFT band bending diagram during NBIS, showing shallow donor formation at the front of the film, and electron accumulation at the back of the film. (Reprinted from [61] with permission of SID)

dark, but, with both 3.4 eV (365 nm) band-gap illumination and with 2.7 eV (460 nm) sub-band visible illumination (in Fig. 9.22b and c, respectively), the threshold voltage was negatively shifted, and there was an associated time-dependent deterioration in the sub-threshold slope and the mobility values as well [57]. The shift in the transfer characteristics, and the increase in sub-threshold slope, are indicative of NBIS-induced positive charge trapping and trap generation in the upper half of the band-gap, respectively. Although the effects were greatest with band-gap light, more attention has been paid to the sub-band light, as this is the wavelength range experienced by the addressing TFTs in active matrix displays. Even without a negative gate bias, optical illumination alone shifted the threshold voltage negatively, as shown by the zero stress time results in Fig. 9.22b, c.

Following the termination of the NBIS tests, and the removal of the illumination and gate bias, there was a slow and thermally activated relaxation of the characteristics over a period of many hours, irrespective of whether bias had been applied or not. An example of the relaxation of the channel current (at $V_G = 0$ V), following illumination alone, is shown in Fig. 9.23a, where the data has been fitted by a stretched exponential, and the insert shows the relaxation activation energy. The illumination-induced threshold voltage shift (both without and without bias [61]), leading to the large, dark channel currents, is referred to as persistent photoconductivity [61, 62].

The above effects have been attributed to photo-ionisation of the neutral oxygen vacancy, V_0 [18, 59, 61, 62]. This vacancy level is in the lower half of the band gap, and, by virtue of its usual neutral charge state and its position below the Fermi level, it does not usually influence the operation of n-channel TFTs. However, under negative gate bias it is raised towards the Fermi level at the surface, and sub-band white light can photo-ionise it by exciting electrons to the conduction band, producing positively charged V_0^+ and V_0^{++} centres. As the oxygen vacancy is a

negative-U centre [18, 62], the ionised levels are above the neutral level, in the upper half of the band gap, and the V_0^{++} level is expected to be close to the conduction band edge [18]. For the centre to have this negative-U behaviour, it is necessary for the lattice to relax, by the movement of adjacent metal ions, when the centre is ionised, and this results in a potential barrier between the ionised and neutral states, which must be overcome for the centre to relax back to its neutral state when the illumination is switched off [62]. This is consistent with the thermally activated relaxation process, shown in Fig. 9.23a, where the measured activation energy is of the same order as calculations of the thermal barrier height [62]. The effects described above are summarised in the illustrative band diagram in Fig. 9.23b [61] of the TFT under NBIS. This shows the upward bending of the bands at the surface, and the localised presence of the V_0^{++} centres, whilst, at the back of the film, the bands are bent downwards to accommodate the photo-generated electrons, and, in this region, the oxygen vacancy is occupied by electrons and is neutral. The band bending will separate the photo-generated holes and electrons, with the field sweeping the holes to the front surface of the film, where they are trapped in the gate dielectric or in interface states.

Although the role of the oxygen vacancy has been widely invoked in the NBIS instability mechanism, there are also results linking the instability to inadequate passivation of the back surface of the film, and AlO_x [68] and Y_2O_3 [69] passivated structures have been shown to have much better stability than unpassivated ones. From the a-IGZO film thickness dependence of the instability, it was also shown that the photo-ionisable defects in the lower half of the band-gap, which underlie the instability in the unpassivated films, were generated on the top (exposed) surface of the film [69]. The greater instability in the unpassivated films has been attributed to the introduction of water molecules or the desorption of O^- ions [68], or possibly due to proton movement from absorbed hydrogen [69].

Whilst improved control of the NBIS instability has been demonstrated, the precise mechanism, as the above review indicates, is still open to debate, and it continues to be the subject of widespread research.

9.4.3.3 Stability Considerations for Active Matrix Addressing TFTs

For active matrix applications, the addressing TFT will experience an alternating combination of positive and negative gate biases, and, in assessing the long-term lifetime of the TFT, it is useful to determine whether this pulsed AC stress produces the same instability as the DC stress discussed above. Figure 9.24 compares the effect of DC stress with both single polarity and bipolarity pulsed bias stress (in an inverted staggered a-IGZO TFT passivated with an SiO_x layer) [70]. In these particular devices, the threshold voltage shifts were comparable for both negative and positive bias DC stresses, but they were reduced almost to zero for pulsed negative bias stress, and halved for pulsed positive bias stress. These pulsed results were for a 50 % duty cycle with a 5 ms pulse width. For this duty cycle, the negative pulse bias results were independent of the absolute pulse width (with ΔV_T

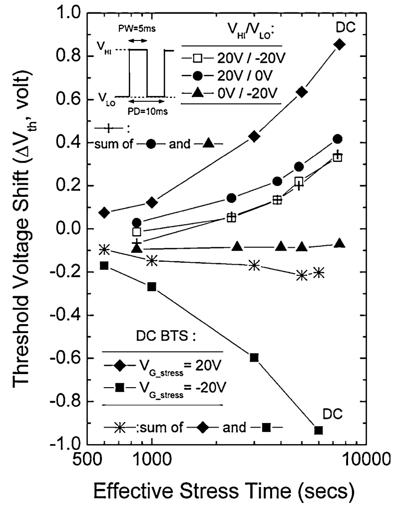


Fig. 9.24 Comparison of the threshold voltage shifts after pulsed bias and DC bias stress of a-IGZO TFTs. (Reprinted from [70] with permission of SID)

remaining close to zero), whilst, for positive pulse bias, ΔV_T increased with increasing pulse width, and tended towards the DC values. The small ΔV_T noted with the negative pulse bias stress was attributed to the slow hole accumulation processes within the material, and the consequent reduction in hole trapping at the surface compared with the DC results [70]. Due to the minimal effect of the negative pulse stressing, the bipolar pulse stressing in Fig. 9.24 (open square symbols) was almost entirely dominated by the positive pulse bias results, and were well approximated by the summation of the negative and positive pulse bias results. In contrast, the summation of the DC results did not predict the effect of bipolar pulse stressing. This investigation did not include negative pulsed bias stress under illumination, which, for DC stressing, produces a much larger ΔV_T. However, this effect has been examined, in a-HfInZnO TFTs [71], as a function of duty cycle and frequency, with a square wave pulse oscillating between +20 V and −20 V. In agreement with the dark, negative pulse bias results of Fig. 9.24, the negative threshold voltage shift with illumination was suppressed for duty cycles greater than ~1 % (positive bias), and the net shift was determined almost entirely by the positive bias stress cycle. Hence, these results indicate that, under pulsed operation conditions, the NBIS instability may be considerably less than observed with DC measurements.

Notwithstanding the above comments, all instability processes should be reduced as much as possible for TFTs used in commercial applications. The interaction of processing procedures and instability effects were discussed in Sect. 9.4.3.1, and improved stability can be achieved by post-deposition annealing of the a-IGZO, the use of a high quality gate dielectric, and effective passivation of the back surface to prevent moisture and oxygen ingress into the TFT. The sequential layer depositions must also be carried out in a way which minimises

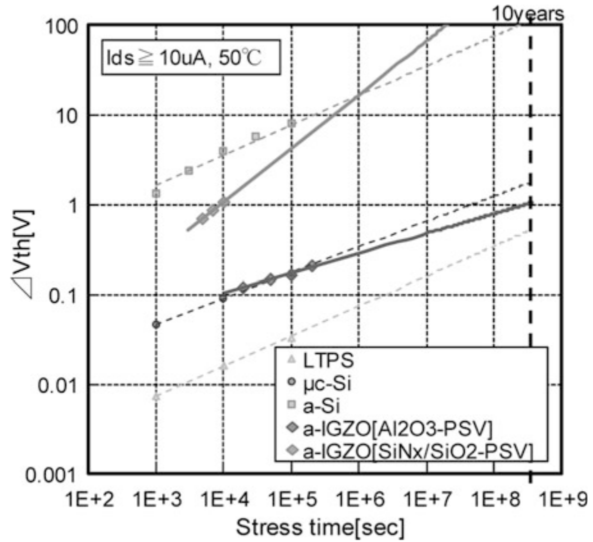


Fig. 9.25 Constant current stress instability of Al_2O_3 and SiO_x/SiN_x passivated a-IGZO TFTs compared with a-Si:H, poly-Si, and micro-crystalline Si TFTs. (Reprinted from [73] with permission of SID)

damage to the underlying films, whilst also being consistent with large area, high-throughput manufacturing. As indicated in Sect. 9.1, there are many examples of demonstrator displays being fabricated with a-IGZO addressing TFTs [2–4, 6, 13], several of which report high stability devices. One example of this [72, 73] was an inverted staggered etch-stop TFT, employing a dual layer gate dielectric of PECVD SiN_x and SiO_x (with the latter uppermost and adjacent to the DC-sputtered a-IGZO), an SiO_x etch-stop layer, Mo source/drain contacts covering the a-IGZO island edges, and a final passivation layer of DC-sputtered Al_2O_3. From positive gate bias stress measurements at 50 °C, an operating life of 10 years was predicted with an extrapolated threshold voltage shift of <1 V. In addition, after 10^4s NBIS at -20 V, using a white light source emitting in the range 380−720 nm, the threshold voltage shift was only −0.2 V, and this was attributed to excellent back-face passivation by the DC-sputtered Al_2O_3 film [72]. With the above measures, the long-term stability of these passivated a-IGZO TFTs for AMOLED displays is expected to exceed that of a-Si:H TFTs, be comparable to micro-crystalline Si, and to approach poly-Si, as shown by the constant current stress data in Fig. 9.25 [73].

9.5 AOS TFT Circuits

In view of the use of AOS material for the pixel driving TFT in demonstrator FPDs, there is widespread interest in exploiting the high carrier mobility to integrate driver circuits into these displays. From considerations of power consumption in digital logic circuits, it is preferable to use a complementary (p- and n-channel) device

technology. As discussed in Sect. 9.2, the AOS materials, including a-IGZO, used for the high electron mobility devices, have a large density of states in the lower half of the band-gap, giving very poor p-channel behaviour [12]. However, by careful choice of the constituent materials, good p-channel TFT operation has been achieved in SnO, due to the valence band edge being made up of spatially spread s-orbitals from the Sn^{2+} ion [74]. The hole mobility was 1.3 cm^2/Vs, but the n-channel TFTs in this material had a field effect mobility of only 1.5×10^{-4} cm^2/Vs [75]. Hence, as yet, there is not a monolithic AOS technology capable of delivering well-matched complementary pairs of TFTs in the same material, and most of the activity in this area has focussed on circuit implementation using the single channel n-type a-IGZO TFTs.

Given these limitations, alternative inverter circuit architectures (compared with the conventional two complementary TFTs) have been investigated to obtain good voltage switching, ideally with low power consumption. One option is to use a depletion device as the load TFT, and this has been engineered by using a double-gated load TFT to give a more negative threshold voltage than the drive TFT [76]. This gave a large output voltage swing, but power consumption was high. An alternative approach used a cross-coupled inverter design, containing six TFTs, to achieve a high output voltage swing, and $\sim$70 % lower power consumption than a conventional 2-stage, single channel inverter [77]. In addition to these specific circuit studies, a range of driver circuits have already been integrated into a-IGZO demonstrator displays, including row driver circuits [78, 79] for AMOLEDs, row and column drivers for an LCD [23], as well as an LCD driver circuit [80] incorporating a common electrode inversion circuit to reduce the overall power consumption (compared with the more common dot inversion technique [81]). (AMLCD drive inversion schemes are briefly reviewed in Sect. 4.3).

9.6 Summary

Transparent amorphous oxide semiconductor materials, and in particular a-InGaZnO (a-IGZO), are attracting increasing attention as an alternative TFT material to a-Si:H and poly-Si, especially for large sized AMOLED displays. This is because the material has an electron mobility $\sim$10 times higher than a-Si:H, and is, therefore, more easily able to deliver the larger drive currents needed for OLEDs. Although the mobility is still an order less than poly-Si, it may have better uniformity by being an amorphous material, and promises a simpler processing schedule. However, the current TFTs are only n-channel, and integrated logic circuits made in this material will be slower and consume more power than the complementary pair circuits available with poly-Si TFTs. Nevertheless, there are now examples of driver circuits integrated into a-IGZO demonstration displays, and attention is being given to the design of low power, single channel circuits.

The high electron mobility in this amorphous material is a consequence of its ionic bonding structure, which also delivers a low density of trapping states near the

conduction band edge. Hence, the TFTs have a sharper turn-on than a-Si:H TFTs, and state-of-the-art devices also display better gate bias stability, which is another important issue for the AMOLED application. However, there still are stability issues with AOS TFTS, especially with negative bias stress under illumination conditions. This instability has been associated with photo-ionisation of the oxygen vacancy, and this is an on-going research topic. From an application point of view, the instability is reduced under pulsed bias conditions, and good passivation of the device has been demonstrated to significantly diminish the effect.

Due to the low DOS, the Fermi level can be moved into the conduction band, where the conduction process in a-IGZO is controlled by percolation. This results in a carrier density dependent mobility, which has to be taken into account when measuring the DOS. In particular, the conventional iterative fit of a device model to the transfer characteristics will over-estimate the DOS if the on-state field-effect mobility is simply used. To avoid these problems, C-V techniques have been established for the DOS measurement, and, by using these DOS values, the carrier-dependent mobility can be extracted from the transfer characteristics.

The device structure is typically either inverted staggered etch-stop or inverted coplanar, which can be made with a 5 or 4 mask process, respectively. In principle, this is a low temperature process, including the deposition of a-IGZO by DC sputtering at room temperature, although post-deposition anneals are required to stabilise the material. Nevertheless, the potential for low temperature processing also makes it attractive for flexible substrate applications. Many current devices are fabricated with metal source and drain contacts directly on the a-IGZO, and attention is being directed towards series resistance issues, with some processing schedules incorporating a metal sinter stage to reduce the contact resistance between the metal and the semiconductor. Device performance is sensitive to ambient oxygen and water, and effective passivation of the structure is essential for the fabrication of high quality TFTs with stable long-term operation.

In summary, AOS TFTs are commanding widespread application interest, with numerous demonstrations of a-IGZO addressed displays. This is supported by a substantial research activity into the details of device behaviour, and further improvements in device physics and TFT performance can be anticipated. In addition, commercial applications to AMOLED displays, and to large, high resolution AMLCDs have been forecast.

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