Chapter 8
Poly-Si TFT Performance

Abstract This chapter deals with the electrical characterisation, and related performance issues, of poly-Si TFTs. The subjects covered include an analytical model for conduction in poly-crystalline material, issues with the measurement of the poly-Si DOS, low field and high field leakage current behaviour, and an overview of the bias stress instability mechanisms in these devices. Finally, there is a discussion of short channel effects, including the role of parasitic bipolar transistor action caused by floating body effects.

8.1 Introduction

Chapter 7 dealt with the preparation of poly-Si material, as well as describing the architecture and fabrication process of poly-Si TFTs. In this chapter, the characterisation and performance of these devices is dealt with in greater detail. Poly-Si is a polycrystalline material, consisting of small grains separated by grain boundaries, and the understanding of this composite material, which is spatially inhomogeneous, is important both in establishing a basic understanding of device behaviour, and in recognising the limitations of some of the assumptions made in analysing its behaviour. Hence, Sect. 8.2 introduces a classical model of conduction in poly-Si [1]. This could be regarded as a model covering polycrystalline material in general, within which grain boundary states play an important role in trapping free carriers. This is a simple analytical model, which establishes some basic physics and concepts in a readily accessible fashion, even though the simplifications in this model have been superseded by more complex numerical models. This point is developed in Sect. 8.3, which discusses the measurement of the density of states, DOS, in poly-Si, and highlights the issues of distinguishing trapping states within the grains from those in the grain boundary regions.

S. D. Brotherton, *Introduction to Thin Film Transistors*,
DOI: 10.1007/978-3-319-00002-2_8,

Section 8.4 describes the low field leakage current behaviour in TFTs from the standpoint of a classical carrier flow and electron–hole pair generation rate model, and relates this to the quality of the poly-Si.

Section 8.5 discusses other performance issues with poly-Si TFTs, in particular, the effects associated with a high electrostatic field at the drain junction. Firstly, it is demonstrated that this is a two dimensional field, which is controlled by both the voltage on the drain and the gate field. The high field is responsible for hot carrier instabilities, and field enhanced leakage currents, in high quality poly-Si TFTs. The high fields are essentially a device architecture issue, rather than a material quality issue, and the solution to this is found in the relief of the drain field by lightly doped drain regions (LDD), as discussed in Sect. 7.4.1.2. Although the hot carrier damage, discussed in Sect. 8.5.2, is a major reliability issue in n-channel TFTs, there are other instability mechanisms in poly-Si TFTs, which are displayed in other biasing regimes, and these are briefly discussed in Sect. 8.6.

Finally, the current understanding of the performance of short channel TFTs is reviewed in Sect. 8.7, which also deals with the issue of floating body effects in the TFTs.

The understanding of the issues discussed in this chapter has been crucial to their resolution, and, as discussed in Chap. 7, this has facilitated the mass-production of stable, high quality poly-Si TFTs for flat panel display applications.

8.2 Electrical Conduction in Poly-Si

8.2.1 Analytical Bulk Conduction Model

As is readily apparent from electron microscopy images of poly-Si, it is a polycrystalline material, consisting of discrete grains, of variable crystallographic orientation, separated by inter-grain regions. These regions need to accommodate the changes in crystallographic orientation in going from one grain to the next, and, rather like the surfaces of crystalline regions, the interruption to the periodic lattice structure of the grain can be expected to introduce defects states into the forbidden band gap at its surface. In addition, there may also be impurity defect states here. Hence, the grain boundary regions will be regions of structural disorder, and will contain deep level trapping states within the forbidden band-gap. Indeed, many aspects of the performance of poly-Si have been ascribed to carrier trapping effects at the grain boundaries, and the resistivity of doped poly-Si is a good example of this.

Figure 8.1a shows the variation of resistivity with boron concentration in p-type poly-Si, for two different grain sizes, and compares it with single crystal Si [2]. There a number of striking differences between the two types of material. Firstly, in single crystal silicon, the resistivity varies almost inversely with boron concentration, and this is only seen at the higher doping levels in poly-Si, where the

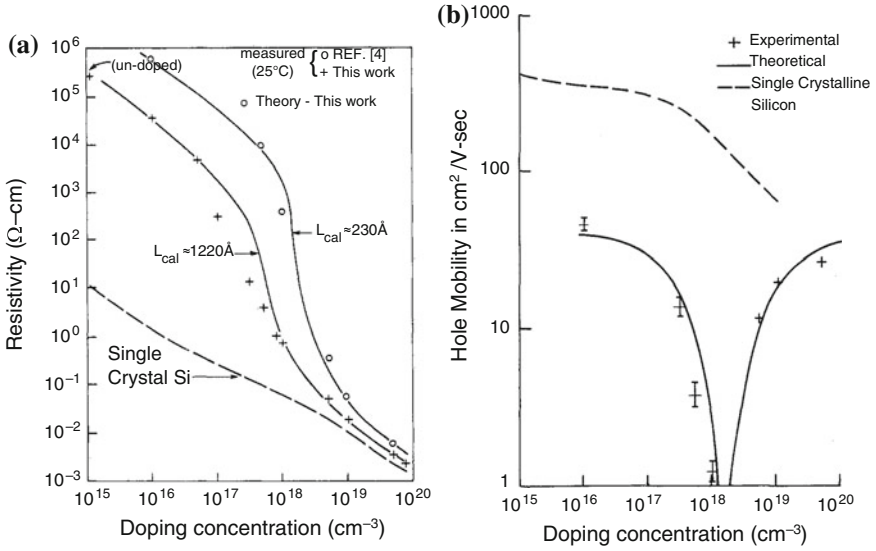

Fig. 8.1 Comparison of parameter dependence on boron doping concentration in poly-Si and c-Si **a** resistivity for two different poly-Si grain sizes (Reprinted from [2] with permission of IEEE), and **b** hole mobility (Reprinted with permission from [1]. Copyright (1975) American Institute of Physics)

resistivity approaches that of c-Si. Secondly, at very low concentrations, the poly-Si resistivity is several orders of magnitude higher than c-Si, and, thirdly, over a narrow range of doping levels, the poly-Si resistivity drops very abruptly. There are also clear differences in the behaviour of the Hall mobility in the two material types, as shown in Fig. 8.1b [1]. Whereas the hole mobility in crystalline Si shows a gradual decrease with increasing doping level, due to increased charged impurity scattering, the Hall-effect hole mobility in poly-Si shows a completely different behaviour, with the mobility falling to a very low value at moderate doping levels, before rising back to a value comparable to c-Si at higher doping levels.

The characteristic behaviour of poly-Si, as shown in Fig. 8.1, has been attributed to carrier trapping in the grain boundaries, GBs, and has been quantitatively described using a simple, analytical model [1]. In this, the material is represented by a combination of trap-free single crystal grain regions, doped with a boron acceptor density N, and separated by planar grain boundary regions containing an areal density, Q_T, of deep donor trapping levels at E_T-E_V, as illustrated in Fig. 8.2. Figure 8.2a shows a single crystal grain of length L, which is separated from the adjacent grains by the grain boundaries. Figure 8.2b shows the charge distribution between the GBs, where the GBs have trapped free holes from the grain. For charge neutrality, the positive trapped charge in the GBs will be balanced by the negative space charge in the regions of length *l* within the grains, where the ionised boron acceptors have lost their holes to the GBs. Hence, to maintain the overall space charge neutrality, the positive charge in the GBs, Q_T^+, will be equal to the

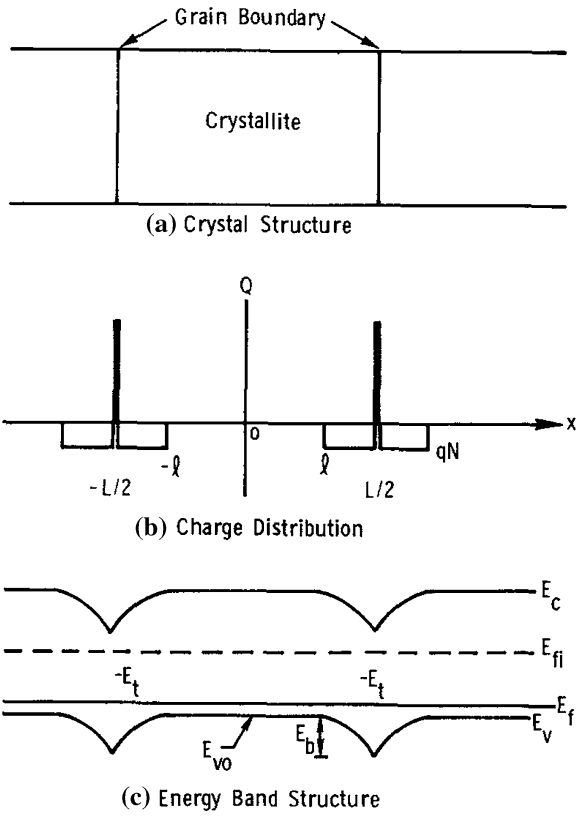

Fig. 8.2 Analytical model for grain boundary effects in poly-Si **a** GB model, **b** space charge distribution, and **c** band diagram, showing band bending (Reprinted with permission from [1]. Copyright (1975) American Institute of Physics)

negative charge, Nl, in the two space charge regions either side of the GB. The band bending, in Fig. 8.2c, is shown for a particular situation, in which the Fermi level is close to the valence band edge, and beneath the GB trapping level, E_T. This represents a heavily doped grain, and fully occupied hole traps. There is a potential barrier at the GB due to the charge Q_T on the traps, and the compensating depletion region extending partially into the grain by the distance l. The band bending in this region can be calculated from Poisson's equation:

$$\frac{d^2V}{dx^2} = \frac{qN}{\varepsilon_0 \varepsilon_s} \tag{8.1}$$

Integrating this twice, and assuming that dV/dx = 0 at l, the potential distribution in the grain is:

$$V = \frac{qNx^2}{2\varepsilon_0 \varepsilon_s} \tag{8.2}$$

and the potential barrier height at the GB is:

$$V_b = \frac{qNl^2}{2\varepsilon_0\varepsilon_s} \tag{8.3}$$

For charge neutrality (and using the depletion approximation and zero Kelvin Fermi–Dirac statistics):

$Nl = 0.5Q_T$, and, therefore, the barrier height, V_b, can be expressed as:

$$V_b = \frac{qQ_T^2}{8\varepsilon_0\varepsilon_s N} \tag{8.4}$$

In other words, for partially depleted grains, and fully occupied traps, where $Nl = 0.5Q_T$, the GB barrier height, V_b, diminishes as the grain doping level increases.

However, in the alternative situation, where $Nl < 0.5Q_T$, all the holes are trapped in the partially occupied GB traps, and the grain is fully depleted, giving rise to the high resistivities seen at low doping levels in Fig. 8.1a. In this fully depleted case, $l = L/2$, the Fermi level will be above the trapping level, E_T, and Eq. 8.3 becomes:

$$V_b = \frac{qNL^2}{8\varepsilon_0\varepsilon_s} \tag{8.5}$$

and, for the fully depleted grains, the GB barrier height increases with grain doping level. For very lightly doped grains, V_b is close to zero, and it increases linearly with doping concentration up to a maximum value, $V_{b(max)}$, of:

$$V_{b(\max)} = \frac{qN^*L^2}{8\varepsilon_0\varepsilon_s} \tag{8.6}$$

at the critical doping concentration, N^*, where $N^*L = Q_T$. Hence, $V_{b(max)}$ is a function of both grain size and GB trap state density, and an example of the V_b and $V_{b(max)}$ dependences on N and Q_T is shown, for mid-gap traps, in Fig. 8.3 [3]. It will be appreciated that increments in doping concentration, above the critical dopant level, N*, now start to add an almost equal number of free carriers within the grain, and this, combined with the reducing barrier height, leads to the steep reduction in resistivity, seen in Fig. 8.1a.

An analytical expression for the conductivity of the material [1] was developed by assuming that, when a bias was applied to the poly-Si material, current flow was limited by the motion of carriers over the potential boundary at the GB, rather than by current flow within the grain itself. The maximum carrier flow over the potential barrier is given by thermionic emission, which is independent of the shape of the potential barrier and is determined only by its height. For simplicity, this mechanism was assumed, where the current density, J_{th}, is given by the number of carriers moving towards the GB with energies sufficient to overcome the potential barrier [4], and a general expression for the thermionic emission current over a barrier of height Φ_b is:

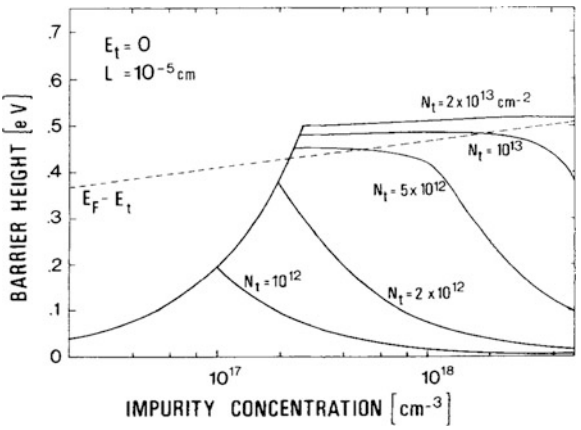

Fig. 8.3 Calculated variation, with doping concentration, of the potential barrier height at a grain boundary. The calculations are for different concentrations, N_t, of a discrete grain boundary trap at mid-gap (Reprinted with permission from [3]. Copyright (1978) American Institute of Physics)

$$J_{th} = qnv \exp\left(-\frac{q\Phi_b}{kT}\right)\left(\exp\frac{qV_a}{kT} - 1\right) \tag{8.7}$$

where, v is the carrier's thermal collection velocity (= $\{kT/2\pi m^*\}^{0.5}$) [5], n is the carrier concentration at the bottom of the barrier, m* is its effective mass, and V_a is the potential drop across the barrier.

In using this expression, the carrier density employed by Seto [1] was the average number, P_a, in the grain, which was calculated by integrating the free hole distribution, p(x), across the grain, and dividing it by L. For a fully depleted grain, p(x) is given by:

$$p(x) = N_V \exp\left[-\left\{qV(x) - E_f\right\}/kT\right] \tag{8.8}$$

and P_a is:

$$P_a = \frac{n_i}{Lq}\left(\frac{2\pi\varepsilon_s\varepsilon_0 kT}{N}\right)^{1/2} \exp\left(\frac{E_b + E_f}{kT}\right) erf\left[\frac{qL}{2}\left(\frac{N}{2\varepsilon_s\varepsilon_0 kT}\right)^{1/2}\right] \tag{8.9}$$

where $E_b = qV_b$, and n_i is the intrinsic carrier concentration. The Fermi level, E_f, is determined by the following equality:

$$NL = \frac{Q_T}{1 + 2\exp\left[\left(E_T - E_f\right)/kT\right]} \tag{8.10}$$

For partially depleted grains, the carrier concentration, p_b, in the undepleted region is approximately equal to N in non-degenerate samples, and is related to the Fermi level by:

$$p_b = N_V \exp -(E_f/kT) \tag{8.11}$$

The average concentration, P_a, of the un-depleted and fully depleted regions is [1]:

$$P_a = p_b\left\{\left(1-\frac{Q_T}{LN}\right)+\frac{1}{qL}\left(\frac{2\pi\varepsilon_s\varepsilon_0 kT}{N}\right)^{1/2} erf\left[\frac{qQ_T}{2}\left(\frac{1}{2\varepsilon_s\varepsilon_0 kTN}\right)^{1/2}\right]\right\} \quad (8.12)$$

From Eq. 8.7, the thermionic emission current, J_{th}, for a voltage V_a applied across a grain boundary, and where $V_b > kT$, is [1]:

$$J_{th} = qP_a\left(\frac{kT}{2\pi m^*}\right)^{1/2}\exp\left(-\frac{qV_b}{kT}\right)\left[\exp\left(\frac{qV_a}{kT}\right)-1\right] \quad (8.13)$$

and, if $qV_a << kT$, Eq. 8.13 reduces to:

$$J_{th} = q^2P_a\left(\frac{1}{2\pi m^* kT}\right)^{1/2}\exp\left(-\frac{qV_b}{kT}\right)V_a \quad (8.14)$$

The conductivity, σ, of a material is related to the current density, J, and the electric field, E, by $J = \sigma E$, so, the poly-Si conductivity can be evaluated from Eq. 8.14 together with Eqs. 8.9 or 8.12:

$$\sigma = Lq^2P_a\left(\frac{1}{2\pi m^* kT}\right)^{1/2}\exp\left(-\frac{qV_b}{kT}\right) \quad (8.15)$$

and from $\sigma = qp\mu$, the effective carrier mobility, μ_{eff}, is given by:

$$\mu_{eff} = Lq\left(\frac{1}{2\pi m^* kT}\right)^{1/2}\exp\left(-\frac{qV_b}{kT}\right) \quad (8.16)$$

Hence, as V_b goes through a maximum with doping level, the effective mobility goes through a minimum, as shown in Fig. 8.1b. A generic version of this equation,

$$\mu_{eff} = \mu_0\exp\left(-\frac{qV_b}{kT}\right) \quad (8.17)$$

is also often used to relate the poly-Si field effect mobility to an assumed GB barrier height in the TFT channel [5, 6].

Using Eqs. 8.15 and 8.16 (together with some scaling parameters), the model was successfully fitted to the resistivity and Hall-effect mobility data by Seto [1]. Examples of these fits by Lu et al. [2] and Seto [1] are shown by the solid lines in Fig. 8.1a and b, respectively. (The scaling parameters are discussed in Sect. 8.2.3). Hence, this simple analytical model, based upon local carrier trapping at grain boundaries, and the associated potential barriers in the valence band, encompassed the essential features of the experimental data. It offered an explanation for the high resistivity of lightly doped poly-Si, the sharp fall in resistivity at a critical

doping level, the asymptotic approach to c-Si data at high doping levels, and the anomalous behaviour of the Hall-effect hole mobility.

The above analysis has been based upon p-type doping of poly-Si, together with GB-associated deep donor traps, and the induced potential barriers in the valence band edge. The essential features of the model have been shown to apply equally well to n-type doped poly-Si, in which potential barriers arise in the conduction band edge due to electron trapping at deep acceptor levels in the upper half of the band gap [3].

8.2.2 Analytical Model of TFT Conduction

The key features of the bulk conduction model have also been used to produce an analytical model for conduction in poly-Si TFTs, in which the dependence of the barrier height on doping level has been replaced by an equivalent dependence upon the carrier density induced in the channel by the gate voltage [5]. In the same way as in the Seto model, this model also assumed discrete trapping levels for the GBs, and thermionic emission over the potential barriers at the band edges. An expression was derived for the channel current as a function of gate voltage, in which the gate voltage controlled the carrier density in the channel, and, hence, the height of the potential barriers at the GBs [5]:

$$I_d = \frac{\mu_0 W C_{ox} V_G V_d}{L} \exp - \left(\frac{q^3 Q_T^2 t_i}{8\varepsilon_s \varepsilon_0 kT C_{ox} V_G} \right) \tag{8.18}$$

W, L are TFT channel width and length, respectively, V_G and V_d are gate and drain biases, respectively, C_{ox} is the gate oxide capacitance, and t_i is the inversion layer thickness (giving the equivalent volume charge density in the channel from $C_{ox}V_G/t_i$). The barrier height term in Eq. 8.18 corresponds to Eq. 8.4, which described the potential barrier at a GB in a partially depleted grain. Also, in this expression, the mobility term, μ_0, was given by qLv/kT (where v was the carrier's thermal collection velocity), and this retained the thermionic emission criterion.

Equation 8.18 can be used to analyse experimental TFT transfer characteristics, by plotting $\ln(I_d/V_G)$ versus $1/V_G$, as shown by the inset in Fig. 8.4, from which, the slope gives Q_T, and the intercept gives μ_0. This plot is from a 2-D simulation of TFT transfer characteristics, with 0.5 μm long grains, and mid-gap traps at the GBs [7], and similar experimental data plots have been published by Levinson et al. [5], and by many other authors. The range of V_G values (within which the plot was linear) was from ~4.5 to 7 V, which corresponded to the sub-threshold/near-threshold current regime, where the increase in channel current was ascribed, by the model, to the reduction in GB-barrier height. For this particular simulation, Q_T could be correctly calculated to be 2×10^{12} cm^{-2}, by taking the inversion layer thickness, t_i, to be 34 nm [7]. However, this value will generally not be

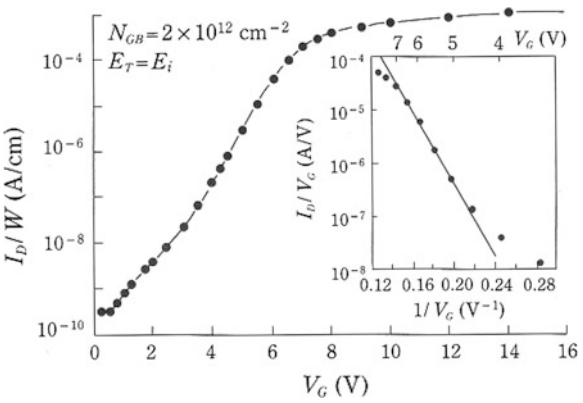

Fig. 8.4 Calculated transfer characteristic of a TFT containing 0.5 μm long grains, with a mid-gap trap at the GB. The inset is a Levinson plot of $\ln(I_d/V_G)$ versus $1/V_G$. (Reprinted from [7])

known experimentally, and this introduces an unavoidable numerical uncertainty in using this technique.

8.2.3 Limitations of Analytical Model

As will be shown in Sect. 8.3, contemporary evaluations of the density of states, DOS, in poly-Si TFTs show a continuous distribution of trapping states across the band gap. Hence, the assumption of just a discrete trapping level is a major simplification, which fails to reflect the true nature of poly-Si, and the value of Q_T extracted from the analytical TFT analysis [5] will be an artefact of this assumption. However, as shown by Fig. 8.5, one of the key features of the model is retained with a distributed DOS [3], namely, the initial increase in GB barrier height with increasing doping level, and then a reduction in height once a critical doping level was exceeded. In this case, the critical doping density, N^*, occurred,

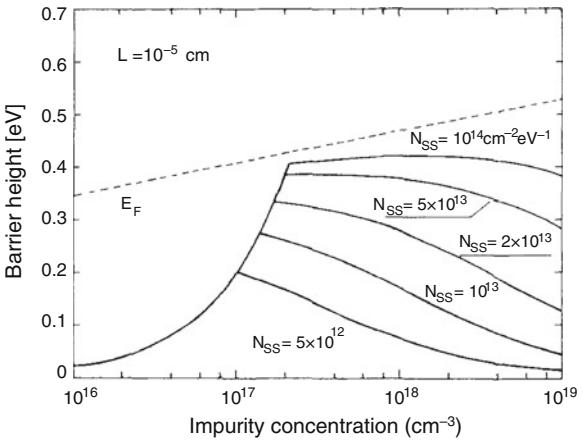

Fig. 8.5 Calculated variation, with doping concentration, of the potential barrier height at a grain boundary. The calculations are for different concentrations of GB traps uniformly distributed across the band-gap. (Reprinted with permission from [3]. Copyright (1978) American Institute of Physics)

for a uniform trap distribution, $N_{GB}(E)$, when the total space charge in the grain, N*L, was equal to the integral of the trapped charge in the distributed GB states, and this equality could be expressed as [3]:

$$N^* = \left(\frac{N_{GB}}{L}\right)\left(1 + \frac{q^2 N_{GB} L}{8\varepsilon_s \varepsilon_0}\right)^{-1} kT \ln\left(\frac{N^*}{n_i}\right) \tag{8.19}$$

which needs to be solved iteratively for N^*.

The other simplifications have been, firstly, the assumption of thermionic emission, as opposed to drift/diffusion carrier transport, and, secondly, the nature of the GB region itself, and whether it is adequately represented by a planar boundary [8]. These issues were raised, in part, by the scaling factors used to fit Eq. 8.15 to the experimental data [1, 8]. The added scaling factors were a pre-exponential term, f, and an ideality factor, n, giving the modified conductivity equation:

$$\sigma = fLq^2 P_a \left(\frac{1}{2\pi m^* kT}\right)^{1/2} \exp\left(-\frac{qV_b}{nkT}\right) \tag{8.20}$$

where f was 0.12 and n was 6.49. It was shown in this later work [8] that, by treating the GB region as an a-Si-like region of ~1–2.5 nm width, with band-tail and deep states, there was trap-limited conduction in this region. Hence, the material's conductivity was not merely limited by transport both within the grains and across the potential barriers at the GBs, but account also had to be taken of transport within finite width grain boundary regions themselves. By adding these further considerations, including drift/diffusion flow over the potential barriers, it was possible to fit the experimental data in Fig. 8.1a, without the arbitrary fitting factors, f and n, used in the earlier work [8].

In spite of these detailed qualifications to the bulk conduction model of Seto [1], its TFT equivalent, Eq. 8.18 [5], has continued to be widely used in many publications to analyse the poly-Si TFT characteristics, and to extract a GB trapping state density, Q_T. In view of the above limitations in the basic model, and the particular problem of knowing the inversion layer thickness, t_i, in Eq. 8.18, the extracted Q_T values should be taken more as a figure of merit for the TFT, rather than as an accurate estimate of the trapping state density associated with the GB region.

8.3 Poly-Si Density of States, DOS

Section 8.2 introduced the role of GB trapping states in explaining the behaviour of bulk poly-Si resistors, and briefly discussed the extension of a simple analytical model [1] to analysing TFT behaviour [5]. This section continues that discussion by looking, more broadly, at the evaluation of the poly-Si DOS, but without the limitations imposed by the simplifications in the analytical model. In general

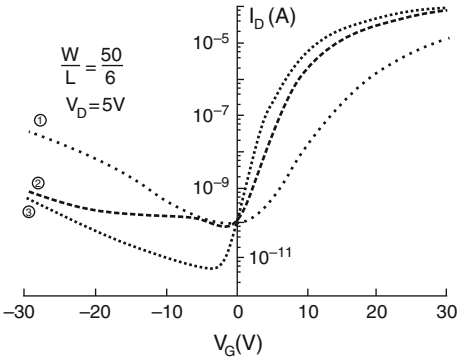

Fig. 8.6 Small grain poly-Si TFT transfer characteristics measured after different exposures times to a hydrogen plasma: (*1*) 0 h, (*2*) 0.5 h, (*3*) 4 h. The increasing exposure times produced reducing densities of states across the band-gap. (Reprinted from [9] Copyright (1991), with permission from Elsevier)

terms, the overall performance of poly-Si TFTs is affected by states within the forbidden band-gap: those near the centre contributing to leakage current, whilst those close to the band-edge will reduce the field effect mobility from the band value, and states in between will determine the sub-threshold slope and threshold voltage. These dependences are illustrated in Fig. 8.6, for a set of poly-Si TFTs, whose different DOS levels were determined by different exposure times to an atomic hydrogen passivation process [9]. Comparing the TFT with zero exposure time (and high DOS) to the device with 4 h exposure (and low DOS), the latter had a higher on-current, lower off-current, lower threshold voltage and smaller sub-threshold slope. The Levinson analysis [5] showed a reduction in effective GB trapping state density from 2.7×10^{12} cm^{-2} to 1.0×10^{12} cm^{-2}, although, as discussed in Sect. 8.2.2, these absolute values are subject to some numerical uncertainty, but the relative change is a more reliable indicator of the overall change in DOS.

Given the limitations of the Levinson analysis, many authors have used a variety of more sophisticated techniques to analyse the TFT characteristics, in order to extract the distribution of trapping states [10–15]. In these analyses, it has also been recognised that certain forms of poly-Si, such as the large faulted grain material produced by the SPC process, are likely to have defects states within the grains themselves, and not merely at the grain boundaries [10, 14]. In addition, the assumption of mono-energetic trapping states was relaxed, and the DOS was evaluated across the back-gap. The techniques have included 1-D analysis of the field-effect conductance, obtained from the TFT transfer characteristic [10], the measurement of the temperature dependent emission of electrons from the traps, using deep level transient spectroscopy [11], or, more commonly, 2-D numerical simulations to reproduce the transfer characteristic [12–15]. From this work, there is a general consensus that there is a continuous distribution of trapping states across the band-gap [10–15], as shown in Fig. 8.7 [12], and this is frequently represented by a double exponential distribution of states in each half of the band-gap:

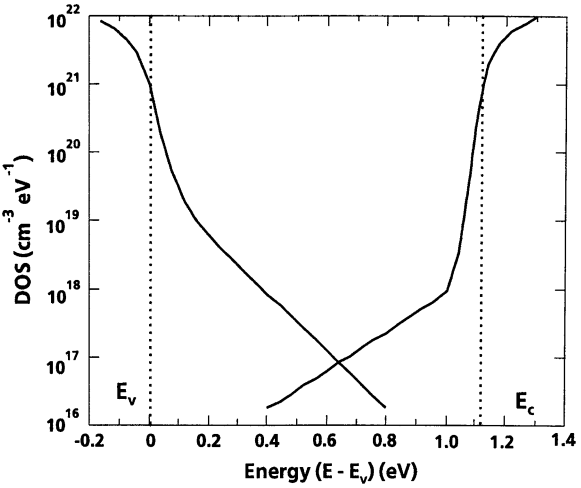

Fig. 8.7 Calculated poly-Si DOS, obtained from a 2-D simulator fit to experimental transfer characteristics (Reprinted with permission from [12]. Copyright (1990) The Japan Society of Applied Physics)

$$N(E) = N_T \exp - \frac{E}{E_T} + N_D \exp - \frac{E}{E_D} \tag{8.21}$$

where N_T and N_D are the band-edge concentrations of tail and deep states, respectively, and E_T and E_D are the characteristic energy widths of these states. The same expression is used for both the acceptor states in the upper half of the band-gap and the donor states in the lower half of the band-gap, although the individual parameter values are usually different in the two halves of the band-gap. The total densities, integrated across the band-gap, are given by $N_T E_T$ and $N_D E_D$, for the tail-states and deep states, respectively.

However, a persistent problem in uniquely determining the DOS in poly-Si has been the difficulty in distinguishing between trapping states within the grains and trapping states at the grain boundaries. This is because the conventional poly-Si grain size is smaller than the typical TFT channel dimensions, and device measurements always yield an effective trapping state density per unit gate area, which can be attributed to an equivalent density of charges trapped in the grains and/or in the GBs. Some authors have attempted to partition the distribution between these two sites [14, 15], whilst others have used a spatially uniform effective density of states [12, 13] (which is also more computationally efficient, as it requires fewer mesh lines within the model). In all these cases, justification for the assumed distributions was based upon demonstrating a good fit of the model to experimental transfer characteristic data. However, with the large number of adjustable parameters in these simulations, and the different underlying assumptions, the question of an unambiguous characterisation of inter-grain and intra-grain defects remained unresolved.

As with the poly-Si resistor analysis, a further problem is the appropriate representation of the grain boundary itself, either as a planar, 2-D distribution of defects, or as a thin disordered, 3-D region of defects between the grains.

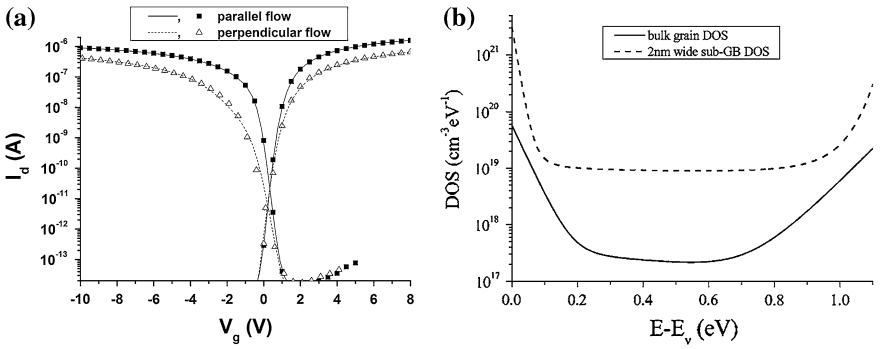

Fig. 8.8 **a** Experimental (*symbols*) and fitted (*lines*) data to SLS poly-Si transfer characteristics, for carrier flow parallel and perpendicular to the sub-GBs in the SLS material, **b** in-grain and GB DOS extracted from the SLS material (Reprinted with permission from [16]. Copyright (2007) American Institute of Physics)

Recent work using long-grain SLS poly-Si has addressed these problems, by exploiting the anisotropic nature of this material (as discussed in Sect. 7.5.2.1), in which the grain size in one direction exceeded the channel length [16]. In that work, the carrier flow parallel to the sub-GBs ($\mu_n = 218$ cm^2/Vs) was assumed to be controlled only by states within the grains, whereas carrier flow orthogonal to the sub-GBs ($\mu_n = 76$ cm^2/Vs) was assumed to be controlled by both the in-grain states as well as by the GB states. Hence, by using data from orthogonal TFTs, the in-grain DOS could be separated from the GB DOS. The temperature dependent transfer characteristics were measured in these two directions, and 2-D simulations of the transfer characteristics and their activation energies were used to establish the DOS for the intra-grain and inter-grain states [16]. The fitted characteristics, measured at 324 K, are shown in Fig. 8.8a, and, to obtain a consistent fit across the range of measurement temperatures, the GB states could not be treated as a 2-D planar distribution of defects, but had to be treated as a 2 nm wide, thin disordered region. This was because, in spite of the mobility differences for parallel and perpendicular flow remaining constant into strong inversion, the activation energy for perpendicular flow was close to zero. Such a small activation energy was not consistent with a GB barrier height large enough to produce the observed mobility difference (Eq. 8.17 predicted a barrier height of 27 meV at 295 K). Within the narrow GB region, the fitted DOS determined the carrier density, and, hence, the resistive current flowing through that region. This resistive current flow was the limiting transport mechanism in the TFT, and was also characterised by a near-zero activation energy, in agreement with the experimental data. The resulting DOS distributions for the in-grain and the GB states are shown in Fig. 8.8b. As with the earlier evaluations, such as in Fig. 8.7, the distribution of both types of states was continuous across the band-gap, with an exponential-like distribution near the band-edges. The results in Fig. 8.8b also demonstrated that there was a much higher integrated volume density of traps within the GB region than in the

grains themselves: for the band-tail states, in the upper half of the band gap, the densities were 7.7×10^{18} cm^{-3} and 1.7×10^{18} cm^{-3} respectively, and the deep state densities were $\sim$50 times larger in the GBs. However, the 2 nm width of the GB region, L_{GB}, compared with the 300 nm grain size, L_G, meant that the total density of GB states per unit surface area of the film (3.4×10^{11} cm^{-2}) was only $\sim$5 % of the equivalent density within the grains (7.2×10^{12} cm^{-2}), where the density per unit surface area, N_{SA}, of GB states, N_{GB}, is given by:

$$N_{SA} = \frac{N_{GB} t_f L_{GB}}{L_{GB} + L_G} \tag{8.22}$$

and t_f is the film thickness.

The detailed analysis of the sub-GB defects in the SLS poly-Si TFTs was consistent with the analysis of conduction in poly-Si resistors [8], which avoided the use of fitting factors, and demonstrated that the results could be most satisfactorily explained by assuming that the GB region was a narrow disordered region, rather than a 2-D plane of defects. Thus, the transport of carriers within this region determined the overall conductivity of the material, rather than the emission of carriers over the potential barrier at the GBs.

In some TFT simulation work [16, 17], the temperature and field dependence of the carrier mobility has been incorporated into the 2-D models by using functions developed for c-Si simulations such as the Canali [18] and Lombardi [19] formulations. In particular instances, such as the simulation of long channel length TFTs [17], the incorporation of the transverse field dependence of the mobility has been essential for the accurate reproduction of the mobility variation with gate bias at large gate biases.

8.4 TFT Off-State Currents

The basic electron–hole pair generation process has been discussed in Chap. 2, and this process, plus the transport of the generated carriers to the contacts, will be used to examine the leakage current behaviour observed in poly-Si TFTs. Experimentally, the leakage current is found to be very dependent upon the magnitude of the field at the drain junction, and low field and high field regimes can be readily distinguished. The former is governed by the field-independent generation processes described in Chap. 2, whilst the latter is determined by field-enhanced emission processes. The low-field generation process will be described in this section, using a simple analytical model to give physical insight into the process, and the high field process will be covered in Sect. 8.5.3, which groups together other drain field dependent processes.

The transfer characteristics, from a range of different channel length TFTs, are shown in Fig. 8.9a–c for different DOS levels. From a leakage current perspective,

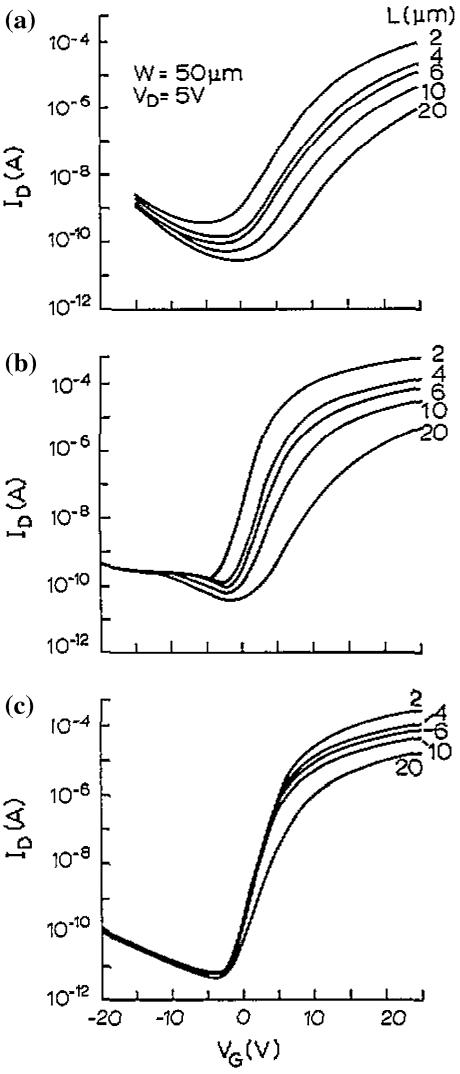

Fig. 8.9 Channel length dependent transfer characteristics for poly-Si TFTs with different DOS levels, after varying degrees of plasma hydrogenation **a** zero, **b** partial, and **c** full hydrogenation (Reprinted from [20], with permission from IOP Publishing Ltd)

the major difference between curves Fig. 8.9a and c, apart from the absolute values of current, is that the leakage current was channel length dependent in the high DOS case, whereas, in the low DOS case, the leakage current was independent of channel length [20]. The corresponding I_D-V_D leakage current curves, for different values of V_G, are shown in Fig. 8.10a–c, for 10μm or 6μm channel length TFTs. For the high DOS devices in Fig. 8.10a, the minimum current varied inversely with channel length [9], and the I_D-V_D curve was linear, suggesting a resistive, or a drift-limited, current flowing through a non-rectifying contact. For the medium DOS device in Fig. 8.10b there was resistive current flow at low V_D, which saturated into a quadratic current at higher V_D, and the applied voltage, at which

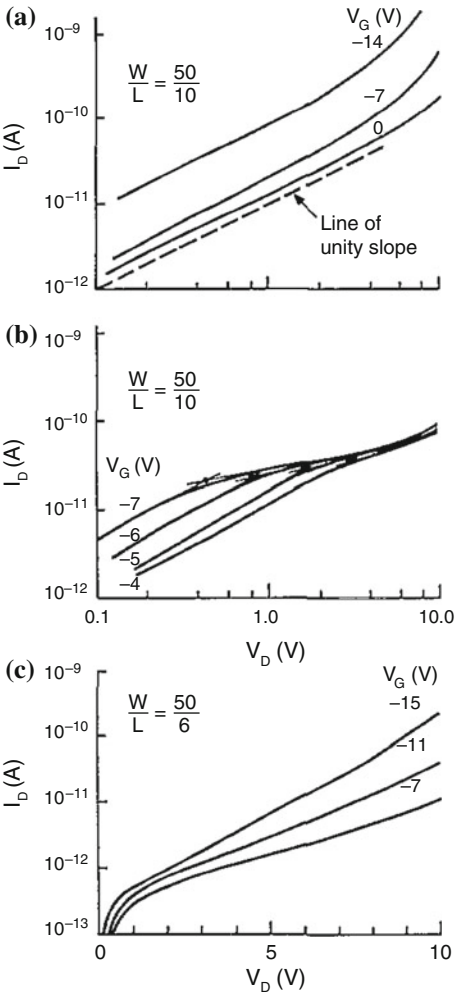

Fig. 8.10 Gate and drain bias dependent leakage current characteristics for poly-Si TFTs with different DOS levels, after varying degrees of plasma hydrogenation **a** zero, **b** partial, and **c** full hydrogenation. (Reprinted from [20], with permission from IOP Publishing Ltd)

this occurred, reduced with increasing negative gate bias. Finally, for the lowest DOS device in Figs. 8.9c and 8.10c, the channel length independence and the exponential increase in current with both V_G and V_D indicates a field enhanced generation current. The leakage current mechanism, displayed in Fig. 8.10a and b, is described below by a simple analytical n^+p junction model [9], and the field enhanced current is analysed in Sect. 8.5.3.

The model used for the low-field currents in Fig. 8.10a and b is shown in Fig. 8.11, in which there is electron–hole pair generation in the drain space charge region, supported by the voltage dropped across this region, V_{gen}, and resistive hole flow to the source junction, causing a voltage drop, V_R, across the neutral

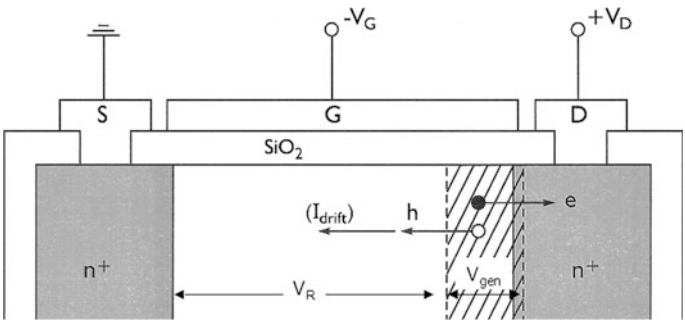

Fig. 8.11 Cross sectional diagram of TFT, showing carrier generation, voltage distribution, and leakage current paths

portion of the transistor body. From Chap. 2, the generation current, J_{gen}, is given by:

$$J_{gen} = \frac{qn_i x_D}{\tau} \tag{8.23}$$

and the drift current, J_R, is given by:

$$J_R = q(n\mu_n + p\mu_p)F \approx q\alpha p_i \mu_p F \tag{8.24}$$

assuming that $p = \alpha p_i = \alpha n_i$ and that $\alpha > 1$ for negative gate biases, where there will be surface accumulation of holes (n_i and p_i are the intrinsic carrier concentrations). The field, F, in the transistor body is given by:

$$F = \frac{V_R}{L - x_D} \tag{8.25}$$

where, from Chap. 2, the space charge width, x_D, is:

$$x_D = \sqrt{\frac{2\varepsilon_s \varepsilon_0 V_{gen}}{qN_T}} \tag{8.26}$$

$$V_D = V_{gen} + V_R \tag{8.27}$$

$$J_{gen} = J_R = J_D \tag{8.28}$$

Therefore,

$$J_D = \frac{-L + \sqrt{L^2 + 4qn_i\alpha\mu_p V_D\left(\frac{N_T\alpha\mu_p\tau^2}{2\varepsilon_s\varepsilon_0 n_i} - \frac{\tau}{qn_i}\right)}}{2\left(\frac{N_T\alpha\mu_p\tau^2}{2\varepsilon_s\varepsilon_0 n_i} - \frac{\tau}{qn_i}\right)} \tag{8.29}$$

Whilst Eq. 8.29 has been fitted to experimental data [9], it is more instructive to look at the predictions of this equation, and to compare it to the general form of the

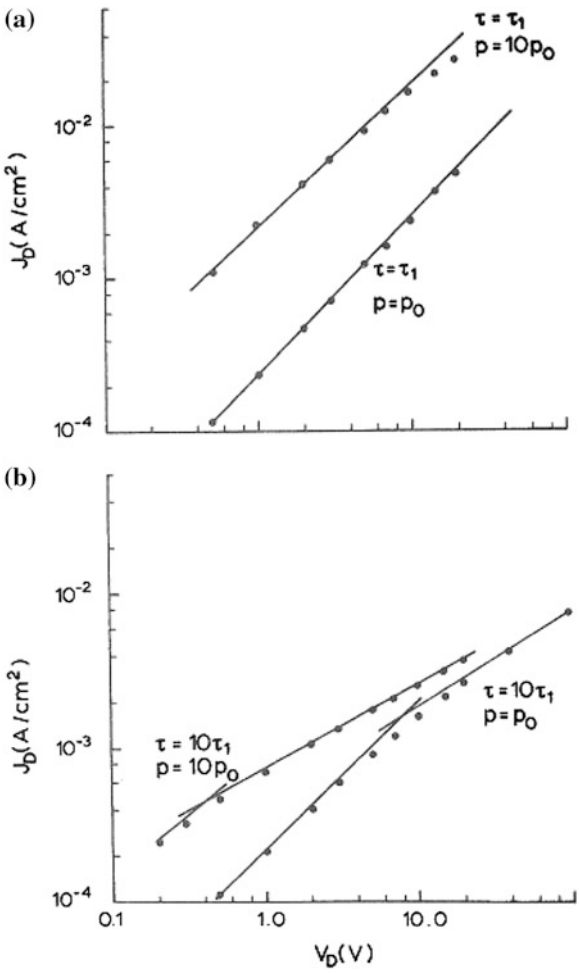

Fig. 8.12 Calculated leakage current curves, J_D-V_D, using Eq. 8.29 **a** low generation lifetime case, $\tau_1 = 10^{-11}$s, and **b** higher lifetime, $\tau = 10\tau_1$ (Reprinted from [9] Copyright (1991), with permission from Elsevier)

data in Fig. 8.10a and b. Some representative calculations are shown in Fig. 8.12a and b, using the parameter values shown in the figure caption. The curves in Fig. 8.12a have been calculated with a low value of the carrier generation lifetime, corresponding to a high DOS near mid-gap, and for two different values of the hole concentration, corresponding to two different degrees of hole accumulation. Under these conditions, the I_D-V_D characteristics are linear, and increasing the hole concentration by a factor of ten increases the current by the same amount. These curves are similar to the experimental ones in Fig. 8.10a. In this case, the junction is not rectifying because the potential electron–hole pair generation rate is so high, that the current flow through the device is not limited by this generation process, but by the transport of holes to the source junction (where it is implicitly assumed that they recombine with electrons). Hence, there is drift-limited conduction, and the resistive current is simply determined by the hole concentration in the film.

In contrast, the curves in Fig. 8.12b were calculated with a ten times higher generation lifetime, and showed the same general form as the experimental data in Fig. 8.10b. The curves had a linear I_D-V_D characteristic only at low values of V_D, and, eventually, the slope reduced to 0.5, when the current became generation rate limited. The slope of 0.5 occurred because the increase in size of the space charge region, within which generation took place, increased only with the square root of V_D, as shown in Eq. 8.26. In this case, the higher lifetime reduced the carrier generation rate, and, as V_D increased, the holes were swept away at an increasing rate, until the generation rate at the drain could not sustain this current flow. When this happened, the current became limited by the generation rate at the drain. It will also be seen that when the hole concentration increased by a factor of ten, the transition from a drift-limited to a generation-limited current occurred at a lower value of V_D. This is because, with the higher hole concentration, there was initially a 10 times higher drift current, which had to be sustained by the generation rate at the drain; but, as V_D increased, the generation rate quickly became insufficient to supply this increasingly large current, and the process became generation rate limited at the lower value of V_D.

As seen above, the simple analytical model in Eq. 8.29 provides physical insight into the low-field leakage current behaviour of poly-Si TFTs, and it can be used to explain the bell-shaped leakage current curves of ELA poly-Si TFTs, as discussed in Sect. 7.2.2.3 and shown in Fig. 7.8. The leakage current curves, as a function of ELA energy density, for L = 6 μm and L = 60 μm TFTs, from a 40 nm thick film [21], are shown in Fig. 8.13. These display the bell-shape already referred to, and, at low ELA energies, the currents scaled inversely with channel length, but were almost independent of channel length at high laser energies. This indicates that, at low energies, and high DOS, the leakage currents were drift-limited, and at high energies, and low DOS, became generation rate limited. In order to model this transition with Eq. 8.29, it is necessary to use the changing

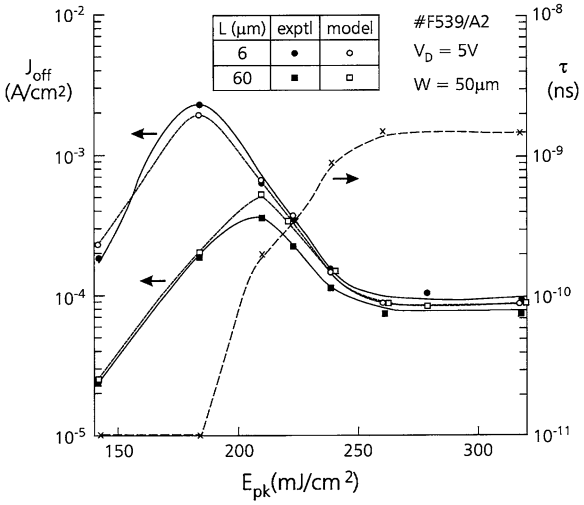

Fig. 8.13 Experimental and modelled (Eq. 8.29) leakage current characteristics, as a function of TFT channel length and ELA energy density, using the generation lifetime, τ, as the adjustable parameter (Reprinted from [21] Copyright (1999), with permission from Elsevier)

values of measured hole mobility as the ELA energy density increased, and this was done in the fitted curve in Fig. 8.13. In fitting this curve to the data, the generation lifetime, τ, was an adjustable parameter, and the values plotted against the right hand axis show, as expected, a monotonically increasing lifetime with increasing ELA energy density. Hence, the initial rise in leakage current with energy density was due to the increasing carrier mobility in the drift-limited arm of the curve, but, at the same time, the generation lifetime was increasing with energy density, leading eventually to a transition to generation-limited currents. Once the current became generation rate limited, it fell with increasing energy density as the lifetime increased due to the reduced DOS in the high quality, optimally crystallised material.

8.5 Performance Artefacts and Drain Field

Three major performance artefacts have been identified even in low DOS, high quality poly-Si TFTs, and these have been associated with high drain fields in the devices. Firstly, the off-state current increases exponentially with both gate and drain bias, as seen in Figs. 8.9c and 8.10c, respectively. Secondly, n-channel TFTs are subject to drain bias stress instability, as shown in Fig. 8.14, and, finally, the output characteristics show poor current saturation, as seen by the insert in

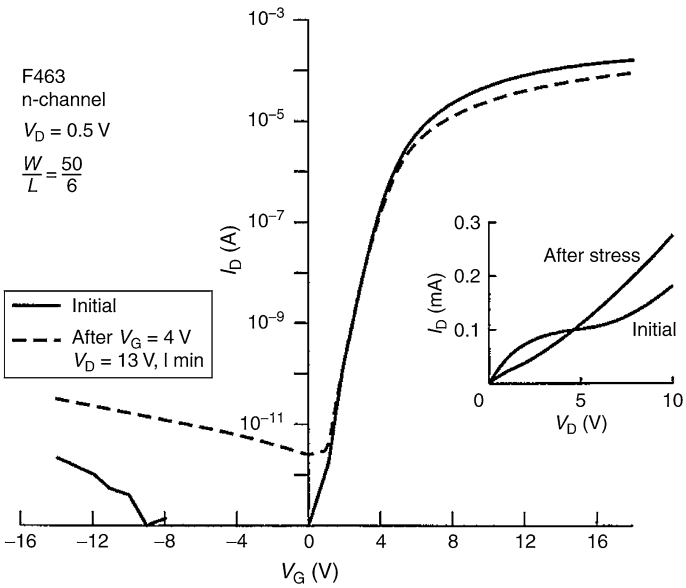

Fig. 8.14 Influence of drain bias stress of 13 V for 60 s on NSA TFT transfer characteristic. The insert shows its effect upon the output characteristic (Reprinted with permission from [24]. Copyright (1998) The Japan Society of Applied Physics)

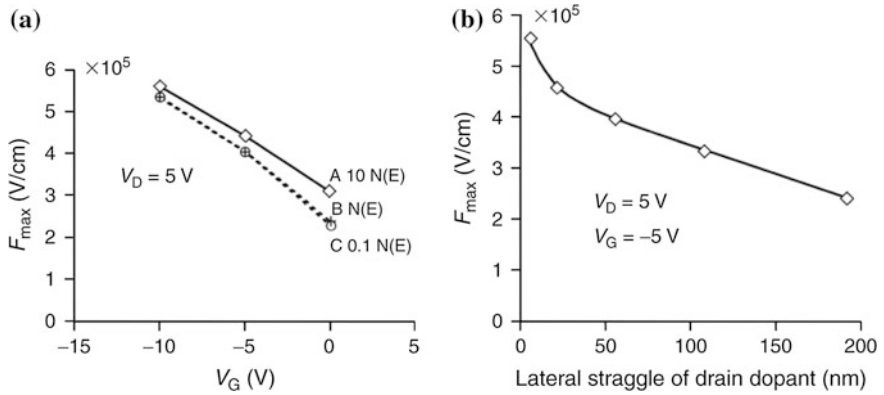

Fig. 8.15 Simulations of the maximum field at the drain/channel junction as a function of **a** gate bias and poly-Si DOS (56 nm lateral dopant spread), and **b** lateral spread of drain dopant. (The DOS, N(E), gave a TFT with a sub-threshold slope, S, of 1 V/dec). (Reprinted with permission from [22]. Copyright (1996) American Institute of Physics)

Fig. 8.14. The details of the instability process and the leakage current effects are discussed further in Sects. 8.5.2 and 8.5.3, respectively, whilst the electrostatic drain field itself is discussed in Sect. 8.5.1.

8.5.1 Electrostatic Drain Field, F

The 2-D electrostatic field in the space charge region of a semiconductor junction is given by Poisson's equation, which relates the space charge density, N_{sc}, and field, F:

$$\frac{\partial F_x}{\partial x} + \frac{\partial F_y}{\partial y} = -\frac{qN_{sc}}{\varepsilon_s \varepsilon_0} \tag{8.30}$$

Using a 2-D simulator, evaluation of this expression, for poly-Si TFTs, showed that the differential terms were opposite in sign, and both were much larger than the space charge term on the right side, such that their difference was only ~10–20 % of their absolute values [22]. Thus, the internal electrostatic field was not controlled by the poly-Si density of states, DOS, as it would be in a 1-D analysis. This is shown in Fig. 8.15a, in which the maximum drain field was calculated as a function of gate bias, with the poly-Si DOS as a scaled independent parameter [22]. In this diagram, the different DOS values produced sub-threshold slopes of 3.0, 1.0 and 0.3 V/dec in the simulated TFT transfer characteristics (for a gate oxide thickness, t_{ox}, of 0.15μm). To put those slopes into context, a high quality poly-Si TFT would have a sub-threshold slope of 0.4 V/decade for this oxide thickness. Therefore, for TFTs of practical interest, with a sub-threshold

slope of < 1 V/dec, the DOS would have no significant effect upon the drain field in the off-state and sub-threshold regime, although there was a weak dependence of drain field on trap state density at large positive V_G, when the device was turned on [24]. However, as shown in the next section, the on-state hot carrier degradation was, nevertheless, greater in the low DOS device.

The simulations showed that the drain field was a 2-D effect, and was determined primarily by the combined effects of the drain and gate biases, the oxide thickness, and the lateral distribution of the drain dopant at its edge [22, 24]. This latter point is shown in Fig. 8.15b, demonstrating that the more abrupt the junction is, the greater is the peak field. The 2-D dependence upon gate bias and oxide thickness meant that, as the transverse gate field increased, so did the lateral drain field, so that, for example, reducing the oxide thickness will increase the drain field.

Because of the significance of the lateral dopant distribution, the drain field in NSA TFTs decreases with increasing ELA shots (due to lateral diffusion of the drain dopant) [23], and, equally, the drain field in SA TFTs is likely to be larger than in NSA TFTs (due to reduced lateral diffusion in the former).

As the poly-Si quality itself had little effect upon the magnitude of the drain field, a change in architecture was required to produce a greater lateral dopant spread, and this is most readily accomplished through the use of lightly doped drain (LDD) regions, the fabrication of which was discussed in Sect. 7.4.1.2. It is worth noting that similar high drain field effects occur in MOSFETs, and these also routinely incorporate LDD regions for field relief.

8.5.2 Hot Carrier Damage and LDD

The high drain field, combined with the high electron mobility, leads to carrier heating and the generation of additional electron–hole pairs by impact ionisation. These additional carriers contribute to the poor saturation of the output characteristics of poly-Si TFTs, and to the so-called ‘kink’ effect when the impact ionisation-induced avalanche currents ultimately dominate the current flow [25, 26]. The impact ionisation, underlying the ‘kink’ effect, is enhanced by parasitic bipolar transistor (PBT) action in the floating body of the TFT [25], and this effect increases with reducing channel length [27]. Further discussion of PBT action is presented in Sect. 8.7, dealing with short channel effects.

The impact of hot carrier damage (HCD) on n-channel TFT transfer characteristics has already been shown in Fig. 8.14, and the changes in both on-state and off-state currents are attributed to the creation of localised electron trapping centres near the drain junction. Also shown by the inset is the change in output characteristics as a result of the HCD: at low drain bias, there is reduced drain current (compared with the unstressed sample) due to the high resistance of the channel near the drain, and, at large drain bias, there is a higher drain current due to the negatively charged trapping states increasing the drain field, and, hence,

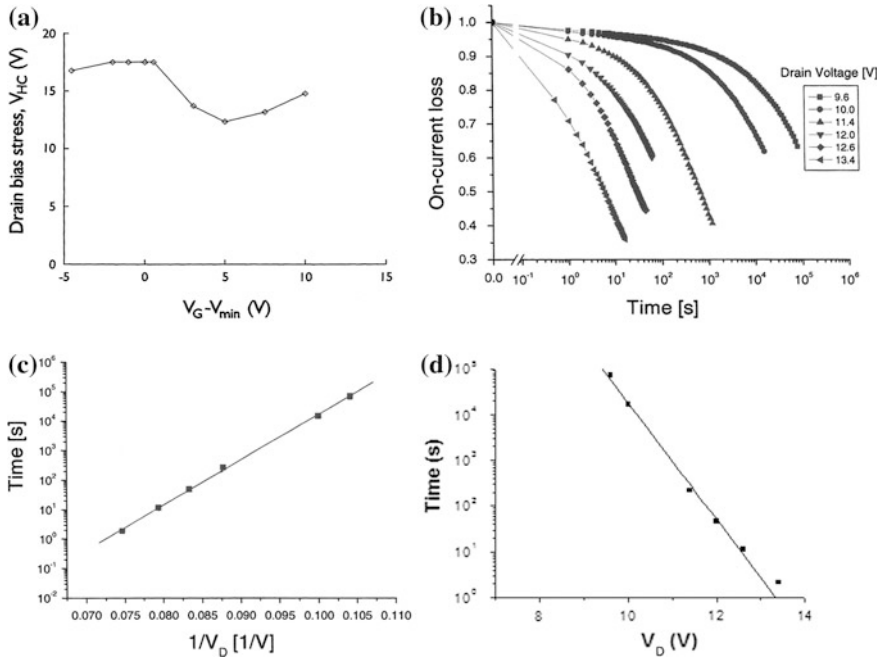

Fig. 8.16 Hot carrier instability effects in NSA TFTs **a** inter-dependence of gate and drain biases for a 30 % reduction in on-current after 60 s stress (L = 6 μm and t_{ox} = 150 nm), **b** variation of on-current degradation with drain bias and stress time (L = 4 μm and t_{ox} = 40 nm), **c** device lifetime (for 30 % on-current loss) versus $1/V_D$, and **d** device lifetime versus V_D. (**a** Reprinted with permission from [24]. Copyright (1998) The Japan Society of Applied Physics)

increasing the avalanche generation rate [28]. Some typical examples of the dependence of the hot carrier instability on gate and drain bias, and stress time, are shown in Fig. 8.16a–d. The 'spoon-shaped' gate and drain bias dependence in Fig. 8.16a is characteristic of the hot-carrier instability, and is discussed further below. The change in on-current in Fig. 8.16b can be used to empirically determine device lifetime, where unacceptable performance can be defined to occur at a given reduction in on-current, such as 30 % [26]. As will be seen in this figure, the stress time needed for a given loss of on-current reduced logarithmically as the drain bias increased. This strong dependence essentially occurred once the drain bias caused the device to go into weak avalanching, and, within this regime, there was an approximately exponential relationship between device lifetime and drain bias. Indeed, from Eq. 8.33 below, the logarithm of this time should scale with reciprocal drain bias, as seen in Fig. 8.16c, and the plot can be extrapolated to determine the maximum drain bias to achieve a given device lifetime. An approximately linear plot can also be obtained directly against drain bias [26], as shown in Fig. 8.16d, and the 0.78 V/dec slope of the fitted line is an empirical measure of the relationship between lifetime and drain bias. This indicated that for each 0.78 V increment in drain bias, the device lifetime decreased by one decade.

The value is specific to this NSA device ($L = 4$ μm, $t_{ox} = 50$ nm), and it will change with device geometry and architecture, so that, for instance, SA devices, with more abrupt junctions, will typically have greater slopes, demonstrating a stronger dependence of lifetime on drain bias. For example, 1μm channel length SA TFTs, with 50 nm thick gate oxides, had a drain bias dependent lifetime of 0.32 V/dec.

Hot carrier damage has been extensively studied in c-MOSFETs, and the damage centres were identified as acceptor states at the Si/SiO_2 interface, as well as positively charged states in the gate oxide itself. From the dependence of these densities upon the gate bias, during drain bias stress, it was concluded that both hot-electron and hot-hole injection into the oxide had to take place, and that the generation of interface traps resulted from a two-stage process of hole capture at oxide traps near the interface and subsequent recombination with injected electrons [29]. It is likely that the recombination energy released by electron capture could break weak interface bonds. There is injection of both carrier types because, under the normal bias-stress conditions of $V_D > V_G$, there is field reversal in the oxide near the drain junction, which promotes hole injection. In spite of this field reversal, significant electron injection can also take place against the field if the hot electron is within a scattering distance of the Si/SiO_2 interface [29].

In analogy with these HCD effects in MOSFETs, the poly-Si damage centres have been widely attributed to states at the poly-Si/SiO_2 interface [24, 26, 28, 30], or, in analogy with defect creation in a-SiH TFTs, attributed to bulk states in the poly-Si [31]. In both cases, good fits were obtained between simulation models and the experimental characteristics, but the latter conclusion was based partly upon the observation of damage at the back of the film. However, subsequent simulation work showed that, even with top gated devices, damage centres are produced at both the front and back interfaces [28, 32].

As mentioned in Sect. 7.4.1.2, the problem of hot carrier damage can be reduced by the use of field relief regions, such as lightly doped drain, LDD, and gate-overlapped lightly doped drain, GOLDD (shown in cross-section in Fig. 7.32), and, by and large, lower doping levels give better field relief. However, dose optimisation for field relief using LDD structures involves a compromise with series resistance and reduced on-current [32]. In contrast, optimisation of dopant concentration in GOLDD structures involves almost no compromise with series resistance in the on-state, although there will be some current reduction due to the increased channel length to accommodate the GOLDD region. Less obviously, the GOLDD structure also gave significantly better field relief, as shown by the comparison of the bias-stress results in Fig. 8.17a–d. In the GOLDD device (Fig. 8.17c), there was almost no reduction in the drain current after a 30 V drain bias stress, compared with the 10–100 times reduction in the LDD device after 10 V stress. There was also no degradation in the output characteristic at low V_d, and the characteristic second saturation regime in the GOLDD TFTs was reduced by the stress [32].

These differences have been explained by applying the MOSFET HCD model to poly-Si TFTs [32], in which the simulated carrier densities and fields in the TFT

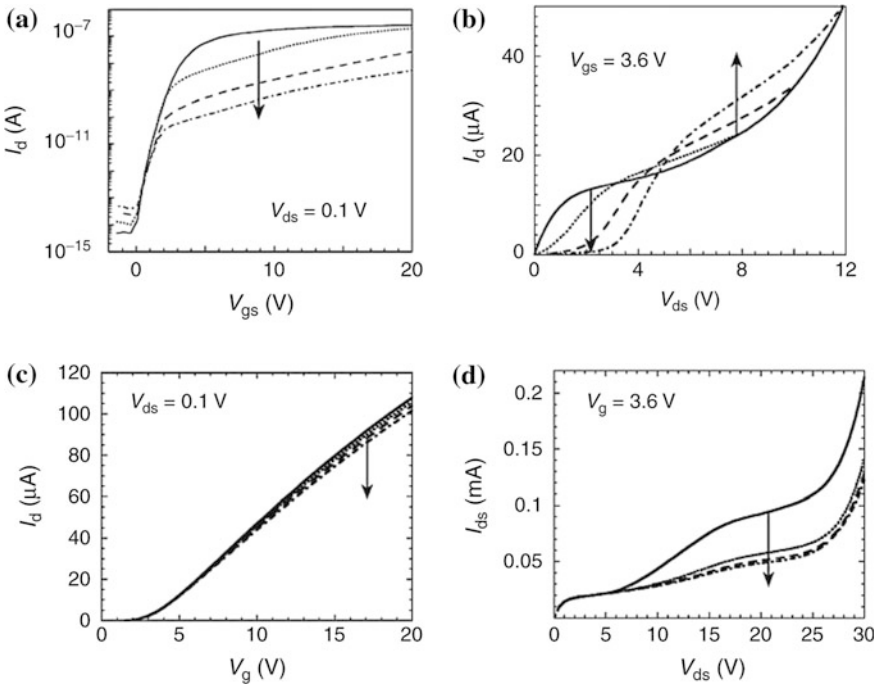

Fig. 8.17 Experimental measurements before and after drain bias stress—*arrows* indicate direction of changes **a** transfer characteristic, and **b** output characteristics of LDD TFTs after drain bias stress at 8, 10 and 12 V for 5,000 s (LDD dose = $1x10^{13}$ P/cm^2), **c** linear transfer characteristics, and **d** output characteristics of GOLDD TFTs after drain bias stress at 30 V for 75, 1,270 and 10,000 s (GOLDD dose = 5×10^{12} P/cm^2). (Reprinted from [32] with permission of IEEE)

were used to model the hot-carrier injection currents into both the top and bottom oxide layers by using the 'lucky electron' model [33]. The hot-electron injection current is given by [32]:

$$J_e(x) = A \int n(x,y) P_e(y) dy \tag{8.31}$$

and the electron injection probability, $P_e(y)$, is given by [33]:

$$P_e(y) \propto \exp - \frac{y}{\lambda} . \exp - \frac{\Phi_b}{F_x \lambda} \tag{8.32}$$

(The x direction is parallel to the semiconductor/insulator interface, and y is perpendicular to it). Φ_b is the zero field oxide barrier height, and λ is the electron mean free path. The first term in Eq. 8.32 describes the probability of an electron, at depth y in the poly-Si, travelling to the interface without an inelastic collision, and the second term is the probability of the hot-electron having enough energy to

surmount the barrier Φ_b. A similar expression holds for hole injection, and the barrier height for electrons (holes) is 3.1 eV (4.7 eV), and the electron (hole) mean free path is 6.5 nm (4.7 nm).

The 'lucky electron' model has also been used to empirically predict device lifetime, τ, [34], by arguing that the device degradation will be determined by the flux of injected hot carriers, which will be proportional to the normalised channel current, I_D/W and the hot carrier injection probability. The expression for τ was given by [34]:

$$\tau = C\frac{W}{I_D}\exp\frac{\Phi_b}{F_x\lambda} \tag{8.33}$$

where C is a constant. Using device simulation, this expression has been evaluated to investigate the gate bias and trap state density dependence of the device lifetime in poly-Si TFTs [24]. The calculated lifetime, as a function of gate bias (with $V_D = 15$ V), is shown in Fig. 8.18, for two values of trap state density. It will be seen that this expression predicts the 'spoon-shaped' dependence on gate bias, as seen in the experimental data in Fig. 8.16a, where the worst-case stress condition is approximately at $V_G = V_T$. The simple physical explanation for this effect is that, up to this gate voltage, the electron surface density (and current) has been increasing exponentially with gate bias, which more than compensates for the reducing drain field. For gate bias values greater than V_T, the electron concentration only increases linearly with gate bias in inversion, and the corresponding, linearly increasing current is not sufficient to compensate for the reducing drain field due to the increasing value of $V_{D(sat)}$. Secondly, it will be seen that the worst-case lifetime is slightly worse in the low DOS device, further reinforcing the earlier argument that improvements in basic poly-Si material quality will not reduce HCD effects.

Using Eq. 8.32, within a 2-D simulator, the device characteristics in Fig. 8.17 have been reproduced [32]. From the calculated hot-carrier injection currents, and

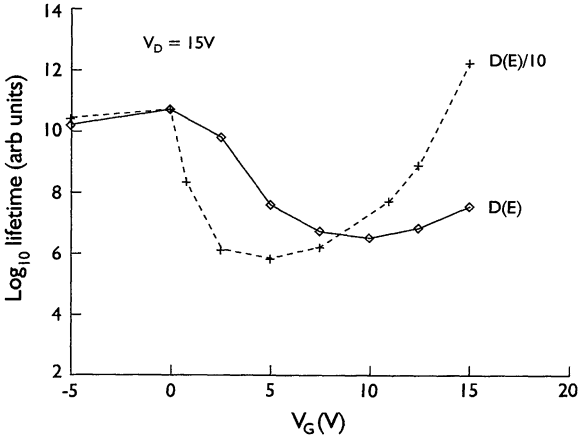

Fig. 8.18 Calculated dependence of relative hot-carrier device lifetime on gate bias, using a 2-D simulator to evaluate Eq. 8.33 (drain bias was 15 V). (Reprinted with permission from [24]. Copyright (1998) The Japan Society of Applied Physics)

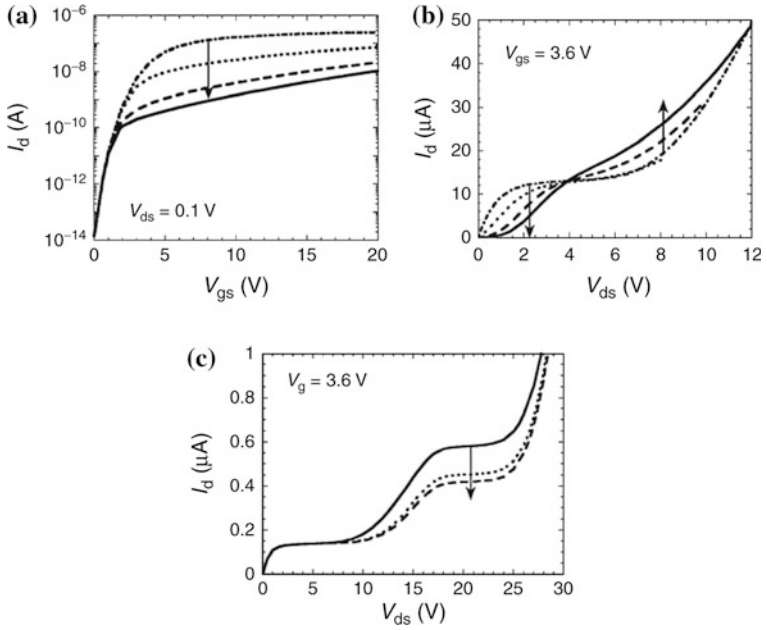

Fig. 8.19 Simulated characteristics before and after drain bias stress—arrows show direction of changes from un-stressed states **a** transfer characteristic, and **b** output characteristics of LDD TFTs following stress at 8 V, 10 V and 12 V for 5,000 s (LDD dose = 1×10^{13} P/cm^2), **c** output characteristics of GOLDD TFT following 23 V stress for 323 and 10,000 s (GOLDD dose = 5×10^{12} P/cm^2). (Reprinted from [32] with permission of IEEE)

the ensuing two stage carrier recombination process within the oxide, the positive charge density (due to trapped holes in the oxide) and the negative charge in interface states was calculated iteratively with time, so that, as these charges built up, their effect upon the field and current distribution in the poly-Si was re-calculated, which then altered the trap generation rates [32].

Figures 8.19a and b show the simulated I_d-V_G and I_d-V_{ds} plots for the LDD devices, and Fig. 8.19c shows the I_d-V_{ds} plot for the GOLDD device. In all cases, these results accurately reflect the experimental data in Fig. 8.17. For the LDD structure, acceptor trap generation started at the channel/LDD interface, where the field was at a maximum. With increasing time and V_{ds}-stress, the trap generation spread into the adjacent channel and LDD regions, at both the top and bottom poly-Si/SiO_2 interfaces. The positive trapped charge started in the same location, but finished up as a bi-modal distribution either side of the high field point. The negative charge in the interface states dominated, and constricted the electron channel current near the drain into the centre of the film. This formed a resistive bottleneck, which was responsible for the loss of on-current [32]. For the GOLDD structure, the generated interface state densities were lower than in the LDD structure, and the positive trapped charge was largely generated near the top Si/SiO_2 interface. This partially compensated the negatively charged interface

states charges at this interface, and resulted in the uncompensated negatively charged traps at the back interface having the greatest net effect. As a consequence of this distribution, the effect of the hot carrier damage on the low V_{ds} on-current near the top interface was minimal. At large V_{ds}, the current was deflected away from the top interface, but the large negative charge density at the back interface maintained the current flow more centrally within the film [32], and this reduced the impact ionisation rate in the second plateau region of the GOLDD TFTs, as seen in Figs. 17d and 19c [32, 35].

As shown, the GOLDD architecture gives significantly better hot carrier stability than the simpler LDD region, but, as with the non-self-aligned architecture, it increases the parasitic capacitance between gate and drain, and the choice of LDD architecture will be dictated by the trade-off in speed and high voltage stability requirements. As discussed in Sect. 7.4.1.2, a sub-micron GOLDD region would be needed for short channel devices, and this has been demonstrated with a conducting spacer technology [36].

P-channel TFTs, in common with p-channel MOSFETs, are far less susceptible to HCD [24, 26], and both MOSFET [37] and TFT [38] results have been successfully modelled with only electron injection. In view of this, there does not seem to be a unified HCD model using the same injection conditions for both n- and p-channel TFTs.

Other instability effects in poly-Si TFTs, over and above HCD, are discussed in Sect. 8.6.

8.5.3 Field-Enhanced Leakage Currents

High quality poly-Si TFTs, when biased in the off-state, show a leakage current characteristic, which is channel length independent, as shown in Fig. 8.9c, and which increases exponentially with both gate and drain bias, as seen in Figs. 8.9c and 8.10c, respectively [20]. The channel length independence indicates a current, which is limited by electron–hole pair generation processes at the drain, rather by resistive flow through the body of the device (which would scale inversely with channel length). However, normal thermal generation processes would produce currents, which have only a square root dependence on drain bias, and an even weaker dependence on gate bias. Hence, these anomalously large currents are described as field-enhanced currents, and Fig. 8.20 schematically shows the range of electron emission processes, which can be expected in the space charge region of a reverse biased junction. As discussed in Chap. 2, the basic leakage current mechanism is controlled by sequential electron and hole emission from deep traps near the centre of the band-gap, and, for simplicity, Fig. 8.20 shows only the electron emission processes to the conduction band. There will be equivalent hole emission processes to the valence band.

At low fields and high temperatures, simple thermal emission (with no field dependence) will dominate, giving drain current activation energies of $\sim E_G/2$. At

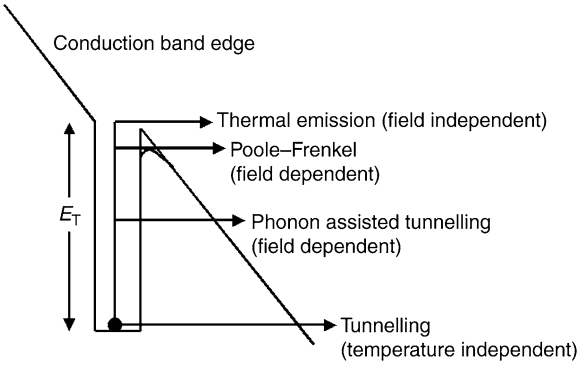

Fig. 8.20 Schematic illustration of electron emission processes into the conduction band from a trap at depth E_T. The trap is located within a reverse biased space charge region

high fields and low temperatures, tunnelling will dominate giving near-zero activation energies. Between these two extremes, two further processes are shown, which are the field-induced lowering of the emission barrier for a Coulombic centre (the Poole–Frenkel effect), and thermal emission to a virtual state followed by tunnelling (phonon assisted tunnelling), both of which are field dependent.

Experimental results, near room temperature, showing thermal activation energies decreasing from $\sim E_G/2$ with increasing V_D [22] and V_G [39] rule out pure tunnelling, and the best fits to the data have been with phonon assisted tunnelling [7, 22, 39–41], although, at the highest biases, band-to-band tunnelling is also significant [40, 41]. The phonon assisted tunnelling can be represented as a field dependent enhancement, $e_n(F)$, of the low-field electron thermal emission rate, e_{n0}, by:

$$e_n(F) = e_{n0}\gamma(F) \tag{8.34}$$

The field enhancement factor, $\gamma(F)$, for a discrete Coulomb centre at E_T, is given by [42]:

$$\gamma(F) = \exp\frac{\Delta E_T}{kT} + \frac{q}{kT}\int_{\Delta E_T}^{E_T} \exp\left\{\frac{E}{kT} - \frac{4E^{1.5}(2m^*q)^{0.5}}{3\hbar F}\right\}\left\{1 - \left(\frac{\Delta E_T}{E}\right)^{5/3}\right\}dE \tag{8.35}$$

where, ΔE_T is the emission barrier lowering due to the Poole–Frenkel effect, and this will be zero for a Dirac centre.

The simplified expression for a Dirac centre can be approximated by [42]:

$$\gamma(F) \approx \frac{2\pi^{0.5}q\hbar F}{(kT)^{1.5}2(2m^*)^{0.5}}\exp\left\{\frac{1}{3(kT)^3}\left(\frac{q\hbar F}{2(2m^*)^{0.5}}\right)^2\right\} \tag{8.36}$$

The exponential term in the above expression is quadratic in F, and the depletion approximation relates the maximum field to the drain bias by $F_{max} \propto$

$V_d^{0.5}$, so that this simplified expression correctly predicts the observed exponential dependence of leakage current on drain bias.

The field-free thermal emission rate, e_{n0}, is given in Chap. 2 by:

$$e_{n0} = v\sigma_n N_C \exp -\frac{E_T}{kT} \tag{8.37}$$

where σ is the electron capture cross section, v is the electron thermal velocity and N_c is the effective density of conduction band states.

Equivalent expressions for $e_p(F)$ and e_{p0} can also be formulated for the hole emission rates, and the leakage current density is given by integration across the drain space charge region, of width d:

$$J = qN_T \int_0^d \frac{e_n e_p}{e_n + e_p} dx \tag{8.38}$$

Although the preceding expressions are for a discrete trap, and the poly-Si DOS is distributed across the band-gap, current generation processes, via electron–hole pair emission, are localised on near-mid-gap centres. This is in order to minimise the sum $e_n + e_p$, and this process can be reasonably accurately represented by discrete near-mid-gap states. In numerical simulations of the leakage current process, the full trap distribution was used [40, 41], and the results remain consistent with the above qualitative considerations, although it has been shown that, at high fields, the most efficient generation centres can be up to 50 meV off mid-gap [43] due to the Poole–Frenkel effect. An interesting aspect of those calculations was the observation that, for distributed traps, the current can be limited by emission from the Coulomb state of the centre, located slightly deeper than $E_G/2$, whereas, for a discrete trap at $E_G/2$, the current would normally be limited by the slower emission from the Dirac state of the centre.

As with the hot carrier instability, the field enhanced leakage currents are a direct consequence of the high drain fields in poly-Si TFTs, and field relief at the drain, using LDD or GOLDD regions, will also reduce these field-enhanced currents [24, 41]. Although the DOS values in high quality TFTs will not influence the drain field itself, the magnitude of the currents will scale with the trap density near mid-gap, and, hence, with the DOS values near mid-gap. Also, in common with the hot carrier instability, field enhanced leakage currents are observed in MOSFETs [44], and are not specific to poly-Si TFTs.

8.6 Other Bias-Stress Instabilities

Section 8.5.2 dealt with hot carrier induced instability, which is at a maximum when high drain-bias-stress is combined with a low gate-bias setting approximately equal to the threshold voltage [23, 24]. Other important bias-stress

combinations are high gate bias without drain bias, and combined high gate and high drain bias.

8.6.1 Gate Bias Stress

8.6.1.1 Ionic Instability

In common with MOSFET technology, alkali ion contamination, particularly sodium, has to be avoided, as, under the influence of positive gate bias-temperature stress, negative threshold voltage shifts occur in poly-Si TFTs. The specific ion contaminant can be identified from its characteristic ion current signature observed during a gate bias sweep at 250 °C [45].

Gate bias stress can also result in threshold voltage shifts, due to charged ion movement, in porous, poor quality gate oxides [46]. As discussed in Sect. 7.3.1, the absorption of water in these films has been identified by characteristic thermal desorption spectroscopy peaks at 100–200° C [47], and the presence of H^+ and OH^- ions in the oxide has led to both negative and positive threshold voltage shifts after positive and negative bias-stressing, respectively [46]. However, current state-of-the-art gate oxide films, formed by PECVD deposition from either oxygen-diluted tetraethylorthosilicate, TEOS [47], or helium-diluted silane and nitrous oxide [48, 49] have deliberately employed dilution conditions to reduce the oxide deposition rate, and to deposit dense, low porosity oxides, which are free from water-induced instabilities.

8.6.1.2 Negative Bias-Temperature Instability

NBTI has been widely studied in MOSFET devices, where it is particularly seen in p-channel transistors stressed with negative gate bias (< 6MV/cm) at elevated temperatures of 100–250 °C [50]. The stress causes an increase in the absolute magnitude of threshold voltage, as well as degradation of sub-threshold slope and g_m. These changes are negligible under comparable positive bias-stress conditions, and also negligible with both positive and negative gate bias-stress in n-channel MOSFETs. The changes in device characteristics have been attributed to a combined increase in trapping states at the Si/SiO_2 interface, as well as positive charge in the gate oxide. The physical model for the trapping state change is the dehydrogenation of previously passivated Si dangling bonds at the interface, although the detailed process whereby this occurs, together with the increase in oxide charge, is still a matter of discussion, with different models invoking the role of mobile hydrogen ions or holes [50].

Similar instabilities have been reported in a wide range of p-channel poly-Si TFTs, made from directly deposited LPCVD poly-Si, solid phase crystallised [51, 52] and excimer laser crystallised material [53–55]. In most of this work [51–53],

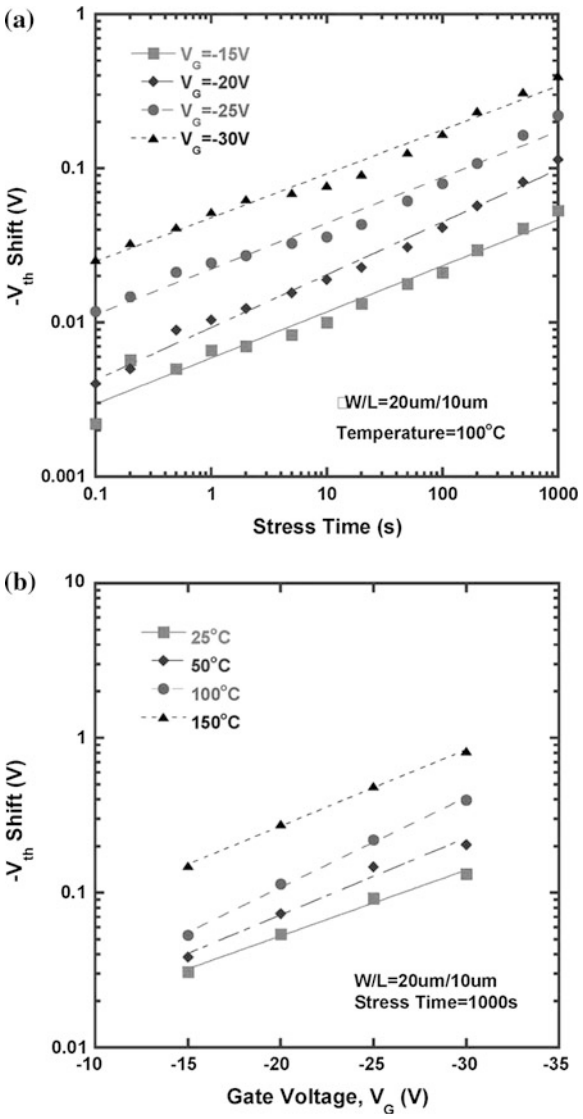

Fig. 8.21 Threshold voltage instability of p-channel poly-Si TFTs with negative gate bias temperature stress (NBTI) **a** time dependence at different gate biases, **b** gate bias dependence at different temperatures (Reprinted from [53] with permission of IEEE)

the increase in threshold voltage was thermally activated over the temperature range 297–430 K, with a power dependence on stress time, and an exponential dependence on gate bias stress, as shown in Fig. 8.21 [53]. This dependence was empirically represented by:

$$\Delta V_T \propto t^n \exp(-E_a/kT) \exp(C|V_G|) \tag{8.39}$$

where n was 0.28–0.34, E_a was $\sim$0.14 eV, and C was a fitting parameter whose value was $\sim$0.1–0.13. The power time dependence was qualitatively similar to

that reported in MOSFETs [50], although the gate bias dependence differed between authors. In the MOSFET work, there was a power dependence of $E_{ox}^{1.5}$ (where $E_{ox} = \{V_G\text{-}V_{FB}\text{-}\Psi s\}/t_{ox}$), rather than an exponential dependence. In other TFT work, there was a linear dependence of ΔV_T on E_{ox} above a critical oxide field of 0.5MV/cm [54, 55].

Notwithstanding some of the differences with the MOSFET data, the TFT results have been broadly interpreted in the same way: namely, by an increase in positive oxide charge, and an increase in trapping state density [55]. In one case [53], the change in sub-threshold slope of the I_d-V_G characteristic was attributed to interface state generation, and the near-threshold part of the characteristic was analysed using the Levinson method [5], and identified an increase in the GB trapping state density. However, as discussed in Sect. 8.3, all trapping states can be represented by an effective density per unit surface area, and identifying the specific physical location of the traps can be difficult. In other work on NSA TFTs [54], numerical simulation of the characteristics after NBTI could satisfactorily account for the NBTI changes by the introduction of an exponential distribution of Si/SiO_2 interface states, $N_{ss}(E)$, without any increase in positive oxide charge. In contrast, SA TFTs showed linear increases in both N_{ss} and oxide charge with E_{ox} [55].

In summary, NBTI is a well documented instability process in p-channel poly-Si TFTs, which has been interpreted in terms of an increase in trapping states in the material, where the state location has been attributed to both Si/SiO_2 interface states as well GB states, and the change in oxide charge seems to be sample dependent.

8.6.2 Combined Gate and Drain Bias Stress

The combination of high gate and high drain bias-stress results in a large current flow through the device, and this can lead to self-heating induced instabilities [55–61], in which the modulus of the threshold voltage of both n-channel and p-channel TFTs increased with increasing bias stress. In addition to the increase in threshold voltage, a decrease in on-current, an increase in off-current, and a degradation in sub-threshold slope have also been observed [56].

As might be expected, the self-heating effects, induced by different combinations of gate bias and drain bias, were best represented by the stress-power dissipation ($= I_d \times V_d$) within the device, and, for a given device geometry, the bias-stress threshold voltage shifts could be uniquely correlated with this power dissipation, as shown in Fig. 8.22 [56]. The self-heating effects have been confirmed by both direct infra-red detector measurements of the surface temperature of the device [56, 58], as well as by numerical simulations of Joule heating within the TFT [56, 57, 59, 61]. The measurements showed surface temperatures from $\sim$100 °C up to $\sim$250 °C, depending upon the specific device geometry and bias conditions [56, 58], and the magnitude of the bias-stress instability has been

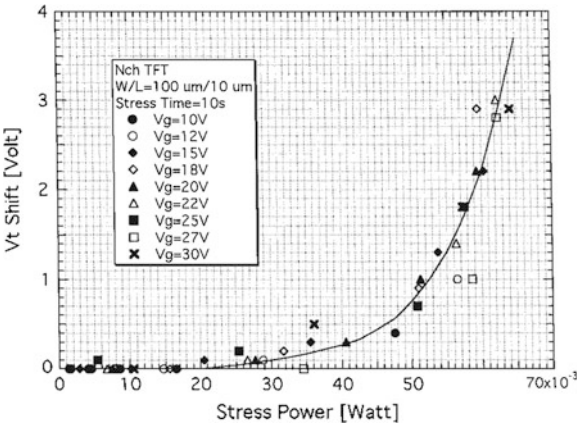

Fig. 8.22 Dependence of threshold voltage shift on stress power, where V_d was varied between 5 and 30 V, and V_G determined the drain current. Stress time was 10 s (Reprinted with permission from [56]. Copyright (2002) The Japan Society of Applied Physics)

correlated with the measured temperature of the device [56, 58], as shown in Fig. 8.23 [58]. The TFTs used for this data set had different grain sizes, resulting in increasing electron mobility with grain size. The mobility differences gave different on-currents for the same bias conditions, and the large grain devices showed the largest threshold voltage shifts after stress. However, when the results were normalised with respect to the measured device temperatures, the results, for different device geometries as well as grain size, fell upon the common curve shown in Fig. 8.23.

The device geometry was identified as a key parameter in determining the internal temperature distribution. This was because the low thermal conductivity of the glass substrate ($\sim$1.3 W/m/K) made it an inefficient route for the dissipation of heat from the TFT channel, resulting in the device edges and its top surface becoming significant channels for heat dissipation. Hence, the size of the device, and particularly the width of the channel (for a given channel length), played an important role in determining its temperature, with wider devices displaying both higher temperatures and greater stress-induced threshold voltage shifts [56, 58, 61], as shown in Fig. 8.24 [56].

In agreement with the experimental measurements, the simulations also predicted channel temperatures of $\sim$120 to $\sim$300 °C [56, 57, 59, 61], depending

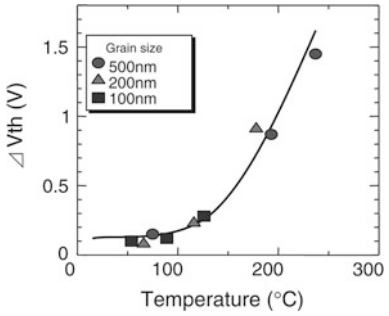

Fig. 8.23 Correlation of self-heating threshold voltage shift with device temperature for TFTs of different grain size and different channel widths (Reprinted with permission from [58]. Copyright (2005) The Japan Society of Applied Physics)

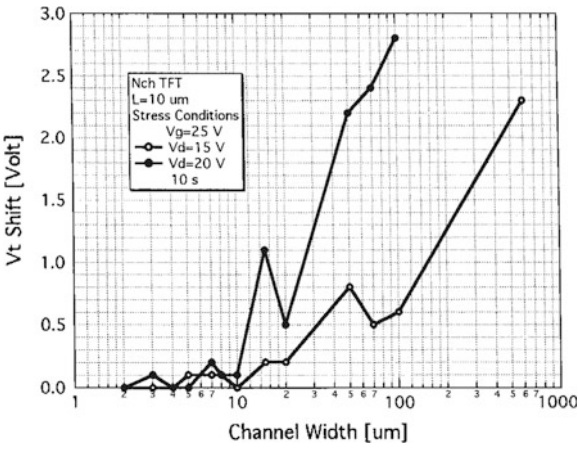

Fig. 8.24 Influence of channel width on self-heating threshold voltage shifts (Reprinted with permission from [56]. Copyright (2002) The Japan Society of Applied Physics)

upon the biasing conditions and the device geometry. In addition, the simulations demonstrated that, even when the temperature rise was not sufficient to cause bias-stress instability, it was sufficient to induce a negative output conductance in high mobility TFTs, due to increased phonon scattering of the channel electrons [59].

The threshold voltage instability has been correlated with an increase in the trapping state density either near the middle of the poly-Si band-gap [56], or at the Si/SiO_2 interface [61], and attributed to thermally-induced Si–H bond breaking either in the poly-Si grain boundaries [56] or at the interface [61]. Other workers have suggested electron injection into the gate oxide [57, 58], in analogy with hot carrier defect generation [57]. However, some of the results have been obtained at drain bias values less than the saturation voltage [56], which would keep the drain field low, and militate against hot carrier injection in those cases.

For p-channel TFTs, there is a similarity with the NBTI effects described in the preceding section, in which the drain-bias-induced self-heating plays the role of the deliberate temperature increase used to observe NBTI. Some authors have correlated the two effects, and argued that the self-heating instability is a manifestation of NBTI, in which the threshold voltage shift was found to be proportional to the oxide field, E_{ox} [54, 55] (see the discussion of Eq. 8.39). Hence, the only difference between the two effects was that, with the self-heating instability, the varying channel potential, due to the drain bias, caused a variation of oxide field, E_{ox}, along the channel, resulting in spatially non-uniform interface state and positive oxide charge creation. The device characteristics after self-heating stress were successfully simulated using the calculated values of the oxide field, E_{ox}, to fit a spatially varying interface state density and oxide charge density to the experimental characteristics [55]. The experimental and simulated transfer characteristics, before and after self-heating bias-stress, are shown in Fig. 8.25a, and, for the 10,000s stressed sample, the calculated interface state density at the source end of the channel was five times higher than at the drain end, due to the larger value of E_{ox} at the source. This spatial asymmetry in the interface state density also

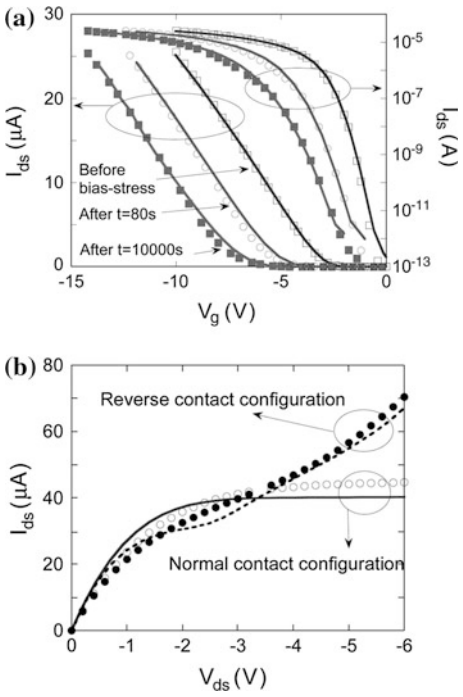

Fig. 8.25 Experimental (*symbols*) and simulated (*lines*) results of self-heating bias stress **a** transfer characteristics before and after stressing at $V_G = -15$ V and $V_d = -9$ V, and **b** output characteristics after 10,000 s stress with normal and reversed source/drain contacts (Reprinted from [55] with permission of IEEE)

successfully explained the change in output characteristics when the source and drain terminals were reversed, as shown in Fig. 8.25b. When the source terminal, with the higher interface state density was used as the drain, this higher density increased the drain field, causing a stronger avalanche current, as seen in the figure.

Whilst self-heating effects have been well established as a reliability issue in poly-Si TFTs on glass, they are a bigger issue with TFTs on flexible, polymer substrates [60, 61], where the thermal conductivity is even lower at ~0.2 W/m/K. Some common solutions have been suggested for both types of substrate, such as multi-fingered devices to avoid large W values, as well as overall device scaling to reduce both device area and drain biases, whilst retaining the required levels of channel current at lower power levels [60]. Alternatively, reduced self-heating effects have been demonstrated with thermally conducting flexible substrates, such as copper [57] or stainless steel [61] foils. The use of thin foils is discussed further in Chap. 11, which reviews the field of flexible substrate technologies for TFTs.

8.7 Short Channel Effects

Short channel effects (SCEs) have been well established, and widely studied, in c-Si MOSFETs [62], and they refer to a range of phenomena for which the

classical long channel model, described in Chap. 3, no longer applies. As channel length, L, is reduced, examples of this behaviour are a drain current, which rises more strongly than 1/L, threshold voltage, which reduces with channel length, sub-threshold currents which increase with drain bias, V_{ds}, and poor saturation in the output characteristics. These are a consequence of a number of inter-related phenomena, such as the size of the source and drain space charge regions becoming comparable to the channel length. This reduces the amount of charge needed on the gate to invert the channel surface, and decreases the threshold voltage with reducing channel length. Also, when the drain space charge region is comparable to channel length, such that the source and drain space charge regions start to overlap, increased drain bias can reduce the potential barrier between the source and the channel (drain-induced barrier lowering, DIBL), giving drain-bias-dependent sub-threshold currents and poor current saturation in the output characteristic. Strategies have been developed to minimise these effects, from simply reducing the gate oxide thickness and/or increasing the substrate doping level. Both of these changes increase the field at the drain (for a given drain bias), as discussed in Sect. 8.5.1, and reduce the spread of the space charge regions along the channel. More sophisticated changes include modifications in device design to tailor the doping level to optimise overall device performance, through to the use of field relief structures [62].

Whilst the gate length in deep sub-micron MOSFETs has been progressively shrunk to the current production values of $\sim$50 nm [63], channel length reduction in poly-Si TFTs has been more modest, with the minimum reported dimension being $\sim$0.5 μm [64–66]. Nevertheless, a variety of short channel effects have been seen in poly-Si TFTs having a channel length of 2–3 μm or less, with the effects becoming stronger as the channel length reduced. The results in the following sub-sections have been taken from SA n-channel, laser crystallised TFTs made in 40 nm thick layers of poly-Si. Some of the effects seen are classical short channel effects, such as a gate length dependent threshold voltage [67], and poor output impedance, as shown in Fig. 8.26a and b, respectively, and both can be mitigated by using a reduced oxide thickness. The threshold voltage measurements in Fig. 8.26a were made at a low drain bias of 0.1 V, and at normalised channel currents of $W/Lx10^{-7}A$, both of which were chosen to minimise other short channel effects to be discussed further below. The solid lines are simulation results derived from a double exponential DOS whose parameters were adjusted in order to give the best fit to the I_d-V_G characteristics across the range of channel lengths [67]. Both the experimental data and the simulations confirm the reduction in SCEs due to a reduced gate oxide thickness. The comparison of the I_d-V_D characteristics in Fig. 8.26b were made using different gate voltages for the two oxide thicknesses in order to normalise the measurements to common values of low field channel conductance. The TFTs with the thicker gate oxide showed very poor current saturation, compared with the thinner gate oxide samples. To quantify the effect of the thinner gate oxide, the current in saturation can be represented by [68]:

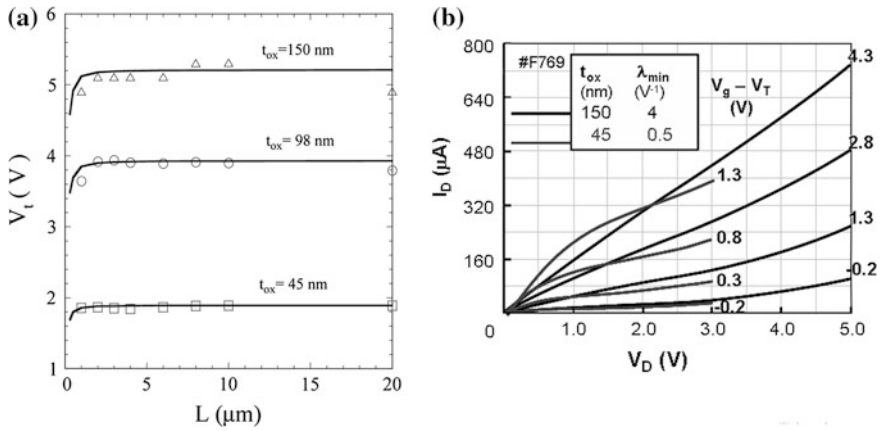

Fig. 8.26 Classical short channel effects in 1μm channel length SA poly-Si TFTs **a** variation of threshold voltage with L and gate oxide thickness (Reprinted from [67] Copyright (2005), with permission from Elsevier), and **b** comparison of output characteristics for two different gate oxide thicknesses

$$I_d = I_{do}(1 + \lambda V_d) \tag{8.40}$$

for $V_d > V_{d(sat)}$, where λ is commonly used in circuit modelling as an output characteristic quality factor, whose value is zero for devices with perfect saturation characteristics. The values for λ are shown in Fig. 8.26b, and they display an 8-fold improvement with the thinner gate oxide.

In addition to these classical effects, a number of other performance artefacts have been reported in short channel poly-Si TFTs, which have included the presence of parasitic contact resistance [65, 67, 69], the 'kink' effect in the output characteristics at high drain bias [27], and drain bias dependent sub-threshold characteristics [72]. The latter two effects are related to floating body effects in the TFTs, and will be discussed separately below. As will be apparent in that section, the floating body related SCEs have features, which are also observed in floating body SOI MOSFETs.

8.7.1 Parasitic Resistance Effects

When the linear regime channel current, in variable length TFTs, is normalised by channel length, a common curve would be expected as a function of gate bias. In contrast, the normalised currents, measured in SA n-channel TFTs, decreased with decreasing channel length, as shown in Fig. 8.27a [69]. This figure demonstrates that only the longest channel device had an approximately linear dependence of current on gate bias, and that, with reducing channel length, the expected linearity deteriorated as the currents failed to scale with 1/L. These results, together with the

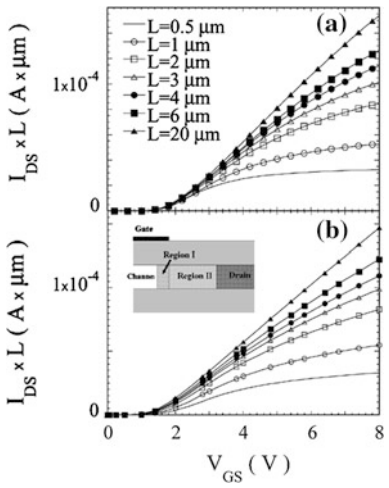

Fig. 8.27 TFT transfer characteristics, normalised by channel length **a** experimental data, and **b** simulations (also shown in the insert is the location of the ion-damaged regions in the simulation model) (Reprinted from [69] with permission of IEEE)

almost saturated nature of the L = 0.5 μm characteristic, are indicative of a parasitic resistance, R_p, in the channel. The total resistance of the device, R_{meas}, will be given by the sum of the channel resistance/unit length, R_{ch}, the doped source and drain resistance, R_n, as well as R_p, i.e.

$$R_{meas} = V_d/I_d = R_{ch}L + R_n + R_p \tag{8.41}$$

and, from a plots of $1/I_d$ versus L, at different values of V_G, the channel resistance can be calculated from the slope, and the average value of R_p across the different channel lengths can be extracted from the intercept (where R_n can be calculated from the sheet resistance of the source/drain dopant and the geometry of these doped regions). The carrier mobility can be derived from the normalised channel resistance, using the linear regime expression for TFT channel current,

$$R_{ch} = 1/\{\mu WC_{ox}(V_G - V_t)\} \tag{8.42}$$

For the TFTs in Fig. 8.27a, this analysis yielded a value of R_p which was ~600ohms [69]. For gate voltages > 6.5 V, this was more than the channel resistance of TFTs with channel lengths < 1 μm, and was responsible for the almost V_G–independent channel currents seen in the L = 0.5 μm TFTs in Fig. 8.27a.

It is significant that this effect was seen only with SA n-channel TFTs, and not with NSA n-channel TFTs nor with SA p-channel TFTs, and, as discussed in Sect. 7.4.1.1, it has been physically associated with residual phosphorus ion doping damage in the poly-Si near the edges of the gate. As also discussed in that section, the magnitude of this damage was determined by the process details, and, in modelling this effect [69], for both high and low values of R_p, it has been found appropriate to represent this damaged area by two adjacent high DOS regions, one, ~50 nm wide, immediately beneath the gate, and the other, ~200 nm wide, extending from the gate edge into the doped regions. Using this model, with DOS

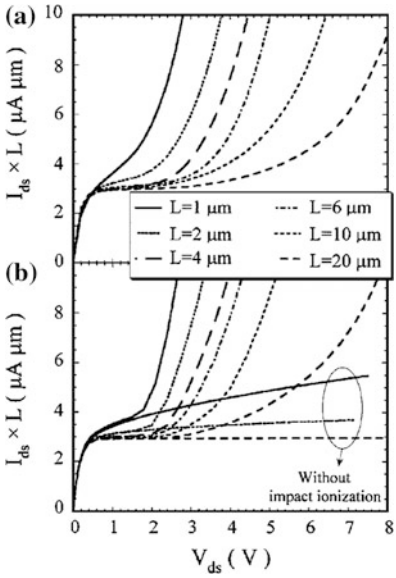

Fig. 8.28 Output characteristics for different channel length TFTs (normalised by channel length) **a** experimental data, and **b** simulations, with and without impact ionisation switched on (Reprinted with permission from [27]. Copyright (2004) American Institute of Physics)

values in region II $\sim$10 times higher than in the channel, it was successfully fitted to the experimental data as shown in Fig. 8.27b.

As is apparent, this SCE is quite different from the classical effects seen in MOSFETs, and is a consequence of the particular processing schedule favoured for SA n-channel poly-Si TFTs.

8.7.2 Floating Body Effects

8.7.2.1 Kink Effect

Figure 8.28a shows measurements of the output characteristics for a range of TFT channel lengths from L = 20 μm to L = 1 μm [27], where the characteristics have been measured at a low enough value of gate bias to avoid the parasitic resistance effects discussed in the preceding section. In this case, the linear regime currents showed good scaling with L, but the saturation currents showed a strong L dependence, with increasingly large non-saturating currents appearing at successively lower values of drain bias. In analogy with SOI MOSFETs, it is these anomalous currents, which have been referred to as the kink effect. However, in non-fully depleted SOI devices, the kink is seen as a step in the saturation current in the output characteristic [70], rather than the continuously increasing current seen in Fig. 8.28a. These latter characteristics are much more similar to the behaviour of fully-depleted SOI devices [71], in which there is not so much a step

in the saturation current, but more of a continuous increase, which has been compared to the open-base breakdown voltage in a bipolar transistor [73].

2-D simulations were used to analyse the results in Fig. 8.28a, where a double exponential DOS was established by fitting to the low V_{ds} transfer characteristics of a long channel length device, and optimised impact ionisation parameters were used to establish a fit to the high V_{ds} output characteristics. The impact ionisation generation rate, G_{II}, was given by [72]:

$$G_{II} = nv_n\alpha_n + pv_p\alpha_p \tag{8.43}$$

where v_n (v_p) is the electron (hole) velocity, and α_n (α_p) is the electron (hole) ionisation coefficient, which is given by the Chynoweth law:

$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \exp -\left(\frac{F_C}{F_{ll}}\right) \tag{8.44}$$

and F_C is the critical electric field and F_{ll} is the field parallel to the current flow. The simulated characteristics are shown in Fig. 8.28b, where $F_C = 2.9 \times 10^6$ V/cm and $\alpha_n = 5 \times 10^5 \text{cm}^{-1}$ [27].

The model was used to examine the relative roles of DIBL and avalanching in the kink effect by comparing simulations with and without the impact ionisation effect switched on. As seen in Fig. 8.28b, impact ionisation was needed to simulate the results. During impact ionisation, electron-hole pairs are produced in the high field region near the drain junction, and the electrons are swept into the drain by this field. In the floating body of the TFT, the holes have to flow through the poly-Si layer towards the source junction, and a steady state concentration of holes will be stored in the layer. This forward biases the junction, permitting a hole injection current into the source. The forward biased source junction will also inject further electrons into the channel, thereby generating parasitic bipolar transistor, PBT, action. The PBT contribution to the overall current, I_{ds}, can be analysed in the following way [27]:

$$I_{ds} = M(I_{ch} + I_e) = I_{ch} + I_e + I_b \tag{8.45}$$

Where M is a multiplication factor, I_{ch} is the channel current in the absence of avalanching, and I_e is the emitter current due to the PBT action. I_b is the base current, given by the flow of holes generated by impact ionisation at the drain (which was calculated from the integral of the impact ionisation rate). The emitter current gain, β, is given by:

$$\beta = (I_e - I_b)/I_b \tag{8.46}$$

and the excess device current, ΔI, due to impact ionisation and the PBT is:

$$\Delta I = I_{ds} - I_{ch} = I_e + I_b \tag{8.47}$$

$$\Delta I/I_{ds} = (\beta + 2)(M - 1)/M \tag{8.48}$$

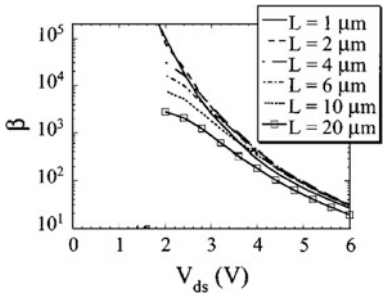

Fig. 8.29 Simulated results showing the emitter current gain, β, as a function of drain bias, for different channel length TFTs (Reprinted with permission from [27]. Copyright (2004) American Institute of Physics)

Hence, the normalised excess current is a function of M and β. The calculated values of M-1 varied with drain bias from $\sim 10^{-8}$ to 10^{-2}, and the corresponding β values are shown in Fig. 8.29. It will be seen that β is greatest, and displays the strongest L dependence, at low values of V_{ds}, where the hole injection is weakest, and the junction injection efficiency is greatest. With increasing V_{ds}, the avalanche rate and I_b increase, which causes a progressive lowering of the source barrier, such that each increment in hole current produced a reduced relative increment in electron current due to the lower barrier height. Nevertheless, the values of β range from $>10^5$, at low V_{ds}, to >10, at large V_{ds}, and demonstrate that the basic avalanche current, I_b, is significantly magnified by the PBT effect. In other words, whilst the kink effect is initiated by impact ionisation in the high drain field, the majority of the current flowing through the device is the result of current amplification due to parasitic transistor action in the floating 'base' of the device. This is analogous to the amplification of the collector–base leakage current in an open-base bipolar transistor [73]. The contribution of the injected current, I_e, as a function of channel length, L, (at $V_{ds} = 4$ V, where $\beta > 100$), is illustrated by the current component comparison in Fig. 8.30 [27]. This figure shows the low values of I_b compared to I_{ds} at all values of L, but, at L = 1μm, the major component of the total current was due to I_e and the PBT effect. In contrast, for L = 20 μm, the PBT effect was much weaker, and the current was essentially a pre-kink, basic channel current.

These TFT results, including the dependence of β and M-1 on V_{ds}, are similar to those reported in fully depleted SOI MOSFET devices [71].

8.7.2.2 Sub-Threshold and Threshold Voltage Effects

This section deals with the drain bias dependence of both sub-threshold currents and of threshold voltage. Whilst these are essentially classical MOSFET short channel effects, the involvement of floating body effects in poly-Si TFTs [72] warrants further discussion.

Figure 8.31 compares the drain bias, V_{ds}, dependent characteristics of short (L = 0.4 μm) and long (L = 20 μm) channel TFTs, in which the L = 20 μm TFT displays classical long channel behaviour, with the sub-threshold currents being

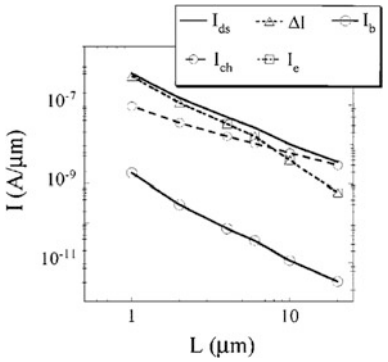

Fig. 8.30 Simulated results showing the different current components of I_{ds} as a function of channel length (at $V_{ds} = 4$ V) (Reprinted with permission from [27]. Copyright (2004) American Institute of Physics)

independent of V_{ds}, while the L = 0.4 μm TFT displays a strong V_{ds} dependence [72]. This dependence will also manifest itself as a V_{ds}-dependent threshold voltage, as shown in Fig. 8.32, where the threshold voltage was measured at $I_d = 10^{-7}$W/L A to minimise series resistance effects. Also shown by the solid lines in this figure are fitted simulation results obtained from optimised DOS and impact ionisation parameters [72], as discussed in the previous section. As will be seen, the influence of drain bias on V_T was much stronger in the short channel TFTs, and is ostensibly similar to a classical short channel DIBL effect.

However, given the presence of impact ionisation in the simulated results, the relative contributions of the direct DIBL and the PBT effects, which will also lower the source-channel barrier, have been clarified [72]. Figure 8.33 shows the simulations of V_T, with and without drain avalanching turned on. At low V_{ds}, the DIBL was primarily responsible for the barrier lowering, but the effect of hole accumulation, via the PBT effect, reduced the barrier at higher values of V_{ds}. As would be expected from Fig. 8.31, both effects increased as the channel length decreased. These barrier-lowering effects were also directly seen in simulations of

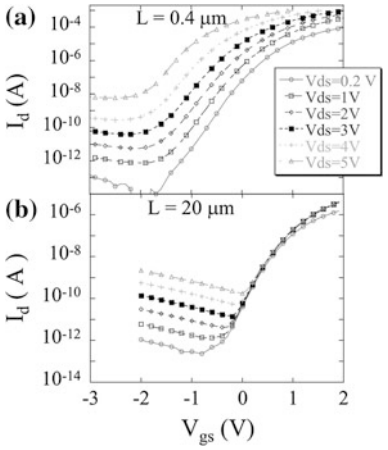

Fig. 8.31 TFT transfer characteristics measured as a function of drain bias **a** L = 0.4 μm, and **b** L = 20 μm (Reprinted with permission from [72]. Copyright (2010) American Institute of Physics)

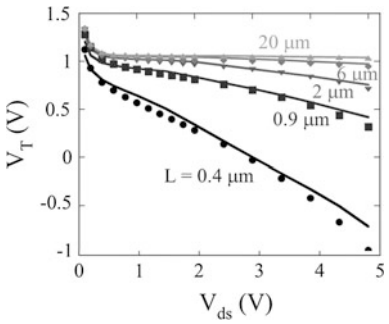

Fig. 8.32 Variation of measured (*symbols*) and simulated (*lines*) threshold voltage as a function of drain bias for different channel length TFTs (Reprinted with permission from [72]. Copyright (2010) American Institute of Physics)

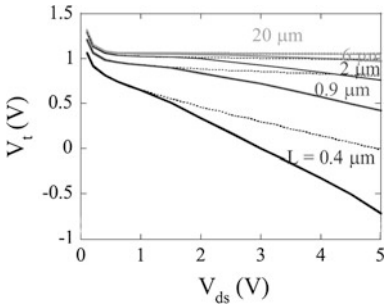

Fig. 8.33 Simulated values of threshold voltage as a function of drain bias, with (*solid lines*) and without (*broken lines*) impact ionisation switched on (Reprinted with permission from [72]. Copyright (2010) American Institute of Physics)

the source barrier height itself [72], with the influence of PBT lowering being much smaller in the longer channel devices.

As can be appreciated, the kink effect discussed in the previous section, and the V_T effects in this section, are related phenomena. Both are caused by the generation of impact ionisation holes at the drain junction, leading to PBT action in the floating body of the TFT. The kink effect discussion introduced these concepts, and focussed on the current gain within the device, and its impact on the total current flow. This section has looked in more detail at the relative contributions of DIBL and the PBT effect to the source barrier height in short channel TFTs.

8.8 Summary

In this chapter, various aspects of the characterisation and performance of poly-Si TFTs have been considered. Whilst much current analysis of poly-Si TFTs is based upon the use of 2-D numerical simulators, a simple analytical model of grain boundary conduction was introduced in Sect. 8.2, as this embodies some key physical considerations of carrier transport through poly-crystalline material. The limitations of this model were discussed, and, in Sect. 8.3, the DOS in poly-Si was shown to be continuous across the band-gap, rather than based upon a discrete trapping level (as assumed in the analytical model). It was found that the DOS

could be well represented by a pair exponentials, which could be related to band edge states and deep states.

In Sect. 8.4, the low-field TFT leakage currents were characterised by an analytical carrier generation rate and transport model, which encompassed all the key features of the drain voltage and channel length dependences of the leakage current in TFTs containing both high and low DOS values. In addition to this classical low field phenomenon, poly-Si TFTs display a number of undesirable artefacts, such as low output impedance, drain bias stress instability and field enhanced leakage currents, which are associated with a large electrostatic field at the drain junction. The drain field, in high quality TFTs, is essentially determined by the 2-D architecture of the device, rather than by the DOS level, and the mechanisms of hot carrier instability and field enhanced leakage currents were described in Sect. 8.5. Other bias instability processes in poly-Si TFTs, including ionic drift under gate bias stress, threshold voltage instability under elevated temperature negative gate stress, and self-heating instabilities under combined gate and drain bias stress were discussed in Sect. 8.6.

Short channel effects, SCEs, were presented in Sect. 8.7, where it was shown that some of these effects were comparable to the well-established SCEs in MOSFETs. However, others, such as parasitic channel resistance effects, are specific to certain types of n-channel TFT technology. A further class of SCEs was enhanced by parasitic bipolar transistor action due to floating body effects in the devices, and are comparable to similar phenomena in silicon-on-insulator MOSFETs.

The extensive investigation of poly-Si TFTs has identified the performance artefacts discussed in this chapter, and the understanding and control of these effects has enabled the mass production of stable, high performance poly-Si TFTs for a variety of flat-panel display applications. As discussed in Chap. 7, these have focussed on the small/medium diagonal display market, and include both AM-LCDs and AMOLEDs.

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