Chapter 7
Poly-Si TFT Technology and Architecture

Abstract This chapter discusses the fabrication of high quality poly-Si films, by the industry standard technique of excimer laser crystallisation of a-Si:H precursor films. Alternative crystallisation procedures are also reviewed, including metal-induced solid phase crystallisation, as well as advanced procedures for achieving large grain and high mobility TFTs, using green solid-state lasers in addition to modified excimer laser techniques. The architecture of poly-Si TFTs is top-gated with a silicon dioxide gate dielectric, and issues with the implementation of self-aligned and non-self-aligned architectures are discussed, and illustrative processing schedules are listed. Finally, a simple qualitative cost model is presented, illustrating why the major commercial application of poly-Si TFTs is in the small-diagonal, portable display market.

7.1 Introduction

The interest in poly-Si, as an alternative TFT material, started soon after a-Si:H TFTs became recognised as the most promising technology for the large scale production of AMLCDs. The low carrier mobility of a-Si:H TFTs (<1 cm^2/Vs) is perfectly adequate for the addressing TFTs within each pixel, but is inadequate for the faster switching circuits needed for addressing the rows and columns in the display itself. In contrast to the carrier mobility in a-Si:H, which has remained within the range 0.5–1.0 cm^2/Vs over the last 20 years or so, the electron mobility in poly-Si has increased, over the same period, from <5 to ~ 120 cm^2/Vs with routine processing, and up to ~ 900 cm^2/Vs with innovative techniques yielding quasi-single-crystal large-grain material [1]. The higher carrier mobility offered by the more crystallographically-ordered polycrystalline silicon was seen as leading to a second generation AMLCD technology, with addressing circuitry and other circuit functions integrated onto the AMLCD plate. Whilst this has been achieved, and

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highly integrated poly-Si displays [2, 3] are now in mass production for small/medium diagonal, portable active matrix flat panel displays, AMFPDs, a-Si:H remains the dominant AMLCD technology, particularly for the larger sized notebook, monitor and TV displays. Hence, the current application of poly-Si is directed towards small/medium diagonal displays, where it accounts for ~36 % of that segment of the AMLCD market [4]. In addition, it has virtually 100 % of the rapidly growing small diagonal AMOLED market, particularly for smart phones [5].

The study of poly-crystalline silicon, as a semiconductor device material, has a long history, and predates the present interest in the low temperature fabrication of TFTs on glass or flexible substrates. Traditionally, its major application has been as a heavily doped layer for the gate electrode in MOSFETs [6], because, as a refractory material, it can withstand high temperature integrated circuit processing. As MOSFET circuit speeds increased, its conductivity was enhanced by combining it with a refractory metal to form a low resistivity metal-silicide. In addition to this, poly-Si resistors have also been used in VLSI circuits [7], leading to detailed studies of conduction in the material [8]. Finally, in the mid-1980s poly-Si TFTs on quartz substrates were fabricated, using a high temperature VLSI-like process, for use in projection AMLCDs [9]. Much of this work formed a useful background to the research and development of low temperature poly-Si TFTs on glass, which is the subject of this chapter and of Chap. 8. A particular example of this information infrastructure is the analytical model of conduction in polycrystalline silicon [8], which is still used to provide a simple numerical and pictorial description of carrier flow over grain boundaries. More sophisticated treatments have now been adopted, but, in view of the continued use of this model, it will be presented in Chap. 8, together with its analytical extension to carrier flow over grain boundaries in TFTs [10].

As mentioned above, highly integrated poly-Si AMLCDs are in mass production, with the level of integration expected to increase as more circuit functionality is added to the panel: the objective being a System-on-Glass, SOG [2, 3, 11]. In order to achieve the higher circuit speeds needed to replace external MOSFET circuits, the performance of the poly-Si TFTs has been leveraged by way of higher carrier mobility and shorter channel lengths. Both of which have been achieved within the constraints of a glass-compatible process.

In Sect. 7.2, the more conventional processing of poly-Si TFTs is presented; in particular, the formation of poly-Si thin films by laser crystallisation. It will be shown that the thin film formation technique determines grain size and structure, and this has a fundamental impact upon carrier mobility and other basic device parameters, such as threshold voltage and leakage current. These performance parameters can also be affected by the gate dielectric and the device architecture, and those topics, together with the process flow for TFT and AMLCD fabrication, are presented in Sects. 7.3 and 7.4, respectively. Advanced crystallisation processes, leading to large grain and high carrier mobility material, are reviewed in Sect. 7.5. Finally, Sect. 7.6 contains a brief overview of the issues underlying the application of poly-Si TFTs to AMFPDs, including the factors favouring it for small/medium sized displays.

In summary, this chapter focuses on poly-Si material preparation, and TFT design and fabrication. The discussion of the performance of these devices is presented in Chap. 8. Throughout these two chapters, parallels are drawn, where appropriate, between the physics and technology of poly-Si TFTs and IC MOSFETs, from which it will be seen that poly-Si TFTs share more similarities with these devices than with the other TFT technologies discussed in this book.

7.2 Poly-Si Preparation

As mentioned above, the electron mobility in poly-Si has increased from <5 [12] to ~900 cm^2/Vs [1] over the last 20 years or so. These increases are due to several evolutionary changes in the preparation of the material, which are the subject of this section and of Sect. 7.5. At the upper end, the mobility is comparable to the low field value of long-channel SOI MOSFETs [1], although, in poly-Si, these are field effect mobility values, which are degraded from the band mobility values by the presence of band gap states near the conduction band edge. The nature and distribution of these states, together with their impact on carrier mobility is discussed in Chap. 8.

In discussing poly-Si performance, the electron mobility is frequently quoted as a figure of merit, and this approach is also used in this chapter. However, it should be appreciated that a large mobility alone is not sufficient for the device to have a useful application in the display-addressing field: it must also be accompanied by a low leakage current and a low threshold voltage. Moreover, these parameters need to be achieved with a glass-compatible process, within which the maximum process temperature is, ideally, kept below ~450 °C. Even this modest temperature requires a harder glass than that used in the lower temperature a-Si:H process, and a brief overview of glass plate issues is presented in Sect. 7.2.1. Finally, the overall complexity of the process needs to borne in mind, as, the more complex the process, the more expensive the final product will be.

7.2.1 Background

Before proceeding to a detailed discussion of the laser crystallisation process, it is worth briefly reviewing the preceding technologies from which the laser process was ultimately identified as the most commercially attractive.

The first generation technology was based upon a well-established LPCVD process, which was employed in the semiconductor industry for the fabrication of MOSFET gate layers. This was the direct deposition of a poly-Si layer at ~620 °C, but which had a small grain size of ~100 nm and yielded an electron field effect mobility of ~5–7 cm^2/Vs [12, 13]. This was a demanding process for glass substrates, as the deposition process approached the substrate's softening temperature, and could lead to warping and distortion of the substrate. In addition,

the finished TFTs required exposure to atomic hydrogen, for several hours at ~350 °C in an RF plasma, in order to passivate defects in the film. The long plasma exposure time was because the hydrogen diffused laterally through the gate oxide before entering the poly-Si. The consequence of this lateral diffusion process was that TFTs, with increasing channel length, required increasingly long exposure times for the defects in the centre of the channel to be passivated [12, 13].

The direct deposition process was superseded by a second generation process, using a precursor film of a-Si. This could be deposited either by LPCVD at 550–600 °C [13–15], or by PECVD (using an a-Si:H reactor) at 350 °C [15], or the standard, small grain LPCVD films could be amorphised by high dose silicon ion implantation [16]. In all cases, the objective was to use pre-cursor films, which were essentially amorphous. These films then underwent a phase transformation into a polycrystalline form by a process of solid phase crystallisation (SPC) [13–16], which relied upon a sparse distribution of incipient seeds or random nucleation within the film, to seed grain growth. For seed-free films, this was a two-stage process consisting of the growth of stable nuclei, which then seeded grain growth. Both of these processes are thermally activated, and the overall activation energy of the SPC process has been found to be within the range 3.1–3.9 eV, depending upon the film preparation technique [16]. The thermal budget for this process was up to tens of hours in the temperature range 580–630 °C [16], and the resulting films had large, faulted dendritic grains, up to 1μm long [14, 16]. These larger grains gave TFTs with electron field effect mobilities up to ~40 cm^2/Vs [13, 15].

Even more than with the direct deposition process, the longer exposure times to high temperatures were particularly demanding on the glass substrate, and the dimensional instability of the glass became an issue. The mechanical properties of glass are determined by its manufacturing process, and, in particular, its cooling rate from the melt determines the temperature at which it solidified. Only at this temperature is the glass in thermal equilibrium, and, at lower temperatures, it will tend to relax to a new equilibrium state. For the glasses used for TFTs, this will be such a slow process at room temperature that it can be ignored, and should be distinguished from reversible dimensional changes governed by its coefficient of thermal expansion. However, at the temperatures used for SPC, the irreversible dimensional changes become significant, as shown by the results in Fig. 7.1 [15]. The results in Fig. 7.1a are normalised measurements of shrinkage (usually referred to as compaction), in a hardened glass substrate, as a function at exposure time to the range of temperatures used for SPC. It will be seen that the compaction is a thermally activated process to an equilibrium state, which, as expected, is temperature dependent. In summary, the higher the annealing temperature, the smaller was the dimensional change, and the faster it occurred. For photolithography, it is essential that the substrate is dimensionally stable through all mask alignment stages, and the required degree of stability is determined by the mask alignment tolerances and the size of the substrate. For instance, with a 30 cm substrate and a 3 μm alignment tolerance, the substrate will need to maintain a dimensional stability of 10 ppm from the first to the last alignment stage. As seen from Fig. 7.1a, the overall dimensional stability of glass was far worse than this,

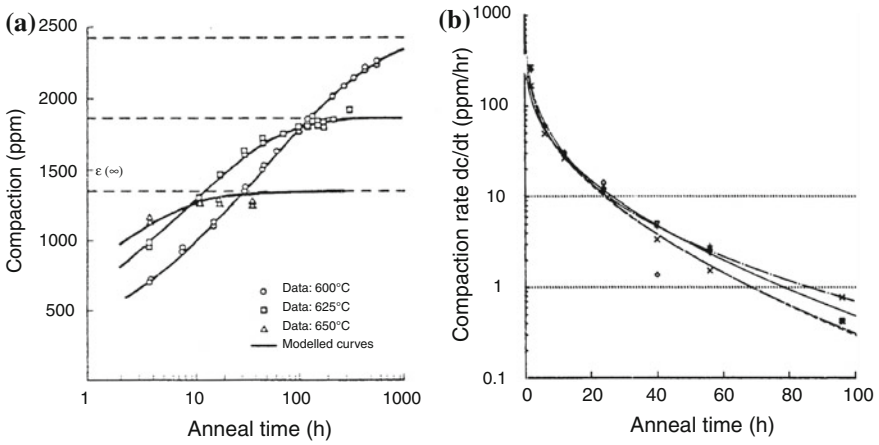

Fig. 7.1 **a** Normalised compaction measurements, on 'hardened' glass plates, as a function of annealing time at 600–650 °C (Reprinted from [15] with permission of SID), and **b** normalised compaction rate measurements at 625 °C

and it was necessary to pre-shrink the glass prior to the first alignment stage. Furthermore, as the equilibrium compaction was a function of the anneal temperature, the substrate needed to be pre-compacted at the temperature at which the SPC process was carried out. The easiest way to determine the required pre-compaction time was from a plot of the differential of the data in Fig. 7.1a, and, as an example, the compaction rate at 625 °C, as a function of the anneal time, is shown in Fig. 7.1b. Hence, if, for example, a 10 h SPC process was used, then a compaction rate, prior to processing, of 1 ppm/h was needed to ensure that $<$10 ppm compaction occurred during the SPC process, and this required a pre-compaction anneal of $\sim$80 h.

As with the direct deposition process, prolonged exposure to atomic hydrogen in an RF plasma was required to passivate the defects in the large, but highly faulted, SPC grains. Nevertheless, demonstration displays, with integrated drive circuits, were fabricated on glass substrates by this process [13, 15]. However, the thermal budgets, the issues with glass, and the plasma hydrogenation process did not make SPC an attractive process for industrialisation. Most of these issues were resolved with the third generation process, which used excimer laser crystallisation, and this is now the industry standard process. A more extensive review of the SPC process can be found in Ref. [17].

The current industry standard crystallisation procedure of excimer laser annealing, ELA, is discussed in Sect. 7.2.2, and in Sect. 7.2.3 other laser techniques are briefly considered, although a more detailed discussion of them is contained in Sect. 7.5, which deals with advanced crystallisation techniques for large grain material. Finally, in Sect. 7.2.4, a variant of the SPC process is presented, which uses metal silicide-mediated crystallisation to reduce the thermal budget of the SPC process.

7.2.2 Excimer Laser Crystallisation

7.2.2.1 Introduction

Excimer lasers are gas lasers operating in the ultra-violet wavelength range, from 193 to 351 nm depending upon the gas mixture chosen. For crystallisation of a-Si, the preferred gas mixture is XeCl, giving a wavelength of 308 nm; similar crystallisation results have been obtained from KrF excimer lasers at 248 nm, but the 308 nm laser is preferred for industrialisation, as the longer wavelength is less damaging to the optical components in the beam path. These are pulsed lasers, with a typical pulse duration of $\sim$30 ns, a maximum repetition frequency of 600 Hz, and can deliver up to 0.9 J/pulse [18]. The raw pulse shape is semi-Gaussian, with dimensions of $\sim$1 cm $\times$ 1 cm, but, for crystallisation, a pencil shaped beam is preferred, and beam shaping optics are used to produce a highly elongated line-beam, whose dimensions can be up to 465 mm in the long axis and down to 350 μm for the short axis [18]. The steep edges in the short axis profile have led to the beam shape being referred to as a 'top-hat' beam, and all the line-beam irradiations discussed in this section will be assumed to have this shape, unless specified otherwise. Measurements of an industrial line-beam profile are shown in Fig. 7.2a, and a schematic illustration of an ELA crystallisation system is shown in Fig. 7.2b, where the key components are an attenuator for controlling beam intensity, the homogeniser and beam shaper to produce the line-beam, and a condensing lens to focus the beam on the underlying plate. The plate is mechanically swept through the short axis of the beam at a rate, which delivers a multi-shot process, of typically 10–30 shots per point for commercial processing, so that the plate translation distance between shots is typically in the range 12–50 μm for short axis lengths of 350–500 μm.

7.2.2.2 Crystallisation Process

At 248 nm and 308 nm wavelengths, the optical absorption depth in a-Si is 5.7 nm and 7.6 nm, respectively, so that the incident energy is strongly absorbed in the silicon film, resulting in intense heating. If the incident energy density is high enough, this will heat the film to its melting point, T_m, of 1420 K, where the optical and thermal constants for a-Si [19] and c-Si [20] are shown in Table 7.1. The required energy density, E_{th}, to cause surface melting can be calculated from the solution of the heat diffusion equation, which yields the following approximate analytical solution [21] (provided the optical absorption depth of the film, $1/\alpha$, is less than the thermal diffusion length, $\sqrt{(D\tau)}$, where $D = k/\rho C_p$):

$$E_{th} = \frac{(T_m - T_0)\sqrt{\pi}\rho C_p \sqrt{D\tau}}{2(1-R)} + \frac{H\Delta z}{\rho(1-R)} \tag{7.1}$$

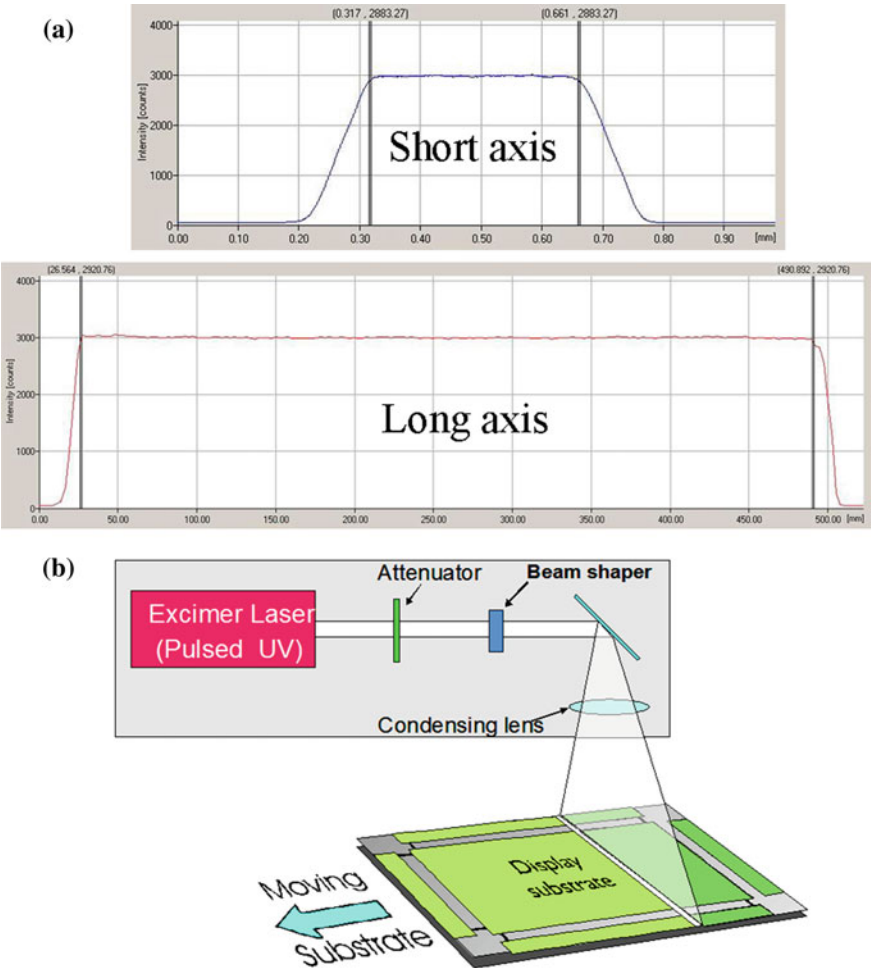

Fig. 7.2 **a** Laser intensity profiles from a 464 mm × 340 μm line-beam excimer laser annealing, ELA, system (data supplied by Coherent GmbH), **b** schematic illustration of an ELA system

The first term in Eq. 7.1 is the intensity to bring the surface of the film up to the melting temperature, and the second term accounts for the latent heat required to melt a thin film of thickness Δz. (T_0 is initial film temperature, ρ is the density of a-Si, C_p is its specific heat, D its diffusion coefficient, τ is the heating time, H is the latent heat of melting, and R is reflectivity).

Evaluation of Eq. 7.1, using the optical and thermal coefficients listed in Table 7.1, predicts a melt threshold energy density of $\sim$75 mJ/cm^2 for a-Si, which agrees well both with full numerical simulations giving 70–90 mJ/cm^2 [22], and experimental data in the range 70–100 mJ/cm^2 [23, 24]. The thermal diffusion length in a-Si, for a 30 ns pulse, is 120 nm, so that we can readily expect films up

Table 7.1 Optical and thermal constants for amorphous, crystalline, and liquid Si [19, 20, 22]

Material	$1/\alpha$ (at 308 nm)(nm)	R (at 308 nm)	$1/\alpha$ (at 248 nm)(nm)	T_m (K)	ρ (gcm^{-3})	C_p $Jg^{-1}K^{-1}$	k ($Wcm^{-1}K^{-1}$)	H (Jg^{-1})
a-Si	7.6	0.57	5.7	1418	2.26	1.1	1.3×10^{-2}	1282
c-Si	6.9	0.66	5.5	1687	2.31	1.0	0.23	1800
Liquid Si	6.9	0.69	6.4		2.52	1.1	0.51	

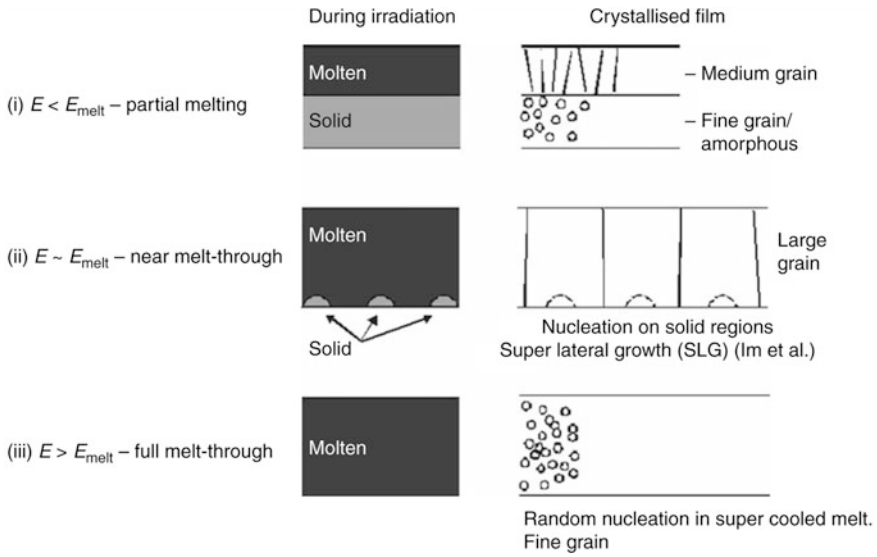

Fig. 7.3 Schematic illustration of a-Si melting regimes during excimer laser irradiation, and the resulting poly-Si grain structure

to at least this thickness to be melted at high enough incident energy densities. Indeed, experimental data have shown the melt depth increasing linearly with energy density up to 145 nm [25], and simulations have predicted the same dependence for melt depths up to at least 300 nm [26].

In fact, current understanding of the crystallisation mechanism of a-Si, has shown that the melt depth of the film is a crucial factor in determining the outcome of the process [27–30]. This is shown schematically in Fig. 7.3, where three melting regimes are identified. Following partial film melting, the crystallised film has a vertically stratified appearance, as shown in Fig. 7.4a, with mid-sized grains ($\sim$100 nm) within the previously melted region, and either a fine grain or amorphous region beneath it. Fig. 7.3b shows the film almost fully melted, with small solid islands remaining at the back of the film, seeding the growth of large ($\sim$300 nm) high quality grains, as the film cools. These columnar grains extend through the entire thickness of the film, which no longer shows vertical stratification. This process was identified by Im et al. [27, 28], and given the name super-lateral growth (SLG). As will be shown below, this is the crystallisation regime, which yields high quality TFTs. Finally, for the fully melted film in Fig. 7.3c, the seeding centres responsible for the SLG growth are lost, and crystallisation of the film relies upon random nucleation in a super-cooled melt, resulting in a fine grain film [27].

From the above scenario, it is apparent that the optimum energy range is that which results in the SLG regime: energy densities above and below this result in smaller grain poly-Si. However, as shown by the grain size results in Fig. 7.4b, the SLG regime occurred over a very limited energy density range of $\sim$45 mJ/cm^2

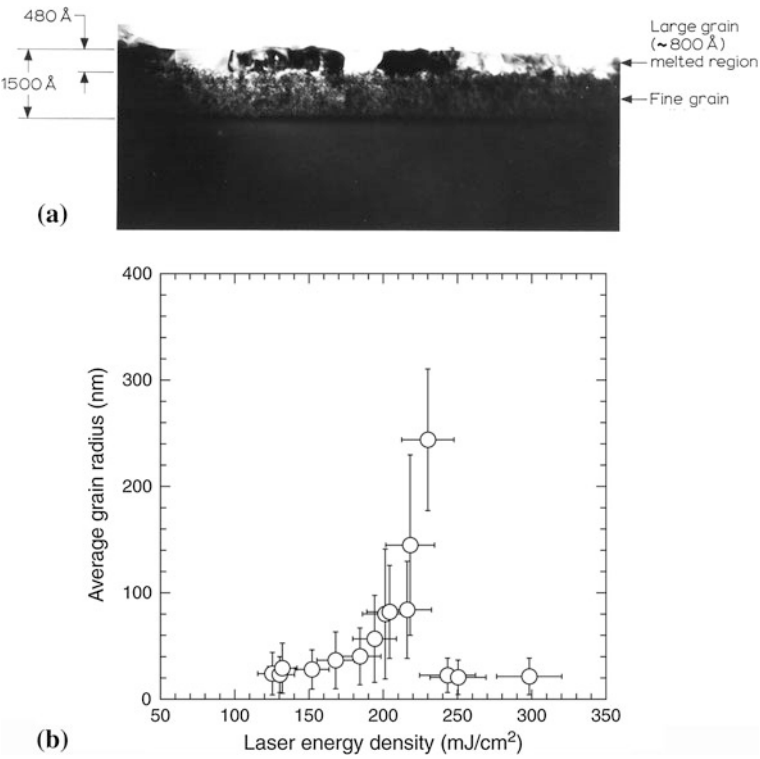

Fig. 7.4 **a** Cross-sectional TEM micrograph of a partially melted 150 nm thick a-Si film, showing the resulting vertically stratified grain structure (Reprinted from [23] with permission of IEEE), and **b** variation of average grain radius with laser energy density for excimer laser crystallized a-Si films (100 nm thick films capped with 50 nm SiO_2). (Reprinted with permission from [27]. Copyright (1993) American Institute of Physics)

from $\sim$195 to $\sim$240 mJ/cm^2 [27]. These particular results were from single shot irradiations [27], and qualitatively identical results were obtained from multi-shot irradiations [30], apart from a growth in SLG grain size with increasing shot number. As discussed below, the limited size of the SLG window has major implications for the implementation of the crystallisation process to produce high performance TFTs.

The essential features of the above process are fully demonstrated in the correlation of TFT behaviour with the energy density used to crystallise the film. This can be most easily seen with static irradiations of a 40 nm thick a-Si film, using the raw, semi-Gaussian excimer laser beam, as shown in Fig. 7.5a–c [25]. It should be emphasised that this mode of irradiation is not the conventional TFT crystallisation procedure (which involves swept, line-beam irradiations), but was used purely as an experimental tool. Figure 7.5a shows a profile of electron mobility measurements made on a line of non-self-aligned TFTs, with a W/L ratio of 50/6 μm, and with a spatial pitch of 220 μm. The profile through the approximately Gaussian distribution

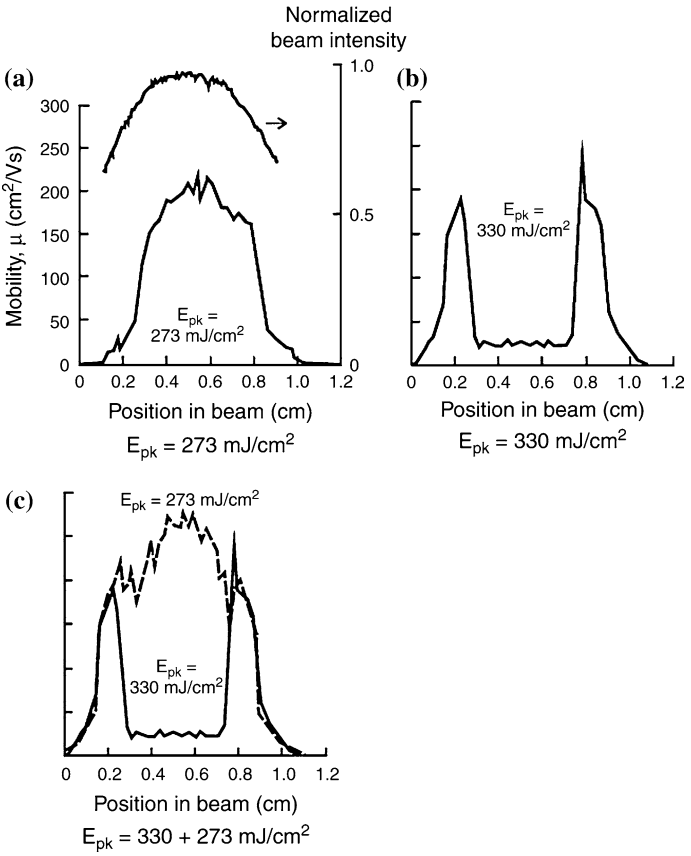

Fig. 7.5 Electron mobility as a function of position in stationary KrF excimer laser beam, measured after irradiations at the following peak intensities: **a** 273 mJ/cm^2, **b** 330 mJ/cm^2, **c** 330 mJ/cm^2 followed by 273 mJ/cm^2. (Reproduced with permission from [34])

of energy densities within the beam facilitates a precise mapping of electron mobility (and other device parameters) against incident energy density [25]. The maximum beam intensity had been set to $\sim$270 mJ/cm^2, which was a value in the SLG regime, and a progressive increase in mobility from zero to $\sim$200 cm^2/Vs is seen as the crystallisation energy increased from zero to its maximum. Also of note are the rapid changes in mobility at the x-axis locations of 0.3 and 0.8 cm, which corresponded to the positions within the beam at which the threshold energy density occurred for the SLG regime ($\sim$225 mJ/cm^2). In Fig. 7.5b, the maximum energy density was increased to 330 mJ/cm^2, which was large enough to induce full melting of the film over the central portion of the beam. The ensuing fine grain material [27] resulted in a reduction of electron mobility, within the centre of the irradiated region, from $\sim$200 to $\sim$25 cm^2/Vs, whilst the edge regions, irradiated at lower energy densities, retained the appearance seen in Fig. 7.5a. The abrupt decrease in mobility

gave an SLG window size of ~45 mJ/cm^2, which is much the same as the energy window in the TEM data of Im et al. [27]. Finally, Fig. 7.5c shows the result of re-irradiating the material from Fig. 7.5b using lower intensity conditions, which corresponded to the SLG regime. This converted the previously fine grain material back into larger grain SLG material, with a consequent recovery in electron mobility. Hence, the material can be cycled in and out of the SLG regime, depending upon the final energy density used to crystallise the film. This has particular implications for the uniformity and process window size of the conventional swept beam process, as discussed in the following section.

7.2.2.3 TFT Crystallisation

An overview of TFT results from swept beam processing is shown in Fig. 7.6 [25, 31]. This figure shows the dependence of electron mobility, in n-channel TFTs, on the irradiation energy density, with the a-Si precursor film thickness as an independent parameter. Figure 7.6a contains results from LPCVD precursor a-Si, crystallised by a 248 nm KrF semi-gaussian beam, and the data in Fig. 7.6b are from the more commonly used PECVD pre-cursor a-Si:H, crystallised by a 308 nm XeCl line beam. The two sets of curves demonstrate the same essential

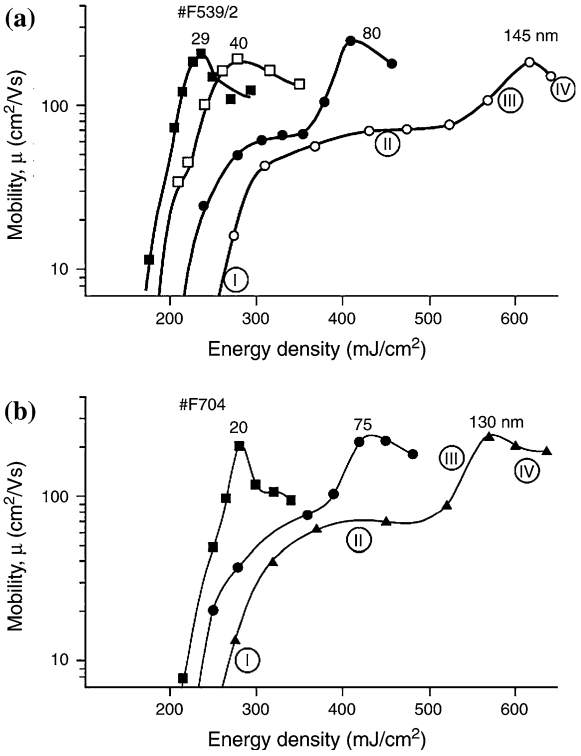

Fig. 7.6 Electron mobility as a function of excimer laser energy density for a-Si precursor films of different thickness (**a**) 248 nm (KrF) irradiation of LPCVD a-Si, (**b**) 308 nm (XeCl) irradiation of PECVD a-Si:H. (Reprinted from [31] with permission of SID)

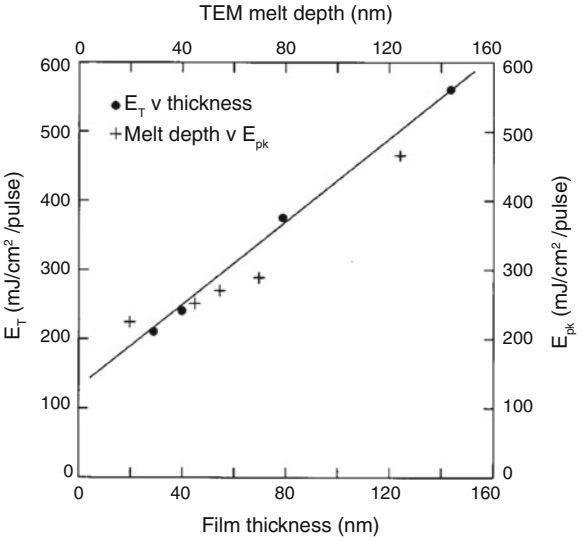

Fig. 7.7 Cross sectional TEM measurements of the melt depth in a 150 nm thick film with crystallization energy density (+ symbol, *top* and *right axes*). Variation of the threshold laser energy density for high mobility TFTs as a function of film thickness (• symbol, *left* and *bottom axes*) (from the TFT measurements in Fig. 7.6a). (Reprinted with permission from [25]. Copyright (1997) American Institute of Physics)

features of the crystallisation process, which were independent of the laser wavelength, the type of precursor material, and the beam shape details. The two most obvious features in these curves are, firstly, that the outcome of the crystallisation process was a strong function of film thickness. In fact, the energy densities required to achieve maximum carrier mobility scaled approximately linearly with film thickness, as shown in Fig. 7.7 [25]. Secondly, the crystallisation process was not a simple monotonic function of energy density. The results in Fig. 7.6 only show electron mobility, and the other key device parameters of sub-threshold slope and threshold voltage showed a corresponding dependence on crystallisation energy density, and qualitatively identical results were also obtained from p-channel TFTs [25]. Figure 7.8 shows the variation of leakage current with laser intensity, and this displays more complex behaviour than the mobility results, insofar as the leakage current initially increased and then decreased. From the dependence of leakage current on channel length, the initial increase in leakage current was ascribed to a resistive, drift current, which scaled with increasing mobility. The current at higher energy density was a generation current, and this decreased as the improving material quality increased the electron–hole pair generation lifetime [25]. The detailed analysis of this data is discussed in Chap. 8.

Figures 7.6 and 7.8 have focussed on specific parameter values, and Fig. 7.9 shows the overall transfer characteristics of high quality, non-self-aligned n- and p-channel TFTs obtained from this process. They illustrate the attainment of low leakage currents, small sub-threshold slopes, as well as high on-currents.

The crystallisation regimes in Fig. 7.6 can be broken down into four phases, which are most clearly seen in the thicker films, but can also be discerned by points of inflection in the thinner films. The four phases were an initial increase in mobility (I), a plateau region (II), a second rise in mobility (III), and, finally,

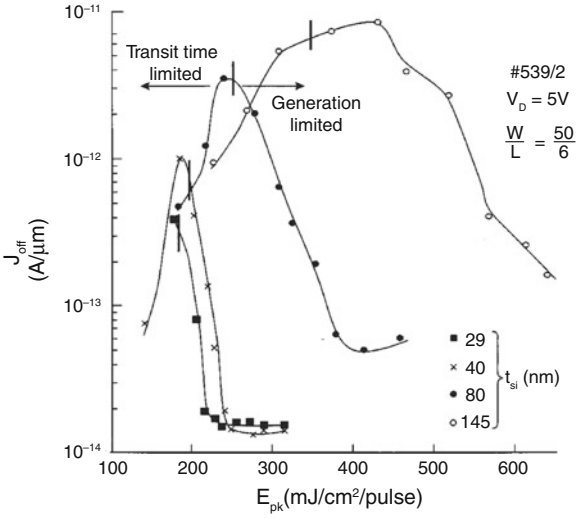

Fig. 7.8 TFT leakage current as a function of excimer laser energy density for a-Si precursor films of different thickness crystallized by swept beam 248 nm (KrF) irradiation. (Reprinted with permission from [25]. Copyright (1997) American Institute of Physics)

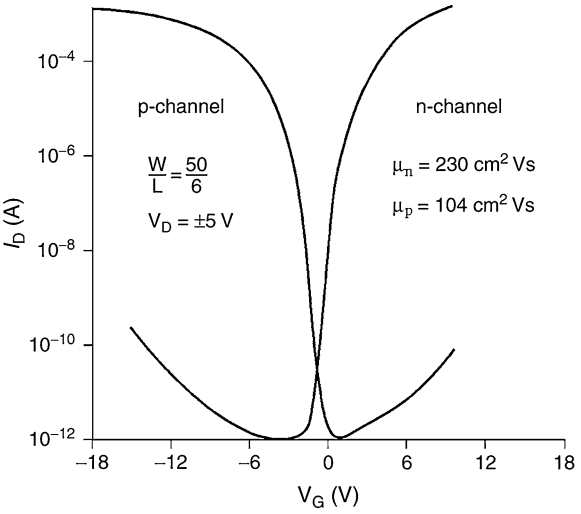

Fig. 7.9 Transfer characteristics of n- and p-channel excimer laser crystallized non-self-aligned TFTs. (Reprinted with permission from [72]. Copyright (1998), The Electrochemical Society)

a decrease in mobility (IV). The initial increase in mobility occurred above the melt threshold energy, as the surface of the film was converted into a polycrystalline form. When the thickness of this region was less than the equilibrium band bending thickness at inversion, the band bending extended into the underlying fine grain/amorphous silicon, as shown schematically in Fig. 7.10a (and this vertical stratification is clearly visible in the TEM micrograph in Fig. 7.4a). As discussed in Sect. 6.2.4, when there is a high trap density within the band bending region, the partition of induced carriers between trapped and free states results in a diminished value of field effect mobility. Moreover, the fewer trapping states there

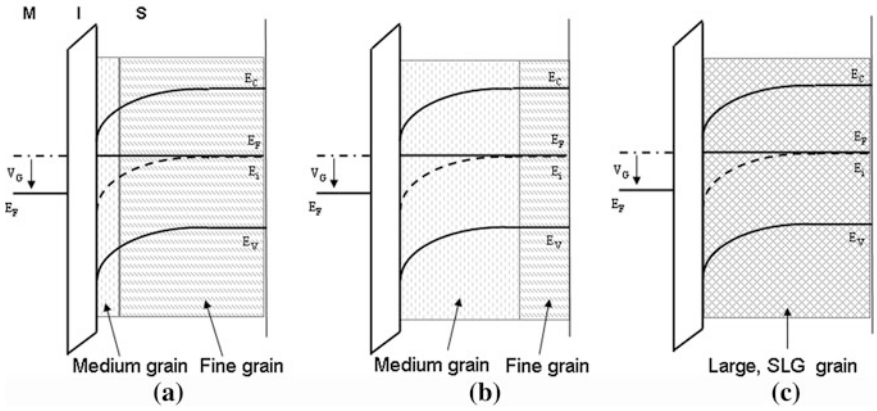

Fig. 7.10 Schematic illustration of band bending diagrams superimposed upon the grain structure regime in the laser crystallized films (**a**) regime I, (**b**) regime II, and (**c**) regime III. (For simplicity, constant values of gate bias and band bending are shown in each diagram)

are in this region, the higher the field effect mobility will be. Figure 7.7 shows that the melt depth increased with increasing crystallisation energy, and, as the thickness of this crystallised region increased, the electron field effect mobility similarly increased (due to the reduced number of carriers going into the fine grain, high trap density material at the bottom of the space charge region). This mobility increase continued until the band bending was contained entirely within the crystallised region, as shown schematically in Fig. 7.10b. When this occurred, regime II was entered, and further increases in crystallisation depth had a minimal effect upon the carrier mobility. The regime II plateau was resolved most unambiguously in the thicker films in Fig. 7.6, and Fig. 7.11a shows a TEM micrograph of the mid-sized grain structure in the upper portion of the partially melted film. Figure 7.6a shows that the threshold energy density for regime II with the 145 nm film was $\sim$300 mJ/cm^2, and, from Fig. 7.7, the melt depth at this energy density was $\sim$50 nm. Hence, the depletion depth for surface inversion was comparable to 50 nm at this energy density, and illustrates why regime II was also seen in the 80 nm film, but was not resolved in the 40 nm film.

Ultimately, with increasing incident energy density, the melt depth increased until the film was almost fully melted, and the SLG regime was initiated. This is depicted in the band bending diagram shown in Fig. 7.10c, and the SLG grain structure is shown in Fig. 7.11b. The increase in grain size and quality, compared with regime II grains (Fig. 7.11a), was responsible for the abrupt increase in electron mobility in regime III, and Figs. 7.6 and 7.7 demonstrate how the energy density for this regime scaled with film thickness [25]. Hence, to obtain maximum carrier mobility, the crystallisation energy density must be matched to the film thickness.

Finally, at the highest energy densities, the electron mobility started to decrease in regime IV, due to the incipient formation of fine grain material. However, the

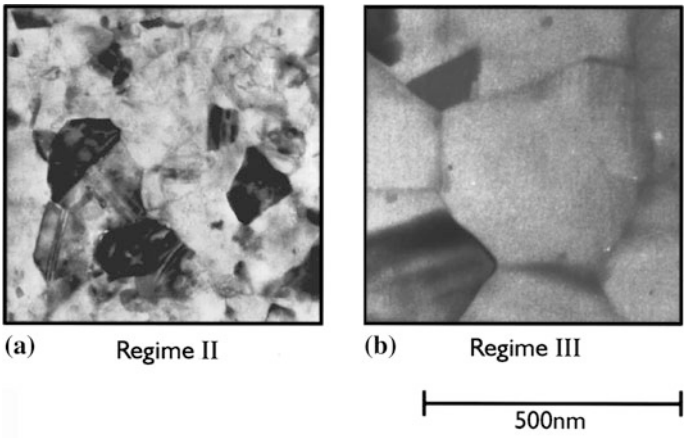

Fig. 7.11 Plan-view TEM micrographs showing the grain structure in ELA poly-Si, crystallised in (**a**) regime II (partial melting) and (**b**) regime III (SLG). (Reprinted with permission from [25]. Copyright (1997) American Institute of Physics)

decrease in mobility was much smaller than seen with the stationary beam process of Fig. 7.5b. This was because, in the swept beam process, subsequent lower intensity pulses, in the trailing edge of the beam, can reset the material back into the SLG regime. As discussed in the next section, the resetting of the material back into the SLG regime is a function of beam shape and shot number, and has implications for the overall trade-off between plate throughput and device parameters.

7.2.2.4 ELA Process Control Issues

As shown by the results in Fig. 7.6, to obtain high carrier mobility devices, the film needs to be crystallised within the SLG regime, and, ideally, at the energy density, E_m, giving the maximum mobility. But, there is limited accuracy in the precise setting of the laser energy density, and, moreover, the pulse-to-pulse fluctuations in energy density [32] mean that samples will occasionally be exposed to higher intensity irradiations, and, where this causes full melt-through, can lead to a consequent degradation in device parameters. Comparison of Figs. 7.5b and 7.6b shows that the magnitude of this degradation is determined by the opportunity, within the process, to re-irradiate the fine grain material, and to convert it back to large grain SLG material. The static irradiations in Fig. 7.5b can be regarded as a zero pulse overlap process (giving gross mobility non-uniformity when full melt-through occurred), whereas the 100-shot, swept beam process in Fig. 7.6b can be regarded as a 99 % pulse overlap process (giving greatly improved uniformity, even after full melt-through). This latter point can be understood by recognising that when an anomalously high intensity pulse has fully melted the stripe of

material exposed to it, the next pulse will overlap most of this poorly crystallised region, and the fine grain material will be re-melted, and converted back to the large grain SLG material. Nevertheless, there will be a thin strip of material (equal to the plate translation distance), which will not be fully overlapped by the top-hat region of the next pulse, but, at best, by its trailing edge. The recovery of this thin strip will then depend upon the relative size of the plate translation step, Δx, and the spatial width of the SLG window on the trailing edge of the beam, X_{SLG}, as illustrated in Fig. 7.12a [33]. Only if the SLG width on the beam edge, X_{SLG}, is greater than the translation step, Δx, will good recovery occur. (Where $\Delta x = W/N$, and W is the beam width, and N is the number of shots in the process).

Hence, the practical issue of plate processing is the trade-off between higher plate throughput (and reduced pulse overlap) and acceptable uniformity within a realistic process window.

This trade-off can be best illustrated within a quantified framework: for example, an acceptable laser process window, ΔE, could be defined as one within which the average carrier mobility, μ_{av}, varies by $<\pm 10$ %, or within which the maximum scatter in mobility ($\mu_{max}-\mu_{min}/\mu_{av}$) is $<\pm 10$ %. (The smaller of these two windows

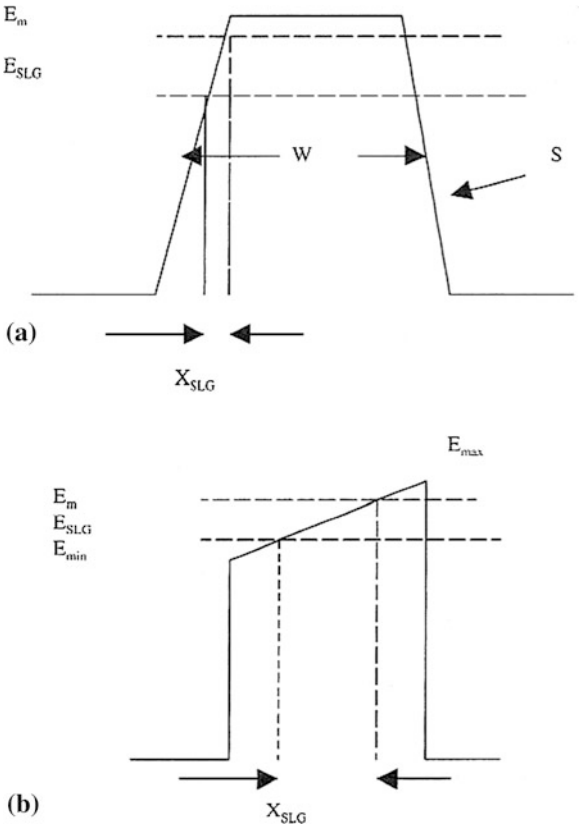

Fig. 7.12 Schematic illustrations of excimer line-beam pulse shape, showing the width of the SLG recovery regions, X_{SLG}, with: **a** top hat pulse, and **b** ramped pulse (where E_{SLG} is the threshold energy for the SLG regime, and E_m is full melt-through energy). (Reprinted with permission from [33]. Copyright (2004) The Japan Society of Applied Physics)

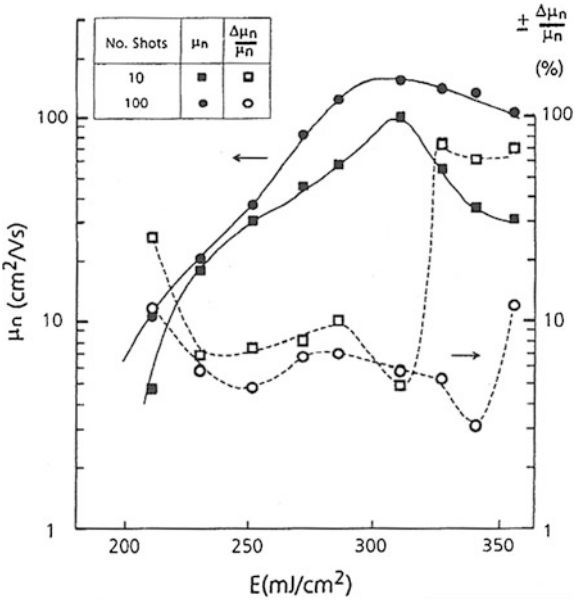

Fig. 7.13 Comparison of electron mobility values, and the maximum scatter in those values, for 100-shot and 10-shot top-hat ELA line-beam processing. (Reprinted with permission from [72]. Copyright (1998), The Electrochemical Society)

would be the relevant one.) Given that the fundamental issue is the tolerance of the process to random fluctuations in laser intensity, which cause full melt-through, this can be examined by deliberately irradiating the sample into this regime, and examining the size of the process window, ΔE, as a function of pulse overlap. This is illustrated in Fig. 7.13, in which crystallisation energy densities above the full-melt threshold are used to compare a 100-shot process (99 % overlap) with a 10-shot process (90 % overlap). The 100-shot process yielded an average mobility of 145 ± 15 cm^2/Vs, within a broad process window, ΔE, of 53 mJ/cm^2, due to good recovery of the full-melt material by the trailing edge of the beam [33, 34]. In addition, the mobility scatter remained well below ± 10 % over this energy range. The 10-shot process resulted in a lower average mobility of 90 ± 10 cm^2/Vs (due to a smaller SLG grain size [30, 31]), and a much stronger fall-off in average electron mobility at the higher energies, giving a significantly smaller process window, ΔE, of 20 mJ/cm^2. In both cases, this window was centred about the optimum intensity, E_{opt}, of 310 mJ/cm^2, which gave the maximum mobility. Hence, for the 10-shot process, the size of the energy window was just ± 3.3 % of the target intensity, E_m, so that random variations in pulse intensity greater than this will cause unacceptable uniformity variations. Associated with the lower average mobility at higher laser intensities, in the 10-shot sample, was also a sharp increase in mobility scatter once the full melt through regime was triggered. This was due to incomplete and variable recovery of the fine grain material by the trailing edge of the pulse, and was consistent with SEM observations of a periodic grain size variation, from small grain to large grain, at the pitch of the plate movement through the laser beam [33]. One way to improve the trailing edge recovery process

is to simply broaden the trailing edge; however, the energy within the pulse can be used more efficiently by ramping the top of the beam instead, as illustrated in Fig. 7.12b. With this beam shape, the size of the energy process window can be increased by a factor of $\sim$2 for a 10-shot process [33].

In view of the uniformity issues with a high throughput and low shot number process, typical plate processing uses a 20-shot process, yielding an electron mobility of $\sim$120 cm^2/Vs, within an energy window of $\sim$30–40 mJ/cm^2. However, the major contributory factor to improved control and uniformity of the ELA process for poly-Si AMLCDs has been improvements in peak-to-peak pulse energy stability [18, 32] to 3 % over $\pm$ 3 sigma. Moreover, when this is combined with a technique to randomise intensity variations along the beam length, the more stringent uniformity requirements for AMOLED displays may also be met [18].

7.2.3 Other Laser Techniques

Whilst excimer laser annealing is the currently preferred technique for the commercial crystallisation of poly-Si, other lasers have been examined as alternatives in order to address some of the ELA issues themselves. These include pulse-to-pulse stability, and the cost of ownership, which includes frequent gas refills, window cleaning, and general downtime for tube and system maintenance. In particular, diode pumped solid state lasers have been advocated to address both the pulse stability and cost of ownership issues, with neodymium-doped yttrium aluminium garnet, Nd:YAG, lasers being the most commonly studied [35–37]. These can be operated either in continuous wave, CW, mode, or in Q-switched mode, delivering short duration pulses ($\geq$10 ns) of 800 mJ/cm^2, with a repetition frequency of 4 kHz and an output power of 200 W at 532 nm [35]. The fundamental output wavelength of these lasers is 1064 nm, which is in the infrared, and radiation at this wavelength would not be efficiently absorbed in thin silicon films. Hence, for crystallisation of a-Si, the Nd:YAG lasers are usually operated in the frequency-doubled mode at a wavelength of 532 nm. This is in the visible radiation band, and these Nd:YAG-based systems are frequently referred to as green laser annealing systems. For CW use, although Nd:YAG lasers have been used [38], Nd:YVO_4 lasers are preferred for high power applications. These are also frequency doubled, and can emit 10 W of radiation at 532 nm [39–42].

Both the pulsed and CW approaches can produce material with comparable properties to the ELA process, but they are also able to produce large grain, high quality material with electron mobilities up to 250 cm^2/Vs [36] and 566 cm^2/Vs [39], respectively. In view of the large grain options with these solid state lasers, it is more appropriate to discuss them in detail in Sect. 7.5, where they can be compared with the large grain processing procedures available with modified excimer laser crystallisation.

7.2.4 Metal Induced Crystallisation

Metal induced crystallisation (MIC) is a solid phase crystallisation (SPC) process, in which the presence of the metal can enhance the crystallisation rate of a-Si into poly-Si. This process has been viewed as a potentially simpler, cheaper and more uniform alternative to ELA. Equally, by accelerating the SPC process, so that it could be implemented at lower temperatures and with shorter crystallisation times, it was seen as a more production-worthy alternative to conventional SPC. However, the resulting TFTs have had persistently high leakage currents, which has limited the commercial application of the technique, although these can be minimised by combining it with ELA.

A large number of different metals have been found to promote MIC [43], some of which act in the elemental state, such as In, whilst others, including several transition metals, as well as Pd and Pt, act via the metal silicide. This latter process is sometimes referred to as silicide-mediated crystallisation (SMC). For the application of MIC to poly-Si TFTs, the metal of greatest interest has been Ni, because one of its silicides is a very good lattice match to crystalline Si. The role of Ni in the enhanced crystallisation rate of a-Si is discussed in Sect. 7.2.4.1 and the use of this procedure to fabricate poly-Si TFTs is reviewed in Sect. 7.2.4.2

7.2.4.1 Ni Mediated Crystallisation of a-Si

When thin films of Ni, or high concentrations of Ni are introduced into c-Si, a number of different nickel silicides readily form upon subsequent low temperature annealing. At $\sim$200 °C, Ni_2Si is formed, this is converted into NiSi at $\sim$240–390 °C, and the thermodynamically favoured final phase of nickel disilicide, $NiSi_2$, is formed at $\sim$325–480 °C [43, 44]. $NiSi_2$ is a good lattice match to Si, having the same cubic lattice, and a lattice constant of 5.406 Å, which is within 0.4 % of the Si lattice constant of 5.430 Å. In Ni-doped a-Si films, crystallisation proceeded via a three-stage process of $NiSi_2$ precipitate formation, the nucleation of Si on the precipitates, and the subsequent migration of the precipitates, leaving trails of crystallised Si behind them [44]. In particular, regular octahedral precipitates of $NiSi_2$ formed at $\sim$400 °C, and the good lattice match of $NiSi_2$ to Si made it an effective seed for the crystallisation of a-Si from the {111} faces of the precipitates [44]. Using 95 nm thick a-Si films implanted with Ni, both in situ TEM observation of crystallisation at 660 °C, and TEM examination of 500 °C furnace crystallised samples showed that the crystallisation process produced needle-like grains of Si. These grains propagated in the $< 111 >$ directions from the {111} precipitate faces, and were preferentially orientated in the $< 110 >$ direction to the sample surface. This was the precipitate orientation, which permitted maximum growth within the plane of the film [44]. A TEM micrograph of the needle-like grains is shown in Fig. 7.14 [45].

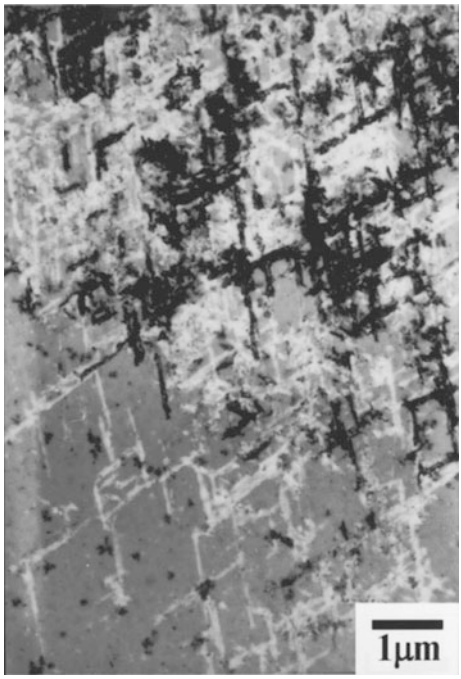

Fig. 7.14 Plan-view TEM micrograph of needle-like grains in $NiSi_2$-mediated crystallisation of a-Si, induced by 20 h annealing at 500 °C. (Reprinted with permission from [45]. Copyright (1997) American Institute of Physics)

The grain propagation took place by the movement of the precipitate through the a-Si, which consumed a-Si at its head and left the thin c-Si grain in its wake [44]. This process is shown schematically in Fig. 7.15a-c, in which the precipitate migrates towards the right, in the direction of the arrow. The overall process was driven by the reduction in free energy due to the conversion of a-Si to c-Si, which occurred with the nucleation of c-Si on one face of the $NiSi_2$ precipitate. In addition, the chemical potential of Ni was lower at the $NiSi_2$/a-Si interface than at the $NiSi_2$/c-Si interface, and the opposite was true of the Si atoms, i.e. the Si chemical potential was lowest at the $NiSi_2$/c-Si interface. It was proposed that the crystallisation process was driven by one of two alternative mechanisms [44]. In the first model, the $NiSi_2$ dissociated at the $NiSi_2$/c-Si interface, with the Si being incorporated into the growing grain, and the Ni diffusing down the chemical potential gradient to the head of the precipitate. On reaching the $NiSi_2$/a-Si interface, the Ni reacted with a-Si to form $NiSi_2$, and propagated the grain forward. This was referred to as the dissociative Ni diffusion process. The alternative mechanism was the non-dissociative diffusion of Si directly from the $NiSi_2$/a-Si interface to the $NiSi_2$/c-Si interface to sustain the migrating-precipitate/crystallisation process. In both cases, the rate limiting process was atomic diffusion within the precipitate, and, although the specific process was not positively identified, it was tentatively ascribed to dissociative Ni diffusion [44].

Given the controlling role played by Ni (or Si) diffusion through the precipitate, faster crystallisation rates were found with thinner precipitates, and crystallite

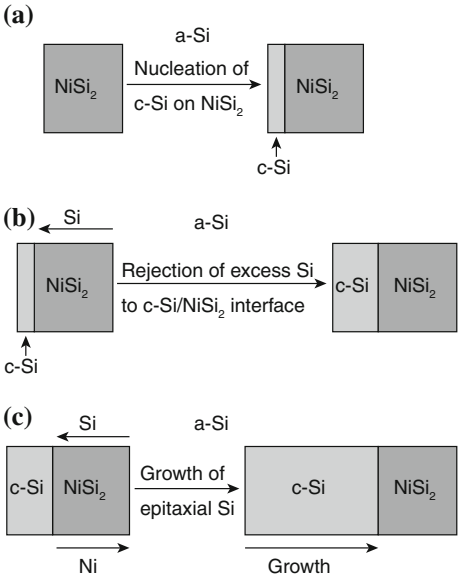

Fig. 7.15 Schematic representation of $NiSi_2$-mediated growth of c-Si grains. (Reprinted with permission from [44]. Copyright (1993) American Institute of Physics)

growth rates of 5 Å/s were measured at ~507 °C for a 50 Å thick precipitate. Progressive crystallisation of large areas occurred due to the migration, and ultimately, intersection of numerous crystalline needles from a multiplicity of seeds, and the complete crystallisation of a film doped with a dose of 5×10^{15} Ni/cm^2 occurred within 5 min at 569 °C [44]. However, the local crystallisation process was essentially one-dimensional along the extending length of the needle-like grains, and with much slower lateral growth of the crystallite width, driven by SPC alone. A UV reflectance study of the change in crystallinity of a Ni doped, 40 nm thick a-Si film, following annealing at 550 °C, showed a two-stage process, in which ~85 % crystallinity was rapidly achieved in ~4–5 h by the SMC process, but a further 100 h was needed to achieve 99 % crystallinity [46]. This slow, second stage of the process was attributed to the solid phase crystallisation of residual a-Si regions, which had remained between the needle-like grains. The activation energy of this latter process was 3.0 eV, which is consistent with the SPC process [16]. In contrast to the high activation energy for the SPC process, the activation energy for the Ni MIC process has been quoted to be 1.5–1.75 eV [43].

A variety of techniques have been used to introduce Ni into a-Si films, and these have included thin metal film deposition, co-sputtering of Ni and Si, ion implantation of nickel [46], and spin-coating of a nickel-containing pre-cursor solution [47], or localised ink-jet printing of Ni containing droplets [48]. By and large, these samples were then used for low temperature SMC over the temperature range 500–600 °C. However, one feature consistently seen in MIC TFTs was a high leakage current, which was initially attributed to Ni contamination of the poly-Si. The qualitative relationship between poly-Si quality and Ni contamination

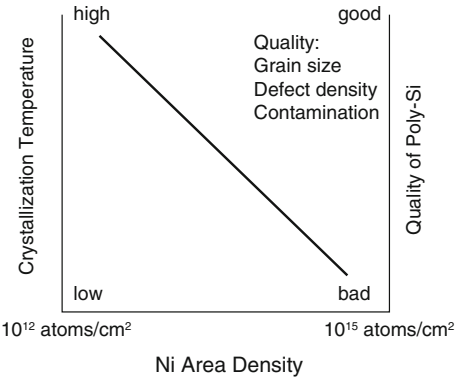

Fig. 7.16 Illustration of the relationship between Ni areal density, MIC crystallisation temperature and the resulting poly-Si quality. (Reprinted from [43] with permission of Springer SBM)

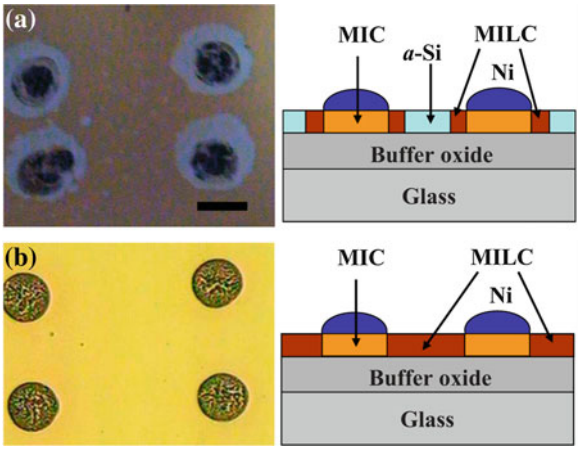

Fig. 7.17 MILC of a-Si using ink-jet printed Ni *dots* (**a**) partial inter-dot crystallisation after 2 h at 580 °C, and (**b**) full crystallisation after 6 h at 580 °C. (Reprinted with permission from [48]. Copyright (2009) American Institute of Physics)

is summarised by the plot in Fig. 7.16, which also illustrates the dependence of the crystallisation temperature on the concentration of nickel [43].

In view of the issue of Ni contamination in MIC material, there has been considerable interest in metal induced lateral crystallisation, MILC, in which the $NiSi_2$ precipitates migrate from localised Ni-doped areas into the adjacent, undoped material and crystallise this [47–51]. Optical photographs of this process are shown in Fig. 7.17a and b, in which a matrix of 80 μm diameter nickel nitrate dots had been ink-jet printed onto an a-Si film and heated at 580 °C for 2 and 6 h, respectively [48]. The lighter area around the Ni dots in Fig. 7.17a shows the extent of the lateral crystallisation beyond the dots after 2 h, and complete crystallisation after 6 h is shown in Fig. 7.17b. The two situations are illustrated schematically in the accompanying line drawings. Although lateral crystallisation can be used to reduce the level of direct Ni contamination in the poly-Si, it does not eliminate it completely. SIMS measurements have shown a 100-times reduction of the Ni concentrations in MILC areas compared with the MIC areas, but only a 10-times reduction in the precipitate areas at the head of the crystallisation front [50].

7.2.4.2 SMC Poly-Si TFTs

A survey of MIC and MILC poly-Si TFTs, fabricated within the temperature range 500–600 °C, showed that the majority of devices had electron field effect mobilities between $\sim$70 and $\sim$100 cm^2/Vs [43], which is higher than achieved with conventional SPC, but lower than with ELA. Also, the leakage currents of the SMC TFTs were higher than in good quality ELA material, typically being within the range of 1–100 $\times$ 10^{-12} A/μm (of channel width) for SMC TFTs, but $\sim 2 \times 10^{-14}$ A/μm for ELA TFTs (when measured at 5–10 V drain bias) [52]. However, direct comparisons between different publications are not straightforward due to the use of different measurement biases and different gate oxide thicknesses. Both of these parameters determine the drain field, and, as discussed in Chap. 8, the TFT leakage current, at high drain fields, is exponentially dependent upon the electrostatic field at the drain. Hence, the most useful comparisons are those made in the same publication. Nevertheless, the figure of $\sim 2 \times 10^{-14}$ A/μm quoted for ELA TFTs makes a good reference point when assessing SMC TFTs. The role of Ni contamination was highlighted when comparing MIC and MILC TFTs, with values of 8.8×10^{-12} A/μm and 3.6×10^{-13} A/μm, respectively, measured at 1 V drain bias [49]. Although the MILC device had $\sim$20 times lower leakage current than the MIC device, it was still more than 10 times higher than an ELA device. However, for Ni concentrations below $\sim 2.5 \times 10^{19}$ cm^{-3}, in MIC devices, the leakage current of $\sim 2 \times 10^{-12}$ A/μm was independent of the Ni doping level [46], suggesting contributory factors, other than metal contamination, to the leakage current, including the crystal structure.

Other authors have clarified the role of the local grain and grain boundary structures in MILC TFTs, where a continuous grain boundary has been identified at the MIC/MILC boundary, as shown in Fig. 7.18a, and a further major grain boundary has been identified when two MILC fronts meet [51]. Where these boundaries are perpendicular to current flow, and are located in the channel or at the source or drain junctions, they can be expected to degrade device behaviour. There are, thus, a variety of device configurations, with respect to these grain boundaries, determined by their relative locations, as shown in Fig. 7.18b. The device location represented by '111' encompasses all three boundaries (where the MIC regions have also been used for the source and drain regions), and '000' encompasses just the MILC material itself. Figure 7.19 shows the device structures used to engineer these two situations, where, in Fig. 7.19a, the Ni seeding region was offset from the ultimate location of the source junction, and MILC growth was unidirectional in the channel area. In Fig. 7.19b, the MIC/MILC junctions were coincident with the source and drain junctions, and the bi-directional MILC fronts met in the centre of the channel. The resulting n-channel TFT characteristics are shown in Fig. 7.20, and, interestingly, the mid-channel continuous GB had only a minor effect upon the electron mobility, by reducing it from 78 to 70 cm^2/Vs, whereas the minimum leakage current, at $V_d = 5$ V, for the '111' TFT was 3×10^{-11} A/μm compared with 2×10^{-12} A/μm for the '000' TFT [51]. Hence, the continuous GBs at the junction boundaries had a strong

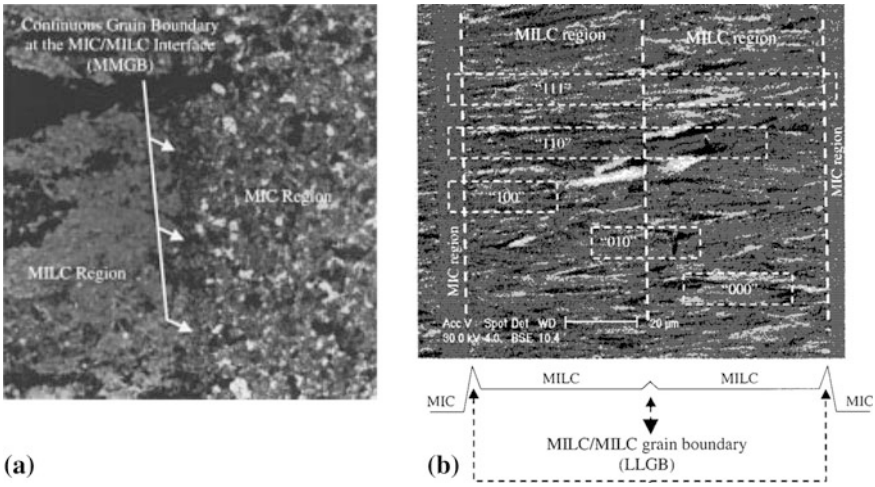

Fig. 7.18 **a** Plan-view TEM micrograph showing the continuous grain boundary at the MIC/MILC boundary, and **b** optical micrograph of MIC and MILC regions, where the numbered areas show the device locations within the material. (Reprinted from [51] with permission of IEEE)

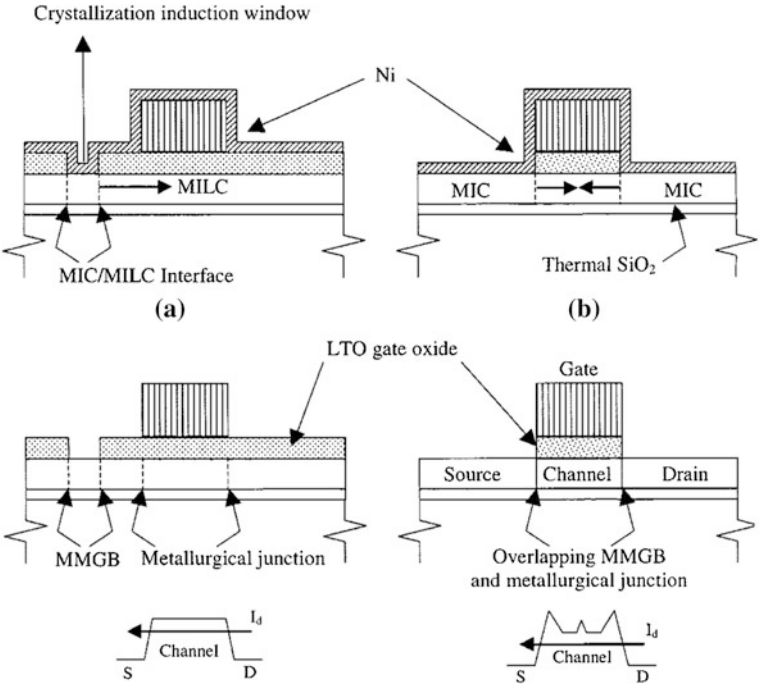

Fig. 7.19 Illustration of device and grain boundary locations within (**a**) a unilateral MILC TFT and (**b**) a MIC/MILC TFT. (Reprinted from [51] with permission of IEEE)

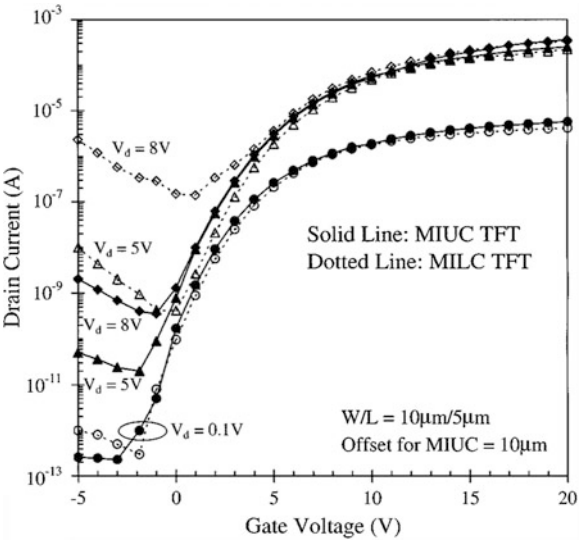

Fig. 7.20 Transfer characteristics obtained from unilateral MILC (MIUC) and MIC/MILC TFTs (see Fig. 7.19a and b, respectively). (Reprinted from [51] with permission of IEEE)

degrading effect upon the leakage current, but, even in their absence, the leakage current still remained high in the '000' device compared with ELA TFTs.

This again points to fundamental aspects of the grain structure, and not just Ni contamination or continuous grain boundaries, being responsible for high leakage currents in SMC TFTs. In confirmation of this, the only SMC devices with substantially lowered leakage currents were those in which the crystal structure was changed by a further process, such as excimer laser annealing. One example of this was with a process referred to as L-MIC [53], in which the samples used for post-MIC ELA had originally been implanted with 5×10^{13} Ni/cm^2, and then annealed at 550 °C to achieve >90 % crystallinity. These samples had typical MIC characteristics, with an electron mobility of $\sim$85 cm^2/Vs, and a minimum leakage current at $V_d = 5$ V of 2.5×10^{-12} A/μm. Following a subsequent 7-shot ELA process, the changes in electron mobility and leakage current are shown in Fig. 7.21, from which it will be seen that the minimum leakage current density was reduced to 2.5×10^{-14} A/μm, and the electron mobility increased to $\sim$210 cm^2/Vs [53]. In addition, the electron mobility results were obtained within an energy density window of $\sim$70 mJ/cm^2, which is much larger than obtained from the conventional ELA process (see Fig. 7.13 for a comparison with a conventional 10-shot ELA process), and the low leakage current could be obtained with as few as two shots with L-MIC process. The explanation for these results was that in the near-melt-through SLG regime, un-melted MIC grains at the bottom of the film seeded the re-growth, and this process also crystallised any residual a-Si regions, which had remained between the MIC grains [53].

Other groups have also employed a process comparable to L-MIC, to produce high performance TFTs, using a process referred to as continuous-grain-silicon (or CGS) [54, 55]. This implemented a MIC process in 45 nm thick films of a-Si,

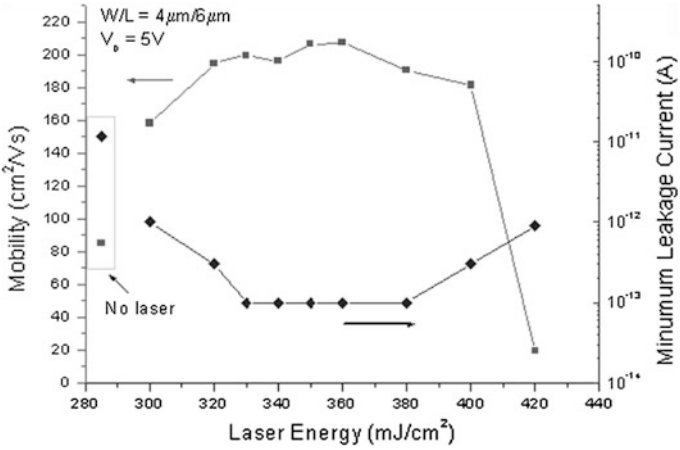

Fig. 7.21 Changes in electron mobility and TFT leakage current as a function of post-MIC ELA, using a 7-shot process. (Reprinted from [53] with permission of IEEE)

using a spin-on solution of Ni in acetic acid, and a crystallisation stage, which was carried out below 550 °C. Following the Ni-mediated crystallisation, the samples were passed through an ELA process to improve the crystal quality of the layer, and self-aligned TFTs were then made using thermally activated boron and phosphorus ion doping for the source and drain regions of p- and n-channel poly-Si TFTs, respectively. (A general discussion of poly-Si architecture and processing can be found in Sect. 7.4). The thermal activation of the phosphorus-doped regions was also described as a gettering process, which reduced the Ni content in the TFT channels. These devices were compared with ELA TFTs, in which the MIC stage had been omitted, and the CGS and ELA TFTs showed electron mobilities of 320 and 115 cm^2/Vs, respectively, and identical, low leakage currents of 5×10^{-14} A/μm (at $V_d = 1$ V) [55].

These results are comparable to the L-MIC work [53], in which the electron mobilities were higher than in conventional ELA TFTs. To clarify the differences between CGS and ELA material, the grain structures were compared by electron backscatter diffraction pattern (EBSP) analysis and by transmission electron microscopy [55]. The EBSP measurements for CGS material, within 10 μm $\times$ 20 μm sampling areas, showed that, at a pitch of 200 nm, the point-to-point changes in mis-orientation angles were just a few degrees. Whereas for a 2 μm $\times$ 2 μm area of ELA material, 30 nm point-to-point measurements gave abrupt changes of mis-orientation angle by 30–60° between grains, but was nearly zero within the grains. The absence of these large changes in the CGS material led to the identification of 7–15 μm sized 'domains', within which the misorientations were <5°. No such domains were identified in the ELA material, just individual grains in the size range 0.2–0.5 μm. In the CGS material, [111] planes dominated the crystal orientation normal to the sample surface, which was consistent with the $< 111 >$ preferred crystallisation direction of the $NiSi_2$ precipitates.

TEM analysis confirmed the sharp grain boundaries between the ELA grains, but, for the CGS material, the grains were larger than 1 μm, and were frequently separated by low angle grain boundaries. These fundamental differences between the grain structure of CGS and ELA material, with the large CGS 'domains' containing only low-angle grain boundaries, suggest reduced grain boundary scattering, explaining the higher carrier mobilities. It is also clear that the crystallographic nature of this material, even after the ELA treatment, contains a grain structure strongly influenced by the original Ni-mediated crystallisation process.

In summary, the SMC process was originally investigated as a low cost, and simpler, alternative to conventional ELA, but, for reasons still not fully clarified, the resulting poly-Si TFTs suffered from unacceptably high leakage currents. However, when combined with an ELA process, the leakage current issues were resolved, and higher performance TFTs, than from ELA alone, were fabricated [52–55]. Moreover, as shown in some of this work [53], this could be achieved with a low-shot ELA process and a large process window.

7.3 Gate Dielectrics

The preferred gate dielectric for poly-Si TFTs is silicon dioxide, as it is for single crystal Si devices, in contrast to the use of silicon nitride, which is preferred for a-Si:H TFTs. As discussed in Chap. 5, the preference for a-SiN_x:H in a-Si:H TFTs is determined by the meta-stability of this material and the reduced DOS resulting from the positive charge in the nitride. For poly-Si, these meta-stability considerations do not apply, and the positive charges in the nitride cause unnecessarily large negative shifts in threshold voltage; in addition, the nitride itself is also susceptible to gate bias induced trapping instabilities. These reasons also militate against the use of Si_3N_4 in MOSFET devices. In the following section, the use of SiO_2 as a gate dielectric is discussed, and there is a brief review of alternative dielectrics in Sect. 7.3.2.

7.3.1 Silicon Dioxide

The quality of the gate oxide in a TFT is crucial to the performance of the device, and the oxide needs to have low leakage current, low densities of fixed charges and interface states, high breakdown field, low pin-hole density, and good bias-stress stability. Moreover, for the low temperature TFTs of interest in this book, the oxide deposition process must be implementable below the glass softening point, and, for practical purposes in commercial processing, this means below $\sim$450 °C, and, finally, over large areas with good uniformity. The temperature constraint rules out the thermally grown oxide, which has underpinned the crystalline silicon integrated circuit industry. Nevertheless, the properties of thermal oxides have

been widely used as a benchmark against which to measure TFT oxides, and the closer these properties have matched the better has been the performance of the low temperature oxides. The correlation of electrical properties, such as the density of states at the Si/SiO_2 interface, can be readily understood, but even mechanical properties such as the etch rate in hydrofluoric acid is a good indicator of the density of the film [56], and this density has been correlated with the films porosity and its propensity to absorb water [57]. Furthermore, this porosity has been associated with gate-bias-stress induced threshold voltage instability in the TFT, due to the motion of adsorbed H^+ and OH^- ions in the oxide [58]. Hence, a number of simple measurements have been used to screen potential oxide candidates.

A powerful technique for the assessment of the porosity of the film, and its water content, has been thermal desorption spectroscopy (TDS), [57], in which, as the temperature of the film is steadily raised, the desorbed gases from the film are analysed in a mass spectrometer, set to atomic mass 18, to detect water. The TDS plots in Fig. 7.22 were obtained from films deposited by PECVD from TEOS (tetraethylorthosilicate) and O_2 in helium carrier gas, and show three characteristic water desorption peaks obtained from SiO_2 films. The two low temperature peaks at 100–200 and 150–300 °C have been associated with adsorbed water at room temperature in porous films. This was confirmed by noting that the heights of these peaks could be increased by prolonged air exposure at room temperature, and decreased by vacuum annealing at elevated temperatures. Hence, dense, low porosity films should show minimal desorption peaks at these two temperatures. The high temperature peak at 350–650 °C was associated with isolated silanol, Si–OH, bonds formed during film growth, and, unlike the lower temperature peaks, was seen in all high quality oxides. As will also be seen from Fig. 7.22, the overall peak heights were determined by the TEOS + He/O_2 flow ratios, and the highest oxygen dilution ratio led to the densest and least porous film.

In addition to the use of TEOS and O_2 gas mixtures in PECVD reactors [57, 59], SiO_2 depositions can also be obtained from SiH_4 and N_2O gas mixtures [42, 60, 61].

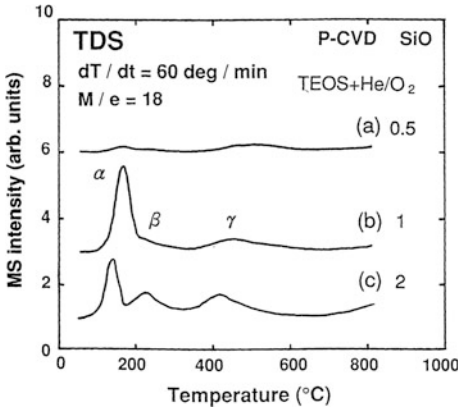

Fig. 7.22 Thermal desorption spectra (TDS) measured on PECVD TEOS films of SiO_2, deposited with different levels of TEOS + $He:O_2$ dilution. (Reprinted with permission from [57]. Copyright (1993) The Japan Society of Applied Physics)

These PECVD depositions at 300–400 °C are typically carried out in parallel plate reactors operating at 13.56 MHz, or 27 MHz, and, given the large area capabilities of these reactors [59], PECVD deposition is the mainstream technique used for the deposition of high quality gate oxides for poly-Si TFTs. As mentioned above, the highest quality oxides have been obtained at low growth rates, which were achieved by a large dilution of the silicon bearing gases by using high volumes of either oxygen or helium carrier gas [56, 57, 60, 61].

Other oxides, which have been examined as possible gate dielectrics in poly-Si TFTs, have included deposition by:

- APCVD from SiH_4, and O_2 [58],
- remote plasma, RPCVD, from SiH_4, O_2 and He at 300–350 °C [62],
- ECR-CVD at 2.45 GHz from SiH_4, O_2 and He at 25–270 °C [63, 64].

Comparative TDS measurements from some of these low temperature oxides are shown in Fig. 23a [61] and b [65], and it will be seen from Fig. 7.23a that only the helium-diluted SiH_4/N_2O films deposited at 250–300 °C showed low porosity, which also correlated well with an etch rate comparable to thermal SiO_2 [60]. Hence, the minimum deposition temperature for this oxide is above 250 °C, which is not a problem for TFTs on glass, but is an issue for TFTs on low-temperature polymer substrates. However, low-deposition-temperature ECR oxides were of high density and low porosity, and are possible candidates for poly-Si TFTs on polymer substrates [64]. This topic is discussed further in Chap. 11. The TEOS oxides in Fig. 7.23b were deposited above 300 °C with high O_2 dilution ratios, and compare well, in terms of low porosity, with the helium diluted SiH_4/N_2O reference sample, and are widely used in state-of-the-art TFT processing. The APCVD oxides in Fig. 7.23a show large, low temperature desorption peaks, which, as mentioned above, have been correlated with gate bias instability in TFTs [58], and these oxides are not compatible with high quality TFTs.

The other essential treatment in producing a device quality oxide is a post-deposition anneal in the temperature range 300–400 °C to reduce both the fixed oxide charge in the film and the interface state density [56, 60, 63, 64]. This is the same as the low temperature hydrogen passivation anneal, used with thermal oxides in MOSFET technology, to reduce both of the above states. Hydrogen containing ambients, such as forming gas, or wet-N_2, are used, and the treatment is frequently carried out after final metallisation, and may be referred to as a post-metal anneal. In the latter case, reducing gate metals, such as aluminium, can react with hydroxyls in the film releasing hydrogen even in an inert annealing ambient such as N_2. In order to avoid the problem of separating interface trapping states from trapping states in the poly-Si film itself, the assessment of this treatment is usually carried out by C–V measurements of the film deposited onto a lightly doped silicon substrate. Figure 7.24 demonstrates the effectiveness of a forming gas anneal at 400 °C on a dense, helium diluted SiH_4/N_2O oxide deposited at 350 °C, in which the positive charge density in the oxide was reduced from $\sim 8 \times 10^{11}$ to $\sim 2.5 \times 10^{11}$ cm^{-2}, and the near-mid-gap interface density was reduced from $\sim 1 \times 10^{12}$ to $\sim 4 \times 10^{10}$ $cm^{-2}eV^{-1}$ [56].

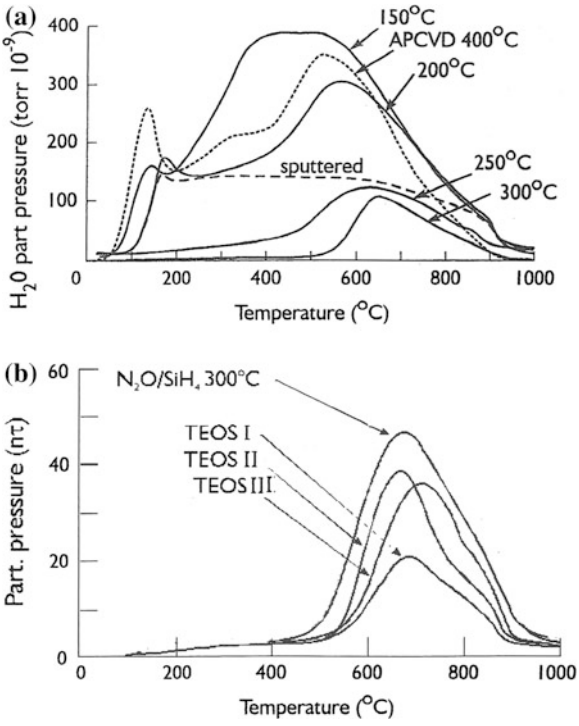

Fig. 7.23 TDS spectra of SiO_2 films (**a**) by PECVD deposition using He-diluted SiH_4/N_2O gases at different temperatures, plus an APCVD film and a sputtered film (Reprinted from [61] with permission of SID), and (**b**) various PECVD O_2-diluted TEOS films together with a reference He-diluted SiH_4/N_2O film (unpublished data from Dr N D Young of Philips Research)

Whilst the above post-deposition anneal is extensively used, various other post-deposition annealing regimes have been reported as leading to an improvement in oxide quality, such as an excimer laser anneal, at an energy below the silicon melt-threshold, which led to improvements in carrier mobility, oxide charge density and gate bias and drain bias stress stability [66]. Another procedure giving similar results was a high-pressure water vapour anneal at 1.3 Mpa and 260 °C [67]. However, it is not clear that these, or other techniques, have achieved widespread

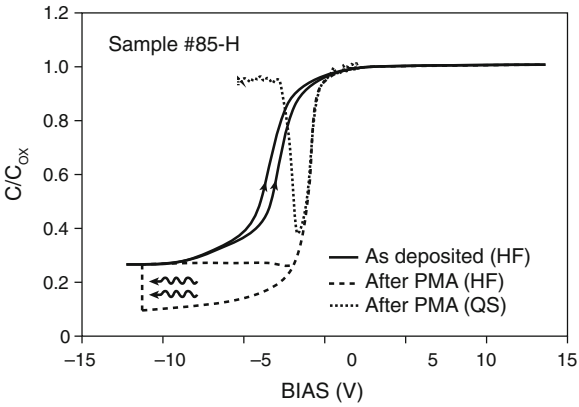

Fig. 7.24 MOS high frequency and quasi-static C–V measurements on a 350 °C PECVD He-diluted SiH_4/N_2O SiO_2 film, before and after a post-metallisation anneal, PMA, at 400 °C for 30 min. (Reprinted with permission from [56]. Copyright (1986) American Institute of Physics)

application. Moreover, there is always a cost consideration in implementing a more complex processing schedule, which needs to be balanced against the level of improvements which might be achieved when applied to the current state-of-the-art high performance TFT process.

In terms of basic dielectric properties, the dense, helium diluted SiH_4/N_2O oxides display a high breakdown field of ~ 8 MV/cm, as shown by the large area (5.2×10^{-3} cm^2) capacitor results obtained from single crystal Si substrates [56], and by the large area poly-Si TFTs ($W = L = 100$ μm) in Fig. 25a and b, respectively. The latter results demonstrate a thickness independent breakdown field, which is important for short channel TFTs, where the gate oxide thickness needs to be scaled down with reducing channel length in order to suppress short channel effects. The use of SiO_2 films down to 20 nm thickness is demonstrated in this data, but at 10 nm thickness premature breakdown was observed, indicating the current limit of oxide thickness scaling. This probably results from a combination of the rough poly-Si surface, giving poor film integrity at this thickness, as well as step coverage problems over the edges of the poly-Si islands. In the following section, some alternative dielectric strategies are discussed for thin oxides.

In addition to the gate dielectric application, high quality oxides are also needed for interlayer dielectrics separating different levels of metallisation, such as the gate and drain layers, and also for capping the glass substrates. The capping layer has the double purpose of providing an electronically well-controlled layer at the back interface of the TFT, as well as acting as a diffusion barrier to alkali ions

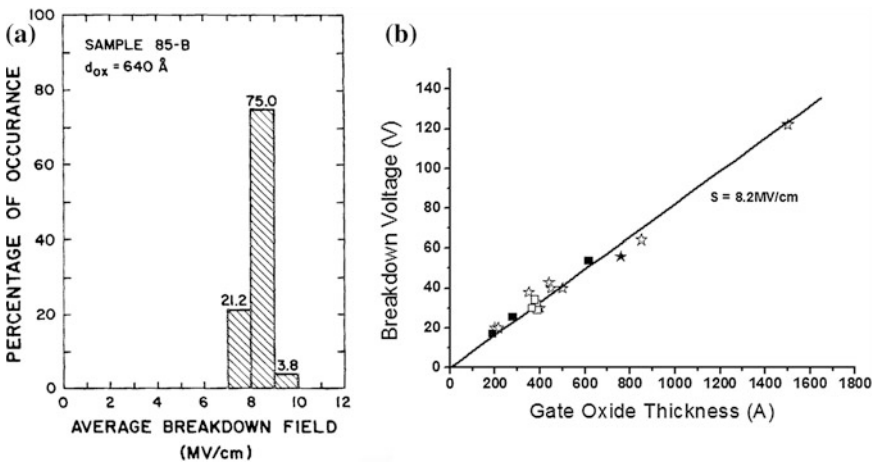

Fig. 7.25 Electro-static breakdown measurements on He-diluted SiH_4/N_2O SiO_2 films (**a**) breakdown field of large area capacitors of 64 nm thick films on c-Si substrates (Reprinted with permission from [56]. Copyright (1986) American Institute of Physics), and (**b**) breakdown voltage measurements as a function of SiO_2 film thickness in poly-Si TFTs (Reprinted from [76] with permission of SID)

from the substrate. In fact, for the latter purpose, it is common to deposit SiN directly onto the glass surfaces, as it is a better diffusion barrier than SiO_2, and then to cap this with SiO_2. Typical thicknesses for these two layers are 100 nm SiN and 400 nm SiO_2.

7.3.2 Alternative Dielectrics

In sub-0.1micron channel length MOSFETs, the scaling of gate oxide thickness has resulted in ultra thin SiO_2 films of <15 Å, where leakage current and reliability concerns have become important issues. This has led to the study of high-k dielectrics [68] as a way to use thicker films, whilst still maintaining the same equivalent oxide thickness, EOT, and, hence, the same g_m. There have not been the same fundamental issues with the SiO_2 layers used in poly-Si TFTs, but, as discussed in the previous section, a limit has been identified in the minimum thickness of SiO_2, which can be reliably used, and some investigations have been reported on the use of higher-k dielectrics for this TFT application. The dielectric constant of SiO_2 is 3.9, and the two alternative dielectrics were PECVD a-SiN_x:H (k = 6.5) [69] and sputtered Ta_2O_5 (k = 11–25) [70]. (The dielectric constant for bulk Ta_2O_5 is 25, but the thin film layers only gave a value of 11.) In both cases, a dual dielectric approach was followed, in which a thin layer of SiO_2 was used as an interfacial layer between the poly-Si and the high-k dielectric. This process was adopted in order to maintain the electronic quality of the poly-Si/SiO_2 interface.

For the dual dielectric system, the EOT is given by:

$$EOT = t_{SiO_2} + \frac{3.9t_2}{k_2}$$

where t_2 and k_2 are the thickness and dielectric constant of the high-k layer, respectively.

The p- and n-channel devices made with the a-SiN_x:H/SiO_2 dielectric contained either 5 nm or 10 nm thick layers of SiO_2, and gave good TFT characteristics down to an EOT of 9.8 nm. The device parameters such as mobility, breakdown field and drain bias stability were largely independent of the SiO_2 layer thickness [69], and this dielectric combination is a plausible route to thin oxide TFTs with an EOT at least down to 10 nm.

The TFTs with the SiO_2/Ta_2O_5 gate dielectric had a minimum EOT of 46 nm, and needed several hours post-metallisation annealing, at 350 °C in mixed gas, to achieve low threshold voltages and high carrier mobilities [70], indicating the need for further optimisation of this higher-k system in order to achieve an acceptable combination of TFT performance and processing schedule.

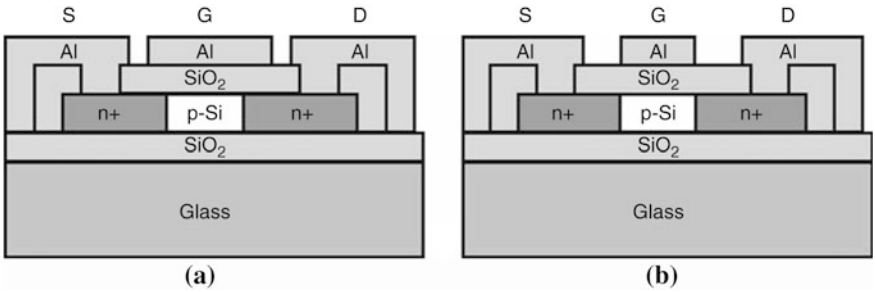

Fig. 7.26 Schematic cross-sections of n-channel, top-gated poly-Si TFTs (**a**) non-self-aligned architecture, and (**b**) self-aligned

7.4 Poly-Si TFT Architecture and Fabrication

7.4.1 Architecture

Poly-Si TFTs are most commonly implemented as top-gated structures, as shown in Fig. 7.26a and b for non-self-aligned (NSA) and self-aligned (SA) devices, respectively. As will be seen, this is a different architecture from the inverted staggered architecture of a-Si:H TFTs (see Chap. 5), and is much more similar to the architecture of single crystal silicon-on-insulator (SOI) MOSFETs. Further points of similarity with the SOI MOSFETs, and distinction from a-Si:H TFTs and emerging TFT processes in organic or amorphous oxide materials, are that both n-channel and p-channel poly-Si TFTs, with comparable performance, can be fabricated with a common process. Secondly, the source and drain doping is usually accomplished using ion shower doping of boron for p-channel TFTs and phophorus for n-channel TFTs. This process has a number of similarities to ion implantation for MOSFETs, in that both involve the high-dose implantation of selected ions. In other words, the architecture and a key fabrication stage of poly-Si TFTs are closer to MOSFETs than to devices fabricated in other thin film materials. However, this high-dose ion doping process is potentially damaging to the crystallographic order of the poly-Si film, particularly for the heavier phosphorus ion compared with boron. The degree of damage will be determined by the ion dose, ion energy and substrate temperature, and, it has been shown that, for high enough doses into single crystal silicon, the damage can be sufficient to cause complete amorphisation of the implanted layer [71]. This is also an issue in poly-Si, and is discussed further in Sect. 7.4.1.1.

The essential difference between the two architectures in Fig. 7.26 relates to the formation of the source and drain regions, and this determines the overlap of the gate electrode across these regions. For the NSA structure, with significant overlap, the source and drain regions can be ion doped prior to the crystallisation of the film, and the dopants in these regions will then be activated during film crystallisation. This process can be implemented with direct ion doping into bare a-Si,

and results in a high level of dopant activation, with minimal residual ion damage. A doping process employing a phosphorus dose of 1×10^{15} cm^2 at 10 keV, typically gives a doped region sheet resistance of $\sim$300 ohms/square. Subsequent to this stage, the gate dielectric is deposited and defined, followed by gate, drain and source metal deposition and definition. The overlap between the gate metal and the doped source and drain regions is determined by the alignment rules for the process, and is likely to be up to $\sim 3\mu$m. This is a simple and robust fabrication procedure, and is well suited to the basic study of material parameters (as described in Sect. 7.2), but the architecture suffers from larger parasitic gate-drain capacitance, which will degrade high frequency transistor performance. In addition, it is not well suited to the fabrication of shorter channel devices ($L < 3\mu$m) due to alignment issues, and the possibility of uncontrolled channel shortening due to lateral diffusion of the source and drain dopant during the laser crystallisation stage.

The above limitations are removed with the SA architecture, but, in several respects, it results in a more complex fabrication process, primarily associated with the source and drain doping stage, which is discussed in the following section.

7.4.1.1 Self Aligned Source and Drain Doping

The self-alignment between the edges of the gate and the edges of the source and drain regions is achieved by using the gate electrode as an ion doping mask during the doping stage, which means that the dopants are implanted through the gate dielectric. In order to penetrate this layer, the doses and energies will be larger than those used for the NSA TFTs. Furthermore, as the doping occurs after the transistor channel layer has been crystallised, a further processing stage has to be introduced to activate the dopant: this can be either a second pass through the laser or a thermal activation process in a furnace, or by rapid thermal annealing, RTA. For the furnace process, the constraints imposed by the glass substrate dictate a low thermal budget, such as a few hours at a maximum temperature of 450 °C, and relies upon the re-growth of the ion-damaged film being seeded by an undamaged poly-Si layer at the bottom of the film. Hence, to ensure this seeding, full film amorphisation must be avoided, otherwise the thermal budget will increase to the values quoted in Sect. 7.2.1 for the SPC process. As mentioned above, amorphisation is a more serious issue with the heavy phosphorus ions, and the effects discussed below were not seen with boron doping for p-channel TFTs. Figure 7.27 shows the variation of poly-Si sheet resistance as a function of phosphorus ion dose, and compares laser and furnace activation. With laser activation, the sheet resistance varied inversely with phosphorus dose, as would be expected, but, with furnace activation at 450 °C, this was only seen at the lower doses. At the higher doses, the sheet resistance began to increase with dose and, at the highest dose, it was above the measurement limit of 1×10^6 ohm/square. A broader data set showed that there was a critical combination of ion energies and doses [72], above which thermal activation at 450 °C was ineffective. This was confirmed to be due

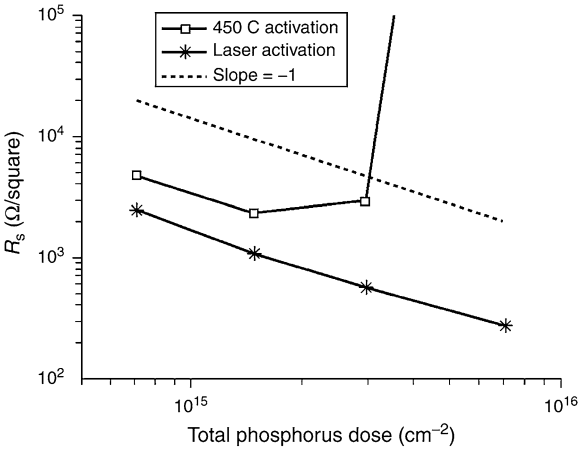

Fig. 7.27 Variation of sheet resistance of phosphorus implanted poly-Si as a function of dose and activation method (80 keV implant through 145 nm of SiO_2)

to film amorphisation, since doses, which could not be activated in 40 nm thick films, could be activated in 80 nm thick films. Finally, it should be noted that even where furnace activation was achieved, it resulted in a higher sheet resistance than obtained with laser activation. This is likely to be due to lower dopant solubility at the lower temperature. Hence, from the standpoint of comparing phosphorus activation, the 450 °C process resulted in higher sheet resistance and a smaller useable dose range than laser activation. A similar difference in the sheet resistance between laser activated and thermally activated regions was also found when higher temperature rapid thermal annealing was used instead of a 450 °C furnace process [73].

Further issues in the SA doping process are revealed when the resulting TFT transfer characteristics, processed with furnace or laser activation, are compared in Fig. 7.28 [72]. One obvious feature in these curves, and in other publications [74, 75], is the higher minimum leakage current in the laser-activated n-channel TFTs, which is due to residual ion-doping damage at the edge of the drain junction [72, 75]. Cross-sectional TEM of a more heavily phosphorus-implanted sample showed a 200 nm wide residual amorphous region, located in the doped region near the gate edge, and also extending beneath the gate [34] (due to lateral end-of-range damage not exposed to the laser). Very similar results have been reported in arsenic doped n-channel TFTs, where the leakage current and TEM-imaged crystallographic damage in the exposed silicon near the gate edge have been correlated with diffraction of the laser beam by the gate edge [75].

Another feature in Fig. 7.28 is the lower on-current in the furnace activated n-channel TFT, due to this activation process giving higher sheet resistance in the source and drain regions, as shown in Fig. 7.27. Finally, the field effect mobility extracted from laser crystallised n-channel TFTs was less than from identically crystallised NSA TFTs [72]. As with the leakage current, this has also been seen in arsenic doped TFTs, and, again, associated with the diffraction-induced residual damage effects at the gate edge [75]. This damage can also have a significant

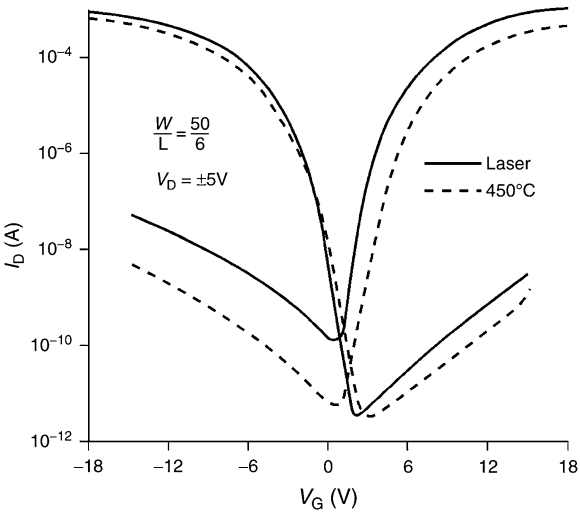

Fig. 7.28 Transfer characteristics of self-aligned n- and p-channel poly-Si TFTs, showing the influence of laser or furnace dopant activation. (Reprinted with permission from [72]. Copyright (1998), The Electrochemical Society)

impact upon the operation of short channel TFTs [75–77], as shown by the field effect mobility results in Fig. 7.29 [76]. The mobility values in this figure were corrected for the series resistance in the doped regions themselves, and were used to calculate the parasitic resistance specifically induced by the phosphorus ion doping process.

Various techniques have been reported for minimising the general ion doping damage effects in SA n-channel TFTs, including a careful control of ion dose and energy [72]. For the laser activation process, in particular, oblique-incidence laser irradiation has been shown to minimise the gate-edge diffraction [78], and, thereby, reduce the associated damage effects on leakage current and carrier mobility. A technique producing comparable results is the use of an off-set gate, in which the gate length is reduced by lateral etching after ion doping, so that the diffraction and masking effects at the gate edge no longer interfered with the full

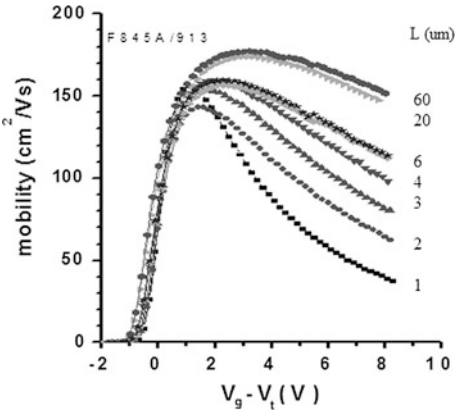

Fig. 7.29 Dependence of electron field effect mobility measurements on channel length, for SA aligned n-channel poly-Si TFTs. (Reprinted from [76] with permission of SID)

melting of the doped region. This can lead to complete damage removal, as shown in Fig. 7.30 by the TFT characteristics of a device with a 0.5 μm off-set gate [34]. The off-set gate is also one of a number of techniques, to be discussed in Sect. 7.4.1.2, for reducing the field at the drain edge, which are used to improve the drain-bias-stress stability of poly-Si TFTs. Finally, laser activation, followed by furnace activation, can be used to reduce the leakage current to the lower value seen in furnace activated TFTs.

As is apparent from the above discussion, the process for fabricating SA TFTs, with minimal performance artefacts, is considerably more complex than the NSA TFT process, and this is the reason for favouring the use of NSA TFTs for basic poly-Si materials studies, such as those presented in Sect. 7.2. However, the potentially superior performance of SA TFTs, due to lower parasitic capacitances, and their better compatibility with sub-micron channel length TFTs makes them the preferred choice for many poly-Si applications.

7.4.1.2 Drain Field Relief

When poly-Si TFTs are exposed to a drain-bias stress, there can be a critical fall-off in performance, as illustrated by the results in Fig. 7.31. The exposure of the device, to a 13 V drain bias for 60 s, led to an increase in off-state current and a reduction in on-state current, as well as a major change in the shape of the output characteristics [79]. This phenomenon has been widely ascribed to hot electron damage [80, 81], and the physics of this process are discussed in Chap. 8, where it is shown that an alteration in device architecture is needed to suppress this instability. The architectural change is one in which the field at the drain/channel

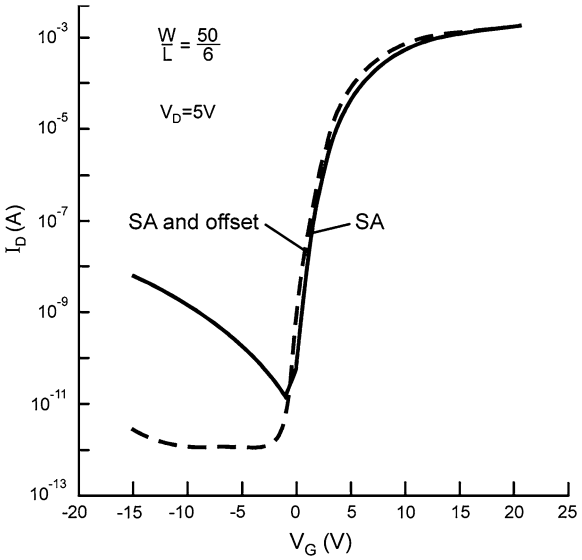

Fig. 7.30 Effect of gate offset in removing the residual ion doping damage from laser activated n-channel SA poly-Si TFTs. (Reproduced with permission from [34])

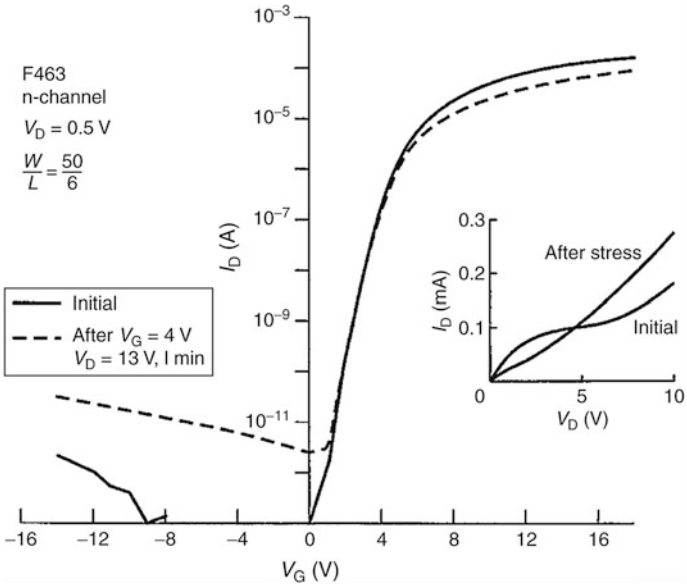

Fig. 7.31 Influence of drain bias stress of 13 V for 60 s on NSA TFT transfer characteristic. The insert shows its effect upon the output characteristic. (Reprinted with permission from [79]. Copyright (1998) The Japan Society of Applied Physics)

junction is reduced, and this is most easily accomplished by the use of lightly doped drain (LDD) regions, as shown schematically in Fig. 7.32a and b. These two figures illustrate two LDD variants, where the lightly doped region is either external to the gate, or is overlapped by the gate (GOLDD). In both cases, an extra masking and processing step is involved to form this region, and, as with the drain region itself, the LDD region is formed by phosphorus ion doping, but with a lower dose in the poly-Si. (It is typically in the range $5 \times 10^{12} - 5 \times 10^{13}$ cm^{-2}, in contrast to the fully doped drain region where the dose is likely to be in the range $5 \times 10^{14} - 1 \times 10^{15}$ cm^{-2}). When the region is defined photo-lithographically, its size will be determined by the process design rules, and is likely to be of the order of 1–3 μm.

The qualitative trade-off with dose is that lower doses will give more field relief, and hence, better stability, but a larger series resistance, and hence, lower on-current. This trade-off is minimised with GOLDD, where the gate modulates the conductivity of the GOLDD region, and it also gives better device stability (see Chap. 8). However, as with the NSA architecture, GOLDD gives greater parasitic capacitances, and is less compatible with short channel length devices.

To obtain sub-micron LDD regions, a non-lithographic definition procedure is required, such as the lateral etch-back of the gate, as used to form the off-set gate. With this technique, the gap can be left undoped, with reliance upon the lateral diffusion of the drain dopant, during a laser activation stage, to dope the LDD region. Alternatively, a low dose implant can be used to deliberately dope the

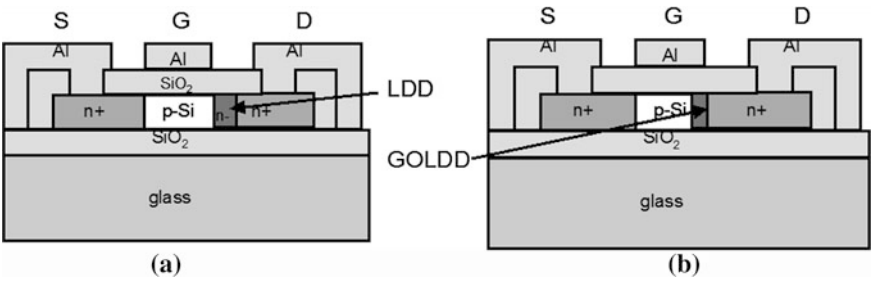

Fig. 7.32 Cross-sectional diagrams of SA poly-Si TFTs showing LDD regions (**a**) conventional LDD, and (**b**) gate overlapped LDD, GOLDD

region [82]. This procedure requires good control of the lateral etching process, because too large a gap will give increasingly large series resistance in the on-state.

A potentially more controllable sub-micron process is to use a sidewall spacer on the gate to define either an undoped off-set gate [83], or a doped LDD region, which can be a GOLDD region if the spacer itself is conducting [84].

7.4.1.3 Other TFT Architectures

Although the top-gated structures discussed above are the most widely used, bottom gated NSA TFTs have been implemented [85]. SA bottom gate TFTs have also been demonstrated by using backside exposure of photoresist on the top of the plate, where the bottom gate acts as an in situ mask to define the channel length [86].

It is also possible to fabricate NSA top-gated TFTs, without using ion doping, by sequentially depositing intrinsic a-Si and n^+ doped a-Si, and removing the n^+ a-Si from the channel region [87]. This is similar to the back-channel-etch process in a-Si:H TFTs (see Sect. 5.3.1). Following the clearance of the channel region, laser crystallisation is used in the normal way on both channel and doped regions, and is followed by gate oxide deposition, contact window opening, and metallisation to complete the TFT fabrication process.

7.4.2 Fabrication Process

Two examples of the poly-Si TFT fabrication process are shown in Figs. 7.33 and 7.34, and these list both the major processing steps and the photolithography stages. The fabrication of a simple NSA n-channel TFT (whose cross-section is in Fig. 7.26a) is listed in Fig. 7.33, and it is a 4-mask process involving the definition of the poly-Si island, the source and drain doping locations, contact window opening through the gate oxide, and definition of the metal contact areas. The SA

1.	Glass plate capping by SiN and SiO_2	
2.	a-Si:H deposition by PECVD	
3.	De-hydrogenation at 400-450°C in N_2	
4.	Poly-Si island definition	M1
5.	Low dose B^+ ion doping	
6.	Source and drain definition, and P^+ ion doping	M2
7.	Laser crystallisation	
8.	Gate oxide deposition by PECVD	
9.	Contact window definition	M3
10.	Source, drain and gate metal deposition and definition	M4
11.	Anneal at 350°C in N_2/H_2 to sinter contacts	

Fig. 7.33 Fabrication stages for non-self-aligned poly-Si n-channel TFTs

n-channel TFT (see Fig. 7.26b) is also a 4-mask process, with island definition, gate metal definition, contact window opening, and source and drain metal definition. These 4-mask process flows are the minimum number of mask stages needed to fabricate a device without field relief. For the fabrication of an AMLCD, with CMOS drive circuits and stable n-channel TFTs, an increase in the number of depositions and mask stages is needed, and a 9-mask process is shown in Fig. 7.34. Compared with the single channel TFTs, the extra stages are separate photolithographic definitions for the source and drain areas for the n- and p-channel TFTs, definition of the LDD area for the n-channel TFTs, contact windows for the ITO pixel electrodes, and the ITO patterning itself.

For both architectures, two other stages are frequently necessary, namely, dehydrogenation, and low dose B^+ doping, in steps 3 and 5, respectively. The a-Si:H pre-cursor film typically contains $\sim$10 % hydrogen, and, if this film is exposed to a top-hat laser beam, there will be an explosive release of hydrogen, causing severe blistering of the film. A low temperature thermal anneal at 400–450 °C is used to reduce the hydrogen content to $\sim$1 % or less, at which level the film can be exposed to a top-hat beam without risk of mechanical damage. An alternative to this process is higher temperature deposition of a-Si, giving a lower H-content, or multi-shot irradiations at increasing energy density, to progressively heat the film leading to controlled out-diffusion of the hydrogen [88]. The same effect can also be achieved with a shaped laser beam, in which the leading edge is much less sharp than in the top-hat beam [89]. This leads to more gradual heating of the film over several incrementally higher intensities, giving controlled exo-diffusion of hydrogen before the film is ultimately exposed to the maximum laser beam intensity.

The low dose boron ion doping is used to compensate for an intrinsic electron richness in the crystallised poly-Si film, which is due to a combination of positive charges in the oxides above and below the film, and/or the neutral level of the poly-Si band-gap states being above mid-gap. The net effect of these centres is to shift the threshold voltage of the TFTs in a negative direction. Boron doping is

1.	Glass plate capping by SiN and SiO_2	
2.	a-Si:H deposition by PECVD	
3.	De-hydrogenation at 400-450°C in N_2	
4.	Poly-Si island definition	M1
5.	Low dose B^+ ion doping	
6.	Laser crystallisation	
7.	Gate oxide deposition by PECVD	
8.	Gate metal deposition and definition	M2
9.	LDD definition & P^+ ion doping (n-channel only)	M3
10.	Definition of n-ch source, drain, and P^+ ion doping	M4
11.	Definition of p-ch source, drain, and B^+ ion doping	M5
12.	Dopant activation (laser or furnace)	
13.	Capping oxide deposition	
14.	Contact window definition	M6
15.	Source and drain metal deposition, and definition	M7
16.	Anneal at 350°C in N_2/H_2 to sinter contacts	
17.	Capping oxide deposition	
18.	Contact window definition	M8
19.	ITO deposition and definition	M9

Fig. 7.34 Fabrication stages for a poly-Si AMLCD, containing complementary self-aligned TFTs, and with LDD field relief for the n-channel TFTs

used to compensate this shift, and to achieve symmetrically positioned transfer characteristics of p- and n-channel TFTs either side of $V_G = 0$ V (as seen with the characteristics in Figs. 7.9 and 7.28).

Much of the processing of poly-Si TFTs and AMLCDs can be accomplished with the equipment used for the fabrication of a-Si:H AMLCDs, and this would include plate cleaning, photolithography and etching stages, as well as the deposition of various metals such as aluminium and ITO. Also, the PECVD deposition of the gate oxide and a-Si:H precursor films can be deposited in standard, large area PECVD reactors, using the same deposition conditions as for the a-Si:H TFT films. However, there are also large area PECVD reactors, which can deposit a-Si at temperatures up to ~400–450 °C, and incorporate an in-situ de-hydrogenation anneal, so that the films are ready for laser crystallisation without any further treatment [90]. The additional items of equipment needed for poly-Si TFTs are a laser crystallisation system [18], and a large area ion doping system [91]. The ion doping system will deliver a rectangular (or ribbon-shaped) beam of ions, through which the substrate plates are scanned in a direction parallel to the short axis of the beam. The beam will not have the high-resolution mass-separation of a semiconductor industry ion implanter, but will have sufficient ion mass filtering to ensure that hydrogen is excluded from the beam, that phosphorus and boron cross-contamination is avoided, and that for a phosphorus doping stage, say, only P^+ ions are selected, whilst other species such as P_2^+ are removed. (The original ion doping systems lacked these refinements.) The other item of equipment, which

might be employed, is a high-resolution photolithography station, if short channel TFTs are used for the addressing circuits. These will need higher resolution than the 3μm typically available with the large area LCD-industry aligners.

7.5 Advanced Processing

7.5.1 Large Grain Poly-Si

As discussed above, the conventional ELA technique produces devices with limited electron mobility (<200 cm^2/Vs), limited throughput and a small laser processing energy window. Various techniques have been explored to address some of these problems, with one aim also being larger grain poly-Si, giving higher carrier mobility. These techniques have included both solid state green lasers, as well as modified excimer laser crystallisation procedures. The modified excimer laser procedures include sequential lateral solidification (SLS) [29, 92–94], phase modulated excimer laser annealing, PMELA [1, 95–97], and a micro-Czochralski process, μ-Cz, for location controlled single grain growth [98, 99]. In all these cases, a technique has been developed to control and extend lateral grain growth during the SLG process, rather than relying upon the random process, which occurs during conventional ELA. These techniques are discussed in Sect. 7.5.2.

As briefly discussed in Sect. 7.2.3, solid state green lasers have been advocated to overcome some of the technical and cost of ownership issues with ELA, as well as being able to produce large grain material [35–42], and these approaches are presented in Sect. 7.5.3. Finally, a comparison is made between the excimer and green laser approaches in Sect. 7.5.4.

7.5.2 Modified Excimer Laser Crystallisation

The SLS and PMELA techniques are conceptually similar in that both procedures expose the substrate to a spatial intensity fluctuation, varying from a below-melt-threshold intensity to a value high enough to fully melt the silicon film. At the boundary between these two regions, there will be a portion of material which will experience near-melt-through conditions, where the normal SLG process will occur. Those grains seed lateral growth into the adjacent fully molten regimes, giving grain growth of a few microns or more. SLS directly achieves the intensity fluctuation by passing the laser beam through a projection mask, containing alternate clear and occluded regions. With PMELA, the laser beam is passed through a phase shifting mask, so that optical interference in the emergent beam produces the required intensity fluctuation. However, the implementation is different, with SLS using a multi-shot scanning procedure to promote grain

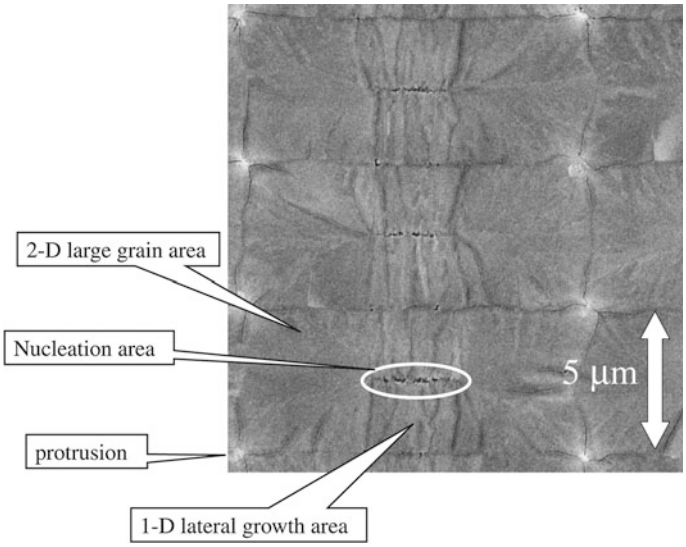

Fig. 7.35 SEM micrograph of location-controlled large grain arrays grown by PMELA. (Reprinted with permission from [96]. Copyright (2008) The Japan Society of Applied Physics)

propagation, whereas PMELA uses a single shot technique to produce an array of location controlled large-grain (or single crystal) areas, typically 5 μm square, as shown in Fig. 7.35 [96]. The SEM micrograph shows a combination of large grain areas, lateral growth areas plus the nucleation area. To achieve this well defined, location-controlled grain structure, with a robust fabrication process, the phase shift mask has evolved from its original, simple form, of etched depressions in a quartz plate [95], to a complex matrix of variably sized pits and humps on the quartz plate, which is referred to as a 2-dimensional bipolar phase modulator plate, 2-D BPM [96, 97].

The large grains from the SLS and PMELA processes yielded high electron mobility values of up to $\sim$600 cm^2/Vs [93] and $\sim$900 cm^2/Vs [1], respectively. For the PMELA assessment, TFTs with W = 2 μm and L = 1 μm were used, so that they were entirely contained within the 5 μm × 5 μm large-grain areas. In $\sim$10 % of these grains, both p- and n-channel PMELA TFTs matched the performance of single crystal SOI MOSFETs, which were identically processed (apart from the crystallisation stage). These high performance TFTs were located in regions of {100} pseudo-single-crystal (PSX) material; however, as the PSX regions accounted for only 10 % of the crystallised areas, techniques still need to be established to improve uniformity by generating this orientation in all crystallised regions [1].

In contrast, to the above two techniques, the μ-Cz technique [98] requires the Si film to be patterned rather than modulating the incident laser beam. This is achieved photo-lithographically, by etching shallow, small diameter (<100 nm) holes into a layer of SiO_2 which is subsequently coated with a-Si. The a-Si film

fills the holes, so that the Si film thickness at these points is greater than on the surrounding surface, and, when exposed to a laser intensity sufficient to melt the surrounding film, the film remains solid at the bottom of the hole. Hence, there will be a transition region in the hole, within which the normal ELA process will form some crystallites, and these will seed lateral grain growth into the surrounding molten Si, as shown schematically in Fig. 7.36a [99]. By controlling the diameter of this hole, it can act as a grain filter and reduce the number of seeding crystallites to unity, with the objective of producing single crystal areas. As with the PMELA technique, this procedure has been implemented to produce an array of square, abutting grains, whose sides are ~ 6 μm in length, with the seeding region sited in the centre of these grains. The grain structure is shown in Fig. 7.36b, and electrical assessment of the material was carried out with small channel TFTs (W and L ~ 2 μm), which were able to fit within the individual grains [99]. Figure 7.36b illustrates different TFT positioning within the grains, and those sited directly over the grain filter, such as 'C', had the worst characteristics. For those TFTs horizontally or vertically displaced from this location, such as 'X' or 'Y', the device

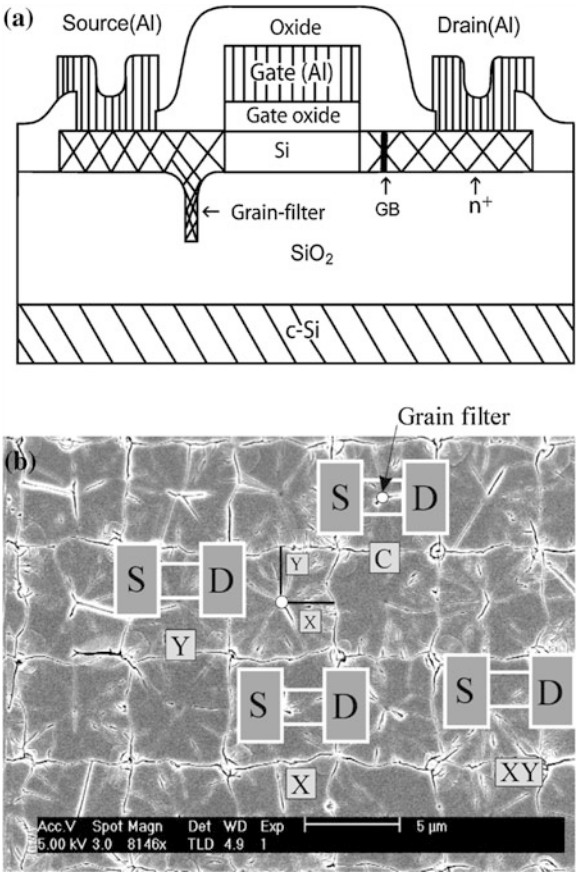

Fig. 7.36 **a** Cross-sectional diagram of μ-Cz process and c-Si TFT channel sited within a single grain, and **b** SEM micrograph of an array of location controlled grains grown by the μ-Cz technique. Superimposed on this image are TFT locations with respect to the grain filter positions. (Reprinted from [99] with permission of IEEE)

characteristics were much better, with electron mobilities up to $\sim$600 cm^2/Vs. However, the standard deviation in these values was $\pm$100 cm^2/Vs [99], and it is likely that uniformity improvements will be needed for routine implementation of this process.

Both the PMELA and μ-Cz processes have been implemented with single shot crystallisation, whilst the minimum shot number in SLS is two, and all processes use beam intensities sufficient to cause full melt-through. Hence, these techniques offer the potential for higher throughput and a larger energy density processing window than conventional ELA (in addition to the improved TFT performance through higher carrier mobility). At the moment, the SLS technique appears to be the closest to commercial implementation [100], and it will be described in more detail in the following section.

7.5.2.1 Sequential Lateral Solidification

As mentioned above, SLS uses a spatially varying beam intensity, which consists of a number of beamlets, just a few micrometers wide in one direction and several millimetres in the other. The beamlets are produced by projecting the homogenised excimer laser beam through a mask having alternate clear and occluded stripes [29, 32], and the ensuing crystallisation process is shown schematically in Fig. 7.37a–c. Within the high intensity beamlet areas, full film melting takes place and, at the edge of these regions, there will be an SLG region, which seeds the lateral growth into the molten region. Following single shot irradiation, two scenarios are shown, depending upon the relative widths of the beam, W_B, and of the seeded lateral growth distances, L_{lat}. For $L_{lat} < W_B/2$, the centre of the molten region undergoes random nucleation before the lateral growth front reaches this region, and results in fine grain material in the centre of each exposed stripe. To avoid this happening, the beamlet size needs to be $<\sim$5 μm (in contrast to the conventional line beam ELA, in which the beam is $\sim$350–500 μm wide), resulting in the situation shown in Fig. 7.37c. In this case, the two lateral growth fronts meet in the centre of the previously melted region, and produce a collision-front grain boundary. In the orthogonal direction, there are low angle sub-grain boundaries running parallel to the lateral growth direction.

Following this first shot, the material consists of alternating stripes of a-Si and poly-Si, and further irradiations are required to complete the crystallisation process, as shown schematically in Fig. 7.38a and b. In Fig. 7.38a, the plate is moved a distance Δx prior to the next irradiation, where $\Delta x < W_B/2$, such that the original melt-front-collision GB is melted by the second pulse, and the remaining polycrystalline material seeds further lateral growth, propagating the grain to the right. With an appropriate projection mask design, this process can be indefinitely repeated to produce grains tens or hundreds of micrometres long. The main constraint with this implementation of the process is the throughput, which will inversely scale with the number of grain-propagating laser shots.

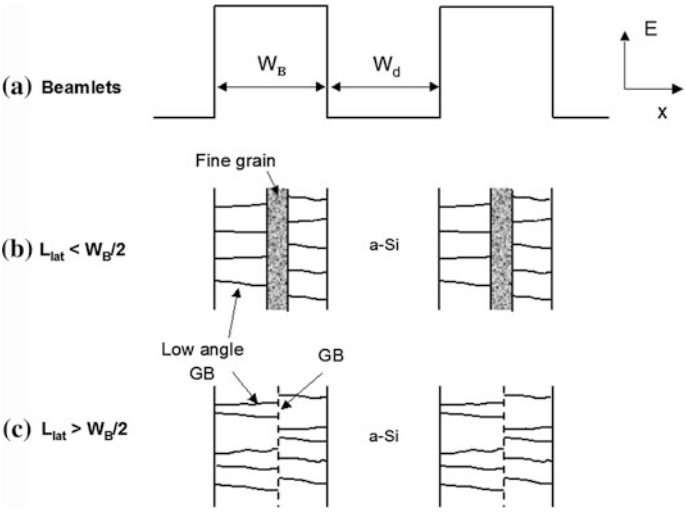

Fig. 7.37 Schematic illustration of the SLS process: **a** micro-beamlets of width W_B, separated by gap W_d, **b** lateral grain growth, and random nucleation when W_B is too large, and **c** complete crystallisation of the melted area when W_B is less than the ateral growth limit

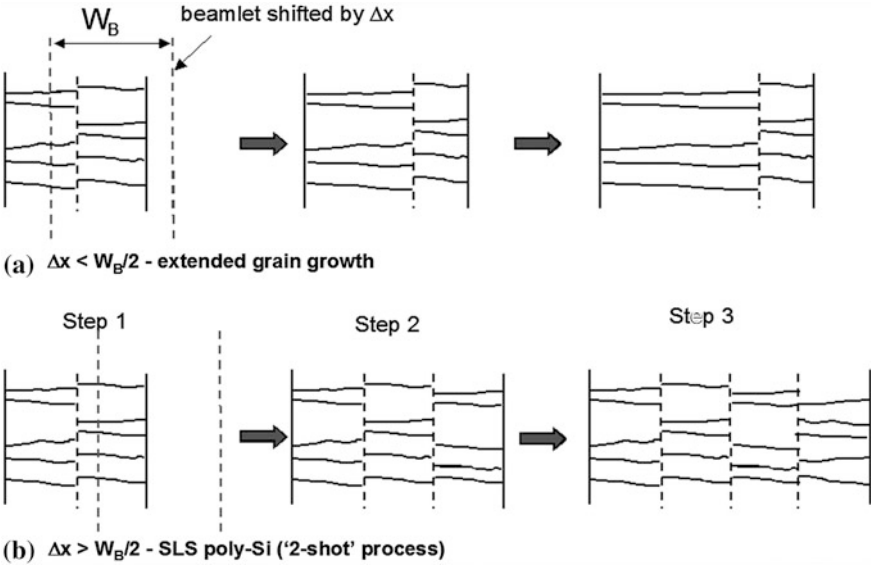

Fig. 7.38 Illustration of the SLS grain propagation process: **a** generation of extended grain material, where the beamlet stepping interval, $\Delta x < W_B/2$, and **b** repeating array of poly-Si grains, where $\Delta x > W_B/2$

When $\Delta x > W_B/2$, the situation shown in Fig. 7.38b is produced, and the original collision-front grain boundary is retained, and a similar grain structure is generated by the second irradiation. With an appropriate mask design, this process can be implemented as a 2-shot process, giving the highest throughput obtainable with SLS. The grain structures resulting from these two SLS implementations are shown in Fig. 7.39a and b, respectively [100]. Figure 7.39a is an SEM micrograph of the multi-shot grain propagation process, giving grains >15 μm long, with closely spaced sub-grain boundaries running parallel to the propagation direction. The spacing of these sub-grain boundaries increases with increasing film thickness [101], and, with increasing grain propagation, there is grain filtering and a tendency for the low-angle sub-grain boundaries to become high-angle [102]. The micrograph in Fig. 7.39b is of the 2-shot SLS process, showing the regularly spaced collision-front grain boundaries, as well as the low-angle sub-grain boundaries.

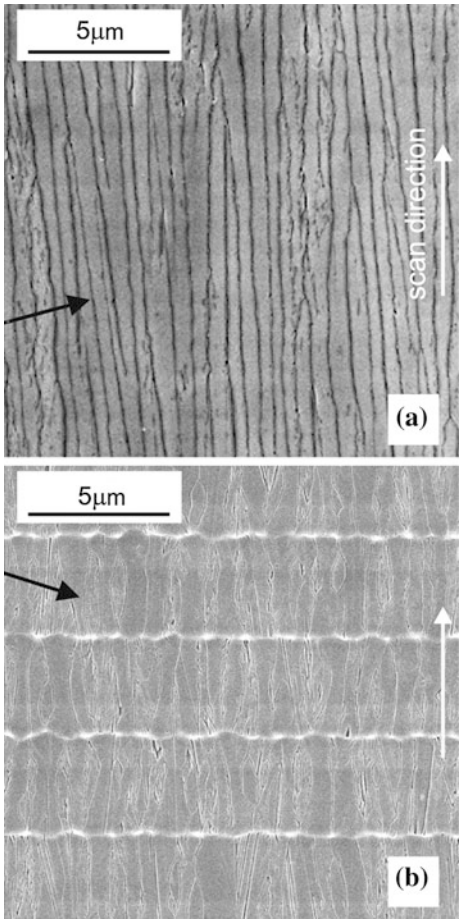

Fig. 7.39 SEM micrographs of SLS Si: **a** extended grain material, and **b** '2-shot' SLS poly-Si. (Reprinted from [100] with permission of ITC'07)

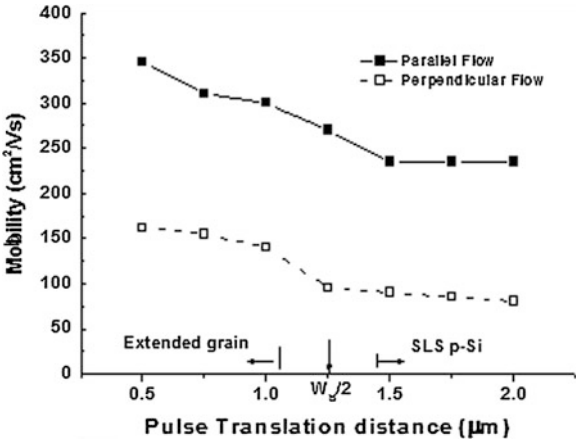

Fig. 7.40 Variation of electron mobility with pulse translation distance, Δx, in SLS material, for carrier flow parallel and perpendicular to the low angle grain boundaries. The demarcation line between extended grain and '2-shot' SLS poly-Si is shown at $\Delta x = W_B/2$ ($W_B = 2.5$ μm, $t_{Si} = 100$ nm)

Some of the characteristic features of SLS material are shown by the TFT results in Fig. 7.40 [103]. The electron mobility is plotted as function of the substrate translation distance between pulses, Δx, and results are shown for carrier flow parallel and perpendicular to the sub-grain boundaries. These results were taken from 100 nm thick poly-Si films, with a sub-GB spacing of 0.37 μm. The two major features in this plot are, firstly, the reduction in mobility for carrier flow perpendicular to the sub-grain boundaries, due to the GB anisotropy giving greater carrier scattering in this direction of current flow. Secondly, for parallel flow, the reduction in electron mobility from $\sim$300–350 cm^2/Vs to $\sim$240 cm^2/Vs, with increasing plate translation distance, is due to the change in material from the extended grain form ($\Delta x < W_B/2$) to '2-shot SLS' material containing regularly spaced collision-front grain boundaries ($\Delta x > W_B/2$). Qualitatively identical results have also been obtained for the hole mobility in p-channel TFTs. Within the two specific types of material, extended grain and '2-shot SLS', the process was able to yield good mobility uniformity of ±6–7 %, and ±2–3 %, respectively [103]. The better uniformity of the '2-shot' material was most likely due to better averaging of grain properties over those much smaller grains. In other work, optimisation of the high throughput, '2-shot SLS' process has given electron mobility values up to 350 cm^2/Vs [94].

The above discussion has focussed on the formation of 'directional' material by scanning line-beamlets. The technique can also be implemented to give localised single crystal regions by the use of chevron shaped beamlets [29], or by implementing the 2-shot process in two orthogonal directions [104]. However, 'single crystal' SLS material has not been electrically characterised as intensively as the PMELA and μ-Cz materials.

7.5.3 Green Laser Crystallisation

Diode pumped solid state lasers have been advocated to address both the pulse stability and cost of ownership issues associated with ELA, and Q-switched Nd:YAG and CW Nd:YVO_4 lasers have been the most widely used solid state lasers [35–42]. The fundamental output wavelength from both lasers is 1064 nm, and, in order to achieve efficient absorption into thin a-Si films, the second harmonic phase at 532 nm has been utilised, where the absorption depth in a-Si and poly-Si is 100 nm and 125 nm, respectively [24]. This is $\sim$10 times greater than the absorption depth of 308 nm radiation, so that the coupling efficiency is smaller, although the authors of the green laser work argue that the greater absorption depth gives a more uniform temperature profile in the silicon, which is discussed further below.

7.5.3.1 Pulsed Nd:YAG Lasers

In the Q-switched mode at 532 nm, Nd:YAG lasers can deliver short duration pulses ($\geq$10 ns) of 800 mJ/cm^2, with a repetition frequency of 4 kHz and an output power of 200 W [35]. The basic beam shape from a Nd:YAG laser is circular, with a Gaussian distribution of energies across its diameter, and an a-Si crystallisation system has been developed in which this shape has been optically converted into a line-beam [35]. In this system, the length of the line beam, which had a top-hat profile, was 105 mm, whilst, in the short direction, the Gaussian shape was retained, with a full width at half maximum of 40 μm, as shown in Fig. 7.41. For crystallisation, the plate scanning direction was parallel to the short axis, with typical translation stage movements of 1–5 μm between pulses [35–37], giving a multi-shot process of 40–8 shots, respectively. The pre-cursor a-Si films were typically in the thickness range 50–100 nm, and, when crystallised into poly-Si, three energy

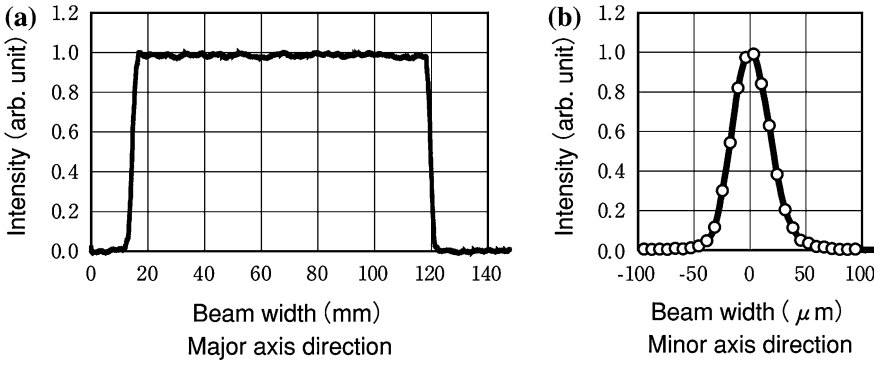

Fig. 7.41 Beam profile measured in 532 nm, Q-switched Nd-YAG laser crystallisation system. (Reprinted from [35], with permission of Ulvac)

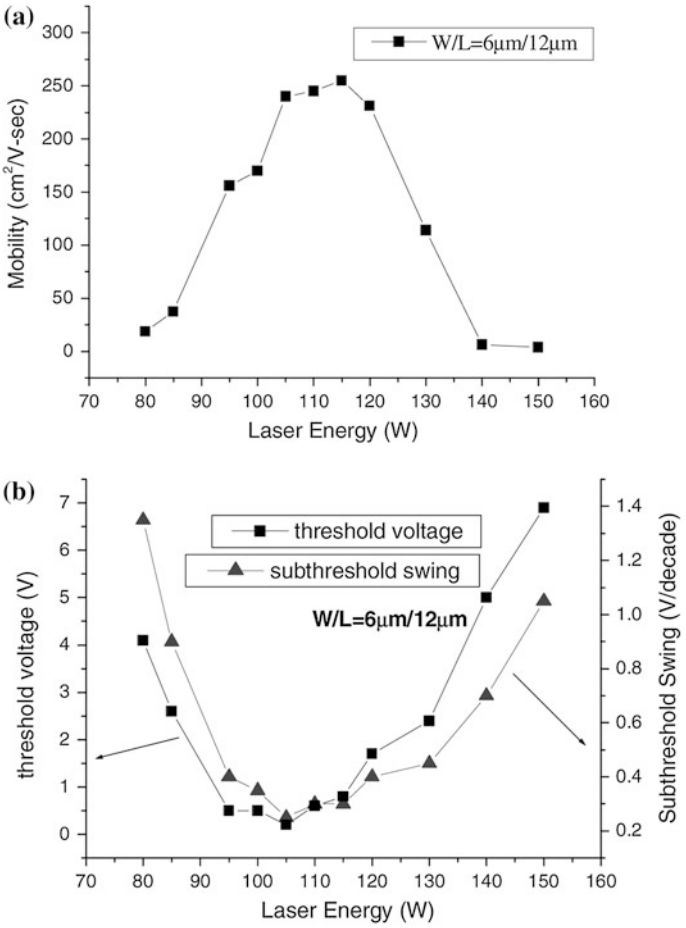

Fig. 7.42 Dependence of TFT characteristics on Q-switched 532 nm Nd:YAG laser power (**a**) electron mobility, and (**b**) threshold voltage and sub-threshold slope. (Reproduced with permission from [36])

density regimes were identified [36]: the first, at low energies (85–95 W laser power), was referred to as vertical crystallisation, and gave grains of ~100 nm, or more, in partially melted films. The second regime (105–120 W) was named SLG, which occurred when the film had fully melted and yielded larger grains, and the third regime (above 130 W) yielded fine grain material. When the TFT device parameters were measured as a function of laser power, as shown in Fig. 7.42, they showed a good correlation with the power-dependent grain structure, and gave a maximum electron mobility of 250 cm^2/Vs over the optimum laser power range of ~105–120 W for a 20 shot process [36]. As will be apparent, these regimes, and the associated device properties, are similar to the regimes identified with ELA. However, the authors argue that there is a fundamental difference due to the ~10 times

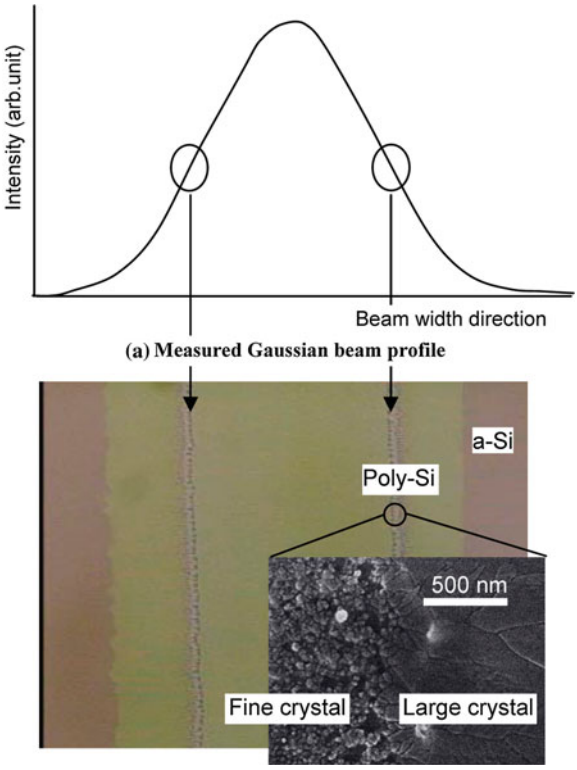

Fig. 7.43 Relationship between Q-switched 532 nm Nd:YAG laser beam profile and local poly-Si grain morphology. (Reprinted from [37] with permission of SID)

larger absorption depth of the green laser [35–37], which produces a more uniform temperature distribution through the depth of the film. As a result of this, the SLG process does not start from the bottom interface, but from the edges of the melted area [35–37]. In support of this argument, the micrographs in Fig. 7.43 show fine grain silicon in an area fully melted by the Nd:YAG beam, with large grain silicon appearing at a specific energy density on the edge of the irradiated area. Moreover, it was shown that this laterally seeded large grain region could be laterally propagated as the plate is stepped through the beam, leading to a larger processing window and larger grains than with the standard ELA process. The process comparison, in terms of the range of energy densities over which high carrier mobility TFTs can be produced, is shown in Fig. 7.44 [37].

However, this Nd:YAG process appears to be similar to the SLS process [29], discussed in Sect. 7.5.2.1, which also operates in full melt-through, relying upon seeded crystallisation from the edges of the melted areas, and uses small plate stepping intervals of 2–3 μm to propagate large sized grains. In view of these similarities between Nd;YAG irradiations and excimer SLS, the features of the Nd:YAG process cannot be uniquely attributed to the greater optical absorption depth of 532 nm radiation in a-Si. Indeed, as discussed above, in Sect. 7.2.2.2, the

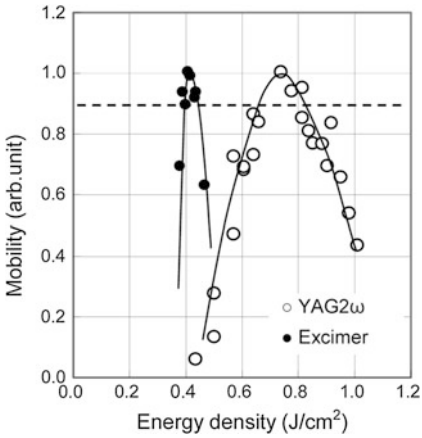

Fig. 7.44 Comparison of electron mobility and processing window sizes for ELA and Q-switched Nd-YAG crystallisations. (Reprinted from [37] with permission of SID)

large thermal diffusion length in a-Si leads to full melting of excimer laser irradiated thin films up to at least ~200 nm.

In summary, pulsed Nd:YAG crystallisation can lead to a larger process window, and potentially higher performance devices than conventional ELA, together with good pulse-to-pulse stability and lower cost of ownership. However, SLS also offers a larger processing window, and better device performance than conventional ELA. From a manufacturing perspective, system throughput and complexity are also important considerations, and these are compared in Sect. 7.5.4.

7.5.3.2 CW Nd:YVO_4 Lasers

For CW crystallisation, Nd:YVO_4 lasers are preferred to Nd:YAG lasers, as they operate with higher power and can deliver 10 W at 532 nm, with a power stability of better than 1 %. However, the conditions for successful crystallisation, using the high power CW laser, were more restrictive than for pulsed lasers, with the major problems being de-lamination of the a-Si film and damage to the glass substrate. To avoid these problems, the a-Si film was pre-patterned into discrete islands, rather than left undefined, and the preferred patterning was into close-packed 50 μm × 200 μm lozenge-shaped areas, with an inter-island spacing of 5 μm [39, 40]. These areas were large enough to accommodate 1–2 TFTs with W = 3 μm and L = 5 μm. Secondly, crystallisation of films thicker than 300 nm damaged the glass substrate, and, to avoid this, the a-Si thickness range was restricted to 50–150 nm, and, thirdly, high speed scanning at more than 20 cm/s was required. All these measures served to limit both the amount of energy absorbed by the film and coupled into the substrate, although clearly the power setting of the laser played a role as well.

The laser spot size was 200 μm × 20 μm, which was scanned in a direction parallel to the short axis along the length of the pre-defined a-Si islands. The resulting crystal structure displayed a strong interdependence on scan speed and

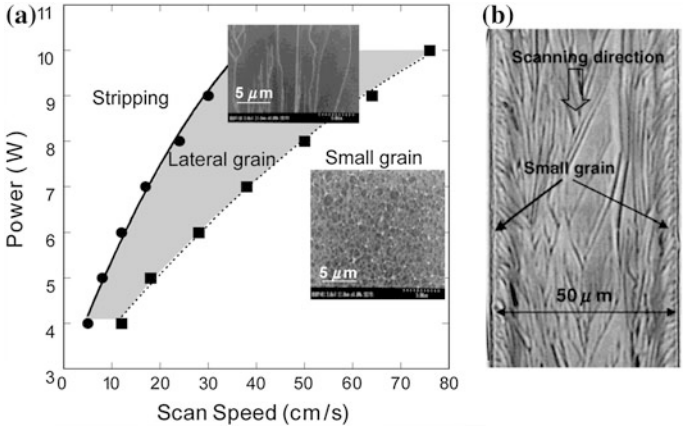

Fig. 7.45 CW Nd:YVO_4 laser crystallisation of poly-Si at 532 nm: **a** dependence of grain size and structure on laser power and scan speed, and **b** optical micrograph of pre-defined Si island, showing the Secco-etched large grain poly-Si in the centre of the island. (Reprinted with permission from [40]. Copyright (2002) The Japan Society of Applied Physics)

laser power setting, as shown by the results for 150 nm thick films in Fig. 7.45a [40]. Three crystallisation regimes were identified: at low power or high scanning speeds, small grain silicon was formed, whose appearance (as shown by the insert), at 10 W and 100 cm/s, was comparable to the SLG grains in ELA processing, whilst at 200 cm/s the grain structure was more consistent with solid phase crystallisation [39]. At higher powers and/or slower scan speeds, large laterally propagated grains were formed (see insert), whose dimensions were $\sim 3\ \mu m \times 20\ \mu m$, with the grain boundaries running parallel to the beam scanning direction. At the slowest scan speeds and highest powers the film and substrate were damaged.

The large grains were formed preferentially in the central regions of the pre-defined Si islands, because faster cooling rates along the edges of the islands resulted in smaller grains there, as shown in Fig. 7.45b. The transfer characteristics from high performance p- and n-channel TFTs, formed in a 150 nm thick film crystallised with 6 W, at a scan speed of 20 cm/s, are shown in Fig. 7.46. The high carrier mobility was attributed both to the large grain size and to the (100) surface orientation of these grains (although 100 nm thick films had a mixture of (110) and (111) oriented grains). The more general dependence of electron mobility on plate scan speed is shown in Fig. 7.47, together with the associated grain structures. The TFT transfer characteristics in Fig. 7.46 were for carrier flow parallel to the grain boundaries, and the data in Fig. 7.47 are for carrier flow both parallel and perpendicular to the grain boundaries. For perpendicular flow in the large grain material, the mobility was considerably lower than for parallel flow, which is similar to the situation with SLS silicon, due to the scattering effect of the grain boundaries. For the smaller grain, ELA-like material, the grains were equi-axed and there was no anisotropy in electron mobility.

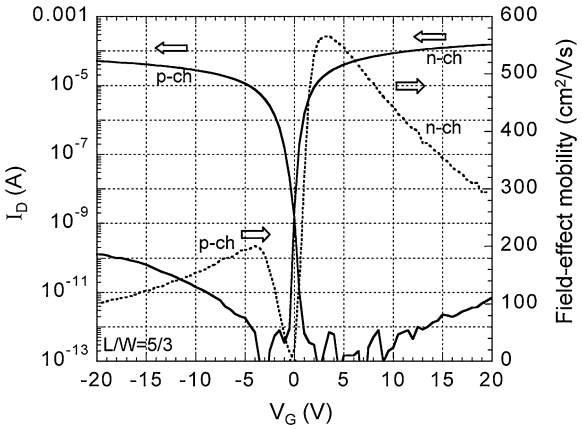

Fig. 7.46 Transfer characteristics of n- and p-channel large grain TFTs crystallised by CW Nd:YVO_4 laser at 532 nm. (Reprinted with permission from [40]. Copyright (2002) The Japan Society of Applied Physics)

The uniformity of device characteristics has not been published [39, 40]. However, in view of the spatial variation in grain structure across the width of the crystallised islands (shown in Fig. 7.45b), there must be some concern, although earlier work on unpatterned films showed better uniformity than ELA [41].

There is clearly a trade-off in scan speed and material quality with this process, and this issue is compared with SLS and pulsed Nd:YAG crystallisation in the next section.

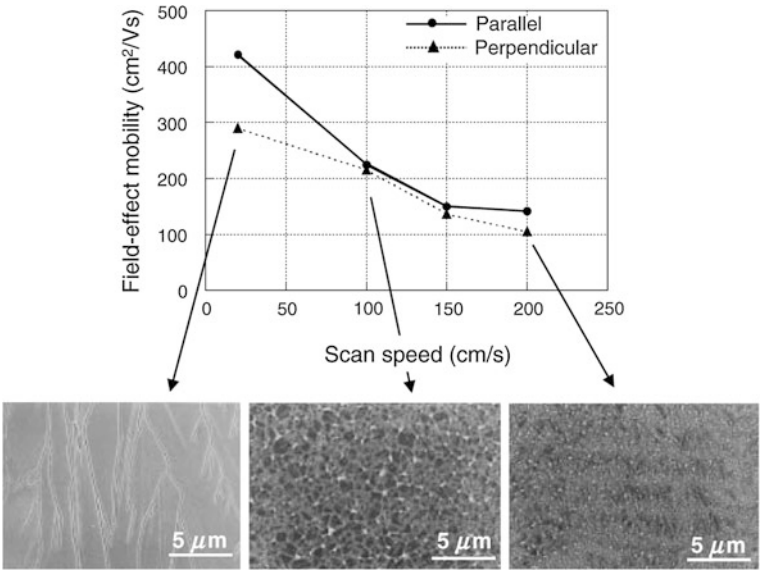

Fig. 7.47 Electron field effect mobility (for parallel and perpendicular current flow) and grain structure as a function CW Nd:YVO_4 laser scan speed. (Reprinted with permission from [39]. Copyright (2002) The Japan Society of Applied Physics)

7.5.4 Comparison of Large Grain Crystallisation Systems

All the crystallisation systems considered in this section can produce large grain, high quality TFT material, as well as being revealing tools with which to investigate the crystallisation process itself. Where a direct comparison can be made, they also offer a solution to some of the technical issues with conventional ELA, such as the size of the processing window and the associated pulse stability problem, and, in the case of the solid state lasers, they offer lower cost of ownership. These latter points are largely manufacturing issues, and a key consideration in this industrial context is plate throughput. To a large extent, throughput will scale with both the power of the system, which will determine the beam area and shot frequency, and with the efficiency of the usage of this power, which will also embrace the number of shots in the process. Taking these simple considerations into account, the crystallisation rate, R, can be calculated using: $R = \frac{A_b f}{N}$ for pulsed lasers, and $R = \frac{A_b v}{L_{\min}}$ for the CW laser. Where A_b is the beam area on the plate, f is the pulse frequency, N is the number of shots in the process, v is the plate scan velocity, and L_{min} is the small axis beam dimension.

The key features of the ELA [18], SLS [32, 94], pulsed Nd:YAG [35] and CW Nd:YVO_4 [39] systems are compared in Table 7.2, where a first order estimate of throughput is provided by the crystallisation rate, R. It should be emphasised that this is only a first order estimate as it does not account for the deceleration period of the plate translation stage at the end of each scan, and its movement and acceleration intervals for the next scan. In addition, the smaller the beam dimensions, the more scans will be needed to crystallise a whole plate, and the more significant the scan interruptions will be.

From this table, it is clear that the throughput of the Nd:YAG system is significantly lower than the ELA system, although it offers a larger process window, better pulse stability and lower cost of ownership. To what extent these beneficial features offset its lower throughput would need to be determined in a manufacturing environment. However, the overall system costs will play a role, as these determine whether it is economic to have a larger number of Nd:YAG systems as a way of maintaining the required plate processing capacity. It is also interesting to

Table 7.2 Comparison of crystallization rates in different laser annealing systems

Laser system	Power (W)	Beam size (cm × cm)	Freq (Hz)	Shot no.	Step size (μm)	Scan vel (cm/s)	Crystn rate (cm^2/s)
ELA [18]	600	$46.5 \times 3.5 \times 10^{-2}$	600	20	17.5		48.8
SLS [32, 100]	315	2.5×0.15	300	2	2.5		56.3
Nd:YAG [35]	200	$10.5 \times 4.0 \times 10^{-3}$	4000	20	2		8.4
Nd:YVO4 [39]	10	$4.0 \times 10^{-2} \times 2.0 \times 10^{-3}$	CW			50	2

note that the crystallisation rate figures for these two systems do not simply scale with system power (for the same shot number), as there is a further discrepancy by a factor of two when normalising R by power. Whilst, the overall optical efficiency of the two beam shaping systems will play a role here, there is also reduced coupling efficiency of the 532 nm radiation into the thin film because of its larger absorption depth. Hence, if a given absorbed energy density is required to melt a film of a given thickness, a higher incident density will be required with the 532 nm laser. For a given maximum output pulse energy, the incident energy density will be determined by the final beam dimensions, A_b, on the plate, and this directly controls R.

Given the sub-optimal absorption from green lasers, the use of a solid state, 445 nm blue laser has been reported [105]. The radiation at this wavelength will be more strongly absorbed, but this is an undeveloped process, with no device results reported to date.

The CW Nd:YVO4 system produces large grain material comparable to the 2-shot SLS process, and avoids the SLS system complexity of projection masks and the high resolution optical system required to produce 4–5 μm beamlets. However, its crystallisation rate is ~25 times lower than the SLS system. In recognition of this low basic crystallisation rate, a high throughput system has been designed [41], in which a number of laser sub-beams were used to simultaneously, and selectively, irradiate just the TFT areas of a display plate. This is shown in Fig. 7.48, and a crystallisation rate of 48 cm^2/s was calculated using sixteen 30–50 μm sub-beams, scanned at 2 m/s, in order to crystallise pixel TFTs at a pitch of 148 μm [41]. At this high scan speed, the electron mobility was ~150 cm^2/Vs (see Fig. 7.47), which is perfectly adequate for pixel TFTs. The peripheral driver TFTs occupy a much smaller area than the display area, but a higher carrier mobility is beneficial. For these areas, four 150 μm sub-beams were scanned at 50 cm/s, delivering a crystallisation rate of 2.4 cm^2/s, and produced TFTs with an electron mobility of 400–600 cm^2/Vs.

At the time of writing, in spite of these solid-state laser alternatives, ELA continues to be the dominant crystallisation process for poly-Si TFTs.

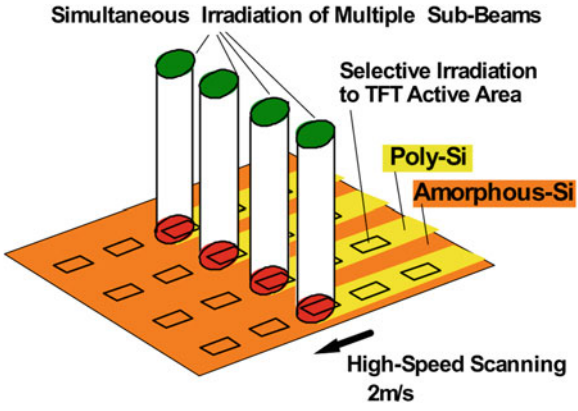

Fig. 7.48 Illustration of multiple sub-beam CW Nd:YVO_4 laser system for high throughput crystallisation. (Reprinted from [41] with permission of SID)

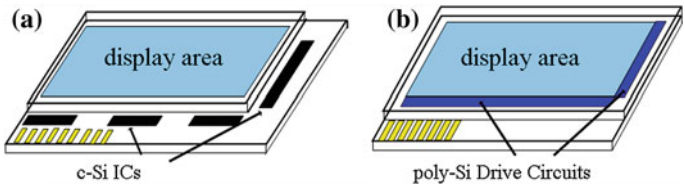

Fig. 7.49 Illustration of active matrix display cells showing drive circuits: **a** a-Si:H TFT display with externally mounted c-Si ICs, and **b** poly-Si TFT display with monolithically integrated poly-Si drive circuits

7.6 Poly-Si Applications

In order to deliver the appropriate signals to the pixels in an AMLCD (or AM-OLED display), using line-at-a-time addressing (see Chap. 4 for a detailed discussion of active matrix display operation) it is necessary to apply appropriate drive signals to the rows and columns of a display. For an a-Si:H display, where the switching speed of the a-Si:H TFTs is too slow to perform these functions, it is necessary to mount external silicon ICs around the edge of the display, as shown schematically in Fig. 7.49a. These circuits may be directly attached to the plate, or connected to the plate by flexible foils, upon which the ICs are mounted (as discussed in Sect. 4.5.4). The number of these ICs will be determined by the resolution of the display, i.e. the number of rows and columns to be addressed, and this will feed through into the cost of the display module in terms of the direct chip costs plus their mounting costs. The higher carrier mobility in poly-Si enables the direct fabrication of these addressing circuits on the active plate, as illustrated in Fig. 7.49b, and thereby reduce the module cost.

However, the cost saving due to the integration of the drive circuitry needs to be balanced against the increased cost of manufacturing the poly-Si active matrix plate. This is due to the greater number of masking and deposition stages (typically 9-mask stages, as shown in Sect. 7.4.2), as opposed to the 5-mask process for a-Si:H AMLCDs (see Sect. 5.3). In addition, there is the specific extra capital equipment needed to make poly-Si TFTs, principally the laser crystallisation and the ion doping systems (as discussed in Sect. 7.4.2), as well as extra aligners and deposition systems to give a balanced manufacturing process with the higher mask and deposition process count. Finally, there is a possible difference in yield in the more complex poly-Si process, where yield modelling is handled by assuming that the yield, Y, is given by a Poisson distribution of random defects, of density D, in a defect-sensitive area, A [106]:

$$Y = \exp -DA$$

and D is given by Nd, where d is the defect density per photolithographic step, and N is the number of steps. Hence, more mask stages can be expected to reduce process yield and add to unit costs.

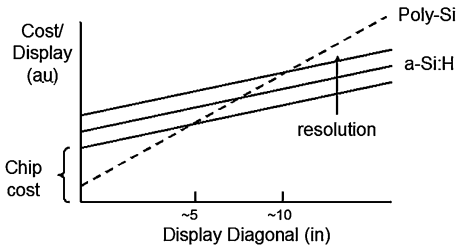

Fig. 7.50 Comparison of qualitative cost models, for a-Si:H displays with external drive circuits, and poly-Si displays with integrated drive circuits

Whilst detailed a detailed cost model, based on the evaluation of the above factors, is beyond the scope of this book, a qualitative model can give insight into the essential features of the price comparison, and this is shown in Fig. 7.50. In this figure, the cost of an individual display is plotted as function of the display diagonal, where it is assumed that there is a fixed cost for processing a glass plate of a given size, using either the poly-Si or the a-Si:H process. As shown, the smaller the display diagonal, the more displays there will be per glass plate, and, hence, the cost per display scales with its size. The slopes of the lines represent the different plate manufacturing costs for the low mask-count a-Si:H process and the higher mask-count poly-Si process. The intercept of these lines on the y-axis is determined by the number and cost of the externally added ICs, which is governed by the display resolution rather than by the display diagonal. Hence, these circuits represent a higher relative fixed cost as the display diagonal reduces, and these considerations demonstrate that poly-Si AMLCDs are most cost effective for small display diagonals. A cost cross-over point at 8-10 inch diagonals is shown as an approximate representation of the current situation, but this will vary with future IC costs and changes in the economics of plate manufacturing.

Thus, the major current application for poly-Si AMLCDs is in the high volume, ‘mobile’ display market (mobile/smart phones, digital camera view-finders, personal media players etc.), where circuit integration offers further advantages over and above the cost benefit. For instance, these portable displays need to be rugged, light-weight, and compact, and the poly-Si integrated circuits eliminate the risks of IC chip de-lamination due to mechanical shock. They also reduce the size of the glass module itself by reducing the space reserved for chip bonding. Finally, for higher resolution, small diagonal displays, the reduced pixel pitch can become a limiting factor for aligning and bonding the external ICs, but can be more easily met with the integrated drivers.

The poly-Si TFT CMOS circuits currently integrated into poly-Si displays include the row and column shift registers, level shifting circuits, 6-bit D/A converters for the column drivers, charge pumps and control logic [2, 11, 107, 108]. In contrast to these n- and p-channel CMOS circuits, which require the high mask count discussed above, it has been suggested that a lower level of circuit integration could be achieved at a lower processing cost, by using just p-channel TFTs [109]. This would reduce the mask count by three masks, by eliminating the separate masking stages for the n- and p-channel dopant locations, since the gate

electrode alone is sufficient to define the source and drain regions in single channel SA TFTs. In addition, the LDD mask can be removed as the superior drain bias stability of p-channel TFTs obviates the need for drain field relief. These process simplifications can lead to a more cost competitive technology compared with a-Si:H for large diagonal displays, albeit at the expense of reduced circuit performance. This is because single channel inverters conventionally have a greater power dissipation, smaller dynamic range and slower switching speed than CMOS inverters, but various single channel circuit alternatives have been proposed to reduce these performance limitations [110].

The other emerging application for poly-Si TFTs is in small/medium diagonal AMOLED displays, particularly for smart phones. At the moment, poly-Si is the preferred pixel transistor in these commercial displays, as it can provide the higher drive currents needed for OLEDs. Moreover, this application requires a high duty cycle on-current, and, under these conditions, poly-Si TFTs also have better bias stability than a-Si:H TFTs. However, amorphous oxide semiconductor, AOS, TFTs, using, for instance, a-indium-gallium-zinc-oxide, have also been identified as potential candidates for commercial AMOLED products [111], and a comparison of the stability of the major TFT technologies for this application is shown in Fig. 9.25 (in Sect. 9.4.3.3). For a fuller discussion of the background issues associated with AMOLED pixel design, see Sect. 4.6.2.2.

7.7 Summary

Poly-Si TFTs are now in mass production, particularly for small/medium diagonal, portable displays, containing integrated drive circuits. The circuit integration is facilitated by the high carrier mobility, and this has been achieved through a number of technology evolutions. The current, commercial fabrication process relies upon excimer laser crystallisation of a-Si:H pre-cursor layers, where the preferred excimer laser wavelength is 308 nm, which is obtained from a XeCl gas mixture. These are pulsed lasers, with a pulse duration of $\sim$30 ns, and the combination of UV wavelength and short pulse duration enables the a-Si film to be melted without undue heat transmission into the underlying glass substrate. The resulting grain structure displays a complex dependence upon the fractional melting of the film, where the optimum grain structure, and device performance, results from almost full melting of the a-Si films. Under these conditions, high quality $\sim$300 nm sized grains are formed, and the resulting electron field effect mobility lies between $\sim$100 cm^2/Vs and $\sim$250 cm^2/Vs, depending upon the number of laser shots in the process. The most uniform films, giving the highest performance devices, result from high shot number processing, but this gives the lowest throughput. Hence there is a trade-off between uniformity, performance and throughput, with typical manufacturing processes employing 20–30 shot processing.

In view of these well understood issues, alternative lasers and crystallisation procedures have been reported, including green solid-state lasers, as well as modified excimer laser technologies. These have all been able to produce larger grain material, with increased electron mobility values, which, in some cases, approach single crystal values. In addition to these laser-based techniques, there has also been interest in enhanced SPC procedures, using a metal catalyst to increase the speed of this inherently slow process. This is fundamentally a homogeneous large area process, which offers improved large area uniformity in contrast to the laser techniques. With a laser, the beam area itself is always far smaller than the substrate plate, and, therefore, beam uniformity, pulse-to-pulse energy fluctuations and pulse overlap effects all need to be carefully controlled to produce acceptable uniformity. The favoured metal for the enhanced SPC process is nickel, because it has a silicide phase, which is well lattice-matched to Si. This seeds the crystallisation of a-Si by a process variously referred to as silicide-mediated crystallisation (SMC) or metal-induced crystallisation (MIC). TFTs produced using this process have tended to have high off-state leakage currents, which have limited their practical application. However, it has been established that a subsequent excimer laser crystallisation stage can resolve that problem, and produce high performance TFTs. Nevertheless, in spite of these widely investigated alternatives, the current industrial production of poly-Si TFTs is still largely based upon excimer laser crystallisation.

The prevailing architecture of poly-Si TFTs is top-gated, and self-aligned (SA), with an SiO_2 gate dielectric, all of which are more similar to the semiconductor industry's silicon-on-insulator MOSFETs, rather than to the AMLCD industry's inverted staggered a-Si:H TFTs. In addition, this structure is implemented using ion doping for the source and drain dopants. However, the use of high-energy phosphorus ions, for the n-channel TFTs, is potentially damaging to the lattice within the doped regions. This damage needs to be carefully controlled to minimise device performance artefacts, namely increased leakage current and reduced on-state currents. For some purposes, particularly for basic materials investigation, a non-self-aligned structure (which is also top-gated and ion doped) offers a simpler process, and avoids the ion damage issues of the SA process. However, the SA process is necessary for short channel TFTs, and is the standard industry architecture. The other architectural feature specific to n-channel poly-Si TFTs is a lightly n^--doped region adjacent to the drain junction, which is needed to reduce the drain field, and, thereby, suppress drain-bias-stress induced hot carrier instabilities. It also diminishes other performance artefacts associated with a high field at the drain, in particular field enhanced leakage currents and poor current saturation of the output characteristics. These latter device performance issues are discussed in detail in Chap. 8.

Single channel TFTs of either architecture can be produced using a four-mask process. However, for a poly-Si AMLCD, with integrated complementary TFT drive circuits, a higher mask count than for a-Si:H AMLCDs is necessary, and a nine-mask process is illustrated. This higher mask count, and a more complex process, influences the commercial application of poly-Si TFTs, and a simple,

qualitative cost model illustrates why the current application is limited to small/medium diagonal displays.

In summary, poly-Si TFTs are now in mass-production, particularly for small/medium diagonal displays, where the integration of drive circuitry can give both cost and performance benefits. The circuit integration is facilitated by the high carrier mobility in poly-Si, and this can be achieved in both p- and n-channel TFTs, which enables complementary TFT circuit design. Within the small/medium display market, poly-Si accounts for $\sim$40 % of the AMLCD product revenues, and dominates the current smart phone AMOLED market.

References

1. Mitani M, Endo T, Taniguchi Y, Katou T, Shimoto S, Ohno T, Tsuboi S, Okada T, Azuma K, Kawachi G, Matsumura M (2008) Ultrahigh performance polycrystalline silicon thin-film transistors on excimer-laser-processed pseudo-single-crystal films. Jpn J Appl Phys 47(12):8707–8713
2. Nishibe T, Nakamura T (2004) Realization of new-concept Input Display by p-Si SOG technology. Proc AMLCD'04:85–88
3. Harada K, Kimura H, Miyatake M, Kataoka S, Tsunashima T, Motai T, Kawamura T (2009) A novel low-power-consumption all-digital system-on-glass display with serial interface. SID'09 Digest, pp 383–386
4. Q3'09 Quarterly small/medium shipment and forecast report. Displaysearch, Oct 2009
5. http://www.displaysearch.com/cps/rde/xchg/displaysearch/hs.xsl/120105_amoled_display_revenue_to_surge_in_2011_from_smart_phone_adoption.asp (Accessed Feb 2012)
6. Parrillo LC (1983) VLSI process integration. In: Sze SM (ed) VLSI technology. McGraw-Hill, New York
7. Lu NC-C, Lu C-Y (1984) I-V characteristics in polysilicon resistors at high electric field and the non-uniform conduction mechanism. Solid State Electron 27(8/9):797–805
8. Seto JYW (1975) The electrical properties of polycrystalline silicon films. J Appl Phys 46(12):5247–5254
9. Morozumi S, Oguchi K, Misawa T, Araki R, Ohshima H (1984) 4-25-in. and 1.51-in. B/W and Full-Color LC Video displays addressed by Poly-Si TFTs. SID'84 Digest, pp 316–319
10. Levinson J, Shepherd FR, Scanlon PJ, Westwood WD, Este G, Rider M (1982) Conductivity behaviour in polycrystalline semiconductor thin film transistors. J Appl Phys 53(2):1193–1202
11. Moon K-C, Kim C-H, Kim C-M, Park K-C, Joo S-Y, Kim I-G, Park T-H, Kang J-K, Chung E-J, Kim C-W (2004) 2-inch qVGA SOG-LCD employing TS-SLS. Proc AMLCD'04, pp 21–24
12. Brotherton SD, Ayres JR, Young ND (1991) Characterisation of low temperature poly-Si thin film transistors. Solid-State Electron 34(7):671–679
13. Mimura A, Konishi N, Ono K, Ohwada J-I, Hosokawa Y, Ono YA, Suzuki T, Miyata K, Kawakami H (1989) High performance low-temperature poly-Si n-channel TFTs for LCD. IEEE Trans ED-36(2):351–359
14. Hatalis MK, Greve DW (1988) Large grain polycrystalline silicon by low-temperature annealing of low pressure chemical vapour deposited amorphous silicon films. J Appl Phys 63(7):2260–2266

15. Brotherton SD, Young ND, Edwards MJ, Gill A, Trainor MJ, Ayres JR, Clarence IR, Bunn RM, Gowers JP (1994) Low temperature furnace processed poly-Si AMLCDs. Proc SID IDRC, pp 130–133, (Monterey, Ca, 1994)
16. Iverson RB, Reif R (1987) Recrystallisation of amorphised polycrystalline films on SiO2: temperature dependence of the crystallisation parameters. J Appl Phys 62(5):1675–1681
17. Brotherton SD (1995) Polycrystalline silicon thin film transistors. Semicond Sci Technol 10:721–738
18. Paetzl R, Brune J, Herbst L, Simon F, Turk BA (2009) Advanced laser crystallisation for active-matrix display manufacturing. Proceeding of 5th international TFT conference ITC'09, 10.2, France
19. Forouhi AR (1985) Optical functions of a-Si and a-Si:H. In: Properties of amorphous silicon (EMIS data reviews No. 1). IEE Inspec, London
20. Aspnes DE (1988) Optical functions of intrinsic Si. In: Properties of silicon (EMIS data reviews No. 4). IEE Inspec, London
21. Baeri P, Campisano SU (1982) Chapter 4. In: Poate JM, Mayer JW (eds) Laser annealing of semiconductors, Academic Press, New York
22. De Unamuno S, Fogarassy E (1989) A thermal description of the melting of c- and a-silicon under pulsed excimer lasers. Appl Surf Sci 36:1–11
23. Brotherton SD, McCulloch DJ, Clegg JB, Gowers JG (1993) Excimer-laser-annealed poly-Si thin film transistors. IEEE Trans ED-40(2):407–413
24. Fogarassy E, Prevot B, De Unamano S, Elliq M, Pattyn H, Mathe EL, Naudon A (1993) Pulsed laser crystallisation of hydrogen-free a-Si thin films for high-mobility poly-Si TFT fabrication. Appl Phys A56:365–373
25. Brotherton SD, McCulloch DJ, Gowers JP, Ayres JR, Trainor M (1997) Influence of melt depth in laser crystallised poly-Si thin film transistors. J Appl Phys 82(8):4086–4094
26. Leonard JP, Bessette MA, Gupta VV, Im JS (1997) The effect of film thickness and pulse duration variation in excimer laser crystallisation of thin Si films. Mat Res Symp Soc 452:947–952
27. Im JS, Kim HJ, Thompson MO (1993) Phase transformation mechanisms in excimer laser crystallisation of amorphous silicon films. Appl Phys Lett 63(14):1969–1971
28. Im JS, Kim HJ (1994) On the super lateral growth phenomenon observed in excimer laser-induced crystallisation of thin Si films. Appl Phys Lett 64(17):2303–2305
29. Im JS, Crowder MA, Sposili RS, Leonard JP, Kim HJ, Yoon JH, Gupta VV, Jin Song H, Cho HS (1998) Controlled super-lateral growth of Si films for microstructural manipulation and optimisation. Phys Stat Sol (a) 166(2):603–617
30. Kim HJ, Im JS (1994) Multiple pulse irradiations in excimer laser-induced crystallisation of amorphous Si films. Mat Res Soc Symp Proc 321:665–670
31. Brotherton SD, McCulloch DJ, Gowers JP, French ID, Gale I (2000) Issues in laser crystallisation of poly-Si. Proc IDMC'2000, Seoul, pp 65–69
32. Herbst L, Simon F, Rebhan U, Osmanov R, Fechner B (2004) New technology for creation of LTPS with excimer laser annealing. Proc Asia Display/IMID'04, Korea, pp 319–321
33. Brotherton SD, McCulloch DJ, Gowers JP (2004) Influence of excimer laser beam shape on poly-Si crystallisation. Jpn J Appl Phys 43(8):5114–5121
34. Brotherton SD, McCulloch DJ, Gowers JP, Ayres JR, Fisher CA, Rohlfing FW (2000) Excimer laser crystallisation of poly-Si TFTs for AMLCDs. Mat Res Soc Symp Proc 621:Q7.1.1–Q7.1.12
35. Tamagawa K, Ikeda H, Oonishi T, Yamamoto Y, Kikuchi M, Morimura T, Hashimoto M, Asari S (2006) Green laser annealing system for manufacturing LTPS TFTs. Ulvac Tech J 64E:32–36
36. Zan HW, Huang CY, Saito K, Tamagawa K, Chen J, Wu TJ (2006) Crystallization mechanism of Poly-Si thin film using high-power Nd:YAG Laser with Gaussian Beam profile. Mater Res Soc Symp Proc 910:A14–03

37. Morikawa K, Okamoto T, Kojima T, Yura S, Nishimae J, Sato Y, Tanaka M, Inoue M (2004) Comparison of Poly-Si TFT characteristics crystallized by a YAG2ω laser and an excimer laser. SID 04 Digest, pp 1088–1091
38. Helen Y, Gautier G, Mohammed-Brahim T, Bonnaud O, Andra G, Bergmann J, Falk F (2001) High field effect mobility polysilicon thin film transistors involving frequency doubled cw-Nd:YAG-laser crystallisation. Proc AMLCD-01, pp 187–188
39. Hara A, Takei M, Takeuchi F, Suga K, Yoshino K, Chida M, Kakehi T, Ebiko Y, Sano Y, Sasaki N (2004) High performance low temperature polycrystalline silicon thin film transistors on non-alkaline glass produced using diode pumped solid state continuous wave laser lateral crystallization. Jpn J Appl Phys 43(4A):1269–1276
40. Hara A, Takeuchi F, Takei M, Suga K, Yoshino K, Chida M, Sano Y, Sasaki N (2002) High-performance polycrystalline silicon thin film transistors on non-alkali glass produced using continuous wave laser lateral crystallization. Jpn J Appl Phys 41(3B):L311–L313
41. Sasaki N, Hara A, Takeuchi F, Mishima Y, Kakehi T, Yoshino K, Takei M (2002) High throughput CW-laser lateral crystallization for low-temperature poly-Si TFTs and fabrication of 16 bit SRAMs and 270 MHz shift registers. SID 02 Digest, pp 154–157
42. Hara A, Takeuchi F, Takei M, Yoshino K, Suga K, Sasaki N (2001) Ultra-high performance poly-Si TFTs on a glass by a stable scanning CW laser lateral crystallization. Proc AMLCD'01, pp 227–230
43. Jang J (2004) Poly-Si TFTs by non-laser crystallization methods. In: Kuo Y (ed) Thin film transistors, materials and processes: polycrystalline silicon thin film transistors, vol 2. Kluwer Academic publishers, Dordrecht
44. Hayzelden C, Batstone JL (1993) Silicide formation and silicide-mediated crystallization of nickel-implanted amorphous silicon thin films. J Appl Phys 73(12):8279–8289
45. Yoon SY, Kim KH, Kim CO, Oh JY, Jang J (1997) Low temperature metal induced crystallization of amorphous silicon using a Ni solution. J Appl Phys 82(11):5865–5867
46. Van der Zaag PJ, Verheijen m A, Yoon SY, Young ND (2002) Explanation for the leakage current in polycrystalline-silicon thin-film transistors made by Ni-silicide mediated crystallization. Appl Phys Lett 81(18):3404–3406
47. Meng Z, Zhao S, Wu C, Zhang B, Wong M, Kwok H–S (2006) Polycrystalline silicon films and thin-film transistors using solution-based metal-induced crystallization. IEEE J Disp Technol 2(3):265–273
48. Lee J-S, Kim M-S, Kim D, Kim Y-M, Moon J, Joo S-K (2009) Fabrication and characterization of low temperature polycrystalline silicon thin film transistors by ink-jet printed nickel-mediated lateral crystallization. Appl Phys Lett 94(12):122105-1–122105-3
49. Lee S-W, Joo S-K (1996) Low temperature poly-Si thin- film transistor fabrication by metal-induced lateral crystallization. IEEE Electron Dev Lett 17(4):160–162
50. Wong M, Jin Z, Bhat GA, Wong PC, Kwok HS (2000) Characterization of the MIC/MILC interface and its effects on the performance of MILC thin-film transistors. IEEE Trans Electron Dev 47(5):1061–1067
51. Meng Z, Wang M, Wong M (2000) High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for System-on-Panel applications. IEEE Trans Electron Dev 47(2):404–409
52. Murley D, Young N, Trainor M, McCulloch D (2001) An investigation of laser annealed and metal-induced crystallized polycrystalline silicon thin-film transistors. IEEE Trans Electron Dev 48(6):1145–1151
53. Yoon SY, Young N, van der Zaag PJ, McCulloch D (2003) High-performance poly-Si TFTs made by Ni-mediated crystallization through low-shot laser annealing. IEEE Electron Dev Lett 24(1):22–24
54. Sakamoto H, Makita N, Hijikigawa M, Osame M, Tanada Y, Yamazaki S (2000) 2.6 inch HDTV panel using CG Silicon. SID 00 Digest, pp 1190–1193
55. Mizuki T, Matsuda JS, Nakamura Y, Takagi J, Yoshida T (2004) Large domains of continuous grain silicon on glass substrate for high-performance TFTs. IEEE Trans Electron Dev 51(2):204–211

56. Batey J, Tierney E (1986) Low-temperature deposition of high-quality silicon dioxide by plasma-enhanced chemical vapor deposition. J Appl Phys 60(9):3136–3145
57. Hirashita N, Tokitoh S, Uchida H (1993) Thermal desorption and infrared studies of plasma-enhanced chemical vapor deposited SiO films with tetraethylorthosilicate. Jpn J Appl Phys 32(4):1787–1793
58. Young ND, Gill A (1992) Water-related instability in TFTs formed using deposited gate oxides. Semicond Sci Technol 7:1103–1108
59. Asari S, Kurata T, Kikuchi T, Hashimoto M, Saito K (2002) Evaluation of gate insulation film for large-scale substrate in low temperature poly-Si TFTs. Proc IDMC'02
60. Young ND, Harkin G, Bunn RM, McCulloch DJ, French ID (1996) The fabrication and characterisation of EEPROM arrays on glass using a low-temperature poly-Si TFT process. IEEE Trans ED-43(11):1930–1936
61. Young ND, McCulloch DJ, Bunn RM, French ID, Gale IG (1998) Low temperature poly-Si on glass and polymer substrates. Proc Asia Display'98, pp 83–93
62. Okumura F, Yuda K (1998) High-quality low-temperature gate oxide for poly-Si TFTs. Electrochem Soc Proc 98–22:133–142
63. Higashi S, Abe D, Hiroshima Y, Miyashita K, Kawamura T, Inoue S, Shimoda T (2002) High-quality SiO_2/Si interface formation and its application to fabrication of low-temperature-processed polycrystalline Si thin-film transistor. Jpn J Appl Phys 41(6a):3646–3650
64. Maiolo L, Pecora A, Fortunato G, Young ND (2006) Low-temperature electron cyclotron resonance plasma-enhanced chemical-vapor deposition silicon dioxide as gate insulator for polycrystalline silicon thin-film transistors. J Vac Sci Technol A 24(2):280–285
65. Young ND Private communication, unpublished results
66. Lee J-H, Shin M-Y, Moon KC, Han M-K (2004) Reliable poly-Si TFT employing XeCl excimer laser irradiation on gate oxide. Phys Scr T114:199–201
67. Miyashita M, Sugawara Y, Uraoka Y, Yano H, Hatayama T, Fuyuki T, Sameshima T (2005) Improvement of reliability in low-temperature Poly-Si thin film transistors by water vapor annealing. Proc AM-LCD'05, pp 277–280
68. Wilk GD, Wallace RM, Anthony JM (2001) High-k gate dielectrics: current status and materials properties considerations. J Appl Phys 89(10):5243–5275
69. O'Sullivan MP, Young ND, French ID, Wilks RW (2003) Low threshold voltage poly-Si TFTs formed using silicon dioxide/silicon nitride dual layer dielectric. Proc IDW'03, pp 443–445
70. O'Sullivan MP, Young ND, Glass C, Wilks RW (2003) Low threshold voltage poly-Si TFTs formed using Ta_2O_5 gate dielectric. Proc IDW'03, pp 335–338
71. Ryssel H, Ruge I (1986) *Ion implantation*, chapters 2 and 9. Wiley, New York
72. Brotherton SD, Ayres JR, Fisher CA, Glaister C, Gowers JP, McCulloch DJ, Trainor MJ (1998) The technology and application of laser crystallised poly-Si TFTs. In: Kuo Y (ed) Thin film transistor technologies IV, proceedings, vol 98–22. Electrochemical Society, New Jersey, pp 25–42
73. Yoneda K (1997) State-of-the-art low temperature processed poly-Si TFT technology. Proc SID-IDRC'97, pp M40–M47
74. Peng D-Z, Chang T-C, Zan H-W, Huang T-Y, Chang C-Y, Liu P-T (2002) Reliability of laser-activated low-temperature polycrystalline silicon thin-film transistors. Appl Phys Lett 80(25):4780–4782
75. Park K-C, Nam W-J, Kang S-H, Han M-K (2004) Incomplete laser annealing of ion doping damage at source/drain junctions of poly-Si thin-film transistors. Electrochem Solid-State Lett 7(6):G116–G118
76. Brotherton SD, Lee S-G, Glasse C, Ayres JR, Glaister C (2002) Short channel poly-Si TFTs. Proc IDW'02, pp 283–286
77. Valletta A, Mariucci L, Fortunato G, Brotherton SD (2003) Surface scattering effects in polycrystalline silicon thin film transistors. Appl Phys Lett 82(18):3119–3121

78. Nam W-J, Park K-C, Jung S-H, Park S-J, Han M-K (2003) Observation and annealing of incomplete recrystallized junction defects due to the excimer laser beam diffraction at the gate edge in poly-Si TFT. Mat Res Soc Symp Proc 762:A17.8
79. Ayres JR, Brotherton SD, McCulloch DJ, Trainor M (1998) Analysis of drain field and hot carrier stability of poly-Si TFTs. Jpn J Appl Phys 37(4a):1801–1808
80. Young ND, Gill A, Edwards MJ (1992) Hot carrier degradation in low temperature processed polycrystalline silicon thin film transistors. Semicond Sci Technol 7(9):1183–1188
81. Young ND (1996) The formation and annealing of hot-carrier-induced degradation in poly-Si TFTs, MOSFETs, and SOI devices, and similarities to state-creation in a-Si:H. IEEE Trans ED-43(3):450–456
82. Rohlfing FW, Ayres JR, Brotherton SD, Fisher CA, McCulloch DJ (2000) Fabrication and characterisation of poly-Si TFTs with self-aligned lightly-doped drain. Proc 20th SID-IDRC, pp 119–122
83. Yoshinouchi A, Morita T, Itoh M, Yoneda H, Yamane Y, Yamamoto Y, Tsucimoto S, Funada F, Awane K (1996) Process technologies for monolithic low-temperature poly-Si TFT-LCDs. Proc SID EuroDisplay'96, pp 29–32
84. Glasse C, Brotherton SD, French ID, Green PW, Rowe C (2003) Short channel TFTs made with sidewall spacer technology. Proc AMLCD'03, pp 317–320
85. Gosain DP, Westwater J, Usui S (1995) High performance bottom gate TFTs by excimer laser crystallisation and post hydrogenation. J Appl Phys 34(1):937–941
86. Tsai C-C, Chen H-H, Chen B-T, Cheng H-C (2007) High-performance self-aligned bottom-gate low-temperature poly-silicon thin-film transistors with excimer laser crystallization. IEEE Electron Device Lett 28(7):599–602
87. Mariucci L, Fortunato G, Bonfiglietti A, Cuscuná M, Pecora A, Valletta A (2004) Polysilicon TFT structures for kink-effect suppression. IEEE Trans ED-51(7):1135–1142
88. Mei P, Boyce JB, Hack M, Lujan RA, Johnson RI, Anderson GB, Fork DK, Ready SE (1994) Laser dehydrogenation/crystallization of plasma-enhanced chemical vapor deposited amorphous silicon for hybrid thin film transistors. Appl Phys Lett 64(9):1132–1134
89. Brotherton SD, McCulloch DJ, Edwards MJ (1994) Beam shape effects with excimer laser crystallisation of PECVD and LPCVD a-Si. Solid State Phenom 37–38:299–304
90. Kikuchi M (2006) Plasma CVD system for manufacturing LTPS TFTs. Ulvac Tech J 64E:30–31
91. Suzuki T (2006) Flat panel displays for ubiquitous product applications and related impurity doping technologies. J Appl Phys 99:111101-1–111101-15
92. Sposili RS, Im JS (1996) Sequential lateral solidification of thin silicon films on SiO_2. Appl Phys Lett 69(19):2864–2866
93. Voutsas AT (2003) Assessment of the performance of laser-based lateral-crystallisation technology via analysis and modelling of polysilicon thin film transistor technology. IEEE Trans Ed-50(6):1494–1500
94. Park J-Y, Park H-H, Lee K-Y, Chung H-K (2004) Design of sequential lateral solidification crystallisation method for low temperature poly-Si thin film transistors. Jpn J Appl Phys 43(4a):1280–1286
95. Oh C-H, Matsumura M (1998) Preparation of location-controlled crystal-silicon islands by means of excimer-laser annealing. Proc AMLCD'98, pp 13–16
96. Endo T, Taniguchi Y, Katou T, Shimoto S, Ohno T, Azuma K, Matsumura M (2008) Pseudo-single-nucleus lateral crystallization of Si thin films. Jap J Appl Phys 47(3):1862–1866
97. Taniguchi Y, Katou T, Hiramatsu M, Matsumura M (2008) New phase modulators for next-generation low-temperature crystallization method of Si films. Jap J Appl Phys 45(10A):7753–7760
98. Van der Wilt PC, van Dijk BD, Bertens GJ, Ishihara R, Beenakker CIM (2001) Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films. Appl Phys Lett 79(12):1819–1821

99. Rana V, Ishihara R, Hiroshima Y, Abe D, Inoue S, Shimoda T, Metselaar W, Beenakker K (2005) Dependence of single-crystalline Si TFT characteristics on the channel position inside a location-controlled grain. IEEE Trans ED-52(12):2622–2628
100. Turk BA, Simon F, Pätzel R (2007) 2D-projection-based method for forming uniform and high-quality poly-Si films via sequential lateral solidification. Proc 3rd international TFT conference, ITC'07, Rome, pp 78–81
101. Crowder MA, Limanov AB Im JS (2000) Sub-grain boundary spacing in directionally crystallized Si films obtained via sequential lateral solidification. Proc Mat Res Soc Symp 621E:Q9.6.1–Q9.6
102. Chung UJ, Limanov AB, van der Wilt, PC, Chitu AM, Im JS (2006) Microstructural analysis of directionally solidified materials obtained via line-scan SLS of Si films. Proc IMID/IDMC'06, pp 1744–1749
103. Brotherton SD, Crowder MA, Limanov AB, Turk B, Im JS (2001) Characterisation of poly-Si TFTs in directionally crystallized SLS Si. Proc Asia Display/IDW'01, pp 387–390
104. Crowder MA, Voutsas AT, Droes SR, Moriguchi M, Mitani Y (2004) Sequential lateral solidification processing for polycrystalline Si TFTs. IEEE Trans ED-51(4):560–568
105. Shirai K, de Dieu Mugiraneza J, Suzuki T, Okada T, Noguchi T, Matsushima H, Hashimoto T, Ogino Y, Sahota E (2011) Crystallization behavior of sputtered amorphous silicon films by blue-multi-laser-diode annealing. Jpn J Appl Phys 50:021402
106. Young BE, Young R (1998) Cost and yield model comparison for a-Si and poly-Si displays. SID'98 Digest, pp 1193–1196
107. Ayres JR, Edwards MJ, Young ND, Pook R, Pearson AD, Henzen AV (2002) A highly integrated AMLCD with low voltage operation. Proc 2nd international display manufacturing conference. IDMC 2002:19–22
108. Hashimoto K, Yamashita K, Matsuki F, Watsuda H, Ayres JR, Edwards MJ (2005) A high resolution LTPS AMLCD with integrated DACs. Proc IDW'05, pp 1031–1032
109. Ha Y-M (2000) P-type technology for large size low temperature poly-Si TFT-LCDs. SID symposium digest of technical papers 31(1):1116–1119
110. Hong S, Kim J, Choi B-D (2009) A high-speed and low-power inverter circuit using p-channel metal oxide semiconductor low-temperature polycrystalline silicon thin film transistors. Jpn J Appl Phys 48(3):03B010_1–03B010_5
111. http://www.displaysearch.com/cps/rde/xchg/displaysearch/hs.xsl/120106_oled_display_technology_moving_to_compete_in_the_tv_market.asp (Accessed Jan 2012)