

Chapter 2

Semiconductor Device Physics for TFTs

Abstract Two device physics topics are discussed in this chapter, namely, surface band bending and surface charges in the metal–insulator–semiconductor, MIS, structure, and electron-hole pair recombination/generation processes. The treatment of the MIS structure covers the relationship between the voltage on the metal gate, the induced surface charge in the semiconductor and the resulting surface potential. This is treated analytically, using single crystal equations, and the relationships are fundamental to the understanding of IGFET operation. Equally, the concepts are widely employed in analysing TFT behaviour. The electron-hole pair generation process underlies the leakage current behaviour of many semiconductor devices, and can be applied to the analysis of TFT off-state behaviour. The recombination process determines steady state carrier concentrations under injection conditions, such as optical illumination. Finally, there is a brief discussion of carrier flow in semiconductor devices, including the equations used in numerical simulation packages.

2.1 Introduction

In this chapter, device physics topics are introduced, which are relevant to TFTs, and for following the discussion in later chapters. The emphasis is on background understanding of basic device physics principles, and an analytical approach is followed, using single crystal semiconductor equations. These concepts and equations are modified in later chapters for the more complex situation of the non-single crystal TFT materials.

The first topic presented deals with semiconductor surface physics, focussing on band bending and surface charge in the metal–insulator–semiconductor, MIS, system. This underlies the relationship between the voltage on the metal gate and the induced charge in the semiconductor surface, and introduces the concepts of the flat band voltage and the threshold voltage for surface inversion. The most widely studied semiconductor/insulator interface is the c-Si/SiO₂ interface, and the numerical examples given are based upon this system, although the equations

themselves are quite general. In [Chap. 6](#), these surface space charge equations are re-formulated to include the U-shaped density of states functions found in a-Si:H and other TFT materials, and the influence of these extra states is compared to the simpler situation discussed in this chapter.

The second topic is electron-hole pair generation and recombination. These are basic processes underlying both leakage current effects, and steady state carrier densities in devices under injection conditions, such as optical illumination. Finally, there is a brief discussion of carrier flow and the coupled field/space charge equations, which need to be solved in order to calculate the current–voltage characteristics of a device.

Much current research into device behaviour makes use of commercial device simulators to solve these latter equations. These simulation packages give a deeper insight into device behaviour by relating its current–voltage characteristics to internal field and carrier distributions. However, in published work, the fundamental equations are rarely listed. In the final [Sect. 2.4](#), of this chapter, those equations are presented, and they are built up from the material in the preceding sections of the chapter (but, the numerical techniques used for the solution of the equations go beyond the scope of this book).

As is apparent, the range of device physics topics covered here is limited, and, for a broader coverage of this field, there are many excellent books available, such as Sze and Ng [[1](#)]. Examples of device simulation packages can be found in Refs. [[2](#), [3](#)], as well as a discussion of the numerical solution techniques in [[2](#)].

Some of the key simplified equations, from [Sects. 2.2](#) and [2.3](#), are listed in the Appendix. These are useful for cross-reference purposes in later chapters, and also for direct, analytical calculations.

2.2 Semiconductor Surface Physics

2.2.1 Ideal MIS Capacitor and Surface Band Bending

Figure [2.1a](#) shows the band diagram of an ideal MIS capacitor, on a p-type substrate, in which the Fermi levels in the metal and in the semiconductor perfectly align, such that there is no induced band bending within the structure (In [Sect. 2.2.3](#), a more realistic situation will be discussed, in which there are work function differences between the metal and the semiconductor, and the semiconductor interface contains interface trapping states). In the treatment below, the following conventions will be used: the Fermi potential, V_F , will be measured from the bulk intrinsic level, E_i , and will be taken as positive beneath E_i and negative above it. Similarly, the band bending, V_s , will be measured from the bulk intrinsic level, and the polarity convention will be the same as used for V_F .

When a positive charge, Q_G , is placed on the metal gate, it will induce an equal and opposite negative charge in the semiconductor, Q_s , and this negative charge

will consist of an increase in the electron density and a decrease in the free hole density, thereby, leaving behind immobile, ionised acceptor centres, N_a . In order to accommodate these changes in free carrier density, the bands within the semiconductor will have to bend downwards near its surface, as shown in Fig. 2.1b. It will also be seen that the positive charge on the gate results from a positive bias being applied to the gate relative to the semiconductor. Following the convention discussed above, the Fermi level in the metal is moved downwards in response to the positive gate bias, V_G , and the semiconductor surface potential is $+V_s$. The situation shown in this diagram is for a small positive potential on the gate, such that the surface electron density, n_s , is small compared with N_a , and the surface is said to be *depleted* (of free holes). For a larger positive gate bias, the situation shown in Fig. 2.1c occurs. In this case, there is a corresponding increase in band bending, V_s , and the free electron concentration at the surface is larger than N_a : the surface is now said to be *inverted*. Between these two situations, when the band bending, $V_s = V_F$, the surface will be intrinsic, and $n_s = p_s = n_i$. Further positive

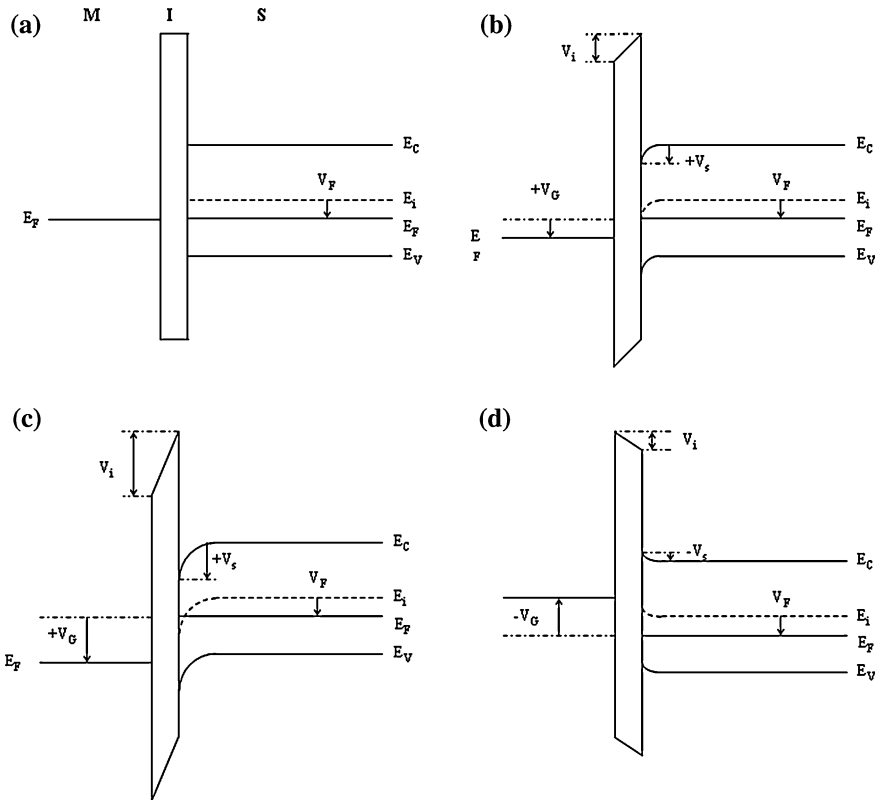


Fig. 2.1 Ideal metal–insulator–semiconductor, MIS, band diagrams, showing different surface charge conditions for a p-type substrate: **a** flat bands, **b** hole depletion, **c** electron inversion, and **d** hole accumulation

band bending beyond this point will lead to $n_s > p_s$. Finally, as shown in Fig. 2.1d, with a negative bias applied to the gate, there is an increase in positive charge induced in the semiconductor, due to an increase in the free hole density. This is associated with the bands bending upwards by an amount $-V_s$. In this case, the surface is said to be *accumulated*. With an n-type substrate, the opposite situation occurs, in that a negative gate bias will cause the surface to be depleted/inverted rather than accumulated, and a positive bias will cause surface accumulation.

To establish the relationship between V_s , and Q_s and V_G , it is necessary to solve Poisson's equation, where:

$$\frac{d^2V}{dx^2} = -\frac{q\rho(x)}{\epsilon_0\epsilon_s} \quad (2.1)$$

ϵ_0 is the permittivity of free space, ϵ_s is the dielectric constant of the semiconductor, and the space charge density, $\rho(x)$ is:

$$\rho(x) = p(x) - n(x) - N_a \quad (2.2)$$

The free carrier densities are defined by the intrinsic carrier concentration, n_i , and the separation of the Fermi level from the intrinsic level, i.e.:

$$p(x) = n_i \exp\frac{q(V_F - V)}{kT} \quad (2.3)$$

$$n(x) = n_i \exp\frac{-q(V_F - V)}{kT}$$

$$p(x) - n(x) = 2n_i shq(V_F - V)/kT \quad (2.4)$$

Where T is the temperature, and k is Boltzmann's constant. At the surface, $V = V_s$, and in the bulk, where $V = 0$:

$$p_0 = n_i \exp\frac{qV_F}{kT} \quad \text{and} \quad n_0 = n_i \exp\frac{-qV_F}{kT}$$

From charge neutrality,¹

$$p_0 - n_0 = N_a = 2n_i shqV_F/kT \quad (2.5)$$

$$\frac{d^2V}{dx^2} = -\frac{2n_i q}{\epsilon_0\epsilon_s} \left[sh\frac{q(V_F - V)}{kT} - sh\frac{qV_F}{kT} \right] \quad (2.6)$$

Using $\frac{d^2V}{dx^2} = \frac{1}{2} \frac{d}{dV} \left(\frac{dV}{dx} \right)^2$, and integrating Eq. 2.6 from the bulk ($V = 0$, and $dV/dx = 0$) to the surface ($V = V_s$, and $dV/dx = -F_s$):

¹ $V_F = (kT/q)\ln(N_a/n_i)$.

Table 2.1 Polarity relationship between band bending, surface field and space charge in an MIS structure

V_s	F_s	Q_s	Free carrier conditions
+ve	+ve	-ve	Reduction of holes and/or increase of electrons
-ve	-ve	+ve	Reduction of electrons and/or increase of holes

$$\left(\frac{dV}{dx}\right)_{V=V_s}^2 \equiv F_s^2 = \frac{4n_i q}{\epsilon_0 \epsilon_s} \left[\frac{kT}{q} ch \frac{q(V_F - V_s)}{kT} - \frac{kT}{q} ch \frac{qV_F}{kT} + V_s sh \frac{qV_F}{kT} \right] \quad (2.7)$$

From Gauss' Law, the surface field, F_s , is related to the total areal charge, Q_s , contained within the surface by:

$$Q_s = -\epsilon_0 \epsilon_s F_s \quad (2.8)$$

Hence, the relationship between Q_s and V_s is given by:

$$Q_s = \pm \sqrt{4n_i q \epsilon_0 \epsilon_s} G(V_s, V_F) \quad (2.9)$$

where $G(V_s, V_F)$ is given by:

$$G(V_s, V_F) = \mp \sqrt{\left[\frac{kT}{q} ch \frac{q(V_F - V_s)}{kT} - \frac{kT}{q} ch \frac{qV_F}{kT} + V_s sh \frac{qV_F}{kT} \right]} \quad (2.10)$$

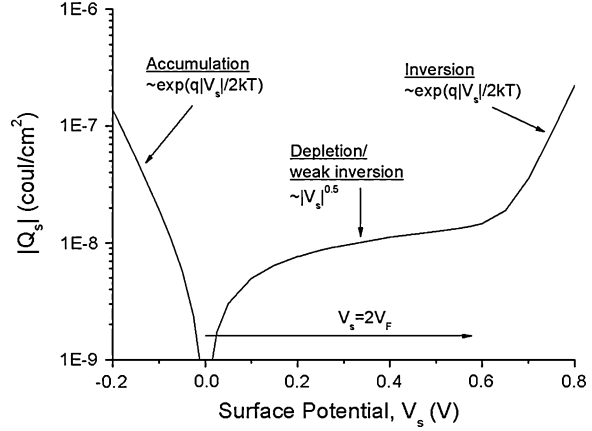
Given the positive and negative values of Q_s in Eq. 2.9, the appropriate signs of V_s , F_s and Q_s are given in Table 2.1, and the correct value of Q_s is given by:

$$Q_s = -\frac{V_s}{|V_s|} |Q_s| \quad (2.11)$$

Equation 2.9 has been evaluated for a crystalline Si substrate doped with 10^{15} acceptors/cm³, and the key features in the relationship between Q_s and V_s are shown in Fig. 2.2.² The three previously discussed regimes of accumulation, depletion and inversion are indicated, and, for accumulation and inversion, Q_s increases exponentially with V_s . In these two regimes, the main contributors to Q_s are the free carriers, so that the hole and electron densities increase exponentially with V_s in accumulation and inversion, respectively. In the third regime of majority carrier depletion, Q_s increases with $\sqrt{V_s}$, and extrapolating the inversion arm of the curve back into this regime shows that the ionised acceptor charge dominates Q_s . Hence, in the three regimes, either free carriers or fixed space charge constitutes the major part of Q_s . As will be seen in Chap. 6, this is not necessarily the case with TFT materials, in which trapping states in the forbidden

² Note that in evaluating Eq. 2.10, if the units of Boltzmann's constant, k , are in eV/K, then q has the value of unity. If SI units are used, then q has its usual value of 1.602×10^{-19} C.

Fig. 2.2 Calculated variation of surface charge density with surface potential (substrate doping density is 1×10^{15} acceptors/cm³)



band gap can continue to make a major contribution to Q_s even when the surface has enough free carriers to support substantial conduction.

For the calculation in Fig. 2.2, the value of qV_F was 0.288 eV below E_i , and the electron concentration in inversion starts to dominate Q_s at $V_s > \sim 2V_F$. In fact, the conventional definition of the threshold for *strong surface inversion* is at $V_s = 2V_F$, where the volume concentration of free electrons at the surface, n_s , is equal to the volume concentration of acceptors, N_a . When $V_s = V_F$, the surface is intrinsic ($n_s = p_s = n_i$), and the band bending regime beyond this, and up to strong inversion, is referred to as *weak inversion* ($p_s < n_s < N_a$).

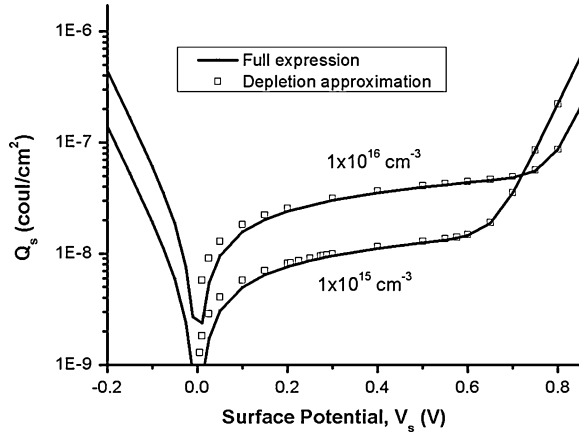
In the depletion/inversion regime, the band bending, V_s , is positive, and for V_s , and $V_F > kT/q$, i.e., more than kT from the flat band position, Eq. 2.9 can be simplified to:

$$Q_s \cong -\sqrt{2q\epsilon_0\epsilon_s} \left[n_i \frac{kT}{q} \exp \frac{q(V_s - V_F)}{kT} + N_a V_s \right]^{0.5} \quad (2.12)$$

The first term in the brackets relates to the free electron concentration, and the second term to the ionised acceptor space charge density, and the dependence of those terms on V_s shows the exponential and quadratic forms, respectively, discussed above. This simplified expression, with the physically obvious terms, provides a good approximation to the full Eq. 2.9, as seen by the calculations in Fig. 2.3. The calculations used two different substrate doping levels, and, for the more heavily doped substrate, with 10^{16} acceptors/cm³, the value of qV_F is 0.348 eV below E_i , and this correspondingly increases the value of V_s at which strong inversion occurs. Also, the increase in Q_s , for the more heavily doped substrate, at a given value of V_s in depletion, is ~ 3 times more than for the less heavily doped substrate, as expected from the $\sqrt{N_a}$ dependence in Eq. 2.12.

Between flat bands and inversion, when the ionised acceptor space charge dominates, Eq. 2.12 can be further reduced to:

Fig. 2.3 Comparison of surface charge density calculations using the full (solid line) and approximate (symbols) expressions from Eqs. 2.9 and 2.12, respectively. (Substrate doping densities of 1×10^{15} acceptors/cm³, and 1×10^{16} acceptors/cm³)



$$Q_s \cong -\sqrt{2q\epsilon_0\epsilon_s N_a V_s} \equiv Q_b \quad (2.13)$$

Where Q_b is the areal acceptor space charge density. Equation 2.13 is the same as directly calculated from Poisson's equation using the depletion approximation, i.e. from:

$$\frac{d^2V}{dx^2} = \frac{qN_a}{\epsilon_0\epsilon_s} \quad (2.14)$$

and integrating this with respect to V . Alternatively, if Eq. 2.14 is integrated with respect to x , then:

$$Q_s = -qN_a x_d \quad (2.15)$$

where x_d is the width of the space charge depletion region at V_s . At inversion, when $V_s = 2V_F$, further increases in band bending cause such large increases in Q_s , due to the exponentially increasing free electron density, that, to a first approximation, the fixed space charge can be regarded as having reached a limiting maximum value, $Q_{b\max}$. This can be obtained by substituting $V_s = 2V_F$ into Eq. 2.13:

$$Q_{b\max} = -\sqrt{2q\epsilon_0\epsilon_s N_a 2V_F} \quad (2.16)$$

and from Eq. 2.15,

$$Q_{b\max} = -qN_a x_{d\max} \quad (2.17)$$

where $x_{d\max}$ is the maximum width of the depletion region, and, from Eqs. 2.16 and 2.17, $x_{d\max}$ is given by:

$$x_{d\max} = \sqrt{\frac{2\epsilon_0\epsilon_s 2V_F}{qN_a}} \quad (2.18)$$

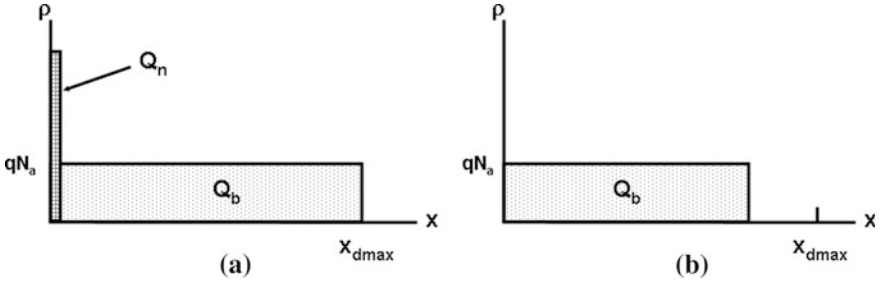


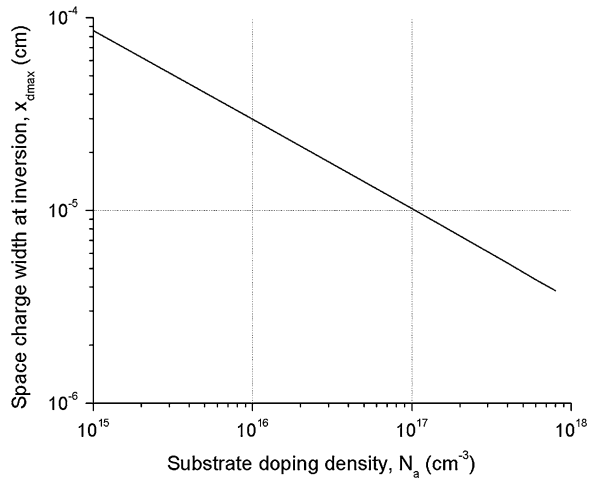
Fig. 2.4 Illustration of bulk depletion layer, Q_b , and inversion layer, Q_n , charge densities in: **a** inversion, and **b** depletion

Q_s in Eq. 2.12 can be represented by the sum:

$$Q_s = Q_n + Q_b \quad (2.19)$$

Where Q_b is the extended depletion layer charge, and Q_n is the areal density of inversion layer electrons. These will be confined close to the semiconductor surface, by virtue of the electrons being in a parabolic potential well of depth V_s . The terms in Eq. 2.19 are pictorially represented in Fig. 2.4a for inversion ($V_s > 2V_F$), and by Fig. 2.4b for depletion ($V_s < 2V_F$). The variation of x_{dmax} with N_a can be calculated from Eq. 2.18, and is shown in Fig. 2.5. From a TFT point of view, assuming a certain equivalence between N_a and the TFT trap state density, a curve of this type can be used to determine whether a thin film is fully depleted or not at inversion. For instance, the maximum equilibrium space charge width, at inversion, for a substrate doped with 10^{17} acceptors/cm³ is 100 nm; therefore, a thin film of 100 nm, with an equivalent volume trapped charge density of $<10^{17}$ cm⁻³, will be fully depleted before $V_s = 2V_F$. As a result of this, the threshold of inversion will occur at a lower value of band bending than for a thicker film having the same trap state density. This is discussed further in Chap. 3

Fig. 2.5 Variation of maximum depletion layer width at inversion, x_{dmax} , with substrate doping level



2.2.2 Gate Bias and Threshold Voltage

Referring to Fig. 2.1, the voltage on the gate, V_G , is dropped partially across the dielectric, V_i , and partially across the semiconductor, V_s , so that:

$$V_G = V_i + V_s \quad (2.20)$$

And, for charge neutrality, the charge on the gate, Q_G , equals the charge in the semiconductor, Q_s , and

$$Q_G = \epsilon_0 \epsilon_i F_i = \epsilon_0 \epsilon_i V_i / d_i = C_i V_i = -Q_s \quad (2.21)$$

Where F_i is the field in the gate dielectric, and C_i is the capacitance/unit area of the gate dielectric. Hence,

$$V_G = V_s - Q_s / C_i \quad (2.22)$$

Equation 2.22 can be used to relate the voltage on the gate of an MIS capacitor to the induced charge density in the semiconductor, Q_s , and to the associated band bending, V_s . It can also be used to calculate the threshold voltage, V_T , of the structure, i.e. the gate voltage necessary to induce band bending of $2V_F$ at the semiconductor surface:

$$V_T = 2V_F + \frac{\sqrt{2q\epsilon_0\epsilon_s N_a 2V_F}}{C_i} \quad (2.23)$$

Figure 2.6 shows the calculated variation of V_G with V_s for the two substrate doping levels used in Fig. 2.3, and for a 150 nm thick gate dielectric of SiO_2 . The more heavily doped substrate requires a larger gate bias to achieve a given degree of band bending in depletion, and, equally, has a larger value of V_T , as shown by Eq. 2.23. Once the surface has gone into strong inversion, the free electron density, Q_n , dominates Q_s , and Q_n is given by:

$$Q_n = C_i(V_G - V_T) \quad (2.24)$$

As will be seen in Chap. 3, this is a widely used expression for the calculation of channel currents in MOSFET devices above threshold. It is equally widely used for similar calculations in TFTs. Hence, the threshold voltage is a key parameter in determining on-state device characteristics, and the dependence of threshold voltage on substrate doping level is shown in Fig. 2.7.

2.2.3 Real MIS Structures

In contrast to the idealised MIS structure shown in Fig. 2.1, real structures may have work function differences between the gate metal and the semiconductor,

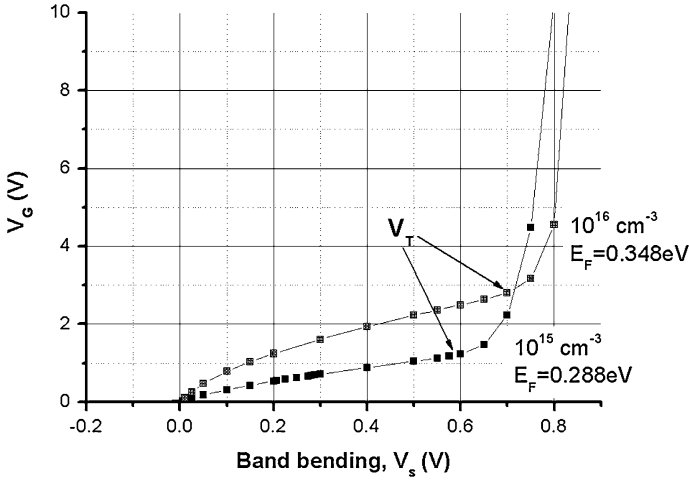
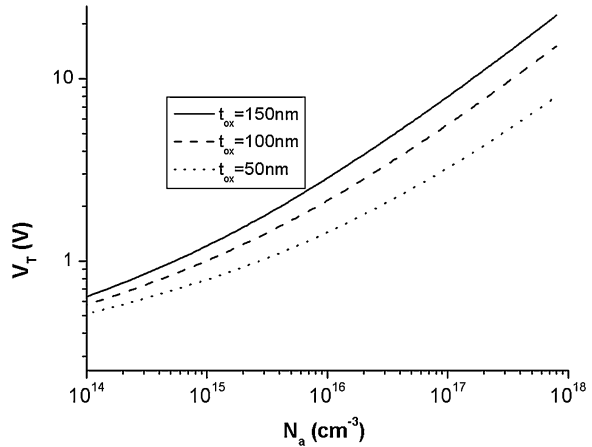


Fig. 2.6 Calculated variation of surface potential, V_s , with gate bias, V_G , in an ideal MIS structure, and showing the threshold voltage points. (Dielectric layer of 150 nm of SiO_2 , and p-type substrate doping of $1 \times 10^{15} \text{ cm}^{-3}$, and $1 \times 10^{16} \text{ cm}^{-3}$)

Fig. 2.7 Calculated variation of threshold voltage with substrate doping level, and thickness of SiO_2 gate dielectric



fixed charges in the oxide, and interface trapping states at the dielectric/semiconductor interface. These will change the zero-gate-bias band bending, and affect the relationship between V_G and V_s and Q_s .

2.2.3.1 Work Function Differences

In general, the Fermi level position in a free metal will be different from the Fermi level in a free semiconductor. These differences are usually expressed in terms of a work function difference, where the work function is the energy required to remove

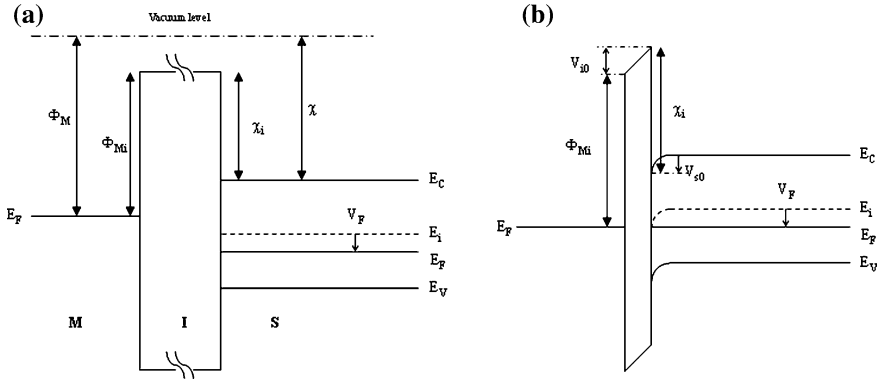


Fig. 2.8 MIS energy band diagrams in the presence of metal–semiconductor work function differences: **a** separated metal–insulator and insulator–semiconductor, **b** MIS system in thermal equilibrium

an electron from the Fermi level to the vacuum level. When the two materials are connected, and in thermal equilibrium, the Fermi levels need to be coincident, and there will be a flow of electrons from one material to the other, resulting in an interfacial dipole, which establishes this equilibrium. In the semiconductor, this will result in surface band bending, the extent of which will be much greater than in the metal due to the short screening length of the latter’s high electron density.

In an MIS structure, it is conventional to reference the Fermi levels to the dielectric’s conduction band edge [4] (rather than to the vacuum level), so that the quoted barriers, Φ_{Mi} and χ_i , are the energies needed to remove an electron to the dielectric conduction band (as shown in Fig. 2.8, and χ is the electro-negativity of the semiconductor). For the Si/SiO₂ system, these barrier energies were experimentally established by photo-emission measurements from the metal gate or the semiconductor into the oxide conduction band, and were 0.5–1 eV less than the respective vacuum values [5]. Figure 2.8a schematically shows the metal and the semiconductor separated, and Fig. 2.8b shows them connected in thermal equilibrium. In this case, electrons have flowed from the metal to the semiconductor to bring the Fermi levels into coincidence. As a result of this, the bands in the semiconductor have bent downwards by V_{s0} , with a corresponding voltage drop across the dielectric of V_{i0} . Equating the potentials either side of the high point in the insulator conduction band:

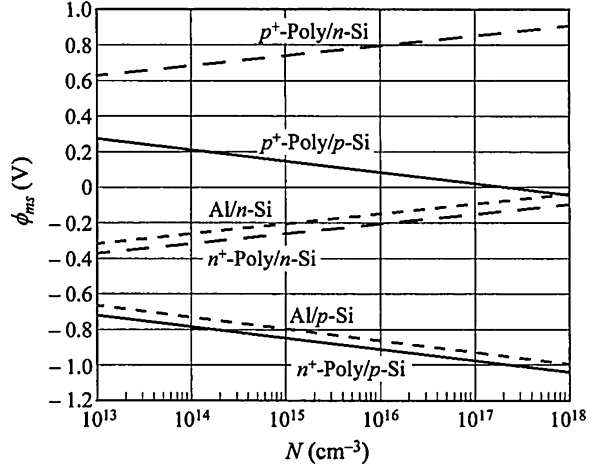
$$\Phi_{Mi} + V_{i0} = \chi_i + E_i/q + V_F - V_{s0} \quad (2.25)$$

The metal–semiconductor work function difference, Φ_{MS} , is, therefore, given by:

$$\Phi_{MS} = \Phi_{Mi} - (\chi_i + E_i/q + V_F) = -(V_{i0} + V_{s0}) \quad (2.26)$$

Thus, to remove the zero gate bias band bending in the system, and to restore flat band conditions, the gate voltage needs to be made more negative to induce

Fig. 2.9 Experimentally determined MOS work-function differences, Φ_{MS} , as a function of Si-substrate doping level, for different gate contact materials. (Reproduced from [1] with permission of John Wiley & Sons, Inc)



more positive charge in the semiconductor surface. The gate voltage at flat bands, V_{FB} , is given by:

$$V_{FB} = \Phi_{MS} = -(V_{i0} + V_{s0}) = -\left(\frac{\sqrt{2q\epsilon_0\epsilon_s N_a V_{s0}}}{C_i} + V_{s0}\right) \quad (2.27)$$

Equally, the gate voltage required to achieve a given degree of band bending, including the threshold for inversion, will be modified by the metal–semiconductor work function difference, so that the expression for the threshold voltage now becomes:

$$V_T = V_{FB} + \frac{\sqrt{2q\epsilon_0\epsilon_s N_a 2V_F}}{C_i} + 2V_F \quad (2.28)$$

As indicated in Eq. 2.26, the work function difference will be a function both of the gate metal, and of the doping level in the semiconductor substrate, as shown in Fig. 2.9 for Al and doped poly-Si gates [1]. Due to its refractory properties, doped poly-Si has been extensively employed as the gate electrode in MOSFET technology, and, with appropriate doping, it can be tailored to produce the required sign of flat band voltage.

2.2.3.2 Oxide Charges and Interface States

Many gate dielectrics, including SiO_2 , are characterised by charged centres in the oxide, which induce an opposite charge in the semiconductor surface. If the charged centres, Q_i , are located at a distance x from the dielectric–semiconductor interface in an MIS capacitor, the charge induced in the semiconductor, Q_s , is:

$$Q_s = Q_i(d - x)/d \quad (2.29)$$

Hence, for charges at the dielectric/semiconductor interface, the induced charge is equal to the charge, Q_i , in the dielectric, whilst those at the metal interface have no effect. In many cases, the location of the charges may not be known, and an effective charge density, Q_{ieff} , will be determined, as though it were located at the dielectric/semiconductor interface.

As with the work function difference, this will result in a non-zero flat band voltage, given by:

$$V_{\text{FB}} = - Q_{\text{ieff}}/C_i \quad (2.30)$$

Positive charges are commonly found in SiO_2 films on Si, and are referred to as ‘fixed’ charges, as their effect is not dependent upon the surface potential in the semiconductor. In other words, they have a constant effect, irrespective of the bias conditions, and present a fixed density.

In real crystalline semiconductor surfaces, the termination of the regular, periodic bulk potential introduces allowed states into the forbidden band gap, usually referred to as surface states. These are intrinsic states at the surface, and, in addition to these, there may be extrinsic states due to impurities. The densities of intrinsic states can be up to $\sim 10^{15} \text{ cm}^{-2}$ on an atomically clean surface, but, in a well-passivated surface, such as the Si/ SiO_2 interface produced by thermal oxidation of Si, these can be reduced to $< 1-5 \times 10^{12} \text{ cm}^{-2}$. The reduction is due to the SiO_2 network providing oxygen pairing atoms for the Si dangling bonds, and further passivation with hydrogen typically reduces the overall density to $\sim 10^{10} \text{ cm}^{-2}$ or less. This combination of thermal oxidation and hydrogen passivation has generated one of the best-controlled semiconductor interfaces, and provided the basis for the Si semiconductor device industry.

Surface or interface states are generally distributed in energy across the forbidden band gap, and, in the case of the Si/ SiO_2 interface, the distribution is U-shaped between the valence and conduction band edges. In contrast to the fixed charge, the charge in interface states will be determined both by their distribution across the band gap, and by the position of the Fermi level at the surface. Using the zero Kelvin approximation, those states beneath the Fermi level can be regarded as filled with electrons, whilst those above will be empty. Take, for example, a constant density, $N_{\text{ss}}(E)$, across the band gap, with acceptor levels in the upper half of the band gap, and donor levels in the lower half, and with a neutral level, E_0 , at mid-gap. This distribution will have zero net charge in the interface states when the surface Fermi level is at mid-gap. However, if this distribution were added to the MIS band diagram used in Fig. 2.1a, where the Fermi level is below mid-gap, there would be a flow of electrons from the interface states below E_0 , leading to positively charged, empty donor states at the surface, and an equal negative charge density in the semiconductor surface. Hence, the semiconductor bands at the surface will be bent down by an amount V_{s0} to ensure charge neutrality between the interface and the bulk, as shown in Fig. 2.10. In this example, the block of donor states between E_F and E_0 would be empty of electrons, and have a positive charge, Q_{ss} , balanced by the negative semiconductor surface charge, Q_s .

In general, the electron occupancy, $F(E)$, of a surface state at energy E is given by the Fermi–Dirac distribution function:

$$F(E) = \frac{1}{1 + \exp(qV_F - qV_S - E)/kT)} \quad (2.31)$$

Using the polarity convention of the earlier sections, E will have a negative value for centres above E_0 (which is at mid-gap), and a positive value for those below. Hence, the total negative charge in the surface states, Q_{ss}^- , with band bending $V_s > V_F$ is:

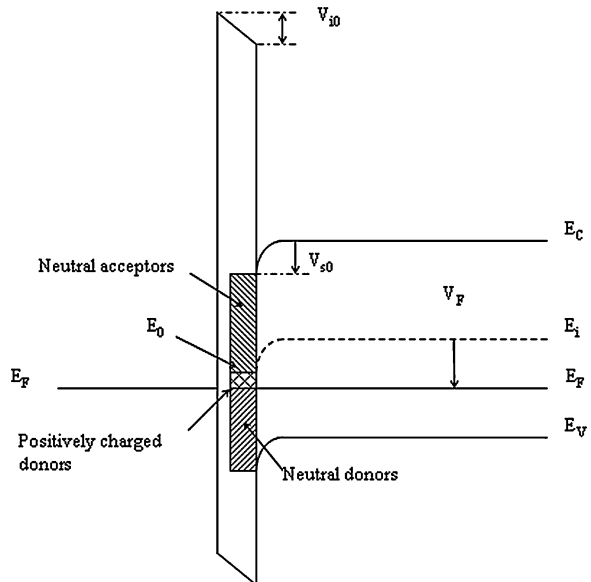
$$Q_{ss}^-(V_s) = - \int_{E_0}^{E_C} qN_{ss}(E)F(E)dE \approx - \int_{E_0}^{E_0+q(V_s-V_F)} qN_{ss}(E)dE \quad (2.32)$$

In Eq. 2.32, the full integral expression, which includes the Fermi–Dirac function, can be reduced to the simpler analytical form by using the zero Kelvin approximation, in which the acceptor states are negatively charged between the neutral level and the surface Fermi level, and neutral above the Fermi level. For a uniform distribution of acceptor states, N_{ss} can be brought outside the integral, and the density of negatively charged states, when $V_s > V_F$, is:

$$Q_{ss}^-(A) = -qN_{ss}q(V_s - V_F) \quad (2.33)$$

Similarly, for $V_s < V_F$ (as shown in Fig. 2.10), the density of positively charged donor states is:

Fig. 2.10 Zero gate-bias MIS band diagram with a uniform distribution of interface states across the band gap, and with the cross-hatched region showing the charged states. (Donor and acceptor states in the lower and upper halves of the band-gap, respectively, and with the neutral level at mid-gap)



$$Q_{ss}^+(D) = qN_{ss}q(V_F - V_s) \quad (2.34)$$

For a constant distribution of surface states, the zero Kelvin approximation is a useful simplification. However, for trapping state distributions where the density varies significantly over an energy interval of kT , it is less accurate, and a numerical evaluation of the full integral in Eq. 2.32 would be required. This issue is discussed further in Sect. 6.2.3, where the volume trap density in a-Si:H varies exponentially with position from the band edge.

As with the work function difference and the fixed oxide charge, a bias, V_{FB} , will need to be applied to the gate to establish the flat band condition in the semiconductor, where V_{FB} is given by:

$$V_{FB} = -\frac{Q_{ss}(D)(V_s = 0)}{C_i} = -\frac{qN_{ss}qV_F}{C_i} \quad (2.35)$$

However, in contrast to the fixed oxide charge, the presence of interface states will give more than just a constant shift in the relationship between V_G and V_s and Q_s . In particular, as V_s is increased, not only does the gate bias need to induce the increasing value of Q_s , but it must also supply the increasing charge going into the interface states. The relationship between V_G and V_s from Eq. 2.22 is modified to be:

$$V_G = V_s - \frac{Q_s}{C_i} - \frac{Q_{ss}^+(D)}{C_i} - \frac{Q_{ss}^-(A)}{C_i} \quad (2.36)$$

and, for the example being used, $Q_{ss}(A) = 0$ for $V_s < V_F$, and $Q_{ss}(D) = 0$ for $V_s > V_F$, and the non-zero values of $Q_{ss}(A)$ and $Q_{ss}(D)$ are negative and positive, respectively.

Figure 2.11a compares the relationship, between V_G and V_s , for an ideal trap-free interface ($N_{ss} = 0$) and an interface containing a range of N_{ss} densities from $1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ to $1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$. The lowest interface state density of $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ is so low that the V_G - V_s relationship is indistinguishable from the trap-free case. However, for the higher densities, increasingly large values of V_G are required to achieve a given amount of band-bending due to the charge going into the interface states. The curves have a common crossing point at $V_s = 0.288 \text{ V}$, when the surface Fermi level is at mid-gap. This corresponds to the neutral level of the interface states, so that all the interface state distributions have the same zero charge in them. The flat band voltages can also be directly read from the curves by the values of V_G corresponding to $V_s = 0 \text{ V}$.

The other parameter which can be extracted from these curves is the value of V_s when $V_G = 0$, which is the equilibrium zero-gate-bias bend banding, V_{s0} , and these values, together with the corresponding values of Q_{ss} (at V_{s0}), are shown in Fig. 2.11b. The 'S'-shaped curves demonstrate some simple physical principles of charge trapping over the range of N_{ss} values used. For low N_{ss} values, such as $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$, the Fermi level position at the surface is dominated by the substrate doping level, and the surface states have almost no effect. In this case, the N_{ss} -

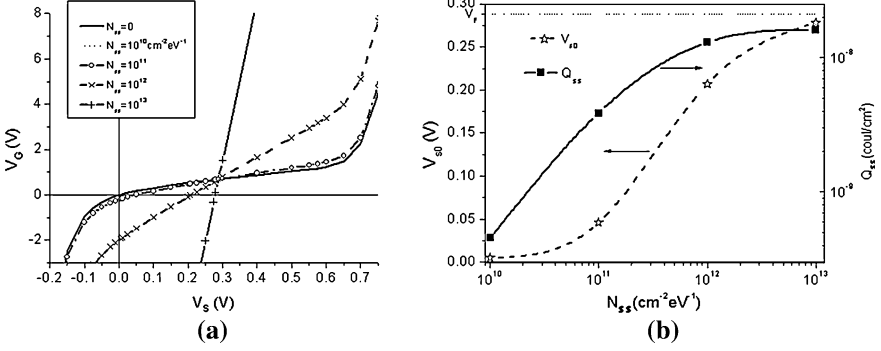


Fig. 2.11 Calculations using the uniform interface state distribution shown in Fig. 2.10 **a** variation of gate bias with surface potential, V_s , for different values of N_{ss} , and **b** variation of zero gate bias band bending, V_{s0} , and Q_{ss} (at V_{s0}) with N_{ss} . (Substrate acceptor density, $N_a = 10^{15} \text{ cm}^{-3}$, $qV_F = 0.288 \text{ eV}$, $t_{ox} = 150 \text{ nm}$, and interface state density, $N_{ss} = 10^{10} - 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$)

induced band bending tends towards zero, and the interface states are ionised almost down to the position of the bulk Fermi level, and $Q_{ss} \sim qN_{ss}qV_F$. Although a substantial fraction of the states are ionised, the charge in them is so low, that negligible band bending is required to produce an approximately equal amount of charge in the substrate. In contrast, for high N_{ss} values, such as $10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, the band-bending is dominated by the charge in the surface states, and the Fermi level tends towards being pinned at the surface state neutral level, i.e. $V_{s0} \Rightarrow V_F$. In this case, $V_F - V_{s0} = 0.01 \text{ V}$, and the surface state neutral level is just 100 meV above the Fermi level. However, with the large surface state density, this still corresponds to a substantial charge, Q_{ss} , in the fractionally ionised donor surface states. For intermediate values of N_{ss} between 10^{11} and $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$, there is a progressive increase in V_{s0} with N_{ss} , and Q_{ss} is given by $qN_{ss}q(V_F - V_{s0})$.

Equation 2.36 also shows that the charge going into surface states has to be allowed for in calculating the gate threshold voltage for surface inversion. The surface potential at which this occurs is still $2V_F$, but the gate bias, in excess of the flat band voltage, to achieve this surface potential is increased to:

$$V_T = V_{FB} + \frac{\sqrt{2q\epsilon_0\epsilon_s N_a 2V_F}}{C_i} + 2V_F + \frac{Q_{ss}(V_s = 2V_F)}{C_i} \quad (2.37)$$

and, as $Q_{ss}(D) = 0$ for $V_s > V_F$, only charge in the acceptor states will contribute, and from Eq. 2.33, $Q_{ss}(A)$ at inversion is given by:

$$Q_{ss}(A) = qN_{ss}q(2V_F - V_F) = qN_{ss}qV_F \quad (2.38a)$$

Finally, the effects of the work function difference, the dielectric charge and the charge in interface states are all independent and additive, so that, in the presence of all three, the flat band voltage is given by:

$$V_{FB} = \Phi_{MS} - Q_{ieff}/C_i - Q_{ss}(V_s = 0)/C_i \tag{2.38b}$$

2.2.4 Evaluation of Surface Potential

From Eq. 2.9, the surface potential, V_s , uniquely defines the space charge density, Q_s , and Eqs. 2.22 and 2.36 define the gate bias, V_G , needed to achieve that potential, with and without surface states, respectively. Therefore, the measurement of V_s facilitates a quantitative insight into the state of a semiconductor surface. A common technique for establishing V_s is through the small signal capacitance-voltage measurement of an MIS diode, where the capacitance is given by:

$$C = \frac{dQ_G}{dV_G} = -\frac{dQ_s}{dV_G} = -\frac{dV_s}{dV_G} \frac{dQ_s}{dV_s}$$

$$\frac{dV_G}{dV_s} = 1 - \frac{1}{C_i} \frac{dQ_s}{dV_s} \text{ and } \frac{dQ_s}{dV_s} = -C_s \tag{2.39}$$

$$\therefore C = 1/(1/C_i + 1/C_s)$$

In other words, the capacitance of the MIS diode is the series combination of the capacitance of the dielectric, C_i , and of the semiconductor surface, C_s , where C_s is given by the differentiation of Eq. 2.9:

$$C_s = \frac{\sqrt{n_i q \epsilon_0 \epsilon_s} [\text{sh}q(V_s - V_F)/kT + \text{sh}qV_F/kT]}{G(V_s, V_F)} \tag{2.40}$$

and $G(V_s, V_F)$ is given by Eq. 2.10. The normalised C–V curves resulting from the evaluation of Eq. 2.40, for a silicon substrate doped with 10^{15} and 10^{16} acceptors/cm³, and a gate oxide thickness of 150 nm, are shown by the solid lines in

Fig. 2.12 Normalised high and low frequency MIS C–V curves (calculated for 150 nm thick SiO₂ gate dielectric)

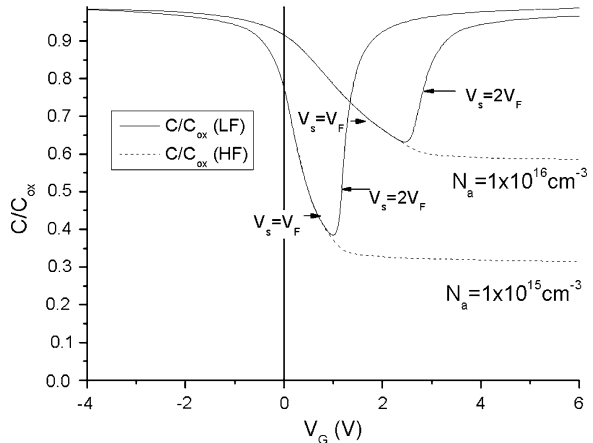


Table 2.2 Relationship between normalised flat band capacitance, minimum C–V capacitance and substrate doping level (for 150 nm SiO₂ gate dielectric)

N_a (cm ⁻³)	C_{FB}/C_i	$C_{min(LF)}/C_i$	$C_{min(HF)}/C_i$
1×10^{15}	0.77	0.38	0.32
1×10^{16}	0.91	0.63	0.59

Fig. 2.12. These curves have a characteristic ‘V’ shape, with the capacitance at negative V_G values tending towards the capacitance of the gate dielectric, due to the large capacitance of the hole accumulation layer. With increasing positive V_G , the capacitance falls due to the growth of the hole depletion region at the surface, which progressively reduces the surface capacitance. Finally, the curves start to rise as the surface becomes strongly inverted, and the large free electron concentration screens the underlying depletion layer, with the total capacitance once again tending towards the value of the gate dielectric.

As these curves have been calculated for an ideal MIS diode, the energy bands will be flat at $V_G = 0$, and, hence, the normalised capacitance at flat bands can be directly obtained from the curves. Given the unique relationship between surface potential and capacitance, the flat band voltage can, in principle, be directly obtained from any experimental C–V measurement using Eq. 2.40, assuming that the substrate doping level is known. Moreover, the minimum capacitance is also a unique function of doping level and dielectric capacitance, so that the doping level can be extracted from the minimum of the experimental C–V curve. The normalised flat band and minimum capacitance values from Fig. 2.12 are listed in Table 2.2, and they have also been extensively tabulated by Sze and Ng [1]. Also marked on the curves in Fig. 2.12 are the capacitance values at which the band bending gives an intrinsic surface ($V_s = V_F$), and the threshold for an inverted surface ($V_s = 2V_F$).

The solid line calculations assume thermal equilibrium, and the increase in capacitance in inversion will only be observed experimentally if the free electrons in the inversion layer can follow the a.c. measuring signal. In a high quality Si/SiO₂ capacitor, the inversion layer response time can be of the order of seconds, or more [6], as it depends upon a thermal generation process within the surface space charge region. Hence, the calculated curves are only likely to be replicated with a low frequency measurement, and the solid line curves in Fig. 2.12 are often referred to as low frequency C–V curves. Moreover, in the presence of interface states, there can be a further complication in the interpretation of the experimental low frequency curves. This will arise if the occupancy of the interface states at the Fermi level can follow the measuring signal, and, hence, contribute an interface state capacitance, C_{ss} , in parallel with the semiconductor surface capacitance C_s . The surface state capacitance, C_{ss} , is given by:

$$C_{ss} = -\frac{dQ_{ss}}{dV_s} \sim qN_{ss} \quad (2.41)$$

where, as discussed in the previous section, Q_{ss} can be approximated by $qN_{ss}q(V_s - V_F)$ for constant (or slowly varying) surface state densities. The presence of C_{ss} in an experimental C–V measurement means that Eq. 2.40 can no longer be used to give a unique relationship between measured capacitance and band bending, V_s . By implication, a high frequency measurement can be used to minimise the capacitive contributions of the surface states, and will also suppress the free electron capacitance in strong inversion. Hence, to interpret the high frequency C–V curves, a high frequency version of Eq. 2.40 is required. This essentially means suppressing the electron response in inversion, and this can be accomplished by expanding the cosh and sinh terms containing V_s , and setting to zero those of the form $\exp(q(V_s - V_F)/kT)$, since, in inversion, $V_s > V_F$ and those terms will govern the electron contribution to the surface capacitance. Hence the high frequency expression, $C_{s(HF)}$ is given by:

$$C_s = \frac{\sqrt{n_i q \epsilon_0 \epsilon_s} [-0.5 \exp -q(V_s - V_F)/kT + \text{sh}qV_F/kT]}{G'(V_s, V_F)} \quad (2.42)$$

and $G'(V_s, V_F)$ is given by:

$$G'(V_s, V_F) = \mp \sqrt{\left[0.5 \frac{kT}{q} \exp \frac{q(V_F - V_s)}{kT} - \frac{kT}{q} \text{ch} \frac{qV_F}{kT} + V_s \text{sh} \frac{qV_F}{kT} \right]} \quad (2.43)$$

The high frequency C–V curve, calculated from Eq. 2.42, for $qV_s > 3kT$, is shown by the dotted lines in Fig. 2.12. The inversion layer response has been suppressed, and the surface capacitance in inversion tends to a constant value, approximately given by:

$$C_{s(HF)} = \frac{\epsilon_0 \epsilon_s}{x_{d(\max)}} \quad (2.44)$$

Where $x_{d(\max)}$ is the limiting maximum thickness of the surface depletion region, as discussed in Sect. 2.2.1, and is given by Eq. 2.18. As with the minimum capacitance value of the low frequency curves, the minimum value of the high frequency curves is also a unique function of doping level, and can be used to establish the doping level in experimental samples. These values are also shown in Table 2.2. More importantly, any horizontal displacement, ΔV_G , of an experimental C–V curve from the theoretical C–V curve can be used to establish Q_{ss} , as a function of V_s , from:

$$Q_{ss}(V_s) = \Delta V_G / C_i \quad (2.45)$$

and N_{ss} can then be derived from dQ_{ss}/dV_s .

Whilst the emphasis in this section has been on high frequency measurements, and the use of the measured MISC capacitance to establish surface potential, there is also a low frequency procedure, called the quasi-static C–V measurement, which uses the change in capacitance, at a given value of V_G , to determine N_{ss} [7, 8]. Finally, to complete this section, one other well-established technique for the

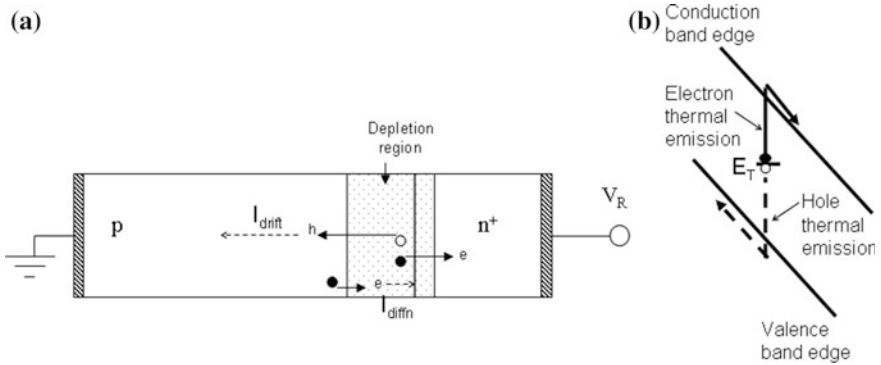


Fig. 2.13 Illustration of **a** reverse biased n^+ - p junction, showing generation and diffusion leakage currents, and **b** e - h pair thermal generation process

evaluation of surface state densities should be mentioned, and this is the a.c. conductance measurement of MISCs [9]. A detailed overview of these procedures can be found in Sze and Ng [1].

2.3 Electron-Hole Pair Generation and Recombination

Electron-hole pair generation and recombination are fundamental semiconductor processes relevant to both off-state leakage currents and to steady-state photocurrents in TFTs.

Two sources of leakage current in semiconductor devices are by ohmic conduction in lightly conducting and/or low generation lifetime material, or by electron-hole pair generation and/or diffusion current flow in reverse biased junctions. The latter processes are illustrated in Fig. 2.13a for a reverse biased n^+ p junction. Due to the field within the space charge region, the holes generated within this region are swept into the p -type substrate, where they constitute an ohmic (drift) hole current to the substrate contact, I_{drift} . Equally, the electrons generated in the space charge layer are swept into the n^+ region, where they flow to the n^+ contact. For current continuity, there will be equal hole and electron currents, and these are referred to as generation currents. The electron-hole pair generation process, from a deep lying centre within the forbidden band gap, is shown schematically in Fig. 2.13b. In addition to the direct generation process, there is also a diffusion current, I_{diff} , of minority carrier electrons from the neutral p -type substrate into the adjacent depletion region.

The role of electron-hole pair generation on leakage currents, including the diffusion current, is discussed in Sect. 2.3.3, and the recombination processes are presented in Sect. 2.3.4.

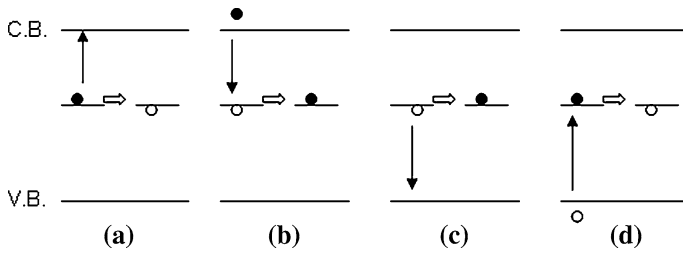


Fig. 2.14 Carrier emission and capture processes from a deep level centre in the forbidden band gap: **a** electron emission, **b** electron capture, **c** hole emission **d** hole capture. The *horizontal block arrow* shows the state's occupancy after the transition

In order to develop the expressions for electron-hole pair generation and recombination, it is necessary to consider the basic processes of carrier emission and carrier capture by a deep level centre, based upon the Shockley, Read, Hall (SRH) recombination statistics [10, 11], and the extension of this analysis to p-n junction characteristics [12].

The term deep level centre refers to intrinsic or extrinsic defects having energy levels within the forbidden band gap of the semiconductor, and which are usually further from the band edges than the shallow level dopant impurities. A deep level centre can behave as a trap, or as a generation centre, or as a recombination centre, depending upon its environment. For instance, in thermal equilibrium, a deep level acceptor in n-type material can capture electrons, thereby, reducing the free carrier density, and is acting as trap.³ In a reverse biased space charge region, it can act as a generation centre, sequentially emitting electrons and holes, resulting in a reverse bias leakage current. Or, in material subject to electron-hole pair injection, it can act as a recombination centre, where the sequential electron and hole capture process establishes the steady-state free carrier density under the injection conditions. Hence, all three terms are often used interchangeably to refer to the same deep level centre, and, for brevity, the term trap is used as the generic term for the centre in this section.

2.3.1 Thermal Equilibrium

For a deep level centre within the semiconductor's forbidden band gap, four carrier transitions can be identified, as shown in Fig. 2.14. If the trap is an acceptor level, it has two charge states, one of which is negatively charged when it is occupied by an electron, and the other is neutral when it is empty of the electron (These two charge states can be equivalently described in terms of hole occupancy, which are empty

³ The Fermi level position and the free electron concentration can be obtained from the numerical solution of the charge neutrality equation: $n + N_T^- = N_d^+$.

and filled, respectively. The same transitions will occur from a deep donor centre, the only difference being that it is positively charged when empty of an electron and neutral when occupied by an electron). Hence, there is a pair of possible carrier transitions from each of the two charge states, as shown in Fig. 2.14. From the negatively charged acceptor centre, these are either (a): electron emission to the conduction band, by a thermally stimulated process, or (d): hole capture from the valence band, and the release of phonon energy back to the lattice. Both leave behind the neutral centre. From the neutral centre, the two possible transitions are (b): electron capture from the conduction band, or (c): thermally stimulated hole emission to the valence band (which is equivalent to electron emission from the valence band). Both leave behind the negatively charged centre.

If the density of traps/generation/recombination centres is N_T , and if the centre and the Fermi level are positioned at E_T and E_F , respectively, above the valence band edge, then the trap occupancy is defined by the Fermi–Dirac distribution function, and from this the carrier transition rates can be calculated. These rates are determined by the number of free carriers and the appropriate occupancy of the centre, for the capture process, or just by the occupancy of the centre for the emission process (where it is implicitly assumed that there are sufficient empty states in the bands to accommodate the emitted carriers). In thermal equilibrium, the fractional electron occupancy of the trap, $F_D(E_T, E_F)$, is given by the Fermi–Dirac distribution function:

$$F_D = \frac{1}{1 + \exp(E_T - E_F)/kT} \quad (2.46)$$

The free carrier densities, n_0 and p_0 , in n-type material doped with N_d donors, are given by⁴:

$$n_0 + N_T^- = N_d = N_C \exp -(E_C - E_F)/kT, p_0 = N_V \exp -E_F/kT \quad (2.47)$$

$$\text{and } n_0 p_0 = n_i^2 \quad (2.48)$$

The electron emission rate, R_{ee} is:

$$R_{ee} = e_n N_T^- = e_n N_T F_D \quad (2.49)$$

where e_n is the electron emission rate constant. Similarly, the rate of hole emission, R_{he} , is:

$$R_{he} = e_p N_T^0 = e_p N_T (1 - F_D) \quad (2.50)$$

where e_p is the hole emission rate constant. The rates of electron capture, R_{ec} , and hole capture, R_{hc} , are:

$$R_{ec} = c_n n_0 N_T^0 = \sigma_n v_{th} n_0 N_T (1 - F_D) \quad (2.51)$$

⁴ From 2.47, if $N_T \ll N_d$, $E_F = kT \ln(N_d N_V / n_i^2)$.

$$R_{hc} = c_p p_0 N_T^- = \sigma_p v_{th} p_0 N_T F_D \quad (2.52)$$

where the electron and hole capture rate constants, c_n and c_p , are given by the product of the trap's capture cross section, σ_n and σ_p , respectively, and the carrier's thermal velocity, v_{th} . The thermal velocity is $\sqrt{(3kT/qm^*)}$, where m^* is the effective mass, so that the thermal velocities for holes and electrons are different from each other. However, for simplicity in this analysis, they are taken to be the same.

In thermal equilibrium, the rate of electron capture must equal the rate of electron emission, and the equivalent equality must also exist for the hole transitions. Hence,

$$e_n N_T F_D = \sigma_n v_{th} n_0 N_T (1 - F_D) \quad (2.53)$$

And substituting for F_D and n_0 , using Eqs. 2.46 and 2.47, respectively:

$$e_n = \sigma_n v_{th} N_C \exp -(E_C - E_T)/kT \quad (2.54)$$

Similarly, for the hole transitions:

$$e_p = \sigma_p v_{th} N_V \exp -E_T/kT \quad (2.55)$$

Hence, the thermal emission rate constants, e_n and e_p , are fundamental properties of the trap itself, and not dependent on the local concentrations of carriers. Moreover, their values are exponentially dependent upon the separation of the trap from the band edges.

2.3.2 Non-equilibrium, Steady State

Under steady state, non-thermal equilibrium conditions (where $np \neq n_i^2$), the trap will achieve a new occupancy, described by its quasi-Fermi level, and determined by the equality of the net electron transition rate and the net hole transition rate,⁵ i.e.

$$\frac{dN_T^-}{dt} = R_{ec} - R_{ee} + R_{he} - R_{hc} = 0 \quad (2.56)$$

In contrast to the thermal equilibrium situation, the rates of electron emission and electron capture will not be equal. This is the situation in which there will be a net recombination or a net generation process, depending upon the divergence of the carrier concentrations from their thermal equilibrium values. Substituting the rate constants into Eq. 2.56 gives:

$$nc_n N_T^0 - e_n N_T^- = pc_p N_T^- - e_p N_T^0 \quad (2.57)$$

⁵ If these rates are not equal, then the trap occupancy will change with time.

From Eq. 2.57, and using $N_T^0 = N_T - N_T^-$, the hole occupancy is:

$$N_T^0 = \frac{N_T(e_n + pc_p)}{nc_n + pc_p + e_n + e_p} \quad (2.58)$$

This can be used to calculate the net local electron generation/recombination rate, R_{GR} , which, in steady state, will also be equal to the net hole recombination/generation rate, i.e.:

$$R_{GR} = R_{ee} - R_{ec} = N_T^- e_n - nc_n N_T^0 \quad (2.59)$$

Substituting for the trap occupancy terms:

$$R_{GR} = \frac{N_T(e_n e_p - np c_n c_p)}{nc_n + pc_p + e_n + e_p} \quad (2.60)$$

$$R_{GR} = \frac{\sigma_n \sigma_p v_{th} N_T [\{N_C N_V \exp -(E_C - E_T)/kT \cdot \exp -E_T/kT\} - np]}{\sigma_n (n + N_C \exp -(E_C - E_T)/kT) + \sigma_p (p + N_V \exp -E_T/kT)} \quad (2.61)$$

Eliminating the exponential terms in E_T in the numerator, and replacing the remaining exponential term by n_i^2 , gives the following expression:

$$R_{GR} = \frac{\sigma_n \sigma_p v_{th} N_T [n_i^2 - np]}{\sigma_n (n + N_C \exp -(E_C - E_T)/kT) + \sigma_p (p + N_V \exp -E_T/kT)} \quad (2.62)$$

The numerator shows that the rate of recombination/generation is proportional to the term $(n_i^2 - np)$, which expresses the deviation of the carrier population from thermal equilibrium. For $np > n_i^2$, the free carrier excess stimulates a net recombination process, where the carrier excess could result, for example, from optical illumination of the device, the forward biasing of a p-n junction or avalanche generation at a reverse biased p-n junction. For $np < n_i^2$, the free carrier deficit gives rise to net generation, and the free carrier deficit is most commonly encountered in the depletion region of a reverse biased p-n junction. In thermal equilibrium, the net rates of recombination or generation are zero.

Equation 2.60 (or its equivalents 2.61 or 2.62) would be typically used in device simulation packages to calculate the local rates of recombination or generation, but, for analytical work, a simplified version of this expression is often used by making the simplifying assumption that $\sigma_n = \sigma_p = \sigma$, and:

$$R_{GR} = \frac{\sigma v_{th} N_T [n_i^2 - np]}{n + p + 2n_i \cosh(E_T - E_i)/kT} \quad (2.63)$$

where the following substitutions have been used for N_C and N_V in the denominator:

$$n_i = N_C \exp -(E_C - E_i)/kT = N_V \exp -E_i/kT \quad (2.64)$$

2.3.3 Generation Currents

As mentioned above, the general treatment of generation or recombination is fully specified by the use of Eq. 2.60, and, in this section, an approximate, but more accessible, analytical treatment is presented for describing generation currents. For instance, in the space charge layer of a reverse biased junction, as shown in Fig. 2.13a, the free carrier concentrations can be taken as zero, so that there are no carrier capture processes, and Eq. 2.60 reduces to an expression for the local, steady state generation rate, R_G :

$$R_G = \frac{N_T e_n e_p}{e_n + e_p} \quad (2.65)$$

The steady state leakage current, J_R , due electron-hole pair generation, in a reverse biased p-n junction depletion layer of width W is:

$$J_R = q \int_0^W R_G dx = q R_G W = q W N_T \frac{e_n e_p}{e_n + e_p} \quad (2.66)$$

Where it is assumed that R_G is constant across W , and, in analogy with Eq. 2.18, W is given by:

$$W = \sqrt{\frac{2\epsilon_0 \epsilon_s (V_R + V_0)}{q N_a}} \quad (2.67)$$

V_R is the reverse bias, and V_0 is the built-in p-n junction potential.

Returning to Eq. 2.66, the ratio $e_n e_p / (e_n + e_p)$ is a maximum when the denominator is a minimum, which will occur when $e_n = e_p$, and the traps are sited close to mid-gap. As E_T moves away from mid-gap either e_n or e_p will increase exponentially, as will the sum $e_n + e_p$, whilst the product $e_n e_p$ will be invariant. Hence, any centres located at mid-gap are likely to be the most efficient generation centres, and will dominate the device leakage current, J_R . For mid-gap centres, with equal capture cross sections, σ :

$$e_n = e_p = \sigma v_{th} N_C \exp -E_i/kT = \sigma v_{th} n_i \quad (2.68)$$

$$\therefore J_R = q R_G W = 0.5 q n_i W \sigma v_{th} N_T \quad (2.69)$$

The *generation lifetime*, τ_g , is a figure of merit for the leakage current, and is defined by the following relationship:

$$J_R \equiv q n_i W / \tau_g \quad (2.70)$$

Hence, for mid-gap centres, the generation lifetime is:

$$\tau_g = 1 / (0.5 N_T \sigma v_{th}) \quad (2.71a)$$

If the capture cross-sections are not equal:

$$\tau_g = 1/(N_T \sigma_n v_{th}) + 1/(N_T \sigma_p v_{th}) \quad (2.71b)$$

Equation 2.71b explicitly shows that the rate of the two-stage generation process is determined by the sequential emission of holes and electrons, and, if one capture cross-section is larger than the other, then the overall generation process will be rate limited by carrier emission from the charge state of the centre having the smaller cross-section. In experimental samples, this difference in capture cross-sections is likely to be found. For example, if the trap is an acceptor, then it will be neutral before capturing an electron, and negatively charged before capturing a hole. The Coulombic attraction between the hole and the negatively charged centre will result in the hole capture cross-section being larger than the neutral cross-section for electron capture [13]. As an example of this, one of the most widely studied deep level centres in silicon is gold, which has a near mid-gap acceptor level at 0.54 eV below the conduction band edge, and its capture cross-sections are $1.5 \times 10^{-14} \text{ cm}^2$ and $9 \times 10^{-17} \text{ cm}^2$, for holes and electrons, respectively [14]. In this case, Eq. 2.71b would be more appropriate than 2.71a for calculating the generation lifetime. In both cases, the generation lifetime is inversely proportional to the number of generation centres, and, as would be expected, the leakage current is proportional to this density.

However, if the only deep level centres are off mid-gap by more than a few kT , then, for those in the upper half of the band gap, $e_n \gg e_p$ (and $e_n \ll e_p$ if they are in the lower half). Taking, for example, a centre in the upper half of the band-gap, Eq. 2.66 reduces to:

$$J_R = qWN_T e_p \quad (2.72)$$

and the leakage current is limited by just the smaller of the two emission rate constants (in this case e_p), because, once the hole has been emitted, the following step of electron emission is so much faster that it has a negligible impact upon the overall two stage emission process. Expanding e_p :

$$J_R = qWN_T \sigma_p v_{th} n_i \exp -(E_T - E_i)/kT \quad (2.73)$$

$$\therefore \tau_g = 1/N_T \sigma_p v_{th} \exp -(E_T - E_i)/kT = 1/N_{T(\text{eff})} \sigma_p v_{th} \quad (2.74)$$

$N_{T(\text{eff})} = N_T \exp -(E_T - E_i)/kT$, and is the equivalent number of mid-gap centres, which would give the same leakage current. Hence, the shift in position of a generation centre from mid-gap increases the generation lifetime by $\exp(E_T - E_i)/kT$, and decreases the leakage current by the same amount.

In summary, the reverse bias p-n junction leakage current is characterised by the generation lifetime, τ_g , which is related to the physical characteristics of the deep level generation centres themselves.

The other contribution to junction leakage current is the flow of minority carriers, into the reverse biased space region, from the adjacent neutral material. In an n^+p junction, this will be electrons from the p-type substrate, and those adjacent to the space charge region will be swept through it, and into the n^+ -region. This leaves a deficit of electrons at the depletion region edge, which establishes a local minority carrier concentration profile, thereby, driving a *diffusion current*, J_{diffn} . As the ohmic contact to the p-type substrate cannot readily supply electrons, they need to be generated within the material by thermal generation, and the diffusion current is determined by the generation lifetime, and is given by [4]:

$$J_{diffn} = qn_p \sqrt{D_n/\tau_g} \quad (2.75)$$

Where n_p is the equilibrium electron concentration in the p-type substrate ($=p_0/n_i^2$), and D_n is the electron diffusion coefficient ($=kT\mu_n/q$). A significant difference between the diffusion current and the generation current (Eq. 2.70) is that the diffusion current is not a function of the reverse bias voltage.

The treatment in this section has been limited to basic thermal emission processes, and these are directly used in the discussion of TFT leakage currents in Sect. 8.4. In Sect. 8.5.3, the treatment is extended to include field-enhanced emission processes.

2.3.4 Recombination Processes

Recombination will occur in response to a steady state carrier injection process (such as above band-gap optical illumination), where the injection results in an increase of the free carrier concentration above the thermal equilibrium values. The steady state carrier concentrations are given by the equality:

$$R_{inj} = R_R \quad (2.76)$$

Where R_{inj} is the injection rate, and R_R is the recombination rate given by Eq. 2.60 (or the equivalent Eqs. 2.61 and 2.62). As with the generation process, it is useful to simplify these equations to more physically meaningful forms. For charge neutrality, the injection process will result in an equality of the change in trap occupancy, and in the steady state excess densities of both holes and electrons, given by Δp and Δn , respectively. Where $p = p_0 + \Delta p$, and $n = n_0 + \Delta n$, and p_0 and n_0 are the thermal equilibrium carrier densities, and $n_0 p_0 = n_i^2$.

As with the discussion in the preceding sections, an n-type substrate is assumed, and, depending upon the relative values of Δp and n_0 , two different injection conditions are identified. When $\Delta p \ll n_0$, this is regarded as *low-level injection*, and when $\Delta p \geq n_0$ this is defined as *high-level injection*.

2.3.4.1 Low-Level Injection

Consider an n-type substrate, with low-level injection, meaning that $\Delta p \ll n_0$, so that $n \sim n_0$. The *low-level recombination lifetime*, τ_R , is defined by:

$$R_R \equiv \Delta p / \tau_R \quad (2.77)$$

An examination of the physical recombination process will illustrate how Eq. 2.60 can be simplified to yield a more tractable expression for the recombination lifetime. Under low-level injection, the change in the free electron concentration is so small that the equilibrium Fermi level can still be used to describe the electron concentration. Hence, all trap levels beneath the Fermi level are filled with electrons, and ready to trap a hole as the first stage in the two-stage recombination process. Having captured a hole, with the rate constant $c_p(p_0 + \Delta p)$, the subsequent electron capture will proceed with the rate constant $c_n n_0$, which, given that $n_0 \gg (p_0 + \Delta p)$, will be a much faster process, and will not rate limit the overall recombination process. The only other consideration is whether the hole could be thermally emitted back into the valence band before the electron capture process has been completed. For the electron capture rate to exceed the hole emission rate, we need $c_n n_0 > e_p$, i.e.:

$$c_n N_C \exp -(E_C - E_F) / kT > c_p N_V \exp -E_T / kT \quad (2.78)$$

$$\text{i.e. } E_T > (E_C - E_F) + kT \ln(c_p N_V / c_n N_C) \quad (2.79)$$

Taking the logarithmic term in Eq. 2.79 to be smaller than $E_C - E_F$, Eq. 2.79 simply shows that, for efficient electron capture, the trap level must be further from the valence band edge than the Fermi level is from the conduction band edge. In other words, providing the trap level, E_T , is positioned somewhere between the Fermi level and an equivalent distance from the valence band edge, the recombination process will be limited just by hole capture. Replacing n and p in Eq. 2.62:

$$R_R = \frac{-\sigma_n \sigma_p v_{th}^2 N_T n_0 \Delta p}{c_n n_0 + e_n + c_p (p_0 + \Delta p) + e_p} \quad (2.80)$$

From the above discussion, for $E_F > E_T > E_C - E_F$, then $c_n n_0 > e_n$, e_p , and $c_p(p_0 + \Delta p)$, and Eq. 2.80 reduces to:

$$R_R = -\sigma_p v_{th} N_T \Delta p \equiv \Delta p / \tau_R \quad (2.81)$$

$$\text{and } \tau_R = 1 / \sigma_p v_{th} N_T \quad (2.82)$$

In other words, the recombination lifetime is a function of the trap state density, N_T , and the hole capture cross-section, and is independent of the trap energy level over a substantial fraction of the band gap (as defined above). Equation 2.82 is similar to the generation lifetime for a mid-gap generation centre (Eq. 2.71), but, in contrast to the recombination lifetime, once E_T is more than a few kT from mid-

gap, the generation lifetime increases substantially (as shown by Eq. 2.74). Therefore, except in the special case of a mid-gap centre, the steady state generation and recombination lifetimes can be substantially different.

When E_T lies outside the range prescribed for Eq. 2.81, the recombination lifetime will increase. If $E_T > E_F$, then the traps will be largely empty of electrons, and the number of traps available for hole capture will be low. In this situation, $e_n > c_n n_0$, and Eq. 2.80 becomes:

$$R_R \approx \frac{-\sigma_n \sigma_p v_{th}^2 N_T n_0 \Delta p}{e_n} = -\sigma_p v_{th} N_T \Delta p \exp(E_F - E_T)/kT \quad (2.83)$$

$$\text{and } \tau_R = \exp\{(E_T - E_F)/kT\} / \sigma_p v_{th} N_T \quad (\text{for } E_T > E_F) \quad (2.84)$$

Hence, as E_T rises above E_F , the lifetime is larger than that given by Eq. 2.82, and it increases exponentially with increasing values of E_T .

Similarly, if the separation of E_T from the valence band edge is smaller than the value of $(E_C - E_F)$, then e_p will exceed $c_n n_0$, and, from Eq. 2.80, the recombination lifetime will be:

$$\tau_R = \frac{N_V \exp(E_C - E_F - E_T)/kT}{N_C \sigma_n v_{th} N_T} \quad (\text{for } E_T \leq E_C - E_F) \quad (2.85)$$

In other words, as the trap level gets closer to the valence band edge, and E_T reduces, the lifetime exponentially increases, but is now controlled by the capture cross section for electrons, rather than for holes, as it has been in the previous cases.

2.3.4.2 High-Level Injection

As with low-level injection, the recombination process is described by the general Eq. 2.60 (or its equivalents), and to reduce these to a simpler form, the high-level injection situation of $\Delta p \gg n_0$ is considered. In this case, if $\Delta p \gg N_T$, then charge neutrality will be determined just by equality in the excess free carrier densities, i.e. $n = p = \Delta p = \Delta n$, and the equilibrium Fermi level splits into separate quasi-Fermi levels, E_{Fp} and E_{Fn} , for holes and electrons, respectively, where the quasi-Fermi levels are given by:

$$p = N_V \exp - E_{Fp}/kT \quad \text{and} \quad n = N_C \exp - (E_C - E_{Fn})/kT \quad (2.86)$$

If the recombination centre is sited between the quasi-Fermi levels, such that $E_{Fp} < E_T < E_{Fn}$, then $nc_n > e_n$ and $pc_p > e_p$, and the steady state recombination centre occupancy can be obtained from Eq. 2.58:

$$N_T^0 = \frac{N_T \sigma_p}{\sigma_n + \sigma_p} \equiv N_T (1 - F_D) \quad (2.87)$$

F_D is the centre's Fermi-Dirac function, given by Eq. 2.46, in which the equilibrium Fermi level, E_F , is replaced by the quasi-Fermi level for the recombination centre, E_{FT} . For the special case of equal capture cross sections, $F_D = 0.5$, and the quasi-Fermi level for the recombination centre is located at E_T .

For the recombination centre located between the hole and electron quasi-Fermi levels, the recombination lifetime, τ_R , can be calculated from Eqs. 2.60 and 2.77:

$$R_R = \frac{N_T(e_n e_p - n p c_n c_p)}{n c_n + p c_p + e_n + e_p} \approx -\frac{N_T \Delta p^2 c_n c_p}{\Delta p c_n + \Delta p c_p} \equiv \frac{\Delta p}{\tau_R} \quad (2.88)$$

and

$$\tau_R = 1/\sigma_p v_{th} N_T + 1/\sigma_n v_{th} N_T \quad (2.89)$$

Hence, the difference between the low-injection and high-injection lifetimes is that, at high-injection, the lifetime explicitly accounts for the two-stage electron and hole capture process, and the lifetime is correspondingly longer. This is due to the equal densities of holes and electrons. In contrast, the low-injection lifetime was determined just by hole capture, due to the more rapid electron capture process resulting from the much higher majority carrier density of electrons.⁶

As with low-level injection, once the recombination level is outside the energy interval bracketed by the carrier quasi-Fermi levels, the lifetime will increase exponentially with this separation.

2.4 Current Flow Equations

The purpose of this section is to introduce the concepts underlying the modelling of current flow in semiconductor devices, so that the reader has an appreciation of the equations used in device simulation packages. As explained in the introduction, the numerical techniques used to solve these equations are beyond the scope of this book, and further information on device simulation can be found in Refs. [2] and [3].

To establish the basic equations, one-dimensional flow will be considered initially, and then extended to show the form used in 2-D or 3-D simulation programmes.

For current flow by carrier drift and diffusion, the total current density, J_T , is given by the sum of the electron, J_n , and hole, J_p , drift/diffusion currents [1]:

$$J_T = J_n + J_p \quad (2.90)$$

⁶ The situation described in Sects. 2.3.4.1 and 2.3.4.2 is for n-type substrates, and, for injection into p-type substrates, the low-level lifetime will be determined by electron capture.

$$J_n = q\mu_n nF + qD_n \frac{\partial n}{\partial x} \quad (2.91)$$

$$J_p = q\mu_p pF - qD_p \frac{\partial p}{\partial x} \quad (2.92)$$

Where F is the field, μ is the carrier mobility, n and p are the free carrier densities, and D is the diffusion coefficient. These are essentially low field equations, because, as discussed below, at high fields, carrier velocity saturation can occur [15], requiring the μF product to be replaced by the appropriate high field velocity. In Eqs. 2.91 and 2.92, the first term describes the flow of carriers under the influence of an internal field, which would result from an externally applied bias, and the second term is the carrier flow by diffusion resulting from a non-uniform carrier distribution.

The continuity equation links these equations to local generation and recombination processes by:

$$\frac{\partial n}{\partial t} = G_n - R_{GR} + \frac{\partial J_n}{q\partial x} \quad (2.93)$$

$$\frac{\partial p}{\partial t} = G_p - R_{GR} - \frac{\partial J_p}{q\partial x} \quad (2.94)$$

These equations show that the local rate of change of carrier concentration, within a given volume of material, is determined by the difference in the external carrier generation rate, G , and the internal recombination rate, R_{GR} , plus the difference in the carrier flow into and out of the volume. In *steady state*, the local carrier concentrations are constant, and Eqs. 2.93 and 2.94 are equal to zero. The internal recombination/generation rate, R_{GR} , is given by Eq. 2.60 from Sect. 2.3.2, and the external generation rate, G , could be due to optical absorption of above band-gap light. In this case, the local optical generation rate, G_O is:

$$G_o(z) = \alpha\Phi(1 - R) \exp -\alpha z \quad (2.95)$$

Where α is the optical absorption coefficient, Φ is the incident photon flux, R is the surface reflectivity, and z is the distance in the material perpendicular to the illuminated surface.⁷

Another potential source of carrier generation is high-field generation of electron-hole pairs by impact ionisation. This is also referred to as avalanche generation, since the generated carriers will also be accelerated by the field, and produce further carriers by impact ionisation themselves. This is most likely to occur with high carrier mobility semiconductors, and in high field regions of devices, such as reverse biased junctions. Where the carrier mobility is low, due to short mean free paths and efficient scattering, the carrier is unlikely to gain enough energy from the field. However, where the mean free path is large, the carriers can

⁷ For a 1-D treatment, we require $\alpha < z$ for uniform carrier generation.

be efficiently accelerated and heated by the field. If the carriers attain sufficient energy, then lattice collisions can lead to electron-hole pair generation. The impact ionisation generation rate, G_{II} , is given by [1]:

$$G_{II} = nv_n\alpha_n + pv_p\alpha_p \quad (2.96)$$

Where v_n (v_p) is the electron (hole) drift velocity, α_n (α_p) is the electron (hole) ionisation coefficient, and:

$$\alpha_{n,p} = \frac{qF}{E_I} \exp -\frac{F_C}{F} \quad (2.97)$$

F_C is the critical field, F is the field parallel to current flow, and E_I is the carrier ionisation energy (for Si this is 3.6 eV for electrons and 5.0 eV for holes). A simpler expression [16] has also been used in simulations of TFTs [17], where the ionisation coefficient is:

$$\alpha_{n,p} = \alpha_{n,p}^{\infty} \exp -\frac{F_C}{F} \quad (2.98)$$

and α^{∞} is a constant, which is determined, together with F_C , from simulation fits.

The carrier velocity, in Eq. 2.96, at low fields, is given by $\mu_0 F$, where μ_0 is the low field mobility. At high fields, velocity saturation occurs, and the following relationship between velocity and field was found to provide a good fit to the experimental c-Si data shown in Fig. 2.15 [15]:

$$v_{n,p} = \frac{\mu_0 F}{\left[1 + (\mu_0 F/v_S)^{\beta}\right]^{1/\beta}} \quad (2.99)$$

Where v_S is the saturated velocity ($\sim 10^7$ cm/s for holes and electrons in Si), and β is a constant (~ 2 for electrons and ~ 1 for holes in Si).

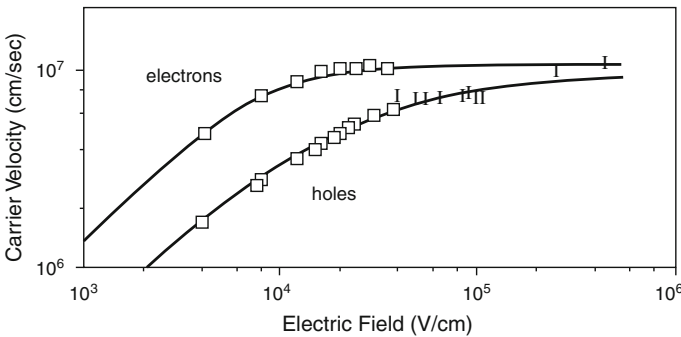


Fig. 2.15 Carrier velocity measurements as a function of the electric field in silicon. The *solid line* is the empirical fit to Eq. 2.99 (Reprinted from [15] with permission of IEEE)

Equations 2.90–2.94 contain the electrostatic field, F , which is the local gradient of the potential, dV/dx , and this has to be established in a self-consistent fashion by the simultaneous solution of Poisson's equation:

$$\frac{d^2V}{dx^2} = -\frac{q\rho(x)}{\epsilon_0\epsilon_s} \quad (2.100)$$

$$\text{and } \rho = p - n + N_d - N_a + N_{Td}^+ - N_{Ta}^- \quad (2.101)$$

where N_d and N_a are shallow donor and acceptor dopants, and N_{Ta} and N_{Td} are deep acceptor and donor defects, respectively. For a TFT, the deep levels could equally well refer to a distribution of defect levels across the band-gap.

The above equations have been presented, for simplicity, in a 1-D format, but, for accurate device simulation, these equations need to be solved in two or three dimensions. In that case, the coupled equations in steady state are [18]:

$$\begin{aligned} \nabla \cdot \nabla V &= -q\rho/\epsilon_0\epsilon_s \\ \nabla \cdot J_n &= -q(G_n - R_{GR}) \\ \nabla \cdot J_p &= q(G_p - R_{GR}) \\ J_n &= -qn\mu_n\nabla V + qD_n\nabla n \\ J_p &= -qp\mu_p\nabla V - qD_p\nabla p \end{aligned} \quad (2.102)$$

These are solved subject to a set of boundary conditions determined by the biases applied to the device terminals, the field continuity conditions across internal material boundaries (such as the semiconductor/dielectric interface), and the conditions at the external boundaries of the device, where, for instance, the field may be clamped at zero.

In the commercial simulators used for Si-based TFTs, the internal recombination/generation rate, R_{GR} , includes additional processes to those considered in Sect. 2.3. In particular, the treatment of carrier emission is extended to include field-enhanced emission processes from traps, as well as band-to-band tunnelling. Those mechanisms are discussed further in Sect. 8.5.3.

2.5 Summary

Some analytical device physics concepts, using single crystal equations, have been introduced as a background topic to later chapters. These simple concepts are widely used in interpreting TFT behaviour, and they provide a solid basis for appreciating the assumptions and approximations used in that work.

The topics in this chapter have been restricted to those of most relevance to TFTs, and have focussed, firstly, on aspects of semiconductor surface physics,

which describe the relationship between gate bias, surface space charge, and band bending in MIS structures. This topic underpins the understanding of IGFET behaviour, which will be the subject of [Chap. 3](#). The second topic is electron-hole pair recombination and generation processes through deep level centres in the forbidden band gap. These processes play a role in establishing steady-state carrier concentrations under injection processes, and determine reverse bias leakage currents from junction depletion regions. Finally, there is a brief overview of the current flow processes, which are incorporated in device simulation packages.

Appendix: Summary of Key Equations

A number of the simplified equations from the text, which can be used in basic analytical calculations, are reproduced below. The equation numbers are retained for quick reference back to the original derivations.

A.1 Semiconductor Surface Band Bending

Relationships between surface potential, V_s , space charge density, Q_s , gate voltage, V_G , and threshold voltage, V_T .

(a) Depletion and Inversion Space Charge Density

$$Q_s \cong -\sqrt{2q\epsilon_0\epsilon_s} \left[n_i \frac{kT}{q} \exp \frac{q(V_s - V_F)}{kT} + N_a V_s \right]^{0.5} \quad (2.12)$$

(b) Depletion Space Charge Density

$$Q_s \cong -\sqrt{2q\epsilon_0\epsilon_s N_a V_s} \quad (2.13)$$

(c) Gate Voltage, Surface Potential and Space Charge Density

$$V_G = V_s - Q_s/C_i \quad (2.22)$$

(d) Gate Threshold Voltage

$$V_T = V_{FB} + \frac{\sqrt{2q\epsilon_0\epsilon_s N_a 2V_F}}{C_i} + 2V_F \quad (2.28)$$

and, from [Eq. 2.5](#), $V_F = (kT/q)\ln(N_a/n_i)$

(e) Depletion Layer Thickness at Inversion

$$x_{d\max} = \sqrt{\frac{2\epsilon_0\epsilon_s 2V_F}{qN_a}} \quad (2.18)$$

(f) Flat-Band Voltage

$$V_{\text{FB}} = \Phi_{\text{MS}} - Q_{\text{ieff}}/C_i - Q_{\text{ss}}/C_i$$

A.2 Carrier Recombination and Generation

Relationships between trap density, N_T , and capture cross section, σ , and the carrier generation/recombination rates.

(a) General Recombination and Generation Rate Expression

$$R_{GR} = \frac{\sigma v_{th} N_T [n_i^2 - np]}{n + p + 2n_i \cosh(E_T - E_i) kT} \quad (2.63)$$

(b) Generation Leakage Current

$$J_R \equiv qn_i W / \tau_g \quad (2.70)$$

(c) Generation Lifetime, τ_g

$$\tau_g = 1 / (0.5 N_T \sigma v_{th}) \quad (2.71a)$$

(d) Carrier Recombination Rate, and Recombination Lifetime, τ_R

$$R_R = -\sigma_p v_{th} N_T \Delta p \equiv \Delta p / \tau_R \quad (2.81)$$

(e) Recombination Lifetime (Low Injection Level)

$$\tau_R = 1 / \sigma_p v_{th} N_T \quad (2.82)$$

(f) Recombination Lifetime (High Injection Level)

$$\tau_R = 1 / \sigma_p v_{th} N_T + 1 / \sigma_n v_{th} N_T \quad (2.89)$$

References

1. Sze SM, Ng KK (2007) *Physics of semiconductor devices*, 3rd edn. Wiley, New York
2. <http://www.iue.tuwien.ac.at/phd/klima/node8.html> (Accessed Aug 2010)
3. http://www.silvaco.com/products/vwf/atlas/2D/tft/tft_03.pdf (Accessed Aug 2010)
4. Grove AS (1967) *Physics and technology of semiconductor devices*. Wiley, New York, pp 278–285
5. Deal BE, Snow EH, Mead CA (1966) Barrier energies in metal–silicon dioxide–silicon structures. *J Phys Chem Solids* 27(11–12):1873–1879
6. Brotherton SD, Gill A (1978) Determination of surface and bulk generation currents in low leakage silicon MOS structures. *Appl Phys Letts* 33:890–892
7. Berglund CN (1966) Surface states at steam-grown silicon–silicon dioxide interface. *IEEE Trans Electron Dev* 13(10):701–705
8. Castagne R, Vapaille A (1971) Description of the SiO₂–Si interface properties by means of very low frequency MOS capacitance measurements. *Surf Sci* 28(1):157–193
9. Nicollian EH, Goetzberger A (1967) The Si–SiO₂ interface—electrical properties as determined by the MIS conductance technique. *Bell Syst Tech J* 46:1055
10. Hall RN (1952) Electron-hole recombination in germanium. *Phys Rev* 87(2):387
11. Shockley W, Read WT (1952) Statistics of the recombination of holes and electrons. *Phys Rev* 87(5):835–842
12. Sah CT, Noyce RN, Shockley W (1957) Carrier generation and recombination in p–n junction and p–n junction characteristics. *Proc IRE* 45(9):1228–1243
13. Lax M (1960) Cascade capture of electrons in solids. *Phys Rev* 119(5):1502–1523
14. Brotherton SD, Bradley P (1982) Measurement of minority carrier capture cross sections and application to gold and platinum in silicon. *J Appl Phys* 53(3):1543–1553
15. Caughy DM, Thomas RE (1967) Carrier mobilities in silicon empirically related to doping and field. *Proc IEEE* 55:2192–2193
16. Chynoweth AG (1958) Ionisation rates for holes and electrons in silicon. *Phys Rev* 109(5):1537–1540
17. Valletta A, Gaucci P, Mariucci L, Pecora A, Cuscutà M, Maiolo L, Fortunato G (2010) Threshold voltage in short channel polycrystalline silicon thin film transistors: Influence of drain induced barrier lowering and floating body effects. *J Appl Phys* 107:074505-1–074505-9
18. Guerrieri G, Ciampolini P, Gnudi A, Rudan M, Bacarani G (1986) Numerical simulation of polycrystalline-silicon MOSFETs. *IEEE Trans ED-33*(8):1201–1206