Chapter 11
TFTs on Flexible Substrates

Abstract The flat panel display industry has been built around TFTs on rigid glass substrates, but there are well-identified applications requiring flexible substrates. This chapter summarises the properties of common plastic substrate materials, and discusses the issues of implementing TFT fabrication schedules on them. It looks in detail at the strategies which have been developed in order to fabricate a-Si:H, poly-Si and organic TFTs on flexible substrates. These have included direct fabrication on the plastic substrates at reduced temperatures, as well as carrier plate and transfer plate processing. For carrier plate processing, the plastic substrates are temporarily bonded to glass carrier plates during processing, and, at its completion, the plastic substrate, plus its TFT layers, are detached from the glass. For the transfer process, the TFT layers themselves are detached from the glass, and bonded to a separate plastic substrate. A third approach has been to use an alternative flexible substrate, which is easier to handle, such as thin foils of stainless steel. In addition to these technological considerations, the mechanics of bending and strain in flexible substrates is summarised.

11.1 Introduction

Chapter 5 has discussed the processing of a-Si:H TFTs on glass substrates, and this is the current, dominant active matrix display technology, irrespective of whether it is for LCD, or electrophoretic e-reader displays. However, there are obvious mechanical limitations in displays made on glass, namely their rigidity and potential fragility. This is particularly true of small portable displays, where mechanical robustness is essential, and, for many of these displays, it is also desirable to minimise their weight and size. The weight reduction may be achieved through the use of thinner, lower density substrates, such as plastic, and the robustness and reduced size can be achieved with increased substrate flexibility, so

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that, for instance, the display may be rolled or folded, when not in use. There are also other applications where the display needs to be conformable to fit, for instance, the contours of a car's dashboard, or to be contoured to be worn on a wrist. These requirements can, in principle, be met with flexible substrates, providing these substrates can be used to make displays, which match the quality of the glass-based displays, and, ideally, at the same or at a reduced cost.

The same arguments can also be applied to poly-Si TFTs, particularly as their major application is in small/medium diagonal portable displays, including both AMLCDs and AMOLEDs, where the need for reduced weight, flexibility and robustness is greatest.

In view of the enormous investment in a-Si:H TFT technology, and its widespread application as the dominant active matrix display technology, it is understandable that there are strong technical and economic reasons to extend this technology, where possible, to new applications. Equally, these arguments can be applied to poly-Si technology, as it currently commands a large fraction of the small diagonal, portable display market. However, as shown in the following sections, the application of the relatively high temperature glass-based processes, to lower temperature plastic substrates, presents many challenges, which are less severe with organic TFTs. Nevertheless, the greater background understanding of the inorganic TFT technologies means that many of today's more sophisticated demonstrator displays and circuits, on flexible substrates, have been made using these devices. Hence, the emphasis in this chapter is on the implementation of these technologies on plastic substrates, with a briefer overview of the work on organic TFTs.

In this chapter, the properties and handling issues of plastic substrates are covered, before looking in detail at the implementation of a-Si:H, poly-Si and organic TFT technologies on flexible substrates. In addition, the impact of substrate flexing on the electrical performance of these TFTs is presented.

To a large extent, the current technological developments have been an extension of the glass-based technology to flexible substrates, and many of the more successful processes have used a hybrid glass/plastic approach in delivering a final plastic-based demonstrator. However, for future low-cost fabrication of flexible devices [1] it is likely that quite different processing technologies will be required, particularly where they can exploit the unique features of flexible substrates, such as roll-to-roll (R2R) processing [1–3]. Whilst aspects of R2R have been demonstrated with a-Si:H TFTs [2], it is better suited to a solution-based organic TFT technology, as this is more compatible with an all-printed process [4]. However, the implementation of an all-printed R2R technology still presents many challenges.

Section 11.2 summarises the properties of the commonly used plastic substrates, and gives an overview of the issues associated with handling them. Section 11.3 discusses the effects of strain on the deposited thin films when the flexible substrate is bent. The strategies for processing a-Si:H, poly-Si and organic TFTs on flexible substrates are described in Sects. 11.4, 11.5, and 11.6, respectively. These sections also summarise the effects of uniaxial strain on the device

characteristics. Finally, the issues of power dissipation in the TFT, leading to its self-heating, and to the subsequent heating of the plastic substrate, are briefly reviewed in Sect. 11.7.

11.2 Substrate Handling

In terms of flexibility and material cost, plastic substrates look very attractive, and have been the subject of considerable research, which has identified and addressed many of the problems involved in shifting from glass to plastic substrates. Some of the issues are related to the differences in thermal and mechanical properties between TFT materials, glass and plastics, and these are summarised in Table 11.1. This table lists key properties of many of the most widely studied plastics, and the corresponding values are also listed for the TFT materials, as well as for glass and steel foil substrates. The plastics are polyimide (PI), aromatic fluorine-containing polyarylates (PAR), polyethersulphone (PES), polyethylene naphthalate (PEN), and polyethylene terephthalate (PET) [5]. The second column lists the maximum processing temperatures for these materials, where the glass transition temperature has been used for the plastics [5], and it will be seen that, for most of the plastics, the maximum permitted processing temperature is well below that for glass substrates. This has the direct consequence that the a-Si :H and poly-Si TFT processing schedules, developed for glass substrates, cannot be directly implemented on plastic substrates, and, therefore, new lower temperature schedules were needed. The two possible exceptions to this are PI and PAR; however, PI is not transparent, and would not be suitable for a back-lit AMLCD display. Nevertheless, it could be used with reflective or emissive displays, and PI substrates are currently used in the development of flexible reflective LC, top-emitting AMOLED and electrophoretic e-reader displays. The issue with PAR is its

Table 11.1 Properties of TFT substrates and layers (*—Glass strain temperature; HS—heat stabilised; many of the figures are illustrative, and will show some variation with substrate preparation technique)

Material	Tmax (°C)	CTE, α (ppm/K)	Y (GPa)	ν	Transparency (%)	WVTR ($g.m^{-2}day^{-1}$)
Glass	666*	3.2	71	0.23	90	0
PI (Kapton)	350	17	2.5	0.32	30–60 (yellow)	
PAR	340	53	2.9		90	
PES	223	54	2.2		90	80
PEN (HS)	150 (200)	13	6.1		>85	2
PET (HS)	80 (150)	15	5.3		>85	9
Steel	>1,000	14	200		0	0
SiN	>1,000	2.7	210	0.25		0
SiO2	>1,000	0.5	70			0
Si	>1,000	2.6	130	0.28		0

coefficient of thermal expansion, CTE, and this general issue is discussed in the next paragraph.

The third column in the table lists the coefficients of thermal expansion, α, and, for the plastics, these are all much larger than the values for glass and for the inorganic TFT materials. Following the deposition of a TFT layer at a temperature ΔT above room temperature, this mismatch between the CTEs of the TFT layers and the plastic substrates will induce room temperature strain, e_M, in the system, given by [6]:

$$e_M = (\alpha_f - \alpha_s)\Delta T \tag{11.1}$$

where the sub-scripts 's' and 'f' refer to the parameter values for the substrate and TFT film, respectively.

The strain in the TFT layers is given by [7]:

$$\varepsilon_f = \left(\frac{(\alpha_f - \alpha_s)\Delta T}{Y_f d_f / Y_s d_s + 1} \right) \tag{11.2}$$

(where Y is Young's modulus, and positive values of ε_f correspond to tensile strain in the film, and negative values to compressive strain). Unless $Y_s d_s \gg Y_f d_f$, the denominator is larger than unity, and the strain in the system is not concentrated just in the TFT film, but is shared with the substrate as well. This is typical for a compliant substrate with a small value of Y_s. So, for the deposition of a thin SiN layer on one side of a plastic substrate, given the CTE differences in Table 11.1, at room temperature the substrate will be constrained from shrinking as much as a free substrate would, and it will be under tensile stress, while the SiN film will be shrunk more than a free film, and it will be under compressive stress. These CTE-induced stresses will cause the structure to distort into a cylindrical shape, with the compressive film on the outer surface of the cylinder. (In contrast, with mechanically induced stress, where the structure is wrapped around a cylinder, the outer surface will be under tension). The detailed relationship between process-induced strain and the radius of the resulting cylinder is discussed further below.

For a rigid substrate, such as glass, with $Y_s d_s > Y_f d_f$, the strain is largely contained within the TFT film, and equation (11.2) reduces to:

$$\varepsilon_f = (\alpha_f - \alpha_s)\Delta T \tag{11.3}$$

The strain in equations (11.2) or (11.3) will have two possible consequences. Firstly, if the strain in the film is too high it will crack, and a rule of thumb, suggesting that the strain should be kept below 0.3 %, can further limit ΔT, and, thereby, limit the maximum processing temperature [8]. This is shown in Fig. 11.1, in which the maximum thickness of silicon nitride, before it cracks, is plotted against the nitride deposition temperature for two engineered, 300 °C plastics having CTE values of 45 ppm/K and < 10 ppm/K. As will be seen, the maximum nitride thickness, at a deposition temperature of 250 °C, was only 200 nm for the nitride on the high CTE substrate [9]. As this may be thinner than

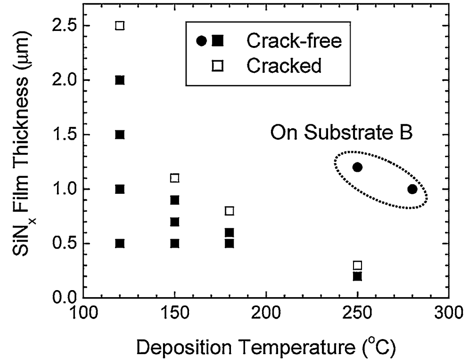

Fig. 11.1 Thickness of cracked (*square*) and crack-free (*filled square*) SiNx films deposited over a range of temperatures on engineered polymer substrates (CTE = 45 ppm/K, and <10 ppm/K for film B). (Reprinted from [9] with permission of SID)

needed for either substrate capping or for the gate insulator layer, the maximum processing temperature must be kept below this temperature if thicker films are required. PAR, with a CTE of 53 ppm/K, will be similarly constrained, and using the rule of thumb of 0.3 % maximum strain, it was recommended that the maximum processing temperature should be kept below 220 °C, which is significantly lower than its glass transition temperature of 340 °C [10].

As mentioned above, with a compliant plastic substrate, having a small Young's modulus compared with the thin film's value, the substrate will buckle into a cylindrical shape, with a radius of curvature, R, given by [6]:

$$R = \left[\frac{d_s}{6(1+v)e_M\kappa\eta}\right]\left[\frac{(1-\kappa\eta^2)^2 + 4\kappa\eta(1+\eta)^2}{1+\eta}\right] \tag{11.4}$$

where, $\eta = {}^{d_f}\!/_{d_s}, \kappa = {}^{Y_f}\!/_{Y_s}$ and d and Y are the thickness and Young's modulus values, respectively, of the thin film and the substrate, and v is Poisson's ratio (which is assumed to be the same for the film and the substrate). For a rigid substrate, such as glass, where $Y_f \approx Y_s$, and for $\eta < 0.1$, the above equation simplifies to the Stoney formula, giving spherical rather than cylindrical distortion [6]:

$$R = \left[\frac{d_s}{6e_M\kappa\eta}\right] \tag{11.5}$$

The normalised radius of curvature is plotted against the ratio of film thickness to substrate thickness in Fig. 11.2, for the two situations of a compliant substrate ($\kappa = 100$), and a closely matched film and substrate ($\kappa = 1$) [6]. (These two cases were chosen to represent a TFT film on plastic or on a steel substrate, respectively. As will be seen below, the use of thin steel foils is one strategy chosen for the fabrication of TFTs on flexible substrates [6]). Figure 11.2 shows that for a typical case of 1 μm thick TFT layers on 100 μm thick flexible substrates, the plastic substrate develops more than ten times greater curvature than the steel substrate. Also, if the $\kappa = 1$ curve is used as an approximate description of a 1 μm thick TFT

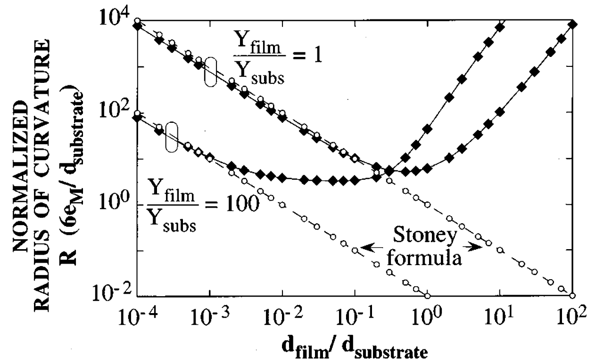

Fig. 11.2 Normalized radius of curvature calculated as a function of the film/substrate thickness ratio, using eqs. (11.4) (solid lines) and (11.5) (broken lines). (Reprinted with permission from [6]. Copyright (1999) American Institute of Physics)

layer on 500 μm thick glass substrate, the curvature of the thinner plastic substrate is ~100 times greater. The curvature in the plastic substrates will need to be handled during processing either by bonding the substrates to a rigid carrier or by using frames to flatten them [10]; either way, this will add extra complication to the processing schedule. Whilst the curvature can be minimised by coating identical capping layers on both sides of the flexible substrate, and, thereby, equalising the surface strains, it will not be practical, nor cost effective, to duplicate all TFT layers on both sides of the substrate. Hence, there will always be CTE-induced bending strain due, for instance, to the SiN_x gate dielectric layer in the TFT. In addition to the unbalanced CTE strains, there may also be residual bending strains in the as-delivered plastic substrates, as well as built-in strain in the films themselves due to the deposition processes [14], all leading to substrate handling issues due to its curvature.

To reduce the CTE mismatch problem, some proprietary, transparent plastic substrates have been developed, in which the CTE values have been engineered to be a closer match to those of the TFT layers, by being less than 10 ppm/K in one case [9], and ~14 ppm/K in another [11]. The first of these substrates also has a maximum processing temperature of ≥300 °C, so that it is also a better match to standard a-Si:H TFT processing schedules [9].

The final column in Table 11.1 lists the water vapour transmission rates, WVTR, in $g/m^2/day$ for the plastic substrates [11], and the high values present another handling issue. This is because water absorption, as well as oxygen absorption, leads to a swelling of the plastic, which compromises its dimensional stability. For photolithography, good dimensional stability is essential for the correct registration of successive mask patterns. In addition, low WVTR values of 10^{-1}–10^{-2} $g/m^2/day$ are needed for LCDs and considerably lower values are needed for encapsulation of AMOLEDs [11]. This problem can be addressed either through impermeable, hard surface coatings deposited by the substrate manufacturer, or by low temperature deposition of SiN_x and/or SiO_2 layers using either sputtering or PECVD. For instance, a PES film coated with a UV-cured acrylate film plus a sputter deposited SiO_x film reduced its WTVR from ~50 to 0.01 $g/m^2/day$ [11]. The coatings also serve to protect the substrates from the potentially

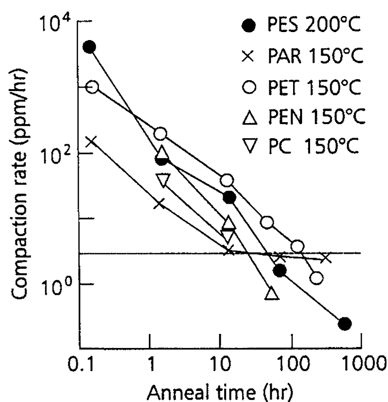

Fig. 11.3 Shrinkage rate measurements of various plastic substrates at 150 or 200 °C. (Reprinted from [12] with permission of SID)

harmful chemicals, which would be used during the device patterning processes. Given the crucial role played by these encapsulation films, they need to be of high quality and pin-hole free.

Finally, the as-delivered plastic films show a tendency to shrink at typical processing temperatures. To maintain dimensional stability throughout the TFT fabrication process, they need to be pre-shrunk, prior to device processing, by annealing them at the intended processing temperature [10, 12]. Shrinkage rate data for many of the common plastics are shown in Fig. 11.3 [12], and this rate parameter can be readily used to match the in-process shrinkage of the film to the required dimensional stability of the substrate. For instance, if a 30 × 30 cm polymer substrate is being processed, and the required alignment tolerance is 3 μm, then the shrinkage of the plate between first and last photolithography stage must be less than 3 μm, or less than 10 ppm. If the total high temperature cycle time after the first lithography stage is 2 h, then the substrate needs to be annealed until its shrinkage rate is <5 ppm/h. From the data in Fig. 11.3, those samples needed to be pre-shrunk for ~10–100 h to achieve this degree of stability.

11.3 Substrate Bending

For displays having an application dependent upon their flexibility, it is important to establish the effect of strain on the performance of the TFT, and, equally, to determine the critical strain at which the device fails. This is usually done by measuring device performance as a function of tensile and compressive strain, by bending the processed substrates around preformed cylinders of defined radius, as shown in Fig. 11.4 [13]. By varying the radius of curvature, R, the strain can be varied, where the relationship between radius and bending-induced strain at the top of the film is given by [6]:

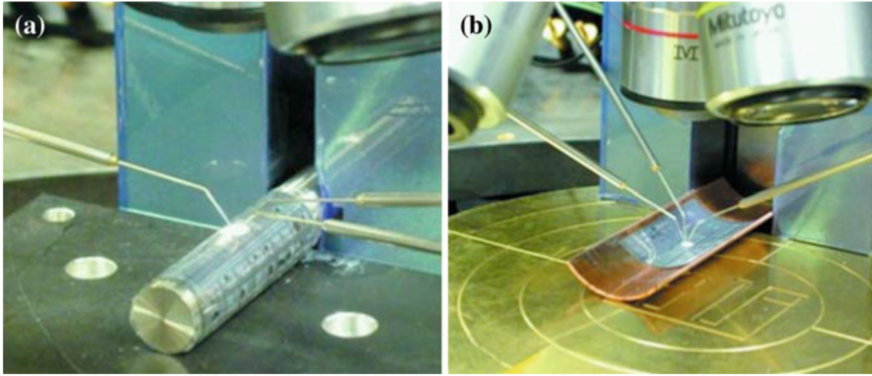

Fig. 11.4 Photographs of steel foils wrapped around cylinders to measure the effects of uniaxial strain on TFT behaviour: (**a**) tensile, and (**b**) compressive strain. (Reprinted with permission from [13]. Copyright (2009) American Institute of Physics)

$$\varepsilon_f = \left(\frac{d_f + d_s}{2R}\right)\left(\frac{1 + 2\eta + \kappa\eta^2}{(1+\eta)(1+\kappa\eta)}\right) \tag{11.6}$$

For externally applied bending strains, if the film is the outer surface of the cylindrical shape it will be under tensile strain.

The normalised surface strain is plotted in Fig. 11.5 as a function of the relative thickness of the film and substrate, for two different ratios of Young's modulus corresponding to well matched elastic properties of the film and substrate ($\kappa = 1$) and compliant ($\kappa = 100$) substrates. For the former, the unity value of the normalised strain corresponds to:

$$\varepsilon_f = \left(\frac{d_f + d_s}{2R}\right) \tag{11.7}$$

and this describes the situation in which the neutral plane is in the centre of the film-substrate bilayer, and the strain in the film increases linearly with the

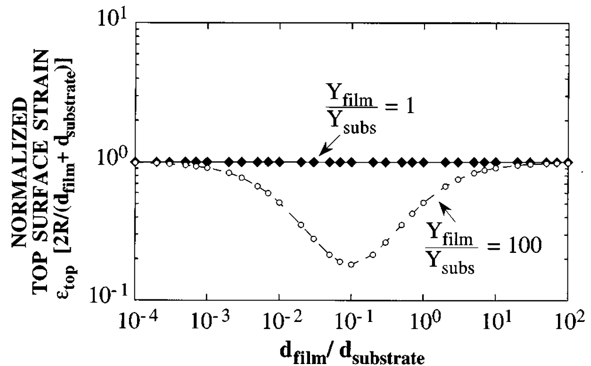

Fig. 11.5 Normalized strain in a film calculated as a function of the film/substrate thickness ratio. Two substrates are illustrated: steel (Yf/Ys ≈ 1) and plastic (Yf/Ys ≈ 100). (Reprinted with permission from [6]. Copyright (1999) American Institute of Physics)

thickness of both materials, and scales inversely with the radius of curvature. This simple situation, of the neutral plane being in the centre of the bilayer, is only approached with the compliant substrate when there is a gross mismatch in the thickness of the film and the substrate, such that $\eta < 10^{-3}$ or $\eta > 10$, and, in these two cases, one material or the other dominates the bending induced strain. For the more typical case of $\eta \sim 10^{-2}$, the neutral plane moves from the centre of the compliant substrate towards the stiffer TFT film, thereby reducing the strain in the film by approximately a factor of two compared with the $\kappa = 1$ case.

From the mechanical stressing of a-Si:H TFTs into tension and compression, the safe strain range for reversible elastic distortion was established, together with the threshold strain beyond which plastic failure occurred. This is shown in Fig. 11.6 [14], and failure under tensile strain occurred at 0.5 % due to crack propagation, whereas, under compressive strain, the failure mode was buckling and de-lamination at the higher strain of 2 %. The failure under tension has been attributed to the propagation of a crack originating at a flaw, where the propagation occurs when the driving force, G, is greater than the surface energy, Γ, of the newly formed crack [15]:

$$G = \beta \frac{(1 - v_f^2)\sigma_f^2 d_f}{Y_f} > \Gamma \tag{11.8}$$

σ_f is the stress in the film, and β is a dimensionless constant dependent upon the elastic properties of the film and substrate, and, for a compliant substrate, β is much larger than one, leading to easy crack propagation [15]. De-lamination occurs when a defective region at the film/substrate interface results in an unbonded area, which is large enough to permit the film to buckle. Once that happens, the internal stresses can propagate the unbonded area like a crack, and the critical unbonded length for buckling, l_c, is given by [15]:

$$l_c = \frac{\pi d_f}{\sqrt{3(1 - v_f^2)}} \left(-\frac{Y_f}{\sigma_f} \right)^{0.5} \tag{11.9}$$

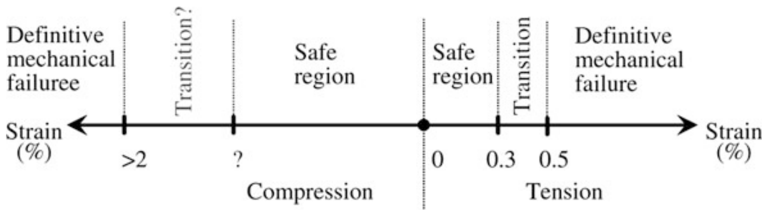

Fig. 11.6 Overview of the response of a-Si:H TFTs to mechanical strain. (Reproduced from [14] with permission of Wiley, Inc)

(where σ_f has a negative value in compression). Given that the compressive failure strain, ε_f, in the film was >2 % [14, 15], the corresponding stress can be determined, giving $l_c < 10d_f \sim 10$ µm. This is an unusually large defective area in a high quality structure, explaining why the films were so stable under compressive strain [15].

Further details of the response of a-Si:H TFTs to mechanical strain are presented in Sect. 11.4.1.1, in which the replacement of the brittle SiN_x by a more resilient hybrid layer of silicon dioxide and silicone polymer (for both substrate capping and the gate dielectric) improved the tensile and compressive failure strains to 5 and 2.5 %, respectively [16].

This discussion has focussed on the direct assessment of strain effects in TFTs on a free-standing polymer substrate. However, in a finished display, the substrate will be attached to another layer to form the display cell. If the elastic properties of this top-plane are a good match to the substrate, the TFT layer would be located near the neutral plane, and would suffer little strain when the whole structure is flexed. Whilst this will be difficult to readily achieve with the inorganic layers used in a-Si:H and poly-Si TFTs, it should be easier to achieve with organic TFTs, and it was shown that the minimum bending radius for pentacene TFTs on PI could be reduced from 5 mm, for the uncoated substrate, to 0.5 mm when it was coated with a thickness-matched parylene capping layer [17].

11.4 a-Si:H TFTs on Flexible Substrates

11.4.1 a-Si:H Fabrication Processes

Given the above discussion on the issues of using and handling the compliant plastic substrates for TFT fabrication, three different strategies have emerged to deal with these problems. The first has been to take the constraints imposed by the plastic substrates, and to develop both lower temperature TFT processing, and substrate handling procedures, in order to implement direct fabrication techniques on these substrates. The second approach is to use an alternative flexible substrate to circumvent the issues with handling plastic substrates, and the material of choice has been polished steel foils. The third strategy has been to maintain as much as possible of the well-established processing techniques used with glass substrates, and, to minimise the handling issues of plastic substrates by bonding them to glass carrier plates during processing, and then separating them from these plates at the end of processing. These three approaches are discussed in the following three sub-sections, and an embryonic, but more innovative, roll-to-roll technology is presented in Sect. 11.4.1.4.

11.4.1.1 Direct Processing on Plastic

In the direct fabrication of a-Si:H TFTs on plastic substrates, the major objectives have been stress control in the films (where the stress arises from both CTE mismatch, as well as intrinsic stress within the film), and optimisation of device performance at the reduced deposition temperatures needed when using the low temperature substrates, such as PES or PEN.

These objectives have been met by modifying the deposition procedures for the a-Si:H and the SiN_x layers. Figure 11.7 shows the variation of strain in SiN_x layers deposited at 150 °C onto 50 μm thick Kapton PI substrates, as a function of deposition power density [18]. In this diagram, the total strain in the film, ε_M, has been split into its constituent components due to CTE mismatch, ε_{th}, intrinsic deposition strain, ε_0, and humidity strain, ε_{ch}. As might be expected, only the intrinsic strain varied with deposition power, and it could be changed from tensile to compressive. Hence, by suitably controlling the deposition power density, the strain can be tuned to the processing requirements of the substrate. The deposition power has also been correlated with the gate bias instability in a-Si:H TFTs [19], in which increasing power density led to improved device stability, and the use of this control procedure is discussed below in the context of a specifically optimised process schedule [8].

As stated above, the deposition power used for the SiN_x layer can affect the gate bias stability of the TFT, and, hence, influences the electronic quality of the layer. The other deposition parameter having an influence upon the quality of the SiN_x layer, as well as upon the a-Si:H layer, is the gas dilution of the reactant gases. The deposition gases are SiH_4 for a-Si:H, and SiH_4 plus NH_3 for SiN_x. For a-Si:H, the electronic quality of the film has been correlated with a high ratio of SiH bonds to SiH_2 bonds, and the SiH bond density can be increased by diluting the SiH_4 with hydrogen [20, 21]. This has been explained mechanistically by arguing that the excess hydrogen acts as an etchant during deposition, and preferentially breaks weak Si–Si bonds to form volatile hydrides. As these weak bonds can form defect states, their removal should increase the quality and improve the bias-stress

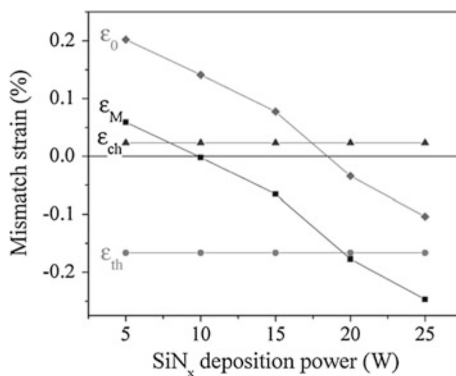

Fig. 11.7 Components of the total mismatch strain, εM, in 300 nm thick PECVD SiNx films deposited at different RF powers onto 50 μm thick Kapton 200E PI substrates at 150 °C. (Reprinted from [18] with permission of SID)

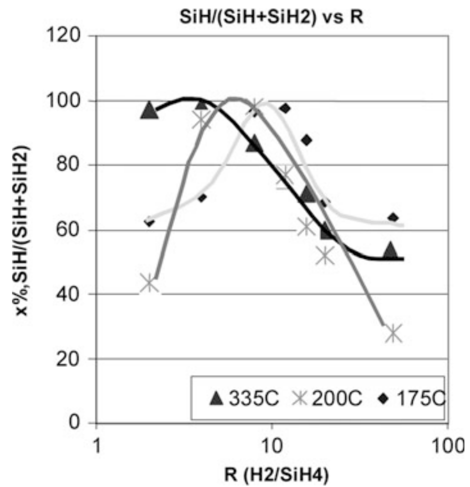

Fig. 11.8 Ratio of SiH:(SiH + SiH2) bond densities in PECVD a-Si:H films, deposited at different temperatures, as a function of the hydrogen dilution of the silane deposition gas. (Reprinted from [21] with permission of SID)

stability of the films [22]. Moreover, as shown by Fig. 11.8, the optimum dilution ratio increased as the deposition temperature reduced [21]; hence, the a-Si:H deposition conditions established for use on glass substrates needed to be re-optimised for use on lower temperature plastic substrates. Similarly, the relative density of NH and SiH bonds needed to be controlled in lower temperature SiN_x films, to prevent the SiN_x becoming either too nitrogen-rich or too silicon-rich, and this was accomplished by dilution of the reactant gases with either hydrogen, helium of argon [21]. An example of this is shown in Fig. 11.9, in which the NH/SiH ratio is plotted as a function of the dilution conditions for the three different carrier gases. Also shown on this figure is the ratio, labelled HT, achieved by conventional SiN_x deposition at 300 °C, and the data point, labelled LT, showing that the ratio was too nitrogen-rich if the same gas composition was used at 200 °C. At this lower temperature, increased gas dilution, with either argon or hydrogen, was needed to restore the film's compositional balance. Suitable

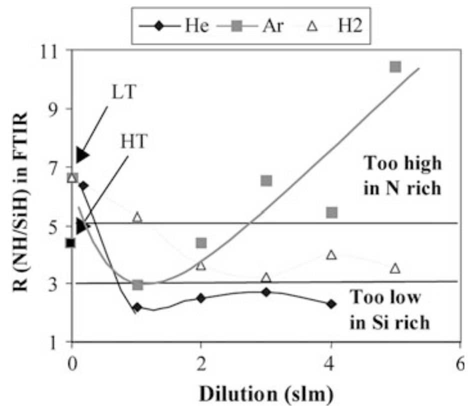

Fig. 11.9 Ratio of NH:SiH bond densities in 200 °C PECVD SiNx films as a function of the dilution of the reactant gases SiH4 and NH3 by He, Ar or H2. (Reprinted from [21] with permission of SID)

dilution ratios were identified for the deposition of the a-Si:H and SiN_x films at 200 °C to produce TFTs with electron mobility, threshold voltage, and gate bias stability comparable to those of the 300 °C control TFTs [21].

In the context of the above background considerations, it is apparent that different groups have selectively used elements of those techniques to minimise strain and to optimise the performance of a-Si:H TFTs on plastic substrates. In many cases, it has been common practice to deposit SiN_x on both sides of the substrate to equalise bending stresses, although the films themselves remained under stress. However, the combined CTE mismatch and intrinsic stresses are greatest in unpatterned films, and can lead to film de-lamination from the substrate [23]. Therefore, one approach has been to pattern the SiN_x gate insulator films into the small areas needed just for the TFTs themselves [23], but this cannot be done to a layer of SiN_x, which is also being used as a barrier film to prevent moisture absorption into the substrate. Hence, a process has been implemented to circumvent these problems [23, 25], by replacing the SiN_x barrier films with 1,200 nm thick layers of a vapour phase polymer consisting of $SiO_xC_yH_x$, and replacing most of the gate dielectric of SiN_x with a 200 nm thick layer of benzocyclobutene, BCB. As the CTE of BCB is 43 ppm/K, it is a good match to that of PES, which was the substrate used in this work. However, to ensure good electronic properties of the a-Si:H TFT, a thin 50 nm layer of SiN_x was retained as the first layer of a conventional triple stack of SiN_x, i a-Si:H (150 nm), and n^+ a-Si:H (50 nm) on top of the thicker BCB gate insulator, and all three layers in the stack were defined down to individual device islands, as shown by Fig. 11.10. The definition of the thin SiN_x gate insulator layer into individual islands led to a significant relaxation of the strain within the structure, as shown by the substrate distortion measurements in Fig. 11.11 [24]. In many respects, the TFT fabrication process was similar to the conventional back-channel-etch process, apart from the extra mask stage needed to define the SiN_x film at the bottom of the triple stack, and the use of aluminium for metal tracks due to its good ductility [25]. In addition, as the PES substrate limited processing temperatures to <220 °C, the SiN_x and a-Si:H depositions at 150 °C had to be optimised to maintain good TFT properties, and this was done by increasing the dilution of the reactant gases with helium [25]. These TFTs fabricated at 150 °C on PES compared well with conventional TFTs

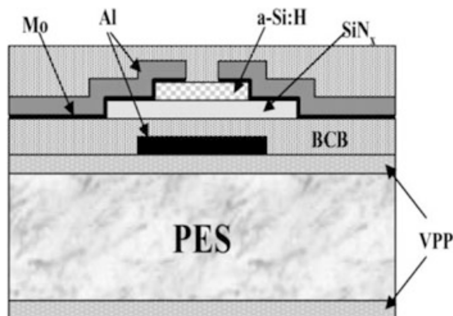

Fig. 11.10 Cross-sectional view of a back-channel-etched a-Si:H TFT with a combined SiNx/BCB gate insulator, within which the SiNx had been locally defined into an island. (Reprinted from [23] with permission of IEEE)

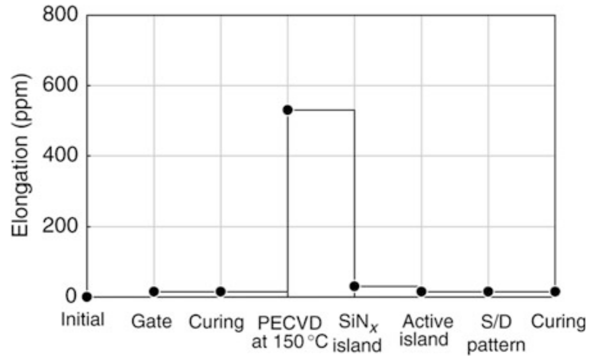

Fig. 11.11 Elongation of the substrate after each process step for an a-Si:H TFT on PES with a combined BCB/SiNx gate insulator. (Reproduced from [24] with permission of Wiley, Inc)

fabricated at 300 °C on glass, and had an electron mobility of 0.4 cm^2/Vs, a threshold voltage of 0.7 V and an insulator leakage current of $<10^{-13}$ A. The transfer characteristics are shown in Fig. 11.12.

Other groups have also looked to replace the stiff SiN_x layers, and Han et al. [16] used a homogeneous hybrid layer of SiO_2 and a silicone polymer, which was deposited at ~23 °C, for both the gate dielectric and for capping the PI substrate. As this hybrid layer was far more compliant than the usual SiN_x layers used for these purposes, the finished devices were less susceptible to cracking under tensile strain, and were able to tolerate ~5 % tensile strain, which was ten times more than the standard SiN_x-based TFTs shown in Fig. 11.6.

An alternative approach has been to use the PECVD deposition power density to engineer the strain throughout the structure, particularly within the SiN_x layers used to coat the clear plastic substrate, whilst deliberately using a high power deposition for the gate insulator SiN_x, in order to maintain good gate bias stress stability in the finished TFTs [8]. Figure 11.13 shows a cross-section of an etch-stop TFT, in which the back-face and top-face layers of SiN_x, used to cap the 75 μm thick plastic substrate, were deposited with compressive stress (at high

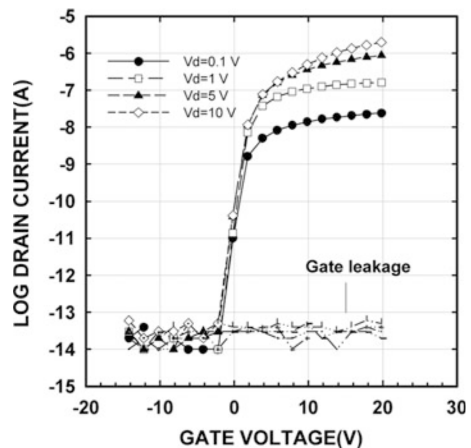

Fig. 11.12 Transfer characteristics of an a-Si:H TFT fabricated on a PES substrate at 150 °C, with a BCB/SiNx gate insulator. (Reprinted from [25] with permission of SID)

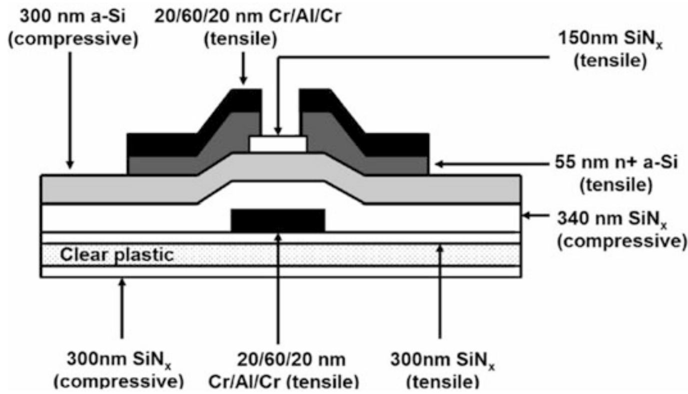

Fig. 11.13 Schematic cross-sectional view of an etch-stop a-Si:H TFT, showing the engineered stresses within each of the layers. (Reprinted from [8] with permission of IEEE)

power density) and tensile stress (at low power density), respectively. In addition, the high power density gate insulator was necessarily deposited with compressive stress, and the etch stop layer, which was deposited at lower power, was under tensile stress (see Fig. 11.7 for the relationship between strain and deposition power). The engineered substrate used for this work had a working temperature of ≥300 °C, a CTE of <10 ppm/K, and the depositions were carried out at 280 °C, with the substrate held flat, but not clamped, by a rigid frame. At the end of processing, the samples had a final anneal in air for 30 min [8].

The process delivered high quality TFTs, with an electron mobility of 0.96 cm^2/Vs, a threshold voltage of ~3.5 V and an on/off current ratio of $>10^7$, which was almost identical to TFTs processed on glass at the same temperature [8]. Of particular concern to the authors was the gate bias instability of these TFTs, as they had previously demonstrated that with reducing deposition temperature there was increased instability. A comparison of the threshold voltage shifts under gate bias stress is shown in Fig. 11.14, for TFT processing at 150, 250 and 300 °C on plastic and glass substrates [8]. Both the a-Si:H and SiN_x films deposited at 150 °C had hydrogen diluted reactant gases, whereas the higher temperature films did not [19]. As expected, the higher deposition temperatures improved device stability, but was not good enough for using these devices as pixel driver TFTs in AMOLEDs [22]. In subsequent work, the authors improved device stability by using 10:1 hydrogen dilution during the a-Si:H deposition to reduce the gate-bias-induced defect generation in the a-Si:H, and further optimised the SiN_x deposition, so that the gate bias stability obtained with 300 °C processing on the low CTE, clear plastic substrate exceeded the industry standard of a-Si:H TFTs on glass [22]. These TFTs had an electron mobility of 0.8–1 cm^2/Vs, a threshold voltage of 1.5–2.5 V, and an off-state current of $\sim 10^{-13}$A, all of which were similar to control devices on glass. Figure 11.15 shows the fractional change in TFT drain current as a function of time, under combined gate (7.5 V) and drain bias (12 V) stress, with the

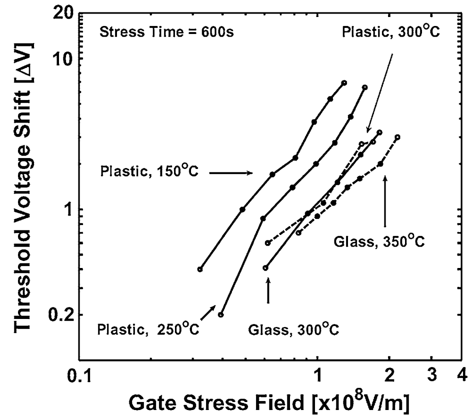

Fig. 11.14 Gate-bias stability measurements on ES a-Si:H TFTs fabricated at different temperatures on glass and plastic substrates. (Reprinted from [8] with permission of IEEE)

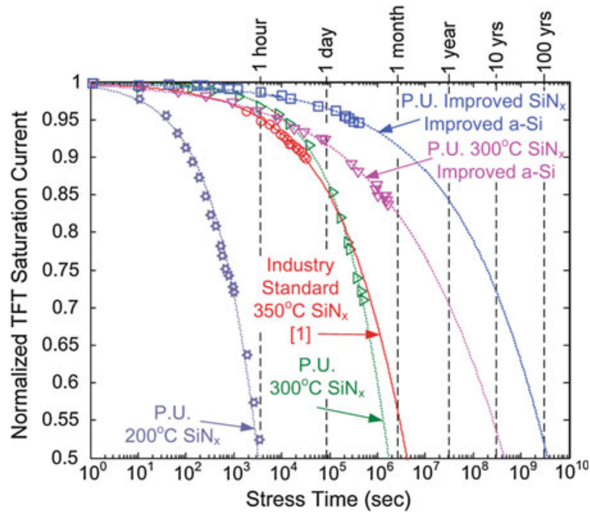

Fig. 11.15 Comparison of bias-stress stability measurements, for different a-Si:H TFT technologies, showing the reduction in normalised saturation current as a function of stress time, after stressing at Vg = 7.5 V and Vd = 12 V. (P.U. is Princeton University). (Reprinted from [22])

improved TFT lifetime exceeding that of the industry standard process, and being suitable for use in AMOLED displays [22].

11.4.1.2 Steel Foil Substrates

Steel substrates have good tolerance to high temperature processing, and, by being impermeable and stiff, they are less susceptible to the dimensional changes induced in plastic substrates by moisture absorption and the deposition of strained TFT layers with a large CTE mismatch. However, the as-delivered steel foil surface can be very rough, with greater than 1 μm peak-to-peak surface roughness reported [26], which needs to be reduced, before device processing, either by

surface polishing and/or by surface planarisation. There is also a need for a thick capping layer on the steel, in order to reduce the capacitive coupling between the TFTs and the conducting substrate [27]. Hence, the surface capping layer has a double purpose, and, in the use of steel foils to investigate pixel design for flexible AMOLEDs, 75 μm thick, 5 cm × 5 cm steel foils were coated with 1.6 μm of a spin-on glass followed by 600 nm of PECVD SiN_x deposited at 280 °C [26]. After deposition and patterning of Cr gates, a conventional triple stack of SiN_x, i a-Si:H, and n^+ a-Si:H was deposited at 280 °C (SiN_x) and 230 °C (a-Si:H). These layers were processed into back-channel-etched TFTs, yielding an electron mobility of 0.5 cm^2/Vs, a threshold voltage of 2 V, and an on:off current ratio of 10^7. The bias stress stability of these TFTs was not specified.

Other work on steel substrates has also sought to make flexible displays, but minimised the handling problems of flexible substrates by temporarily bonding them to rigid carriers during processing [28, 29]. In both cases, the temporary adhesive limited the processing temperature to 180 °C or lower. In one case [28], 100 μm thick steel foils were bonded to rigid carriers, and spin-coated with a 2 μm thick planarising film, followed by 300 nm of SiN_x deposited at 180 °C by PECVD. After Mo gate deposition and patterning, a triple stack of SiN_x (300 nm), i a-Si:H (80 nm) and SiN_x (100 nm) were deposited as the first deposition stage in an etch-stop TFT process. The finished TFTs had an electron mobility of 0.7 cm^2/Vs and a threshold voltage of 1.6 V, but the stability of these low temperature TFTs was not reported.

In the other process [29], 76 μm thick steel foils were attached to a glass carrier plate with a weak adhesive, and chemically polished before planarising them with a 3 μm thick layer of polymer resin, which was then capped with 0.4 μm of 150 °C PECVD SiN_x. The TFTs were processed through a conventional back-etch process, albeit with the PECVD depositions at 150 °C, and the resulting TFTs had an electron mobility of 0.35 cm^2/Vs and a threshold voltage of 1.47 V. Gate bias stressing at 30 V for 1000 s at 60 °C, gave a threshold voltage shift of 2.6 V, which is qualitatively consistent with the conclusions drawn in other work about the increasing degree of gate bias instability as the PECVD deposition temperature is reduced [8]. However, the authors argued that in applying these devices on steel to flexible AMOLEDs, the TFT stability problems could be mitigated by using phosphorescent OLEDs, whose increased efficiency would permit the TFTs to operate at lower values of V_G [29].

11.4.1.3 Carrier Plate Technology

As has been discussed in the preceding two sections, there are considerable problems to be overcome in the direct fabrication of TFTs on flexible substrates, which has included not just the substrate handling issues, but also the impact of reduced deposition temperatures on the bias-stress stability of the TFTs themselves. The handling issues can be minimised if all processing is carried out on the glass substrates familiar to the AMLCD industry, and device performance issues

can also be diminished if conventional processing temperatures are used. One such approach offering all these options is the EPLaR process (electronics on plastic by laser release) [30, 31].

The EPLaR process is implemented on an industry standard glass substrate, but, before processing, a 10 µm thick polyimide film is spun onto the glass and cured at 350 °C to fully polymerise the film. The PI is then coated with a PECVD layer of SiN_x to protect it against the chemicals used in the subsequent TFT process. The cured PI film can withstand processing temperatures up to 350 °C, and can, therefore, be passed through the standard a-Si:H TFT process [30]. At the end of processing, laser exposure, through the back-face of the glass plate, is used to release the PI film, and its TFT layers, from the substrate, yielding an active matrix of TFTs on a flexible plastic substrate. Moreover, as the PI film only increased the weight of the glass substrate by <1 % and its thickness by ~1.4 % [31], the standard robotic handling tools used in an a-Si:H TFT production facility can be used with the EPLaR substrates. This means that the EPLaR process can be introduced into a standard line with a minimum of disturbance, which sets it apart from the other technologies discussed in this and the previous sections. However, the use of non-transparent PI, as the final display substrate, prevents its use in transmissive displays, and the current application of EPLaR is for electrophoretic e-reader displays [31]. A cross-section of the back-channel-etched TFTs made with this process, prior to release from the glass substrate, is shown in Fig. 11.16, and an overview of the process flow is shown in Fig. 11.17 [30]. It has been demonstrated that the performance of the TFTs is unaffected by the laser release from the glass carrier substrate, and 9.7 inch electrophoretic displays have been made with this technology [31].

In contrast to the spin-on PI layer used in EPLaR, more conventional plastic substrates have also been used, and bonded to rigid substrates to avoid the problems of directly processing flexible substrates. Where low temperature plastics have been chosen, the maximum processing temperature is still limited by the T_{max}

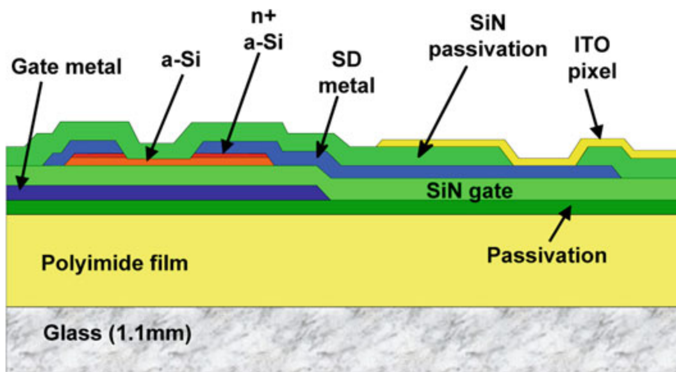

Fig. 11.16 Schematic cross-section of an EPLaR a-Si:H TFT array, shown whilst the PI film is still anchored to the glass substrate. (Reprinted from [30] with permission of SID)

Com. 1	Clean the glass substrate.
EP. 1	Spin-coat a polyimide layer on the glass substrate. Fully cure it and passivate with a thin layer of SiN.
Com. 2	Make a TFT array on the glass substrate.
Com. 3	Cut the glass substrate to form individual displays.
Com. 4	Laminate an electrophoretic foil onto the TFT array.
Com. 5	Attach driver electronics to the glass substrate.
Com. 6	Test the fully working display.
EP 2	Laser release the polyimide from the glass substrate.
Com. 7	Package the display in a display module.

Fig. 11.17 EPLaR process sequence for making flexible electrophoretic displays. (Reprinted from [30] with permission of SID)

of the plastic substrate, or by the temperature at which unacceptable stresses build up in both the films and the adhesive layer during the processing stages [32]. One example of this approach has used pre-shrunk and SiN_x barrier-coated PES [32, 33] and PEN [32, 34] substrates bonded to glass, and processed at 130 and 100 °C, respectively. The bonding, processing and plastic substrate release stages are shown schematically in Fig. 11.18, for both the TFT substrate and a colour filter top-plate on plastic for either an LC display or an electrophoretic e-reader display [35]. For the PES substrate processing, 200 μm thick layers were bonded to glass with an adhesive, which could be released at the end of processing, either thermally or by UV exposure. After bonding, a further SiN_x film was deposited at 130 °C, before the conventional triple stack was deposited, also at 130 °C, for a back-channel-etch TFT process. In order to minimise compressive strain, the layers were deposited at low plasma power [32] (in agreement with other work [8]), and this low power was also found to improve device performance, whereas other work reported that high deposition power was necessary to improve bias stress stability of the SiN_x [8]. The resulting 130 °C TFTs had an electron mobility of 0.5 cm^2/Vs, a leakage current of 10^{-13} A, and an on:off current ratio of 10^7. Gate bias stressing with $V_g = 20$ V and $V_d = 10$ V led to a threshold voltage shift of ~5 V, and ~50 % loss of on-current in 5,000 s, which is comparable to the results presented for 200 °C TFTs in Fig. 11.15. A similar process schedule was used for the 100 °C TFTs on PEN substrates, although the a-Si:H deposition was made at a reduced total gas pressure to improve the device characteristics, and a further anneal at 100 °C was made at the end of processing to reduce the contact resistance of the n^+ layer [32, 34]. These 100 °C TFTs also showed reasonable room temperature characteristics, with an electron mobility of 0.4 cm^2/Vs and an on:off current ration of 10^7. However, bias stress measurements showed a 5 V shift in threshold voltage after 3,960 s, and it is clear that these instability effects need further attention in low temperature TFTs on plastic [32]. However, in spite of the

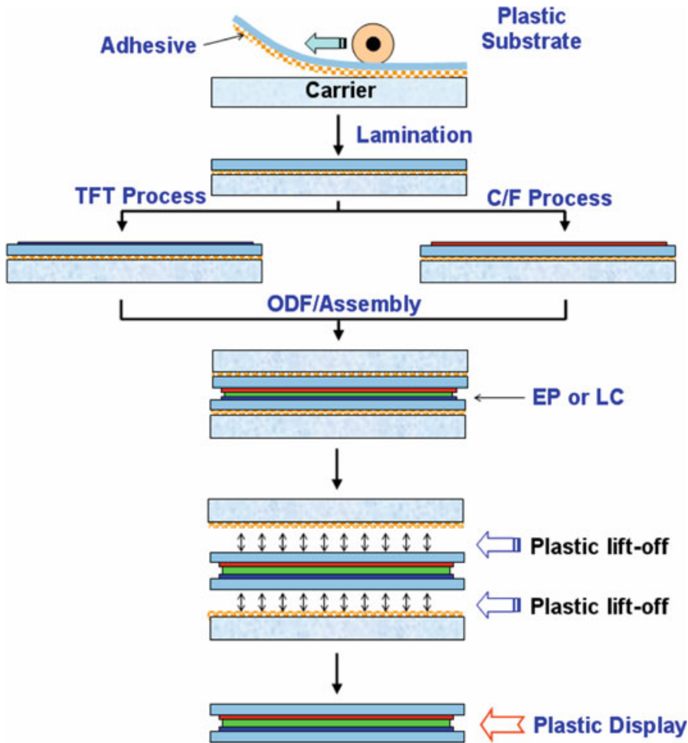

Fig. 11.18 Process sequence for flexible display fabrication using a carrier plate technology. (Reprinted from [35] with permission of SID)

device instabilities, 7 inch transmissive AMLCDs, and 14.3 inch electrophoretic displays were demonstrated on the PES and PEN substrates, respectively.

At the moment, this carrier plate technology, including EPLaR, is the favoured route for developing flexible backplanes of a-Si:H TFTs, using readily available plastic substrates, with a number of groups, in addition to those cited above, demonstrating LCD, electrophoretic and OLED displays [36].

11.4.1.4 Roll-to-Roll (R2R) Processing

Roll-to-roll processing is frequently viewed as the ultimate, low cost route to producing displays on flexible substrates [3]. The ideal R2R process would involve continuous movement of the flexible substrate from its host reel through the different layer deposition and definition stages until the final product is gathered on the collection reel [37]. A detailed discussion of the equipment required, and other R2R issues, is contained in Ref. [37], although no example is given of a particular R2R process being implemented. In this section, a recent application of these principles to the fabrication of a-Si:H TFTs is described [2, 38], using a self-

aligned imprint lithography (SAIL) process. Given the previous discussion on the dimensional instability of plastic substrates, the authors designed a self-aligned process to overcome one of the major hurdles associated with handling plastics. The process imprinted the etch mask on the substrate, so that any deformation in the plastic, causing potential misalignment between one pattern and the next, would also deform the mask by the same amount, thereby cancelling out the pattern shift. The process employed sequential deposition of all layers in the device structure [38], starting with an adhesion layer, the gate metal, the triple stack of SiN_x, i a-Si:H and n^+ micro-crystalline Si to the final metallisation layer without any intermediate pattern definition. Hence, the deposition process could be achieved without breaking the vacuum, leading to reduced contamination problems, and a smaller equipment footprint. Following this, a three-dimensional, UV-transparent elastomer etch mask, which had been wrapped around a quartz roller, was imprinted onto the surface of the device layer stack by rolling the quartz cylinder across the substrate. Whilst the roller was in contact with the sample surface, UV radiation passed through the cylinder and polymerised the imprinted material on the substrate surface. The roller plus imprint stamp is shown in Fig. 11.19a, and an SEM image of a high-aspect ratio and high-resolution imprinted pattern is shown in Fig. 11.19b. The multiple step heights in this pattern were used to define the individual layers in the device stack. In other words, the variable step heights represented the individual mask layers, which would be used in a conventional photolithography process. The use of the imprint pattern to define the device structure is illustrated in Fig. 11.20, and Fig. 11.20a shows the imprinted pattern on top of the device layer stack prior to any etching. Selective etching was used for the removal of individual layers in the stack, as well as for etching and removal of the polymer mask itself. The first etch stage is shown in Fig. 11.20b, in which the total device stack was defined, and Fig. 11.20c shows lateral undercutting of the gate metal, which removed it from narrow 'fuse' areas, such as the source and drain contact lines, assuring good isolation between the source/drain and gate metallisation layers. In Fig. 11.20d, the thinnest mask region had been completely etched away, exposing the stack of layers over the gate contact pad, and Fig. 11.20e shows the removal of those layers, down to the

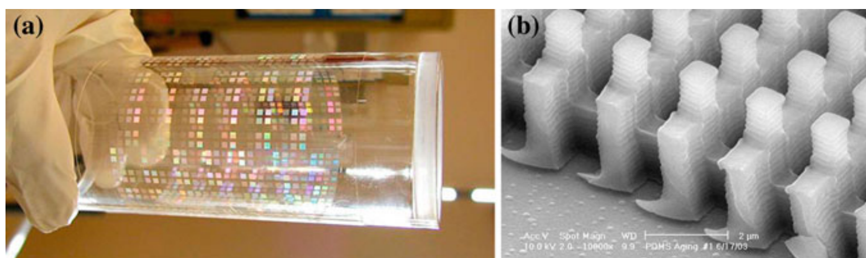

Fig. 11.19 **a** UV-transparent quartz roller with an elastomeric imprint stamp wrapped around it, and **b** SEM image of imprinted polymeric mask pattern used in the roll-to-roll SAIL process. (Reprinted from [38] with permission of SID)

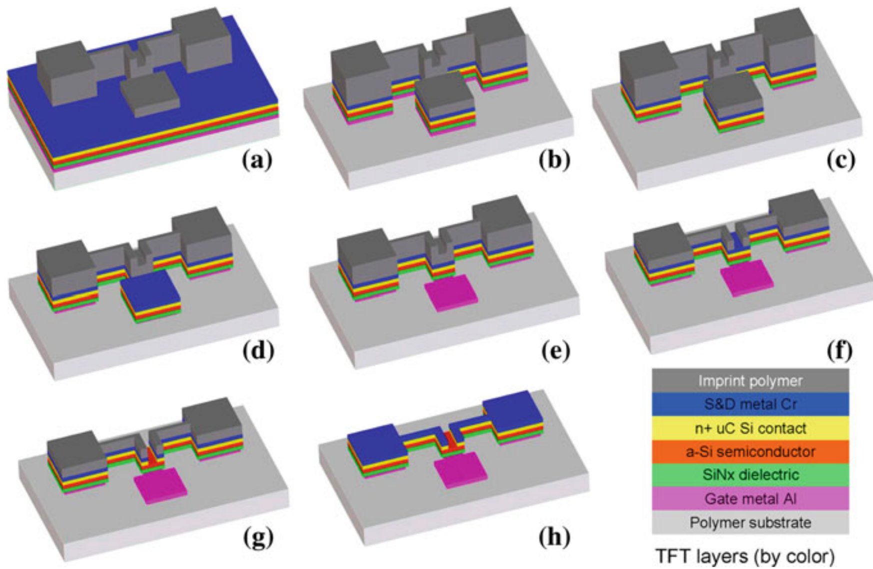

Fig. 11.20 Illustration of SAIL imprint mask and etching sequence to fabricate back-channel etched a-Si:H TFTs. (Reprinted from [38] with permission of SID)

contact pad itself. The next thinnest portion of the etch mask covered the TFT channel region, and, as shown by Figs. 11.20f and g, removal of that masking material permitted the n^+ mc-Si, and the source/drain metallisation, to be removed from the channel region, yielding a conventional back-channel-etched TFT. Figure 11.20h shows the removal of the last remaining layer of masking material, and the consequent exposure of the source/drain contact pads.

The process was implemented on a 13 inch wide and 50 μm thick web of polyimide material, with layer depositions at a maximum temperature of 250 °C, and used dry etching for the removal of the elastomer mask material and the Si-based layers, and wet etching for the metal regions.

The transfer characteristics, normalised by channel size, are shown in Fig. 11.21, and reasonable current scaling was obtained from devices with channel lengths from 100 μm down to 1 μm. The electron mobility in the short channel devices was 0.34 cm^2/Vs, and the on:off current ratio was 10^7. Small electrophoretic demonstration displays were also made using these roll-to-roll processed substrates [38].

11.4.2 Uniaxial Strain Effects on a-SiH TFTs

The effect of uniaxial strain on a-Si:H TFTs was measured by bending the samples around cylinders of different diameter, with the strain parallel to the direction of current flow in the channel. The strain was computed from the bending radius

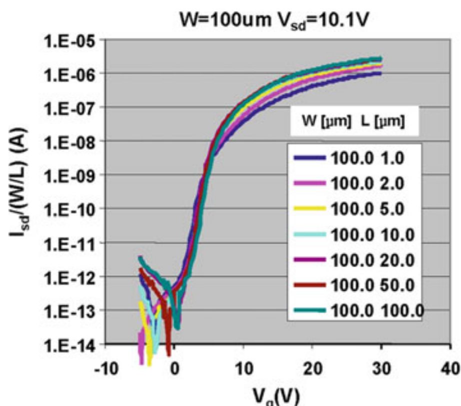

Fig. 11.21 Channel-dimension-normalised transfer characteristics of different channel length a-Si:H TFTs, fabricated by the SAIL process. (Reprinted from [38] with permission of SID)

using equation 11.6, and the samples were under tensile strain when the TFT layer was on the outer surface of a hollow cylinder, and under compressive strain when it was on the inner surface (see Fig. 11.4).

Consistent effects of strain have been reported on differently prepared samples. In one case it was measured on etch-stop TFTs prepared at 150 °C on 50 µm thick polyimide foils, which had used PECVD SiN_x layers for substrate capping and for the gate insulator [39]. In the other case, back-channel-etched TFTs were fabricated on 200 µm thick PES substrates, with an organic layer as the major portion of the gate insulator, topped by a thinner layer of SiN_x, which was defined into small device island areas in order to relieve the overall process-induced strain in the substrates [40]. The variation of electron mobility with strain is shown in Fig. 11.22 [39], where the applied strain values were established to lie within the limits of reversible elastic deformation. Beyond these limits, the samples were found to display irreversible changes in their characteristics, due to the formation of stress-induced cracks. Figure 11.22 shows a linear relationship between mobility and strain, in which compressive strain reduced the mobility and tensile strain increased it. The constant of proportionality in this data set was 26, and, in the other work, nearly identical results were found with a constant of proportionality of 28 [40]. The mobility changes occurred within the time taken to begin the TFT measurements, and there was no dependence of the changes upon the duration of the bending, up to a maximum measured duration of 40 h; and, once

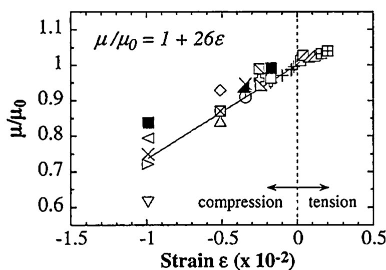

Fig. 11.22 Normalised electron mobility changes in a-Si:H TFTs as a function of uniaxial bending strain. (Reprinted with permission from [39]. Copyright (2002) American Institute of Physics)

the strain was released, the mobility reverted to its pre-strain values [39]. Uniaxial strain has been demonstrated to cause electron mobility changes in crystalline silicon [41] (which is discussed further in Sect. 11.5.2), but it was argued that those mechanisms could not apply to a-Si:H TFTs [39]. A tentative physical explanation for the a-Si:H results was given by noting that the measured electron mobility is governed by the width of the band-tail states, and that these are determined by the structural disorder in the material, which will change with strain [39, 40].

For both sets of samples, the off-state current was found to be independent of strain [39, 40], whilst the threshold voltage had no discernable dependence on strain, and the sub-threshold slope showed a small increase with compressive strain [39].

11.5 Poly-Si TFTs on Flexible Substrates

11.5.1 Fabrication Processes

The introductory section on flexible substrates applies equally to poly-Si TFTs, as to a-Si:H TFTs, and, as discussed, plastic substrates present a number of handling issues in terms of their low maximum processing temperature, dimensional instability and propensity to adopt a cylindrical shape in response to accumulated processing strains. In common with a-Si:H processing, broadly the same three strategies have been adopted in developing a flexible substrate technology for poly-Si TFTs. These are:

- A low temperature process matched to the properties of the plastic substrate,
- A higher temperature process, which could be implemented on thin steel foils,
- A transfer process, as distinct from a carrier plate process, whereby the functional TFT layer was removed from a glass substrate at the end of a conventional fabrication schedule, and transferred to a plastic substrate. This is the easiest technical option in the sense that the poly-Si on glass technology can be directly used, but is more expensive due to the additional process stages for the transfer, plus the extra substrate cost if the substrate cannot be reused.

Each of these three processing strategies is described below, followed by a further section on the response of poly-Si TFTs to bending strains. In Sect. 11.7, there is a discussion of some of the broader issues of device and circuit operation on plastic substrates, particularly for poly-Si TFTs, over and above the previously discussed handling issues.

11.5.1.1 Direct Fabrication on Plastic Substrates

Two approaches can be seen in the poly-Si work: one being to develop an ultra-low temperature process at <200 °C for use on the transparent, lower temperature substrates such as PEN, PET and PES [42, 46, 47] listed in Table 11.1, and the other to modify the established poly-Si process for the higher temperature substrates such as PI and PAR [10, 42]. In all cases, substrate preparation by drying, capping and pre-shrinking (as discussed in Sect. 11.2) was necessary to ensure dimensional stability of the substrates through successive photo-lithography stages.

The low temperature tolerance of the plastic substrates meant that only the excimer laser annealing, ELA, process was suitable for crystallisation of the precursor film, and the deposition temperature of this film, and of the gate oxide film, had to be reduced to meet the temperature constraints of the substrate. Similarly, the thermal budget for the post-metallisation anneal of the TFT, which is important for the reduction of charges and interface states, as discussed in Sect. 7.3.1, also had to be reduced.

For the precursor a-Si film, both conventional PECVD was used at 180 °C or 200 °C for PES and PI substrates, respectively [10], and sputter deposition in He was used for PES substrates [47]. The PECVD films were passed through the standard top-gated, non-self aligned, NSA, process, described in Sect. 7.3.2. The NSA architecture was chosen in preference to the SA architecture, because the latter needs a second laser pass to activate the source and drain dopants, and this could lead to potentially damaging, direct laser exposure of the plastic substrate (in regions where the poly-Si had been removed during the poly-Si island definition stage) [42]. With the NSA architecture, the source and drain dopants were implanted before crystallisation, and the unpatterned a-Si film protected the underlying plastic from direct exposure to the laser beam. Prior to ELA, the excess hydrogen had to be removed from the films, and this was done with a low intensity (230 mJ/cm^2) laser beam, which had a deliberately ramped leading edge for controlled release of the hydrogen. The film was then crystallised in the normal way with a second laser pass at 320 mJ/cm^2. After TFT island definition, the gate oxide layers were deposited at 180 °C and 250 °C for PES and PI substrates, respectively, but as these deposition temperatures were below the 300 °C normally used, the oxide quality was poorer and the interface state densities were higher than normal [10, 42]. The thermal desorption spectra, TDS, of these low temperature oxides [42] have already been discussed in Sect. 7.3.1, and, as shown in Fig. 7.23a, for depositions below 200 °C, the oxides showed high values of the undesired low temperature peaks. Figures 11.23a and b show the changes in n-channel sub-threshold slope and electron mobility, respectively, as a function of the post-metallisation anneal time and temperature [10, 12]. Even the higher quality oxides, deposited at 250 °C, required 1,000 min annealing at 250 °C for the electron mobility to reach 80 % of the standard-process mobility. Whereas, for the oxide deposited at 200 °C, and annealed at this temperature, only ~22 % of the standard-process mobility was reached in this time. This situation was also

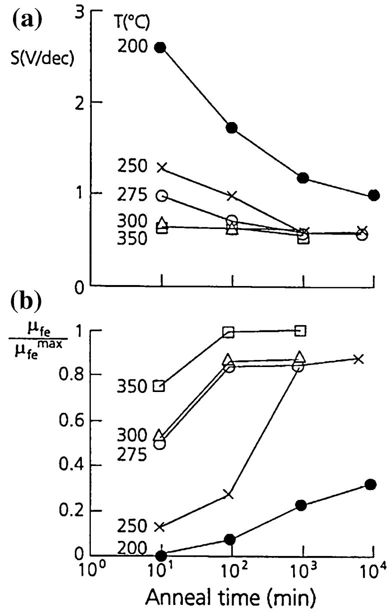

Fig. 11.23 Changes in (**a**) sub-threshold slope and (**b**) normalised electron mobility in poly-Si TFTs with post-metallisation annealing at the SiO_2 deposition temperature. (Reprinted from [12] with permission of SID)

mirrored by the sub-threshold slope results, and it was concluded that acceptable TFT performance could be achieved from a 250 °C process, with the transfer characteristics shown in Fig. 11.24. However, even at this temperature, the p–channel TFTs had larger sub-threshold slopes than the n-channel TFTs, and, at lower annealing temperatures, acceptable device performance was not obtained from p-channel TFTs. Only n-channel TFTS were obtained from a 200 °C process [10, 42, 46], and, hence, the CMOS poly-Si process was only compatible with the higher temperature PAR or PI substrates, and not with the PES substrates.

The reduced temperature oxide deposition process was identified as the processing stage limiting device performance, and, as discussed in Sect. 7.3, ECR

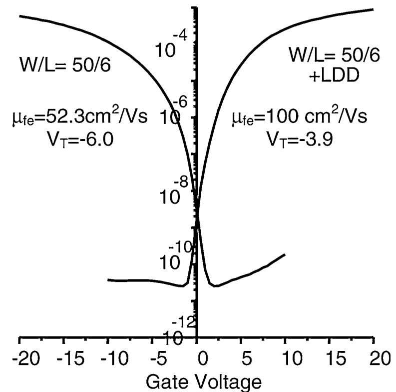

Fig. 11.24 Transfer characteristics of poly-Si TFTs fabricated on PI substrates at a maximum temperature of 250 °C. (Reproduced with permission from [10])

oxides, with good TDS spectra, have been deposited down to room temperature [44], but they have still needed post-deposition annealing above 350 °C to achieve low interface densities and useful TFT characteristics [43, 44].

For the He-sputtered precursor a-Si films on PES substrates [47], it was reported that He removal was easier than hydrogen removal, and this was accomplished with the leading edge of the crystallisation beam [47]. No details were given of the beam shape, but it must be assumed that it was closer to the raw semi-gaussian beam than to a top-hat beam. The overall processing of these samples was quite different from the work described above, and a schematic of the process flow is shown in Fig. 11.25. The gate oxide was deposited by PECVD at 110 °C, and, after gate metal definition, anisotropic plasma etching was used to remove the gate oxide from those areas not beneath the gate electrode. This enabled the exposed source and drain areas to be doped using a plasma-doping procedure in PH_3 or B_2H_6-containing gases, giving SA n- and p-channel TFTs, respectively. The dopants were subsequently activated by ELA, and it was argued that this process also led to heating of the Si/SiO_2 interface, and a consequent reduction of the interface state density. This 110 °C process on PES yielded high quality devices with an electron mobility of 250 cm^2/Vs and a sub-threshold slope of 0.16 V/decade [47]. However, many aspects of this process have not been fully revealed, such as the very low temperature PECVD oxide deposition process, and the overall quality of the resulting oxide. Nor have the details of the ELA activation process been discussed, including its possible impact upon the exposed PES substrate and its role in improving the Si/SiO_2 interface. Without these details, it is difficult to assess whether this process is readily implementable on PES, or on even lower temperature substrates, such as PEN.

11.5.1.2 Fabrication on Steel Foils

As discussed in Sect. 11.4.1.2, when compared with plastic substrates, steel foils are dimensionally stable, can be exposed to elevated temperatures, and are less susceptible to attack by a range of chemicals. Nevertheless, as-delivered steel substrates are too rough for direct use and need to be polished to achieve an acceptable level of surface roughness of a couple of nanometers, they also need to be thoroughly cleaned before use and capped with a thick enough dielectric layer to minimise parasitic capacitive coupling between the conducting substrate and the overlying TFT circuits [27, 48]. In the work quoted below, 125 μm thick polished foils of 304-type steel were used, with an average surface roughness of 3 nm. Both surfaces were coated with 3 μm of PECVD SiO_2 as both a planarising layer, and as a protective barrier to prevent metal ion diffusion into the overlying poly-Si TFTs [48]. This thickness was also necessary to minimise parasitic capacitive coupling between the conducting substrate and the TFTs [27].

The TFTs were fabricated using a SA process, similar to that described in Sect. 7.4.2 and shown in Fig. 7.34. The a-Si precursor layer was 50 nm thick, and was crystallised using an SLS process; then a 50 nm thick PECVD gate oxide was

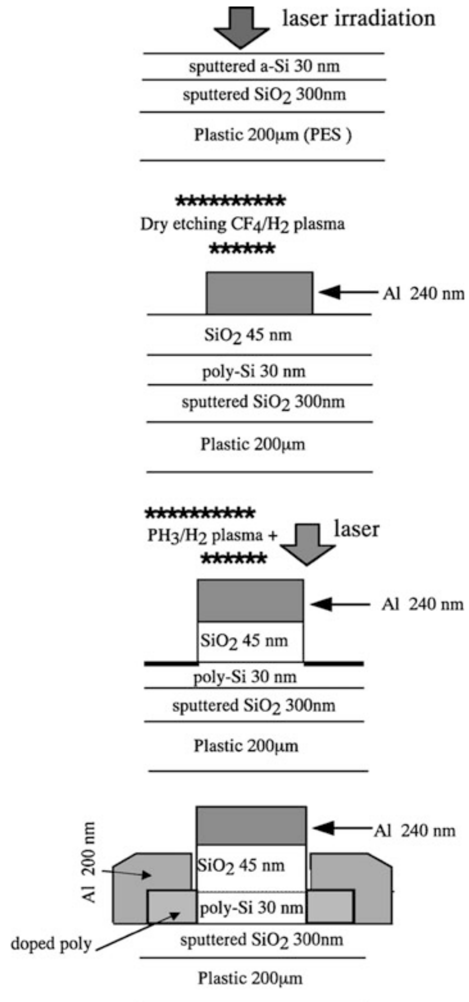

Fig. 11.25 Processing sequence of SA poly-Si TFTs on a PES plastic substrate, showing the crystallisation and plasma doping stages. (Reprinted with permission from [47]. Copyright (2000) The Japan Society of Applied Physics)

deposited from SiH_4 and N_2O, and a doped poly-Si layer was used as the gate electrode. The SA source and drain regions were ion doped and activated by thermal annealing at 650 °C. Following silicidation of the doped regions at 400 °C, the device was exposed to a hydrogen plasma at 300 °C, capped with a 300 nm SiO_2 interlayer dielectric, and, after source and drain metallisation, a final post-metallisation anneal at 300 °C completed the process [48]. Low leakage, high performance, short channel (L = 1 μm) n- and p-channel TFTs, were obtained, with sub-threshold slopes of 0.22 and 0.16 V/dec, and carrier mobilities of ~300 and ~150 cm^2/Vs, respectively.

As will be appreciated, the high processing temperatures tolerated by the steel foils permitted the fabrication of TFTs with performance comparable to conventional glass-based processing, and considerably better than has been achieved

directly on plastic substrates. In addition to the TFTs, a variety of demonstration circuits were fabricated on the foils, including ring oscillators, static shift registers with buffer output stages, decoders, sample-and-hold circuits and 5-bit digital-to-analogue converters [48]. In general, satisfactory performance was obtained from these circuits, although there was a gate-line resistance problem with the ring oscillators associated with the doped poly-Si gates. This would be resolved with lower resistance metal gates—but common metals, like aluminium, could not be used with a 650 °C dopant activation process. However, this is an issue with the specific process implemented on steel substrates in this work, rather than being a limitation imposed by the substrate choice itself. The ring oscillator circuits were fabricated with 1 μm and 2 μm channel length TFTs, and, the delay per stage was 0.88 ns and 1.0 ns, respectively. The speed should scale as $1/L^2$, and, this poor scaling with channel length suggested that the high frequency performance was being limited by parasitic effects [48]. It could be that thicker or lower-k dielectric layers may be needed for substrate capping to reduce the coupling.

11.5.1.3 Transfer Processes

With transfer processes, the basic glass-based processing schedule was retained, and, at the end of it, the TFT layers were detached from the glass and bonded to a plastic substrate. Two examples of this are, firstly, SUFTLA (surface free technology by laser annealing) [49, 50], in which a hydrogen-rich a-Si:H release layer was interposed between the glass substrate and the TFT layer, and, secondly, a glass etching procedure, in which the glass substrate was thinned to several tens of microns [51, 52] before being bonded to a plastic substrate. A third procedure used a different technique, whereby a polymer layer, which ultimately became the plastic substrate, was spun onto the glass substrate before TFT processing, and, at the end of processing, the polymer layer was released from the substrate with the TFT layers attached [53, 54]. This is conceptually similar to the EPLaR process [30, 55], described in Sect. 11.4.1.3, for the fabrication of a-Si:H TFTs on plastic substrates.

The SUFTLA process is shown schematically in Fig. 11.26a–e [50], and, in Fig. 11.26a, the fully processed TFT plate is shown with the sacrificial layer of hydrogen-rich a-Si:H, which had been deposited on the glass substrate prior to TFT processing. Before the removal of the glass substrate, the completed TFTs were mechanically protected from damage during the removal process by temporarily bonding a glass substrate to the top surface with water-soluble adhesive (Fig. 11.26b). The back surface of the original substrate was then exposed to an excimer laser, which released hydrogen from the a-Si:H layer, and detached the TFT layer from the glass substrate (Fig. 11.26c). The TFT layer was then permanently glued to a 400 μm thick plastic substrate (Fig. 11.26d) [49], after which the temporary protective substrate on top of the TFT layer was removed by dissolving the adhesive in water (Fig. 11.26e). The TFT process [49] was a conventional self-aligned fabrication schedule, using a 50 nm pre-cursor a-Si layer,

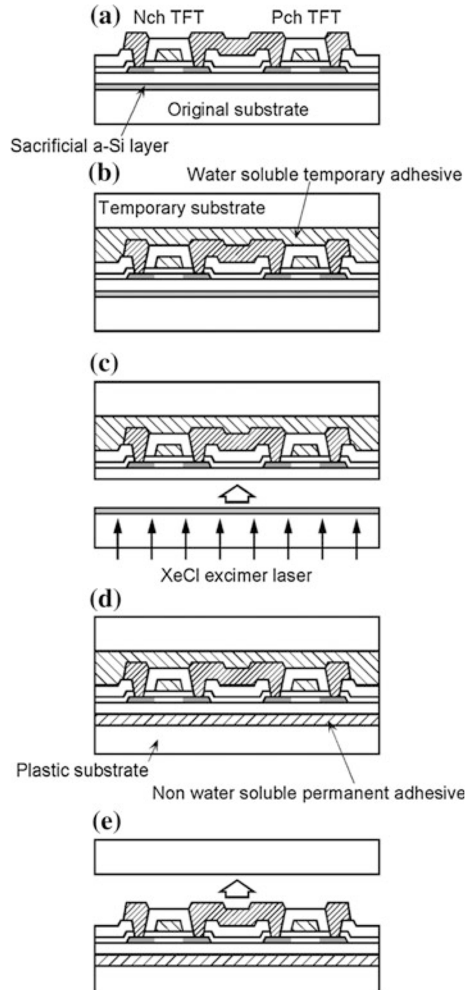

Fig. 11.26 SUFTLA process flow at the end of poly-Si device processing, showing the transfer stages from the glass substrate to the final plastic substrate. (Reprinted from [50] with permission of SID)

which was crystallised by ELA, and capped by a 120 nm gate oxide. After definition of Ta gate electrodes, the source and drain regions were ion doped, and activated at 300 °C. TEOS layers were used as interlayer dielectrics to separate the gate metallisation level from the source/drain metallisation, and also for final capping of the finished devices. Small changes in device characteristics were noted before and after the transfer process, such as electron mobility and threshold voltage changes of 119–124 cm^2/Vs and 3.3–3.9 V, respectively [49]. However, the transfer process was described as high yield, and many demonstration devices were produced with this process, including a 0.7 inch AMLCD [49], a 7.1 inch electrophoretic display, both with integrated drive circuits, and a range of other electronic circuits including an 8-bit microprocessor [50].

The glass etch transfer process was optimised for application to large 300 mm × 350 mm substrates, and the final bonding was to an engineered fibrous

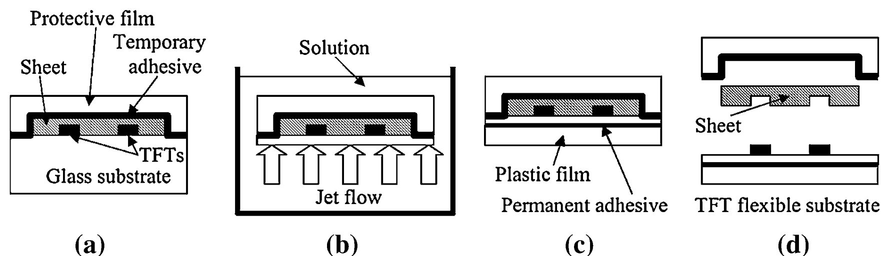

Fig. 11.27 Transfer sequence, at the end of poly-Si TFT processing, showing the thinning of the glass substrate by etching, and the subsequent adhesive-bonding to a plastic substrate. (Reprinted from [52] with permission of IEEE)

glass-reinforced plastic, FRP, substrate [11]. The substrate was designed to have a CTE of $\sim$14 ppm/K, which is lower than most of the plastics listed in Table 11.1, and is a better match to the TFT layers. The adhesive attaching the TFT layers to the FRP substrate was also optimised to reduce de-lamination of the substrate from the TFT layer under bending strain. The transfer process is shown schematically in Fig. 11.27a–d [52], and, in common with the SUFTLA process, the fully processed TFT plate was capped with a protective film, secured by a heat-releasable adhesive, to prevent damage to the TFT layer during the transfer process (Fig. 11.27a). The glass substrate was then jet etched (Fig. 11.27b) to reduce its thickness to a few tens of microns in a uniform fashion, and this left behind a smooth etched surface. The thinned glass was then permanently bonded, using the optimised adhesive, to a 220 μm thick FRP substrate (Fig 11.27c). Finally, the top protective film was removed, by heating the structure to 110 °C for 90 s to release the temporary adhesive, and the finished TFT layer on the plastic substrate was annealed at 150 °C to complete the process. Very good reproducibility of the TFT characteristics was found before and after the transfer process, as shown by the results in Fig. 11.28.

A potentially simpler process option is one in which the TFTs are fabricated directly on a thick spun-on layer, of a suitable polymer, on a rigid substrate, and the double layer of TFTs and polymer film removed from the rigid substrate at the end of processing. In this case, the resulting TFT layer is automatically on a flexible substrate, and a separate substrate attachment stage can be avoided. The implementation of this process [53, 54] used an 8 μm thick spin-on layer of polyimide on an oxidised silicon substrate. Following thermal curing of the PI layer at 350 °C, it had a CTE of 3 ppm/K, which was much lower than the bulk PI film in Table 11.1, and was a good match to the silicon substrate. The cured PI layer was coated with a barrier stack of SiN_x and SiO_2, prior to the growth of a 70 nm thick a-Si pre-cursor layer, capped by a 25 nm thick heavily phosphorus doped a-Si layer. A channel-etched, non-self-aligned TFT process was implemented with these layers [45], but, due to the thermal constraints imposed by the underlying PI layer, the normal 450 °C thermal dehydrogenation process could not be used on the a-Si film. Instead, it was partially dehydrogenated for 18 h at

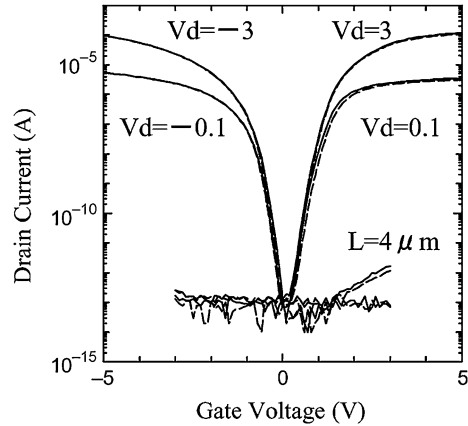

Fig. 11.28 Poly-Si TFT transfer characteristics before (*solid line*) and after (*broken line*) the glass etching transfer process. (Reprinted from [52] with permission of IEEE)

350 °C, before being crystallised with a modified excimer laser beam, having a ramped leading edge designed for the controlled release of hydrogen from the film [53]. The gate dielectric was a 150 nm thick layer of ECR-PECVD SiO_2 [44] deposited at room temperature, and, after deposition and definition of the aluminium source, drain and gate electrodes, there was a post-metallisation anneal at 350 °C. At the end of this process, the poly-Si devices on the 8 μm thick PI layer were mechanically released from the silicon substrate, although the details of the release process have not been revealed. A number of demonstration poly-Si circuits were fabricated on these flexible substrates, including logic gates, ring oscillators, and amplifiers, as well as an integrated humidity sensor [54].

EPLaR has also been used to make poly-Si TFTs [30], but with a conventional self-aligned p-channel process, which included laser activation of the source and drain dopants. However, the PI intermediate layer on the glass substrate was damaged by this direct exposure to the laser, and an unspecified shielding layer was interposed between the TFT layers and the PI to protect it. As with the a-Si TFT implementation of EPLaR, the poly-Si TFT layer on PI was released from the glass substrate by excimer laser exposure of the PI layer through the glass substrate. The TFT characteristics remained unchanged by the release process.

11.5.2 Uniaxial Strain Effects on Poly-Si TFTs

The effect of strain on poly-Si TFTs has been studied with SLS-crystallised devices, made on flexible steel substrates, using the process described in Sect. 11.5.1.2 [27, 48]. Small 20 mm × 35 mm sections of the substrates were cut from the processed foils and bent around hollow cylinders of different radius [13]. The TFTs were under tensile strain when bent around the outside of the cylinders, and under compressive strain when bent around the inner surface, and the dependence of strain on radius of curvature is given by Eq. 11.6.

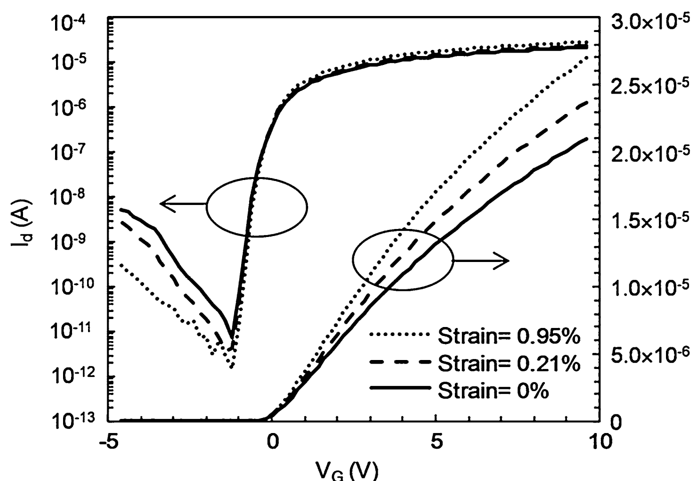

Fig. 11.29 Effect of uniaxial tensile strain on n-channel poly-Si TFTs. (Reprinted with permission from [13]. Copyright (2009) American Institute of Physics)

By measuring the TFT characteristics as a function of the bending radius, the dependence of the various device parameters on uniaxial strain was established [13]. In all measurements, the strain was parallel to the direction of current flow, which itself was parallel to the SLS-induced sub-grain boundaries, and the n-channel characteristics under tensile strain are shown in Fig. 11.29. There was decreased off-current and increased on-current with increasing strain, where the increased on-current was caused by an increase in electron mobility. The opposite trend was found for compressive strain, and the summarised carrier mobility results are shown in Fig. 11.30. This figure also includes the hole mobility results derived from p-channel TFTs; as will be seen, there were opposite trends between hole and electron mobilities. In contrast, the leakage current behaved identically in both channel types: decreasing with tensile strain and increasing with compressive strain. In single crystal silicon p-n junction diodes, the leakage current was also found to increase with compressive stress, which was attributed to stress-induced decrease of the Si band-gap at the rate of ~0.1 meV/MPa [56]; similarly, MOSFET junction leakage current was found to increase with compressive stress and to decrease with tensile stress [57]. The leakage-current in poly-Si TFTs clearly behaves in the same way as in crystalline silicon, and has been similarly attributed to stress-induced changes in the band-gap [13].

The carrier mobility changes have also been correlated [13] with similar stress-induced mobility changes in crystalline Si MOSFETs. For p-channel MOSFETs, compressive stress increased the curvature of the lowest energy valence band sub-band, reducing the hole effective mass [58], and, hence, increased the hole mobility. For n-channel MOSFETs, tensile stress led to splitting and repopulation of degenerate conduction band sub-bands, such that the population in the sub-band having the low transverse effective mass was enhanced at the expense of the

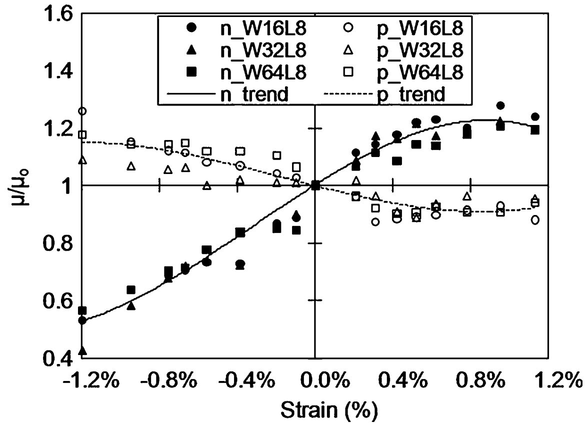

Fig. 11.30 Effect of uniaxial tensile (+) and compressive (−) strain on normalised hole and electron mobilities in poly-Si TFTs. (Reprinted with permission from [13]. Copyright (2009) American Institute of Physics)

sub-band having the higher longitudinal effective mass, thereby increasing the overall electron mobility [59].

The TFT mobility changes, discussed above, were observed in long grain SLS poly-Si, and similar changes have also been reported in metal-induced crystallised poly-Si [60]. In more conventional ELA poly-Si, on thin plastic substrates, no discernable mobility changes were detected down to a bending radius of 1.3 cm [53]. However, using Eq. 11.6, the strain in the TFT layer on the 8 μm thick compliant PI substrate is calculated to be only 0.012 %, which is considerably less than the values in Fig. 11.30, and this may be why no mobility changes were observed.

For the other device parameters, the sub-threshold slope in both channel types increased with tensile stress and decreased with compressive stress, whilst threshold voltage showed no dependence upon compressive stress, but decreased with tensile stress [13]. In contrast to the leakage current and carrier mobility changes, no simple physical models have been advanced to explain these sub-threshold slope and threshold voltage changes.

11.6 Organic TFTs on Flexible Substrates

In principle, the fabrication of organic TFTs on plastic substrates should present fewer issues than is the case with inorganic TFTs, particularly in terms of the temperature constraints imposed by the substrates. As has been discussed above, these constraints set an upper processing temperature limit, determined by the substrate's glass transition temperature, but the actual maximum temperature can be reduced below this by CTE mismatch considerations. For organic TFTs, there should be a better CTE match, and device processing itself is conventionally performed close to room temperature. However, although the upper temperature constraint is less of an issue, other attributes of plastic substrates, such as their

dimensional instability, sensitivity to chemical attack etc., still have to be controlled during processing. To deal with the dimensional instability problem, most groups pre-shrink the substrate before processing; however, details on subsequent substrate encapsulation are left unspecified in a number of publications. Also, some groups have adopted a rigid carrier plate process to reduce the handling problems of flexible substrates.

As is apparent from Chap. 10, there are a large number of organic transistor materials, device geometries, and fabrication processes, which have already been discussed, and those details will not be repeated below. Only those aspects of the process, specific to fabrication on plastic substrates, will be considered, and the reader is referred to Chap. 10 for further information.

In the following two sub-sections, the direct fabrication of OTFTs on plastic substrates, and rigid carrier plate processing are reviewed, and, finally, the impact of substrate bending on TFT performance is considered.

11.6.1 Fabrication Processes

11.6.1.1 Direct Processing

Where discrete TFTs have been fabricated on plastic substrates, particularly to examine bending effects, both PI [17] and PEN [61] substrates have been used, with evaporated gold bottom-gate and top source and drain contact layers. The gate dielectric was a spin-coated PVP (polyvinylphenol) layer, and shadow mask evaporation was used for the pentacene TFT body layer. No details were given of the handling of the substrates. In another example of pentacene TFTs on PEN substrates [62], the substrate handling was more clearly defined, and followed the procedures familiar from the discussion of a-Si and poly-Si TFT processing on plastic substrates. In particular, the substrate was initially annealed at 180 °C to degas and pre-shrink it, and it was then encapsulated with 100 nm thick SiN encapsulation layers. The bottom-gated and bottom-contacted TFTs had a spin-coated PVP gate insulator, which was cured at 180 °C, and the pentacene layer was capped with parylene and Cr/Au in order to photolithographically define it. In order to protect the pentacene from the effects of ambient water vapour and oxygen, the whole structure was encapsulated with a 1 μm thick spin-coated layer of photacryl, which was cured at 150 °C after photo-patterning.

A full-colour 2.5 inch AMOLED demonstrator was fabricated on a 200 μm thick PES substrate, which had been annealed at 180 °C to shrink it prior to processing, and an alignment accuracy of a few microns was obtained over the 4 inch substrate [63]. The evaporated pentacene TFTs were bottom-gated and bottom-contacted, using gold for both, and a 400 nm thick spin-coated organic PVP-OTS (octadecyltrichlorosilane) layer was used for the gate dielectric, which was cross-linked at 130 °C. The TFT structure was then encapsulated in organic

passivation and planarisation layers prior to the evaporation of the OLED structure. The all-organic composition of the display contributed to its satisfactory operation at a bending radius of 20 mm [63].

11.6.1.2 Carrier Plate Processing

A number of groups have used rigid carriers to reduce the handling problems of plastic substrates, where the carriers have either been glass plates (carrying PET [64] and PEN [65] films) or silicon wafers used with PI films [66]. Generally, the plastic substrates were pre-shrunk by baking for 2 h at 120 °C and at 150 °C for the 125 μm thick films of PEN and PET, respectively. Inorganic barrier films of SiN were used in both cases to prevent moisture and oxygen absorption, and, thereby, improve dimensional stability. The plastic foils were then bonded to the carrier plates using temporary adhesives. In all cases, a bottom-gated and bottom-contacted device architecture was used, with pentacene as the semiconducting TFT material. This process was used to make flexible AMOLED displays [64, 65], and electrophoretic display and shift register [66] demonstrators.

In contrast to the bottom-gated pentacene TFTs, a production facility has been established for flexible electrophoretic displays based upon a printing technology, using top-gated and bottom-contacted polyfluorene-based polymer TFTs [67, 68]. The facility can produce 10.7 inch displays by processing Gen 3.5-sized substrates ($\sim$0.62 × 0.72 m^2) of 125 μm thick PET. A major advantage of the printing process is that it can produce devices without the conventional alignment stages, and that the position of the printing head can be locally adjusted to compensate for substrate distortion [67, 68], but the substrates were, nevertheless, temporarily attached to glass carrier plates during the patterning stages [68]. To minimise dimensional instability, the substrates were pre-annealed, and a planarising layer was deposited before the metal source and drain contacts were formed. The device processing was at, or near, room temperature, using a solution-deposited polymer dielectric for both the gate insulator and the interlayer insulator (between the gate electrode and the pixel electrode).

11.6.2 Uniaxial Strain Effects on Organic TFTs

As with the inorganic TFTs, strain effects were assessed by measuring changes in the TFT characteristics as function of the externally applied bending radius, and this was then converted into a strain value using equation 11.6. Bending strain measurements made on pentacene TFTs, fabricated on 125 μm thick PEN substrates, are shown in Fig. 11.31a–d [61]. These were bottom-gated and top-contacted TFTs, with a 900 nm thick PI gate dielectric. The on-current results in Fig. 11.31a and b were obtained with the strain parallel to current flow, but the hole mobility results in Fig. 11.31c and d were obtained with the strain both

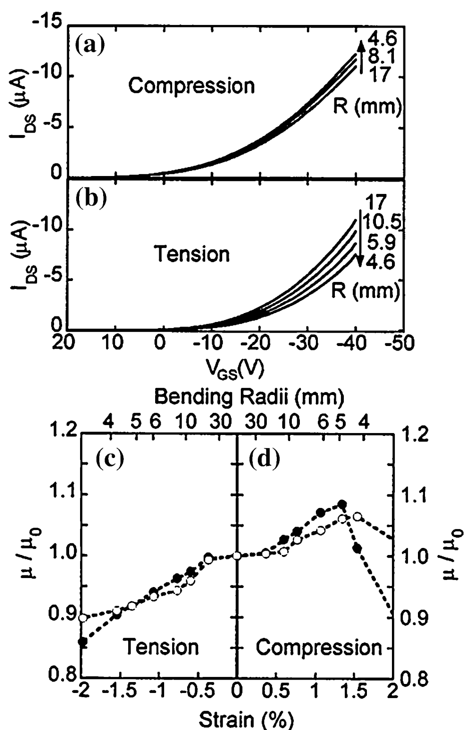

Fig. 11.31 Effect of bending strain on pentacene TFT transfer characteristics under (**a**) compression (**b**) tension, and the effect of bending strain on the hole mobility under (**c**) tension and (**d**) compression (filled and open circles were for current flow parallel and perpendicular to the strain). (Reprinted with permission from [61]. Copyright (2005) American Institute of Physics)

parallel and perpendicular to current flow. As will be seen, the on-currents and hole mobility values increased with compressive strain and decreased with tensile strain, irrespective of the strain direction. The strain effects were explained in terms of hopping transport in the TFTs, where the hopping barrier height was determined by the molecule spacing in the pentacene film, and this decreased under compressive strain and increased under tensile strain [61]. The strain isotropy was attributed to an inter-grain current flow path in which coupled grains were randomly oriented.

The authors also monitored the changes in capacitance, C, of the 900 nm thick PI gate dielectric, and found that it increased by ~3 % with 1.5 % tensile strain, and decreased by ~2.2 % with 1.5 % compressive strain (both of which corresponded to a 4 mm bending radius) [61]. This was explained by changes in the thickness of the gate dielectric caused by the Poisson effect (rather than by changes in dielectric permittivity), where those orthogonal changes are related to the bending radius, R, by:

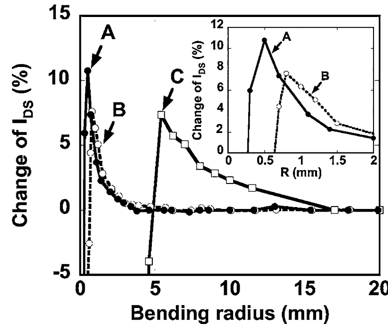

Fig. 11.32 Changes in the on-current in pentacene OTFTs, on 13 μm thick PI substrates, as a function of the bending radius. The TFTs were capped with parylene passivation layers with thicknesses of: (**a**) 13 μm (**b**) 10 μm and (**c**) 0 μm. (Reprinted with permission from [17]. Copyright (2005) American Institute of Physics)

$$1 - C/C_0 = -D/2(1 - v)R \qquad (11.10)$$

C_0 is the unstrained capacitance, D is the substrate thickness, and v is Poisson's ratio, which is 0.4 for the PI film [61]. It was argued that these changes, and other dimensional changes in the TFT geometry, should be taken into account when calculating the strain-dependent carrier mobility values.

As seen in Fig. 11.31d, device failure occurred at a compressive bending radius of ~5 mm, which generated a compressive strain >1.5 %, and led to buckling of the gold electrodes [61]. These measurements were made on un-laminated substrates, in which the TFTs on the substrate surface experienced maximum strain for a given bending radius. In a practical application of TFTs on a flexible substrate, the substrate will be capped by another film, such as an electrophoretic film or OLED layer etc. This will move the TFTs towards the neutral plane, and, thereby, reduce the strain for a given bending radius. The beneficial effect of this is shown in Fig. 11.32, in which the same type of pentacene TFTs, as shown in Fig. 11.31, were fabricated on 13 μm thick PI substrates, and laminated with parylene layers of 13 μm and 10 μm thickness, and compared with an uncapped control sample (curves A, B and C, respectively) [17]. The un-laminated sample C showed the same failure, as previously, at a bending radius of 5 mm, but the well-matched sample A, with the same substrate and top-layer thicknesses of 13 μm, could be bent down to a radius of 0.5 mm before failure.

11.7 Plastic Substrate Issues

Over and above the previously discussed issues of handling and processing TFTs on plastic substrates, other concerns have been identified in their use with high-speed poly-Si devices. A particular issue has been power dissipation in the TFT, leading to self-heating, and subsequent heating of the plastic substrate [7]. Where

this is sufficient to cause a temperature rise above the glass transition temperature of the substrate, thermal deformation of the plastic can occur leading to mechanical damage to the TFT. Self-heating is also a potential problem on glass substrates [69] (where the thermal conductivity is 1.38 W/m/K), leading to threshold voltage instability under on-state stress conditions of combined gate and drain bias (see Sect. 8.6.2). Self-heating is a greater problem on plastic substrates due to their lower thermal conductivity of $\sim$0.2 W/m/K, and, as this means that radiation from the device edges becomes the limiting mechanism for heat dissipation, the device design becomes important. In particular, devices with large values of W and L are vulnerable to self-heating, and the authors [7] recommend replacing large W devices with a number of parallel devices each having a smaller W. Also, the overall power dissipation can be reduced by reducing the drive voltages, and this can be accomplished by scaling down the TFT geometry [7], especially the channel length and the gate oxide thickness, as well as the drain bias, by a scaling factor k. This should reduce power dissipation per unit area, at fixed channel current, by the factor k, as well as increasing the operating frequency by k.

A further recommendation is to improve the energy efficiency of the circuits themselves, by using asynchronous circuits [7]. Conventional MOSFET and TFT circuits are usually termed synchronous, and global clock signals are applied to all logic blocks throughout the system. In asynchronous circuits, the clock signals are only sent to particular logic blocks when they are needed, and poly-Si asynchronous microprocessors have been found to dissipate 73 % less energy than synchronous circuits performing the same function [7].

Hence, both changes in device design and circuit design are advocated for optimising the performance of poly-Si circuits on low-temperature plastic substrates, even where the handling issues of plastic substrates have been circumvented by using a transfer process.

Self heating has also been reported in a-Si:H TFTs on PI substrates [70], in which the width-normalised drain current of TFTs with W/L = 80 μm/8 μm and 10 μm/8 μm agreed at low drain bias, but, at high gate and drain bias, the large W TFT showed a higher current than the small W TFT. In the large W TFT, the current also failed to saturate, as shown in Fig. 11.33a. Hence, the same geometric factors leading to self-heating have been identified in a-Si:H TFTs as in poly-Si TFTs. For self-heating to occur, both gate and drain bias must be applied in order to drive current through the TFT, as is the case in Fig. 11.33a. When threshold voltage stability was investigated under saturation drain bias conditions ($V_D = V_G$-V_T) at large V_D, the threshold voltage shift was found to increase with increasing channel width, as shown in Fig. 11.33b, and this shift was larger than with gate bias stress alone [70]. Device stability has been studied under combined gate and drain bias stress in conventional a-Si:H TFTs on glass [71], where the change in threshold voltage was found to be less than under gate bias stress alone. This was due to the reduced overall carrier density in a pinched-off inversion layer (see Sect. 6.4.3). Hence, the opposite effect was seen when comparing combined bias-stress effects in TFTs on glass and plastic substrates, and the larger shifts seen on the plastic substrates have been attributed to self-heating in large W TFTs [70].

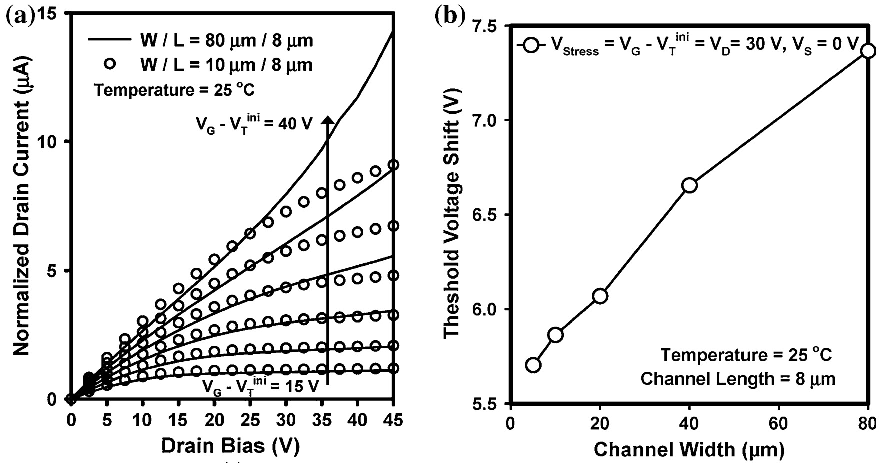

Fig. 11.33 **a** Normalised drain current in a-Si:H TFTs for W = 80 μm, and W = 8 μm, showing higher currents for W = 80 μm at large values of V_G and V_D, and **b** dependence of threshold voltage instability on channel width, W, under saturation bias-stress conditions. (Reprinted from [70] with permission of IEEE)

In addition, the self-heating-induced threshold voltage instability was further increased by bending the substrate down to a 15 mm radius of curvature [70]. Self-heating has been previously reported in short channel a-Si:H TFTs on glass [72], but neither channel width nor device stability effects were investigated in that work. In common with poly-Si TFTs, it is clear that large W TFTs can cause self heating, which, in the case of a-Si:H, exacerbates bias-stress instability effects, and attention to device design is required to minimise these effects.

11.8 Summary

The flat panel display industry has been built around a-Si:H TFTs on rigid glass substrates, but there are clearly identified applications requiring flexible substrates. This has stimulated much research investigating how the established a-Si:H, and also poly-Si, TFT technologies could be implemented on inexpensive plastic substrates. The major issues in using these readily available substrates have been their low maximum processing temperatures, thermal mismatch to the conventional device layers such as SiN_x:H, SiO_2 and Si, and also the dimensional instability of the plastic itself. In view of these problems, a number of processing strategies have emerged, including reduced temperature TFT processing directly onto the plastic substrates, and the use of non-standard plastic substrates, which have been engineered to better match the thermal properties of the TFT layers. Secondly, the use of alternative flexible substrates, principally stainless steel foils, which circumvent many of the handling problems of plastic. Thirdly, and

principally for a-Si:H TFTs, a carrier plate technology, whereby the plastic substrate is temporarily bonded to a glass substrate during processing, or a plastic film is spun onto the glass, which, at the end of processing, is released from the glass carrier plate. For poly-Si, a variant of this has emerged, which is a transfer process, whereby the TFTs and circuits are processed in the conventional way on a glass substrate, and, at the end of processing, they are removed from the glass substrate and transferred to a plastic substrate. The most sophisticated demonstrators so far have emerged from either the carrier process for a-Si:H TFTs or the transfer process for poly-Si TFTs. How economic these processes are will emerge in the longer term, but, for the moment, they are, at least, successful expedients which are able to exploit the well established glass plate technologies. The long-term aspiration in this area is for a truly plastic-based, roll-to-roll technology, which does not try to impose conventional photolithography on dimensionally unstable substrates, and some early examples of this approach have been reported for a-Si:H TFTs.

The alternative to the conventional inorganic TFTs, are organic TFTs, which should have a better match to the plastic substrate constraints of reduced processing temperatures and high coefficients of thermal expansion, although the dimensional instability of the plastic still represents a problem for pattern definition. As with the inorganic TFTs, similar strategies have been adopted, including direct substrate processing, carrier plate processing, plus a printing process, which is less sensitive to the dimensional instability of the substrate. With organic TFTs, the most sophisticated demonstrators, so far, have used the carrier plate process or the print-based process.

In addition to the discussion of device processing, the mechanics of bending and strain in flexible substrates is summarised.

References

1. Sarma KR (2012) Flexible displays: attributes, technologies compatible with flexible substrates and applications. In: Chen J, Cranton W, Fihn M (eds) Handbook of visual display technology. Springer, Berlin, p 2012
2. Jackson WB, Almanza-Workman M, Chaiken A, Garcia RA, Jeans A, Kwon O, Luo H, Mei P, Perlov C, Taussig C, Braymen S, Jeffrey F, Hauschildt J (2008) Active-matrix backplanes produced by roll-to-roll self-aligned imprint lithography (SAIL). SID Symp Digest 39:322–325
3. Yeo J-S, Elder R, Jackson W, Hoffman R, Henze D, Koch T (2011) Paper-like electronic media: the case for R2R-processed full-color reflective displays. SID Inf Disp 27(1):18–23
4. Sarma KR (2012) Flexible displays: TFT technology: substrate options and TFT processing strategies. In: Chen J, Cranton W, Fihn M (eds) Handbook of visual display technology. Springer, Berlin, p 2012
5. MacDonald BA, Rollins K, MacKerron D, Rakos K, Eveson R, Hashimoto K, Rustin B (2005) Engineered films for display technologies. In: Crawford GP (ed) Flexible flat panel displays, Wiley ltd., Chichester, England

6. Suo Z, Ma EY, Gleskova H, Wagner S (1999) Mechanics of rollable and foldable film-on-foil electronics. Appl Phys Letts 74(8):1177–1179
7. Miyasaka M, Hara H, Karaki N, Inoue S, Kawai H, Nebashi S (2008) Technical obstacles to thin film transistor circuits on plastic. Jpn J Appl Phys 47(6):4430–4435
8. Cherenak KH, Kattamis AZ, Hekmatshoar B, Sturm JC, Wagner S (2007) Amorphous-silicon thin film transistors at 300 °C on a free-standing foil substrate of clear plastic. IEEE Electron Device Lett 28(11):1004–1006
9. Long K, Cheng I-C, Kattamis A, Gleskova H, Wagner S, Sturm JC (2007) Amorphous-silicon thin-film transistors made at 280 °C on clear-plastic substrates by interfacial stress engineering. J SID 15(3):167–176
10. Young ND, Trainor MJ, Yoon S-Y, McCulloch DJ, Wilks RW, Pearson A, Godfrey S, Green PW, Roosendaal S, Hallworth E (2003) Low temperature poly-Si on flexible polymer substrates for active matrix displays and other applications. Mat Res Soc Symp Proc 769:17–28
11. Ito H, Oka W, Goto H, Umeda H (2006) Plastic substrates for flexible displays. Jpn J Appl Phys, 45(5B), 4325–4329
12. Young ND, Bunn RM, Wilks RW, McCulloch DJ, Deane SC, Edwards MJ, Harkin G, Pearson AD (1997) Thin-film-transistor and diode-addressed AMLCDs on polymer substrates. J SID 5(3):275–281
13. Kuo P-C, Jamshidi-Roudbari A, Hitalis M (2009) Electrical characteristics and mechanical limitation of polycrystalline silicon thin film transistor on steel foil under strain. J Appl Phys 106:114502-1–114502-5
14. Wagner S, Gleskova H, Cheng I-C, Sturm JC, Suo Z (2005) Mechanics of TFT technology on flexible substrates. In: Crawford GP (ed) Flexible flat panel displays, Wiley Ltd., Chichester, England
15. Gleskova H, Wagner S, Suo Z (1999) Failure resistance of amorphous silicon transistors under extreme in-plane strain. Appl Phys Letts 75(19):3011–3013
16. Han L, Song K, Mandlik P, Wagner S (2010) Ultra flexible amorphous silicon transistors made with a resilient insulator. Appl Phys Letts 96:042111-1–042111-3
17. Sekitani T, Iba S, Kato Y, Noguchi Y, Someya T, Sakurai T (2005) Ultra flexible organic field-effect transistors embedded at a neutral strain position. Appl Phys Letts 87:173502-1–173502-3
18. Cheng I-C, Kattamis A, Long K, Sturm JC, Wagner S (2005) Stress control for overlay registration in a-Si:H TFTs on flexible organic-polymer-foil substrates. J SID 13(7):563–568
19. Kattamis AZ, Cherenack KH, Hekmatshoar B, Cheng I-C, Gleskova H, Sturm JC, Wagner S (2007) Effect of SiNx gate dielectric deposition power and temperature on a-Si:H TFT stability. IEEE Electron Device Lett 28(7):606–608
20. Sazonov A, Nathan A, Murthy RVR, Chamberlain SG (2000) Fabrication of a-Si:H TFTs at 120 °C on flexible polyimide substrates. Mat Res Soc Symp Proc 558:375–380
21. He S, Nishiki H, Hartzell J, Nakata Y (2000) Low temperature PECVD a-Si:H TFT for plastic substrates. SID'00 Digest, 278–281
22. Sturm JC, Hekmatshoar B, Cherenack K, Wagner S (2009) Enabling mechanisms for a-Si TFT's with 100 year lifetimes compatible with clear plastic substrates. Proc 5th Internal TFT Conf, ITC'09, 9.1
23. Won SH, Hur JH, Lee CB, Nam HC, Chung JK, Jang J (2004) Hydrogenated amorphous silicon transistor on plastic with an organic insulator. IEEE Electron Device Lett 25(3):132–134
24. Jang J, Won SH, Kim BS, Hong MP, Chung KH (2005) High-resolution full-color flexible TFT LCDs based on amorphous silicon. In: Crawford GP (ed) Flexible flat panel displays, Wiley, Ltd., Chichester, England
25. Won SH, Lee CB, Nam HC, Jang J, Chung JK, Hong M, Kim BS, Lee YU, Yang SH, Huh JM, Chung K (2003) A high-resolution full color TFT-LCD on transparent plastic. SID 03 Digest, 992–995

26. Kattamis AZ, Cheng I-C, Hong Y, Wagner S (2006) Amorphous silicon 2-TFT pixel circuits on stainless steel foils. Mater Res Soc Symp, 910
27. Afentakis T, Hatalis M, Voutsas AT, Hartzell J (2006) Design and fabrication of high-performance polycrystalline silicon thin-film transistor circuits on flexible steel foils. IEEE Trans ED-53(4), 815–822
28. O'Rourke SM, Venugopal SM, Raupp GB, Allee DR, Ageno S, Bawolek EJ, Loy DE, Kaminski JP, Moyer C, O'Brien B, Long K, Marrs M, Bottesch D, Dailey J, Trujillo J, Cordova R, Richards M, Toy D, Colaneri N (2008) Active matrix electrophoretic displays on temporary bonded stainless steel substrates with 180 °C a-Si:H TFTs. SID 08 Digest, 422–424
29. Ma R, Rajan K, Silvernail J, Urbanik K, Paynter J, Mandlik P, Hack M, Brown JJ, Yoo JS, Kim Y-C, Kim I-H, Byun S-C, Jung S-H, Kim J-M, Yoon S-Y, Kim C-D, Kang I-B, Tognoni K, Anderson R, Huffman D (2009) Wearable 4-inch QVGA full color video flexible AMOLEDs for rugged applications. SID 09 Digest, 96–99
30. French I, George D, Kretz T, Templier F, Lifka H (2007) Flexible displays and electronics made in AM-LCD facilities by the EPLaR process. SID'07 Digest, 1680–1683
31. French I (2009) Flexible e-book displays produced in standard TFT and module factories. SID Inf Disp 25(12):8–11
32. Nikulin, IV, Hwang TH, Jeon HI, Kim SI, Roh NS, Shin SS (2007) Near 100 °C low temperature a-Si TFT array fabrication on flexible PES and PEN substrates. Proc 3rd Internal TFT Conf, ITC'07, 64–67
33. Lee W, Hong M, Hwang T, Kim S, Hong WS, Lee SU, Jeon HI, Kim SI, Baek SJ, Kim M, Nikulin I, Chung K (2006) Transmissive 7 VGA a-Si TFT plastic LCD using low temperature process and holding spacer. SID Digest 06:1362–1364
34. Hwang TH, Lee W, Hong WS, Kim SJ, Kim SI, Roh NS, Nikulin I, Choi JY, Jeon HI, Hong SJ, Lee JK, Han MJ, Baek SJ, Kim M, Lee SU, Shin SS (2007) 14.3 inch active matrix-based plastic electrophoretic display using low temperature processes. SID Digest 07:1684–1685
35. Souk JH, Roh NS (2009) Processing flexible displays. SID 09 Digest, 622–624
36. Ma R, Hack M, Brown JJ (2010) Flexible AMOLEDs for low-power, rugged applications. SID Inf Disp 26(2):8–14
37. Gregg A, York L, Strnad M (2005) Roll-to-roll manufacturing of flexible displays. In: Crawford GP (ed) Flexible flat panel displays, Wiley Ltd., Chichester, England
38. Kim H-J, Almanza-Workman M, Garcia B, Kwon O, Jeffrey F, Braymen S, Hauschildt J, Junge K, Larson D, Stieler D, Chaiken A, Cobene B, Elder R, Jackson W, Jam M, Jeans A, Luo H, Mei P, Perlov C, Taussig C (2009) Roll-to-roll manufacturing of electronics on flexible substrates using self-aligned imprint lithography (SAIL). J SID 17(11):963–970
39. Gleskova H, Wagner S, Soboyejo W, Suo Z (2002) Electrical response of amorphous silicon thin-film transistors under mechanical strain. J Appl Phys 92(10):6224–6229
40. Won SH, Chung JK, Lee CB, Nam HC, Hur JH, Jang J (2004) Effect of mechanical and electrical stresses on the performance of an a-Si:H TFT on plastic substrate. J Electrochem Soc 151(3):G167–G170
41. Thompson SE, Sun G, Choi YS, Nishida T (2006) Uniaxial-process-induced strained-Si: extending the CMOS roadmap. IEEE Trans ED-53(5), 1010–1020
42. Young ND, McCulloch DJ, Bunn RM, French ID, Gale IG (1998) Low temperature poly-Si on glass and polymer substrates. Proc Asia Display'98, 83–93
43. Higashi S, Abe D, Hiroshima Y, Miyashita K, Kawamura T, Inoue S, Shimoda T (2002) High-quality SiO2/Si interface formation and its application to fabrication of low-temperature-processed polycrystalline Si thin-film transistor. Jpn J Appl Phys, 41(6a), 3646–3650
44. Maiolo L, Pecora A, Fortunato G, Young ND (2006) Low-temperature electron cyclotron resonance plasma-enhanced chemical-vapor deposition silicon dioxide as gate insulator for polycrystalline silicon thin-film transistors. J Vac Sci Technol, A 24(2):280–285
45. Mariucci L, Fortunato G, Bonfiglietti A, Cuscuná M, Pecora A, Valletta A (2004) Polysilicon TFT structures for kink-effect suppression. IEEE Trans ED-51(7), 1135–1142

46. Young ND, French ID, Trainor MJ, Murley DT, McCulloch DJ, Wilks RW (1999) LTPS for AMLCD on glass and polymer substrates. Proc IDW'99, 219–222
47. Gosain DP, Noguchi T Usui S (2000) High mobility thin film transistors on a plastic substrate at a processing temperature of 110 °C. Jpn J Appl Phys, 39(3A/B), L179–L181
48. Troccoli MN, Roudbari AJ, Chuang T-K, Hatalis MK (2006) Polysilicon TFT circuits on flexible stainless steel foils. Solid-State Electron 50:1080–1087
49. Inoue S, Utsunomiya S, Saeki T, Shimoda T (2002) Surface-free technology by laser annealing (SUFTLA) and its application to poly-Si TFT-LCDs on plastic film with integrated drivers. IEEE Trans ED-49(8), 1353–1360
50. Miyasaka M (2007) Flexible microelectronics becoming a reality with SUFTLA transfer technology. J SID 15(7):479–484
51. Takechi K, Eguchi T, Kanoh H, Ito T, Otsuki S (2005) High-rate glass etching for transferring polycrystalline silicon thin-film transistors to flexible substrates. IEEE Trans Semicond Manuf 18(3):384–389
52. Takechi K, Eguchi T, Kanoh H, Kanemasa K, Otsuki S (2007) Transfer process for thermally stable large-size TFT flexible substrates. IEEE Trans Semicond Manuf 20(1):20–25
53. Pecora A, Maiolo L, Cuscuna M, Simeone D, Minotti A, Mariucci L, Fortunato G (2008) Low-temperature polysilicon thin film transistors on polyimide substrates for electronics on plastic. Solid-State Electron 52:348–352
54. Fortunato G, Cuscunà M, Maiolo L, Maita F, Mariucci L, Minotti A, Pecora A, Simeone D, Valletta A, Bearzotti A, Macagnano A, Pantalei S, Zampetti E (2009) Flexible electronics based on polysilicon thin film transistor. Proc IMID 2009 Digest, 258–261
55. French I, McCulloch D, Boerefijn I, Kooyman N (2005) Thin plastic electrophoretic displays fabricated by a novel process. Proc SID 05 Digest, 1634–1637
56. Smeys P, Griffin PB, Rek ZU, De Wolf I, Saraswat KC (1999) Influence of process-induced stress on device characteristics and its impact on scaled device performance. Trans IEEE ED-46(6), 1245–1252
57. Wang T-J, Ko C-H, Chang S-J, Wu S-L, Kuan T-M, Lee W-C (2008) The effects of mechanical uniaxial stress on junction leakage in nanoscale MOSFETs. Trans IEEE ED-55(2), 572–577
58. Sun Y, Thompson SE, Nishida T (2007) Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors. J Appl Phys, 101, 104503-1–104503-22
59. Thompson SE, Sun G, Choi YS, Nishida T (2006) Uniaxial-process-induced strained-Si: extending the CMOS roadmap. IEEE Trans ED-53(5), 1010–1020
60. Cheon JH, Bae JH, Jang J (2008) Mechanical stability of poly-Si TFT on metal foil. Solid-State Electron 52:473–477
61. Sekitani T, Kato Y, Iba S, Shinaoka H, Someya T, Sakurai T, Takagi S (2005) Bending experiment on pentacene field-effect transistors on plastic films. Appl Phys Letts, 86, 073511-1–073511-3
62. Han SH, Kim YH, Lee SH, Choi MH, Jang J, Choo DJ (2008) Stable organic thin-film transistor in a pixel for plastic electronics. Org Electron 9(6):1040–1043
63. Yagi I, Hirai N, Miyamoto Y, Noda M, Imaoka A, Yoneya N, Nomoto K, Kasahara J, Yumoto A, Urabe T (2008) A flexible full-color AMOLED display driven by OTFTs. J SID 1691), 15–20
64. Zhou L, Wanga A, Wu S-C, Sun J, Park S, Jackson TN (2006) All-organic active matrix flexible display. Appl Phys Lett, 88, 083502-1–083502-3
65. Nakajima Y, Takei T, Tsuzuki T, Suzuki M, Fukagawa H, Yamamoto T, Tokito S (2009) Fabrication of 5.8-in. OTFT-driven flexible color AMOLED display using dual protection scheme for organic semiconductor patterning. J SID, 17(8), 629–614
66. Gelinck GH, Huitema HEA, Van Veenendaal E, Cantatore E, Schrijnemakers L, Van Der Putten JB, Geuns TCT, Beenhakkers M, Giesbers JB, Huisman B-H, Meijer EJ, Benito EM, Touwslager FJ, Marsman AW, Van Rens BJ, De Leeuw DM (2004) Flexible active-matrix displays and shift registers based on solution-processed organic transistors. Nat Mater 3:106–110

67. Burns SE, Reeves W, Pui BH, Jacobs K, Siddique S, Reynolds K, Banach M, Barclay D, Chalmers K, Cousins N, Cain P, Dassas L, Etchells M, Hayton C, Markham S, Menon A, Too P, Ramsdale C, Herod J, Saynor K, Watts J, von Werne T, Mills J, Curling CJ, Sirringhaus H, Amundson K, McCreary MD (2006) A flexible plastic SVGA e-paper display. SID 06 Digest, 74–76
68. Burns SE (2010) Flexible displays made with plastic electronics. SID Inf Disp 2:16–19
69. Inoue S, Ohshima H, Shimoda T (2002) Analysis of degradation phenomenon caused by self-heating in low-temperature-processed polycrystalline silicon thin film transistors. Jpn J Appl Phys, 41(11a), 6313–6319
70. Kao S-C, Zan H-W, Huang J–J, Kung B-C (2010) Self-heating effect on bias-stressed reliability for low-temperature a-Si:H TFT on flexible substrate. IEEE Trans ED-57(3), 588–593
71. Karim KS, Nathan A, Hack M, Milne WI (2004) Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs. IEEE Electron Dev Letts 25(4):188–190
72. Wang L, Fjeldly TA, Iniguez B, Slade HC, Shur M (2000) Self-heating and kink effects in a-Si:H thin film transistors. Trans IEEE, ED-47(2), 387–397