Chapter 10
Organic TFTs

Abstract A large number of organic TFT materials now display carrier mobility values approaching, or exceeding, those of a-Si:H, and this has stimulated considerable interest in using them for low cost, flexible substrate applications, such as RFID tags, and e-reader displays. This chapter reviews work in this field, and starts by introducing some of the key organic chemistry concepts, which underpin the semiconducting behaviour of these materials. Other topics include molecular ordering, carrier transport, TFT architecture, and the deposition of both semiconductor and dielectric materials, together with their properties. These are linked to device behaviour, with a focus on the key material and design issues, which currently limit TFT performance, such as metal/organic contacts, and ambient and bias stability effects.

10.1 Introduction

The commercial interest in organic TFTs, OTFTs, for display applications started in the early-1990s, when the carrier mobility in small molecule material, particularly pentacene, exceeded 0.1 cm^2/Vs, and began to approach the values of 0.5–1.0 cm^2/Vs obtained in a-Si:H. Since that time, the performance of organic materials has continued to improve, and, when viewed on a 20 year timescale, increases in carrier mobility of several orders of magnitude have been achieved, with the highest values now in excess of 10 cm^2/Vs, as shown in Fig. 10.1 [1]. Four classes of material are labelled in this diagram, but these include sub-divisions of the two main families, which are small molecule (sometimes referred to as oligomer) and long molecule (normally referred to as polymer) conjugated semiconductors. The further sub-division is amongst the small molecule types, where they are specified as vacuum deposited, solution processed and single crystal. (The interest in single crystal organic semiconductors has largely been to

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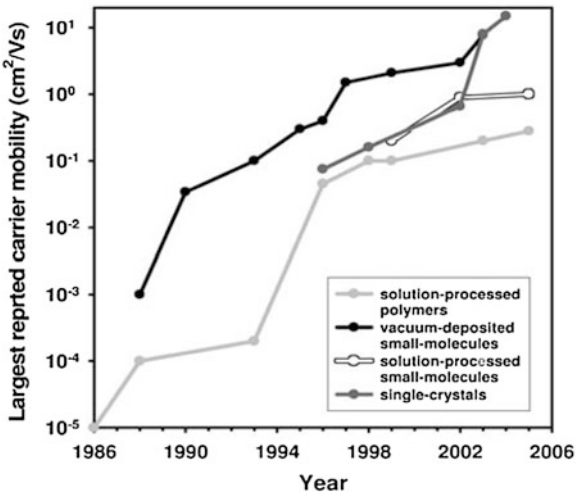

Fig. 10.1 Changes in carrier mobility in organic TFTs between 1986 and 2006. (Reproduced from [1] with permission of John Wiley & Sons, Inc)

identify ultimate performance limits. This type of material has been recently reviewed [2], and will not be discussed further here). The polymer samples are usually solution processed, which means that their deposition is from a liquid phase by printing, casting or spin-coating. This is expected to be the most cost-effective approach to film formation, and underlies the interest in polymers in spite of their lower mobility, as seen in Fig. 10.1.

Although the attainment of a useful mobility is essential for the currently envisaged commercial applications, the mobility alone is not sufficient for organic materials to be seen as potential replacements for a-Si:H. Indeed, there is no likelihood of them challenging the mainstream technology of a-Si:H TFTs on glass in the near future. Rather, the interest in them lies in their compatibility with a flexible substrate technology, using inexpensive polymer substrates, in order to produce light-weight, portable displays, which can be contoured, folded or rolled. Commonly used plastic substrates in this work are polyethylene naphthalate (PEN), and polyethylene terephthalate (PET), which, in their heat stabilised forms, have maximum handling temperatures of 200 °C and 150 °C, respectively. Further properties of these, and other polymer substrates, are shown in Table 11.1. In addition, the challenges in using flexible substrates are discussed in Sect. 11.2, in which it is shown that the issues of maximum processing temperature, the mismatch in coefficients of thermal expansion between the substrate and the layers on them, and general substrate flexing are more acute with the inorganic TFT technologies. Thus, these topics are expected to be more easily manageable with a TFT technology which uses the less rigid, and better physically matched, organic TFT materials. For example, suitably capped OTFT samples, which placed the TFTs in the neutral strain plane, have been reported with a minimum bending radius of 0.5 mm [3], and working displays have been demonstrated with a bending radius of 4 mm [4], as shown in Fig. 10.2.

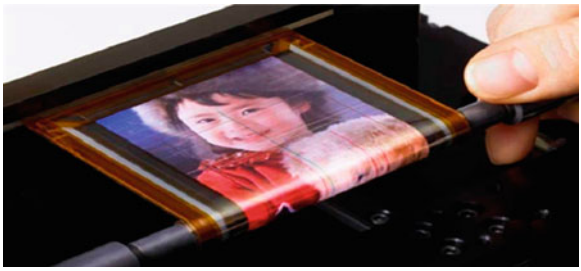

Fig. 10.2 Photograph of a flexible AMOLED display, driven by OTFTs, rolled around a 4 mm radius cylinder. (Reprinted from [4] with permission of SID)

There are now plentiful examples of OTFT research demonstrator displays on flexible substrates, using LCD [5], electro-phoretic, EPD [6–8], and OLED [4, 9, 10] media, as well as demonstration logic circuits [11–13]. The most obvious first application of OTFTs is in low cost RFID tags, and in AMEPDs (due to the reduced pixel drive current requirements). Some e-reader proto-products have been presented [6, 8], in which the ultimate aim is a compact device containing a rollable/foldable screen [8], and the first product, a rigid-framed e-reader for educational use, was announced in late 2011 [14].

In common with other TFT technologies, a mature technology should deliver not merely basic device performance, with an acceptable carrier mobility, leakage current and threshold voltage, but also good device uniformity and reliability. These properties should be delivered in a cost-effective, reproducible process, and offer the prospect of increased device/function integration. Of all the TFT technologies, the OTFT technology is currently the most immature in these respects, with no clear consensus on the preferred organic material, gate dielectric and process flow, but it is driven by the prospect of a low-cost, flexible substrate technology, with laboratory demonstrators and the first product highlighting the potential of this approach.

In another important respect, the activity covered in this chapter is different from the preceding TFT chapters, in that they dealt with just one semiconductor material for the TFT channel. In contrast, the research programmes into OTFTs have investigated an extensive range of different organic materials, both for the TFT channel, and, to a lesser extent, for the gate dielectric and contact metals. Moreover, continued development of new and improved molecular structures is an on-going activity, and recent reviews [15–17] have given a detailed overview of the range of materials examined. Similar specialist coverage of different materials is less appropriate for this book. Instead, the following sections of this chapter will focus on the broader background concepts and issues in using organic materials to fabricate TFTs, and with examples drawn from the polymer and oligomer materials of current interest.

Sections 10.2.1 and 10.2.2 are an elementary introduction to some of the background organic chemistry concepts routinely employed in the study of organic materials for TFTs, and cover the role of the molecular and orbital structure of the material in determining its semiconductor behaviour. Section 10.2.3 reviews the role of structural organisation in optimising TFT performance, including the

growth of ordered domains and poly-crystalline regions. Organic semiconductors are usually prepared undoped, and n- and p-channel behaviour is partially determined by the particular metal used for the contacts, and, specifically, by the alignment of the metal work function and the carrier bands in the semiconductor. Metal/organic contacts have been widely studied, and an overview of the key issues for TFTs is presented in Sect. 10.2.4. Finally, Sect. 10.2.5 reviews the current understanding of the carrier transport mechanisms in these materials.

Section 10.3 discusses the architecture of OTFTs, and Sect. 10.4 deals with the materials and processing procedures used in TFT fabrication. The materials coverage includes sub-sections on the semiconductors, the gate dielectrics and the metallisation options. There is also a sub-section on novel processing schemes, which exploit the self-organising properties of these materials. These techniques differ radically from the more conventional TFT fabrication process of layer-by-layer definition by photo-lithography and etching.

The electrical characteristics of OTFTs are discussed in Sect. 10.5, with an overview of the performance parameters from a range of common semiconductors, but with a more detailed focus on contact and series resistance effects, which play a major role in determining overall TFT behaviour. Finally, the ambient and bias stability issues of OTFTs are reviewed in Sect. 10.6.

10.2 Background and Materials

10.2.1 Conjugated Molecular Systems

The materials used in OTFTs are conjugated molecular systems, which means that they have alternating single and double carbon–carbon bonds, and their molecular π-bonding orbitals are responsible for the ability of the material to transport charge. A simple example of a conjugated molecule is the benzene ring shown in Fig. 10.3a [18], which is a building block for a number of important OTFT compounds. The figure shows the chemical structure of benzene, C_6H_6, which is a planar ring with the alternating double bonds between the carbon atoms. Also shown are the two commonly employed symbols, which are used to represent the benzene ring in more complex molecules, such as those shown in Fig. 10.3b, c. Figure 10.3b is an acene structure, which consists of a number of linearly fused benzene rings, giving a rod-like molecular structure, and the subscript n, in the diagram, refers to the number of repeating units of the bracketed ring structure. A specific example of this structure is the pentacene molecule, consists of five rings, as shown in Fig. 10.3c, and this is the most widely studied small molecule material, yielding high mobility p-channel TFTs.

A similar planar ring structure molecule is thiophene, C_4H_4S, which is shown in Fig. 10.3d, together with its symbolic representation. Thiophene is a building block of another group of OTFT materials, consisting of both small molecule

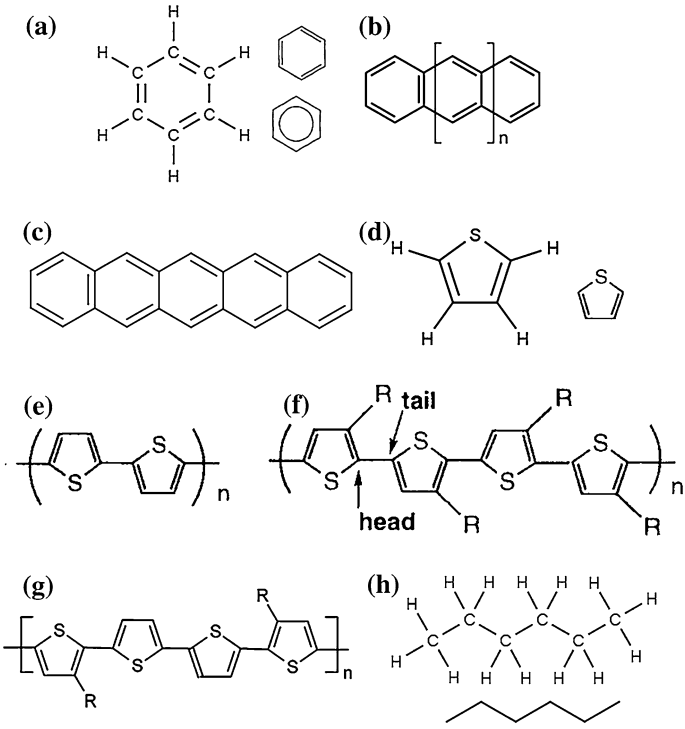

Fig. 10.3 Chemical structure of **a** benzene ring, and its symbolic representations, **b** acene molecule, **c** pentacene, **d** thiophene, and its symbolic representation, **e** polythiophene, **f** regio-regular poly(3-hexylthiophene), P3HT, **g** poly(3,3″ dialkylquaterthiophene), PQT-12, and **h** hexane linear chain molecule, and its symbolic representation. (**f** Reproduced from [22] with permission of John Wiley & Sons, Inc, and **g** Reprinted with permission from [21]. Copyright (2004) American Chemical Society)

oligothiophenes [19], as well as the polymers polythiopene and its derivatives poly(3-hexylthiophene), P3HT [20], and poly(3,3‴ dialkylquaterthiophene), PQT-12 [21], shown in Fig. 10.3e–g, respectively. The substituted side chains, R, on the basic thiophene molecule are alkyls, C_nH_{2n+1}, which are radicals of the alkane group, C_nH_{2n+2}.These are single-bond chains of carbon and hydrogen, and the six carbon molecule, hexane, C_6H_{14}, is illustrated in Fig. 10.3h. (This figure also shows its conventional symbolic representation, although a simple straight line, plus the symbol R, is also widely used for this and other substituents, as in Fig. 10.3f, g). For solution processing of the polymers, alkanes with six or more carbon atoms are favoured for the substituting alkyl groups on polythiophene [21, 22], as seen by the use of hexyl, C_6H_{13}, in P3HT, and dodecyl, $C_{12}H_{25}$, in PQT-12.

The long-range organisation of the molecular structures is essential to give good TFT performance, and this is discussed in Sect. 10.2.3.

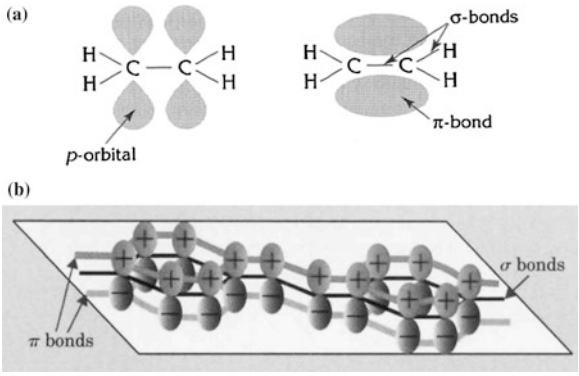

Fig. 10.4 **a** pi molecular orbital formation in an ethene molecule (Reproduced by permission of Hodder Education from [18], copyright (2003)), and **b** schematic illustration of the extended pi-orbitals in a conjugated molecular system (Reprinted with permission from [23]. Copyright (2005) American Institute of Physics)

10.2.2 Molecular Bonding

The isolated carbon atom has two electrons in the 2s orbital and two distributed in the three 2p orbitals, and, when carbon atoms are brought together to form a molecule containing a *double bond*, these four atomic orbitals are converted into three hybrid sp^2 orbitals, leaving one remaining 2p orbital. The three hybrid sp^2 orbitals form covalent bonds with the adjacent atoms, defined by the molecular σ bonding-orbital in the plane of the atoms, and with the 2p atomic orbitals perpendicular to this plane. The overlapping 2p-orbitals, on adjacent atoms in the molecule, form a molecular π-orbital [18], as shown for the simple double bond molecule, ethene, C_2H_4, in Fig. 10.4a. The π-orbital only forms where there is a σ-orbital, and double bonds are composed of σ and π orbitals. For a conjugated molecule, the π-orbital delocalises its electrons within the molecule, or along a conjugated polymer backbone, as shown schematically in Fig. 10.4b [23]. Hence, the π-orbitals support the flow of charge carriers within the material, and, in a solid, the filled π-bonding orbitals form the highest occupied molecular orbital, HOMO, and the empty π-anti-bonding orbitals form the lowest unoccupied molecular orbital, LUMO [23]. These can be thought of as corresponding to the valence and conduction bands in conventional inorganic semiconductors, and are used in the same way to represent the band off-sets between the different constituents of a TFT structure [24].

10.2.3 Molecular Organisation

It has been widely demonstrated that there needs to be a high degree of structural order within the material, together with strong electronic coupling between adjacent molecules, to achieve effective charge transport and high performance TFTs. Hence, as discussed below, the favoured materials show regions of, at least, micro-crystallinity if not poly-crystallinity, in contrast with less favoured, low

mobility amorphous materials [28]. Whilst this structural distinction is widely observed, it would appear not to be universal, as high performance n-channel TFTs have been reported in amorphous material [25]. Although there is a strong theoretical framework underpinning molecular engineering and materials development [26], it is apparent that a full understanding of the correlation between material structure and device performance has not yet been achieved [2]. In the remainder of this section, examples are given of the structural order engineered into both oligomer and polymer materials.

High performance P3HT OTFTs [27, 28] have been achieved with regio-regular molecules, in which there is predominantly head-tail, HT, coupling of the adjacent thiophene rings (at the 2 and 5 positions), with the hexyl substituent, R, in the number 3 position on the ring [22]. This is illustrated in Fig. 10.3f. The HT coupling produces molecules with a torsional twist of $<10°$, indicating good co-planarity, which is required for efficient π-orbital coupling between adjacent molecules. Alternative couplings, such as head-head (the 2, 2 positions), can lead to severe twisting of the molecule by up to 40°, and degraded π-orbital conduction [22]. Detailed discussion of the chemical synthesis of thiophene polymers can be found in Ref. [22], but the topic itself is beyond the scope of this book.

The regio-regular P3HT molecules, with a high HT content, self-organise into micro-crystalline domains containing close packed lamellae, which are vertically aligned to the substrate surface, as shown in Fig. 10.5a [28]. In contrast, in films with a low concentration of HT coupling, the lamellae are oriented parallel to the substrate surface. When these structures were used in OTFTs, the field effect mobility was up to 10^3 times higher in the high HT-content films, as illustrated, in Fig. 10.5b, by the dependence of the field effect mobility on the percentage of HT coupling [27]. This work also demonstrated the large anisotropy in mobility within these films, with the most effective carrier transport being by inter-chain, π–π coupling in these π-stacked materials. Hence, not only is molecular ordering within the film important, but as significant is the orientation of the molecular stacking with respect to the direction of channel current flow. It has also been demonstrated that the formation of vertically aligned molecules can be enhanced by the prior deposition of self-assembled mono-layers, SAMs, onto the substrate surface [29]. As will be seen in Sect. 10.4, the use of SAMs is a widely employed technique for controlling the orientation of organic semiconductor molecules, and can be regarded as comparable to the use of alignment layers in LCD cells to control the alignment of the LC molecules [30].

Another thiophene based molecule, regio-regular PQT-12 (see Fig. 10.3g), has also been demonstrated to self-assemble in an ordered vertical lamellar structure, which is similar to the P3HT discussed above. The stacking is shown schematically in Fig. 10.5c [21], and, for TFT samples, the gate oxide surface was coated with a film of octyltrichlorosilane, OTS, before spin coating with the polymer. X-ray diffraction of the as-spun films showed a loosely packed lamellar structure, but, after annealing at 135 °C, a more highly ordered lamellar stack was observed, oriented perpendicular to the substrate surface. TEM examination of these films showed an inter-stack spacing of 3.7 Å [21]. The hole mobility was 0.14 cm^2/Vs,

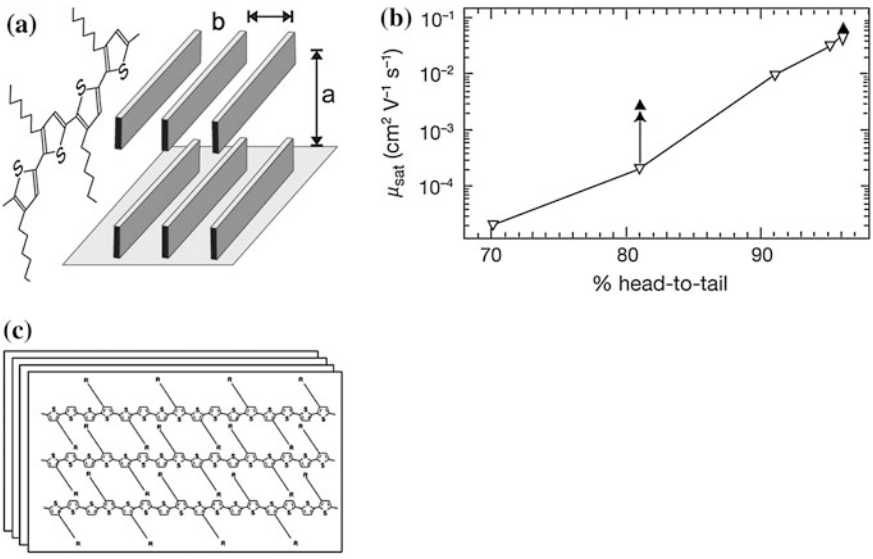

Fig. 10.5 **a** Lamellar molecular ordering of regio-regular P3HT (Reproduced from [28] with permission of John Wiley & Sons, Inc). **b** variation of hole mobility with fractional head–tail coupling in P3HT (Reprinted by permission from Macmillan Publishers Ltd: Nature [27], copyright (1999)), and **c** lamellar molecular ordering of PQT-12 (Reprinted with permission from [21]. Copyright (2004) American Chemical Society)

which is comparable to well ordered P3HT films, but the PQT-12 samples showed much less hysteresis during measurements, and much better long-term ambient stability. This was attributed to the larger ionisation potential of PQT-12, which reduced its susceptibility to oxidation. Device performance issues are discussed in greater detail in Sects. 10.4, 10.5 and 10.6.

The most widely studied small molecule material is pentacene [26], which, under well controlled vacuum evaporation conditions, forms a polycrystalline film on the substrate surface. The grain structure is triclinic, with the (001) plane parallel to the substrate surface [15], and the molecular alignment follows an edge-to-face ('herringbone'), intermolecular stacking pattern. This is one of the characteristic structures for acenes [26], and is shown in Fig. 10.6 [31]. Figure 10.6a shows that the rigid pentacene molecules are arranged in vertically stacked layers, with a pitch of $\sim$15.4 Å, and, within each layer, the molecules are at an angle of $\sim 84 \pm 0.5°$ to the substrate surface, depending upon the termination of the surface [32]. The inter-molecular 'herringbone' pattern, within each layer, is more clearly seen in the image in Fig. 10.6b, which is viewed parallel to the long-axis of the molecule. Given the near vertical alignment of the molecules on the substrate surface, the structure is often schematically illustrated in TFT cross-sections, as shown by Fig. 10.6c. Although single crystal pentacene has been studied, the material is usually poly-crystalline in its thin film form, and an example of the role of grain size on carrier mobility is shown in Fig. 10.6d [33].

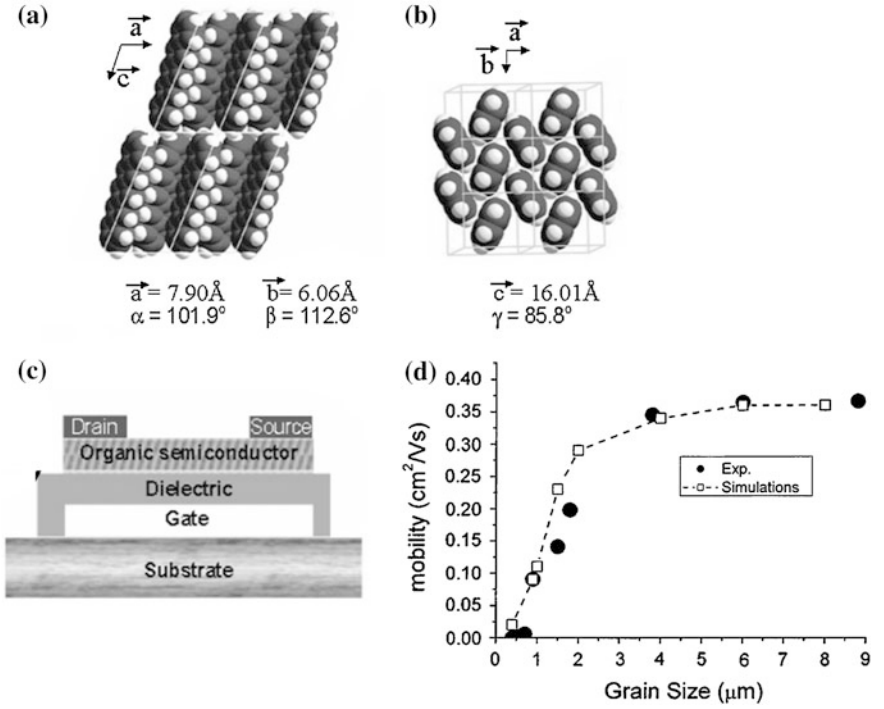

Fig. 10.6 Crystalline structure of pentacene, viewed **a** along, and **b** perpendicular to the plane of the substrate surface. **c** Schematic TFT representation showing the vertically stacked planes of near-vertically aligned molecules (Reprinted with permission from [31]. Copyright (2003) by the American Physical Society), and **d** variation of field effect mobility with pentacene grain size, where the *dashed line* is from a 2-D device model with grain-boundary trapping. (Reprinted with permission from [33]. Copyright (2005) American Institute of Physics)

In his work, the grain size was controlled by varying the pentacene evaporation rate, and was assessed by atomic force microscopy. The TFT geometry was inverted staggered with an SiO_2 gate dielectric layer, and the hole field effect mobility was found to increase with increasing grain size (up to a maximum value of 0.35 cm^2/Vs). The influence of grain size was attributed to grain boundary trapping effects, as shown by the GB modelling of the data [33]. As with the polythiophenes, the carrier transport process in pentacene films is also essentially two-dimensional, by virtue of the better electronic coupling between molecules within a layer, rather than between layers [34].

10.2.4 Metal/Organic Contacts

The organic channel materials are undoped, and the distinction between n-channel and p-channel devices is determined by which carrier is injected from the source

contact. In other words, if the work function of the source metal is close to the LUMO level, electrons will be more easily injected (giving n-channel operation), and, conversely, if it is closer to the HOMO level, holes will be preferentially injected, giving p-channel behaviour. Hence, a key consideration in matching the metal to the organic semiconductor, to achieve n- or p-channel operation, is the relative displacement of the metal work function from the HOMO or the LUMO levels. However, it should be noted that whilst a good injecting contact is necessary for both p- and n-channel device operation, it alone is not sufficient to produce high performance, stable devices, where impurities and carrier trapping will be additional determinants of device behaviour [35]. Indeed, the fabrication of high quality n-channel devices has proven to be more difficult to achieve than for p-channel devices [25, 35], particularly due to electron trapping effects when SiO_2 was used as the gate dielectric [36]. Because of this, well matched complementary p- and n-channel TFTs, for low-power digital circuits, have not been available until relatively recently [25, 37]. The issues with the development of high performance n-channel TFTs are discussed further in Sect. 10.4.3.

In view of the importance of the metal/organic semiconductor contact, it has been extensively studied [24, 38–40]. The HOMO/LUMO energy band representation of the material is particularly useful in considering the contact, as illustrated in Fig. 10.7a, b [39]. Figure 10.7a shows the simple alignment of the metal and the semiconductor vacuum levels in the Schottky-Mott limit. The hole injection barrier, ϕ_h, is then given by the difference between the metal work function, Φ_M, and the semiconductor ionisation energy, IE, and the electron injection barrier, ϕ_e, by the difference between Φ_M and the electron affinity, EA. With knowledge of these values, an appropriate choice of metal may, in principle, be made. Unfortunately, practical systems rarely accord with this simple diagram, irrespective of whether the materials are prepared in UHV [39], or under more realistic conditions, such as air exposure of the metal prior to the deposition of the organic material [24, 38]. Usually, a dipole barrier, Δ, is found at the metal/organic, MO, interface, as shown in Fig. 10.7b, and this may be either positive or negative, resulting in an offset of the work function from the location predicted by the direct alignment of the vacuum levels. In the example shown, the effect of the dipole barrier is to change the metal from a hole injector to an electron injector. Moreover, the metal work function itself is sensitive to its environment, and care is needed in using the text book values. For example, gold is widely used as a contact metal in OTFTs, and its work function is conventionally quoted as $\sim$5.1–5.2 eV [41], and this value is confirmed in the UHV cited work here [39]. However, exposing a gold film to air, or rinsing it in an organic solvent, produced a dipole barrier of 0.7 eV, giving an effective Au work function (the energy gap between the gold Fermi level and the polymer vacuum level) of $\sim$4.5 eV, whereas ozone exposure increased it back to 5.2–5.5 eV [24]. The effective work function of $\sim$4.5 eV was also found following both the deposition of several different π-conjugated polymers onto gold, and UHV gold deposition onto pre-deposited films of the same polymers [24]. The dipole barrier found in this work, of

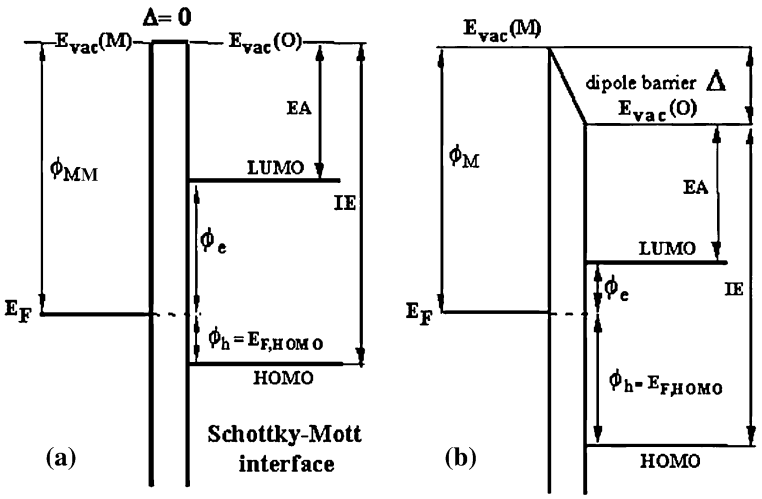

Fig. 10.7 HOMO and LUMO band diagram of an organic semiconductor showing the band offset with respect to a metal contact **a** in the Schottky–Mott limit, and **b** with the formation of a surface dipole layer. (Reproduced from [39] with permission of John Wiley & Sons, Inc)

$\sim$0.7 eV, is well established [38], although values as high as 1.08 eV have been quoted for the UHV deposition of pentacene onto gold [39].

The work function, ionisation energy and dipole barrier values quoted above were derived from ultraviolet photoelectron spectroscopy, UPS, measurements [24, 38, 39]. Most metals have been found to have a non-zero dipole barrier when in contact with organic materials, where the values recorded may be a function of the preparation and handling of the material [24]. Hence, the band diagram shown in Fig. 10.7b is the more appropriate representation of the contact than Fig. 10.7a.

Several models have been invoked to explain the dipole barriers [24, 38–40], including Fermi level pinning at interface states, charge exchange between the materials, and molecular mixing effects. The gold results, cited above, were explained by a more fundamental 'push-back' effect [24], in which the electron density from a clean metal surface decreases exponentially for a few angstroms beyond the surface, and charge neutrality is maintained by the corresponding deficit of negative charge within the material close to the surface. The electron tail produces a surface dipole, and a corresponding dipole potential energy, with which the work function scales. The larger the dipole potential energy (and the work function), the more polarisable the surface is, and the greater the effect of physisorbed layers pushing the electron tail back, and reducing the surface dipole (and the associated work function). Thus, metals like gold, with a large work function, are more sensitive to adsorbed films than low work function metals like Ca [24].

10.2.5 Carrier Transport

Carrier transport in OTFTs, as measured by the field effect mobility, is a function of several parameters [34]. The intrinsic factors include the molecular structure of the material, its ordering to promote good inter-molecular π–π coupling, and the molecular alignment on the substrate surface so that the high conduction direction is parallel to the plane of the TFT channel. The extrinsic factors include some or all of the following: the sample temperature, the lateral electric field, the free carrier density, and the carrier injection efficiency of the source and drain contact materials. The precise details of the charge transfer process, and the resultant mobility values, are still the subject of on-going theoretical study [34, 42]. However, the experimentally measured field effect mobility values are usually described as being limited by an inter-trap hopping process, in highly disordered material [43], or by multiple trapping and release, MTR, from localised defect states, in more ordered material [34, 42] (a process which was discussed in detail in Sect. 6.2.4), or by trapping effects at grain boundaries [33].

Hopping and MTR are thermally activated processes, and the field effect mobility, μ_{FE}, can be described by the generic equation:

$$\mu_{FE} = \mu_0 A \exp -(E_A/kT) \tag{10.1}$$

where μ_0 is the trap-free mobility for hopping, and, for MTR, it is the band mobility, with A proportional to the fractional division of carriers between those in traps and those in the band. As seen for inorganic semiconductors, such as a-Si:H and IGZO (Chaps. 6 and 9, respectively), the increase in trap filling with increasing gate bias leads to a greater relative increase in the free carrier density, and, thereby, increases the field effect mobility. The same has been observed with organic materials, whereby the mobility frequently displays a dependence on the carrier density, and, hence, on the gate bias above threshold. This has been empirically characterised as [44]:

$$\mu(V_G) = \mu_0 \left(\frac{V_G - V_T}{V_{AA}} \right)^{\gamma} \tag{10.2}$$

where the mobility enhancement factor, γ (>0), and V_{AA} were extracted from data fits. A similar power dependence on gate bias has also been theoretically demonstrated for both the MTR model and for hopping in more disordered materials [45]. The influence of this gate-bias-dependent mobility on the TFT current-voltage equations is discussed further in Sect. 10.5.1.

In addition, under lateral fields greater than $\sim 10^4$ V/cm, the mobility may be enhanced by the lateral field, and is attributed to emission barrier height lowering by the Poole-Frenkel effect [34, 46]:

$$\mu(F) \propto \mu_{F0}(T) \exp \beta(T) \sqrt{F} \tag{10.3}$$

where F is the lateral electric field, μ_{F0} is the zero field mobility, and the parameter β is proportional to 1/T. The mechanism of field enhancement is also temperature dependent, and, at cryogenic temperatures, it has been found to change from the thermally activated Poole-Frenkel process to a temperature-independent field emission process [46].

Some, or all, of these effects are seen in many OTFTs. For instance, Eq. 10.1 describes an increase in mobility with increasing temperature, which has been widely reported. Reference [42], for example, reviewed and confirmed this behaviour in more than a dozen oligomer and polymer materials, including both p- and n-channel TFTs, with room temperature carrier mobilities ranging from 0.02 to 0.42 cm^2/Vs. The thermal activation energy, E_A, showed an inverse correlation with the measured mobility, and was 20–30 meV and 40–70 meV for the higher and lower mobility devices, respectively [42]. When using the E_A values to extract μ_0, the μ_0 values were found to be quite similar, within the range 0.2–0.8 cm^2/Vs, and much closer than the wider spread in measured μ_{FE} values, which supported the MTR model of conduction. This thermal excitation of carriers from trapping states is a typical feature of most OTFTs, and distinguishes them from single crystal organic devices. For example, the mobility in crystalline rubrene TFTs had the opposite temperature dependence, and was found to decrease from $\sim$30 to 20 cm^2/Vs as the temperature was increased from 150 K to 300 K, due to increased phonon scattering [47].

In contrast to the widely observed thermal activation of the mobility in OTFTs, its lateral electric field enhancement appears to be less frequently reported, and this is most likely because the strength of the lateral field dependence decreases with the amount of order in the material [34]. For instance, the Poole-Frenkel effect has been reported at room temperature in small-grain pentacene TFTs (with a mobility of 3.3×10^{-3} cm^2/Vs) [48], in P3HT TFTs (with a mobility of 4.6×10^{-2} cm^2/Vs) [47], and in TIPS-pentacene TFTs (with a mobility of 1.1×10^{-4} cm^2/Vs) [47]. However, in other samples of TIPS-pentacene (with a room temperature mobility of $\sim$1.2 cm^2/Vs), the mobility was independent of the lateral field at temperatures above $\sim$200 K [49], and, at high fields, the mobility increased with reducing temperature. Hence, these high mobility TFTs displayed quite different temperature and field dependent behaviour compared with their more disordered and lower mobility counterparts.

10.3 OTFT Architecture

The device architectures which have been used in OTFTs are all non-self-aligned, and are broadly the same as those used for a-Si:H and AOS TFTs, although there is no sign of one particular architecture being identified as the optimum choice for OTFTs. Whereas the a-Si:H TFTs are almost always inverted staggered, both top and bottom gate architectures have been used in OTFTs. The three widely used device configurations are shown in Fig. 10.8 [15], and the nomenclature used is

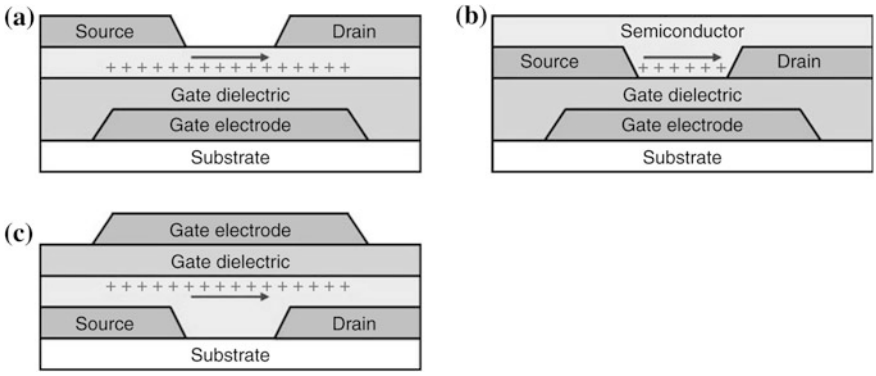

Fig. 10.8 OTFT architecture **a** *bottom* gate, *top* contact, BG/TC. **b** *bottom* gate, *bottom* contact, BG/BC, and **c** *top* gate, *bottom* contact TG/BC. (Reprinted with permission from [15])

slightly different from the inorganic TFTs, in that they are more often labelled bottom gate/top contact (BG/TC) rather than inverted staggered etc.

For much of the simple investigative work into the organic semiconductor layer itself, widespread use has been made of the bottom gated structure formed by using a doped silicon substrate as the gate electrode, and with its thermal oxide layer as the gate dielectric. The choice of the thermal oxide was implicitly assumed to provide a stable, high quality dielectric, such that all performance artefacts in the TFTs could be ascribed to the organic semiconductor itself. However, as will be seen in Sect. 10.4.3, SiO_2 films caused their own artefacts with respect to the performance of n-channel TFTs. Nevertheless, with the simple Si/SiO_2 structure, the main architectural choice is between top or bottom source/drain contacts, together with the issues related to the deposition and patterning of the source/drain contacts themselves. With bottom contacts, the metal can be deposited, and then defined using standard lithography techniques. This has the benefit that small channel lengths can be readily achieved, but the presence of the metal can interfere with the molecular alignment of the organic channel layer in the boundary region between the SiO_2 gate dielectric layer and the metal. Moreover, due to the large difference in conductivity of the OTFT channel and the metal contacts, the current flow from the channel to the contacts will be preferentially through the edge of the metal electrode in these BC structures [50]. In addition, molecular orientation discontinuities at this edge lead to contact resistance problems, as observed in pentacene TFTs with gold contacts [50, 51]. This effect is shown schematically in Fig. 10.9a [1], where the near vertically aligned molecules on the polar SiO_2 layer lose their order on the non-polar metal surface [50], and is responsible for the bright line at the SiO_2/Au boundary in the AFM image in Fig. 10.9b. The use of self-assembled mono-layers, SAMs, has been demonstrated to be effective in changing surface polarity, and increasing the overall polarity of the coated metal surface. This helps to maintain the same molecular ordering on the metal as on the SiO_2, giving the improved contrast uniformity at the SiO_2/Au

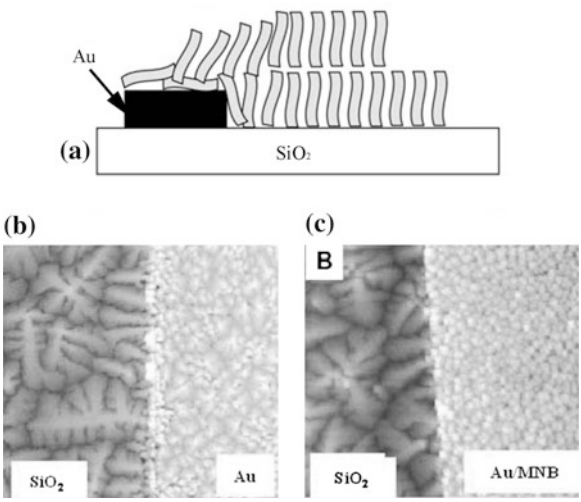

Fig. 10.9 **a** Illustration of pentacene misalignment at SiO_2/Au edges in BC TFTs, and AFM images of pentacene on SiO_2 and at the edge of the Au electrodes on **b** untreated surfaces, and **c** surfaces coated with a SAM. (Reproduced from [1] with permission of John Wiley & Sons, Inc)

edge in the AFM micrograph in Fig. 10.9c. Similar effects have been reported with 8 nm thick PMMA buffer layers [51]. The use of these layers has also been demonstrated to reduce contact resistance effects in BC TFTs [50, 51], and, because of the self-limiting thickness of SAMs, their direct contribution to series resistance is small [50].

For the simple process top-contact (BG/TC) OTFTs, a particular issue is potential damage to the organic layer both during the metal deposition, and in patterning it using conventional lithography, where the chemicals (photoresist, developer, etchant and solvent) may attack the organic layer [52]. To avoid these problems, it is common practice to use shadow-mask evaporation for the top contacts, thereby avoiding on-plate patterning. The major limitation with this approach is the minimum achievable channel length, which is likely to be of the order of $\sim$10–20 μm. Hence, this approach is not appropriate for devices with a channel length of just a few microns. Without the use of SAMs in BC devices, TC devices have usually given higher performance [50], but this difference has been substantially removed with SAMs in BC structures. One of the residual differences is then the additional series resistance in the BG/TC device due to the flow of current through the vertical thickness of the film from the channel at the bottom of the film to the contacts on the top of the film [53]. The impact on device performance of these architectural differences in BC and TC devices is discussed in greater detail in Sect. 10.5.3.

Another issue with the simplified device technology, irrespective of the contact position, is the patterning of the organic film itself. The patterning is to ensure that the channel width is sufficiently well defined to avoid the TFT performance artefacts discussed in Sect. 5.4.2, such as high leakage currents and erroneously large field effect mobility values. Given the problems associated with the lithography chemicals, active device area definition has been achieved, in some

instances, by simple scratch-isolation to form a trench around the device [19], or by shadow mask depositions [54]. However, more precise techniques have been implemented, which use lithography, but protect the organic film from direct chemical exposure. One example of this approach is to coat the structure with an organic solvent barrier, such as parylene [54], define it photolithographically, and use this film as a dry etch mask to pattern the organic layer beneath it. (This process is discussed further in Sect. 10.4.6). It has also been argued that some polymer semiconductors, such as poly(9,9-dioctylfluorene co-bithiophene), F8T2, do not need patterning, as its inherent conductivity is very low [55], but, further published work showed that island definition was used in high-quality demonstrator displays in order to obtain low-enough off-currents in the pixel TFTs [57].

The above non-lithographic techniques, using doped silicon substrates as a BG, have the merit of simplicity, and do not require extensive fabrication facilities, but are clearly only suitable for basic test devices, and are not appropriate for sophisticated demonstrator displays, nor for manufacturing. Nevertheless, these investigations have provided the background understanding of many materials, which have been incorporated into the range of contemporary demonstration displays, and which employ both top and bottom gates. An important consideration when comparing the processing of top and bottom gate structures, particularly with solution processing, is the solubility of the first deposited layer in the second, and this needs to be avoided by using orthogonal solvents for the different layers. Finally, a potential advantage of a TG structure, compared with a BG, is the automatic encapsulation of the active layer by the gate dielectric in the TG structures, and this can be used to suppress the ambient instability shown by many organic materials [56]. With BG structures, an encapsulant will need to be incorporated into the process if the channel material is susceptible to air-instabilities.

All three principal architectures have been used in demonstrators, as illustrated by the following examples: for oligomer-based displays, one group has implemented the BG/TC architecture for flexible AMOLED [4] and AMEPD [7] displays, whilst another group has used BG/BC for an AMOLED display [10]. For polymer materials, AMEPDs have been made with a TG/BC architecture [57], and high mobility, n-channel TFTs have been reported with the same TG/BC architecture [25, 58]. The processing conditions used to fabricate these devices are discussed in Sect. 10.4.6. The one architecture which has been little used is the TG/TC, almost certainly due to carrier injection problems.

10.4 Materials and Fabrication Processes

Sections 10.4.2–10.4.5 contain details of the materials used for the different device layers in OTFTs, in particular, the organic semiconductor, the gate dielectric and the metallisation layers, with the focus on the more widely studied materials, and those of current interest. The details include an overview of the deposition

procedures, and, as background to this, Sect. 10.4.1 briefly reviews solution processing techniques.

The most widely studied OS materials give p-channel TFT behaviour, and these are presented in Sect. 10.4.2, and, for clarity, the n-channel materials are discussed separately in Sect. 10.4.3. Examples of illustrative process flows for TFTs used in display demonstrators are shown in Sect. 10.4.6, and less conventional printing-based fabrication processes are reviewed in Sect. 10.4.7.

10.4.1 Solution Processing Techniques

One of the attractive features of OTFTs is the potential for low cost manufacturing by solution processing. Several techniques have been reported to implement this, including spin-coating, drop-casting, zone-casting, and printing, which are briefly reviewed below.

10.4.1.1 Spin-Coating

This process is commonplace for photo-resist application in conventional photo-lithography, and the controlling parameters to achieve a film of the required thickness are the volume of liquid deposited on the plate, the spin speed and the spin duration. The substrate temperature, or the post-spin anneal temperature, are also important for organic semiconductor films in order to control the solvent evaporation rate and the crystallisation of the film. In some cases, the poly-crystalline film is formed directly after spin-coating on SAM coated substrates [59], whilst for other materials post-deposition baking [60] or solvent annealing was required [61]. Hence, the details of the required preparation procedure are very much material dependent.

10.4.1.2 Drop-Casting

Drop casting has been demonstrated for the deposition of triisopropylsilylethynyl pentacene (TIPS-pentacene) [62], which is a solution processable derivative of pentacene. The drop casting technique is illustrated in Fig. 10.10a [63], in which a solution of TIPS-pentacene in toluene was dropped from a capillary needle onto the TFT substrate tilted at 3.5° in a sealed jar, and allowed to evaporate. The process can also be implemented with horizontal substrates [64], but, with the tilted substrate, the lower drop line spread down the substrate, whilst its upper contact line remained pinned. Nucleation started at this upper line, and the crystallite stacking axis grew down the substrate, giving ribbon-shaped grains 200–800 nm thick, 20–80 μm wide, and 200 μm–5 mm long [63].

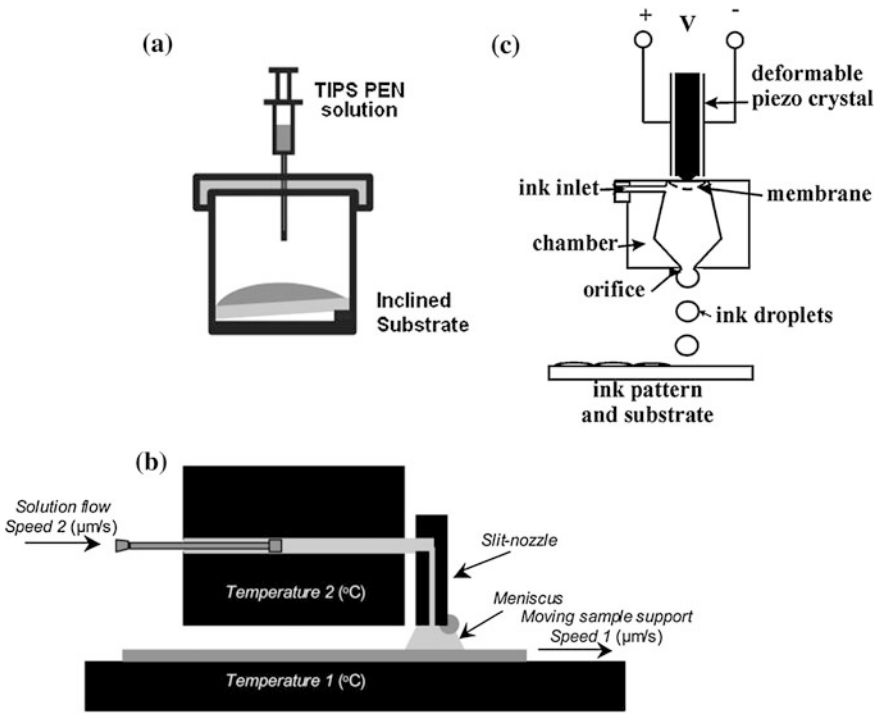

Fig. 10.10 Semiconductor layer deposition by **a** drop-casting (Reprinted with permission from [63]. Copyright (2007) American Institute of Physics). **b** Zone-casting (Reprinted with permission from [65]. Copyright (2008) American Chemical Society), and (c) inkjet printing (Reprinted from [71] with permission of IEEE)

10.4.1.3 Zone-Casting

Zone casting is a deposition technique in which the solubilized organic material is delivered to a moving substrate through a slit-like nozzle, as illustrated in Fig. 10.10b [65], and has been demonstrated with pentacene films derived from a solution of pentacene in an anhydrous chlorinated solvent. Grain size and quality was controlled by the temperature of both the liquid and the substrate, as well as by the substrate scanning speed and the flow rate of the liquid [65]. Under conditions optimised to obtain stationary film solidification, long grains were produced, with a width of 10–100 μm, and a length extending to millimetres in the substrate scanning direction. With this particular implementation using pentacene, the choice of substrate surface (which would be the gate dielectric in a BG TFT) was critical, and the best results were obtained with a BCB (divinylsiloxane-bis-benzocyclobutene resin) buffer layer on top of SiO_2. This gave extended grain growth, whereas bare SiO_2 resulted in cracks across the width of the grains [65].

10.4.1.4 Printing

Film deposition by printing has the major benefit of in-built pattern definition, as it delivers material only to those locations where it is needed. Hence, conventional lithography can be avoided, and, moreover, some of printing's unique features, such as sensitivity to substrate surface energy, can be exploited to deliver novel processing schemes [66], as discussed in Sect. 10.4.7. However, printing has a number of specific material requirements, such as the availability of appropriate inks for the printing of conductors, semiconductors, dielectrics, and of solvents for via hole opening. In addition, the inks need to have the correct viscosities and evaporation rates. The printing technique also has its own inherent limitations with respect to feature size, resolution, film thickness and plate throughput. Several different printing processes are available, including screen, offset, gravure and inkjet, which have quite different characteristics in terms of these parameters, and are reviewed in references [67, 68]. Although there are examples of all-printed TFTs and circuits using offset [69], and screen printing [70], more attention has been directed towards inkjet printing. Compared with the other printing techniques, inkjet can achieve relatively high resolution and alignment accuracy, although throughput is lower [67]. The preferred implementation of this technique is by piezo-electric drop-on-demand (rather than by continuous droplet delivery), and a schematic diagram of the print head is shown in Fig. 10.10c. A signal to the piezo crystal causes it to expand against a membrane, thereby increasing the pressure in the ink chamber, and ejecting an ink droplet [71]. Large area systems, with piezo-electric control of the printing nozzles, have been designed to release droplet volumes in the range 1–10 pL, with a positional accuracy of ±5 μm [72]. Controlling the droplet size is crucial to line width control and positioning, and this will determine one of the most critical TFT dimensions, which is its channel length. For both top and bottom contact TFTs, this will be determined by the separation of the source and drain contacts. For example, 1 pL nozzles have been demonstrated to give 25 μm wide metallic tracks, using a silver ink [73], although repeated printing was necessary to produce lines of sufficient thickness to give an acceptable line resistance of 0.36 Ω/□. All other layers were also inkjet printed in this work, including the silver gate, the PVP gate dielectric, and the TIPS-pentacene active layer. As the dimensions of these layers were greater than those of the source/drain contacts, a 10 pL nozzle was used for faster printing. The finished device was a BG/BC structure with W/L = 150/11 μm, and had a field effect mobility of 0.05 cm^2/Vs [73]. For smaller channel lengths, down to 1 μm, a sub-femtolitre inkjet printing process has been demonstrated, using an ink containing silver nano-particles for the critically dimensioned source/drain contacts. In this case, n- and p-channel BG/TC OTFTs were fabricated, with the slow, but high-resolution, sub-femtolitre inkjet printing process used just for the source/drain contacts [74]. An alternative approach has been to use surface energy conditioning of the substrate to control its wetting properties, and to confine the droplet within these appropriately conditioned regions [55, 66, 67]. This process is discussed further in Sect. 10.4.7.

10.4.2 Organic Semiconductor Layers for p-Channel TFTs

10.4.2.1 Vacuum Thermal Evaporation

Pentacene is one of the most widely studied small molecule materials, largely because of its high performance, with mobility values equalling or exceeding those of a-Si:H. It has been extensively prepared from a purified source by vacuum evaporation at 10^{-4}–10^{-5} Pa, where the deposition rate has a strong influence on the grain size. This is seen in Fig. 10.11a–c by the AFM images from 60 nm thick films grown at different deposition rates on a SiO_2-coated substrate. All films showed a granular surface structure, where the largest grains were in films grown at 0.12 nm/min, and the smallest at 12 nm/min [75]. Very similar results have also been obtained for depositions onto PVP and PMMA coated substrates. The hole mobility directly correlated with increasing grain size, as shown in Fig. 10.11d, with the maximum mobility value approaching 2 cm^2/Vs for the largest grains [75]. In view of this result (and similar ones in Fig. 10.6d), evaporated pentacene is usually deposited at a rate of $\sim$0.1 nm/min at room temperature. Higher substrate temperatures may be used, but there is a tendency for the evaporated film to contain an increasing fraction of the bulk pentacene crystalline form, rather than the 'thin-film' form, which would lead to reduced TFT performance.

In spite of its large mobility, one of the limitations of pentacene is its sensitivity to oxidising reactions, which, in unencapsulated devices, leads to device instability during ageing under ambient conditions [13, 76]. The instability is a reduction in hole mobility, which has been attributed to shallow state formation near the HOMO level [77]. Oxidation is a chemical reaction which involves electron transfer from pentacene to the oxidising agent, and the susceptibility of material to oxidation can be reduced by changing the molecular structure to one with a greater ionisation energy, and, hence, a deeper HOMO level [13, 76]. In principle, this would have the effect of increasing the injection barrier height for preferred contacts, such as gold, and, thereby, increasing the contact resistance [76]. However, whilst there is evidence for this effect [76], it does not appear to be universally present, and examples exist in which the molecular structure has been changed from pentacene to alternative molecules [13, 78], with a HOMO $\sim$0.4 eV deeper, in which there was improved ambient stability, and only a small increase in the measured contact resistance [78]. The explanation for this variability in contact resistance between different samples is most likely due to the influence of different interfacial dipole layers. These more stable materials, shown in Fig. 10.12a, b, were di(phenylvinyl)anthracene (DVAnt) [78], and dinaphtho-[2, 3-b:2′,3′-f]thieno[3,2-b]thiophene (DNTT) [13], with ionisation energies of 5.4 eV (compared with 5.0 eV for pentacene). Both were vacuum evaporated onto substrates held at 60 °C, and had similar TFT characteristics to pentacene, with hole mobilities of 0.3 and 0.6 cm^2/Vs, respectively. There is greater contemporary interest in DNTT due to its better air stability and mobility [15].

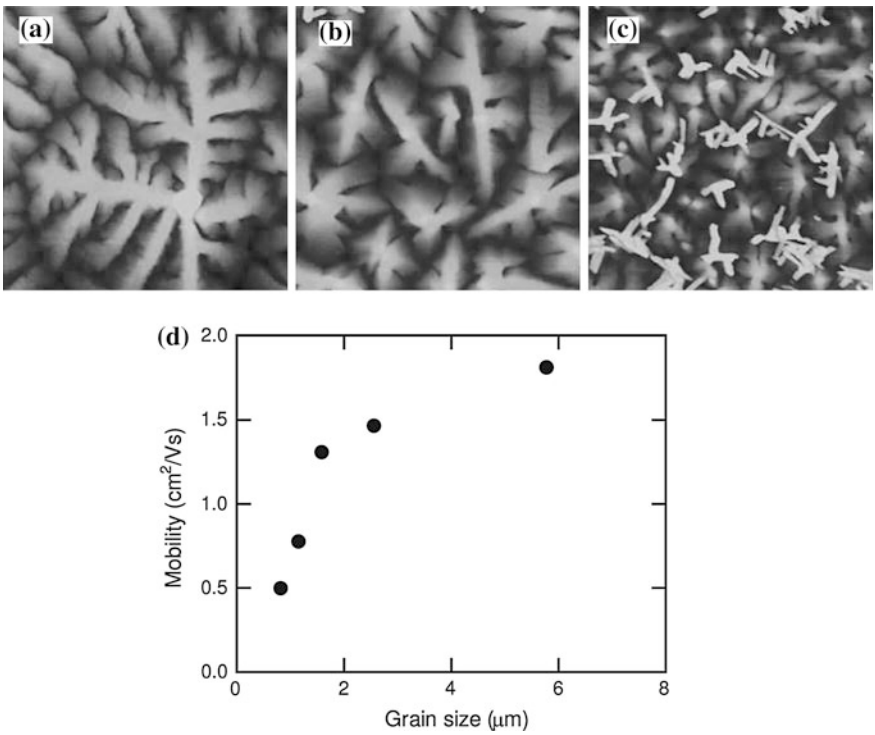

Fig. 10.11 AFM images of pentacene grains grown at deposition rates of **a** 0.12 nm/min, **b** 1.2 nm/min, and **c** 12 nm/min. The AFM image size is 5 μm × 5 μm. **d** variation of mobility with pentacene grain size (Reprinted from [75], with permission from IOP Publishing Ltd)

Although DVAnt and DNTT showed improved air-stability as a result of increased ionisation energies (which were achieved without a significant impact upon the effective height of the source injection barrier), there is a limit to the extent to which the ionisation energy can be increased without injection becoming a problem. An alternative approach has been to engineer the molecule so that it is inherently less reactive with oxygen, without increasing its HOMO, by adding substituents on the periphery of the molecule [79]. An example of this is vacuum-deposited 3,9-diphenyl-peri-xanthenoxanthene (Ph-PXX) (see Fig. 10.12c, with the H substituent). This is a derivative of peri-xanthenoxanthene, PXX [4, 79], and has an ionisation energy of 5.1 eV (i.e. similar to pentacene), but it displayed much better air-stability. The molecular packing structure was face-to-face, as opposed to the herringbone arrangement of pentacene, although the long molecular axis was similarly stacked perpendicular to the substrate surface. This material has been used in a 4.1in wide rollable AMOLED display, where the measured hole mobility of $\sim$0.4 cm^2/Vs was $\sim$4 times larger than pentacene prepared under identical conditions [4].

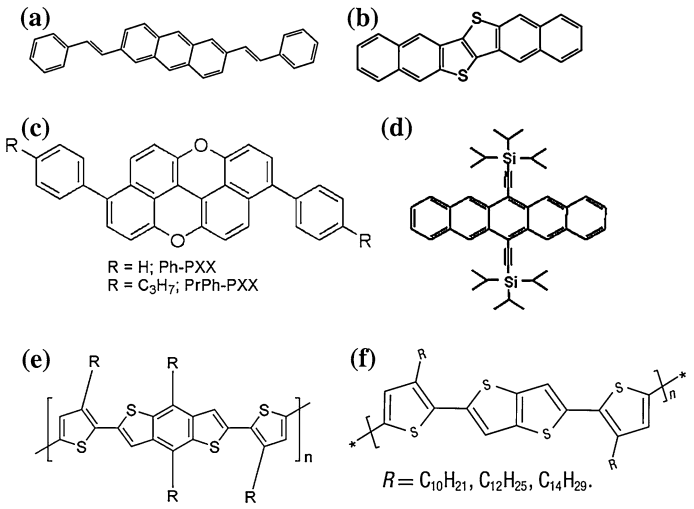

Fig. 10.12 Vacuum deposited small molecule semiconductors **a** di(phenylvinyl)anthracene, (DVAnt) (Reproduced from [78] with permission of John Wiley & Sons, Inc). **b** Dinaphtho-[2, 3-b:2',3'-f]thieno[3,2-b]thiophene, (DNTT) (Reproduced from [13] with permission of John Wiley & Sons, Inc), and **c** peri-xanthenoxanthene derivatives, Ph-PXX and PrPh-PXX (Reprinted with permission from [79]. Copyright (2009) American Chemical Society). Solution processed materials **d** triisopropylsilylethynyl pentacene, (TIPS-pentacene) (Reprinted with permission from [63]. Copyright (2007) American Institute of Physics). **e** poly(4,8-dialkyl-2,6-bis(3-alkylthiophen-2-yl)benzo[1,2-b:4,5-b']dithiophene), R = hexyl (Reprinted with permission from [87]. Copyright (2007) American Chemical Society), and **f** poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b] thiophene) (PBTTT) (Reprinted by permission from Macmillan Publishers Ltd: Nature Materials [60], copyright (2006))

10.4.2.2 Solution Processing

As discussed previously, solution processing is regarded as a more cost effective deposition technique than vacuum thermal evaporation, and has traditionally been used with polymer materials. Although much of the early work on pentacene used vacuum evaporation, there are now solubilised examples of pentacene and its derivatives, as well as of the PXX molecule discussed above. The oligomer and polymer materials are reviewed in the following two sub-sections.

Small Molecule Materials

Soluble pentacene pre-cursors have been used to deposit films of pentacene from solution, by, for instance, spin-coating a soluble derivative in chloroform solution, and then converting it into pentacene by annealing between 130 and 200 °C for 25 or 1.5 min, respectively [80]. A more extensive investigation compared spin-coating, drop-casting and zone-casting from a solution of pentacene in an anhydrous chlorinated solvent [65]. Under optimised deposition conditions, zone-casting was found

to give the best, and most continuous, long range grain structure, and the resulting TFTs had mobilities within the range 0.4–0.7 cm^2/Vs (which compared well with vacuum deposited pentacene films) [65]. Pentacene TFTs have also been printed, but with a non-conventional printing technique, using organic vapour jet printing, which was solvent free, and has been compared to thermal evaporation [81]. As with other solution based processing procedures, the performance of the printed TFTs compared well with TFTs made using vacuum deposited films.

Another solution processable material is triisopropylsilylethynyl pentacene, TIPS-pentacene, which is a functionalised derivative of pentacene with tri-iso-propylsilylethynyl substituents (the molecular structure is shown in Fig. 10.12d). It self-assembles in the solid-state with co-facial π–π stacking, rather than the herringbone stacking of pentacene, leading to closer packing of the pentacene molecules, and is also expected to be more oxidative stable than pentacene [83]. It has been widely investigated for solution processing using drop-casting [63], spin-coating [82], and, in another publication, optimised spin, dip, and drop-casting were compared [83]. In that work, when comparing both the structural organisation of the films, and the hole mobility in the TFTs, the drop-casting was found to give the best results, and spin-coating the worst. The spin and drop-cast films had mobilities of 0.05–0.2 and 0.2–1.8 cm^2/Vs, respectively. The mobility differences correlated with the differences in structural organisation, and were attributed to slower solvent release and slower film growth in the drop-cast films [83]. Compared with these high mobility TFTs, ink-jet printed TIPS-pentacene TFTs only had a mobility of 0.05 cm^2/Vs, which was associated with contact resistance effects to the ink-jet printed silver source/drain electrodes [73].

Another derivative of the molecule peri-xanthenoxanthene, PXX (which was discussed in Sect. 10.4.2.1 as having improved air-stability compared to pentacene) has been developed for solution processing. This is 3,9-bis(p-propylphenyl)-peri-xanthenoxanthene (PrPh-PXX) [7, 79], which differs from Ph-PXX by the replacement of hydrogen by the propanyl substituent on the phenyl end groups (see Fig. 10.12c). It has a HOMO level comparable to Ph-PXX. Films of PrPh-PXX were prepared by spin-coating a solution of it onto a PVP gate dielectric, which was then cured in air at 120 °C to remove the solvent and to crystallise the film. The resulting BG/TC TFTs had a hole mobility of $\sim$0.5 cm^2/Vs, and were used in a 13.3in UXGA flexible AMEPD demonstrator [7]. The same material was also used to make a smaller, ink-jet printed 4.8in VGA AMEPD [84].

As is apparent from the above overview, high-performance solution-processed small molecule TFTs have been obtained using a number of different molecular materials and preparation techniques, but these procedures mainly produced undefined, large area films, which then needed patterning for TFT applications. Hence, while there are some examples of ink-jet printing of small molecule materials, it would appear that there is a need for the printing technologies to be further developed for widespread application to these materials.

Polymer Materials

Two extensively studied regio-regular polymers are P3HT [27, 85, 86] and PQT-12 [21] (see Fig. 10.3f, g), where the PQT-12 molecule has been engineered to give better air-stability then P3HT [21]. Solution processing has dispensed the purified material in a suitable solvent using spin-coating, dip-coating or drop-casting. For P3HT dissolved in chloroform, dip-coating gave the best results, and further improvement was obtained after annealing at 160 °C for 3 min in N_2, giving a mobility of 0.11 cm^2/Vs [86]. Spin-coating has, however, been successfully used with the solvent 1,2,4-trichlorobenzene [85], which has a higher boiling point than chloroform. This led to much slower drying of the films (compared with the chloroform solvent), and, following vacuum annealing at 100 °C, resulted in better controlled development of the characteristic crystalline domain structure discussed in Sect. 10.2.3, and shown in Fig. 10.5a. The hole mobility in these devices was 0.12 cm^2/Vs, which was 100 times greater than films spin-coated using a chloroform solvent. Similarly, PQT-12 has been applied by spin-coating, and post-deposition annealing at 120–140 °C improved both the lamellar packing and the hole mobility from 0.02–0.05 to 0.07–0.12 cm^2/Vs [21].

Other solution processable polymers have been reported, which have improved behaviour compared with P3HT and PQT-12, such as poly(4,8-dialkyl-2,6-bis (3-alkylthiophen-2-yl)benzo[1,2-b:4,5-b′]dithiophene) [87] (see Fig. 10.12e for its molecular formula). This was spin-coated from a 1,2-dichlorobenzene solution onto an OTS coated substrate, where it directly formed a well organised lamellar structure without post-deposition annealing. It solidified into $\sim 1 \times 1$ μm domains, giving a hole mobility of ~ 0.2 cm^2/Vs, and displayed improved air-stability compared with P3HT and PQT-12. Another polymer was poly(2,5-bis (3-alkylthiophen-2-yl)thieno[3,2-b]thiophene) (PBTTT) (see Fig. 10.12f), which was a higher mobility polymer, with better air-stability [60]. The films were formed by spin-coating a solution of PBTTT in 1,2-dichlorobenzene, and annealing at 120–160 °C for 10–15 min. With the C14 alkyl substituents, this gave 200 nm grains, and a hole mobility of 0.6 cm^2/Vs. This mobility is larger than usually found with polymers, and is comparable to the better small molecule materials. PBTTT has a liquid crystal phase, which was established during the post-deposition annealing, and the high mobility was attributed to the organised assembly of the molecular chains in the LC phase, and their retention, as the structure crystallised [60].

As discussed in the previous section, the preferred deposition technique for low cost TFT fabrication is by printing. Amongst the polymers, P3HT has been deposited by inkjet printing, and TG/BC TFTs prepared by this process compared well with spin-coated TFTs, where the hole mobilities were ~ 0.08 and ~ 0.09 cm^2/Vs, respectively [88]. An inkjet printed proprietary p-channel polymer had better TFT characteristics, with a mobility of ~ 0.25 cm^2/Vs, whilst the mobility of its spin-coated control was 0.6 cm^2/Vs [88]. Although PQT-12 has also been ink-jet printed, its performance was poor, with a mobility of 1×10^{-4} cm^2/Vs, which was attributed to non-optimised preparation conditions [89]. The polymer poly(9,

9-dioctylfluoreneco-bithiophene), F8T2 [55], and other polyfluorene-based materials [57, 90], have been inkjet printed in demonstration displays. These materials had low mobilities of ~ 0.03 cm^2/Vs [57], but were, nevertheless, good enough for AMEPDs.

10.4.3 Organic Semiconductor Layers for n-Channel TFTs

The development of high-performance OTFTs has traditionally been much easier with p-channel TFTs than with n-channel TFTs. A 2004 review paper [35] identified several issues with the operation of n-channel TFTs, including the high injection barrier with large work function metals and the ambient instability of low work function metals, low electron mobilities (in many cases $\ll 0.1$ cm^2/Vs), the instability of these devices due to electron trap formation in the presence of oxygen and water vapour, and high threshold voltages with some high mobility materials [35]. Indeed, the question was raised whether there were fundamental reasons preventing the carrier mobility in n-channel TFTs from matching that in p-channel TFTs [36]. As mentioned above, a simple practical issue was the mismatch of the work function of the commonly used gold source/drain material with the LUMO level of the organic semiconductor. To resolve this injection problem, the LUMO had to be deeper, or a lower work function metal, such as Ca, had to be used. Neither approach solved the problem of poor n-channel performance. However, as discussed in Sect. 10.3, much of the basic materials work on OTFTs used a thermally oxidised Si substrate as a combined gate dielectric and gate electrode, and one of the key observations with n-channel operation was that hydroxyl molecules on the surface of the SiO_2 gate dielectric formed silanol, SiOH, electron traps at the dielectric/channel interface [36]. The trapping mechanism is shown in Fig. 10.13a, and the trapped electrons result in negatively charged defects, which compensate the gate field, and can result in very high threshold voltages. Although the silanol coverage of high quality SiO_2 surfaces is very small, at <10 % of a monolayer, this equates to a potential areal trap density of 3 to 7 $\times$ 10^{13} cm^{-2}, which is more than an order of magnitude greater than the electron densities induced by the gate bias. Hence, with an SiO_2 gate dielectric, a large fraction of the induced electrons were trapped at interface defects, and similar trapping effects were also observed with some other commonly used dielectrics including poly(vinyl phenol), PVP, and polyimide, both of which contain hydroxyl groups [36]. Using the poly-fluorene based semiconductor poly(9,9-dioctylfluorene-alt-benzothiadiazole), F8BT, the influence of the gate dielectric is shown in Fig. 10.13b. There was no TFT behaviour with the F8BT directly deposited onto a bare SiO_2 layer, but, after spin-coating the SiO_2 with a layer of polyethylene, good TFT operation was displayed, and the on-current increased by several orders of magnitude. Intermediate results were obtained with several SAMs, none of which was able to completely eliminate electron trapping at SiOH groups. These devices showed initial n-channel behaviour, but this was

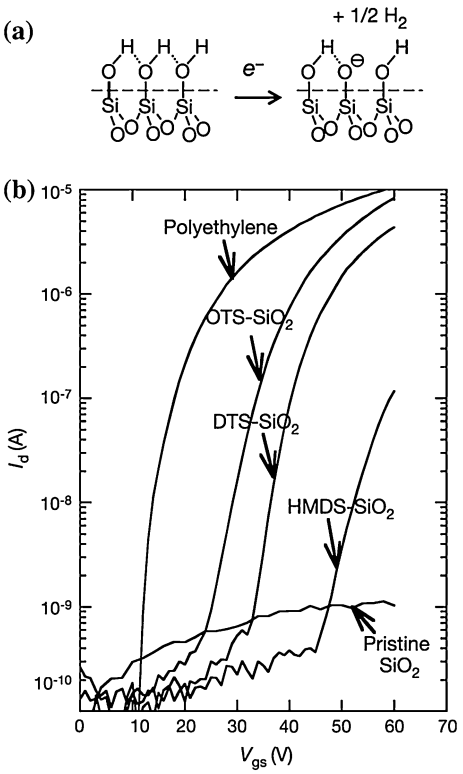

Fig. 10.13 **a** Silanol electron trapping mechanism at the semiconductor/SiO2 interface, and **b** transfer characteristics of F8BT n-channel TFTs with different gate dielectrics and SAMs (OTS, DTS and HMDS). (Reprinted by permission from Macmillan Publishers Ltd: Nature [36], copyright (2005))

quenched by strong air-instability effects [36]. It was also noted that the sensitivity to silanol trapping reduced with increasing depth of the LUMO level.

Although the use of an appropriate dielectric layer can suppress electron traps associated with silanol, this will not necessarily solve the problem of air-instability. The material's susceptibility to oxidation reactions is enhanced by the presence of channel electrons at the relatively shallow LUMO level, and these are able to react with oxygen and moisture in the ambient. Ambient instability in n-channel TFTs was reviewed in a 2007 paper [91], and, to address this instability, there is a requirement for either a dense molecular structure to suppress oxidant ingress [35, 91], or a deep enough LUMO to suppress the oxidation reactions [91, 92]. For the former, fluorinated side-group substituents may act as a kinetic barrier to the diffusion of oxidising species [35], and perfluorinated copper phthalocyanine, F_{16}CuPc, (see Fig. 10.14a) is a widely studied, air-stable n-channel material [35, 91, 93]. For LUMO-controlled instability, a minimum LUMO value of 4 eV has been identified [92], and this is consistent with other reports of air-stable n-channel TFTs using materials with LUMO values of 4.8 eV and 5.05 eV [93, 94]. It is worth noting that F_{16}CuPc, with a LUMO of 4.8 eV, possesses both attributes, but has a modest mobility of $\sim$0.08 cm^2/Vs [93].

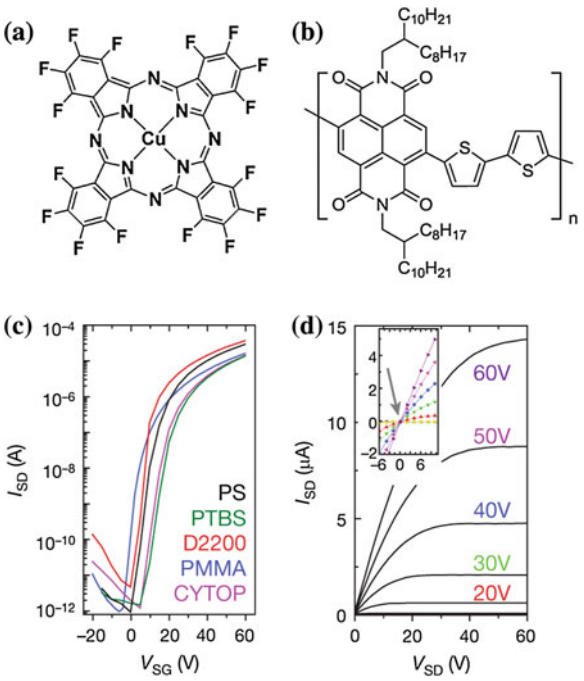

Fig. 10.14 **a** $F_{16}CuPc$ (Reprinted with permission from [91]. Copyright (2007) American Chemical Society). **b** P(NDI2OD-T2). **c** transfer characteristics of P(NDI2OD-T2) TG/BC TFTs (W/L = 1000/50) with different gate dielectrics (Cytop—(poly(perfluoroalkenylvinyl ether), k = 2.1), PTBS—(poly(t-butylstyrene), k = 2.4), PS—(polystyrene, k = 2.5), ActivInk D2200—(polyolefin-polyacrylate, k = 3.2) and PMMA—(poly(methylmethacrylate), k = 3.6), and **d** output characteristics of P(NDI2OD-T2) TFT with a PMMA gate dielectric. (Reprinted by permission from Macmillan Publishers Ltd: Nature [25], copyright (2009))

Many of the air-stable materials, with electron mobility values in the range ~0.1–0.6 cm^2/Vs, are oligomers, and are most easily deposited by vacuum evaporation [91, 93, 94], whereas an ideal n-channel material would be solution processable [37]. Such materials, which are air-stable, and have a mobility ≥0.1 cm^2/Vs, appear to be few in number [95], but, a promising candidate is the polymer poly{[N,N9-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)-2,6-diyl]-alt-5,59-(2,29-bithiophene)}, (P(NDI2OD-T2). This has a LUMO level of ~4.0 eV, an optical band-gap of 1.45 eV, and its structure is shown in Fig. 10.14b [25]. The material is soluble in xylene and dichlorobenzene, and can be deposited by spin-coating, gravure printing or inkjet printing. It has been demonstrated in TG/BC structures, with a range of spin-coated polymer dielectrics, giving air-stable, n-channel TFTs with mobilities in the range 0.1–0.85 cm^2/Vs [25]. The highest mobilities of 0.65–0.85 cm^2/Vs were with a proprietary polyolefin-polyacrylate dielectric, D2200, but a PMMA dielectric gave the next highest mobility values in the range 0.2–0.45 cm^2/Vs. The transfer characteristics of devices made with P(NDI2OD-T2), and with a range of different spin-coated organic gate dielectrics, are shown in Fig. 10.14c. These have broadly similar characteristics, yielding high mobilities, as well as low threshold voltages, and on:off current ratios of 6–7 orders of magnitude [25]. In addition, the TFT output characteristics in Fig. 10.14d displayed good operation in both the linear and saturation regimes. Further commercial developments of P(NDI2OD-T2) have yielded a proprietary material for solution processable, air-stable n-channel TFTs

with a mobility of $\sim$3.0 cm^2/Vs [96]. This has been demonstrated in spin-coated and inkjet printed TG/BC TFTs, using a proprietary gate dielectric, and fabricated on PET and PEN substrates. These devices displayed minimal degradation during 1400 h of accelerated bias-stress stability measurements, and this was assessed to be equivalent to an operating life of >10,000 h under typical AMOLED operating conditions [96].

One of the reasons for interest in n-channel TFTs is to enable the fabrication of low-power-dissipation complementary logic circuitry [25, 35, 37], and this was demonstrated with p- and n-channel TFT inverter circuits using P3HT and P(NDI2OD-T2) layers, respectively. These devices, with a common PMMA gate dielectric layer and Au contacts, showed inverter switching gains of 25 and 60 at supply voltages of 20 and 40 V, respectively [25]. Whilst there are many demonstrations of complementary inverter circuitry (for instance [11, 70, 88, 89, 94]), it has been argued that a simplification to the fabrication process may be achieved with a single ambipolar material, rather than with two separate materials for n-channel and p-channel operation. An important proviso for the ambipolar material is that it can deliver high performance, well-matched p- and n-channel operation using the same injecting electrodes [97]. (This necessarily requires small bandgap material, so that the injection barriers are low enough for each carrier type, and, equally, the material needs good transport properties for both holes and electrons). Ambipolar material would also ease potential compatibility issues with the dielectrics and contact materials for the two device types, as well as simplifying the definition stages for the device layers [97]. As with the more direct complementary devices, there are many reports of ambipolar material (for instance [42, 92, 95, 97–99]).

An example of ambipolar complementary device behaviour is shown in Fig. 10.15a–d [97]. The material for these devices was PSeDPPBT, which is a low bandgap polymer based upon a diketopyrrolopyrrole (DPP) core flanked with two selenophene rings (thiophene with the S replaced by Se) and a benzothiadiazole (BT) monomer. The device architecture was BC/TG with Au contacts. Both the PSeDPPBT, and the PMMA gate dielectric, were deposited by spin-coating, and, following annealing at 200 °C, saturation hole and electron mobilities of 0.46 cm^2/Vs and 0.84 cm^2/Vs, respectively, were obtained [97]. Although the material had a bandgap of 1.05 eV, current crowding, due to injection problems from the Au electrodes, is visible in the output characteristics at low drain biases. Figures 10.15a, c show the p-channel behaviour (at negative gate and drain biases), and the complementary n-channel behaviour with positive biases is seen in Fig. 10.15b, d. However, conventional p-channel and n-channel behaviour is only seen over certain voltage ranges (e.g. large negative gate and drain biases for p-channel, and the opposite conditions for n-channel). Outside these ranges, and in contrast to the usual unipolar devices, there are anomalous features in the transfer and output characteristics. For instance, for the ‘p-channel’ operation, at large negative drain bias and small positive gate bias, there is an increasing minimum off-current with increasing drain bias, which is characteristic of ambipolar device behaviour [98]. Over this voltage range, the surface adjacent to the negatively

biased 'drain' terminal becomes electron accumulated, with the terminal acting as the 'source' for n-channel conduction. Hence, the anomalous appearance of the characteristics occurs when the device is ceasing to act as a unipolar device, and is, instead, supporting ambipolar conduction. This is also responsible for the absence of saturation in the output characteristics at low gate biases in Fig. 10.15c, d. The potentially poor off-currents adversely affect the power dissipation in inverter circuits (compared with conventional complementary TFT inverters), and ambipolar inverters are also unable to fully switch the output voltage between the supply voltage and ground [97, 98]. Hence, the trade-off with ambipolar inverters is potentially simpler device processing, but with reduced inverter performance.

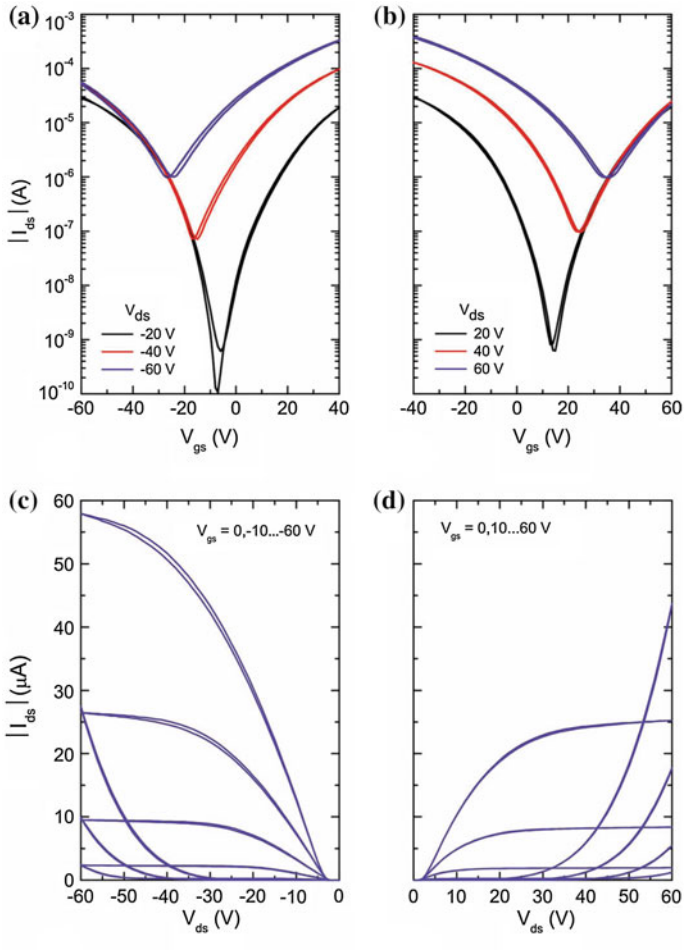

Fig. 10.15 Transfer and ouput characteristics obtained from a PSeDPPBT ambipolar device. **a** and **c** p-channel, and **b** and **d** n-channel behaviour at negative and positive gate and drain biases, respectively. (Reproduced from [97] with permission of John Wiley & Sons, Inc)

Nevertheless, there is continuing interest in this approach, and PSeDPPBT inverters (using pairs of self-aligned ambipolar TFTs) had gains of >30 and >40 at supply voltages of 10 and 20 V, respectively, and 3-stage ring oscillators operated at 182 kHz, with a small delay/stage of 0.91 μs at a supply voltage of 50 V [97].

10.4.4 Gate Dielectric

As is clear from the preceding sections, much of the simple investigative materials work has been carried out using thermally grown SiO_2 (dielectric constant, $k = 3.9$) as the gate dielectric, but this material is not relevant to low cost glass and polymer substrates, which is where the main application of OTFTs is expected to be. Moreover, as discussed in Sect. 10.4.3, SiO_2 also gave unacceptably poor n-channel TFT performance [36]. Hence, there was a clear need for alternative dielectrics to SiO_2. Nevertheless, the basic materials research using this dielectric identified the critical importance of the semiconductor/dielectric interface [100], and the key role of SAMs in tailoring the interface to promote the required ordering of the semiconductor on both the dielectric [101], and on the metal contacts in BC structures.

The dielectric material requirements for high performance OTFTs are similar to those of other TFTs, namely: a very good dielectric/semiconductor interface (which generally requires a smooth surface), low leakage currents and low pin-hole densities, and a high dielectric breakdown field in excess of several MV/cm [102]. Three broad classes of dielectric have been investigated: (a) inorganic layers, such as SiN_x and SiO_x, as well as some other inorganic materials chosen for their large dielectric constants (high-k materials), (b) organic layers, many of which have dielectric constants, k, in the range 2.0–4.5 [101], and (c) self-assembled monolayers [101–103]. As mentioned previously, SAMs are also extensively used in combination with many other dielectric layers, and two of the more common SAMs are octadecyltrichorosilane (OTS) and hexamethyldisilazane (HMDS).

There are other desirable TFT attributes, which can be enhanced by the appropriate choice of gate dielectric, such as low voltage operation, and solution processing. However, the particular material choices may be constrained in order to mitigate their effect upon other parameters. For instance, low voltage operation would, in principle, require a thin dielectric layer, but this may be incompatible with a low leakage current and low pin-hole density, and, indeed, the thickness range of organic dielectrics is $\sim$300 nm, or more, to minimise gate leakage [102]. On the other hand, SAMs are especially thin, and have been demonstrated as gate dielectrics of potential interest [102–104]. An alternative approach to low voltage operation is the use of high-k materials, which would favour inorganic dielectrics, but these would not necessarily be compatible with solution processing. In addition, the higher dielectric constant insulators are more polar, and have been found to degrade TFT performance due to increased carrier trapping in disordered

interfacial regions [101, 105, 106]. For solution processed materials, it is also essential to use orthogonal solvents with the different layers, so that the deposition of the organic semiconductor does not dissolve the already-deposited dielectric layer in BG structures, and vice versa in TG structures. The three dielectric options listed above are briefly reviewed in the following sub-sections.

10.4.4.1 Inorganic Dielectrics

High performance OTFTs, using both solution-processed PQT-12 and pentacene, have been demonstrated using PECVD SiO_x ($k \sim 4.0$) and SiN_x ($k = 4.5–7.2$) as the gate dielectric in combination with the SAMs OTS or β-phenethyltrichlorosilane (PTS) [107, 108]. It was argued that the extensive experience of these dielectrics within the inorganic TFT industry, including the availability of large area deposition equipment, makes them a low-risk route to manufacturing. However, the well-established dielectric deposition processes are at $\sim$300 °C, and pentacene TFTs with a 300 °C SiN_x dielectric had comparable performance to devices with a thermal SiO_2 gate dielectric [108]. In contrast, PQT-12 TFTs processed on plastic substrates, using SiN_x deposited at 150 °C and SiO_x at 180 °C, showed a smaller carrier mobility compared with higher temperature depositions of these materials [107]. (Details of the PECVD deposition processes for SiN_x and SiO_x can be found in Sects. 5.5.3 and 7.3.1, respectively).

Other inorganic insulators have been grown by oxidation of the gate metals Al and Ta, forming AlO_x [109] and Ta_2O_5 [10, 110], respectively. The AlO_x was grown by plasma oxidation of the Al gate, and coated with a SAM, to produce complementary TFT inverter circuits (using pentacene and $F_{16}CuPc$) on a polyimide substrate [109]. The Ta_2O_5 ($k = 24$) was formed by anodization of the Ta gate, and was then coated with an HMDS SAM before vacuum deposition of pentacene. These TFTs were used as drive transistors in an AMOLED display on a PEN substrate [110].

Some other high-k dielectrics, which have been used in low-voltage pentacene TFTs, were HfO_2 ($k = 14.9$) [111], and HfLaO ($k = 10.4$) [112]. The 50 nm thick HfO_2 films were deposited by atomic layer deposition at 200 °C, and its surface was modified with phosphonic acid to passivate the polar surface groups, and to improve the pentacene morphology. The resulting TFTs displayed low voltage operation with a sub-threshold slope of 120 mV/dec, a threshold voltage of −0.4 V, and a carrier mobility of 0.4 cm^2/Vs [111]. In contrast, 40 nm thick HfLaO films, deposited by RF sputtering, required annealing in NH_3 at 400 °C, and did not display such low voltage operation, with the sub-threshold slope and threshold voltage being 0.26 V/dec and −2.6 V, respectively [112]. It is clear that the differences in the TFT parameter values between these two dielectrics cannot be simply ascribed to differences in film thickness and dielectric constant. The HfLaO films did not have any surface modification beyond the NH_3 exposure, and it is possible that the polar dielectric was degrading the interface, as has been reported with other polar dielectric films [105, 106]. Indeed, by deliberately

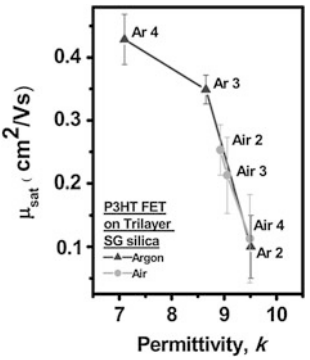

Fig. 10.16 Field effect mobility in P3HT TFTs as a function of the dielectric constant of the tri-layer sol-gel silica gate dielectric. (Reprinted with permission from [106]. Copyright (2009) American Institute of Physics)

changing the dielectric constant, k, over the range 7–10, in tri-layer sol-gel silica gate dielectric films, the carrier mobility in both pentacene and P3HT BG/TC TFTs was found to reduce as the dielectric constant was increased, as shown in Fig. 10.16 [106]. In these samples, the dielectric constant was modified by exposing the first and second surfaces in the tri-layer films to an argon or air plasma, before the deposition of the next sol-gel layer. This changed the concentration of polar OH groups in the films, and it was concluded that the polarisability of the film influenced the carrier flow in the TFT channels [106]. Parallels were drawn between this result and comparable k-dependent mobility values seen with organic dielectrics [105], as discussed in the next section.

10.4.4.2 Organic Dielectrics

The interest in organic insulators stems, in part, from their solution processability, and the characteristics of a wide range of organic dielectric films have been extensively reviewed [101, 102, 105]. Some of the more widely investigated materials (with dielectric constants comparable to, or greater than, SiO_2) are PVP (polyvinylphenol, k = 4.5), PMMA (polymethylmethacrylate, k = 3.5), and PVA (polyvinylalcohol, k = 7.8), and amongst the lower-k materials are Cytop (k = 2.1), and PPCB (polypropylene-co-butene, k = 2.3). The chemical structures of these materials are shown in Fig. 10.17a–e. They are usually solution processed, by, for instance, spin-coating, and then annealed to remove the solvent and also to cross-link the film. When the low-k dielectrics were used with several different TFT materials, including P3HT, F8T2, and the low-mobility amorphous polytriarylamine semiconductor (PTAA), they were found to result in higher carrier mobilities than observed with PVP, PMMA, PVA and other high-k dielectrics [101, 105]. This is illustrated for PTAA by the dependence of mobility on dielectric constant, in Fig. 10.18a, and by the temperature dependence of the mobilities in Fig. 10.18b [105]. In Fig. 10.18b, the field effect mobility for different dielectrics is compared with the bulk mobility (evaluated by time of flight, TOF, measurements), and the reducing absolute values of field effect

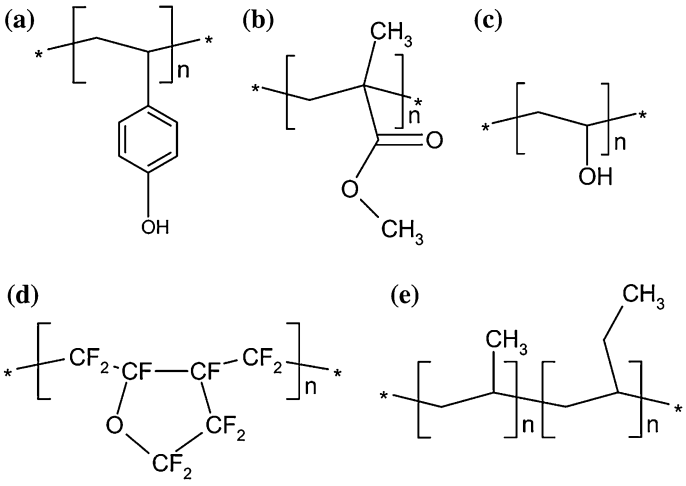

Fig. 10.17 Chemical structures of common organic gate dielectrics **a** PVP, **b** PMMA, **c** PVA, **d** Cytop, and **e** PPCB. (Reprinted with permission from [101]. Copyright (2004) American Chemical Society)

mobility, and their increasing activation energy, with increasing dielectric constant were attributed to increased carrier localisation at the semiconductor/dielectric interface. The model for this is shown in Fig. 10.18c, with a Gaussian DOS distribution in the semiconductor. The effect of the random orientation of dipoles in the high-k, polar dielectrics was to increase the energy fluctuations, and, hence, the disorder, in the semiconductor surface. This was characterised by a broadening of the DOS at the interface, leading to increased carrier trapping. It was also suggested that the use of SAMs not only improved the packing order of the organic semiconductor molecules in BG structures, but also partially screened the effects of the polar dielectric, thereby making a further contribution to increased carrier mobility [105].

The influence of the organic dielectric on pentacene film growth, and TFT performance, has been studied with the dielectrics PVP, PVA, poly(2-vinylnaphthalene) (PVN), polystyrene (PS), and poly(4-methylstyrene) (PMS) [100]. The dielectrics were selected for their differing glass transition temperatures, T_G, and surface contact angles. Polymer dielectric thicknesses of 320–360 nm were used in BG/TC structures by spin-coating them onto thermally oxidised silicon, and then vacuum baking them at 80 °C. (Uncoated SiO_2 layers, referred to as 'bare', were used as control samples). For pentacene evaporated onto substrates held near room temperature, the gate dielectric was found to influence the pentacene grain size, as shown in Fig. 10.19, but this varying grain size had little impact upon device performance and carrier mobility. The largest grains were on the PVP and 'bare' surfaces, which had the lowest contact angles, and were the most hydrophilic. This permitted greater movement of the pentacene molecules on the dielectric surface, resulting in the larger grains. The worst samples were grown on the PVA film,

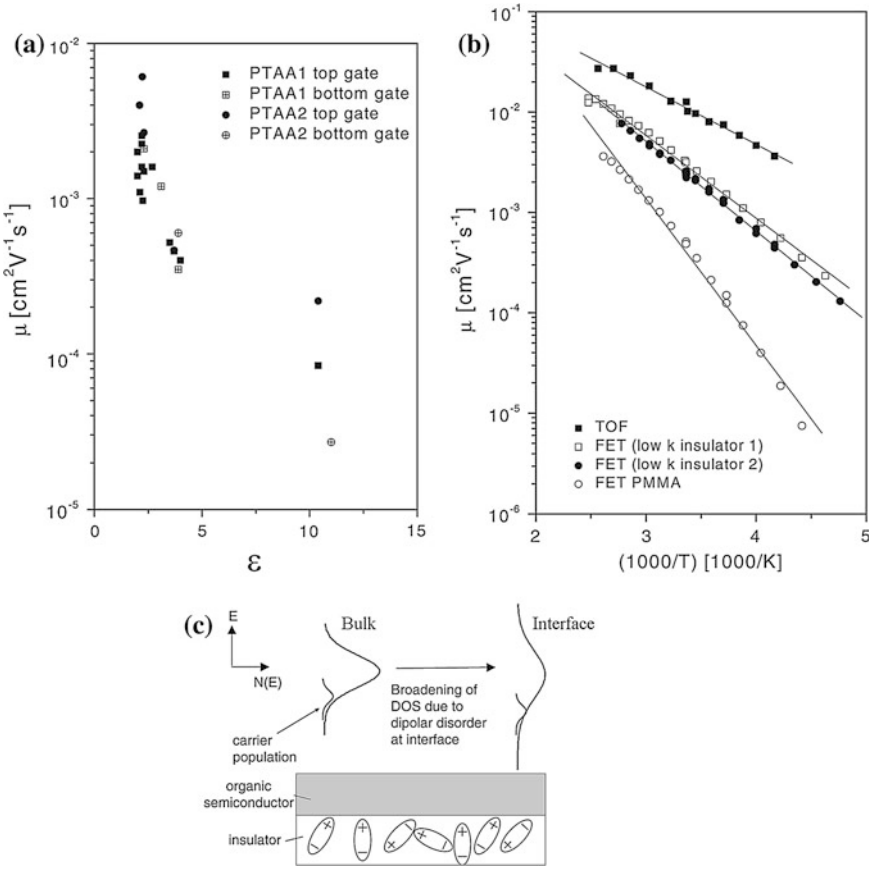

Fig. 10.18 **a** Carrier mobility measured in PTAA TFTs as a function of the dielectric constant of the gate dielectric. **b** Temperature dependence of the mobility for different gate dielectrics, and **c** schematic illustration of the effects of disorder induced in the DOS at the semiconductor surface by a polar dielectric. (Reproduced from [105] with permission of John Wiley & Sons, Inc)

which has a bulk T_G of 49 °C, whereas the others were >100 °C [100]. The small grain size with PVA was attributed to a surface T_G smaller than the bulk value, which perturbed the film during pentacene deposition, resulting in a rough interface. For the other films, it was concluded that for grain sizes above ∼0.8 μm, grain boundary trapping had only a secondary effect on charge transport [100]. It was also noted that, in these samples, the dielectric constant had a smaller impact upon the carrier mobility than reported in other work. Indeed, there are examples in the literature, in which the trends with k were the opposite from those discussed above [101, 102]. Hence, the detailed understanding of the role of the dielectric in OTFTs is still incomplete.

The largest grains in Fig. 10.19 were grown on a PVP dielectric, and this material, which can be inkjet printed [73], as well as spin-coated, is widely used as

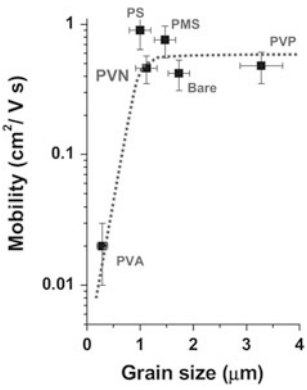

Fig. 10.19 Influence of organic gate dielectric on pentacene grain size and carrier mobility. (Reproduced from [100] with permission of John Wiley & Sons, Inc)

a polymer dielectric in TFT studies. It has also been used in demonstrator displays on flexible substrates, in which it was mixed with OTS to reduce the cross-linking anneal temperature [4, 7].

10.4.4.3 Self-Assembled Monolayers

The use of SAMs as gate dielectrics has been reviewed in Ref. [102], in which layers $\sim$3 nm thick have displayed good dielectric properties. For instance, 2.8 nm thick OTS SAMs gave low leakage currents of 10^{-8} A/cm^2 at 5 MV/cm, and breakdown fields of 9–12 MV/cm. Improved TFT performance was achieved by adding a phenoxy end group to OTS, forming PhO-OTS ($k = 2.5$), which displayed closer molecular packing than OTS, and facilitated the fabrication of BG/TC pentacene TFTs [113]. (The OTS SAM alone had not functioned as an effective gate insulator with pentacene due to their intermixing). With the 2.5 nm PhO-OTS SAM insulator, the pentacene TFTs had a sub-threshold slope of 100 mV/dec, a threshold voltage of -1.3 V, and a mobility of 1 cm^2/Vs. Other SAM insulators of interest have been alkylphosphonic acid molecules, in which the length of the alkyl chain C_nH_{2n+1} was optimised for minimum gate leakage currents and good pentacene TFT performance, by using n values of 14–16 [104].

10.4.5 Metals

The metals used in TFTs are for the gate, and the source/drain contacts, and for the bus bars in displays and circuits, and, although the latter are usually the same metals as used in the TFTs, they can be different. Where the structure has a BG, it is often convenient to use evaporation or sputtering to deposit the gate metal, and lithography to define it. For TG structures, with a polymer gate dielectric, this may be less practical, and solution processing is one option. For the source/drain contacts, gold

is widely used in both experimental TFTs, as well as in demonstrator devices, but its deposition is limited to vacuum evaporation. For full solution-processing of devices, other materials have been investigated for both the TG metal and source/drain contacts. These have included inkjet printing of dispersions of inorganic metallic nano-particles [90], such as silver, which had a resistivity 8 μΩcm, and repeat printing was used to build up 200 nm thick layers, with a sheet resistance of 0.4 Ω/□ [70]. However, although Ag has very good conductivity, its work function is quite low at 4.7 eV [114], and contact resistance effects have been noted in printed TIPS-pentacene TFTs with Ag contacts [70, 114]. The use of thiol-based SAMs has been demonstrated to reduce the injection barrier at the Ag/TIPS-pentacene interface, and this improved the mobility from 0.01–0.04 cm^2/Vs to 0.04–0.17 cm^2/Vs for bare and treated Ag electrodes, respectively [114]. Source/drain contacts have also been inkjet printed using poly(ethylenedioxythiophene) doped with poly(styrene sulfonic acid) (PEDOT/PSS) [90]. This has low contact resistance into many TFT materials, but its large resistivity of 0.01 Ωcm makes it unsuitable for bus bars and gate lines [90].

10.4.6 Process Flow

Given the variety of materials used for both the organic semiconductor and for the gate dielectric, plus the various deposition options, there is not, at this moment, a consensus on the preferred choice of components, and, hence, there is not a typical device processing schedule. In view of this, the following two examples are simply illustrative of processes which have been implemented with small molecule and polymer semiconductors, and should not be regarded as representative of the industry as a whole.

The first example is of a flexible AMOLED display, addressed by BG/BC pentacene TFTs on a PEN substrate [10, 110]. Some of the key process stages in the process are illustrated in Fig. 10.20, and are listed below:

(i) RF sputter deposition of SiO_2 and SiN_x films onto the PEN substrate as barrier and adhesion layers,
(ii) RF sputter deposition of Ta, and its definition into gate electrodes by reactive ion etching,
(iii) Anodisation of Ta gate to form 170–200 nm thick Ta_2O_5 gate dielectric,
(iv) Deposition and definition of Cr/Au source/drain contacts, and ITO pixel electrode,
(v) Deposition of HMDS SAM,
(vi) Vacuum deposition of 100 nm of pentacene,
(vii) Room temperature CVD deposition of parylene (2 μm) and sputter deposition of SiO_2 (50 nm),
(viii) Photoresist application and photolithographic patterning,

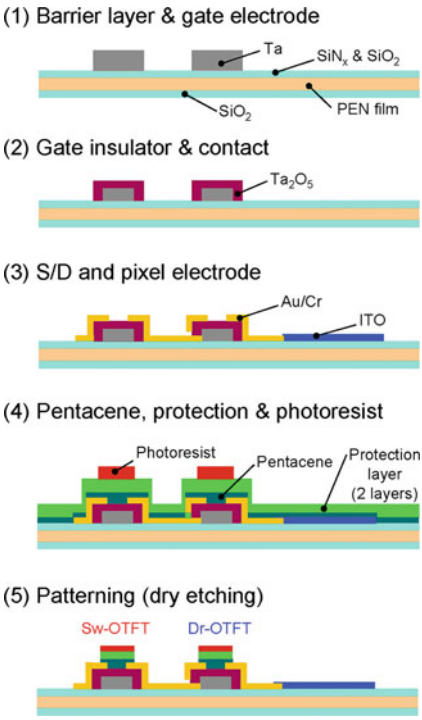

Fig. 10.20 Fabrication stages of pentacene TFTs for an AMOLED display. (Reprinted from [10] with permission of SID)

(ix) CF_4 plasma etching of SiO_2, which then acted as the etch mask for oxygen plasma etching of the parylene and pentacene layers.
(x) Final encapsulation with parylene and a photosensitive polymer.

These TFTs had a mobility of 0.05–0.1 cm^2/Vs, an on:off ratio of $>10^6$, and a threshold voltage of 12 V.

The second example is of a flexible AMEPD using TG/BC unpatterned polymer TFTs, and the pixel/device cross section is shown in Fig. 10.21 [115]. The processing steps were based upon direct-write solution processing and laser patterning, without the need for mask alignment. The main fabrication stages were:

(i) PET substrate planarization,
(ii) Source/drain metal deposition (unspecified procedure),
(iii) Unpatterned polyfluorene-based semiconductor deposition (unspecified procedure),
(iv) Spin-coat polymer dielectric layer,
(v) Inkjet print Ag gate electrode,
(vi) Deposition of organic dielectric passivation layer (10 μm),
(vii) Via hole opening by laser ablation,
(viii) Inkjet print PEDOT/PSS pixel electrode.

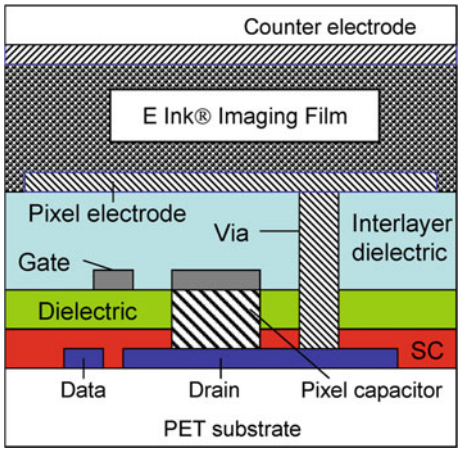

Fig. 10.21 AMEPD pixel/TFT cross section. (Reprinted from [115] with permission of SID)

These TFTs had a mobility of 0.01 cm^2/Vs, an on:off ratio of 10^4, and a threshold voltage of -5 to -10 V. The poor on:off ratio was attributed to the undefined channel layer, and, in later work, this ratio was improved to 10^5–10^6 by patterning the semiconductor [57].

10.4.7 Novel Processing

One of the challenges with inkjet printing is achieving fine lines and short channel lengths, and surface energy conditioning procedures have been demonstrated to address these issues [90], and even to facilitate sub-100 nm channel lengths [66]. The key feature in this approach was to change the wetting-angle of the sample surface, so that hydrophobic and hydrophilic regions were defined, which were then used to localise water-based conducting polymer ink drops. This procedure is shown in Fig. 10.22a, in which the surface of a hydrophobic layer was locally exposed to a laser beam to create hydrophilic regions. Because of the high resolution and positioning accuracy of the laser, gaps of a few microns were defined between the exposed regions, which became the TFT channel regions. When the water-based PEDOT/PSS inks were printed over these areas, the inks were rejected from the hydrophobic regions and retained within the hydrophilic regions. These regions formed the source and drain contacts, with a separation down to 10 μm. Then a polymer semiconductor, such as F8T2, was inkjet printed over these contacts, followed by solution deposition of a polymer gate dielectric, and inkjet printing of a 45 μm wide silver gate electrode, with a positional accuracy of ±20 μm [90]. The devices with L = 10 μm had a mobility of 8×10^{-3} cm^2/Vs and an on:off ratio of 10^5, which was comparable to more conventionally fabricated devices with photolithographically defined gold electrodes. Alternative surface conditioning procedures were also described, such as the use of an electron

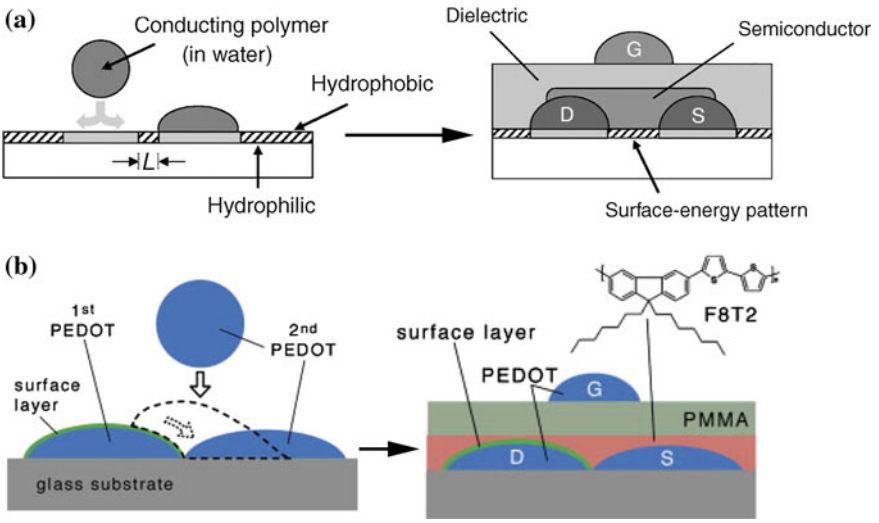

Fig. 10.22 **a** TG/BC TFT printing, using substrate surface patterning to confine the water-based droplets of PEDOT-PSS forming the source and drain regions (Reprinted from [90]. Copyright © Materials Research Society 2003), and **b** sub-100 nm channel length TFTs using self-separating source/drain regions, formed by surface modification of the first droplet. (Reproduced from [66] with permission of John Wiley & Sons, Inc)

beam to write a fine exposure pattern in a PMMA photoresist film, which had been deposited on a SiO_2 layer. These PMMA patterned areas were ultimately used as a template to localise the subsequently printed PEDOT/PSS source/drain regions, giving sub-micron channel lengths [90].

A further extension of this procedure is shown in Fig. 10.22b, and this avoided the direct surface energy patterning of the substrate itself [66]. In this case, the surface of the first droplet was modified to make it hydrophobic, such that, when the second droplet was released onto it, it slid off leaving a small gap between the two. This self-alignment of the source and drain areas did not require precise alignment of the second droplet. The surface of the first PEDOT/PPS ink droplet was made hydrophobic by either exposing it to a CF_4 plasma, which fluorinated it, and, at the same time, the exposed glass substrate surface was made hydrophilic by the etching action of the plasma. The alternative procedure was to have a suitable surfactant within the ink, which segregated to the surface on drying. Device processing was completed with the addition of solution processed layers of F8T2, a 120–130 nm thick PMMA dielectric, and the inkjet printing of the top gate. The channel length in the published device was estimated to be ~ 60 nm, with an on:off ratio of 10^4 for $V_d < -5$ V [66]. The devices had significant contact resistance, and displayed other short channel effects, which is understandable in a device with such a short channel and thick gate dielectric. (More detailed information on short channel effects, and their amelioration, can be found in Sect. 8.7).

10.5 OTFT Characteristics

10.5.1 General

A representative set of transfer and output characteristics for a Ph-PXX p-channel TFT, with L = 50 μm, is shown in Fig. 10.23a, b, respectively [79]. Similar curves have been published for other high quality p-channel OTFTs, and Fig. 10.14c, d show the equivalent set of characteristics for a P(NDI2OD-T2) n-channel TFT [25]. The Ph-PXX transfer characteristics measured in saturation, at a drain bias of −40 V, are shown in Fig. 10.23a, and the right hand axis is a plot of the square root of drain current versus gate bias. This shows reasonable linearity, and, as with inorganic TFTs, the simple MOSFET equations developed in Chap. 3 were used to extract the performance parameters of OTFTs from their transfer characteristics. In the saturation regime, the field effect mobility is calculated from the slope of the $\sqrt{I_d} - V_G$ plot using Eq. 3.18, i.e.

$$\mu_{FE} = \frac{2L}{WC_i}\left(\frac{d\sqrt{I_d}}{dV_G}\right)^2 \tag{10.4}$$

and the threshold voltage is given by the extrapolated intersection of this curve with the V_G axis. In the example shown, the mobility was ∼0.42 cm^2/Vs, and the threshold voltage was ∼0 V [79]. The output characteristics in Fig. 10.23b show good saturation and negligible current crowding at zero drain bias, which is indicative of good injecting contacts. With these contacts, it would be possible to extract the mobility at low drain bias in the linear regime, however, as injection problems are frequently encountered in OTFTs, the mobility is more commonly extracted in the saturation regime.

Examples of good and bad injecting contacts in TIPS-pentacene TFTs, with Ag source/drain contacts, are shown in Fig. 10.23c, d, respectively [114]. The difference between the two TFTs was in the surface treatment of the Ag electrodes by different thiophenol-based SAMs. These changed the effective work function of the Ag, which, in the good case, was a much closer match to the HOMO of the TIPS-pentacene, and gave the linear $I_d - V_d$ curves at low drain bias in Fig. 10.23c. The key characteristic of the bad contact, in Fig. 10.23d, was the non-linearity of the curves near zero drain bias, which is referred to as current crowding, and would preclude an assessment of field effect mobility in the linear regime. The series resistance associated with this injection barrier was also responsible for the order of magnitude reduction in the current in the saturation regime compared with the good sample. It is worth noting that the impact of series resistance at the injecting contact is also a function of its magnitude relative to the channel resistance, and a good injecting contact, at low gate bias and long channel length, can become a poor one as the channel resistance is decreased by either reducing the channel length and/or increasing the gate bias [53, 117]. Contact effects are discussed further in Sect. 10.5.2.

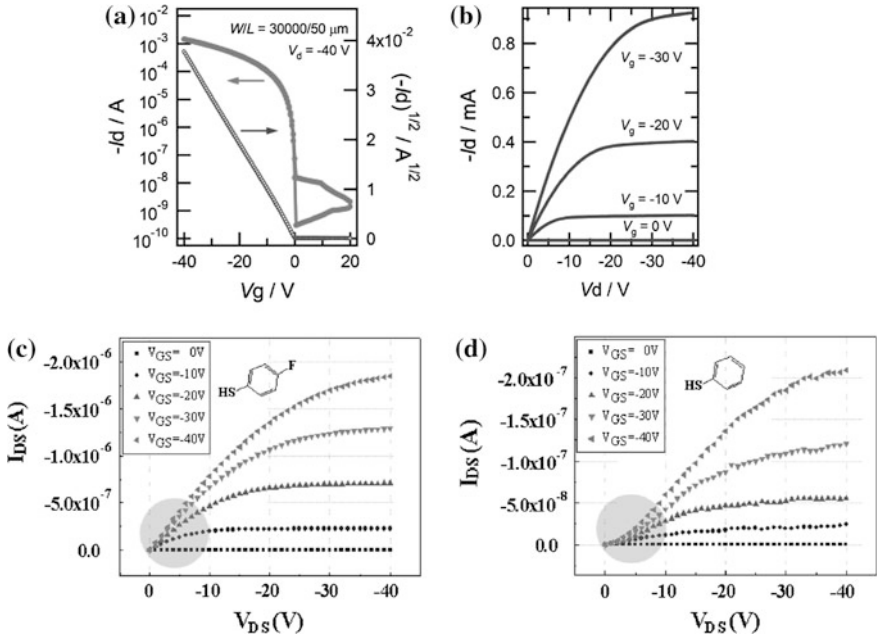

Fig. 10.23 **a** Transfer characteristics, and **b** output characteristics of a Ph-PXX TFT (Reprinted with permission from [79]. Copyright (2009) American Chemical Society). Output characteristics of TIPS-pentacene TFTs, with Ag S/D contacts covered with different thiophenol-based SAMs, showing **c** good, and **d** poor injecting contacts. (Reprinted with permission from [114]. Copyright (2008) American Institute of Physics)

Table 10.1 summarises the parameter values which have been extracted from a number of TFT materials discussed in the preceding sections. The mobility values and on:off current ratios are usually quoted in publications as simple figures of merit, and, where available, the threshold voltage, V_T, and sub-threshold slope, S, values have also been listed. However, these latter parameter values scale inversely with the gate dielectric capacitance, and this needs to be taken into account when comparing V_T and S values between different samples. Unfortunately, the dielectric film thicknesses were not always published, so it is difficult to identify meaningful differences in these parameters across the whole sample set, although the smallest sub-threshold slope of 0.1 V/dec clearly correlates with a very thin gate dielectric of just 5.3 nm [13]. Where the dielectric thicknesses have been quoted, comparisons can be made between the normalised sub-threshold slope values, S_N, in which the measured values have been normalised to a fixed dielectric capacitance of 3.45×10^{-8} Fcm^{-2} (which is equivalent to 100 nm of SiO_2). The smallest S_N value is for the TIPS-pentacene TFT, and is indicative of a lower overall density of trapping states in that material. Comparable, but slightly larger values are seen for the PXX and N3000 TFTs as well, and are also indicative of modest trap state densities, compared with the polymer p-channel materials,

Table 10.1 Summary of basic TFT performance parameters from a range of organic semiconductors

Material	Channel	Gate dielectric	Dielectric thickness (nm)	Mobility (cm^2/Vs)	Threshold voltage (V)	On:off ratio (log_{10})	S (V/dec)	S_N (V/dec)	Ref #
P3HT	p	SiO_2 + HMDS	230	0.05–0.1	–	>6	1–1.5	0.44–0.65	116
PQT-12	p	SiO_2 + OTS	100	0.14	–	>7	1.5	1.5	21
Pentacene	p	SiO_2 + OTS	–	1.00	−5	7	0.5	–	78
DVAnt	p	SiO_2 + OTS	–	1.30	−16	7	0.5	–	78
TIPS-pentacene	p	SiO_2 + HMDS	370	0.65	3.4	8	0.5	0.14	83
PXX	p	PVP/OTS	400	0.40	–	7	0.6	0.17	4, 79
Pentacene	p	AlO_x + SAM	–	0.50	–	>5	–	–	109
DNTT	p	AlO_x + SAM	5.3	0.60	–	6	0.1	–	13
$F_{16}CuPc$	n	AlO_x + SAM	–	0.01	–	>4	–	–	109
P(NDI2OD-T2)	n	PMMA	600–900	0.2–0.45	5–10	6–7	3–5	0.6–0.4	25
N3000	n	D2000	400–700	3.00	–	7	1.0	0.24–0.14	58

S_N is the normalised value of S, using a fixed dielectric capacitance of 3.45×10^{-8} Fcm^{-2}

P3HT and PQT-12. The other general points to note from this table are that the mobility values for the majority of materials are ~0.4 cm^2/Vs or greater, and that the on:off current ratios are 6–7 orders of magnitude, which are sufficient for active matrix addressing.

Although there is near-universal use of the basic MOSFET equations for the simple extraction of carrier mobility and threshold voltage from OTFTs, a compact model, representing a more accurate description of device behaviour, is needed for circuit simulation [45, 118]. As with the inorganic TFTs (see Sects. 6.3.1 and 9.4.2.2), this needs to take account of non-ideal effects such as series resistance, channel length shortening and the dependence of mobility on gate bias. For example, incorporating the effects of series resistance, and the mobility enhancement factor, γ, from Eq. 10.2, the following dependence of channel current on gate and drain bias has been derived [45]:

$$I_d = \frac{W\mu_0 C_i}{L(\gamma+2)}\left[(V_G - V_T - V_S)^{\gamma+2} - (V_G - V_T - V_D)^{\gamma+2}\right] \tag{10.5}$$

where V_S and V_D are the channel potentials adjacent to the source and drain contacts, and reflect both series resistance effects plus any voltage drops across the Schottky barrier contacts themselves. Equation 10.5 is similar to the a-Si:H TFT Eq. 6.38, in which the exponent $\gamma + 2$ is replaced by α, and, in both cases, this represents the influence of the band gap DOS in partitioning the gate-induced charge between free and trapped states. The evaluation of γ, V_S and V_D from experimental OTFT characteristics, and the good fit of the model to the data, is presented in Ref. [118].

10.5.2 Contact Effects

The source and drain metal contacts frequently have a voltage offset between the energy level of their work function and the HOMO (p-channel) or the LUMO (n-channel) levels of the semiconductor channel material. As discussed in Sect. 10.2.4, due to the presence of surface dipole layers, these offsets are often different from expectations based upon the published values of the work functions of clean metals [41]. The source junction is effectively a reverse biased Schottky barrier, and, if the barrier height is too large, severe injection problems will result. For a given choice of semiconductor and dielectric materials, if this injection barrier is too high it can dominate device performance, particularly as channel length reduces [117, 120, 121]. The contact effect may be characterised in terms of an effective series resistance, and channel width-normalised series resistance values spanning the range 10 kΩcm–10 MΩcm have been reported [117]. (To put these values into context, performance artefacts have been noted in poly-Si, AOS and a-Si:H TFTs with series resistance values of 3 Ωcm, 30–250 Ωcm, and 7.8 kΩcm, respectively—for further information on these values see Sects. 8.7.1,

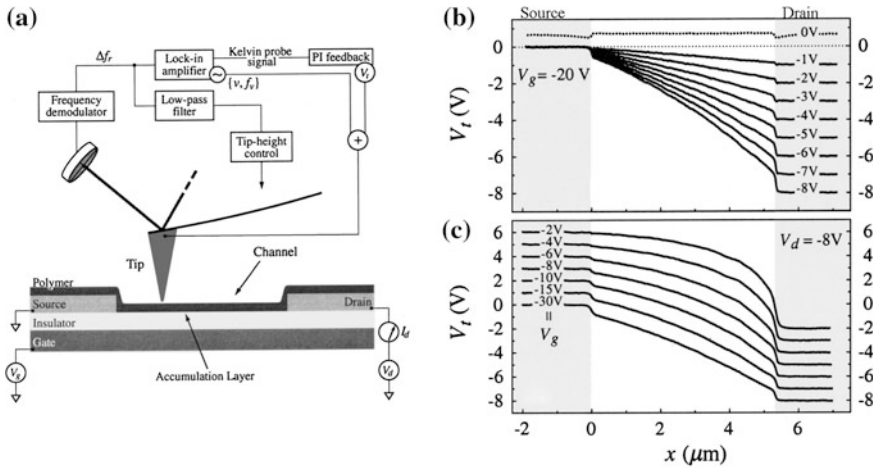

Fig. 10.24 SKPM potentiometry measurements (**a**) measurement setup using an AFM probe head. Surface potential measurements on a P3HT TFT with Au contacts (**b**) in the linear regime with different drain biases, at a fixed gate bias, and **c** different gate biases at a fixed drain bias. (Reprinted with permission from [119]. Copyright (2002) American Institute of Physics)

9.4.1 and 6.3.1, respectively). In view of the large values observed in OTFTs, considerable attention has been paid to the choice of contact materials, and to the evaluation of the injection barriers. This has been by direct barrier measurement in operating TFT structures, using scanning Kelvin probe microscopy [119], as well as by UV photo-electron spectroscopy measurements of dipole layer effects in simpler test structures [24, 38, 39]. These measurements are key contributors to the detailed understanding of the observed series resistance effects in OTFTs. In these studies, several issues were addressed, namely the effect of dipole layers on barrier heights, the injection process at the source [40] and how this translates into a measured resistance, and the influence of device architecture (TC vs BC) on the total series resistance. For instance, in the TC structure, there is vertical current flow through the body of the semiconductor, whilst in BC structures the current injection may be limited to the edge of the source contact adjacent to the channel. An overview of investigations into contact and parasitic resistance effects in OTFTs is presented below.

Non-contact, scanning Kelvin probe microscopy, SKPM, which is based upon the use of a scanning force microscope, has been used to measure the semiconductor voltage along the surface of an operating BG/BC TFT [119], and 2-D device simulations confirmed that the surface potential closely followed the channel potential [122]. The experimental set-up is shown in Fig. 10.24a, and the voltage on the conducting tip of the probe is proportional to the channel potential. Figures 10.24b, c show the potential measurements made along the surface of a P3HT TFT with gold contacts and 5.2 μm channel length [119]. In the first case, with a gate voltage of −20 V, the device continued to operate in the linear regime

as drain bias increased from −1 to −8 V, and in (c) the device went from the saturation regime to the linear regime when the gate bias increased from −2 to −30 V, with a fixed drain bias of −8 V. These profiles confirmed the applicability of the simple, first order MOSFET model, with good linear potential drops along the channel in the linear regime, and a progressive transfer of voltage to the drain end of the channel as the device moved into saturation. The steep voltage drops, ΔV, at either end of the channel in the linear regime were due to the contact resistances, R_c, which can be simply evaluated as $\Delta V/I_d$, where I_d is the channel current. In this sample, ΔV was the same at both ends of the channel, and the total series resistance was 50 kΩcm. As will be seen below, the situation in which $\Delta V_s = \Delta V_d$ is indicative of a low injection barrier, and there are many examples in which the inappropriate choice of contact metal led to significantly larger values of ΔV_s at the source end of the channel. In other measurements, the voltage drop at the drain was not observed [123], and 2-D simulations have demonstrated that this voltage drop can be associated with low mobility, disordered material adjacent to the contacts [124]. The disorder had the effect of restricting current flow at the vertical edges of the contacts, and forcing it along the horizontal surface of the contacts, where the carrier density was much lower than in the channel.

The field effect mobility, and its field dependence, was also extracted from the potential profiles using:

$$I_d = W\mu_{FE}(V_G, V(x))C_i[V_G - V(x)]dV(x)/dx \tag{10.6}$$

The SKPM procedure has been applied to a variety of materials and contact metals, including P3HT [117, 119], F8T2 [117] and pentacene [123]. Figures 10.25a, b show further measurements on P3HT with Cr-Au contacts (where Cr was used as an adhesion layer on the SiO_2 gate dielectric) and Cr contacts, respectively [117]. These measurements were made in the linear regime at $V_G = -40$ V and $V_d = -8$ V, and the Au contact results, in Fig. 10.25a, were consistent with the comparable measurements in Fig. 10.24b, c. In particular, the values of ΔV_s and ΔV_d were very similar, whilst, for the Cr contact, $\Delta V_s > \Delta V_d$, and this was taken to be indicative of a substantial injection barrier at the Cr source contact. The value of ΔV_s at the source end of the channel is a direct measure of the reverse bias developed across the Cr Schottky barrier contact at the source, and it reduces both the effective gate-source and source-drain biases to $V_G - \Delta V_s$, and $V_d - \Delta V_s$, respectively. The consequence of this is a self-consistent reduction in channel current, for the given terminal biases V_G and V_d, as is required for current continuity through the large source barrier and the channel.

Taking the ionisation potential, IP, of P3HT to be 5.0 eV, the difference in injection barriers in Fig. 10.25a, b correlated with the different work functions, Φ_M, of Au (5.2 eV) and Cr (4.7 eV). (In this work, the dipole barrier was not measured, but it was assumed that the usual reduction in effective work function would be comparable for Au and Cr, and that Au would, therefore, give the smaller injection barrier [117], whilst the barrier would be >0.3 eV with Cr). From the values of ΔV_s

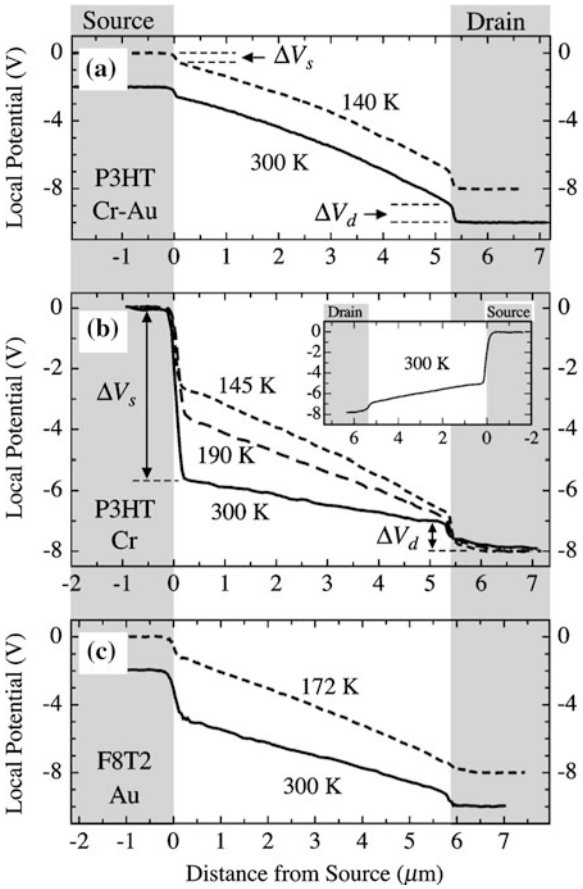

Fig. 10.25 SKPM measurements on P3HT and F8T2 TFTs with Au or Cr contact metals **a** P3HT with Cr-Au, **b** P3HT with Cr, and **c** F8T2 with Au. (Reprinted with permission from [117]. Copyright (2003) American Institute of Physics)

and ΔV_d, the total series resistance was estimated to be 5400 kΩcm for Cr and 22 kΩcm for Au. The more usual way of determining series resistance is from the channel length dependence of the drain current at fixed gate voltages, and the SPKM measurements agreed well with those measurements [117]. (For further information on the conventional series resistance measurement, the background to it was presented in Sect. 9.4.1). Finally, the difference in injection barriers identified by SKPM correlated with low-voltage current crowding in the output characteristics of the TFTs with Cr contacts, whilst it was absent with the Au contacts.

Figure 10.25c shows SKPM measurements on an F8T2 TFT with Au contacts. In contrast to the measurements of P3HT TFTs with Au contacts, F8T2, which has an IP of 5.5 eV, displayed a substantial injection barrier at the source contact, which correlated with a value of $\Phi_M - IP > 0.3$ eV [117].

Carrier flow over the barrier is often assumed to be due to thermionic emission in 2-D modelling work on OTFTs [121], but analysis of the temperature dependence of both the barrier height and the carrier mobility argued against this simple model, and favoured a thermally assisted tunnelling process [117].

As is apparent from Fig. 10.25, the forward-biased drain junction was not found to present a significant barrier to current flow in any sample. However, the small barrier at this junction did represent an element of series resistance, which was also present at the source of the Cr-Au P3HT TFT. This resistance was found to scale inversely with the carrier mobility of the material, and was attributed to carrier flow through a narrow depletion region at the edge of the drain junction. This was also assumed to be the case at the source junction in the Cr-Au P3HT TFT, where the injection barrier was estimated to be close to zero [117].

The above results were for polymer semiconductors, and broadly similar effects have been seen with pentacene TFTs. For example, measurements of SKPM and of the output characteristic of BC TFTs, with the dual-metal contacts of Pd and Pt, gave the results shown in Fig. 10.26a, b, respectively [123]. The SKPM measurement showed a near-zero injection barrier when Pt was used as the source contact (and Pd as the drain), but a substantially larger one with the contacts reversed, with Pd as the source. This correlated with the greater current crowding in the output characteristics when Pd was used as the source contact. Whilst the dipole layers on the metals were not directly measured, the injection barrier differences were consistent with the different work functions of $\sim$5.8 and 5.1 eV for Pt and Pd, respectively [41]. However, in measurements of TFTs with Pd and Ni dual-metal contacts, which have similar work functions, the use of Ni as the source contact showed a much larger injection barrier than Pd, and also worse current crowding. This was attributed to oxidation of the Ni surface during UV-ozone cleaning of the substrates prior to the pentacene deposition. The dipole layers were not measured on these samples, but these results indicate the varying sensitivities of different metal surfaces to chemical exposure, as has also been reported for Au [24]. The contact resistance values were directly evaluated from measurements of the channel length dependence of the total device resistance, as a function of gate bias, in Pd-contacted TFTs [121]. These characteristics were de-convolved (as discussed in Sect. 9.4.1) to separate the channel and parasitic resistances, and are shown in Fig. 10.26c. The resistance curves demonstrate that the parasitic resistance was comparable to, and about 3 times less than, the channel resistances in 10 μm and 30 μm channel length TFTs, respectively. Hence, the injection barrier associated with the Pd contacts had an increasing impact upon the operation of TFTs as the channel length reduced from 30 μm, and the series resistance associated with Au contacts was even higher in this work [121]. The width normalised contact resistances at $V_G = -20$ V were 6.9 kΩcm and 51 kΩcm for Pd and Au, respectively.

It is apparent from these results that the contact resistance in OTFTs consists of two separate elements: a carrier transport resistance between the channel and the source and drain contacts (which is comparable at both contacts), and, secondly, where there is a large offset between the carrier band (HOMO or LUMO) and the metal work function, an injection barrier resistance at the source electrode, which can exceed the transport resistance. Hence, the overall series resistance is sensitive to the choice of metal, and its chemical exposure, and to the choice of semiconductor, particularly its carrier mobility. In addition, the resistance is also affected by the use of SAM layers in BC TFTs to improve the molecular organisation of the

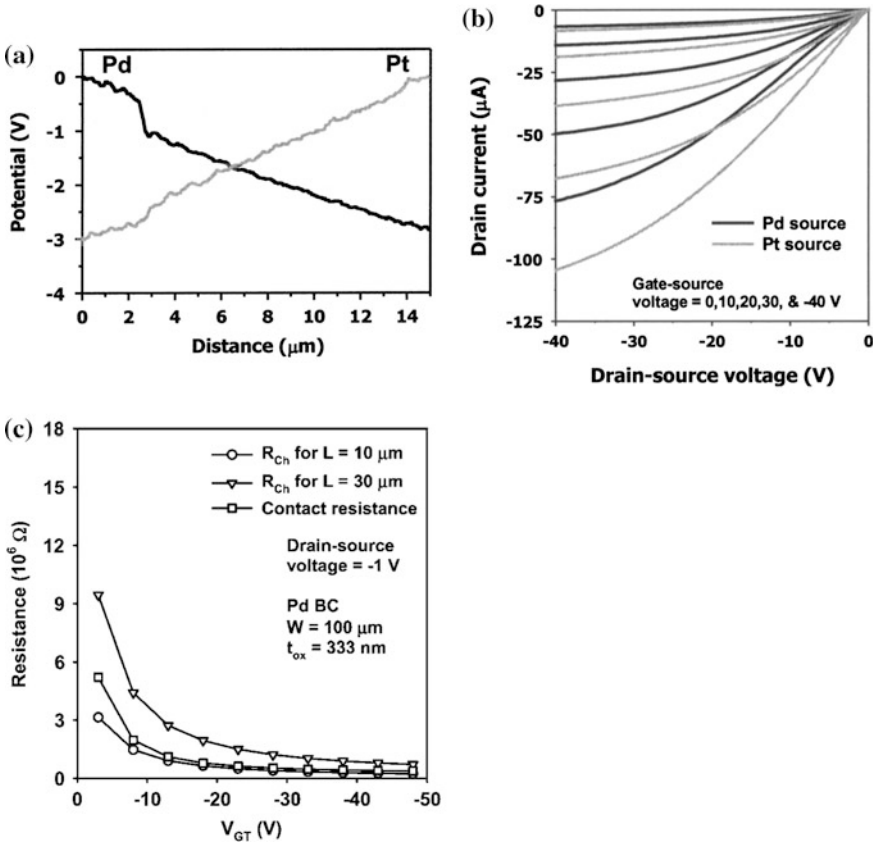

Fig. 10.26 Measurements of pentacene TFTs with reversible Pt and Pd dual-metal source/drain contacts. **a** SKPM measurements. **b** output characteristics (Reprinted with permission from [123]. Copyright (2003) American Institute of Physics). **c** Channel and series resistance values as function of V_G on Pd-contacted BG/BC pentacene TFTs. (Reprinted with permission from [121]. Copyright (2006) American Institute of Physics)

semiconductor material on the electrode itself. Improved understanding and optimisation of contact resistance is an on-going activity [40, 122, 125], and is essential for the meaningful reduction of channel length, L, in order to improve OTFT circuit speed. Indeed, speed will only scale as $1/L^2$, when the series resistance is significantly less than channel resistance.

10.5.3 Contact Architecture

Given the importance of the contact effects discussed in the preceding section, there has been much interest in whether top or bottom contact devices display different

contact limitations in their performance. For instance, with staggered BG/TC (or TG/BC) devices there is a requirement for vertical current flow through the bulk of the device, from the channel to the contacts, which is film thickness dependent [53, 126]. On the other hand, there is more opportunity in the staggered device for the channel current to be distributed along the width of the contacts, due to the overlap of the gate and contact electrodes [126], whereas, in a coplanar BG/BC structure, the current flow is limited to the contact electrode edges.

So far as TFT measurements are concerned, there are varied reports on the relative values of contact resistance in BG/BC and BG/TC TFTs. For pentacene with Au contacts, in some studies the BC TFTs were observed to have the higher contact resistance [121, 127]. In other work, whilst the lowest resistance was found with 20 nm thick pentacene films in TC structures, the resistance in the TC structures increased with film thickness, and lower contact resistance was found in the BC TFTs with 40-80 nm thick pentacene films [53]. For Pd-contacted pentacene films, the contact resistance was lowest in BC structures at low gate bias, and it then became lower in TC devices as the gate bias increased [128]. These different experimental results are no doubt related to subtle differences in device technology and processing.

A more fundamental investigation of contact effects can be obtained from 2-D device simulation, and, in these studies, TC devices have been consistently found to have lower values of contact resistance, and better performance, than BC structures [121, 122, 129]. This has been partially explained by the carrier tail from the channel extending into the substrate, and reducing the bulk resistance, and also by the spreading of the carriers along the contacts themselves. An example of the computed difference between TC and BC structures is shown in Fig. 10.27, in which the output characteristics were calculated for three different injection barrier heights of 0, 0.2 and 0.3 eV [121]. For the 0 eV barrier, the two sets of curves were identical, indicating that, in these calculations, the differences in transport resistance were negligible between the two architectures. However, as the barrier height increased, the device operation was modulated by the size of the injection barrier, and this effect was far greater in the BC TFT. In explaining these, and

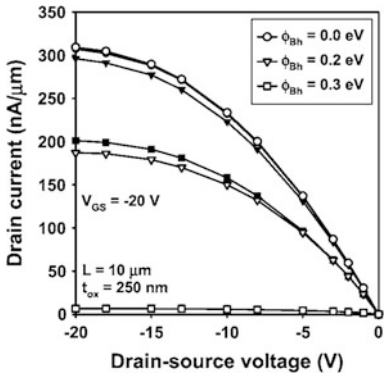

Fig. 10.27 2-D simulation of TC (filled symbols) and BC (open symbols) TFTs, with source injection barriers of 0.0, 0.2, and 0.3 eV. (Reprinted with permission from [121]. Copyright (2006) American Institute of Physics)

other TC simulations, one topic which was not reported was the capacitive coupling of the gate to the Schottky barrier source contact, and the influence of the gate bias on the injection barrier height at the TC. It has also been noted that injection barriers of <0.3 eV are needed for the efficient operation of OLEDs, whereas the operation of OTFTs seems to be tolerant of apparently much larger barriers [131]. An obvious difference between the OLED and the TFT structures is the presence of the gate in the latter, and, in subsequent work [130–132], there has been increasing recognition of the role of the gate bias in modulating the height of the reverse biased source barrier.

In one case [130], dealing with poly-crystalline material in staggered OTFTs, it was reported that the hole accumulation layer, induced by the gate bias, increased the field at the source and lowered the source barrier by the Schottky effect [133]. In another publication [131], 2-D simulation was used to compare gate-bias-induced barrier lowering in coplanar and staggered TFTs. In the coplanar TFTs, the direct Schottky effect was identified between the edge of the source contact and the adjacent hole accumulation layer, with a continuous reduction in barrier height with increased gate bias. The Schottky effect was also invoked for the staggered structure, but it was shown that the effect saturated at large gate biases. The saturation was attributed to the hole accumulation layer, on the opposite side of the film from the source, screening the source contact from further increases in the gate-induced space charge field. However, these evaluations were carried out at low values of reverse bias on the source, and did not allow for the increased field at the source once its reverse bias was increased, and started to deplete the hole accumulation layer [134]. Indeed, in a comprehensive 2-D numerical analysis of staggered OTFTs, it was shown that the field at the source was due to the combination of both the gate bias and the source reverse bias, and that gate bias alone (at low values of V_D) had only a very small impact upon the source barrier height [132]. This work demonstrated significant barrier lowering at the source contact due to the combined effects of the gate and source biases. Whilst these papers have identified the involvement of the gate in barrier height control in OTFTs, there is presently not a consensus on the precise details, and further analysis can be anticipated on the broad topic of gate-bias-controlled series resistance effects in OTFTs.

In this context, it is worth mentioning a novel form of TFT, called the Source-Gated Transistor, SGT, which has both a BG/TC structure, and a Schottky barrier source. In the SGT, it is argued that, in saturation, the height of the reverse biased source barrier is controlled by the electrostatic coupling of the gate potential, and this determines the source-drain current in injection-limited structures [134–136]. Moreover, 2-D simulations of these structures have indicated that they can enhance the performance of low mobility organic materials compared with their use in conventional TFTs [136]. The physics of SGT operation is presented in Chap. 12, where the current understanding of SGT behaviour is compared with recent analyses of source barrier effects in OTFTs.

10.6 Instability Effects

A variety of instability effects have been observed in OTFTs, and, to a certain extent, these reflect the different materials, transistor designs, and preparation techniques used with these devices [137]. Nevertheless, it is possible to define some of the more common and representative instabilities, including ambient instability, hysteresis during sample measurement, and longer-term bias stress instability. It should be noted that the specific details are likely to be a function of the particular organic semiconductor, its gate dielectric, and the conditions under which the instability is assessed. For instance, depending upon the materials, the ambient has been found to have an important effect, as demonstrated by differences observed between devices measured in vacuum, dry gases, air, and high humidity environments.

10.6.1 Air-Instability

Air-instability is related to the material's sensitivity to the presence of oxygen and water, which are able to diffuse through many semiconductor materials, and to cause an oxidising reaction. Oxidation is a process involving electron transfer from the host material to the oxidant [18], and the more tightly bound the electrons are in the host, the lower its susceptibility to this process. Hence, for a p-channel organic semiconductor, the greater its ionisation potential (or HOMO level), the more air-stable it should be. The same argument applies with respect to the LUMO level of a semiconductor under electron accumulation (i.e. for an n-channel device in the on-state), and the deeper the LUMO level is the more air-stable it should be.

As mentioned in Sect. 10.4.2, the air-instability effect most commonly observed was a reduction in carrier mobility, due to trap creation by the oxidation reactions, but changes in threshold voltage and off-current have been noted as well [76]. Amongst the more widely studied p-channel TFT materials, pentacene and P3HT were shown to be affected by air exposure, and more stable materials, such as DNTT [13], DVAnt [78], have been developed with deeper HOMO levels. An alternative approach was to change the molecular structure, such as with Ph-PXX [4, 79], in which substituents were added to the periphery of the molecule to passivate reactive sites, and thereby reduce its sensitivity to oxygen. A comparison of the air stability of pentacene and Ph-PXX is shown in Fig. 10.28a, and illustrates the much better ambient stability of Ph-PXX. Similarly, PQT-12 has a modified molecular structure compared with P3HT, which improved its oxidative stability, even though its HOMO was only 0.1 eV deeper [21].

Early n-channel materials, which were used in TFTs were made on SiO_2 gate dielectrics, were very sensitive to oxidation by silanols on the insulator surface. This reaction resulted in the formation of electron traps, which suppressed electron conduction, and also precluded ambipolar behaviour in good p-channel materials

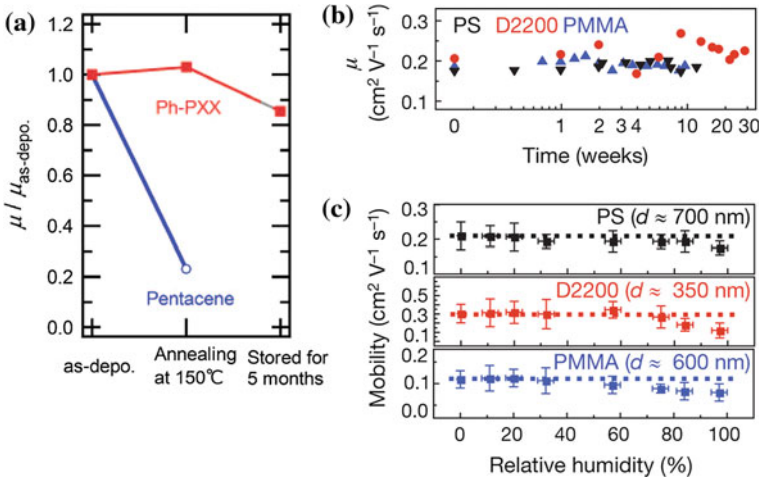

Fig. 10.28 **a** Comparison of the air-stability of pentacene and Ph-PXX TFTs (Reprinted with permission from [79]. Copyright (2009) American Chemical Society). Stability of electron mobility in n-channel P(NDI2OD-T2) TFTs with different gate dielectrics {PMMA, PS (polystyrene), and commercial D2200 (polyolefin-polyacrylate)}: **b** During ambient storage at relative humidity levels of 20–60 %, and **c** after 24 h storage at different humidity levels. (Reprinted by permission from Macmillan Publishers Ltd: Nature [25], copyright (2009))

[36]. Hydroxyl-free insulators, such as BCB, polyethylene, PMMA and parylene were demonstrated to remove/reduce this electron trapping problem, and gave good n-channel behaviour [36]. However, n-channel materials were still sensitive to air-degradation, due to the diffusion of oxygen and water through the film, and it was predicted that the LUMO level had to be deeper than ∼4 eV to suppress the oxidation reaction [92]. Good air-stability was subsequently demonstrated with the n-channel materials F_{16}CuPc [93], and FPTBBT [94], having LUMO levels of 4.8 eV and 5.05 eV, respectively. An alternative approach was to use a dense molecular structure to impede the ingress of oxidants, and high performance, air-stable n-channel TFTs were obtained with P(NDI2OD-T2) [25], although its LUMO level was only ∼4.0 eV. The excellent air-stability of the electron mobility in P(NDI2OD-T2) TFTs, with different gate dielectrics, is shown in Fig. 10.28b, and these devices also displayed good stability at relative humidity levels up to ∼60 %, as seen in Fig. 10.28c [25].

10.6.2 Gate Bias Stress Instability

Given the earlier development of high quality p-channel TFTs, a substantial body of work has been published on the bias-stress instability of these devices. By and large, the most significant instability has been under gate bias stress, with the drain bias having a relatively minor effect (as with a-Si:H TFTs). As bias stress instability is

such a fundamental aspect of device performance, most semiconductor and gate dielectric materials of interest have been routinely evaluated under gate bias stress. The most common instability was an increase in threshold voltage towards the value of the stress bias. In other words, there was a negative shift in threshold voltage with negative gate bias stress, and a positive shift with positive bias stress. This has been particularly true with the SiO_2 gate dielectric, which, in many studies, was deliberately chosen as a highly stable material, in order to focus on the instability within the organic semiconductor itself. However, it should also be noted that some TFTs with organic dielectrics, such as PVP [138, 139], have given the opposite polarity shifts, where the TFT behaviour has been dominated by instabilities within the organic dielectric material.

The typical features of gate bias stress instability include the polarity effect described above, in which the saturated shift in threshold voltage tended towards the value of the gate bias stress voltage. This direction of threshold voltage shift is also equivalent to a reduction in the on-current at a fixed value of gate bias, as can be seen in Fig. 10.29a. This figure shows the time dependent change in the transfer characteristics, due to the application of a gate bias stress of −20 V to a PTAA TFT with a thermally grown SiO_2 gate dielectric [140]. The change, which is characteristic of this type of instability, was initially rapid (and could be observed on a time scale of seconds), but it progressively slowed down, and continued over periods of hours or more. In view of the extensive time scale of the effect, it is frequently represented on a logarithmic time axis, as shown in Fig. 10.29c. Moreover, given the initially fast rate of change, the threshold instability may also be observed as hysteresis in a transfer characteristic between the outward and return gate voltage sweeps. The time dependence can be empirically fitted with a stretched exponential [137, 140–142], as shown by the dashed line in Fig. 10.29c [140]. The trends shown for the PTAA TFT in Fig. 10.29 have also been found in similarly prepared devices containing the following alternative channel materials: pentacene, P3HT, F8T2, PTV (polythienylene-vinylene), and 3-BuT5 (3-butyl-quinquethiophene) [140, 141]. Similar results have also been measured in single crystal rubrene, TIPS-pentacene, and tetracene TFTs on parylene dielectric layers [142].

The stretched exponential fitted to the data in Fig. 10.29c has the form:

$$\Delta V_T = V_0\{1 - \exp -(t/\tau)^{\beta}\} \tag{10.7}$$

where $V_0 \sim V_{Gstress}$, the exponent β was weakly temperature dependent, with a value in the range 0–1, and the characteristic relaxation time, τ, was thermally activated, and given by:

$$\tau = \tau_0 \exp(E_A/kT) \tag{10.8}$$

For the device shown in Fig. 10.29c, which was measured in air at 30 °C, the fitted parameter values were $V_0 = 19$ V, $\beta = 0.43$, $\tau = 10^4$ s, and the activation energy, E_A, was ~0.6 eV [140]. However, when stressing in vacuum, the instability was much slower, with $\tau = 10^6$s, although the other parameters remained much the same. Similar behaviour was seen with the semiconductors pentacene,

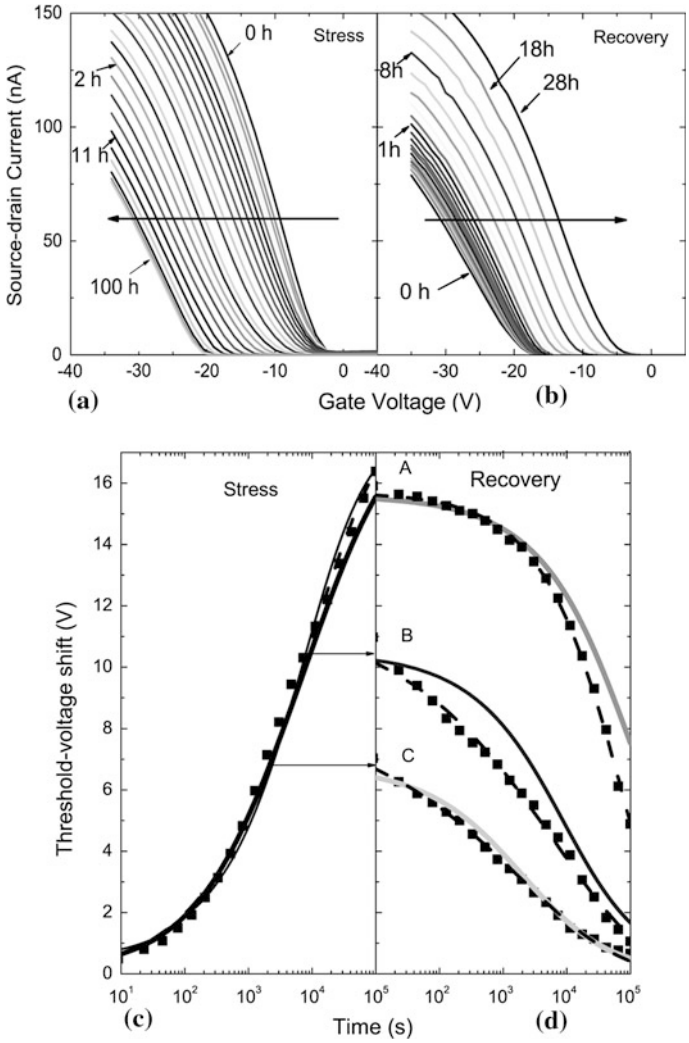

Fig. 10.29 Transfer curves measured on a PTAA TFT as a function of time in air **a** with −20 V gate bias stress, **b** recovery after removal of gate bias, **c** gate bias stress data (*symbols*), and fitted stretched exponential (*dashed line*), and **d** recovery data (*symbols*), and fitted stretched exponential (*dashed line*) (Reprinted with permission from [140]. Copyright (2010) by the American Physical Society)

P3HT, F8T2, PTV, and 3-BuT5, and, in particular, they all had comparable activation energies of ∼0.6 eV, indicating the same underlying instability mechanism. Where they differed was in the values of their relaxation time, τ, which scaled inversely with the HOMO level of the semiconductor, as shown by the results in Fig. 10.30 (taken at 25 °C, in vacuum) [141]. In this plot, the materials with the deepest HOMO levels were the least stable. A qualitatively

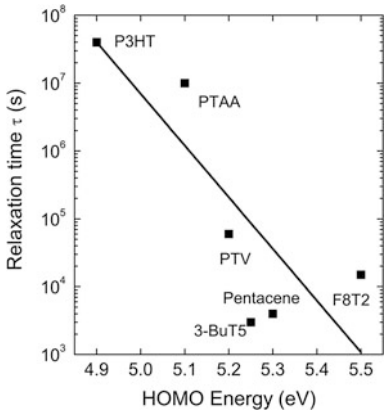

Fig. 10.30 Variation of the characteristic stress relaxation time, τ (at 25 °C in vacuum) with the HOMO level of the semiconductor. (Reprinted with permission from [141]. Copyright (2011) American Institute of Physics)

similar dependence of relaxation time on the HOMO level was also seen with the single crystal samples of rubrene, TIPS-pentacene and tetracene, albeit with a smaller slope than the data in Fig. 10.30 [142], indicating that these broad trends are quite common.

The other common features to the instability process are that it is reversible once the gate bias is removed, as shown in Fig. 10.29b, and that the time dependence could also be fitted with a stretched exponential, as shown by the dashed lines in Fig. 10.29d [140]. There are three sets of recovery data in this figure, which started at different points in the stress cycle (as indicated by the arrows from Fig. 10.29c), and one of the key features of the recovery process was that the fitted recovery time, τ, increased with the duration of the initial stress, t_s. The τ values were 7.7×10^4 s, 6.5×10^3 s, and 2×10^3 s for curves A ($t_s = 10^5$ s), B ($t_s = 10^4$ s), and C ($t_s = 2 \times 10^3$ s), respectively. Hence, the characteristic recovery time was more than 100 times longer for the stress of 10^5 s (curve A) than it was the 2×10^3 s stress (curve C). The correlation between the stress duration and the recovery speed has been reported previously in PQT-12 [143], and, in some cases, authors have noted that full recovery had not been achieved within a given recovery time [142, 143].

The type of gate bias instability seen in Fig. 10.29a has been widely observed, and attributed to carrier trapping either in the semiconductor, in the dielectric or at the interface [137]. However, in interpreting the instability effects in Fig. 10.29, account was taken of the fact that humidity has been found to strongly influence gate bias stability, and, in the cited results, there were large differences in the relaxation times between vacuum and air stressing, and that gate bias instability was greatly reduced with the hydrophobic gate insulator Cytop [140]. This indicated that water played a role in the instability, and the instability was attributed to proton generation from water at the semiconductor/SiO_2 interface, and its subsequent diffusion into the gate dielectric. One of the reasons for proposing proton participation was because its activation energy for diffusion in SiO_2 was 0.5 eV, and this was comparable to the instability activation energy of $\sim$0.6 eV [140,

144]. The detailed microscopic model involved an electrolytic reaction between free holes and water molecules at the semiconductor/SiO_2 interface, which produced protons by:

$$2H_2O + 4OS^+ \Rightarrow 4H^+ + O_2 + 4OS \tag{10.9}$$

and the reverse reaction of protons back to holes:

$$2H^+ + 2OS \Rightarrow H_2 + 2OS^+ \tag{10.10}$$

where OS^+ and OS represent holes and neutral sites in the semiconductor, respectively. Hence, the instability was triggered by the conversion of free holes into protons, and the establishment of equilibrium densities of protons across the interface. This was assumed to be a fast process, and the dynamics of the instability were governed by the diffusion of the protons away from the interface, into the gate oxide. The role played by the individual semiconductor HOMO level was in stimulating the reaction shown in Eq. 10.9, because a free hole density (equivalent to an absence of electrons) in the semiconductor can be regarded as representing the oxidised state of the material, and, the deeper the HOMO is, the less stable the oxidised state, OS^+, is [140, 141]. Hence, this carrier driven instability is the opposite of the ambient instability, in which the most unstable samples are those with the shallowest HOMO levels.

The model also accounted for the recovery behaviour of the material, since removing the gate bias removed the hole accumulation layer, and this disturbed the equilibrium between holes and protons at the interface. The absence of holes stimulated the back reaction at the interface (Eq. 10.10), and produced a reverse diffusion gradient of protons back to the interface. Hence, the longer the bias-stress period, the further the protons had diffused into the oxide, and the longer it took them to return to the interface, where they were neutralised by conversion into holes, and were then swept into the contacts. (The solid lines in Fig. 10.29 were based upon the detailed kinetics of the proton diffusion controlled instability model [140], although the generation of protons has not been confirmed by direct measurements [144]). The conclusion drawn from this work was that water had to be suppressed from the material in order to achieve good bias stress stability.

As mentioned above, the single crystal samples of rubrene, TIPS-pentacene and tetracene displayed qualitatively similar results, but a different microscopic model was advanced. In this model, the holes were captured in a distribution of tail states above the HOMO level in the parylene dielectric, and the deeper the semiconductor HOMO level, the greater the density of tail states available to it in the parylene. Once captured in the tail states of the dielectric, the holes then drifted towards the gate electrode under the influence of the gate field [142]. With the parylene and tetracene HOMO levels at $\sim$7.0, and 6.2 eV, respectively, tetracene showed much faster instability than rubrene, with its shallower HOMO at 4.2 eV. The detailed kinetics of this instability model, based upon the drift of holes in the dielectric, gave a stretched hyperbolic function, which was fitted to the data [142].

There are evidently qualitatively similar gate bias stress results across a range of organic semiconductors, with the semiconductor's HOMO level playing an important role, but no current agreement on a common microscopic model.

Finally, it is worth noting the role of the dielectric layer in qualitatively changing the type of results discussed above. In particular, those instances in which the polarity of the instability has been reversed, whereby a negative gate bias produced a positive threshold voltage shift. This is also related to ambient effects, in that it has been observed for PVP stressed in air [138, 139] and also for PVA [145], but not for PVP stressed in vacuum, where the normal polarity of threshold voltage shift was displayed [139]. The anomalous threshold voltage shift [146] has been variously attributed to electron injection from the gate electrode [138, 145], the movement of ionic impurities, or the polarization of water molecules in the dielectric, given its sensitivity to moisture in the atmosphere [147]. In most of those studies the dielectric was thermally cross-linked, and it was shown that deep UV curing of the material led to more complete cross-linking, and suppressed the instability [146]. For the above two dielectrics, ambient moisture played a role in the bias instability, as was also cited for the proton diffusion model in SiO_2 [140, 141], and better device stability has been reported with a moisture-excluding, hydrophobic dielectric, such as Cytop [148].

In summary, whilst devices with good bias-stability (comparable to a-Si:H TFTs) have been demonstrated [96, 137], there is a complex range of phenomena present in OTFTs, involving both the semiconductor and dielectric materials, as well as their sensitivity to ambient effects. In addition, there are different microscopic models for seemingly similar phenomena, and it is presently unclear whether there are, indeed, quite distinct instability mechanisms taking place in different material combinations.

10.7 Summary

A large number of organic TFT materials now display carrier mobility values approaching, or exceeding, those of the bench-mark TFT for the flat panel display industry, namely a-Si:H. This has stimulated considerable interest in using OTFTs for low cost, flexible substrate applications, such as RFID tags, and e-reader displays. Indeed, many research demonstrator displays have been presented, not just for AMEPDs, but for AMLCDs and AMOLEDs as well.

The current organic semiconductors of choice have been engineered with the appropriate molecular structure and ordering to give efficient charge transport in a TFT structure, and a wide range of both small molecule and polymer materials have been identified. Generally, better performance is obtained from vacuum-deposited small molecule materials, but polymer materials more readily lend themselves to lower-cost, solution processing. However, a range of solution-processable small molecule materials have now also been developed. Initial materials research used oxidised Si as a combined gate electrode and gate

dielectric, but this is not practical for commercial applications, and, in tandem with the semiconductor developments, considerable attention has been paid to alternative dielectrics. These have included both low temperature inorganic dielectrics, as well as a range of organic insulators, and there is continuing research to optimise the use of these materials.

The typical device architecture is a non-self-aligned structure, similar to those used for a-Si:H and amorphous oxide TFTs, although, unlike those technologies, there is not one clearly preferred architecture. Equally, the industry has not identified a particular combination of semiconductor and dielectric layers as optimum, with a range of materials continuing to be used in research demonstrator displays.

As with other TFT materials, OTFTs display various instabilities, including ambient and gate bias stress instability. The ambient instabilities have been addressed both by modifying the molecular structure of the material to reduce its sensitivity to oxygen and water, or by decreasing its permeability to these molecules. Gate bias instability most commonly results in a threshold voltage shift of the same polarity as the stress bias, and, in a number of cases, the instability time constant has been related to the depth of the semiconductor's HOMO level. However, there is not a single, accepted microscopic model for the underlying the instabilities. At a practical level, gate bias instabilities in well engineered structures have been demonstrated to match those of a-Si:H TFTs, and the appearance of a first AMEPD product has been slated for 2012.

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