Materials Processing

4

Materials processing by implantation of energetic ions into solid surfaces has been applied in many fields of modern production technologies. For the last 40 years, ion implantation became the key technology especially in semiconductor technology for the production of ultra-large-scale integrated (ULSI) circuits, for example, silicon processors and memory devices. The type and value of semiconductor conductivity can be selected by the type and amount of implanted doping ions, for example, implantation of boron, gallium, or indium ions for p-type doping and of phosphorous, arsenic, or antimony ions for n-type doping of silicon. The necessary dopant concentration to be implanted is below 0.1 at.%. On the other hand by implanting high ion fluences, high impurity concentrations of tens of at.% can be achieved giving the possibility to synthesize buried layers of compound materials, for example SiO_2 layers in Si by high fluence oxygen ion implantation. The well-known relations between ion energy and ion penetration depth for all important dopant–semiconductor combinations meet the demands of microelectronic technology for introducing doping concentrations with an error smaller than ± 1 %. Lateral doping homogeneities over large wafer areas with an error of ~1 %, multiple implantation steps of different ions without significant interaction of the introduced dopants are standard for the ion implantation technique. Ion implantation is the only doping technique for the fabrication of device structures with dimensions in the nanometer range.

The knowledge of fundamentals of ion–solid interactions, mainly the penetration depth or ion depth distribution in the material as described in Chap. 2 is the prerequisite for the application of ion implantation in materials processing.

4.1 Ion Irradiation Effects in Crystalline Materials

At ion irradiation of solids (mostly called ion implantation) energetic ions penetrate into the material to a range R proportional to the ion energy E, whereas the concentration of the introduced impurity atoms N is directly proportional to the ion current density j or the ion fluence Φ. Due to magnetic ion mass separation

B. Schmidt and K. Wetzig, *Ion Beams in Materials Processing and Analysis*,
DOI 10.1007/978-3-211-99356-9_4,

the purity of introduced atoms is extremely high. Furthermore, impurity concentrations above their solubility limit in the solid target can be easily achieved, because ion implantation concerns a thermodynamic nonequilibrium process. The shape and depth position $N(x)$ can be adjusted by variation of the ion energy and the incidence angle of the ion beam relative to the sample surface normal. Usually the low target temperature prevents in-diffusion of disturbing other impurities from the ambient. Doping by ion implantation causes structural changes (radiation damage) which are especially important in crystalline targets (e.g., semiconductors), overlaying the doping process. Therefore, subsequent thermal annealing of ion beam-induced crystal defects by re-crystallization of the crystal lattice and the simultaneous electrical activation of impurity atoms (localization of dopants on crystal lattice sites) is an integral part of ion implantation in many cases.

4.1.1 Depth Profiles and Ion Channeling

The ion distribution $N(x)$ [see (2.26) in Chap. 2] normally distributed around R_p drops by one, two, and five decades at the following depth values x, respectively,

$$\begin{aligned} N(x) &= 10^{-1} \cdot N_{max} \quad \text{at} \quad x = R_p \pm 2 \cdot \Delta R_p, \\ N(x) &= 10^{-2} \cdot N_{max} \quad \text{at} \quad x = R_p \pm 3 \cdot \Delta R_p, \\ N(x) &= 10^{-5} \cdot N_{max} \quad \text{at} \quad x = R_p \pm 4.8 \cdot \Delta R_p. \end{aligned} \tag{4.1}$$

The values x in (4.1) can be used for the estimation of necessary layer thicknesses for implantation masking on patterned substrates.

The three-dimensional $N(x, y, z)$ ion distribution including the transversal ion straggling ΔR_l for example at the edge of an implantation mask in the y-direction can be approximated by simple Gaussian distributions, with two straggling parameters ΔR_p (longitudinal straggling) and ΔR_l (lateral straggling).

The ratio of lateral and longitudinal ion straggling $\Delta R_l/\Delta R_p$ has been determined in [1]. For masks with perpendicular edges one has taken into account that there exists a lateral straggling component underneath the mask but due to masking the opposite component is missing. Therefore, the impurity concentration near to the edge is lower compared to implanted areas which are far from the mask edge at least by the lateral straggling ΔR_l. Directly below the mask edge the concentration amounts $N(y) = N_{max}/2$. For light ions the lateral straggling is slightly higher compared to the longitudinal straggling. For heavy ions the lateral broadening of the profile is nearly constant and the ratio $\Delta R_l/\Delta R_p \approx 0.3$–$0.4$ becomes constant. At implantation in masking windows with small dimensions of <1 μm the lateral ion straggling becomes more important and has to be taken into account. To minimize ΔR_l, the edges of the masking layer are often tapered rather than perfect steep, so that ions are gradually prevented from entering the target.

In practice, R_p, ΔR_p, and ΔR_l are tabulated for most common impurities implanted, for example, into Si, Ge, GaAs, SiO_2, Si_3N_4, Al_2O_3, and photoresists

as a function of ion energy and can be found in [2, 3]. Alternatively, $N(x)$, R_p, and ΔR_p can be easily calculated using the well-known SRIM code (http://www.srim.org) developed by Ziegler et al. [4].

The Gaussian approximation for $N(x)$ represents the most simple approximation for the description of the ion range distribution. This approximation to the profile is good for lower energies, but is less correct of higher energies where the profile becomes asymmetric or "skewed." Nevertheless, the Gaussian profile approximation is very useful as a fit to experimental data for the profile near its peak. For example, the peak value N_{max} is mostly within 1 % of the measured value (except for very shallow profiles).

The ion depth distribution $N(x)$ can be characterized in terms of its moments, where the projected range R_p is the normalized first moment and the standard deviation ΔR_p the second moment. Higher moments are the skewness γ describing the asymmetry of the distribution and the kurtosis β indicating how flat the top of the distribution is. A negative skewness means that the distribution is shifted toward the surface, for example due to back scattering of light ions (e.g., B in Si). This case is common for light ions at high energies. At positive skewness the distribution is shifted away from the surface, for example due to ion channeling [see (2.23) and (2.24) in Chap. 2] and which is common for heavy ions at low ion energies. Several different distributions have been employed to give a more accurate fit to the moments of an ion implant distribution than is possible using one Gaussian. The most popular of these are the semi-Gaussian in the case of small asymmetry of profiles ($\gamma < \Delta R_p$), and the Pearson-IV distribution or dual Pearson-IV distribution for amorphous and crystalline targets, respectively [5–10] in the case of large asymmetries of implanted profiles. These semiempirical models are based on both experimental data and physically based models with verified accuracy.

Another approach which simulates ion implantation depth profiles is based on Monte Carlo simulations using the formalism for the binary collision of primary ion–target atom and secondary target–target atom collisions (see Chap. 2). The Monte Carlo approach is used in the development of the physically based models, and these models help to provide the theoretical foundation required in understanding ion implantation, and in technology development and process control. In the case of amorphous targets with only random ion scattering in the target, the SRIM code (http://www.srim.org) and in the case of crystalline targets with possible ion channeling in the crystal, the Crystal-TRIM code [11] are widely used. These two Monte Carlo simulation codes calculate not only the as-implanted ion depth distribution $N(x)$ but provide also the defect concentration and their distribution over depth. The program Crystal-TRIM simulates ion implantation into single-crystalline targets (e.g., Si, Ge, diamond) with up to ten amorphous overlayers of arbitrary composition (with up to three components). The code can be used to calculate as-implanted range and damage distributions as function of depth. Not only atomic ions but also molecular ions (with up to three components) may be considered. Dynamic simulation of ion-induced damage accumulation in single-crystalline substrates (including the formation of amorphous layers) can be carried out.

The applicability of Monte Carlo computer simulations codes based on the binary collision approximation and mentioned before is limited in that they do not account for the modification of the target composition during ion implantation, target removal by sputtering, and target swelling. Thereby, reliable results can only be expected for relatively low implantation fluences of $\Phi \leq 1 \times 10^{16}$ cm^{-2}. At high fluences, a significant reordering of the lattice atoms due to collision sequences may occur. This leads, for example, to a change of the local concentrations in polyatomic or multilayered substances. Furthermore, the implanted ions may, at sufficiently high concentration, play a significant role in the dissipation of collision cascades. Based on the TRIM code the program TRIDYN developed by Möller and Eckstein [12] simulates the dynamic change of thickness and/or composition of multicomponent targets during high fluence ion implantation in amorphous targets. Up to five different atomic species, including those of the ion beam, may be considered. It is possible to use in the beam up to four different ion species with different energies and angles of incidence. The initial target may consist of up to four different species (up to five if some amount of a beam species is already present in the target). Effects such as ion deposition and reflection, sputtering, and ion mixing at interfaces can be computed. The main fields of application of TRIDYN include high fluence ion implantation, ion beam synthesis, sputtering and ion mixing of polyatomic solids, ion beam- or plasma-assisted deposition of thin film, and ion beam- or plasma-assisted etching. An overview about the development of different models for determining of ion implantation profiles and the conditions under which they can be applied to provide useful predictions can be found in [13].

In crystalline targets, for example semiconductor materials (Si, Ge, GaAs, SiC, etc.), the ion range distribution can be significantly influenced by the ion channeling effect as described in Chap. 2. Selected examples of as-implanted depth distributions in dependence on the tilt angle and the rotation degree are shown in Figs. 4.1 and 4.2. As demonstrated in these figures channeling effects are also successfully simulated in a highly accurate manner by using, for example, the dual Pearson model [14] and the Crystal-TRIM code [17] which are shown in Figs. 4.1 and 4.2, respectively.

Due to beam scan angle α_s and/or the wafer misscut and bow angles α_b, the incidence angle of ions relative to the surface normal can vary across the wafer in the order of $\leq 1°$. The resulting channeling variations cause the depth distribution to vary across the wafer. As the extent of local channeling is difficult to control, channeling must be further reduced by additional methods. Channeling does not occur if there is significant implant damage that turns the implanted layer into an amorphous one. Heavy ions such as P^+ and As^+ at large fluences do not show channeling. Light ions and/or low dose implants are prone to channeling. In such instances, channeling can be prevented by:

- Implanting through a thin amorphous layer (e.g., silicon oxide) to randomize the directions of the ions as they enter the crystal lattice
- Using heavy ions, for example BF_2 or heavier molecules rather than boron

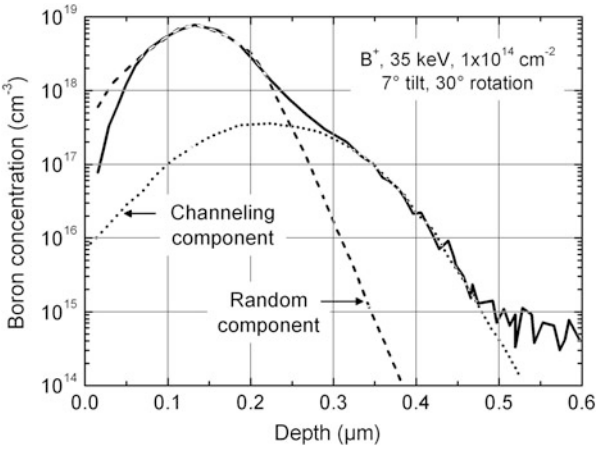

Fig. 4.1 Fit of the one-dimensional dual Pearson distribution (*dotted line*) to the experimental boron profile measured by SIMS (*solid line*) [14]

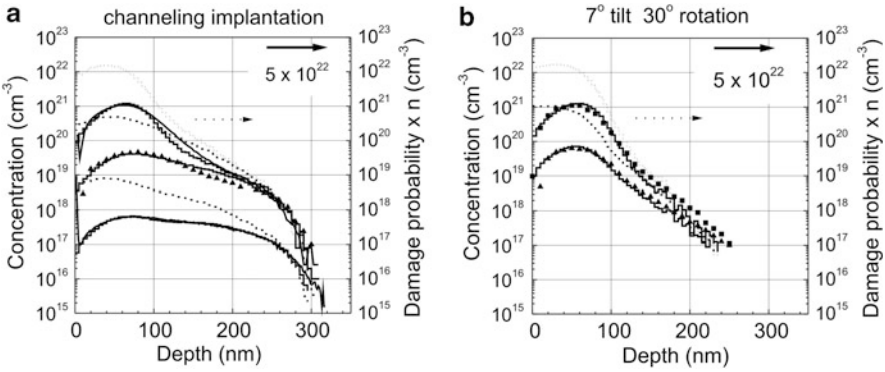

Fig. 4.2 Range and damage distributions for 15 keV B^+ implantations into (100)-Si, in the [15] axial channel direction (**a**), for three different fluences: 1×10^{13} (*bottom curves*), 5×10^{14}, and 8×10^{15} cm^{-2} (*top curves*). The corresponding profiles for tilted implants (**b**) are given for two fluences: 5×10^{14} (*bottom curves*) and 8×10^{15} cm^{-2} (*top curves*). The SIMS data (*continuous lines*, *triangles*, and *squares*) were taken from [16]. The histograms were obtained by Crystal-TRIM simulations [17]. The damage profiles, given by the damage probability multiplied by the atomic density of Si, are shown by *dashed* and *dotted curves*

- Implanting heavy, but electrically inactive species, such as Si or Ge, prior to the actual dopant implantation. The preimplantation turns the wafer surface into an amorphous layer

These and other issues associated with ion channeling are described more in detail in [18].

4.1.2 Implantation-Induced Crystal Damage

Energetic ions traveling through the crystalline target lose their energy in a series of nuclear and electronic collisions and come to rest many atom layers below the surface. Only nuclear collisions with the target atoms result in their displacements referred as damage or disorder. At the collision the ions transfer kinetic energy and momentum to the target atom. The displaced target atom (energetic recoil lattice atom) itself can displace other target atoms resulting in a collision cascade and generation of additional disorder. Along collisional cascades an agglomeration of vacancies and interstitial atoms (Frenkel pairs) and more complex defects (defect clusters) are formed in the crystal lattice. Due to higher nuclear stopping heavy ions transfer more energy to displaced atoms compared to light ions for which electronic stopping dominates. With increasing ion fluence the damaged lattice volumes begin to overlap and finally form a completely amorphous layer without any long-range lattice order. The number of defects and their depth distribution $N_d(x)$ in a target depend on the ion–target mass ratio M_i/M_t, ion energy E, fluence Φ and the fluence rate (or ion flux) J, and the target temperature. As an example the defect evolution in Si at 40 keV P^+ ion irradiation is schematically shown in Fig. 4.3.

Compared to the implanted impurity depth profile the maximum of the damage depth distribution is always shifted to the surface due to the ion energy loss in displacements of lattice atoms $E_d > 0$ [19]. The amorphization fluence Φ_a can be roughly estimated using formula (4.2) if one assumes that all target atoms are displaced:

$$\Phi_a = \frac{2 \cdot E_d \cdot N_t}{(dE/dx)_n}, \tag{4.2}$$

where N_t is the atomic density of the target and $(dE/dx)_n$ the energy loss at nuclear collision per length (depth) unit. In many cases (4.2) underestimate the amorphization fluence because annihilation (annealing) effects during implantation, e.g., outdiffusion of vacancies or collisions with already displaced atoms, are not taken into account. A more correct calculation of the amorphization fluence is given by Morehead and Crowder [20]. Table 4.1 gives calculated and measured amorphization fluences for common ions used for implantation in semiconductors at room temperature.

For some important ions used in silicon technology, the dependence of the amorphization fluence on the silicon target temperature is shown in Fig. 4.4. At the fast rise of the amorphization fluence Φ_a the corresponding temperature T_a means that heating crystalline silicon samples to this temperature amorphization of silicon can be avoided. For example, sample heating to $T_a \approx (400–450)\ ^\circ C$ suppresses amorphization of silicon for all shown ions. Furthermore, Fig. 4.4 demonstrates that for light ions (e.g., boron) amorphization of silicon cannot be achieved at room temperature and at common fluences $<10^{17}\ cm^{-2}$.

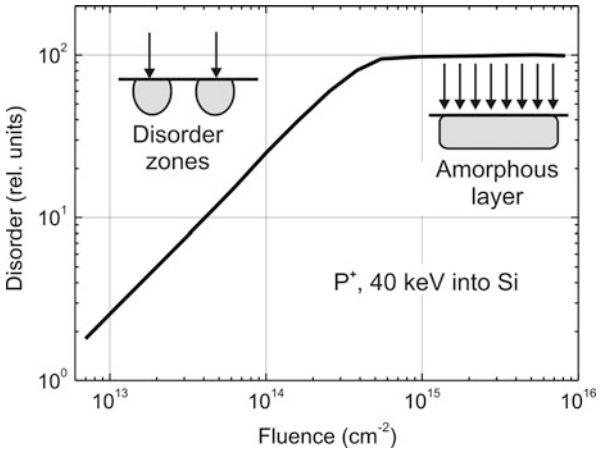

Fig. 4.3 Defect evolution in Si at 40 keV P^+ ion implantation as a function of ion fluence

Table 4.1 Amorphization fluence for common ions in different semiconductors

Semiconductor	Ion	Ion mass of the main isotope	Amorphization fluence Φ_a (cm^{-2})	Reference
Si	B	11	8×10^{16}	[20]
	Al	27	$\geq 5 \times 10^{14}$	[21]
	P	31	6×10^{14}	[20]
	Ga	70	2×10^{14}	[20]
	As	75	2×10^{14}	[20]
	Sb	122	1×10^{14}	[21]
	In	204	1×10^{14}	[21]
	Bi	209	5×10^{13}	[21]
Ge	B	11	2×10^{16}	[20]
	P	31	–	–
	Ga	70	–	–
	As	75	–	–
	In	204	5×10^{13}	[20]
GaAs	C	12	1×10^{15}	[22]
	Si	28	2×10^{14}	[22]
	Zn	64	3×10^{13}	[23]
	Cd	114	3×10^{13}	[23]
GaP	Te	130	1×10^{14}	[24]

For high energy light ions, most of the energy loss is due to electronic collisions which do not produce displacement damage. With increasing penetration depth, light ions lose energy until the cross-over of the electronic and nuclear energy losses $(dE/dx)_e$ and $(dE/dx)_n$, respectively, is reached below which the nuclear stopping becomes dominant (e.g., at $E < 10$ keV for 80 keV B^+). Therefore, most lattice damage occurs in the part of the light ion trajectory beyond this

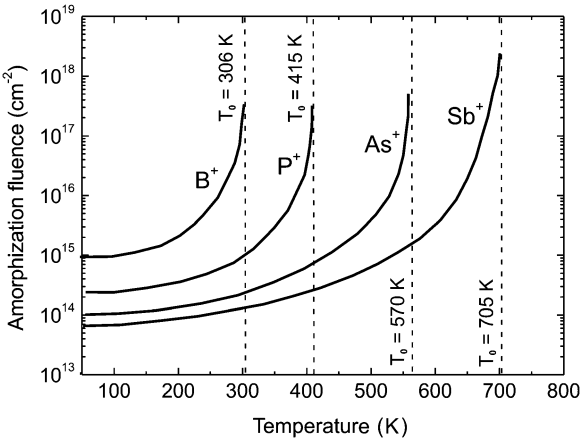

Fig. 4.4 Amorphization fluence as a function of target temperature for common ions used ion implantation into silicon taken from [20]

point. This light ion-induced damage is characterized by a small damage volume density which amounts to ~2 × 10^{20} cm^{-3} and ~0.2 % of Si atoms. Light ions produce only trails of primary Si recoils around the trajectory of the implanted light ion. The low energy recoiled atoms are separated only by small distances from the vacancies they leave. This explains possible dynamic annealing of these defects and therefore no formation of amorphous layers in silicon during room temperature and high fluence B^+ implantation. The light ion-induced damage is thus characterized by primary crystal defects (mostly vacancies and interstitials) which require different annealing procedures compared to crystalline regrowth of implantation-induced amorphous layers. The most important effects of crystal damage and defects induced by ion implantation are summarized in Fig. 4.5.

Comparing experimental data for the amorphization fluence with the number of displaced atoms per ion one can conclude that other effects than only the ion fluence can influence the creation of damage. Besides the target temperature and the ion mass, the defect density around the ion trajectory in the target highly depends on the diffusion of vacancies (V) and interstitial atoms (I). The defect density increases with increasing ion mass because the contribution of the nuclear energy loss to the overall energy loss increases. The mobility of defects becomes higher with increasing target temperature and depends on the remaining crystal order. At low defect density the diffusivity of vacancies and interstitials is higher and thus the probability for their recombination is higher leading to a partial defect annealing during ion implantation. High defect densities prevent the effect of self-annealing and the situation becomes more complicated if interaction between vacancies (formation of di-vacancies, V–V), between vacancies and dopants (e.g., vacancy–boron complex, V–B), and between vacancies and other impurities in silicon (e.g., vacancy–oxygen complex, V–O) with different mobilities takes place.

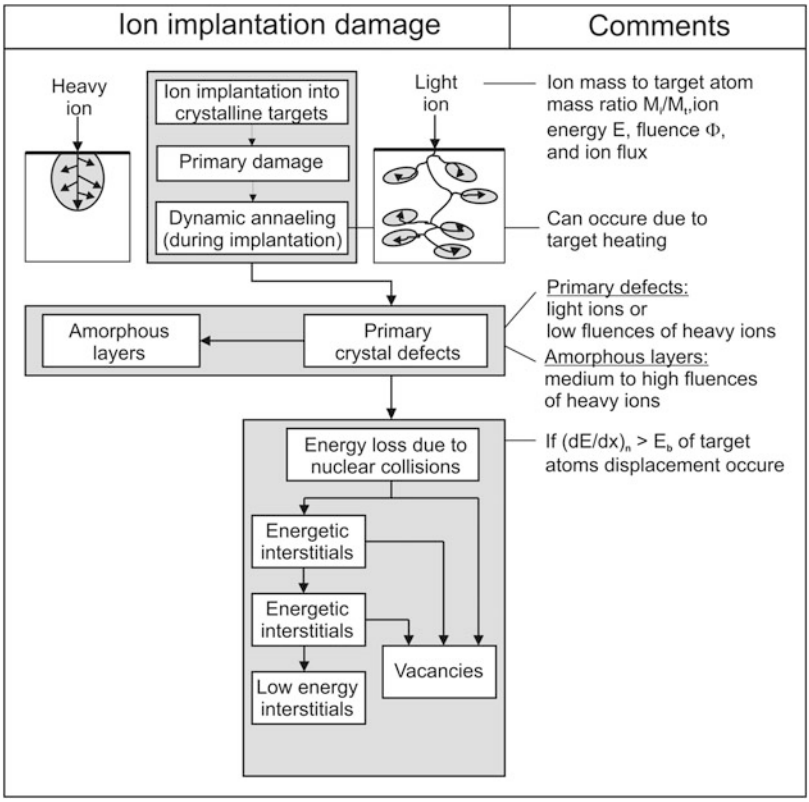

Fig. 4.5 Most important effects of crystal damage and defects induced by ion implantation in crystalline targets

4.1.3 Sputtering Effects and Implanted Profile Change

High fluence ion implantation with $\Phi > 10^{16}$ cm^{-2} leads to effects which usually do not occur in implantations with fluences $<10^{16}$ cm^{-2} performed for conventional implantation doping of semiconductors. The main effects are the dynamical change of the target properties during the implantation process (density, composition, chemical properties, stopping power), diffusion, and surface sputtering. Sputtering (the escape of target atoms, ions, and clusters from the target surface due to physical knock-on process caused by the incident ions) depends on the ion mass and energy as well as the properties of the target material (see Chap. 2). The depth distribution of the implanted atoms for a fluence $\Phi = j{\cdot}t$ (targeted fluence) is then given by Krimmel and Pfleiderer [25]:

$$N(x,\Phi) = \frac{N_t}{2\cdot Y}\cdot\left[\operatorname{erf}\frac{x - R_p + \frac{\Phi\cdot Y}{N_t}}{\sqrt{2}\cdot\Delta R_p} - \operatorname{erf}\frac{x - R_p}{\sqrt{2}\cdot\Delta R_p}\right], \tag{4.3}$$

where Y is the sputtering coefficient and N_t the atomic target density ($N_t = \rho/M_t \cdot m_a$ with ρ the mass density, M_t the target atom mass, and $m_a = 1.66 \times 10^{-24}$ g the atomic mass unit) and with the actual surface being always at $x = 0$. The proportion of re-sputtered implanted ions Φ_s can be approximately calculated by integrating $N(x, \Phi)$ over the range $x \leq 0$ and becomes

$$\Phi_s(\Phi) = \left(\frac{\Phi}{2} - \frac{N_t \cdot R_p}{2 \cdot Y}\right) \cdot \left[\operatorname{erf} \frac{\frac{\Phi \cdot Y}{N_t} - R_p}{\sqrt{2} \cdot \Delta R_p} + 1\right] + \frac{\Delta R_p \cdot N_t}{\sqrt{2\pi}} \cdot \exp \frac{-\left(\frac{\Phi \cdot Y}{N_t} - R_p\right)^2}{2 \cdot \Delta R_p}. \tag{4.4}$$

The difference $\Phi_r = \Phi - \Phi_s$ is that fraction of the implanted ions which is actually deposited in the target (the retained fluence). For high fluence implantation at low ion energies, a saturation of surface concentration is reached which corresponds in the equations above to the case of assuming that Φ is infinite. Then, it follows from (4.4) that the maximum density of implanted atoms at the surface is $\sim N_\infty = N(0, \infty) = N_t'/Y$. For the new target density N_t' it can approximately be assumed that $N_t' = N_t + N_\infty$. Therefore, at the surface the implanted impurity density is $N_\infty = N_t/(Y - 1)$. Furthermore, from (4.4) a saturation fluence of

$$\Phi_\infty = \Phi_r(\infty) = \frac{N_t \cdot R_p}{Y - 1} \tag{4.5}$$

can be found.

As an example, Fig. 4.6 shows Co^+ implantation profiles in silicon calculated from (4.3) for different implantation fluences. For the highest fluence of 1×10^{17} cm^{-2} the distribution corresponds to the saturation case with maximum concentration at the surface. The calculation does not include the effect of cobalt-atom diffusion during implantation.

Calculating retained fluence Φ_r according to (4.4) for 35 keV Co^+ implantation in Si at a sputtering yield of $Y = 3$ and a fluence of 1×10^{17} cm^{-2} we get that the retained to targeted fluence ratio Φ_r/Φ is only in the range of ~50 % if the saturation stage is reached. At saturation the maximum implanted impurity concentration is located always at the target surface and depends on the sputtering coefficient Y which is given at normal incidence by the Sigmund formula [27, 28]. In this formula, target swelling, blistering, and re-deposition of sputtered target material are neglected. With increasing ion mass the sputter yield increases with a maximum of the ion energy dependence usually between 10 and 500 keV depending on the M_t/M_i ratio. Sputter coefficients are extensively investigated for metals irradiated with noble ions (He, Ne, Ar, Kr, Xe) and other ions and can be found for example in [27, 29]. As shown in Fig. 4.7, for Si, sputter coefficients for common ions (B, P, Ga, As, Sb, and Bi) have been measured and calculated by different authors and are published in [27, 30, 31]. Sputtering yields at noble ion

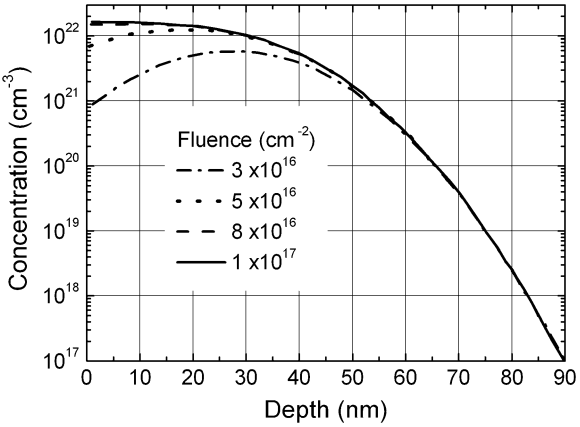

Fig. 4.6 Calculated cobalt concentration profiles for various implantation fluences of 35 keV Co^+ ions in silicon at normal incidence ($R_p = 33$ nm; $\Delta R_p = 12.8$ nm; $Y = 3$) [26]

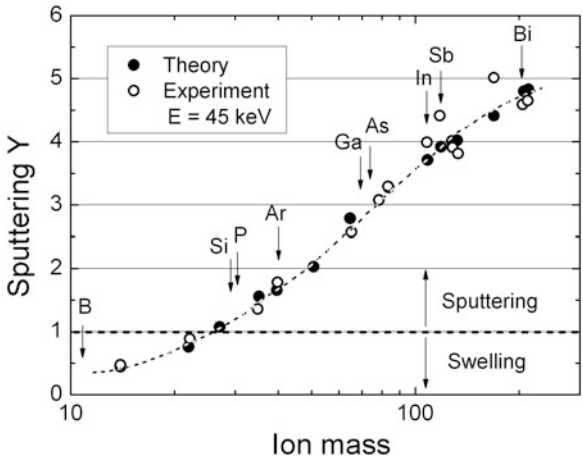

Fig. 4.7 Sputtering yield of 45 keV ions for silicon as a function of ion mass at normal incidence; *open cycles* of experimental data are taken from [30] and *full cycles* of theoretical values are taken from [27]

irradiation of III–V- (GaAs, InP, GaSb, InSb, GaN) and II–VI- (CdS, CdSe, CdTe, HgTe, ZnTe, PbTe) semiconductors also have been intensively investigated and are published in [32, 33].

Applying the TRYDYN simulation code to high fluence ion implantation the change of the profile due to surface layer removal by sputtering can be very well predicted, as shown in Fig. 4.8 for 60 keV Co^+ implantation into silicon at normal incidence. The example in Fig. 4.8 demonstrates that at the surface the maximal atomic fraction of Co in Si introduced by ion implantation is limited to 33 %. The black bars at the beginning of each profile indicate the location of the actual surface for each implanted fluence, or, in other words, the thickness of the sputter-removed

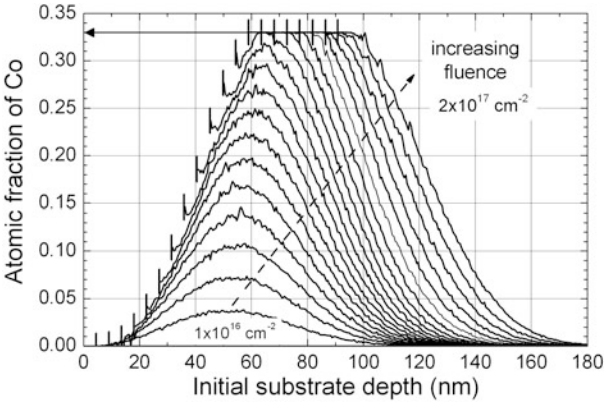

Fig. 4.8 Change and shift of the Co concentration depth profile in dependence on implanted fluence in the range (1–20) $\times$ 10^{16} cm^{-2} for 60 keV Co^+ implantation into silicon. The fluence increment between the profiles is 1 $\times$ 10^{16} cm^{-2} (Röntzsch L private communication)

Si layer which amounts, for example, 90 nm at an implanted Co^+ fluence of 2×10^{17} cm^{-2}.

Because high fluence ion implantation produces drastic changes in the target (target density, target composition, phase changes crystalline to amorphous) at low sputtering yields for light ions (ion mass M_i comparable or smaller than target atom mass M_t), swelling of the target can appear. For sputtering investigations, this effect can be neglected in most cases at very high fluences but at moderately high fluences the swelling effect has to be taken into account. In the case of Si^+ implantation into silicon, the sputter coefficient is around or ≤ 1 depending on ion energy as shown in Fig. 4.9.

The mechanisms and effects of ion implantation-induced damage and ion sputtering in compound semiconductors strongly depend on the semiconductor group. The III–V semiconductors are usually easily amorphized at relatively low fluences (on the order of 10^{14} cm^{-2}), but there is also evidence of some re-crystallization taking place at higher fluences. The implantation damage behavior of the II–VI and HgCdTe semiconductors is very similar to that of metals. Several mechanisms can cause bombardment-induced compositional changes in multicomponent materials. For example, in the case of Ar^+ bombardment of InP, the experimental results indicate that the cause of surface compositional changes is mainly preferential sputtering, while for argon bombardment of GaAs, bombardment-induced diffusion and segregation effects are the dominant mechanisms. In general, particular compositional change mechanisms can appear in most mentioned compound semiconductor systems and also in SiC [34, 35]. Especially, for SiC and diamond-like carbon (DLC), for example ta-C layers, in the nonsteady state case, the drastic change of the target density due to amorphization and therefore to swelling must be taken into consideration [36].

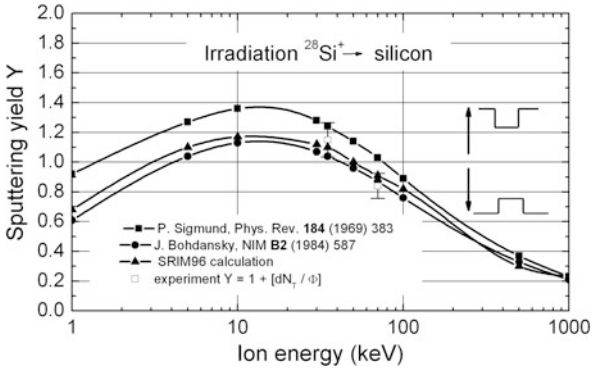

Fig. 4.9 Sputtering yield for Si^{+} ion irradiation of crystalline silicon showing the ion energy dependence of both sputtering and swelling (Bischoff L private communication)

Processes leading to surface sputtering may also inject one species into another through interfaces in a sandwiched target, and therefore lead to transmission sputtering or interface mixing. In general, such processes may give rise to changes in the depth profile of the composition of a multicomponent target.

As described in Chap. 2 one may distinguish between recoil implantation and cascade mixing. The former effect is due to direct ion–target collisions and therefore strongly directional, while the latter process is due to target–target collisions and therefore more or less isotropic. Moreover, recoil implantation involves few atoms with moderate and high energies while cascade mixing strongly peaks toward low recoil energy. Recoil implantation causes a net displacement of the depth profile of the light species relative to that of the heaviest species in the direction of the beam, whereas cascade mixing is roughly equivalent with an interdiffusion, with a diffusion coefficient essentially independent of target temperature [37, 38]. The effect of recoil implantation was intensively investigated for implantation into and through masking layers, for example SiO_2 and Si_3N_4, on silicon, as often used in microelectronic technology [39–42] and applied to direct shallow doping of different substrates using specific surface layers [43, 44].

In general, recoil ion implantation or recoil ion mixing is based on atom relocation by single-collision events. The energy E_R transferred to the recoiled target atom M_2 by the incident ion M_1 with an energy E_0 during single collision at the interface between the substrate S and the layer L is equal to

$$E_R = E_0 \cdot \frac{4 \cdot M_1 \cdot M_2}{(M_1 + M_2)^2} \cdot \cos^2\vartheta, \tag{4.6}$$

where ϑ is the scattering angle. The maximum transferred energy E_{Rmax} is achieved at $M_1 = M_2$ and at $\theta = 0$ (head-on collision) but the most probable collisions are at large angles (soft collisions) with decreasing transferred energy E_R.

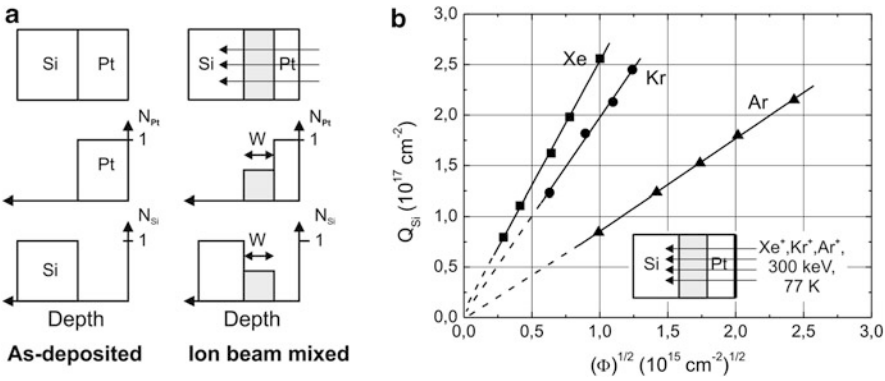

Fig. 4.10 (**a**) Schematic drawing of recoil ion beam interface mixing and (**b**) example of ion mass and fluence effects in an ion mixed Pt/Si layer. The amount Q_{Si} is the amount of silicon in the mixed layer w. The ion mixing rate is proportional to $(\Phi)^{1/2}$ (from [45] and [46])

If w is assumed as the thickness of mixed layer between S and L the amount of mixing Q is equal to the number of S and L atoms in the layer w (Fig. 4.10a). Q increases with ion mass M_1 because $(dE/dx)_n$ scales with ion mass and is proportional to the square root of the fluence Φ or the irradiation time t at constant ion flux (Fig. 4.10b).

Several processes are responsible for the ion mixing effect, all of which are initiated by the interaction of an energetic ion with a solid. Both ballistic and cascade effects depend on the mass of the incident ion. By increasing the mass of the ion the amount of energy deposited in nuclear collisions per unit length traveled by the ion also increases. The influence of mass and fluence effects on ion mixing is clearly evident as shown in Fig. 4.10. The average thickness of reaction at the Pt/Si interface is given in units of Si atoms cm^{-2}, which increases with both increasing mass of the incident ion and the increasing fluence Φ. At the Pt/Si interface the mixing rate for all ion irradiations is proportional to $(\Phi)^{1/2}$. Ion beam mixing gives the ability to produce ion-modified materials with higher solute impurity concentrations at lower irradiation fluences than can be achieved with conventional high fluence ion implantation, for example of an Au/Cu interface [47].

The isotropic broadening observed in thin buried marker layers strongly suggests that a series of single-event, forward-momentum recoils is not the dominant mixing mechanism. Instead, in many cases the symmetric marker broadening appears to be more related to processes dominated by the isotropic displacement mechanism caused by collisional cascades [48].

For the simulation of ion implantation into multilayer systems including recoil implantation and ion mixing at interfaces, the dynamic binary collision code TRIDYN is favored to be used. Because TRIDYN considers both of ballistic interactions of an energetic ion with target atoms (direct ion–target collisions and target–target collisions) as well as dynamic change of depth-dependent composition changes in stacked layers, ion mixing at layer interfaces can be simulated very well. An example of $Si/SiO_2/Si$ stack mixing by Si^+ ion irradiation with the aim of Si nanocrystal formation in thin gate oxides can be found in Sect. 4.3.3.

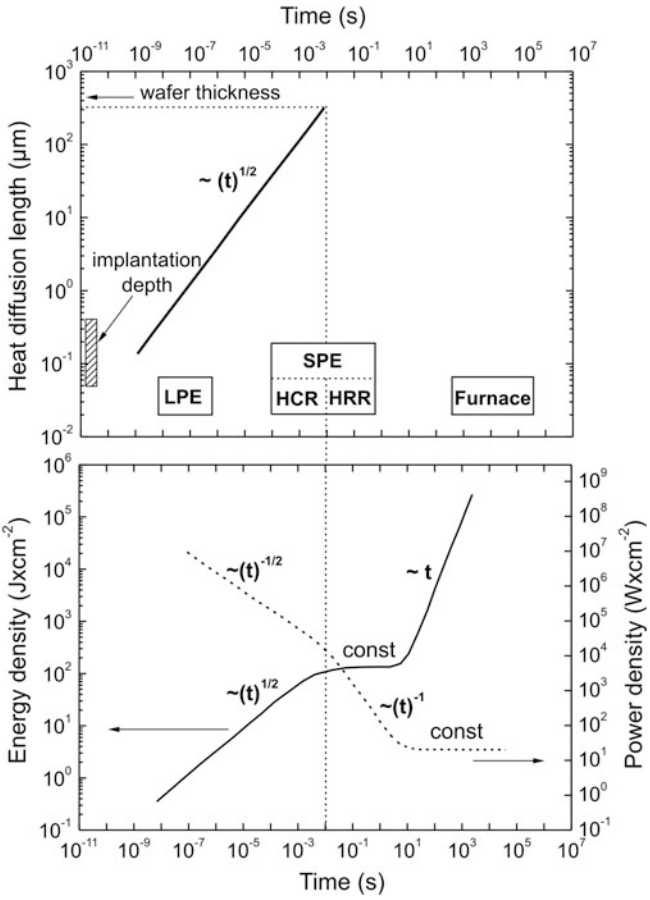

Fig. 4.11 Schematic classification of different regimes for radiation damage annealing in dependence on time of energy transfer to the sample (wafer) during heating [49]. The *upper part* shows the heat diffusion length during energy transfer and the *lower part* the energy density necessary for annealing at different regimes of liquid phase epitaxy (LPE), solid phase epitaxy (SPE), heat conduction regime (HCR), and heat radiation regime (HRR)

4.1.4 Radiation Damage Annealing

The major problem associated with ion implantation in semiconductors (Si, Ge, GaAs, SiC, etc.) is the removal of damage in the substrate lattice which has negative influence on materials and device properties. This is conventionally achieved by furnace annealing at temperatures up to about 1,000 °C. In semiconductors one has to distinguish between defect annealing, re-crystallization of amorphous layers, and electrical activation of implanted dopants by placing them on crystal lattice sites. In Fig. 4.11 characteristic properties of different annealing regimes are summarized as a function of the heating time. In this scheme all methods using heating times less

than 1 s are called nonconventional annealing techniques in which short pulses or writing beams are used to transfer the energy of light into the lattice of the semiconductor.

The two principal annealing regimes are the annealing (recrystallization) in the liquid phase (liquid phase epitaxy) and the annealing in the solid phase (solid phase epitaxy). Extremely short pulses of ≤ 1 μs heat the amorphized layer not long enough to allow a complete recrystallization by solid phase epitaxial regrowth (SPE). Full recrystallization can only be achieved by melting of the damaged layer followed by a liquid-phase epitaxial regrowth process (LPE). In these short pulse times, the diffusion length of the heat is in the same order of magnitude as the implantation depth. That means, only the damaged surface region is thermally affected by the annealing process. At liquid phase epitaxial regrowth the implanted layer melts and recrystallizes with high crystal perfection from the undamaged volume to the surface on a time scale $<10^{-7}$ s and at energy densities of ~1 J cm^{-2}. For this regime, pulsed and scanned lasers are applied. Because impurity diffusion coefficients in liquids are several orders of magnitude higher than in the solid phase, a significant redistribution of the implanted species occurs due to diffusion and segregation [50].

For heating times of 10^{-4} to 1 s the rapid thermal annealing (RTA) process has been shown to take place analogous to the conventional thermal (furnace) annealing by solid phase epitaxial regrowth. As the activation energy for impurity diffusion is higher than that for epitaxial regrowth, the redistribution of the implanted profile is negligible in times required to recrystallize an amorphous layer. During furnace annealing (FA) a noticeable redistribution of impurity atoms can be observed, only due to the fact, that contrary to the nonconventional methods, the necessary annealing time is strongly exceeded. Therefore, the nucleation of small defects (e.g., point defects) to extended defects (e.g., dislocation loops) and their growth observed at thermal furnace annealing can also be altered by nonconventional annealing techniques.

It is appropriate to subdivide the SPE regime into two different time–temperature regimes—the heat conduction regime (HCR) and the heat radiation regime (HRR). At HCR during short pulses (≤ 1 ms, e.g., for silicon wafers with a thickness of >300 μm) there is a strong temperature difference between the illuminated side and the other side of the wafer. This is a consequence of the finite heat diffusion through the wafer during the pulse duration. After the pulse the surface temperature is rapidly lowered due to temperature equalization over the wafer thickness by heat conduction. Before this rapid cooling has taken place the annealing process must be completed. In the HRR during longer pulses (≥ 10 ms), the diffusion length of the heat exceeds the wafer thickness and the heating of the whole sample material is nearly uniform. Provided that the sample is thermally isolated the heat is stored for a long time (typically ~1 s) because the cooling is dominated by heat radiation to the surrounding medium. Because the heating times of both regimes (HCR and HRR) differ by three orders of magnitude, differences in the annealing behavior of the implanted samples can appear.

Within the end of the 1970s years it has been demonstrated that both scanned cw lasers and scanned electron beams [51] offer powerful tools in the solid phase annealing. Nevertheless, only after 20 years especially laser annealing received renewed interest, e.g., for dopant activation, by either melt quenching a surface layer or as a high-temperature submelting pretreatment prior to a standard RTA [52–55].

One of the approaches of rapid thermal processing to the elimination of implantation damage is flash-lamp annealing (FLA) in the time scale of ms [56–58]. It is likely that RTA and FLA steps today play the most important role in Si device fabrication, possibly with more stringent control over time and temperature, as has been the experience with advances in planar CMOS technology [59]. For a number of excellent reviews of RTA methods, the reader is referred to some references [60–63]. Dopant activation by rapid thermal processing requires exquisite control of wafer temperature because diffusion and electrical activation of the dopants are governed by high thermal activation energies, typically in the range 3–5 eV. Controlling diffusion with a tolerance of ± 1 %, as may be required by the silicon IC technology, corresponds to controlling the temperature of 1,000 °C to better than ± 1 K. Thus, temperature control for critical annealing steps would have to be better than ± 1 K across 300 mm wafers. The performance of current advanced RTA equipment is in the range $\pm(2–3)$ K. The RTA techniques can be divided into two categories: (1) rapid wafer transfer between a steady heat source and a heat sink, and (2) a fixed wafer heated by rapid modulation of the heat source. Heat is exchanged for the most part normal to the wafer surface by radiation, gas convection, and gas thermal conduction. The wafer temperature is usually determined by infrared-based optical pyrometers that incorporate systems for measuring wafer radiance and emissivity. Pyrometry is the favored method because it is noncontacting and, owing to Planck's radiation law, the errors in temperature are relatively less than the errors of change of sample radiance and emissivity due to different surface properties (e.g., different patterned of SiO_2, Si_3N_4, poly-Si, thin metal layers, etc.).

In the *LPE annealing regime* energy irradiation sources of high-power pulsed lasers, for example Nd-glass, Nd-YAG, and Yb-YAG lasers, with wavelength in the visible and near-infrared region (1,064–355 nm) as well as XeCl- and KrF-excimer in ultraviolet region (308–248 nm) with energy densities of ≥ 1 J cm^{-2} and pulse duration times of 10^{-7}–10^{-8} s are required. For melting of near-surface layers, there exists a light pulse energy barrier E_L which depends on the light absorption coefficient α, the light wavelength λ, and on the sample temperature. With increasing sample temperature the absorption coefficient increases for most of semiconductor materials. With increasing light pulse length t_p the energy barrier increases with $E_L \sim (t)^{-0.5}$, because the diffusion time of the generated heat from the surface layer into the substrate is also reduced, and at the same time the maximum melting depth d_{max} decreases corresponding to the relation $d_{max} \sim (t)^{0.5}$. For epitaxial regrowth of amorphous layers, the depth of the melted layer must be larger than the thickness of amorphous layer. In this case the formation of defects such as stacking faults, dislocations, and precipitates can be eliminated to high degree

during LPE. The significant redistribution of the implanted dopant profile during LPE is caused by the very high diffusion coefficient in the melt which is orders of magnitude higher compared to that in the solid material. The redistribution of the profile depends on the melt duration t_m, the melt depth d_m, and segregation coefficient k_0, which represents the ratio between the equilibrium dopant solubility in the growing crystalline solid material and that in the liquid near the interface. For silicon the values are <1 [64], which means that during regrowth of the melted layer the dopants are rejected into the melt which becomes progressively enriched with dopants.

In the case of high segregation coefficients (e.g., B, P, As), the redistribution of impurities is mainly driven by their diffusion in the melt, whereas for small coefficients $k_0 < 10^{-2}$ the redistribution is mainly caused by the segregation at the liquid–solid interface. A high amount of impurities is pushed in direction of the surface where eutectic precipitates can be formed. During the high cooling rates during LPE point defects remain in the re-crystallized layer which can be partially removed at subsequent conventional low-temperature annealing, for example in a hydrogen atmosphere. Furthermore, during LPE the thermal solubility limit of dopants in the melt is much higher compared to their solubility in the solid state of silicon which leads to complete electrical activation of introduced high fluence-implanted impurities even above the equilibrium solid state solubility limit [50, 65, 66].

In the *HCR annealing regime with SPE* scanned continuous wave (cw) lasers or pulsed lasers with wavelength in the visible and near-ultraviolet range (~400–800 nm) with irradiation times in the order of 0.5 ms $< t <$ 20 ms are applied to damage annealing [51]. On this time scale of energy supply for damage annealing, higher energy densities up to 100 J cm^{-2} are necessary due to heat loss by heat conduction into the substrate (and the ambient). The laser beam spots have usually diameters of 10–100 µm and must be scanned over the sample surface with appropriate scan velocity or repetition and dwell time. In this regime, no significant redistribution of the implanted profiles and segregation effects at the surface are observed if the concentration of implanted impurities in the substrate is in the order of their solubility at given annealing temperature. For re-crystallization at sufficient energy in the laser beam spot very low concentrations of remaining point defects, especially in <100>-oriented silicon substrates, and a high degree of electrical activation up to 100 % can be achieved.

Among thermal pulsed-laser annealing *flash-lamp annealing (FLA)* [67] can be applied for greater suppression of dopant diffusion effects. FLA uses a high optical flux for faster heating to either melt the surface of the wafer or selectively raise the surface temperature. Upon termination of the light pulse, the surface temperature rapidly cools by thermal diffusion from the near-surface region into the bulk of the sample. The rapid quenching can lead to lattice defects and dopant metastability, and consequently to dopant redistribution during subsequent thermal processing steps. FLA has also been implemented in a lamp-based RTA system as a modification of the chamber shown in Fig. 4.12a, where the upper bank of lamps was replaced by Xe flash-lamps, emitting in the 300–800 nm wavelength range and to produce a 0.5–20 ms pulse at the peak temperature [68].

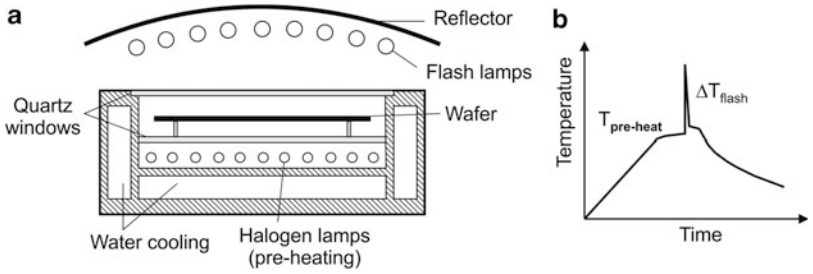

Fig. 4.12 Schematic buildup of a FLA annealing chamber (**a**) and typical $T(t)$ characteristics (**b**)

The heating and cooling rates are very high and in the order of 10^6 K s^{-1}, which can easily lead to sample breakage due to high introduced mechanical stress. The lower bank of incandescent lamps is used to heat the wafer up to about 600 °C. The upper bank of lamps is energized by an electric discharge to produce a short pulse of radiation with an energy density up to 100 J cm^{-2}. Figure 4.12b schematically illustrates the surface temperature versus time profile for FLA. As has been shown, the results indicate a high electrical activation of dopants with negligible diffusion in the region of the junction in the case of BF_2 implantation and several nanometer diffusion in the case of As implantation into silicon [69].

In principle for *SPE in the HRR regime* the same energy sources as in the HCR regime can be applied, but in recent years large area light radiation heaters (mostly arrays of incandescent lamps systems and of high-power arc lamps) became accepted because of higher productivity during annealing of large wafers up to 300 mm diameter. The sample exposure time in this regime is higher than 100 ms. Due to the continuous heating over the sample thickness, the irradiation time can be varied over a broad range without significant change of damage annealing behavior. Shorter times are preferred if diffusion effects (profile broadening) have to be minimized. The annealing conditions do not change if the sample (wafer) is irradiated from the nonimplanted back side. At these conditions possible influence of patterned surface layers on the front side on energy absorption can be excluded. After annealing in the HRR regime residual defects of rod-like dislocation with some tens of nanometer extension, no significant redistribution and phase separated precipitates of impurities have been observed.

Several steady light heat source methods have been developed mainly for purposes of common rapid thermal annealing (RTA) of implantation damage annealing in silicon and other semiconductors. The *cold-wall RTA method* that uses incandescent lamps for heating, wafer rotation for uniformity, and gas levitation for thermal isolation and quench cooling was developed to replace prolonged furnace annealing. Incandescent lamp systems are now most prevalent in IC manufacturing. Figure 4.13a illustrates the process chamber of a modern lamp-based system with wafer heating from the top side and wafer temperature measurement from the bottom side [70]. The heating lamps are arranged in a closed-packed two-dimensional array and are powered in concentric annular zones. The power distribution among the zones is controlled by temperature sensors along the radial direction underneath the wafer.

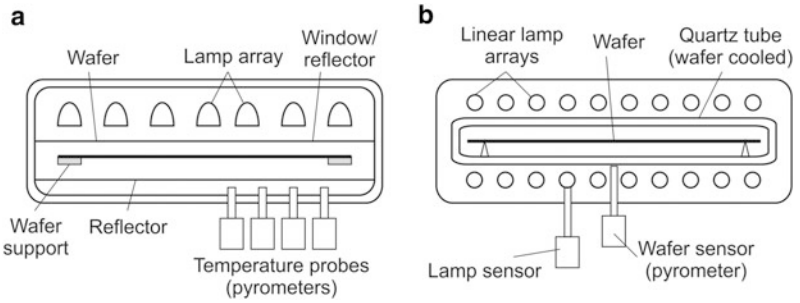

Fig. 4.13 Typical buildups of a cold-wall RTA system: (**a**) asymmetric lamps, single-sided heating, and (**b**) linear lamps, double-sided heated

Another RTA system, illustrated in Fig. 4.13b, has a chamber that efficiently surrounds the wafer with heating lamps [71–73]. The reflective enclosure contains linear lamps arranged in rows with the filaments parallel to the wafer and includes a quartz isolation tube to control the gas ambient. The linear lamps in the upper and lower banks may be mutually parallel or perpendicular. The power distribution among the lamps is adjusted to produce uniform temperature distribution over the wafer. Two radiation probes are used to determine the wafer temperature by a technique denoted as ripple pyrometry [74]. The probe with the view of the wafer collects a mixture of radiation emitted by the wafer and the lamps. The other probe (ripple pyrometer system) samples radiation from the lamps for reference.

High-power arc lamps have been used for RTP, particularly for *spike annealing*. Spike annealing techniques were introduced to control dopant diffusion in shallow junction formation [75]. Current spike annealing methods use infrared heating that is characterized by near thermal equilibrium across the wafer thickness of the wafer, similar to RTA. The variables are heating rates, which depend on the intensity and wavelength of the infrared radiation source, the switching time from heating to cooling, and the cooling rate, which involves radiative, convective, and thermal conductive dissipation of wafer heat. Typical temperature versus time traces for spike anneals with arc and incandescent lamps are shown in Fig. 4.14.

Both curves were produced by abruptly turning off lamp power at or near the peak temperature. Typical heating rates are in the range 100–400 K s^{-1}. The wafers cool by chamber absorption of the emitted radiation at rates up to 150 K/s. Sharper spike peaks are achieved for an arc lamp compared to incandescent lamps, because arc lamp method produces the sharper spike with an inherent response time of ~10 μs. The incandescent lamp method produces a spike with a more rounded peak because of incandescence after-glow in tungsten filaments, which has a time constant of about 0.5 s. In spike annealing wafers are cooled by turning off the heating lamps or by withdrawing the wafer from the heated environment. Initial cooling at high temperature is dominated by radiative heat transfer. Cooling can be augmented by thermal conduction and gas convection at lower temperatures, e.g., by using He gas as the exchange medium.

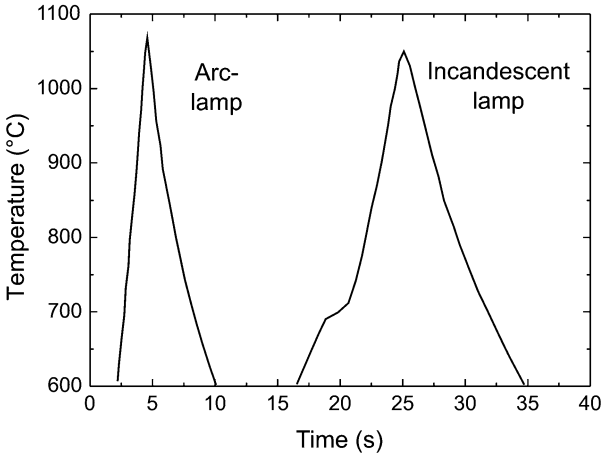

Fig. 4.14 Typical temperature versus time traces for spike anneals with arc and incandescent lamps

In some cases rapid thermal processing is carried out by briefly inserting the sample into a quartz tube furnace. The modern technique is oriented on so-called *hot-wall RTA* in a vertical quartz tube furnace (bell jar furnace) and utilizes the uniformity and reproducibility inherent in a steady furnace-based heat source (Fig. 4.15) [76]. The wafer is transported by fast elevation in a bell jar furnace heated with a vertical temperature gradient. The temperature at the top of the bell jar is several hundreds K higher than the maximum targeted wafer temperature. The desired heating rate and maximum wafer temperature determine the peak furnace temperature. The bottom of the chamber is water cooled and serves as a heat sink for cooling the wafer when it is moved down. The temperature is measured by a pyrometer that detects the wafer radiance and subtracts background interference from the furnace radiation. The pyrometry uses 0.95 μm wavelength, where optical transmission through Si is negligible.

A comprehensive review of the detailed operation of RTA systems with respect to the dynamic response of the sample (wafer) temperature to light irradiation can be found in [77].

During *furnace annealing* on the time scale of >10 min, the implanted and damaged sample is at thermal equilibrium with the surrounding inert gas ambient in a heated high-purity quartz or poly-Si tube. The recrystallization of amorphous Si layers (activation energy 2.3 eV) in most cases takes place in the temperature range of 600–800 °C and the annealing of different kinds of crystal defect as well the electrical activation of dopants in a higher temperature of 800–1,000 °C. If the implantation conditions are not sufficient to create an amorphous layer, lattice repair occurs by the generation and diffusion of point defects in the crystal. This process has an activation energy of about 5 eV and requires therefore higher annealing temperatures to remove all the defects. It is thus easier in many cases

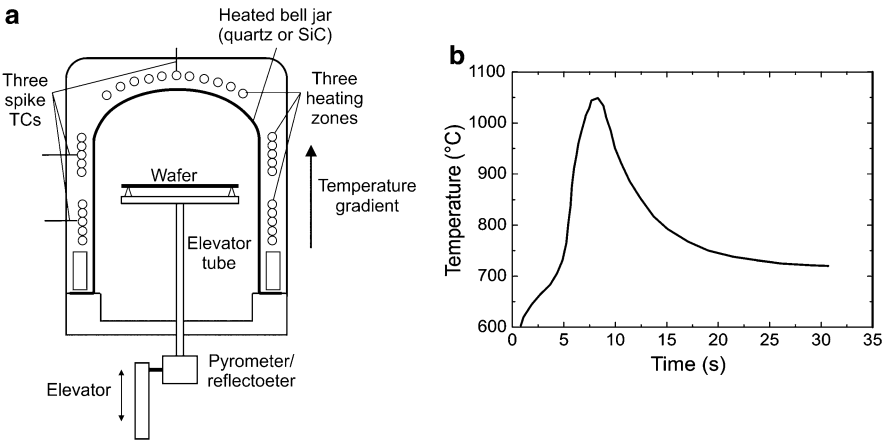

Fig. 4.15 Hot-wall RTA using a vertical quartz (or SiC) tube furnace (bell jar furnace) (**a**) and typical temperature–time trace (**b**)

to repair a fully amorphized layer than a partially damaged one. The result of incomplete annealing is a reduction in the fraction of active dopants which in principle has to be as high as possible. This means that in the furnace regime the recrystallization of amorphous layers in silicon takes place during heating up the furnace to the desired annealing temperature at 800–1,000 °C. The annealing process depends on time–temperature characteristics of heating-up rate, constant temperature annealing time and cooling-down rate because the furnace annealing regime is a thermodynamic equilibrium process. The thickness of the recrystallized layer is given by the expression:

$$d_{\mathrm{R}} = a \cdot v_0 \cdot t \cdot \exp - \frac{E_{\mathrm{a}}}{k \cdot T}, \tag{4.7}$$

where v_0 is the phonon frequency (e.g., in the Si lattice 10^{11}–10^{12} s^{-1}), a is the crystal lattice constant (e.g., for Si 0.543 nm), and E_{a} the activation energy for atom movement (e.g., for Si 2.3 eV).

The phonon frequency v_0 depends on the crystal orientation and the concentration of introduced impurities. The recrystallization velocity of an amorphous Si layer between 1 and 50 nm min^{-1} increases with increasing doping concentrations and in order of B, P, As, Ga, In and of orientations <111>, <110>, <100> as shown in Fig. 4.16. In the nonabrupt transition depth between the amorphous layer and the crystalline substrate, the damage concentration continuously decreases leading to an increased concentration of point defects and dislocations. Therefore, during long-time furnace annealing these defects, depending on annealing conditions, can extend into the crystalline substrate as well into the recrystallized layer.

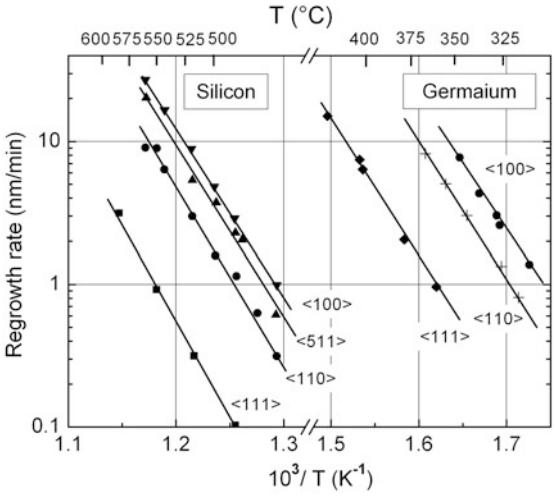

Fig. 4.16 Recrystallization velocity in Si and Ge for different crystal orientations (from [78])

Due to the complexity of processes for defect dissolution, defect generation, recrystallization, electrical dopants activation in crystalline materials, and the placement of annealing processes in the full device fabrication process, many optimized thermal annealing regimes have been developed. Especially multistep annealing at different temperatures and times with different heating and cooling rates are of great importance because low residual defect concentration and high electrical activation can be achieved [79]. The disadvantage of furnace annealing is the redistribution of dopants (lateral and vertical broadening of the as-implanted profile) by defect-enhanced diffusion which is observed already at lower temperatures and thermal diffusion at high temperatures. The emission of vacancies during annealing increases the diffusion coefficient of the implanted atoms. The time constant of vacancy emission is in the order of minutes. In general, implantation induced release of vacancies (V), and, especially, in the case of boron in Si the release of interstitials (I) can increase the diffusion coefficient significantly. The increase of the boron diffusion coefficient denoted as transient enhanced diffusion (TED) is explained by the formation of (I–B) complexes with a high diffusivity in silicon [80–85]. A defect-enhanced diffusion has been also observed for stable dislocation defects often induced by high fluence implantation.

In advanced silicon manufacturing technology, more ion implant annealing is done by RTA in single wafer process tools than in batch furnaces. This is especially true for shallow junction implant annealing, where RTA is believed to be a better method. Depending on the implanted dopants, the ion energy, and fluence, the annealing can require temperatures up to 1,100 °C [86]. The advantage of RTA is to access these high temperatures while minimizing the thermal budget by reducing the annealing time at a given temperature. A very short annealing time at higher temperatures, spike-anneal with a very fast ramp up/down rate has been introduced

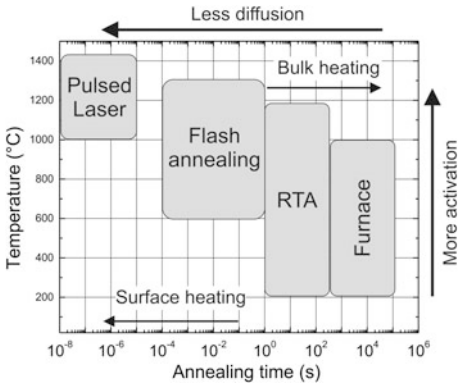

Fig. 4.17 Temperature–time map of various thermal annealing techniques used in the semiconductor industry

as an effective shallow junction implant annealing to electrically activate implant species with no significant diffusion. The annealing time is typically shorter than 1 s. For ultra-shallow junction (USJ) formation with $x_j < 50$ nm, excimer laser-based SLA and nonfilament-based FLA techniques using arc lamps are being actively investigated [68, 87, 88]. For further reduction of the diffusion of implanted species during annealing, SPE of implanted silicon at lower temperatures (600–700 °C) using RTA has been investigated [89].

The temperature–time characteristics of common thermal annealing techniques introduced in silicon processing for VLSI circuits are summarized in Fig. 4.17.

Usually, all the active device regions are located at the near-surface region within a depth of <1 μm on Si substrates (wafers) with a thickness of 400–800 μm. From the viewpoint of minimizing dopant diffusion and defect generation during annealing, selective surface heating without significant heating of the bulk Si wafer is an ideal thermal treatment. The two modes of LPE (surface melting) and SPE (submelt modes) of SLA have been investigated for USJ fabrication [90]. The LPE mode of SLA annealing gives a high electrical activation, but has process integration problems. The SPE mode of SLA annealing reduces the problems of process integration and gives reasonable electrical activation of implanted dopants. For both SLA modes, the annealing area is limited by the size of the laser beam and requires significant pulses repetition, as well as scanning systems for dopant activation over the full wafer surface. In the future, the semiconductor industry will target USJ junction depths below 20 nm. High quality pn-junctions with $x_j < 10$ nm will require annealing techniques without broadening of the implanted profiles or less than <3 nm due to diffusion. There are numerous annealing options which depend on the gate stack structure and on process integration including: (1) high-temperature ms-FLA or SLA, (2) spike-RTA with lower spike annealing temperatures of <900 °C, (3) SPE at higher annealing temperatures of >700 °C, and (4) combinations of spike + ms annealing or ms + spike annealing [91].

4.2 Ion Implantation into Semiconductors

Ion implantation is one of the most important processing steps in semiconductor technology. During the progress of ion implantation technology over the past 30 years, remarkable progress has been made in understanding the particle-solid collision phenomena so that range profiles of implanted dopants in semiconductors can be calculated with considerable accuracy. The annealing conditions to remove the implantation-induced crystal damage in semiconductors and to leave the implanted dopants on lattice sites, and fully electrically active, have also been well explored. The engineering challenges are related to the development of low and high energy implantation processes to accommodate the many implantation steps used in the fabrication of integrated semiconductor circuits. With decreasing dimensions in integrated circuit technology new physical and engineering challenges are focused on the interaction between the defects and dopants introduced during implantation. Now, with device dimensions deep in the submicrometer range, quantitative information about dopant-defect interactions are needed and must be taken into account in modern semiconductor device technology. The flexibility and compatibility of ion implantation with other fabrication processes enables the fast implementation of changes in new and advancing technology.

4.2.1 Ion Implantation into Silicon

Silicon is the most important semiconductor in the microelectronics industry and the basic material in VLSI and ULSI technology. Compared, for example, to germanium silicon has a larger bandgap ($E_g = 1.1$ eV) resulting in lower leakage currents allowing the device operation at higher temperatures up to ~150 °C. With the widespread and intensive silicon processing developments in integrated circuit technology based on MOS (or CMOS) device structures, ion implantation replaced the conventional diffusion doping for almost all planar silicon device structures. Ion implantation has become an essential doping process for manufacturing of MOS, CMOS, BiCMOS, and bipolar solid state silicon devices [92]. Therefore, the developments in ion beam processing of silicon mainly for CMOS technology stimulated the development of appropriate ion implantation tools and the application of ion implantation for other kinds of silicon devices, for example silicon detectors and sensors.

In *advanced CMOS technology* much more than 100 process steps are required to fabricate silicon integrated circuits (memory and processor devices). The wafers have to be lithographically patterned, doped, etched, and coated with various thin films. The advances in device design and shrinking of transistor dimensions require well-controlled fabrication processes, such as ion implantation, capable of uniform, controlled, and reproducible introduction of dopants into silicon. Ion implantation has become quite complex to meet the demands of small device structures such as the typical gate lengths of $<$100 nm in a complementary MOS (CMOS) device

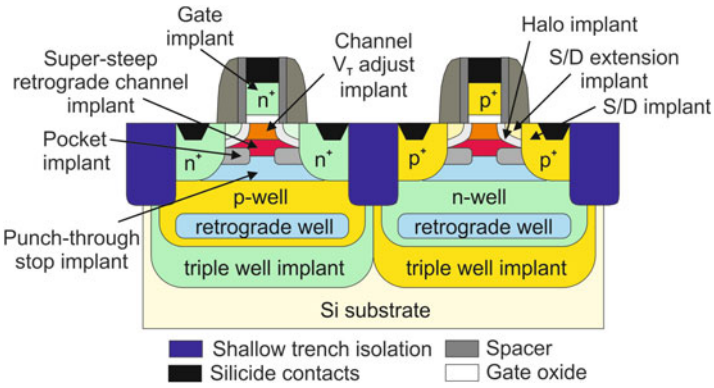

Fig. 4.18 Ion-implanted regions in a common CMOS transistor

shown in Fig. 4.18. The basic parts of the CMOS device are two MOS field-effect transistors (MOSFETs) consisting of one p-channel FET and one n-channel FET. To form both types of transistors in the same substrate, regions of opposite doping types are required separated by a shallow trench isolation (STI).

Figure 4.18 illustrates the sophistication of current implantation technology. More than 20 different implantations covering a wide range of energies (0.1 keV–1 MeV), fluences of 10^{11}–10^{16} cm^{-2}, and dopant species (mainly B, P, As, In) are typically used to tailor dopant profiles during device fabrication. The lowest energies are for junction formation and the highest for substrate or well doping. As shown in Fig. 4.18 ion implantation plays an important role in the fabrication of various integral parts of a CMOS transistor, where the most important ones are the formation of the transistor channel and the contact areas of source and drain as well as the doping of the wells. Scaling down the transistors in size, many implantation processes must meet the requirements for lower energies and higher doses to improve advanced transistor performance. Therefore, implantations such as source-drain extension implants, halo formation, and gate-electrode doping in the low energy regime have attracted widespread attention. All implantation processes in the fabrication of advanced silicon CMOS devices are summarized in the ion fluence-energy map of Fig. 4.19.

For all implantation processes shown in Fig. 4.19 the typical implantation parameters are summarized in Table 4.2.

Most of efforts in shallow pn-junction fabrication are focused on the formation of shallow source/drain junctions. Since boron has much higher diffusivity than phosphorous and arsenic, shallow p^+n-junctions have proven to be more difficult to form in CMOS devices compared to P- or As-doped shallow n^+p-junctions. The formation of shallow boron p^+n-junctions is limited by three effects: (1) small ion mass of boron and therefore relatively large projected range (penetration depth) requires ultra-low energy implantation with $E \leq 1$ keV, (2) increasing channeling of boron with decreasing ion energy, and (3) anomalous diffusion in the tail region

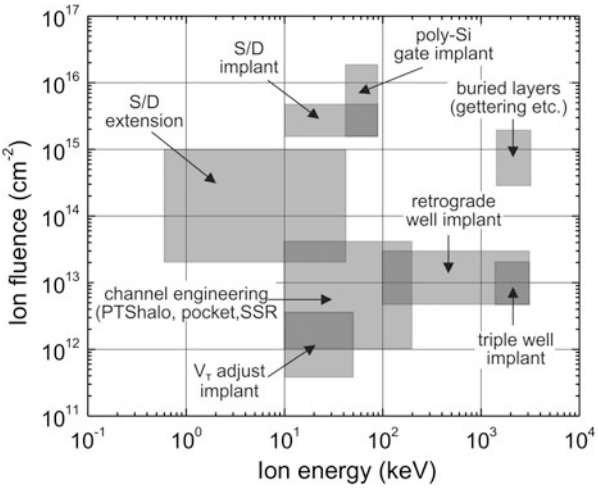

Fig. 4.19 Ion fluence–energy map of different ion implantations for silicon MOS-device and process technology (adapted after [93])

Table 4.2 Implantation processes and parameters for advanced CMOS transistor technology

Transistor region	Ions	Energy (keV)	Fluence (cm^{-2})	Remarks
Channel formation	P, B	10–80	1×10^{12}–5×10^{13}	Halo, PTS, LATIPS, Pocket, SSR
	As, In, Sb	80–200		High tilt angles and wafer re-depositioning
Transistor threshold voltage adjust	B, BF_2, As	10–50	4×10^{11}–4×10^{12} ($\rightarrow 1 \times 10^{11}$)	Transistor threshold voltage
Source/drain deep contacts	As, BF_2, B	10–80 ($\rightarrow$1–30)	2×10^{15}–8×10^{15} ($\rightarrow 1 \times 10^{15}$–$4 \times 10^{15}$)	Conducting source/drain areas
Source/drain extension	As, BF_2, B	0.5–30	3×10^{13}–1×10^{15}	Electric field reduction near S/D
poly-Si gate doping	B, BF_2, P	30–80 ($\rightarrow$2–30)	3×10^{15}–2×10^{16} ($\rightarrow 1 \times 10^{15}$–$8 \times 10^{15}$)	Conducting gate material
Preamorphization	Ge, Si	5–50	5×10^{13}–2×10^{15}	Channeling suppression
Retrograde wells	B, P	1,500–3,000	5×10^{12}–3×10^{13}	Off-state leakage current reduction
Triple wells	P, B	1,200–3,000 ($\rightarrow$5,000)	5×10^{12}–3×10^{13}	p- and n-well separation
Buried layers	B, P	1,500–3,000	2×10^{13}–5×10^{13}, 3×10^{14}–2×10^{15}	Subcollector in bipolar transistors
Proximity gettering	C, N, O, F, Si	1,500–3,000	5×10^{14}–5×10^{15}	Carrier lifetime improvement
SOI wafer fabrication	O	30–100	3×10^{16}–1×10^{17}	SIMOX
	H, He			Smart-Cut

of the implanted profile during high-temperature annealing due to transient-enhanced diffusion (TED).

Furthermore, scaling of supply voltage does not happen as fast as geometrical device scaling, such as gate length and gate oxide thickness. Because of this, the electric field in the device increases with scaling, resulting in aggravation of short-channel effect (SCE). Short channel effects impact MOSFET device characteristics such as threshold voltage V_{th}, subthreshold currents, and I–V behavior beyond threshold. In addition, it has been recognized that also increased reliability concerns such as hot carrier effect (HCE) and gate oxide reliability. Various transistor design techniques have been proposed and investigated to deal with SCE and HCE. One of the most important developments in transistor design to deal with SCE and HCE is the use of lightly doped drain (LDD) in conjunction with polysilicon gate sidewall spacer (see Fig. 4.18). Various other ion beam processing steps have been adopted in transistor fabrication. These include retrograde channel implantation, super-steep retrograde channel (SSR) implantation, halo or pocket implant with a large tilt angle, preamorphization implant (PAI), punch-through stopper (PTS), and large tilt-angle punch-through stopper implantation (LATIPS). Because silicon CMOS technology is one of the most developed semiconductor technologies, the used ion beam processing steps will be described in the principal sequence of their application to the CMOS transistor fabrication (see Fig. 4.18):

- Twin-well processing (or triple-well process)
- n-well and p-well processing
- Transistor channel processing
- n- and p-type source and drain processing
- Poly-Si gate processing

The principal ion implantation sequence in the advanced CMOS device manufacturing process starts with high energy implantation to form the retrograde wells, after that the medium energy implantation for punch-through stop (PSS) and low energy implantation for threshold voltage (V_{th}) adjustment. After gate patterning low energy source/drain extension (SDE) implantation, and halo implantation under high tilt angles are carried out. The final implantation steps are the doping of deep S/D areas by medium energy implantation.

Step 1: Retrograde n- and p-wells implants

The areas where the transistors will be fabricated—the n-channel MOSFET in the p-well and the p-channel MOSFET in the n-well—are achieved by high energy implantation of B^+ and P^+ (or As^+) ions, respectively, at energies ranging from a few 100 keV to several MeV with a peak concentration at a depth of about 1–2 μm below the surface. The ion energy depends on the device type and its application for high speed logic (processor) and DRAM memory devices with relatively shallow wells and for SRAM and flash memories with deeper wells. In former fabrication processes, the p- and n-wells were formed by medium energy implantation followed by a deep thermal in-diffusion which is eliminated in modern technology, allowing the use of RTA with a small thermal budget. This eliminates lateral dopant diffusion and permits better device scaling (higher transistor packing density). Retrograde well implantation is normally self-aligned to the already performed

oxide-filled shallow trench isolation (STI). Profiled well implantation can be performed with an arbitrary impurity distribution to optimize many device characteristics almost independently. Buried layers with n-profiled and p-profiled wells are fabricated alternatively using multiple high energy ion implantations (B^+ for a p-well and P^+ for an n-well) by controlling ion energy and fluence independently. The resulting multiple depth profile is usually called triple well structure. The application of triple well structures provides important advantages to several different CMOS devices. They include memory devices (DRAM, flash, and SRAM) and embedded CMOS technologies with memory and logic devices on the same chip [94]. In triple well technology, the addition of moderate fluence high energy P^+ and B^+ ion implants allows the creation of separate p-wells and n-wells which are isolated from p- and n-substrates, respectively. To take full advantage of triple well structures, high energy (2–3 MeV) ion implantation is preferred over other approaches, like deep diffusion with long thermal treatment at high temperatures (~1,150 °C). In typical triple well processes, the deep n-well that forms the added isolation of the third well requires P^+ implantation with an ion energy up to 3 MeV at a fluence of 1×10^{13}–1×10^{14} cm^{-2} Additionally, the boron p-well, which is implanted into the deep n-well, will require up to 1 MeV at a fluence of 1×10^{13}–1×10^{14} cm^{-2}. Typically, these processes form 2.5–3.5 μm deep buried n- and p-wells with a retrograde dopant profile (low subsurface dopant concentration). In order to pattern and mask the very deep implants, thick photoresist masks are required with thicknesses of 3.5–5.5 μm. Thermal diffusion treatment is not required, and dopant activation and implantation damage recovery can be achieved by the subsequent thermal processes, for example during the gate oxidation step. Retrograde triple well processing allows the formation of a buried n-well beneath selected n- and p-wells without surface compensation of dopants, which can lead to improved device performance. The impurity concentration at each depth determines the respective CMOS-FET device characteristics, such as threshold voltage, hot carrier generation, punch-through voltage, junction breakdown voltage, junction capacitance, latch-up susceptibility, soft-error immunity, etc. Isolation characteristics, inter-well or intra-well, are also determined by impurity concentrations at certain well depths. Since a high energy implanted well can usually be made shallower than a conventional diffused well, the trenches for isolating wells also become shallower and easier to fabricate.

Step 2: Anti-punch-through and threshold shift implants

The anti-punch-through implant following the well implantations is applied to create a higher doped region between the transistor channels and the maximum of the well-implanted profiles to prevent punch-through from the drain depletion regions extending to source depletion regions. The anti-punch-through implantation is usually carried out at medium ion energies of 50–200 keV and low fluences of 10^{12}–10^{13} cm^{-2}. The natural threshold of the NMOS transistor is about 0 V and that of the PMOS transistor is about –1.2 V. An implantation for p-type doping is used to make the NMOS transistor harder to invert and the PMOS transistor easier resulting in both threshold voltages balanced around $V_{th} \approx 0$. The threshold voltage can be adjusted to the desired level by increasing the doping level through a low energy

and low fluence ion implantation into the channel region. The threshold adjust implantation is very sensitive to doping variations and requires very reproducible ion beam energies and fluences. The energy depends on the thickness of the gate oxide present during implantation. The threshold voltages of both n-type (V_{thn}) and p-type (V_{thp}) transistors are adjusted to typically equal values of +0.6 V and −0.6 V, respectively.

In modern CMOS technology for V_{th} adjustment implantation, light ions B^+ and P^+ are often substituted by heavy ions (e.g., In^+ for B^+ in n-channel MOSFETs and Sb^+ for P^+ in p-channel MOSFETs) to reduce its diffusivity and dopant redistribution during subsequent thermal processes [95]. These so-called super-steep retrograde (SSR) channel profiles allow the fabrication of deep-submicron MOSFETs with suppressed punch-through effect, improved electron mobility, and lowered interface dopant concentration level [96]. The need for nonuniform channel doping is described more in detail by Taur and Ning [97].

Step 3: Implantation of lightly doped source/drain regions

After patterning of the gate insulator and gate electrode, shallow doped ($\sim 10^{20}$ cm^{-3}) source and drain regions next to the more lightly doped ($\sim 10^{18}$ cm^{-3}) active channels of the MOSFETs are fabricated in a self-aligned manner by low energy and low fluence implantation. These shallow S/D profiles are called S/D extensions and are commonly found in modern MOS device designs. The doping profiles in the S/D regions have a profound impact on the channel performance (e.g., short channel effects). As a result, considerable effort has been also put into the optimization of the S/D. The shallow S/D extension was originally motivated by a desire to relieve high electric fields and the resulting breakdown of the device due to hot electron effects [15]. For modern high performance devices however, the S/D extension is stronger motivated by the trade-offs between short channel effects and the S/D resistance. The S/D extensions represent a shallow effective S/D junction to the channel regions, while at the same time, minimize the contribution of the S/D regions to extrinsic resistance through the presence of the deep S/D regions. The S/D extensions are formed by using of low dose and low energy dopant implantations.

Step 4: Source/drain halo implantation

Lateral channel engineering is used extensively to improve device performance. Typically, lateral engineering is accomplished by angled implants into the channel region following gate patterning. The halo implant is normally performed under high angles of 30–60° to counterdope the source/drain extension regions, which is done after poly-silicon gate patterning but before nitride spacer formation. Halo implants need to be performed with four 90° rotations of the wafers to dope both sides of the differently orientated transistors. The lateral implants cause an increase in doping concentrations near the edges of the SDE regions. The use of halo implants can improve short channel effects [98] and thereby control the so-called threshold voltage roll-off [99]. For devices with long channel lengths, the impact of the halo implant is minimal. As the channel length is decreased, the portion of the channel with an increased dopant level becomes more and more significant, leading to an increase in the effective channel doping level with decreasing channel length.

Step 5: Implantation of the heavily doped sources/drain regions

Only after the formation of the spacers, the higher fluence and higher energy dopant implantations are then followed to form the source/drain region by using the spacers as masks. Additionally to the completed sources and drain doping, this step provides the implantation of ohmic contact areas into the p- and n-wells and into the substrate. For S/D- (and well) contact areas it is important that they have a lowest possible resistance which requires medium energy (10–80 keV) and high fluence implantation with fluences in the order of ~(1–5) $\times$ 10^{15} cm^{-2} for As^+ in the case of n-channel MOSFETs and for B^+ (or BF_2^+) in the case of p-channel MOSFETs. At these implantation conditions highly doped ($>10^{20}$ cm^{-3}) S/D contact areas adjacent to the more slightly doped (~10^{18} cm^{-3}) S/D-extensions are formed. As^+ ions are preferred due to their low diffusivity and higher solubility in Si compared to P^+ ions. Because boron has a higher diffusivity it is more difficult to fabricate shallow S/D-junctions in p-channel MOSFETs. S/D areas have an opposite conductivity to create a pn-junction and a good isolation to the surrounding wells. Junction depths of $\leq$100 nm are typical for scaled MOSFETS with channel length below 0.25 μm [100].

Step 6: Poly-Si gate implantation

As a gate contact material polycrystalline silicon (poly-Si) with a thickness of ~300 nm is deposited by LPCVD on top of the gate insulator and subsequently highly doped by high fluence implantation. This step is carried out simultaneously with the S/D implantation because ion energies and fluences in both cases are comparable. n^+-type poly-Si doping for n-channel MOSFETs and p^+-type poly-Si doping for p-channel MOSFETs are usually achieved by P^+ or As^+ and B^+ (BF_2^+) implantation, respectively. The dopant activation in poly-Si during subsequent annealing must be done carefully to avoid their diffusion through the gate insulator (SiO_2, HfO_2, etc.) into the transistor channel, which can lead to undesired V_{th} variation [101]. For p^+-type doping of poly-Si low energy B^+ is preferred because of fluorine enhanced diffusion of boron through ultrathin gate oxides that occurs at annealing of BF_2-implanted poly-Si [102]. This effect can be reduced by forming a gate oxinitride, either during oxidation or by N^+ co-implantation.

In order to fabricate more and more shallow pn-junctions, recent efforts are done with respect to the following ion implantations: (1) lowering the ion energy to around 100 eV, (2) use of heavier ion species and in some cases of molecular and gas cluster ions (e.g., decaborane $B_{10}H_{14}$, octadecaborane $B_{18}H_{22}$), and (3) preamorphization by Si^+, Ge^+, or Xe^+ ion implantation to avoid channeling effects.

Co-implantation of N^+, F^+, and C^+ ions together with boron implantation for shallow source/drain doping is often used in deep submicron MOSFET fabrication to suppress transient-enhanced diffusion (TED) of boron [103] and boron deactivation (so-called reverse annealing) [104] during subsequent thermal annealing. Furthermore, applying N^+ co-implantation to the gate doping, the gate silicon oxide can be nitrided, thus suppressing the boron penetration through the SiO_2 and improving the reliability and hot carrier resistance of the gate oxide.

The different ion implantation processes described earlier are included in advanced CMOS technology to fabricate MOSFETs with 28 nm gate length and

with metal/high-K gate structures. As dopant ions B^+, BF_2^+, P^+, As^+, Sb^+, and In^+ as well as heavy boron molecule and cluster ions are implanted to form several types of MOS transistors. Implantation steps with Ge^+ or Xe^+ ions for silicon preamorphization, the stress memorization by As^+ implantation into the poly-Si gate electrode to increase the charge carrier mobility in the transistor channel [105], and co-implantation of C^+, F^+, N^+ are employed. Thus, the application of all these implantation steps results nowadays in a total number of 40–50 ion implantations.

Discrete high-power devices with current handling capability ranging from 100 A to several 1,000 A at high voltages can be divided into majority carrier devices (Schottky diodes, power MOSFETs, junction field-effect transistors—JFETs) and minority carrier devices (thyristors, bipolar transistors, isolated gate bipolar transistors—IGBT and pin-diodes).

The charge carrier lifetime significantly influences the operation parameter of bipolar power devices such as diodes, thyristors, and IGBTs. High charge carrier lifetime (~0.1–1 ms) is required, in order to keep on-state charge carrier losses low. On the other hand, power devices required to operate at high frequencies need a short carrier lifetime in certain device regions, in order to achieve a fast turn-off state and a minimization of the reverse recovery charge. The reduction of the carrier lifetime can be achieved by introducing recombination centers either by in-diffusion of metallic impurities (e.g., Au, Pt) before final device contact metallization or by irradiation with high energy light ions (H^+, He^+) from the device back side, which is usually the last step in power device processing sequence. Compared to diffusion of metal impurities the advantages of high energy ion irradiation with H^+ and He^+ ions are the local decrease of carrier lifetime by ion-induced defects with precise spatial damage location and defect density in the device depletion zone, no metal contamination, and low device leakage current [106–108]. H^+ and He^+ (or He^{++}) irradiation are carried out at typically 1–10 MeV ion energy with fluences of about 10^{10}–10^{12} cm^{-2}. At these irradiation conditions the mostly damaged regions (depth of the Bragg peak) are located in a depth of 10–500 μm and of 3–70 μm for 1–10 MeV H^+ and 1–10 MeV He^+ irradiations, respectively. Among other created defects (single vacancies, interstitials, vacancy-impurity complexes, etc.) the most useful ion induced defects in these regions are silicon singly negative-charged divacancies ($V_2{}^{-1}$) with a deep level in the band gap ($E = E_C$−0.41 eV, [109]) and a concentration of about ~10^{14}–10^{16} cm^{-3} at typical irradiation with 5 MeV H^+ and He^+ ions and a fluence of 1×10^{12} cm^{-2}, respectively. The silicon divacancy is of special interest because it is temperature stable until 300 °C which is important for reliable device operation. At this deep level an enhanced charge carrier recombination can be achieved due to a low recombination lifetime τ_R preserving at the same time a high generation lifetime τ_G time for low reverse currents. Consequently, the aim of lifetime engineering in power devices by high energy ion irradiation is a maximization of the lifetime ratio τ_G/τ_R and therefore to ensure increased switching speed (higher frequencies) and decrease of power losses (heat reduction).

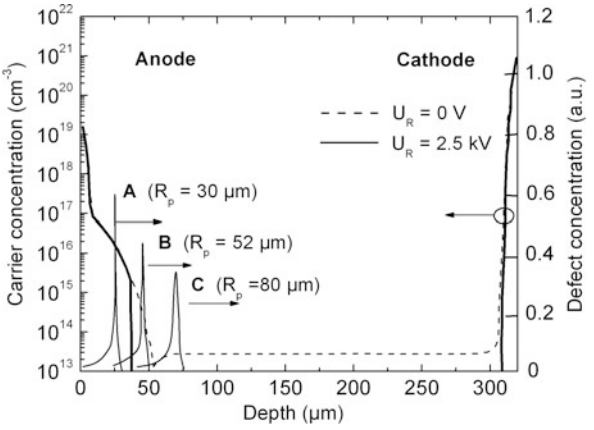

Fig. 4.20 Charge carrier profiles in a P^+PNN^+ diode at reverse voltages of $U_r = 0$ V (*dashed*) and $U_r = 2.5$ kV (*solid*) with simulated profiles of the damage resulting from ion irradiation into regions A, B, C

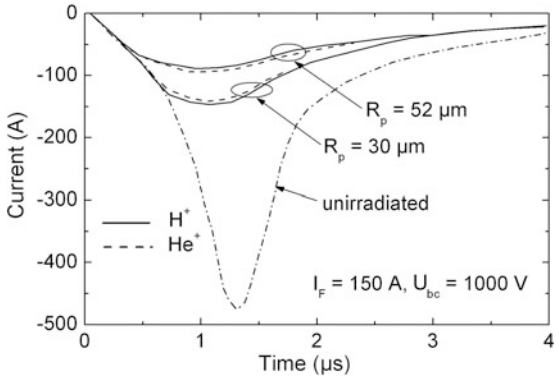

Fig. 4.21 Reverse recovery waveforms of an unirradiated diode and diodes irradiated by H^+/He^{2+} ions (fluence $5 \times 10^{12}/5 \times 10^{11}$ cm^{-2}, *solid/dashed*)

As an example of local lifetime engineering in power diodes, the implantation conditions and the resulting reverse current recovery behavior are shown in Figs. 4.20 and 4.21, respectively [108, 110].

In this case, ion energies of 1.8, 2.4, and 3.0 MeV for H^+ and 7.1, 9.6, and 12.1 MeV for He^{2+} were chosen in that way to place the damage peak into three qualitatively different regions of the diode [anode side of the junction outside (A) and inside (B) of the space charge region, and the N-base side of the junction (C)]—see Fig. 4.20. The chosen ion energies guarantee identical projected ranges in silicon R_p (30, 52, and 80 µm) for both projectiles. The fluences were set differently for H^+ and He^{2+} ions (2×10^{11}–5×10^{12} and 2×10^{10}–5×10^{11} cm^{-2},

respectively) to provide equivalent carrier recombination rates. After irradiation, all diodes were annealed at 200 °C for 60 min to stabilize the radiation defects.

The effect of H^+ and He^{2+} irradiation on the turn-off characteristics (Fig. 4.21) is identical, if the H^+/He^{2+} fluence ratio is set to 10. As can be seen, local lifetime control by ion irradiation can speed-up the diode switching and soften the current recovery by leaving enough charge on the cathode side. Moving of the projected ion range R_p close to the anode (from region C to A) reduces the storage time and fastens the space charge region development. Nevertheless, the effect of local lifetime control on reverse current I_r and break-down voltage U_{br} is more complex and varies according to the location of the damage maximum [110, 111].

It is shown that optimal lifetime structuring over device depth giving superior recovery characteristics is achieved by a well-balanced combination of two or more consecutive local lifetime treatments. Beside the ion irradiation fluence, the irradiation procedure involves a proper choice of irradiation energy [112]. Since any radiation defect profile can be created by superposition of several irradiation steps, the combination of ion and electron irradiation provided further device improvement.

Another example for improvement of power device performance by back-side high energy ion irradiation of metal oxide semiconductor gate turn-off thyristors (MOS-GTOs) is given in [113]. This type of power device seems to be very promising especially in high voltage applications, thanks to a very low voltage drop and good switching performances. He^+ ion irradiation was executed at ultra-high ion energy of 40 MeV in the fluence range of (0.25–1.0) $\times$ 10^{10} cm^{-2} using a cyclotron in order to obtain a local damage peak at a depth of ~700 μm for charge carrier lifetime lowering at the transition between N^- drift and N^+ buffer layers of the MOS-GTOs. The irradiation in this case was performed with He irradiation from the back side of the wafer thus avoiding any damages at the gate oxide of MOSFET placed on the device front side. Experimental results show that He^+ irradiation can significantly improve the turn-off switching performances of the MOS-GTO without affecting its on-state and turn-on switching characteristics. A proper localization of defect peak concentration, obtained by changing the parameters of the irradiation (energy and fluence), has been used to optimize the device characteristics and to improve significantly its switching performances. A reduction by more than 30 % of the turn-off energy losses compared to nonirradiated MOS-GTO devices was demonstrated using ultrahigh He^+ ion irradiation.

Among ion irradiation based local defect engineering, ultrahigh energy boron implantation for doping of deep pillar-like p-type regions into depths up to 40 μm is of great interest for high-voltage super-junction devices (SJDs) and was firstly introduced by Infineon's CoolMOS technology between 1998 and 2000 [114–116]. The CoolMOS™ high voltage MOSFET devices do not show bipolar current contribution like the well known tail current observed during the turn-off phase of IGBTs. Advantageously, the CoolMOS™ device virtually combines the low switching losses of a MOSFET with the on-state losses of an IGBT.

For the vertical p-type pillars devices, the state of the art successive epitaxial growth of n^--type layers (overall thickness ~35 μm) combined with local p-type

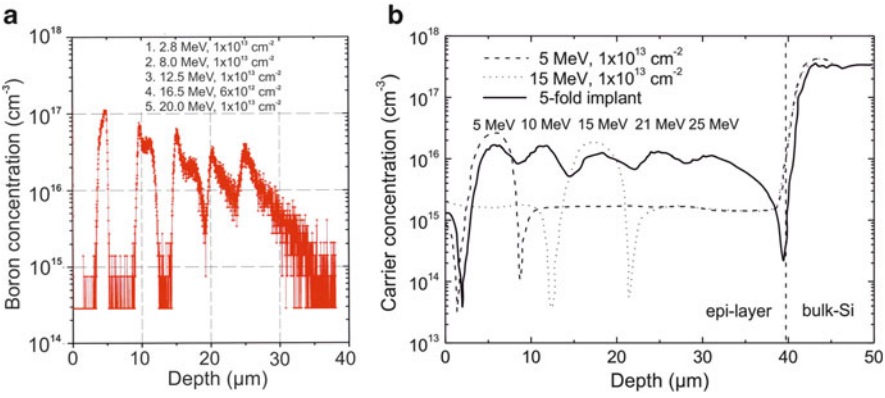

Fig. 4.22 (**a**) Boron depth profile measured by SIMS of a fivefold B^+ implantation using ion energies between 2.8, 8.0, 12.5, 16.5, and 20 MeV, and (**b**) corresponding charge carrier depth profile obtained by spreading resistance measurement. The n-type epi-layer has a thickness of 40 μm and a carrier concentration of 2×10^{15} cm^{-3}. The high charge carrier concentration of the n^+-substrate is ~4×10^{17} cm^{-3} [118]

diffusion and/or low energy ion implantation is time consuming and cost intensive. As an alternative low cost vertically structured doping process, recently ultra-high energy boron implantation was proposed to form the vertical p-type pillars [117, 118]. This concept represents a major simplification of SJDs fabrication since the overall number of process steps is drastically reduced.

For the patterned implantation of high-energetic boron ions, silicon stencil masks are placed in proximity to the wafer. In order to ensure safe masking even for 25 MeV, B^+ ions with a projected range of $R_p = 34$ μm the thickness of the silicon mask had to be 45 μm [118]. The ultra-high energy boron implantation consists of a fivefold implantation sequence with B^+ ion energies between 2.5 and 25 MeV and fluences from 5×10^{12} to 1×10^{13} cm^{-2} per implantation step. Due to the high aspect ratio (7:1) of the Si stencil mask the implantation was carried out perpendicular to the wafer surface. The as-implanted boron profile measured by SIMS in Fig. 4.22a clearly shows the well-separated boron doped regions of the fivefold implantation sequence. Each peak shows a characteristic distribution with contributions from channeled and dechanneled ions.

The strong influence of axial channeling is evident as the implantations were performed under normal incidence conditions. Whereas for the lowest energy the peak distribution is mainly determined by channeled ions the influence of the channeling decreases with increasing energy. To obtain a continuously p-type doped pillars the wafers were subsequently annealed at 1,150 °C for 6 h enabling p-type regions with charge carrier concentrations of $n_A \sim 10^{16}$ cm^{-3} in a depth between 2 and 40 μm and a sufficient homogeneity in the spatial carrier concentration which was confirmed by spreading resistance depth profiling shown in Fig. 4.22b [118]. It was demonstrated that the developed high energy implantation process yields fully functional high-voltage MOS transistors with high blocking voltages and low reverse leakage currents. A more detailed description of the device properties is given in [119].

Today, silicon planar technology including ion implantation is being utilized extensively to advanced *silicon sensor and detector technologies* [120–125]. In these areas, attention was first focused on microsensor (i.e., microfabricated sensor) development.

Today, common ion implantation is implemented in sensor and detector technology to fabricate doped regions in different device structures (diodes transistors, resistors, etc.). In some sensor applications, ion implantation is often followed by a diffusion step to get wanted impurity profiles going deeper than a few parts of a micrometer normally achieved by implantation. In this way, ion implantation is used as a predeposition technique, using its high ion fluence accuracy to improve the accuracy of the doping concentration. So, boron-implanted resistors for piezoresistive micromachined sensors have a resistance value accuracy down to 1 %, which is much better than that achievable with the thermal diffusion technique. Therefore, ion implantation is the dominating way of making advanced piezoresistive sensors.

In the field of radiation detectors (photodetectors, charged particle, and X-ray detectors), high responsivity and collection efficiency of charge carriers generated by radiation are required. This can be only reached using low damage shallow pn-junctions in the radiation entrance window of the radiation sensing device. Although radiation sensors are relatively simple in design with relatively large structure sizes in comparison with integrated microelectronic circuits the requirement of maintaining the high-quality silicon properties (e.g., extreme low impurity concentration, high minority charge carrier lifetime of $\geq$1 ms) during processing did not allow a straightforward application of the microelectronic planar technology. The requirements on ion beam processing in some aspects are more stringent due to the processing of commonly used high purity Float-Zone silicon (FZ-Si) without degradation of its properties, for example, by the introduction of impurities or the creation of defects, the processing of both wafer sides without damaging the opposite surface, and the production of even wafer-sized defect-free radiation detectors.

Using the flexibility of ion implantation, for example, tailoring of doping profiles with exact location of its maximum at the SiO_2/Si interface implanting through thin SiO_2 layers or producing of buried doping profiles is easily possible. In the following selected examples for the application of high energy ion implantation to the fabrication of advanced radiation sensing devices will be described. The aim of high energy ion implantation for the fabrication of buried doping layers is the optimization of the electric field distribution $E(x)$ and the increase of the high electric field strength in the device depletion region without breakdown. This approach has been introduced to replace high-temperature deep diffusion processes and epitaxial growth of doped silicon layers in the fabrication process of radiation sensing devices.

In *Avalanche Photodiodes* (APD) a high electric field is necessary to reach the regime of photon generated charge carrier multiplication up to a level of $M \sim 10^2$–10^3 at low dark currents. Figure 4.23 shows typical doping profiles and electric field distribution for a conventional silicon $N^+P\pi P^+$ APD with a deep diffused P-layer (Fig. 4.23a) and an $N^+\pi P\pi P^+$ APD with a buried MeV-implanted P-profile [126] (Fig. 4.23b), respectively.

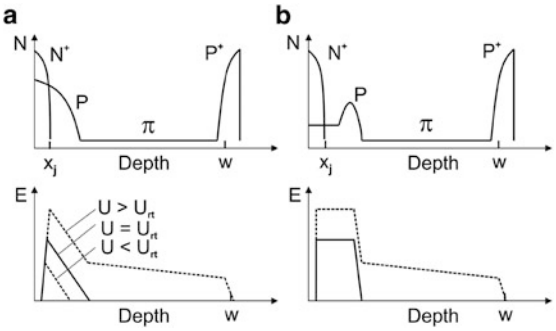

Fig. 4.23 Principal doping profiles and typical electric field distributions of a conventional silicon $N^+P\pi P^+$ APD with a deep diffused P-layer (**a**) and an $N^+\pi P\pi P^+$ APD with a buried MeV-implanted P-profile (**b**). U_{rt} is the so-called reach-through voltage

As can be seen in Fig. 4.23a the highest electric field in the $N^+P\pi P^+$ structure is restricted to a very small depth region at the N^+P-junction whereas for the $N^+\pi P\pi P^+$ structure in Fig. 4.23b with a buried MeV-implanted P-profile the electric field has a constant high value of (1–3) $\times$ 10^5 V cm^{-1} over a certain depth region. As an advantage of high energy boron implantation, the width of the constant high electric field region and the electric field strength can be precisely tuned by changing the ion energy and the ion fluence, respectively. For the deep B^+ ion implantation, the maximum of the buried P-layer is located at a distance of 2.75 and 3.1 μm from the surface for ion energies of 1.5 and 1.8 MeV, respectively. The ion fluence is low—in the range of (1–2) $\times$ 10^{12} cm^{-2}—and has to be carried out with high demands to homogeneity and fluence accuracy with errors <1 % [126]. Precise control of the conditions for the two implantation steps ensures good process reproducibility, which is particularly easy to do for epitaxial π/P^+ wafers, and also a good fabrication yield. APDs obtained in this way offer excellent photoelectric performance, e.g., low dark current ($I_0 < 1$ nA) close to the breakdown, high gain of $M > 150$, resulting in a sensitivity greater than 75 A/W, as well as excellent uniformity in the avalanche set point (ASP) of $\leq \pm 5$ % and improved correction of ASP temperature dependence.

The sensitive area of APDs could be also increased thanks to the excellent spatial homogeneity offered by the implantation technique compared to APDs fabricated only by diffusion processes. Figure 4.24 shows, for example, typical dependence of the multiplication factor M on the bias voltage U of an APD with $x_j = 400$ nm of the N^+p-junction for different B^+ ion fluences implanted at 1 MeV. As can be seen the $M(U)$ characteristics of the APD depend very sensitive on the B^+ ion fluence.

Silicon PIN diodes are also widely used for the detection and spectrometry of ionizing radiation, in particular of charged particles, e.g., electrons (e), protons (H^+), α-particles (He^+), and heavier ions (see also Sect. 3.4.5). Today ion implantation is the standard doping process for the fabrication of shallow p^+n-junction regions and n^+-contacts in n-type high resistivity silicon using low energy

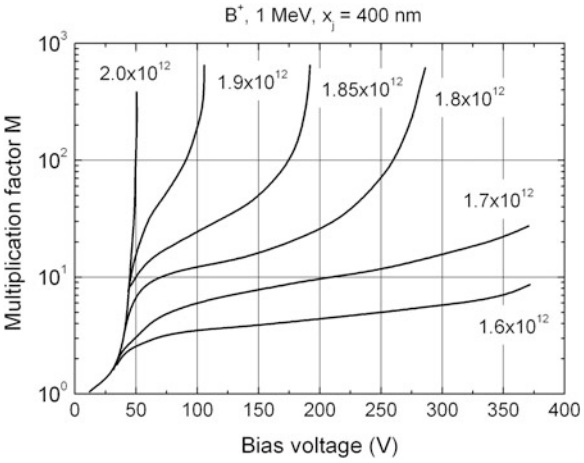

Fig. 4.24 Typical dependence of the multiplication factor M on APD bias voltage *U* for different B^+ ion fluences (in cm^{-2}) implanted at an ion energy of 1 MeV [127]

implantation of boron and arsenic/phosphorous (10–30 keV, 10^{14}–10^{15} cm^{-2}), respectively, which was introduced by the pioneer works of Kemmer [128, 129]. This detector technology and a variety of advanced structures such as strip or pixel detectors, the silicon drift chamber detectors (SDCDs), or fully depleted junction charge-coupled devices (CCD's) have been further developed during the last decade [123–125, 130]. Besides, relatively high energy ion implantation (300–600 keV) has been used to implant deep $n^{(+)}$ or $p^{(+)}$ layers into high resistivity silicon for fully depleted CCDs, SDCDs, or for junction field-effect transistors (JFETs) monolithically integrated on these detectors [131, 132].

In the following some examples for applications of the MeV ion implantation technique in the detector fabrication technology will be discussed. The motivation, as also in the case of APDs, arises from the fact that local changes of the substrate doping can be used to modify the vertical electric field distribution of silicon pn-junction detectors. Low dose MeV implantation of phosphorous in n-type silicon has been applied to realize pn-junction detectors with high field regions (HFR) extending from the surface to a depth of several micrometer ($p^+nn^{(-)}n^+$ structure). Using silicon pn-junction detectors with classical $p^+n^{(-)}n^+$ structure for heavy ion spectroscopy two particular problems arise, namely the plasma delay and the pulse height defect (PHD). This PHD is usually defined as the energy difference obtained in the spectrum between the peak position of heavy ions and protons (or α-particles) of the same incidence energy. The PHD is caused by three effects: the nonnegligible energy loss of heavy ions in the detector entrance window (front contact and p^+-layer), the increasing contribution of the nonelectronic nuclear stopping with increasing ion mass, and the deficit due to the plasma recombination of charge carriers along the ionization track of the incident particle. It is well known that the effective silicon dead layer and the plasma recombination at ionization densities

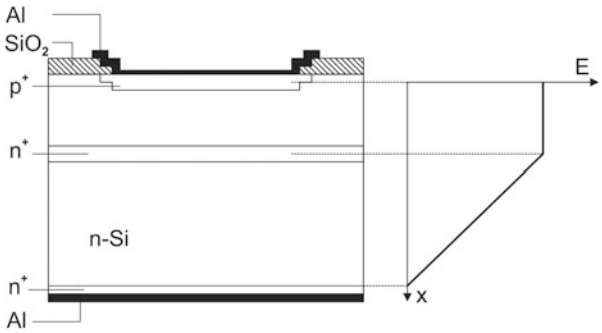

Fig. 4.25 Schematic view of the modified detector structure with a buried n^+ doping profile and the electric field distribution of the reverse bias detector

$\geq 10^{19}$ e/h-pairs per cubic centimeter depends on the electric field strength [133, 134]. Therefore, detectors with enhanced internal electric fields of $E > 10\,\text{kV cm}^{-1}$ are preferred for the spectroscopy of heavy ions owing large electronic stopping power. Silicon detectors with such high internal electric field have been fabricated applying MeV ion implantation of P^+ ions into high resistivity n-type detector-grade silicon [135, 136]. The novel silicon detector structure proposed in [135] with a high internal field strength up to $E = 200\ \text{kV cm}^{-1}$ is shown schematically in Fig. 4.25.

The conventionally employed p^+n-junction structure based on high resistivity n-type material ($\rho \geq 2{,}000\ \Omega$ cm) is modified by a 10 MeV P^+ high energy ion implantation at low fluences in the range of 1×10^{11}–$1 \times 10^{12}\ \text{cm}^{-2}$ leading to a buried region of enhanced n-type bulk doping with the maximum of the profile at a depth of 4.75 μm. The depth of the HFR and the maximum electric field strength can be established separately by the energy and the fluence of the MeV implantation, respectively, as shown Fig. 4.26.

Figure 4.26 shows the calculated electric field distribution for a detector modified by a P^+-implantation at 10 MeV with different fluences. The local enhancement of the bulk doping due to the MeV implantation results in an increased and nearly constant electric field up to the depth of the buried layer at ~4 μm. Behind the $n^{(+)}$ layer the electric field linearly decreases analogous to the conventional detector configuration. This field distribution is similar to diodes, which are produced using epitaxial $n^{(+)}$ layers on high resistivity material. Implantation fluences above $\Phi > 2.5 \times 10^{11}\ \text{cm}^{-2}$ result in high field regions with $F > 50\ \text{kV cm}^{-1}$, which exceed those of conventional heavy ion detectors. For an implantation fluence of $1 \times 10^{12}\ \text{cm}^{-2}$ even an electric field strength above $100\ \text{kV cm}^{-1}$ can be easily realized, which is more than a factor of ten higher compared to conventional $p^+n^{(-)}n^+$-diodes. The performance of detectors with different high field regions has been tested using oxygen ions with energies between 0.9 and 8.5 MeV [135]. Figure 4.27 shows the measured ion energies as a function of the electric field strength. The bias voltage for all detectors was changed from 5 up to 200 V to obtain an electric field overlap between detectors with different HFRs.

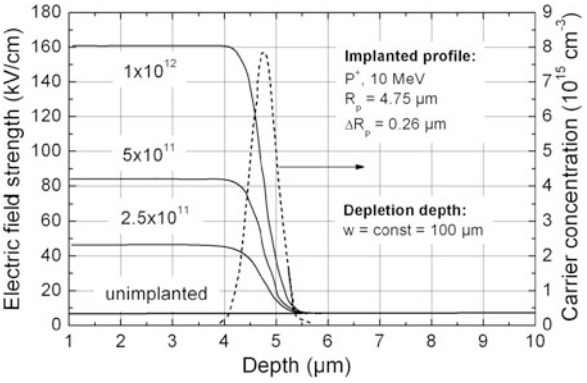

Fig. 4.26 Electric field strength versus depth of a HFR silicon detector (P^+, 10 MeV) as a function of ion fluence for a fixed depletion depth of 100 μm

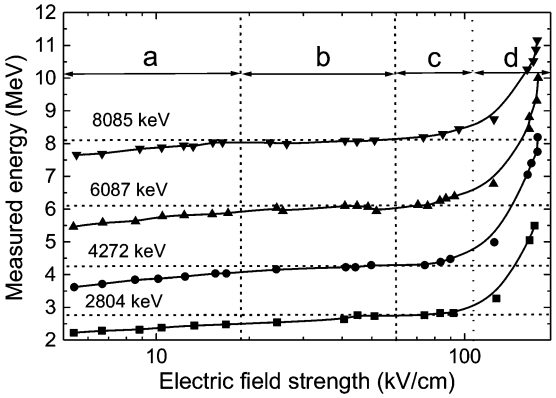

Fig. 4.27 Measured signal amplitudes of different HFR detectors in dependence on the electric field strength for various ion energies of oxygen (2.80, 4.27, 6.09, and 8.09 MeV); parameter: P^+, 10 MeV: (a) unimplanted, (b) 2.5×10^{11} cm^{-2}, (c) 5.0×10^{11} cm^{-2}, (d) 1.0×10^{12} cm^{-2}

Three regions can be clearly distinguished. The measured energy continuously increases with the electric field up to a constant value, which is obtained at around $F = 35$ kV cm^{-1}. The following nearly constant part of the curves can be interpreted as the region of maximum carrier collection from the window and the ionized track in the depletion zone. At electric fields above 100 kV cm^{-1} a significant enhancement of the pulse height was measured caused by charge carrier multiplication (avalanche effect). The beginning avalanche multiplication at moderate field strength of about 80 kV cm^{-1} is surprising and gives rise to the conclusion that the electric field is strongly enhanced near to the end of the "conducting needle" of the plasma track.

Recently, silicon detectors with HFR have been also developed for the detection of electrons in modern electron lithography tools [136]. In principle the electron detector consists of a conventional p^+n-junction diode where the pn-junction area is covered with an additional electron beam patterned heavy metal layer (2.5 μm thick Cr/W layer), which possesses well-defined windows of various dimensions in the micrometer and nanometer range. This heavy metal layer acts as an absorber allowing the electrons to penetrate the sensitive junction area only through these windows. From the evaluation of the detector signal arising from a scanned beam across windows of different size one can derive information about the properties of the incoming beam such as spot size, homogeneity, current density, skewness, etc. [137]. The requirements for electron beam lithography tools are closely related to the use of higher electron energies (30–50 keV to maintain better pattern fidelity) and higher electron current densities (to increase the throughput). Even more critical, tighter beam specifications have become more and more important. Consequently, the diagnostics and control of the e-beam parameters in the e-beam writer are of fundamental relevance. One main problem of conventional Si pn-junction detectors applied for the diagnostics of intense electron beams is the nonlinearity between the incoming electron current and the detector response measured as an output voltage after external signal processing. For typical electron beam current densities of several ampere per square centimeter, ionization leads to the formation of a nearly spherical volume with a high electron/hole (eh) concentration of 10^{17}–10^{18} eh-pairs/cm^3 (often called plasma cloud). During the characteristic plasma time (some ns), this cloud screens the external field and eh-recombination is favored. Standard Si detectors made from high resistivity Si (resistivity ~ kΩ cm) which are characterized by a triangular field distribution with a maximum field strength of only 2–3 kV cm^{-1} do not enable complete eh-separation without any charge loss for the diagnostics of intense electron beams (the same problem as for heavy ion detection). Because the plasma time is roughly inverse proportional to the electric field strength an increase of the electric field is necessary to lower plasma-based charge losses in such electron detectors. For this purpose, detectors with an enhanced electric field strength of about 10–20 kV cm^{-1} have been fabricated in a standard planar process including a high energy (MeV) ion implantation step with nearly the same implantation parameters as used for heavy ion detectors. Considerations concerning the ion energy are derived from the electron ionization depth distribution shown in Fig. 4.28a.

The stopping power peak shifts from 1 μm to about 5.5 μm by increasing the electron beam energy from 20 to 50 keV. Furthermore, for higher energies the distribution is characterized by a larger width and a lower value of the stopping power. As shown in Fig. 4.28b over the interesting depth the electric field strength between 20 and 30 kV cm^{-1} can be easily varied by choosing an appropriate implantation fluence in the range (1.0–2.5) × 10^{11} cm^{-2}. As the HFR is formed only at a small part (~3.5 %) of the larger p^+n-junction area (52 mm^2) implantation masks suitable for MeV ion implantation are required. Low implantation fluences allow to use thick film photoresist masks of 20–25 μm thickness. The fabrication of the p^+- and n^+-layers (see Fig. 4.25) was carried out in a conventional procedure

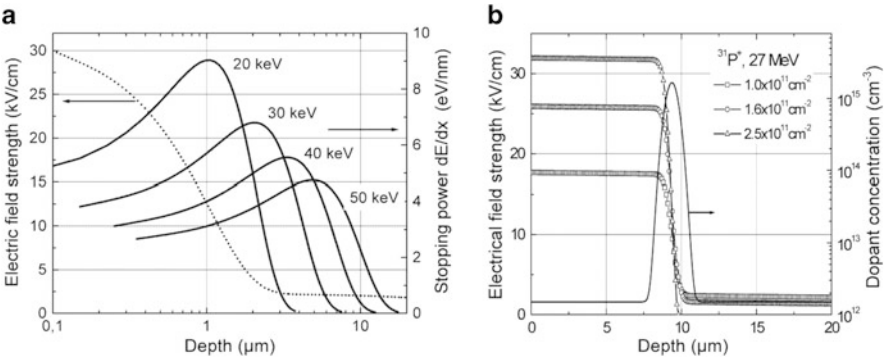

Fig. 4.28 (**a**) Stopping power due to ionization for electrons ($E = 20$–50 keV) in Si and electric field distribution for conventional deep diffused n^+-region limited to about 2 μm. (**b**) Electric field distribution of the HFR pn-junction detector with a buried implanted $n^{(+)}$ layer ($^{31}P^+$, 27 MeV) determined for a reverse bias detector voltage of 30 V which represents different values of the depletion layer width w (115, 80, 9.8 μm) for implantation fluences of 1.0, 1.6, and 2.5×10^{11} cm^{-2}, respectively

using ion implantation of B^+ and P^+ ions at 50 keV with fluences of 5×10^{14} cm^{-2}, respectively. Measurements of the linearity behavior of the electron detectors were performed with electrons of 50 keV energy using different incident electron currents (beam spot area $A < 2$ μm^2). It was demonstrated that the linearity range extends with increasing implantation fluence and increasing detector bias. For the highest P^+ ion fluence of 3.7×10^{11} cm^{-2}, high e-beam currents up to 200 nA corresponding to a very high current density of 20 A cm^{-2} have been detected without significant charge carrier loss. If the linearity range is plotted versus the electric field strength, a linear correlation was obtained (Fig. 4.29).

This behavior agrees with the assumption that deviations from the linearity are caused by charge loss due to plasma related recombination, which is in first order inversely proportional to the electric field strength [138, 139].

4.2.2 Ion Implantation into Germanium

Although the first transistor was made of germanium (Ge), today most integrated circuits are fabricated using silicon substrates. The main reasons for the change from Ge to Si are the excellent physical properties of the SiO_2/Si interface which are crucial in CMOS technology. Today SiO_2 is increasingly replaced by high-k dielectrics. This fact and the advantage that the carrier mobility in Ge is higher than in Si (3,900 cm^2 V^{-1} s^{-1} compared to 1,450 cm^2 V^{-1} s^{-1} of Si) have led to a renewed interest in germanium as a candidate for future integrated devices, such as high mobility transistors [140] and high quality photodetectors [141]. For successful device applications of Ge, however, low resistivity, shallow, and low leakage germanium pn-junctions are required.

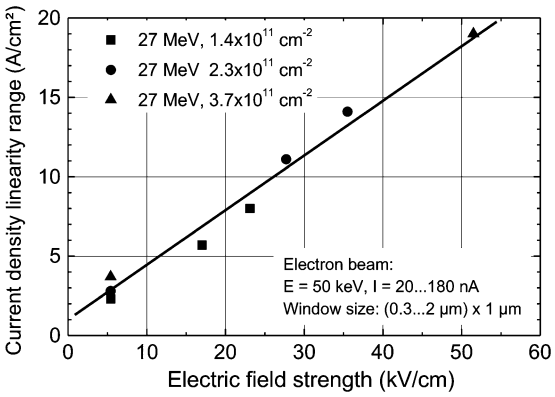

Fig. 4.29 Dependence of the linearity range of the electron detectors on the electric field strength in the HFR. *Different symbols* for the same implantation fluence represent different detector bias values

Recent investigations on the formation of ultra-shallow junctions by ion beam processing have shown that p^+-doping using B^+ ion implantation yields junctions that meet the requirements for the 22 nm technology node, whereas the formation of n^+p-junctions by P^+ or As^+ ion implantation is complicated by the high diffusivity, the low solubility of these dopants in germanium, and by low activation of these dopants and the difficulty in defect annihilation during subsequent annealing [142]. Ga^+-implanted ions as p-type dopants in Ge are another interesting alternative for shallow junctions because their higher atomic mass reduces both the ion straggling and the channeling of the as-implanted profile, as demonstrated for P^+ and As^+ ion implantation in Ge-MOSFET device fabrication [143]. Additionally, compared to boron Ga has a very high solubility in Ge of ~5×10^{20} cm^{-3}. However, Ga that seemed to be very attractive for p-type doping suffers from an important dose loss due to evaporation during annealing [142].

Because boron has a very low diffusivity in Ge the as-implanted profile defines the pn-junction depth. For example, as shown in Fig. 4.30 for 6 keV B^+ implantation into Ge at a fluence of 3×10^{15} cm^{-2} followed by RTA annealing up to a temperature of 400 and 600 °C for 60 s no movement of B takes place and the as-implanted and annealed profiles overlap [144].

Sheet resistance measurements showed that a higher activation level of 1×10^{19} cm^{-3} (dashed line in Fig. 4.30a) compared to the solid solubility of B into Ge of 6×10^{18} cm^{-3} (full line in Fig. 4.30a, b) was reached. Therefore, results for B^+ ion implantation for p-type junctions in Ge are promising. To reduce boron channeling (deeply extended tail of the boron profile into the bulk in Fig. 4.30a) an amorphization of Ge over a depth of ~100 nm can be performed by self-implantation of Ge^+ ions at 100 keV and a fluence of 1×10^{15} cm^{-2}. During annealing the amorphous layer re-crystallizes by solid phase epitaxial Ge regrowth with activation of B atoms onto substitutional sites. As shown in Fig. 4.30b, the

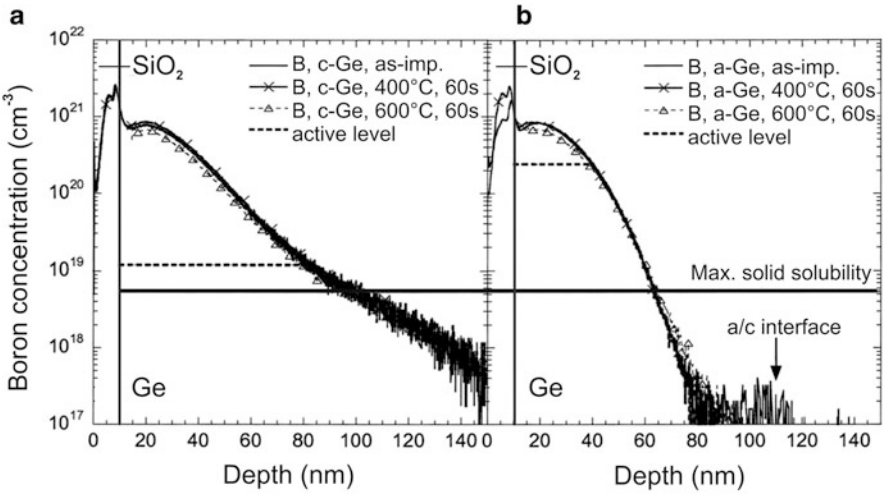

Fig. 4.30 6 keV B^+, 3×10^{15} cm^{-2} as-implanted, and annealed at 400 and 600 °C for 60 s, boron depth profiles in Ge measured by SIMS without (**a**) and with (**b**) preamorphization by a Ge implant of 100 keV Ge + ions to a fluence of 1×10^{15} cm^{-2} [144]

activation level reaches 2×10^{20} cm^{-3} (dashed line), which is two orders of magnitude above the equilibrium solid solubility (full line in Fig. 4.30a, b). However, at the maximum of the implanted profile the boron concentration reaches 1×10^{21} cm^{-3}. Evidently, an important part of the B atoms is not activated.

The application of Ga^+ ion implantation to the fabrication of p^+n-junctions in Ge was recently investigated to study the diffusion behavior of the implanted Ga at RTA annealing for 60 s in the temperature range of 300–700 °C with SiO_2 capping layers to prevent Ga outdiffusion during heat treatment [145]. The results suggest that Ga has nearly the same diffusion behavior as B in Ge. Implanting Ga^+ ions (40 and 80 keV, 3×10^{15} cm^{-2}) into crystalline Ge, no diffusion was observed after the RTA annealing at 300–700 °C. For annealing 60 s at 550 °C, an electrical activation level of 4.4×10^{20} cm^{-3} was achieved which is close to the Ga solubility in Ge. Ge preamorphization followed by SPER did not yield a higher activation level, although ion channeling was suppressed. Additionally, an increased Ga diffusivity in the amorphous phase was observed at temperatures >400 °C. The high activation level and the absence of diffusion make Ga^+ ion implantation in c-Ge to form p^+n-junctions very promising for implementation in a Ge technology.

The formation of n^+-doped junctions by P^+ ion implanation is more critical as phosphorous and does not show a high level of active concentration. Maximum concentrations of $(5–6) \times 10^{19}$ cm^{-3} have been reached, which are below its equilibrium solid solubility of 2×10^{20} cm^{-3} [146]. It has been assumed that most of the P atoms are not in an electrically active configuration and are possibly paired with point defects such as vacancies. At phosphorous concentrations above $(2 - 3) \times 10^{19}$ cm^{-3}, the diffusion coefficient in Ge is dopant concentration dependent leading to a box-like profile during annealing (Fig. 4.31) [147].

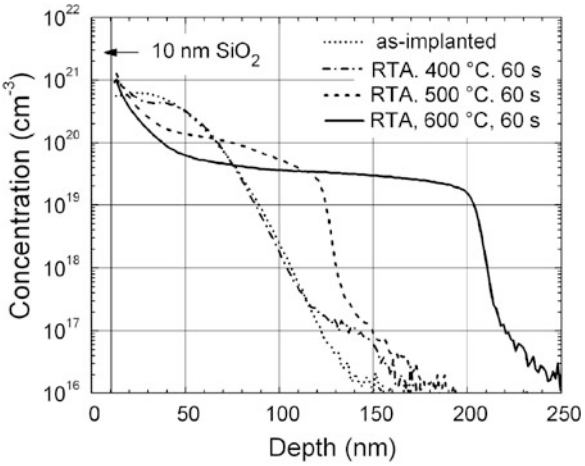

Fig. 4.31 Phosphorous profiles after 60 s RTA at 400 °C (*dashed/dotted line*), 500 °C (*dashed line*), and 600 °C (*thick line*). The as-implanted profiles are shown for comparison (*dotted line*). Before annealing the thickness of the amorphous layer was 150 nm. The P profiles were measured by SIMS

Prior to ion implantation of the profiles in Fig. 4.31, the samples were capped with 10 nm SiO_2 by sputter deposition. Preamorphization implantation (PAI) was performed by Ge^+ ions at energies of 150 keV and at a fluence of 1×10^{15} cm^{-2}. Phosphorous was implanted at 30 keV and 3×10^{15} cm^{-2} and rapid thermal annealing (RTA) of the samples was performed at 400, 500, and 600 °C for 60 s. Recently, for suppression of phosphorous diffusion and achievement of a high activation degree at the same time, FLA in the ms range instead of RTA has been applied [148]. Shallow n^+ layers in Ge were formed by P^+ ion implantation (30 keV, 3×10^{15} cm^{-2}) and subsequent millisecond (3 and 20 ms) flash-lamp annealing. In contrast to conventional RTA annealing, a high activation up to 6.5×10^{19} cm^{-3} is achieved without any dopant redistribution and noticeable phosphorous diffusion. Furthermore it was shown that the optimum of FLA treatment should not strongly depend on the pretreatment by preamorphization implantation (PAI), preannealing by RTA, and the solid phase epitaxial recrystallization (SPER) of amorphous layers. The results suggest that independently of pretreatment the maximum activation should be obtained at a flash energy that corresponds to the onset of P diffusion. To obtain a high electrical activation, the thermal annealing needs to be carefully designed so that phosphorous can be effectively activated before diffusion. Optimized RTA or FLA annealing process can yield a maximum active P concentration of $\sim 1 \times 10^{20}$ cm^{-3}, which is its solid solubility limit. Usual RTA temperatures for Ge, about 400–600 °C, are used for less than 60 s.

In general annealing behavior for high fluence-implanted phosphorous, doping levels can be quite complicated due to outdiffusion of phosphorous (losses to gas phase or capping SiO_2 layer), indiffusion deeper into the sample, and precipitation

of P-containing clusters at locations of peak concentration [149]. These undesirable effects can be avoided if P^+ ions are implanted to concentrations at the peak activation level of $\leq 5 \times 10^{19}$ cm^{-3} [143].

Compared to other n-type dopants phosphorous is preferred for the implantation of highly doped n^+p-junctions. This is related to the fact that high fluence implantation above 5×10^{14} cm^{-2} of the heavier dopant ions (As, Sb, Bi) and also Ge for preamorphization creates serious roughening of the surface, near-surface void formation, or even porous surface layers [150]. The formation of voids and clusters of voids has been observed in Ge during ion implantation of heavy ions such as Ga, Ge, As, In, and Sb into Ge at ion energies $\geq$30 keV and fluences above ~1×10^{15} cm^{-2}. A complete surface coverage with cluster voids and pronounced porous layers often appears at higher fluences of $\geq 1.0 \times 10^{16}$ cm^{-2} [150, 151]. The morphology of the near-surface damage strongly depends on ion mass. For example, in the case of Ga^+ and As^+ ion implantation the induced surface roughness is purely a surface related effect which can be prevented by adding a 10–30 nm SiO_2 capping layer prior implantation. In the case of In^+, Sb^+, and heavier ion (e.g., Bi^+), implantation subsurface void formation by the clustering of vacancies takes places. This subsurface void formation appears abruptly at fluences between 5×10^{14} and 10^{15} cm^{-2} and cannot be removed during subsequent thermal treatment. The initial void and porous structure formation is discussed in the literature in terms of very effective vacancy clustering [152–156] and "microexplosion" theories [157–159]. Nevertheless, results of extended investigations indicate that neither the vacancy clustering nor microexplosion theory can solely explain void formation [151]. In summary, surface roughening, near-surface void, and porous layers formation in germanium suggest that ion implantation conditions must be chosen carefully in Ge-based device processing with common p- and n-type dopants (Ga^+, In and As^+, Sb^+, respectively) and with Ge^+ ions for preamorphization. Ion fluences above 5×10^{14} cm^{-2} could result in void and porous layer formation which cannot be removed via annealing.

Among the increasing use in microelectronic technology, Ge with high doping by ion implantation recently becomes interesting in research and development of new Ge-based superconducting and spintronic devices [160, 161].

4.2.3 Ion Implantation into Compound Semiconductors

In comparison with group IV semiconductors (Si, Ge) ion implantation into *III–V semiconductors* exhibits some peculiarities which are connected with the physical properties of these compound materials. Nevertheless, ion implantation is extensively used to fabricate n-, p-doped layers in III–V compounds because no reliable diffusion technology exists due to the low evaporation temperature (already above 500 °C) of the group V species (As, P). Furthermore, the annealing for damage removal and dopant activation is more complicated compared to Si and Ge (different temperature regions for recrystallization, annealing of defects, and electrical activation of implanted dopants [162–164]). It has been shown that it is much more

difficult to obtain high degree of dopant activation in GaAs compared with Si, that the achieved activation levels and mobility values of the carriers in some cases are lower than the theoretically expected ones. Usually, the highest activation is obtained if amorphization of the crystalline material is prevented and the best electrical device performances are obtained using rapid thermal annealing (RTA) in combination with suitable capping layers. RTA is chosen in the temperature range 500–900 °C for some seconds. As mentioned, the surface of III–V wafers has to be protected from thermal decomposition during annealing which is achieved by dielectric layer deposition (e.g., of SiO_2, S_3N_4, or Al_2O_3, etc.) and/or by same wafer material proximity or the maintenance of group V over pressure in the annealing ambient [165–167].

Ion implantation processes in III–V compound semiconductor technology were developed for shallow n-type, shallow p-type doping, and for material compensation by deep level impurities in most commonly used GaAs, $Al_xGa_{1-x}As$, InP, $In_{0.53}Ga_{0.47}As$, $In_{0.48}Al_{0.52}As$, and InSb [168]. The most preferred implanted ion is Si^+ to obtain n-type doping because of its easy activation at relatively low temperatures and its low diffusivity (e.g., $D_{Si} \approx 10^{-14}$ cm^2 s^{-1} in GaAs). Other possible ions for n-type doping are S^+, Se^+, Te^+, Sn^+, and Ge^+, but they do not meet demands on low diffusivity and thermal stability (S), low crystal damage (Se, Te, and Sn), and high activation (Ge) [169]. For Si^+ ion implantation, for example, into the source and drain regions of GaAS-MOSFETS fluences of ~(1–5) $\times$ 10^{14} cm^{-2} at ion energies $\leq$200 keV are used. Implanted silicon is usually activated by rapid thermal annealing at 850–1,000 °C (800–875 °C) and l–10 s for GaAs (InP, InGaAs), respectively. At relatively poor activation of Si the maximum electron concentration one can achieve in GaAs is limited to (2–3) $\times$ 10^{18} cm^{-3}, whereas in the case of InP an activation of 80–100 % has been obtained and the electron peak concentration reaches ~10^{19} cm^{-3} [170]. At increased high Si^+ fluences, to avoid amorphization and to obtain higher Si activation, the implantation can be performed at elevated target temperatures of ~200 °C. But also in this case the maximum electron concentration is limited to $\approx 10^{19}$ cm^{-3}. Another attempt to obtain high electron concentrations is the co-implantation of Si^+ and S^+ ions. Both Si and S are donor impurities in III–V compounds occupying group III and V lattice positions, respectively. Using Si^+ and S^+ co-implantation, a maximum electron concentration of 3 $\times$ 10^{18} cm^{-3} in GaAs and 2 $\times$ 10^{19} cm^{-3} in InP have been obtained. A high Si activation giving an electron concentration of $\approx$ 10^{19} cm^{-3} was observed in $In_{0.43}Ga_{0.57}As$ too [166].

For p-type doping of III–V semiconductors, the most preferred implanted ion is Be^+ with low ion mass (low crystal damage), but also other ions, such as Zn^+, Mg^+, and Cd^+, are often used. The p-doping by these ions is more problematic compared to n-doping due to their relatively high diffusivity during annealing [165, 167, 171].

In contrast to n-dopants (Si^+, S^+, Se^+, Te^+, Sn^+ ions), for p-type dopants (Be^+, Mg^+, Cd^+, Zn^+ ions) implanted into GaAs, an activation close to 100 % can be obtained for peak concentrations up to $\approx$2 $\times$ 10^{19} cm^{-3} [172]. It is interesting to note that, in Ga-based III–V compounds the maximum achievable electron concentration by donor implantation doping is limited to values of $<$4 $\times$ 10^{18} cm^{-3},

whereas hole concentrations $>10^{19}$ cm^{-3} can be easily achieved by acceptor doping. In indium-based III–V compounds there is the opposite situation. Implantation of nearly all ion species of group II, IV, VI, and inert gases into GaAs and other III–V compound semiconductors have been reported in the literature.

High energy (MeV) ion implantation is extensively used in III–V compound semiconductor technology (GaAs, InP) to obtain buried doped layers (Si^+ implantation), deep material compensation (high resistivity layers), and selective area device isolation implants (O^+ implantation) [170, 173, 174]. MeV O^+ ion implantation is used in order to isolate thick multilayer device structures, for example in heterojunction bipolar transistors and a variety of semiconductor lasers. As reported in [173] the formation of high resistivity layers in highly doped n- and p-type epitaxial GaAs (and InP) layers has been achieved in the fluence range of 5×10^{13}–5×10^{15} cm^{-2} by 25–50 MeV O^+ ion implantation with projected ranges of these ions of 14.0 and 28.8 μm in GaAs, respectively. The sheet resistance of thin (0.5 μm) epitaxial surface device layers exposed to such ions increases roughly by two orders of magnitude with fluence in the range 10^{13}–10^{15} cm^{-2} but, depending on the initial doping concentration, may decrease slightly again at higher O^+ fluences. For the fabrication of buried, highly doped, layers in GaAs, an InP high energy (30–70 MeV) Si^+ ion implantation at ion fluences of 5×10^{14} cm^{-2} has been also investigated [173]. From sheet resistance measurements it was concluded that the electrical activation of implanted Si in GaAs and InP slightly increases by ~50 % with increasing ion energy from $\leq$200 keV to high energies of 10–100 MeV for conventional Si^+ implantation and high energy implantation, respectively. Possible applications for high energy ion implantation are the fabrication of thick (>4 μm) multilayer photonic devices such as quantum infrared detectors and III–V semiconductor lasers which contain several different III–V materials and in which low energy ions are insufficient to penetrate the active layer structure.

Among oxygen ion implantation, the compensation of III–V compound semiconductors (radiation damage, local introduction of compensating deep or mid-gap levels) has been achieved also by implantation of other chemically inactive ion species such as H^+, He^+, Ne^+, N^+, etc. [168] or by implanting chemically active substitutional impurities like transition metal ions (Fe^+, Co^+, Ti^+, etc.). To create deep compensation levels, implanted transition metal ions have to be driven into the substitutional sites by annealing the material at (750–900) °C, whereas at light gas ion bombardment the implantation damage itself provides these levels. Compensation by light ion bombardment has a poor thermal stability at temperatures above 500 °C, whereas substitutional compensation by transition metal ion implantation is thermally stable enabling further processing of the material at high temperatures.

With improving crystal quality of the *group III-nitride materials (GaN, AlN, InN)* ion implantation becomes an emerging doping technique in exploring new dopant species and device structures. The reasons for recent intense research are possibilities in fabrication of high brightness light emitting diodes as well as in fabrication of electronic devices that operate at high power or high temperature [175]. Already heterostructure field effect transistors, junction field effect transistors, and heterojunction bipolar transistors have been demonstrated. For

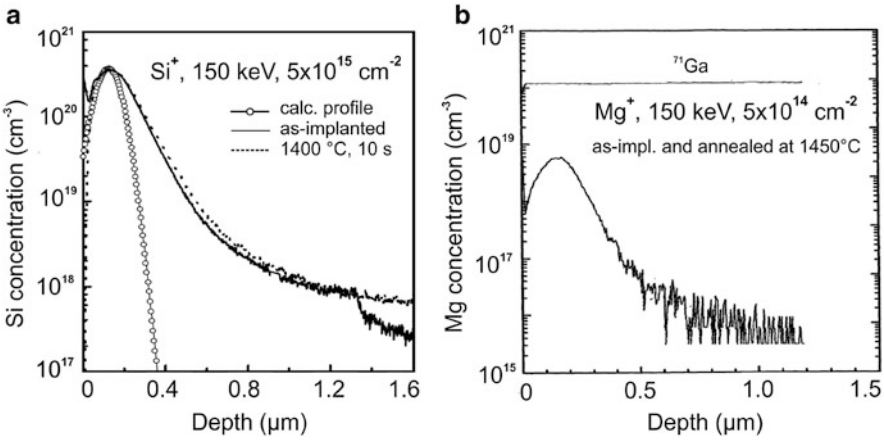

Fig. 4.32 Depth profiles of Si^+- (**a**) and Mg^+-(**b**) implanted GaN before and after annealing at 1,400 and 1450 °C, respectively (the profiles practically coincide) [177, 178]

III-nitride ion implantation is used for improvement of device luminescence, material doping, and local compensation in these materials [176]. Common dopant ions for S/D formation in III-nitride FETs are Si^+, S^+, Te^+, Be^+, Mg^+, C^+, Ca^+, and Zn^+, where for n-type doping mostly Si^+ but also S^+, Te^+ ions (energy 100–600 keV, fluence 5×10^{14}–5×10^{14} cm^{-2}) and for p-type doping Be^+, Mg^+, C^+, and Ca^+ ions (50–150 keV, (3–5) $\times 10^{14}$ cm^{-2}) often with co-implantation of P^+ ions have been used. Channel implantation in III-nitride FETs is carried out at lower fluences in the range of 10^{13}–10^{14} cm^{-2}. For the annealing of crystal damage in GaN and activation of implanted impurities usually higher temperatures of $\geq$1,000 °C are necessary. Both conventional furnace annealing and rapid thermal annealing (RTA) have been tried, using annealing temperatures up to 1,200–1,500 °C. At such high temperatures, annealing of GaN is complicated due to material decomposition (loss of nitrogen from the GaN surface), which becomes pronounced for prolonged annealing times already at temperatures of above 800 °C. Therefore, GaN surfaces have to be protected during annealing by appropriate capping layers (e.g., AlN) or the annealing must be carried out under high pressure N_2 ambient. For example, it was shown that for Si^+-implanted and AlN-capped GaN a high activation with almost 100 % of Si on Ga sites can be achieved at 1,100 °C, 15 s RTA annealing.

Most of the common acceptor and donor ions implanted into GaN show a very low diffusivity at high temperatures [177], as shown, for example, for Si as a n-type dopant in Fig. 4.32a and for Mg as a p-type dopant in Fig. 4.32b.

This behavior is important for the fabrication of GaN-based power devices such as thyristors and insulated gate bipolar transistors that will require creation of doped well or source/drain regions by implantation. The low diffusivities of implanted dopants in GaN allow a quite precise control of the junction and there will be fewer problems with lateral diffusion of the source/drain regions towards the gate. A comprehensive overview of ion implantation into GaN and related phenomena is given in [179].

O^+ ion implantation into GaN has been investigated with respect to selective area isolation between device structures. For this purpose multienergy O^+ ion implantation with different fluences has been applied, e.g., 50 keV, 1×10^{14} cm^{-2}; 100 keV, 2×10^{14} cm^{-2}; 200 keV, 3×10^{14} cm^{-2}, resulting in a total fluence of 6×10^{14} cm^{-2}. At these implantation conditions the sheet resistance of the as-grown GaN was increased approximately by six orders of magnitude up to 10^9–10^{10} Ω sq^{-1} [180]. Selective area isolation in GaN can be achieved also by implantation of n- and p-type GaN with Ti^+, Fe^+, or Cr^+ ions forming deep defect levels and insulating layers with maximum sheet resistances of ~10^{12} Ω sq^{-1} in n-type and ~10^{10} Ω sq^{-1} in p-type GaN.

The *wide bandgap compound semiconductor SiC* is the favored material for high-temperature, high-power, and high-frequency device applications [181]. In the last years, intensive research has been performed on n-type doping of SiC by N^+, P^+, S^+, and Sb^+ and on p-type doping of SiC by Al^+, B^+, and Ga^+ ion implantation which is reviewed, for example, in [182]. Whereas N^+ implantation has been mostly applied in order to produce low resistivity, n-type SiC regions, the development of efficient processes for p-type doping is still a challenging task. High fluence Al^+ implantation seems to be the most promising procedure to fabricate low resistivity, p-type regions in SiC and, therefore, many studies have been performed in this field in order to find out the optimum conditions for the implantation and the subsequent damage annealing. Compared to silicon processes, ion implantation into SiC requires much higher temperatures at subsequent annealing (~1,200–1,800 °C) to achieve acceptable electrical activation of donor or acceptor ions. Annealing of implanted SiC needs to be performed in high-purity inert gas ambient such as argon. High-temperature annealing in nitrogen ambient produces thin nitride layers on the surface of SiC. One of the issues related to ion implantation is to achieve doping levels of ~10^{19} cm^{-3} in order to get ohmic contacts with specific contact resistance below 10^{-5} Ω cm [183]. Another issue is the need of high energy (MeV) ion implantation to form deep p^+n-junctions. Since introduction of dopants by thermal diffusion is not possible in SiC, MeV ion implantation of acceptor ions (Al^+, B^+, Ga^+) is necessary to create p-wells for CMOS field-effect transistors and other devices that require deep p-type regions [184]. Most of these ion beam processes are based on carrying out implantation at elevated temperatures (~500–800 °C) using patterned high-temperature masking materials (e.g., SiO_2, Si_3N_4). The target temperature during implantation promotes some self-annealing during the implantation, so that damage and segregation of displaced Si and C atoms do not become excessive, especially at high fluence implantation employed for ohmic contact formation. Protecting the SiC wafer surface during implantation annealing is very important. Annealing performed without SiC surface protection results in surface roughening due to the sublimation and re-deposition of Si species such as Si, Si_2C, SiC_2, etc. on the crystal surfaces. The Si sublimation results in SiC surface material and implanted impurity loss during annealing [185]. For high-temperature annealing above 1,400 °C, capping layers of SiO_2 and Si_3N_4 are not applicable due to their volatility at these high temperatures required for annealing implanted SiC. AlN encapsulation has proved useful in protecting the SiC sample surface

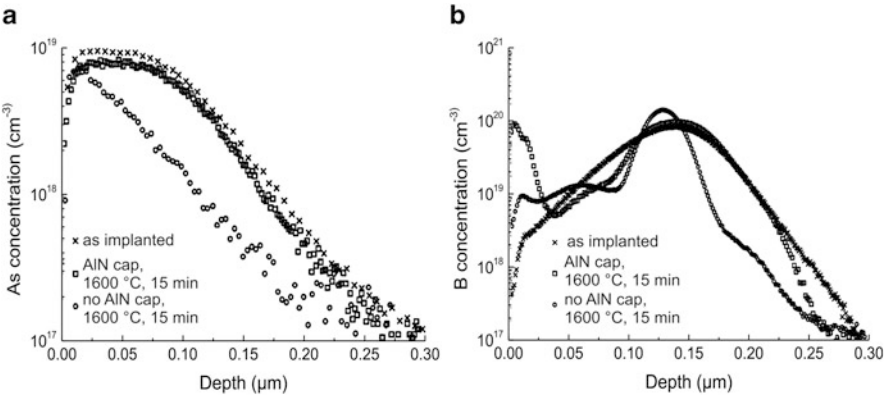

Fig. 4.33 SIMS depth profiles for (**a**) As^+-, and (**b**) B^+-implanted SiC before and after annealing with and without AlN encapsulant [186]

during postimplantation annealing up to 1,650 °C for 10 min [186]. The importance of this capping layer at high-temperature annealing of SiC is demonstrated in Fig. 4.33 where, for example, the depth profiles of As^+- and B^+-implanted SiC after annealing with and without an AlN capping layer are shown.

The As profiles in Fig. 4.33a were achieved after a multiple As^+ implantation (20, 40, 80, 140, and 220 keV) with a total ion fluence of 1.2×10^{14} cm^{-2} at 800 °C target temperature. For the B-profiles in Fig. 4.33b, the implantation conditions were 50 keV, 8.8×10^{14} cm^{-2} at an implantation temperature of 700 °C.

It was demonstrated that N, P, and Al dopants are thermally stable in SiC during postimplant annealing, with or without encapsulation. In the case of shallow As^+ and Sb^+ implantations, when the annealing was performed at 1,600–1,650 °C without capping layer, more than 50 % of the implanted ions are lost due to sublimation related surface damage, but these implantation profiles remained thermally stable when annealed with an AlN capping layer. The AlN capping layer could not prevent the out-diffusion of B near the SiC surface over a depth of ~(50–100) nm (see Fig. 4.33b) and the redistribution of the B profile. It is assumed that the redistribution is associated with the implantation-induced defects and not with the defects created at the surface during annealing. Nevertheless, in the case of a multiple energy B^+ implantation over a depth of 0.7 μm the uniform B concentration profile remained stable everywhere except at the surface [184].

Among conventional furnace and RTA annealing, FLA was used for crystal recovery and activation of high fluence Al-implanted SiC wafers [187]. In comparison with furnace and RTA, the free hole concentration can be remarkably increased to higher acceptor atom concentrations ($N_A \geq 10^{20}$ cm^{-3}). Aluminum was implanted into n-type SiC epitaxial layers at 400 °C with four different energies and fluences in order to obtain a box-shaped (500 nm thick) profile with plateau concentrations of Al up to 1.5×10^{21} cm^{-3}. The samples were annealed in Ar

ambient by FLA at maximum sample temperatures during the flash (duration 20 ms) of about 2,000 °C. As demonstrated, FLA is a promising annealing technique for the formation of very high doped p^+(Al)-layers in SiC-based electronic devices because of the higher hole concentrations and lower resistivity as well as the weak temperature dependence of the electrical material parameters for Al concentrations $\geq 5 \times 10^{20}$ cm^{-3}.

4.3 Ion Beam Synthesis of New Phases in Solids

Except the application of ion implantation in microelectronic device and integrated circuit technologies ion beams became a valuable and innovative tool for processing, for example, of advanced materials with novel electrical, optical, and magnetic properties. At conventional low and medium fluence ($<10^{16}$ ions/cm^2) ion implantation in microelectronics, the concentration of introduced dopants is usually below their solubility limit in semiconductor materials. At certain annealing temperatures the impurity atoms are solved in Si and located on crystal lattice sites or, as a small part, remain as soluted interstitial atoms. If the concentration of impurity atoms introduced by high fluence implantation ($\geq 10^{16}$ cm^{-2}) exceeds the solubility limit, ion implantation leads to a far-from-equilibrium state (supersaturated solid) which relaxes towards thermodynamic equilibrium during subsequent annealing by phase separation through precipitation and ripening (Ostwald ripening) of nanoclusters (NC) [188].

Phenomenologically, ion beam synthesis (IBS) can be divided into several stages, schematically shown in Fig. 4.34:

Accumulation and supersaturation. After ions have been slowed down by electronic and nuclear stopping, they are incorporated into the target material. Thermal activation at common implantation temperatures is usually too low to allow impurity diffusion over larger length. The impurity distribution remains frozen in, especially at low impurity concentrations.

Nucleation or early phase separation. Upon annealing, thermal fluctuations could initiate phase separation through the (homogeneous) nucleation of precipitates. The necessary energy barrier can either be reduced by heterogeneities (defects) in the substrate giving rise to inhomogeneous nucleation or by considerably higher supersaturations.

Growth. Second phase precipitates formed by nucleation grow as long as the local monomer concentration is above the equilibrium concentration of these precipitates. All precipitates grow on the expense of the reservoir of dissolved impurity atoms.

Coarsening and Ostwald ripening. The monomer concentration decreases during further annealing and a competitive coarsening process called Ostwald ripening takes place. Large NCs grow on the expense of smaller one, which finally dissolve.

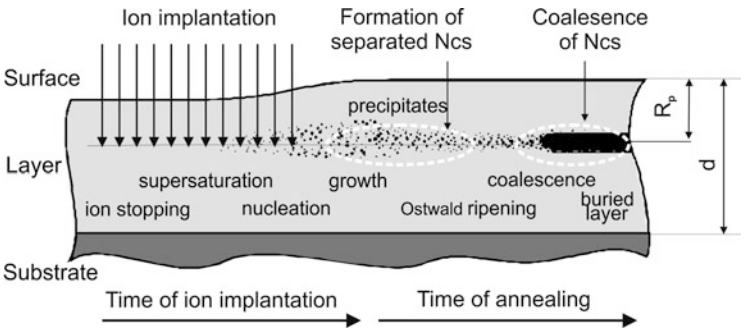

Fig. 4.34 Scheme of major stages at ion beam synthesis (IBS) of new phases. NCs nucleate and grow during ion implantation or, for impurity atoms immobile during implantation, during subsequent thermal treatment. The mean NC size as well as their spatial and size distribution changes during Ostwald ripening. At very high fluences, buried compound layers can form by coalescence of NCs

Coalescence and percolation. During NC growth, neighboring NCs might touch each other and coalesce to a larger one. This process is more likely for very high ion-fluence implantations aimed at the formation of buried continuous layers.

According to the classical nucleation theory (CNT) the initial supersaturation of impurity atoms dispensed in a matrix is metastable and thermal fluctuations may lead to the precipitation of second-phase nanocrystals. In general, the nucleation rate I can be written as $I = A{\cdot}\exp(-W/kT)$, where W is the thermodynamic nucleation barrier and A a dynamical factor increasing with impurity concentration. This case is referred to as homogeneous nucleation. In contrast, the so-called inhomogeneous nucleation is triggered by system inhomogeneities, such as defects, grain boundaries, interfaces, or impurities. The inhomogeneous reaction rate $I_i = A_i{\cdot}\exp(-W_i/kT)$ can be much higher than the homogeneous one, since mostly, due to an effectively lower interface energy contribution to the nucleation barrier, $W > W_i$. According to classical nucleation theory, the energy barrier for homogeneous nucleation decreases with increasing supersaturation and the nucleation rate increases with the concentration of dissolved impurity atoms and (exponentially) with temperature. The single second-phase precipitates nucleated from an initial supersaturation interact with the initial phase by monomer exchange. Thereby, the equilibrium concentration of monomers near the phase boundaries is reached if the attachment and detachment rates are equal, which is also a function of the local curvature of the phase boundary. For spherical precipitates, this relation is given for the diffusion controlled case by the Gibbs–Thomson (GT) relation formula [189]:

$$c^{\mathrm{GT}}(R) = c_\infty \cdot e^{\left(\frac{R_c}{R}\right)}, \quad R_c = \frac{2 \cdot \sigma \cdot V_a}{k \cdot T}, \tag{4.8}$$

where c_∞ denotes the impurity equilibrium concentration at a flat phase boundary (i.e., the solidus concentration), and R_c the capillary length given by the material

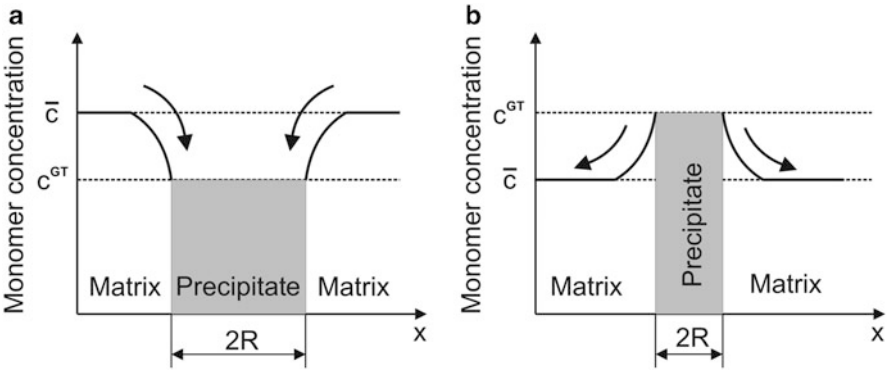

Fig. 4.35 Concentration profile of dissolved monomers near a precipitate. Depending on the average monomer concentration the cluster grows at $\bar{c}>c^{GT}$ (**a**) or shrinks at $\bar{c}<c^{GT}$ (**b**)

parameters surface tension σ and atomic volume V_a. The precipitate will grow if the average surrounding concentration $\bar{c}$ is higher than c^{GT}, the cluster acts as a sink for the diffusing monomers leading to cluster growth. On the opposite, for a lower average concentration $\bar{c}$ of surrounding monomers compared to c^{GT} the cluster emits monomers and therefore acts as a source and will shrink, as shown in Fig. 4.35.

In an early growth stage after nucleation all clusters will feeded from the reservoir of dissolved monomers. At that stage the average monomer concentration is still large compared to the equilibrium concentration c^{GT} of the individual clusters. The clusters do not interact directly with each other and the total volume of the precipitated second phase increases in time at a constant rate. However, when supersaturation becomes insufficient to dominate the system evolution, the system tends to diminish its free energy via a decrease of the total interfacial area. This minimization occurs by diffusional mass transfer from smaller (dissolving) to larger (growing) precipitates, which results in an increasing average precipitate size but decreasing total surface area. This stage of phase transition is also known as Ostwald ripening [190] or coarsening. If the density of NC is high, it is possible that NC touch, and then rapidly minimize their energy by surface diffusion of adatoms, such that a larger spherical cluster emerges (coalescence). The theory of Ostwald ripening, developed by Lifshitz and Slyozov [191] and by Wagner [192], is known as LSW theory. A more recent theory including the case of ripening during ion-implantation can be found in [193–195]. The LSW theory predicts the time evolution of the particle size distribution $f(R, t)$ and yields in the asymptotic limit $t \to \infty$ the following temporal power laws:

$$\overline{R}(t) = k_R^D \cdot t^{1/3} \quad N(t) = k_R^D \cdot t^{-1} \quad \text{(coarsening regime)} \tag{4.9}$$

for the time evolution of the average particle radius $\overline{R}(t)$ and the particle density $N(t)$. If the evolution is instead interface controlled, the growth law reads as

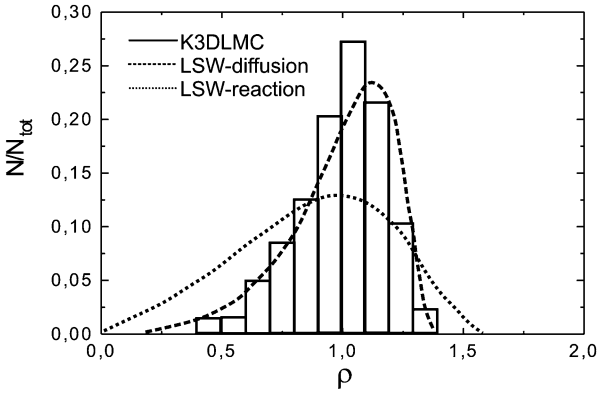

Fig. 4.36 Histogram of the nanoparticle radius distribution with $\rho = R/\overline{R}$ obtained by kinetic Monte Carlo simulation of second-phase precipitation. Both stationary distributions of the LSW theory are included [195]

$$\overline{R}(t) = k_{\mathrm{R}}^{\mathrm{D}} \cdot t^{1/2} \quad N(t) = k_{\mathrm{R}}^{\mathrm{D}} \cdot t^{-3/2} \quad \text{(diffusion limited growth regime)}. \quad (4.10)$$

The corresponding rate constants $k_{\mathrm{R}}^{\mathrm{D}}$ can be found in [191, 192] and have been reexamined for the more realistic case of nonzero solubilities and nonideal solution [196, 197]. The LSW theory further predicts that the particle size distribution $f(R, t)$ is time invariant (for $t \to \infty$) under the scaling of the average particle size $\overline{R}$.

For the modeling of ion beam synthesis, atomistic approaches such as the kinetic 3D lattice Monte Carlo (K3DMC) method were developed by Heinig et al. (see [195] and references therein) which allow to study the evolution of a given distribution of impurity atoms in a neutral matrix also for a time-dependent concentration of impurity atoms. An example of Monte Carlo simulations for studying the NC formation and determining the nanoparticle size distribution is shown in Fig. 4.36.

As can be seen in Fig. 4.36 the nanoparticle size distribution is in reasonable accordance with the stationary form (LSW) of the particle radius distribution of diffusion-limited Ostwald ripening (OR), but it is on the average somewhat smaller and seems to be more symmetric.

In the above description effects of interfaces, surfaces, spacial gradients of supersaturation, and the finite size of the supersaturation region were neglected although they have a significant influence on the evolution of spatial and size distribution of nanoparticles. So, the effect of sharp gradients in the initial concentration of impurity atoms has been discussed by Reiss et al. [193] for ion beam synthesis of buried SiO_2 structures (see Sect. 4.3.1).

The division of IBS in all these stages is to some degree artificial. The borders between the individual steps are rather ill-defined and depend on the specific implantation and annealing parameters. Tailoring of the size and size distribution of NCs could be achieved by a control of implantation parameters (ion energy, flux

and fluence, sample temperature) and annealing parameters (temperature, time, ambient conditions, etc.). Phase separation of ion-implanted, immiscible impurity atoms from the surrounding matrix, i.e., the formation of NCs, can also occur during the implantation process if the impurity atoms are sufficiently mobile due to collisional ion mixing; otherwise a subsequent annealing is always necessary.

Phase separated precipitates or NCs can lead to significant modification of the electrical, mechanical, magnetic, and optical properties of the host material. Formation of nanoclusters by ion beam synthesis (IBS) has been documented for a large variety of ion species and host materials. The examples include metal NPs [198] and semiconductor NCs in inert hosts [199], compound NCs formed as a result of chemical reaction between the implanted and substrate atoms, e.g., silicide formation for metal implantation into Si [200], metal alloys [201], and compound semiconductors formed by co-implantation or sequential implantation of various atom types, e.g., II–VI, III–V, or IV–IV semiconductor NCs in SiO_2 [202], Al_2O_3 [203], or Si [204]. In the following chapters, selected examples of ion beam synthesis with technological relevance, namely IBS of insulating and silicide layers buried in silicon as well as ion beam synthesis of semiconducting nanocrystals in insulators will be described.

4.3.1 Buried Insulating Layers in Silicon

An example for high fluence ion implantation into silicon where the concentration of implanted ions exceed the solid solubility limit is the O^+ ion implantation leading to highly oxygen supersaturated silicon. During subsequent high-temperature annealing, this state relaxes to thermodynamic equilibrium through phase separation into SiO_2 and Si, SiO_2 precipitation, Ostwald ripening of SiO_2 precipitates, and their coalescence to a continuous buried SiO_2 layer. This technique of ion beam synthesis was called *S*eparation by *IM*planted *OX*ygen (SIMOX) [205, 206] and is today well established in microelectronic device fabrication to produce thin silicon layers of high crystalline quality with an abrupt interface to a stoichiometric buried SiO_2 layer [207]. Similar IBS techniques were developed with high fluence nitrogen implantation (*S*eparation by *IM*planted *NI*trogen—SIMNI) [208, 209] and separation by high fluence implantation of both oxygen and nitrogen (SIMON) [210].

In the frame of the SIMOX technology, the buried oxide (BOX) is synthesized by internal oxidation following the deep implantation of O^+ ions at high fluences of 1.8×10^{18} cm^{-2} into the crystalline Si substrate at elevated temperatures (~500 °C) (Fig. 4.37). Annealing at high temperature (~1,300 °C, for some hours) is necessary to recover a suitable crystalline quality of the top Si film. High current implanters (100 mA, 180–200 keV) have been developed to produce 200 mm wafers with good thickness uniformity, low defect density (except threading dislocations with an areal density of 10^4–10^6 cm^{-2}), sharp Si–SiO_2 interfaces, and high charge carrier mobility in the top Si device layer.

As shown in Fig. 4.37, during high fluence O^+ implantation a Gaussian-like distribution in the depth of the substrate is created which in the annealing stage

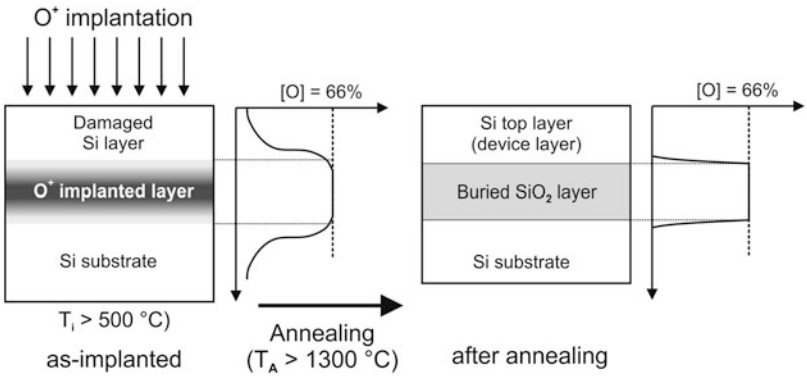

Fig. 4.37 SIMOX process for BOX formation at 0.4–1.8 × 10^{18} cm^{-2}, 100–200 keV, 1,320–1,350 °C, 6 h in Ar/O_2

redistributes into a rectangular shape and forms the desired buried layer. During ion implantation and the subsequent annealing, different steps of evolution merging into one another are run through. At the beginning an oxygen supersaturation in the Si substrate is created, followed by the nucleation of SiO_2 compound precipitates. Immediately after nucleation, the SiO_2 precipitates grow at the expense of the oxygen supersaturation. Later on, while annealing is in progress, the mean radius of SiO_2 precipitates increases due to Ostwald ripening which diminishes the interface energy. Finally, the SiO_2 precipitates become so large that they may overlap and coalesce towards a closed buried SiO_2 layer, thereby further diminishing the interface energy. Especially, the Ostwald ripening is recognized as the principal mechanism for the redistribution of the implanted profile [193]. The modeling approach for Ostwald ripening [188] for BOX layers gives consistent results using the experimentally confirmed initial condition of a band of homogeneously distributed precipitates.

The evolution of the oxygen depth profiles during high fluence oxygen implantation into silicon has been modeled by Maydell-Ondrusz and Wilson [211] and by Jäger [212–214]. The model takes into account the change of the ion range profile with changing target composition, the swelling of the target by the collected oxygen, and the surface sputtering. If the implanted oxygen exceeds the SiO_2 stoichiometry, initially at the profile maximum, the excess oxygen is assumed to diffuse readily to substoichiometric regions, i.e., towards surface and bulk, thereby oxidizing silicon in the interface region to SiO_2. In this way, the shape of the oxygen depth profile changes with the increasing fluence from Gaussian-like to flat topped profile as shown in Fig. 4.38.

The model describes the modification of the profiles by in situ "internal oxidation" during the implantation process. The microstructure of the top Si and buried SiO_2 layers as well as the redistribution of oxygen affected by postimplantation or in situ annealings are not taken into account. Nevertheless, the calculations reproduce fairly well the thickness and the depth position of the buried oxide layer, but

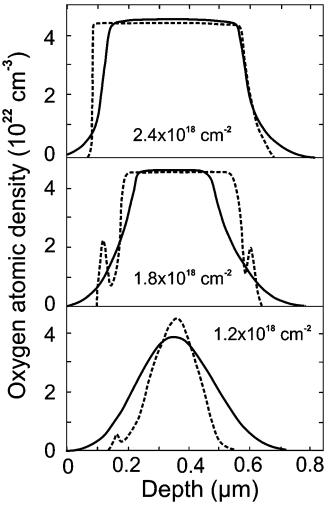

Fig. 4.38 Depth profiles of the oxygen concentration in samples implanted with 150 keV O^+ ions to various fluences. The theoretical results (*solid lines*) are given together with AES depth profiles (*dashed lines*). The experimental profiles have been measured in annealed samples and these data have been normalized by assuming a stoichiometric oxygen concentration for the plateaus [213]

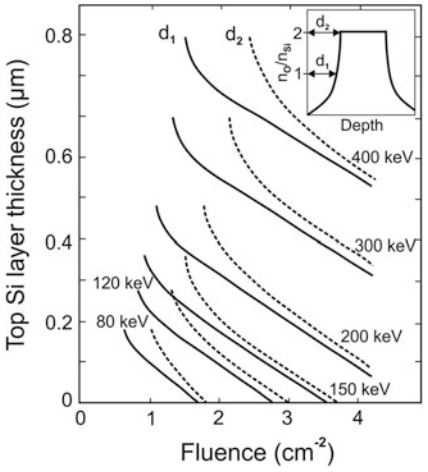

Fig. 4.39 Surface silicon device layer thicknesses versus implanted oxygen fluence for various implant energies [213]

allow only rough estimates of the width of the interphase region between the SiO_2 layer and the single-crystal surface layer in the SOI substrates. The results shown in Fig. 4.39 are considered to be of practical relevance. The thickness of the top silicon device layer is shown in dependence on the implanted O^+ fluence and for various ion energies, and is in good agreement with available experimental data. The two

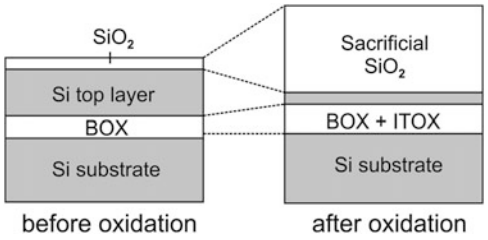

Fig. 4.40 Schematic representation of the ITOX process (low fluence SIMOX)

distances d_1 and d_2 given there indicate the width of the transition region to the BOX layer. If with increasing implanted fluence the oxygen depth profile becomes more and more rectangular, the two curves in Fig. 4.39 approach each other and have the same slope. The thickness of the BOX layer is not shown since it depends essentially only on fluence, but not on ion energy.

For considering the O^+ ion fluence required to reach an oxygen-to-silicon ratio of 2.0 in the sample (so-called the stoichiometric fluence) it was concluded that the stoichiometric fluence increases with increasing ion energy. At IBS of BOX layers as substrates for SOI wafers, the material should receive fluences which exceed the theoretical value given in [213]. Otherwise, no homogeneous SiO_2 layer (usually 200–400 nm thick) but a mixture of amorphous SiO_2 precipitates and Si nanocrystals may be obtained. For ion energies $E \geq 150$ keV the formation of the oxide layer starts at a depth coinciding with the projected range R_p of the O^+ ions in silicon. At these ion energies the effects of sputtering and changing ion range compensate that of target widening (swelling).

To improve the quality of the BOX layers in SIMOX wafers, high-temperature annealing in oxygen containing atmosphere for internal thermal oxidation (ITOX) has been applied. At these annealing conditions the ion fluence can be significantly reduced from 1.8×10^{18} cm^{-2} (for Si^+, 200 keV) to 4×10^{17} cm^{-2} (low fluence SIMOX) [215–217]. The ITOX process improves the stoichiometry of the BOX and slightly increases the overall thickness of the buried oxide, which is shown in Fig. 4.40.

The lower oxygen fluences are needed for large SIMOX wafers with ultrathin silicon device layers and BOX layers for ultra-large-scale integrated (ULSI) CMOS circuits and implies a considerable gain in IBS processing time and wafer cost. The material properties for standard SIMOX and low fluence SIMOX wafers together with the corresponding process parameters of ion beam synthesis are summarized in Table 4.3.

The flexibility of ion beam processing allows also the fabrication of double SIMOX structures with a Si device top layer and a Si layer sandwiched between the two buried oxides which, for example, can serve for interconnects, wave guiding, additional gates, or electric shielding. Furthermore, if the O^+ ion implantation is carried out through a patterned masking layer (e.g., patterned SiO_2), laterally isolated single-transistor islands and interrupted BOX layers as SOI regions

Table 4.3 SIMOX wafer material properties and process parameters

Wafer parameter	Standard SIMOX	LF-SIMOX (ITOX)
Wafer diameter	≤200 mm	≤300 mm
Si device layer thickness	210 nm	20–145 nm
Si device layer thickness uniformity	±0 nm	±2 nm
BOX layer thickness	375 nm	135, 145 nm
BOX layer thickness uniformity	±10 nm	±5 nm
Surface roughness	0.7 nm	<0.15 nm
Dislocation density	$<10^3$ cm^{-2}	$<10^3$ cm^{-2}
BOX pipe (pinhole) areal density	<0.1 cm^{-2}	<0.1 cm^{-2}
BOX dielectric electric field breakdown	$>5 \times 10^6$ V cm^{-2}	$>7 \times 10^6$ V cm^{-2}
IBS process parameters	Standard SIMOX	LF-SIMOX (ITOX)
O^+ ion energy	150–200 keV	≤100 keV
O^+ ion fluence	1.8×10^{18} cm^{-2}	4×10^{17} cm^{-2}
Implantation temperature	~500 °C	~500 °C
Annealing process	1,320–1,350 °C (Ar)	1,320–1,350 °C (Ar/O_2)

integrated into a bulk Si wafer can be fabricated [218]. The advantages of ion beam synthesis of buried SiO_2 layers compared to other SIO techniques are that SIMOX is compatible with silicon device processes (ion implantation and thermal annealing). On the other hand, as a disadvantage high fluence implantation up to ~2×10^{18} cm^{-2} and high-temperature annealing up to ~1,350 °C require special implantation and annealing equipment demanding attention to impurity contamination during both processes. Compared to crystalline Si bulk material remaining crystal defects (e.g., threading dislocations) and SiO_2 precipitates in the top Si layer as well as pin holes, trapped charges, and Si precipitates in the BOX layer can influence the electrical properties of devices fabricated in SIMOX wafers.

4.3.2 Ion Beam-Synthesized Silicide Layers

Using high fluence ion implantation, this problem can be solved and buried crystalline silicide layers can be fabricated in both (111)- and (100)-oriented substrates with satisfying electrical characteristics. The internal silicide growth process during annealing after high fluence ion implantation is often called "mesotaxy" by analogy with epitaxy which refers to single-crystal growth on surfaces [219, 220].

The formation of metal-silicide layers in silicon by ion beam synthesis is a two-step process, in which a sufficient amount of metal ions such as Co^+, Ni^+, Fe^+, or Cr^+ with high fluence is first implanted into heated Si substrates (300–500 °C) to retain crystallinity during implantation. During the second step, the Si substrates are subsequently annealed at elevated temperatures (600–1,000 °C) until a monocrystalline planar silicide layer epitaxially embedded in monocrystalline silicon is formed. A detailed description of these processes can be found, for example, in [200].

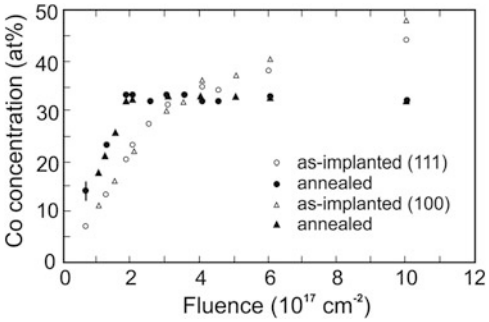

Fig. 4.41 Co peak concentration in as-implanted and annealed (100)- and (111)-oriented Si samples as a function of ion fluence for a Co^+ ion energy of 200 keV [200, 222]

The most thoroughly investigated silicides with metallic behavior formed by ion beam synthesis are $CoSi_2$ and $NiSi_2$ because of their superior material properties and therefore of their possible applications as contacts and electrical interconnects in silicon technology. $CoSi_2$ and $NiSi_2$ with a cubic CaF_2 lattice structure have a lattice constant which is close to that of Si and the lattice mismatches relative to Si amounts to only -1.2 % for $CoSi_2$ and -0.4 % for $NiSi_2$ leading to well-controlled epitaxial growth of crystalline layers in silicon. For ion beam synthesis of $CoSi_2$, Co^+ ions in the energy range of ~(100–250) keV high fluences of (1–5) $\times$ 10^{17} cm^{-2} are implanted into silicon at a substrate temperature of 350 °C. The annealing is carried out in two steps: at 600 °C for 1 h in vacuum (or inert gas atmosphere) to initiate the silicide precipitation and regrowth of the silicon followed by a 1,000 °C, 30 min, annealing step for the coalescence of the cobalt silicide precipitates to a well-defined 110 nm thick $CoSi_2$ layer buried under a crystalline silicon overlayer with a thickness of ~60 nm in the case of a 200 keV Co^+ implantation [221]. Experimentally it was found that for ion beam synthesis of buried $CoSi_2$ layers a Co peak concentration c_{peak} ~ 18 at.% is required. Therefore, at an ion energy of 200 keV ion fluences exceeding 10^{17} cm^{-2} are necessary. For the 200 keV Co^+ implantation carried out at 350 °C, Fig. 4.41 shows the dependence of the Co peak concentration on ion fluence in Si for as-implanted and annealed samples [222].

As can be seen, in the as-implanted state the Co peak concentration depends linearly on the ion fluence up to $\Phi \approx 3 \times 10^{17}$ cm^{-2} beyond which the dependence becomes nonlinear. This value nearly coincides with the calculated value of ~2.7×10^{17} cm^{-2} at which the peak concentration achieves the composition of $CoSi_2$ [200]. In the region of linear fluence dependence, the synthesized layers after implantation are Si-rich and consist of isolated $CoSi_2$ precipitates. At a fluence above 3×10^{17} cm^{-2}, where the slope changes, the peak concentration reaches the stoichiometric value for $CoSi_2$ and epitaxial aligned $CoSi_2$ layers are already formed during ion implantation.

For samples annealed at $T \geq$ 1,000 °C, the dependence of the Co peak concentration on ion fluence in the region of $\Phi < 1.8 \times 10^{17}$ cm^{-2} increases compared to

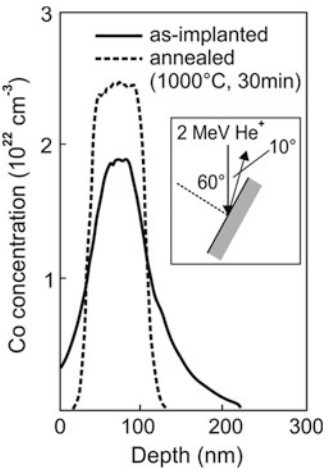

Fig. 4.42 Co concentration profiles obtained from RBS measurements after 170 keV Co^+ implantation of 2×10^{17} cm^{-2} and subsequent annealing at 1,000 °C for 30 min [223]

the as-implanted state. At fluences above 1.8×10^{17} cm^{-2} a distinct discontinuity appears in the slope and the Co concentration becomes constant where $CoSi_2$ layers of stoichiometric composition are formed. As can be concluded from Fig. 4.41 for a critical Co^+ ion fluence of $\Phi_{crit} = 1.8 \times 10^{17}$ cm^{-2}, the Co concentration in the maximum of the implanted profile amounts to $c_{crit} = 19$ at %. The criterion for the peak concentration $c_{peak} > c_{crit}$ where continuous $CoSi_2$ layers can be formed by IBS is only a necessary, but not a sufficient condition for the formation of a uniform planar buried layer, because IBS depends on implantation and annealing conditions. The epitaxial growth of $CoSi_2$ during annealing is shown in Fig. 4.42 where Co depth profiles obtained by RBS measurements for the as-implanted (170 keV, 2×10^{17} cm^{-2}) and the annealed (1,000 °C, 30 min) are compared [223].

The steep increase and decrease of the Co concentration at the boundaries of the buried silicide layer shows that this layer is very uniform and has sharp interfaces to the silicon substrate. During growth of the silicide layer from the initial Gauss-like depth profile, a depletion of Co occurs in the tails of the initial profile due to the dissolution of Co from smaller silicide precipitates, followed by diffusion of Co towards larger $CoSi_2$ precipitates in the region of increasing Co concentration (Ostwald ripening). The ripening leads to a contraction of the initial depth distribution towards the maximum concentration of the profile. With increasing annealing time precipitates grow and finally coalesce to a continuous buried layer. For Co and other silicides, the reaction is nucleation controlled and the moving species are the metal atoms.

As confirmed by structural investigations (TEM) the single-crystalline $CoSi_2$ layers have atomically abrupt interfaces in both (100)- and (111)-oriented Si. The observation of misfit dislocations at the $Si/CoSi_2$ interfaces indicates that the silicide is not pseudomorphic with the Si crystal. The achieved resistivities of

the ion beam-synthesized $CoSi_2$ layers in (100)-Si are about ~1 μΩ cm and lower by a factor of two than those of the best UHV-deposited $CoSi_2$ layers [224]. Because the structural quality of the silicide layers is not as high as for MBE grown layers this unexpected result may be due to the inherent cleanliness of the IBS process. Since the silicide layers form beneath the surface of the silicon substrate prior cleaning procedures of the Si surface are not critical. Moreover, the Co^+ ions are mass selected and do not contain common contaminants (e.g., oxygen, nitrogen, carbon) present in typical evaporation sources.

For the other cubic disilicide $NiSi_2$ similar results have been achieved [225, 226]. In general, ion beam-synthesized films of nickel disilicide have a much higher residual resistivity than those of $CoSi_2$, perhaps because of residual crystal defects, but comparable to or better than MBE grown films. Since $NiSi_2$ melts at 980 °C, the annealing is limited to lower temperatures than for the $CoSi_2$, which may be the reason for some of the structural and electrical differences. The structural and electrical characteristics of ion beam-synthesized $NiSi_2$ films strongly depend on the postannealing temperature and time. The poly-crystalline nickel disilicide already forms during ion implantation with a fluence of 1×10^{17} cm^{-2} at a sample temperature of ~100 °C. A good sheet resistance of $NiSi_2$ film correlated with the Si/Ni ratio has been achieved at ion fluences of ~1×10^{17} cm^{-2} and subsequent annealing at 550 °C for 30 min. The achieved minimum sheet resistance of $NiSi_2$ layers is in the order of 50 μΩ cm and somewhat larger compared to $CoSi_2$. The thickness of a buried silicide layer can be tailored by the choice of the ion energy and the ion fluence. If the implanted ion fluence exceeds the threshold value Φ_{crit} nearly all the implanted atoms will be located in the synthesized layer after high-temperature annealing. The thickness d of the buried layer depends linearly on the ion fluence Φ and is given by $d = \Phi/n$ for $\Phi > \Phi_{crit}$ where n is the atomic density of the metal atoms in the silicide. Layers in the thickness range between 15 and 400 nm have been prepared, using ion energies between 20 keV and 6 MeV.

Ion beam synthesis of other metallic silicides has been also investigated, for example, WSi_2 with regard to the possibility of using them as a gate and interconnect metallization material in semiconductor devices [227]. It was shown that good sheet resistance of tungsten silicide films is achieved and continuous epitaxial layers of WSi_2 with smooth surface morphology can be effectively produced with 40 keV W^+ ions at an ion fluence of 1×10^{17} cm^{-2} with a one-step annealing at 800 °C for 30 min. The ion beam synthesis of semiconducting transition metal silicides ($CrSi_2$ [228], β-$FeSi_2$ [229]) and Ru_2Si_3 [230] has been studied extensively because of their direct or indirect band gap in the order of ~(0.3–0.8) eV and of promising applications in silicon heterostructures (e.g., narrow base hetero-bipolar transistors) and optoelectronic devices in silicon (e.g., efficient light sources in silicon). Ion beam-synthesized rare earth silicides ($ErSi_2$ [231], and $ErSi_{1.7}$, $YSi_{1.7}$, and $Er_{0.5}Y_{0.5}Si_{1.7}$ [232]) are of technical interest with regard to application in infrared light detection and in ohmic contacts.

As minimum feature sizes decrease in integrated circuit technology, ion beam synthesis of silicides without the requirement for a defining mask to delineate the implanted area can be carried out with a focused ion beam (FIB) [233–235].

The FIB implantation of Co^+ ions is an alternative to the critical and costly process of transferring submicrometer patterns where the masking layer must withstand high-fluence implantation. As has been demonstrated the ion beam synthesis of $CoSi_2$ structures by FIB with deep submicron feature sizes can be achieved either by conventional two-step furnace annealing or by short-time flash-lamp annealing (FLA) in the melting regime. At FLA the common physical process of $CoSi_2$ precipitation and coalescence is replaced by the physical process of local melting and recrystallization [236]. During FLA (3 ms pulse, energy density $J = 120$ J cm^{-2}, 700 °C preheating) regions of transiently molten silicon are selectively formed at locations where the implanted patterns provide efficient nucleation centers. The implanted Co dissolves in the molten region immediately. During rapid cooling of the wafer surface, the recrystallization of molten regions lasts only a fraction of a second. During resolidification, the strong segregation of Co at the moving solid–liquid interface results in an increase of the Co concentration in the melt. This process stops when the eutectic concentration is reached which is close to the concentration of Co in the stoichiometric $CoSi_2$. The final width of the $CoSi_2$ NWs is proportional to the amount of implanted cobalt within the transiently molten region, assuming the formation of a stoichiometric silicide in the stripe.

With the FIB a small beam spot (typically <200 nm in diameter) is rastered across the sample to form the implanted silicide. Compared to conventional broad-beam ion implantation with ion current densities of ~10 μA cm^{-2} the current densities of FIB systems are typically ~1 A cm^{-2}. At such high current densities ion fluence rate (ion flux) effects at implantation into Si for ion beam synthesis must be taken into account [234]. It was found that the damage of the Si lattice has a strong influence on the $CoSi_2$ layer formation and that the increased damage accumulation at long dwell times of the FIB prevents the formation of continuous $CoSi_2$ layer. Cobalt disilicide layers have been produced by 70 keV Co^{++} implantation with a spot size of 200–300 nm into silicon heated to a temperature of 400 °C. The beam was scanned meander-like on an area of 40 × 40 μm^2 using subsequent pixels with a distance of 80 nm. The total fluence was about 1×10^{17} cm^{-2}, corresponding to 3×10^1 and 3×10^3 frames at dwell times of 100 and 1 μs, respectively. The samples were furnace annealed by the usual two-step procedure for 60 min at 600 °C and 30 min at 1,000 °C in a nitrogen atmosphere. The annealed samples show that continuous $CoSi_2$ layers can only be formed using sufficiently short pixel dwell times of the FIB spot (see Fig. 4.43).

When the dwell time is increased, the layers exhibit holes and are completely disintegrated at a dwell time exceeding 100 μs. The use of short dwell times results in a lower damage of the target. For example, for the implantation using 1 μs dwell time the silicon surface layer remains crystalline, whereas for a dwell time of 250 μs the surface layer becomes amorphous. Thus, it was concluded that different dwell times (ion fluxes) result in a different degree of damage due to dynamic defect annealing.

Co^+ ion implantation with a FIB was applied in [235] to study ion beam synthesis of $CoSi_2$ nanowires (NW) in silicon (see Figs. 4.44 and 4.45). Two

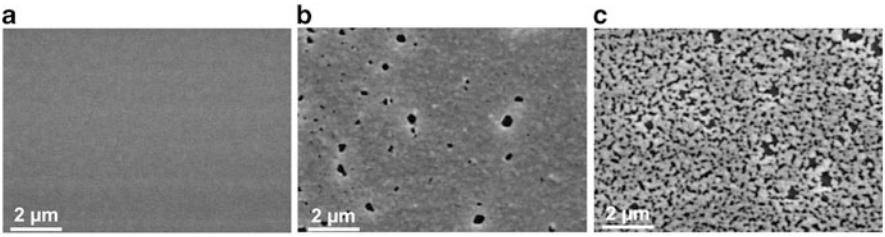

Fig. 4.43 Plane view SEM images of the influence of different FIB dwell times on $CoSi_2$ layer formation. (**a**) $CoSi_2$ layer fabricated with a short pixel dwell time of 1 µs. The layer is continuous and smooth. (**b**) The dwell time is increased to 50 µs and the layer shows some holes and an enhanced roughness. (**c**) Increase of dwell time to 100 µs leads to totally disintegrated layer. Experimental parameters are: (111) Si substrate, fluence of 1×10^{17} cm^{-2}, ion beam spot size of 300 nm, ion current density of 1 A cm^{-2} [234]

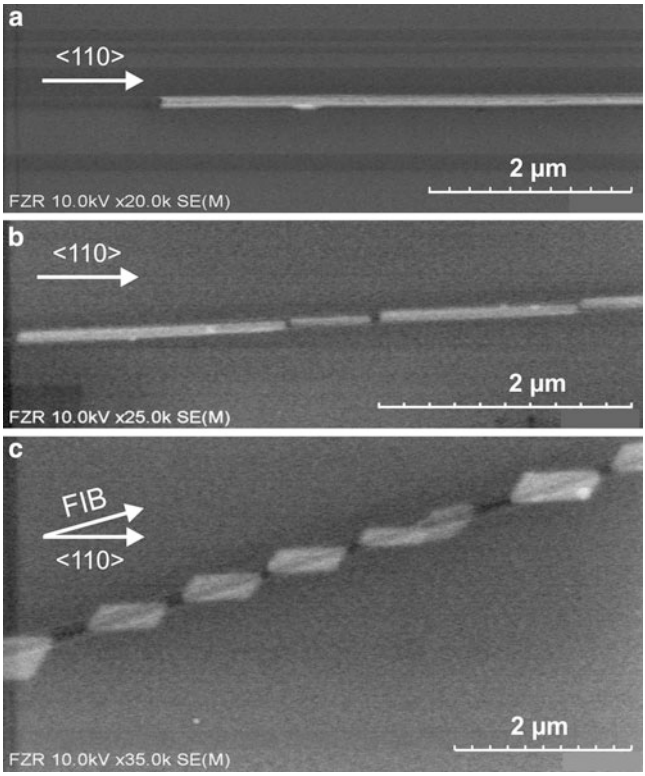

Fig. 4.44 $CoSi_2$ nanowires in (100)-Si (**a**), in (111)-Si with a small misalignment (**b**), and with a misalignment angle of about 15° (**c**). The Co^{++} FIB implantation fluence was 1×10^{17} cm^{-2} [235]

mechanisms of $CoSi_2$ nanowire formation were investigated: first, conventional synthesis by Co^{++} FIB implantation at elevated temperatures into silicon along in-

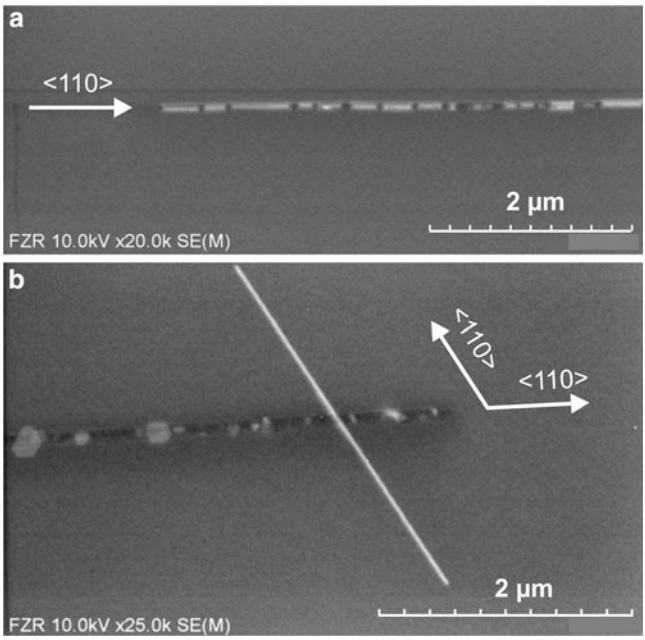

Fig. 4.45 $CoSi_2$ NW in (100)-Si implanted with a fluence of 7×10^{16} cm^{-2} (**a**) and in (111)-Si, implanted with a fluence of 3×10^{16} cm^{-2} (**b**) [235]

plane ⟨110⟩ Si crystal direction and subsequent conventional two-step annealing, and second, self-aligned $CoSi_2$ nanowire growth in cobalt supersaturated silicon on defects induced by FIB at room temperature during subsequent annealing.

Conventionally synthesized NWs (Co^{++}, 60 keV, 1×10^{17} cm^{-2}) showed lengths of 10–20 µm and diameters of 100–150 nm in the case of FIB implantation along the chosen ⟨110⟩ direction. A small deviation of the FIB trace from this direction leads to a decay of the NW into shorter fragments and larger angles of FIB trace misalignment cause the formation of chains of more or less prolonged $CoSi_2$ nanoparticles. Further reduction of the NW diameter was expected by decreasing the concentration of Co atoms implanted in silicon at the same FIB spot. NWs synthesized at lower fluences of 1×10^{16}–7×10^{16} cm^{-2} are not stable and decay into shorter NW fragments with a diameter of about 50 nm. Moreover, because of the existence of the other ⟨110⟩ crystalline directions crossing the FIB trace, there is a certain probability of spontaneous and self-aligned NW growth in these two directions. This effect has been explained by the existence of the well-known {311} defects in silicon induced during FIB implantation [237]. These defects are closed between two {311} planes and are elongated in the ⟨110⟩ direction. During annealing the implanted and solved Co atoms diffuse and can be gettered in the {311} defects. They react with silicon and form silicide precipitates along these defects, i.e., along the ⟨110⟩ direction which is the most preferable direction for the one-dimensional $CoSi_2$ crystalline structure growth. This process stabilizes the

defect structure and hinders dissolution of the rod-like defects. Subsequent Oswald ripening of the silicide precipitates along this ⟨110⟩ direction leads to the formation and alignment of initial oblong $CoSi_2$ nanoparticles at the defect position. During further heating the solved cobalt atoms are still available around the nanoparticles and diffuse to them promoting the growth of crystalline $CoSi_2$ NWs. This finally results in the formation of some micrometer long NWs. In contrast to conventional ion beam synthesis of $CoSi_2$ NWs by high-fluence FIB implantation along a narrow trace, the defect induced and self-aligned NWs seem to be more stable.

4.3.3 Ion Beam Synthesis of Nanocrystals in Insulators

With the combined utilization of ion–solid interactions that lead to far-from-equilibrium states and thermodynamic processes resulting in relaxation toward equilibrium, tiny nanostructures [often called nanoparticles (NP), nanoclusters or nanocrystals (NC)] of controlled composition can be formed in virtually any matrix. Still, the size of the nanostructures obtained in this self-organization approach is much below the capabilities of present days direct structuring techniques, as, e.g., extreme ultraviolet optical lithography or direct writing electron beam lithography. By now literature contains a wealth of publications on different ion–matrix combinations that potentially might trigger applications of these novel nanoscale materials [238–242]. The properties of nanoparticles are dominated mainly by two effects:

1. Increasing surface energy associated with increasing surface-to-volume ratio for small NPs which determine their physical and thermodynamic properties (e.g., melting point, solid phase transition, and bulk modulus)
2. With decreasing NP size change of the band structure (e.g., transition from indirect to direct semiconductors, widening of band gap) and electron confinement in NPs

Both effects lead to novel electronic properties showing a wide range of effects, for example, large nonlinear optical susceptibility of metal nanoparticles, effective photoluminescence, and charge storage properties of semiconducting NPs.

Ion beam synthesis of metal NPs (e.g., Au, Ag, Cu) in an inert dielectric medium (e.g., SiO_2, Al_2O_3) concerns to change or improve the properties of optical materials such as reflectivity, absorption, refractive index, and luminescence. This application of IBS is driven by the demands on optical materials with higher data transfer velocity and the fabrication of purely optical devices and integrated circuits. For example, metallic NPs in a dielectric matrix enhance the third-order susceptibility near the surface plasmon resonance frequency (see, for example [243]). Due to the nonlinearity in the refractive index caused by this effect, these systems have attracted much interest for use in all-optical switching devices. Additionally, the frequency of light absorbed by these metallic NPs shifts to shorter wavelengths as a function of decreasing NP size. Thus, measuring the absorption spectra of an ensemble of embedded NPs is an indirect method of determining their size. Typical process parameters in fabrication of metallic NPs for changing of

Table 4.4 Implantation and annealing conditions at IBS of Cu, Ag, and Au NPs

Process parameter	Cu	Ag	Au
Energy E (keV)	30–160; 3,500	50–300; 3,500	1,500–4,400
Fluence Φ (cm^{-2})	(1–10) × 10^{16}	(0.1–60) × 10^{16}	(0.1–15) × 10^{16}
Current density j (μA cm^{-2})	0.7–10	0.2–14	0.5–2.0
Target temperature T_i (°C)	RT–1,100	RT–600	LN_2, RT-600
Annealing temperature T_A(°C)	–	400–700	700–1,200
Annealing time t_A (h)	1 (at implantation)	12 ns–1 h	0.5–36
Annealing atmosphere	Vacuum (implant. chamber)	Vacuum (implant. chamber)	Air, O_2, Ar + 4% H_2 (furnace)

linear absorbance, luminescence, and producing of nonlinear optical effects are summarized in Table 4.4.

At ion beam synthesis of metal NPs in optical materials the ion energy is chosen in a broad range from some tens of keV up to some MeV with corresponding high fluences in the range of ~1 × 10^{15}–1 × 10^{17} cm^{-2} to achieve impurity concentration in the order of (1–10) at % in the maximum of the implanted profile. The annealing conditions are selected specifically for the kind of implanted metal ions. The NP growth kinetics and the NP size distribution are significantly influenced by the implantation as well as annealing parameters. In contrast to Au, the NP formation during ion irradiation without subsequent annealing is more pronounced for Cu (and sometimes for Ag) ions implanted into silica. Annealing for the formation of certain Ag and Au NP cluster sizes is usually carried out at (400–700) °C and (600–1,200) °C, respectively. The influence of the target temperature during implantation into quartz glass and the ion current density on the NP size distribution has been investigated in [244, 245]. At room temperature implantation and at relatively low ion current densities a more sharp NP size distribution with a mean NP diameter of (5–10) nm is formed. With increasing both the target temperature T_i and ion current density j, the NP size rises up to (25–30) nm with a broader distribution.

For Cu the distribution of NP size in dependence on the impurity concentration in the maximum of the Cu depth profile shows a linear behavior with $d_{NP}(nm) = 0.15\ N_{Cu}(cm^{-3})$ [246]. For example, such correlations are helpful in tuning the metal NP sizes during IBS.

The formation of Ag NPs has been observed already at 150 keV Ag^+ ion implantation into different types of glasses without annealing where the mean cluster diameter is in the range of 6–40 nm for ion fluences of 2 × 10^{16} cm^{-2} and 7.6 × 10^{17} cm^{-2}, respectively [247, 248]. For Ag NPs it was found that the chemical composition of the glass can influence the NP growth and the final size distribution. Subsequent annealing of Ag^+-implanted glasses leads to dissolution of large NPs into smaller ones and at higher annealing temperatures (or heated samples during implantation) and to an increased Ag solution in the glass matrix [249].

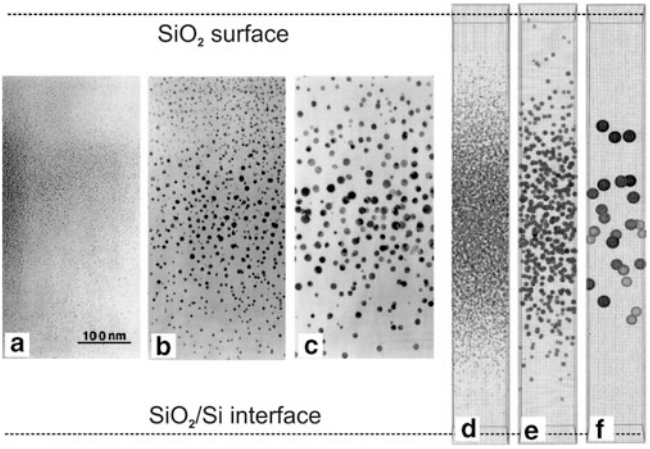

Fig. 4.46 *Left*: Cross-section TEM images of 2.75 MeV Au^+-implanted fused silica for a fluence of 1.5×10^{17} cm^{-2} and implantation temperatures at (**a**) room temperature, (**b**) 400 °C, and (**c**) 600 °C (TEM images were taken from the central region of the implanted profile). *Right*: KLMC simulation results of Au NP formation during ion implantation. (**d**)–(**f**) show the NC distributions immediately at the end of implantation for the investigated parameter T_i and a constant j (taken from [252])

The IBS of Au NPs is usually carried out using MeV Au^+ ion implantation with fluences 3×10^{16}–1.5×10^{17} cm^{-2} where the nucleation and NP growth depend on implantation temperature T_i and ion current density j [250, 251] and can be additionally changed at subsequent annealing. In the as-implanted state, Au NPs with a mean size of <5 nm have been observed. During subsequent annealing at (900–1,100) °C, the mean Au NP size increases up to ~30 nm. Investigations of the NPs growth kinetics showed a time dependence of the NP growth with $\overline{R} \sim (t)^{1/3}$, which is typical for Ostwald ripening. Kinetic 3D lattice Monte Carlo (KLMC) method has been applied to describe nucleation and growth of Au NPs in SiO_2 [252]. This system is well suited for fundamental studies of the mechanisms of NP formation, because (1) Au does not tend to form an oxide or silicide since Au atoms are chemically inert with respect to the constituents of the host material and (2) Au is observed to precipitate during the implantation stage. The basic dependences of the depth-dependent NC size distribution on the main implantation parameters, i.e., the implantation temperature T_i and the ion current j (ion flux) have been modeled. Using the KLMC model, the principal dependences of the observed particle size distributions can be understood and are qualitatively in good agreement with corresponding experiments.

In Fig. 4.46 fused silica or thermally oxidized silicon wafers with an oxide thickness of 1.7 μm were implanted with Au^+ ions at an energy of 2.75 MeV to fluences in the range of 3×10^{16}–1×10^{17} cm^{-2}. At this energy the projected range of the Au^+ ions is about 0.9 μm. The current density j was approximately 1 μA cm^{-2} and the substrate temperatures during implantation T_i have been varied

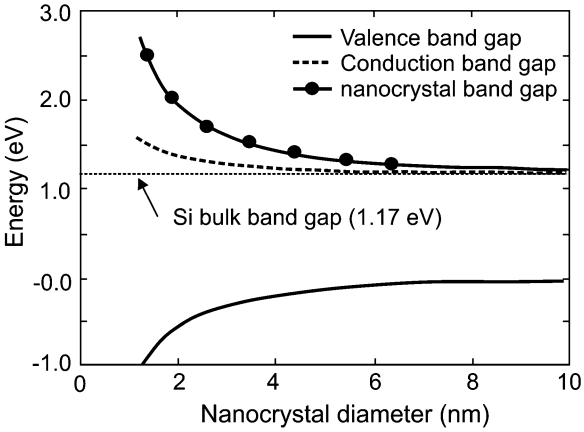

Fig. 4.47 The band gap energy as function of the NP radius shown for spherical Si quantum dots [254]

from room temperature to 600 °C. As shown in Fig. 4.46 a qualitatively good agreement between simulated and experimentally observed NC size distributions has been observed with respect to the different implantation temperatures.

In many publications among the structural (NP size and distribution) and chemical properties (compound formation, embedding into the host matrix), the optical properties have been investigated intensively, for example in [238, 245, 251, 253]. It must be mentioned that for ion beam-synthesized metallic NPs a volume fraction of NPs in the range of (1–10) % can be achieved. This value is by a factor of 10^3–10^4 higher compared to incorporation of colloidal NPs during glass melting at thermodynamic equilibrium. Consequently, one can expect approximately the same absorbance of a 0.2 µm thick ion beam modified layer compared to ~1 mm thick conventional optical glasses.

In contrast to metallic NPs, semiconducting NPs (Si, Ge) show for sizes of a few nanometers pronounced luminescence, due to the fact that with decreasing NP size the electronic band structure changes and direct electron transition into the conduction band becomes possible. As an example, the size-dependent energy gap for Si NPs is shown in Fig. 4.47, which inherently affects the electronic and optical behavior of ion beam-synthesized NPs.

The recombination of electrons into the valence band is accompanied by photoemission (photo- or electroluminescence). Due to the tininess, the NP can be considered as a "quantum dot," i.e., its electronic states are quantized and the density of states is singular, i.e., an electron can occupy the quantized energy level. The energetic spacing between neighboring energy levels increases with decreasing cluster size. For an insulating matrix surrounding the NP, the NP can be regarded as a potential well of finite depth. In this context, the NP acts as a trap for electrons or holes, since it confines them. This effect of quantum (or rather electron/hole) confinement is a principal aspect of semiconducting NPs for

electronic and opto-electronic applications in charge carrier storage and electroluminescent devices, respectively. So, band-to-band recombination of confined excitons in the NCs yields a near-infrared luminescence which is much more efficient than that of bulk silicon (photoluminescence quantum efficiency of about 59 % [255]). Moreover, the surface-to-volume ratio of NPs is significantly larger in comparison with bulk materials which implies that the electrical and optical properties of the NPs are remarkably determined by NP surface or rather NP-insulator interface contributions. Si (and also Ge) nanocrystals (NCs) are a very promising material in silicon-based memory and optoelectronic technologies (e.g., Si NC-based laser devices [256] and photovoltaic solar cells [257]) fully compatible to modern complementary metal oxide semiconductor (CMOS) processing.

The development of luminescing device structures based on ion beam-synthesized Si and Ge nanocrystals in a well-controlled fabrication process requires information about the depth distribution of the nanoclusters embedded usually in the SiO_2 layer thermally grown on silicon. Implanted metals (e.g., Au, Ag, Cu) in a glassy or SiO_2 matrix often show a significant redistribution after thermal treatment with preferred accumulation of metal NPs at the surface or internal interfaces (e.g., [258]). On the contrary, the low diffusion coefficient of Si and Ge in SiO_2 suggests a depth distribution of semiconductor nanoclusters, which corresponds to the as-implanted profile [259, 260].

The implantation (ion energy and fluence) and annealing (temperature and time) conditions at ion beam synthesis of Ge and Si NPs depend on the provided application and on the substrate material. As substrates often fused silica, sapphire and SiO_2 layers thermally grown on silicon are used. For optical and electronic device applications, thermally grown SiO_2 is the common insulator material, allowing the device and circuit fabrication in a CMOS compatible process. Depending on the SiO_2 layer thickness, the Si^+ and Ge^+ ion energies are used in a wide range from low to high ion energies (1 keV–1 MeV) at relatively high ion fluences in the order of $\sim(1–10) \times 10^{16}$ cm^{-2}. The phase separation through precipitation and Ostwald ripening is achieved usually at annealing temperatures of $T_A \approx$ (600–1,200) °C in inert gas atmosphere using RTA or furnace annealing for $t_A \approx$ (30–300) s and $\approx$ (0.5–4) h, respectively. In contrast to the formation of metallic NPs in a glassy matrix, the ion current density during ion implantation does not have an observable influence on NP size and size distribution. However, the impurity redistribution and NP evolution can be strongly influenced by the annealing ambient as has been reported in [261] for Ge-implanted SiO_2 layers. The origin of this behavior is the in-diffusion of an oxidant from the annealing atmosphere, which changes substantially the Ge depth profile and NP distribution. It should be emphasized that even for atmospheres having oxidant (moisture) concentrations as low as a few ppm, such unusual Ge redistributions have been found [262]. These effects of influence of the annealing ambient, for example, on the microstructure of Ge-implanted SiO_2, have been studied by annealing in N_2, Ar, or dry O_2 atmospheres with different concentrations of chemical reactive components (H_2O, O_2). 500 nm thick SiO_2 layers thermally grown on (100)-oriented Si wafers were implanted with 350 keV Ge^+ ions and fluences between

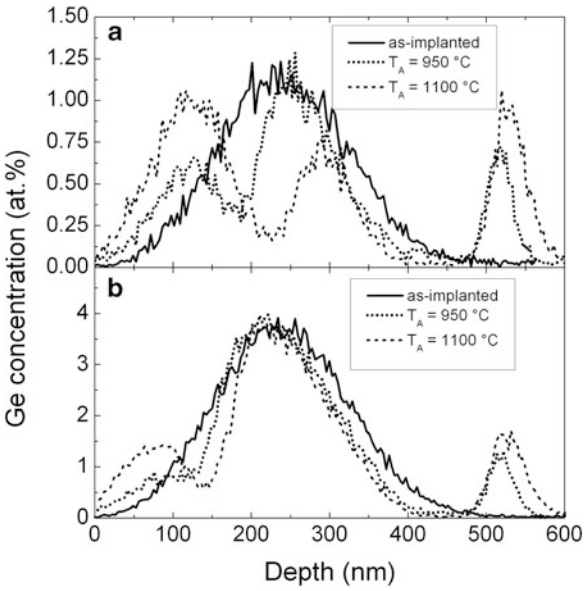

Fig. 4.48 Ge concentration profiles obtained from RBS spectra of 500 nm thick SiO_2 layers on Si which were implanted with 350 keV Ge^+ and subsequently annealed in N_2 for 1 h. (**a**) $\Phi = 1.5 \times 10^{16}\ cm^{-2}$, (**b**) $\Phi = 5.0 \times 10^{16}\ cm^{-2}$ [262]

5×10^{15} and $5 \times 10^{16}\ cm^{-2}$, which results in peak concentrations of implanted Ge of (0.4–4.0) at.%, respectively. The annealing was performed at 950, 1,000, and 1,100 °C in a standard furnace for 15–180 min using the "inert" gases of N_2, Ar, or the "reactive" gas of dry O_2 (all of 5.0 purity). In Fig. 4.48 the Ge depth distributions measured by RBS are shown. The as-implanted Ge profiles are located inside the SiO_2 layer, i.e., the Ge concentrations at the surface and the Si/SiO_2 interface are below 1 % of the peak concentration.

For both fluences the RBS spectra show unusual changes in the Ge depth distributions after annealing at 950 °C in N_2. Three well-separated peaks are found, whose separation from each other increases with increasing annealing temperature. The width and height of the central Ge peak decrease and the two satellite peaks grow. As it has been shown by STEM-EDX analysis [263], the Ge at the Si/SiO_2 interface is located within a thin Si layer at the Si/SiO_2 interface where it forms a few monolayers of a Si–Ge alloy. At the higher annealing temperature of 1,100 °C, Ge diffuses partly into the Si substrate as it can be expected from the complete miscibility of Ge and Si. After annealing (see Fig. 4.49b, c), in the center of the SiO_2 layer Ge NPs appear which are related to the central peak in the RBS spectrum (see Fig. 4.48b).

For the Ge nanocluster distribution of Fig. 4.49c, a mean cluster size of 6 nm was observed, which is in good agreement with the mean cluster size of (6.4 ± 0.7) nm measured by XRD. Towards the SiO_2 surface, the Ge cluster band is terminated by a very narrow (11.1 nm) edge region, which is in contrast to the smooth tail of nanoclusters facing the Si substrate. No Ge clusters were found between the sharp edge of the cluster band and the SiO_2 surface, where a pronounced subsurface peak

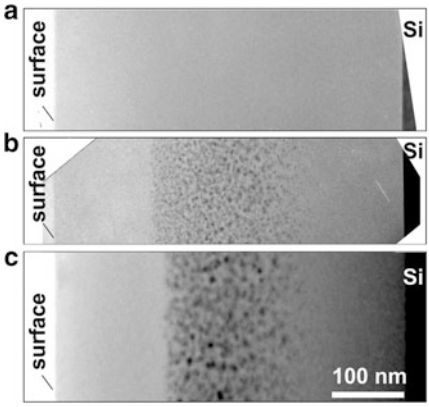

Fig. 4.49 Cross-sectional TEM micrographs of 500 nm thick SiO_2 on Si implanted with 5×10^{16} cm^{-2} at 350 keV prior to annealing (**a**) as well as after annealing at 950 °C for 1 h (**b**) and 1,100 °C for 1 h (**c**) [262]

of Ge was observed by RBS (Figs. 4.48 and 4.49). XPS measurements reveal that Ge 2p3/2 photoelectrons coming from the central, cluster-related peak and from the interface peak can be attributed to elemental Ge, whereas the energy of photoelectrons from the subsurface peak is shifted indicating Ge–O bonds [264]. The Ge redistribution and nanocluster evolution of identically implanted but Ar annealed SiO_2 layers are quite similar to the samples annealed in N_2. However, the Ge redistribution can be largely suppressed by the deposition of a 20 nm thick capping layer of LPCVD-Si_3N_4 on top of the SiO_2 layer before ion implantation. The disappearance of the drastic Ge redistribution during annealing in samples protected by a diffusion barrier underlines the strong influence of the annealing ambient on Ge and Si NP formation in SiO_2. After annealing in dry O_2 for 15 min (Fig. 4.50a) the general features of the NP depth and size distribution appear to be similar to samples annealed in N_2 (Figs. 4.48 and 4.49) or in Ar. However, the evolution of NPs is faster and/or occurs at lower temperatures. At longer annealing times (30 and 45 min) the sharp edge of the NP band of elemental Ge shifts progressively into the depth of the layer. In contrast to annealing in N_2 (or Ar), on the rear side of the moving sharp edge of the Ge NP band a layer of diffuse precipitates was observed (Fig. 4.50b, c).

In comparison to annealing in N_2 (or Ar), annealing in dry O_2 increases the surface concentration of the oxidant by orders of magnitudes which overcompensates the smaller diffusivity of O_2 compared to H_2O. Thus, the zone of GeO_2 formation shifts towards the edge of the nanoparticle band. Finally, the arriving oxidant cannot be consumed completely by dissolving Ge which results in direct oxidation of Ge nanocrystals. These GeO_2 nanoclusters can be seen in the TEM images of Fig. 4.50d. Due to their lower specific Ge density and amorphous structure, they can be distinguished from Ge NPs by a lower Z-contrast, diffuse boundaries, and the absence of lattice plane imaging by HRTEM. For the explanation of Ge redistribution due to chemical effects, the following model was proposed [262]: Ge^+ ion implantation forms a highly supersaturated solution of Ge in SiO_2.

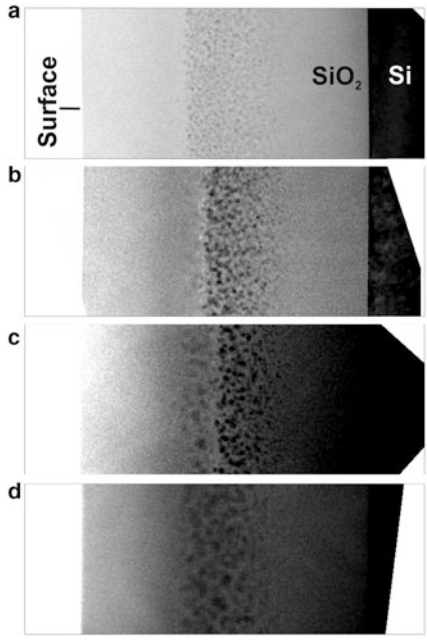

Fig. 4.50 Cross-sectional TEM images of 500 nm SiO_2 layers on Si implanted with 5.0×10^{16} cm^{-2} at 350 keV after annealing at 950 °C in pure O_2 for 15 min (**a**), 30 min (**b**), 45 min (**c**), and 90 min (**d**). Amorphous diffuse GeO_2 nanoclusters can be seen in (**c**) and (**d**) [262]

At the initial stage of annealing most of Ge (Si) precipitates to tiny Ge NPs, whereas a small fraction of Ge (Si) remains dissolved in SiO_2. The concentration c of dissolved Ge (Si) around a nanoparticle is given by the Gibbs–Thomson relation (4.26). In an ensemble of nanoparticles, the average supersaturation $\langle c - c_{sol} \rangle_{av}$ is proportional to $1/R_{av}$, where R_{av} is the mean NP radius. During annealing an oxidant (e.g., moisture) can diffuse into SiO_2 where it oxidizes dissolved Ge (Si). Assuming for both species comparable diffusion coefficients, the zone of GeO_2 formation should be between the surface and the cluster band. This explains two features of the experimental data: (1) As the oxidant reacts with Ge dissolved in SiO_2, the resulting GeO_2 does not form NPs within the SiO_2 matrix. Thus, the Ge accumulated there as GeO_2 can be seen as a peak in the RBS spectra, however NPs were not observed in cross-sectional TEM images. (2) The small distance between the sink (the zone of GeO_2 formation) and the source (the layer of Ge NPs) of Ge monomers leads to a steep gradient of dissolved Ge. Therefore, an effective dissolution of nanoparticles occurs only within a narrow layer of the nanoparticle band whose width is in the order of the diffusional screening length $\lambda = (4\pi R_{av} n_{NP})^{-1/2}$, where n_{NP} is the NP density. Estimating R_{av} from Fig. 4.49 and calculating n_{NP} with the aid of the implanted fluence, the diffusional screening length can be calculated to be $\lambda = 10$ nm. This value is in excellent agreement with the width of the edge of the nanoparticle band. At the Si/SiO_2 interface (see Fig. 4.48) the concentration c of Ge dissolved in SiO_2 is lower than c_{sol} because the Ge–Si bond strength is more than 10 % larger than the Ge–Ge bond strength. In

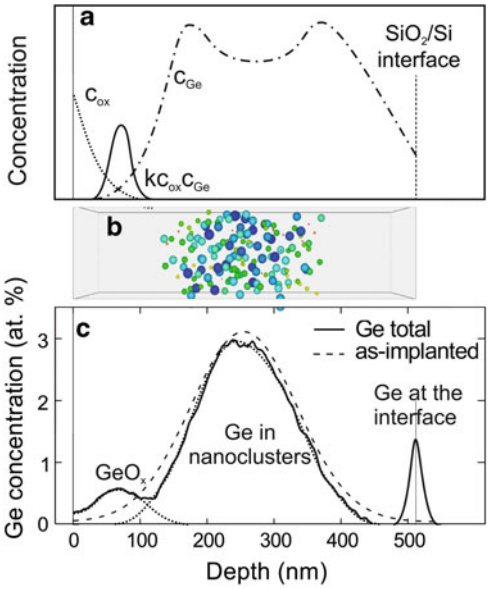

Fig. 4.51 KLMC simulation of the Ge redistribution and cluster formation in a 500 nm Ge^+ ion-implanted SiO_2 layer on Si during annealing. (**a**) Scheme of the oxidant (H_2O) concentration c_{ox}, the Ge monomer concentration c_{Ge}, and the Ge oxidation rate $k \cdot c_{ox} \cdot c_{Ge}$ in SiO_2. (**b**) The spatial and size distribution of Ge NPs. (**c**) The calculated total Ge depth profile (*full curve*), which evolved from the as-implanted profile (*dashed curve*) during annealing, consists of the three Ge components: (1) GeO_x (subsurface peak), (2) Ge in nanocrystals (*central peak*), and (3) Ge accumulated at the interface [265]

the nanocluster region c is higher than c_{sol}, therefore, the resulting concentration gradient leads to a diffusion flux and to an accumulation of Ge at the interface. There, Ge can either grow epitaxially on top of the Si substrate, or, for sufficiently high annealing temperatures, it can diffuse into the Si substrate.

Kinetic 3D lattice Monte Carlo (KLMC) computer simulations of Ge precipitation, diffusion, and oxidation as well as of cluster coarsening were performed supporting the proposed model [265]. In the simulation code, two kinds of impurities (Ge, oxidant) have been considered. Figure 4.51b, c show the results of a KLMC simulation. The Ge atoms have been deposited into the SiO_2 layer according to a Gaussian depth profile (dashed line in Fig. 4.51c).

Using appropriate diffusion coefficients for H_2O and Ge in SiO_2 as well as the Ge–Ge and Ge–Si bond strength, the total Ge profile (full line in Fig. 4.51c) is in excellent qualitative agreement with the RBS spectrum shown in Fig. 4.48b. The KLMC simulations facilitate the understanding of the driving forces for Ge redistribution, nucleation, and Ostwald ripening of NPs in SiO_2. The results of Ge redistribution were additionally supported by XPS depth profiling measuring the depth-dependent chemical bond states of Ge in the SiO_2 layer [264].

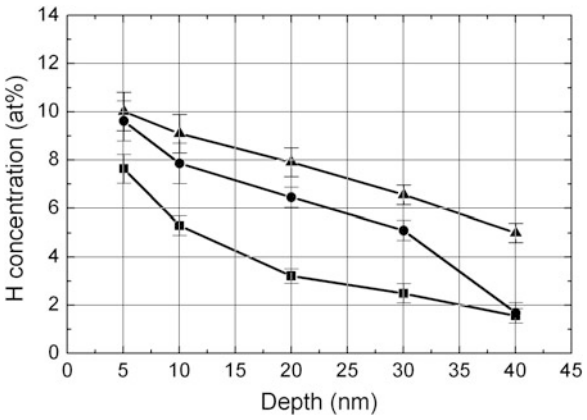

Fig. 4.52 Hydrogen depth profiles of Si^+-, Ge^+-, and Sn^+-implanted SiO_2 after storage. The ion fluence was 5×10^{15} cm^{-2} for all ions [(*filled square*) Si^+, $E = 13$ keV; (*filled circle*) Ge^+, $E = 22$ keV; (*filled triangle*) Sn^+, $E = 26$ keV] [268]

Redistribution of Ge- and Si-implanted SiO_2 by partial oxidation, possible out-diffusion, and diffusion to underlying interfaces becomes more and more critical with decreasing oxide layer thickness. For example, one of specific applications is the IBS of Si nanocrystals in thin gate oxides (SiO_2) for nonvolatile memories with a very promising performance as proposed by Tiwari et al. [266]. Because for this application the SiO_2 layer thickness of the gate oxide in the MOS-FET has been reduced below 20 nm, an increased impact of ambient on the ion beam damaged thin oxide not only during subsequent annealing but also during sample storage has to be expected.

High-fluence ion implantation (1×10^{15}–1×10^{17} cm^{-2}) for IBS of NPs in SiO_2 layers leads to a high degree of destruction of the amorphous network. In the case of low energy ion implantation ($E < 30$ keV) into SiO_2, the damaged layer will be located very near to the SiO_2 surface. The large number of broken bonds in the SiO_4-tetrahedra due to displaced Si and O atoms results in rearrangements of the fundamental ring structure within the glassy network [267] in which moisture from the ambient can be absorbed. Water molecules adsorb at the surface, and damage-enhanced inward diffusion can take place. Therefore, chemical reactions of the implanted impurities with hydrogen and oxygen must be expected during subsequent annealing which can interfere with precipitation and Ostwald ripening of nanocrystals. The incorporation of water from the ambient in stored, as-implanted SiO_2 layers and during different preparation steps in the IBS of NPs has been studied by hydrogen depth profiling using NRA [268]. The results of H depth profiling after storage (at 40 % rel. humidity in clean room) are shown in Fig. 4.52 for ions of different ion masses, implanted into SiO_2.

Concentrations of hydrogen up to 10–12 at.% due to water absorption from the ambient at a depth of 5 nm and 6–8 at.% at the projected range R_p (20 nm of different implanted ions) were measured. Moreover, this penetration of hydrogen atoms was found to increase with the energy losses provided by the implantations, i.e., increased with the fluence and the atomic mass of the implanted ions. The high amounts of incorporated hydrogen and oxygen are sufficient to interfere significantly with the precipitation and Ostwald ripening of NPs during IBS, namely to

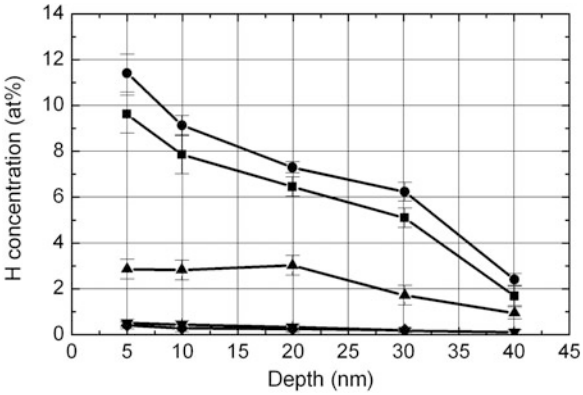

Fig. 4.53 Hydrogen depth profiles in Ge^+-implanted SiO_2 after different preparation steps [(*filled square*) storage after implantation, (*filled circle*) wet chemical cleaning (SPM), and (*filled triangle*) 600 °C annealing for 10 min in dry N_2]. For comparison, the H concentration profiles in the unimplanted, as-grown, oxide (*filled inverted triangle*) and in oxide, which was only wet-chemically treated (Piranha clean, H_2O_2/H_2SO_4) (*filled diamond*), are included [268]

enhance the precipitation and ripening process by the presence of hydrogen on one hand and to oxidize the implanted impurities partially or fully by incorporated oxygen on the other hand.

Figure 4.53 shows the results of H depth profiling after different preparation steps (storage, wet chemical cleaning, and 600 °C annealing for 10 min in dry N_2). For comparison, the H concentration in the unimplanted as-grown SiO_2 and in SiO_2 that was only wet-chemically treated (Piranha clean, H_2O_2/H_2SO_4) is included. The measured H concentration in these samples was smaller than 0.5 at.%, which is near the NRA sensitivity limit of 0.05 at.%. Wet chemical cleaning of the as-implanted samples slightly increases the H content in SiO_2 by nearly 2 at.%. Therefore, it was concluded that the H concentration up to a SiO_2 depth of (40–50) nm is caused by water absorption from the air humidity and defect-enhanced inward diffusion at room temperature. The annealing reduces the H concentration approximately by a factor of two in the depth of R_p. The reduction of the H content near the SiO_2 surface is more pronounced due to possible outward diffusion of H and OH^- and/or H_2O molecules during thermal treatment. From the measured H depth profiles, one can conclude that half of the H concentration is equal to an oxygen concentration of 3–4 at.% (most probably OH groups are present) at R_p, which is of the same order of impurity concentration in the maximum of the implanted profile. Therefore, one can expect in the initial state of postimplantation annealing (sample heating up) a very fast redistribution of the implanted profile occurs, due to the rapid formation, for example, of SiH_x and GeH_x compounds, leading to fast precipitation and even H-stimulated outward diffusion of the implanted atoms. With increasing temperature and time, oxidation (like wet oxidation of Si) of the implanted atoms Si, Ge, and Sn or of precipitates and nanocrystals takes place. The penetration and final concentration of H_2O molecules do not depend on the relative humidity in the

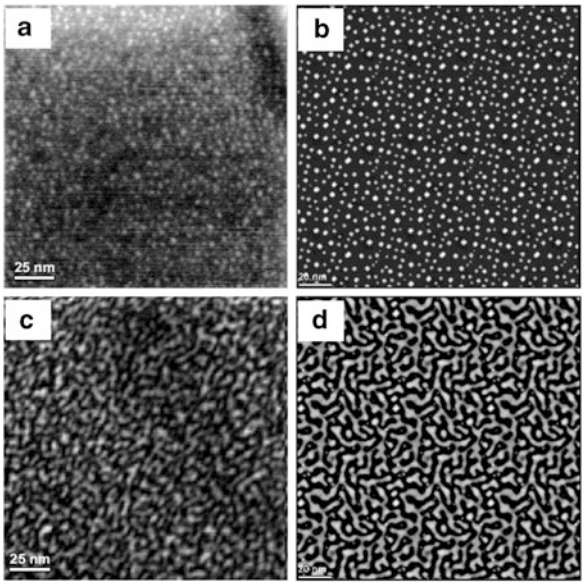

Fig. 4.54 Comparison between the morphologies of phase separated Si NPs in SiO_2 obtained by XTEM (PEELS-STEM) imaging [*left*, (**a**, **c**)] and KMC simulations [*right*, (**b**, **d**)]. Nucleation of Si NCs is observed (**a**) for a Si fluence of 1×10^{16} cm^{-2} and predicted with the same morphology for (**b**) 3×10^{15} cm^{-2}. Spinodal patterns are imaged (**c**) for 2×10^{16} cm^{-2} and simulated (**d**) for 8×10^{15} cm^{-2}. *Bright* and *dark regions* correspond to Si and SiO_2 phases, respectively (from [271])

atmosphere but are mainly limited by the degree of damage, i.e., the concentration of defects, in the SiO_2 matrix.

Unexpected nanocrystal distributions, especially in very shallow implanted SiO_2 layers, can be explained by these chemical effects during IBS. The observed water incorporation is very important in IBS for the case of Si, Ge, and Sn NPs in ultrathin gate oxides (10–30 nm thick) that were intensively investigated because of their potential application in nanocrystal-based nonvolatile memory devices [269]. For example, studies on low energy 1 keV Si^+ ion beam synthesis of Si NP embedded in 10 nm thick SiO_2 layers have been done [270, 271]. The morphology of Si NPS thin gate oxide layers has been investigated by TEM imaging (PEELS-STEM) and compared with kinetic three-dimensional lattice Monte Carlo (KLMC) simulation. Remarkable agreement between the atomistic simulations and the PEELS-STEM images was found. However, the predicted Si^+ ion fluences are significantly lower than the experimental ones. A substantial fraction of the implanted Si is lost by parasitic oxidation with atmospheric humidity as shown in Fig. 4.54.

The quantitative analysis of the characteristics of Si NPs populations shows that only a fraction of the implanted fluence (up to 40 %) has precipitated into NPs. Furthermore, the KMC simulation well predicts the transition from isolated NCs, obtained through the nucleation and growth, towards a network of connected particles, obtained through the spinodal decomposition of a highly supersaturated matrix.

Besides extensive fundamental research, e.g., on quantum confinement of charge carriers or on effects in structural phase transitions, semiconducting NPs exhibit promising applications as well as large technological potential: (1) for opto- and

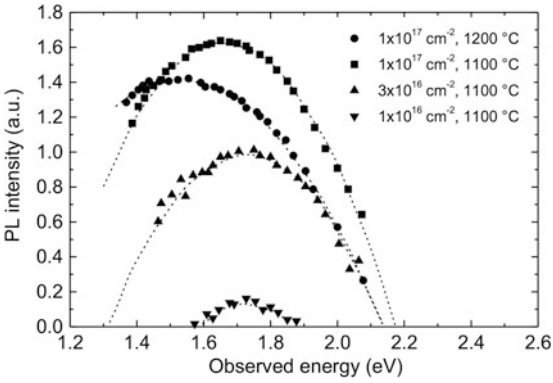

Fig. 4.55 PL spectra from Si NPs in a 100 nm SiO_2 layer implanted with 40 keV Si^+ ions at given fluences and annealed at indicated temperatures (1 h, for 3×10^{16} cm^{-2} 5 h). The PL was excited by irradiation of the samples at a wavelength of $\lambda = 355$ nm [280]

electro-luminescence from Si and Ge NCs in SiO_2 the understanding and controlling of their microstructure seems to be vital for a tailoring of efficient devices [272, 273], and (2) within the challenges of miniaturization in microelectronics the promising use of Si (and Ge) NPs in nonvolatile memories [274] and even as single-electron transistors [275].

Typically, for Si-NPs, the photoluminescence (PL) and electroluminescence (EL) spectra extend from 600 to 1,000 nm. The effects on the luminescence spectrum of the NP density, size and distribution, annealing temperature and time, ion fluence, and the sample temperature during implantation have been extensively studied. Most investigations on IBS of Si NPs report a PL peak at around 1.7 eV (728 nm). The often reported blue–violet PL in the region of (2.7–3.2) eV in Si^+-, Ge^+-, and Sn^+-implanted SiO_2 appears to come from oxygen deficiency centers in the implanted SiO_2 matrix or at the interface between NPs and SiO_2 rather than the NPs themselves [273]. The position of the luminescence peak at around 1.7 eV appears to be dependent on the implanted fluence of silicon [272, 276–278], with a red shift in PL peak position generally with an increasing fluence and depends on the experimental conditions. The highest PL peak intensity has been reported for implanted SiO_2 with an excess Si content of ~10 at.% Si [276, 277]. For SiO_2 containing 10 at.% Si, the PL intensity initially increases with annealing time, after which it saturates. During the initial stages of annealing, among Si NP growth some kind of NP surface passivation takes place [279]. Reaching a critical radius during annealing the Si NP size stabilizes, as does the number of dangling bonds at the Si/SiO_2 interface. Furthermore, it was found that a second annealing step at 500 °C in forming gas (95 % N_2, 5 % H_2) results in an increase in PL intensity and a red shift in the emission peak. This increase in PL intensity may be a result of the passivation of nonradiative defects by hydrogen (e.g., Si dangling bonds) [278]. For example, a typical PL spectrum from Si NPs in thermally grown SiO_2 on silicon is shown in Fig. 4.55 [280].

The PL spectrum in Fig. 4.55 was obtained from 100 nm thick SiO_2 layers implanted with fluences from 1×0^{16} cm^{-2} to 1×10^{17} cm^{-2} of Si^+ ions at 40 keV corresponding to a silicon excess between 2 and 25 at.% at a depth $R_p \approx 60$ nm in

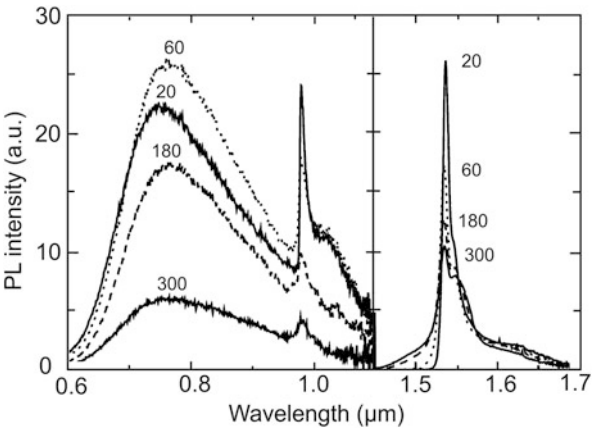

Fig. 4.56 PL spectra at different temperatures (in K) showing a broad Si NP spectrum in the wavelength region of 600–1,100 nm, and two sharp Er luminescence lines at 982 and 1,536 nm. The Er concentration was 1.8 at.%. The PL was excited at $\lambda = 458$ nm with a pump power of 1 mW [283]

the SiO_2 layer. The annealing was carried out at 1,000, 1,100, and 1,200 °C for 0.5–5 h in dry N_2.

Recently, it was shown that if additionally Er^+ ions are implanted into silicon dioxide containing Si NPs fabricated by IBS room temperature, photoluminescence (and electroluminescence) at near-infrared wavelength of $\lambda = 1.54$ μm is observed [281–283]. The PL (EL) shown in Fig. 4.56 is of interest because Erbium-doped optical amplifiers are important components in optical telecommunication because the optical transition of Er^{3+} at 1.54 μm is in the region of optimum transmission of silica-based glass fibers.

The Er and Si NP doped SiO_2 was fabricated by Si^+ ion implantation at 35 keV with a fluence of 6×10^{16} cm^{-2} into a 100-nm-thick thermally grown SiO_2 layer and by subsequent annealing at 1,100 °C for 10 min in vacuum resulting in Si NPs with sizes in the range 2–5 nm and a concentration of ~10^{19} cm^{-3}. The Si NP doped SiO_2 was then implanted with 125 keV Er^+ ions and a fluence of 5.1×10^{15} cm^{-2}. The peak of the implanted Er profile with a peak concentration of 1.8 at.% is located at a depth of ≈ 50 nm which coincide with the maximum of the Si NP depth distribution. Vacuum annealing at 1,000 °C was carried out to remove Er^+ implantation-induced damage. At least the samples were annealed at 800 °C for 30 min in forming gas (N_2 + H_2) to reduce defect-related luminescence. It was shown that at 1.8 at.% Er concentration the Er/Si NP ratio ≈100:1. Nevertheless, the observed maximum excitable Er concentration was only ≈(1–2) $\times$ 10^{19} cm^{-3} and therefore in the order of the Si NP volume concentration, which means that a single Si NP can effectively excite only ~1–2 Er ions. The model proposed by Polman [284] suggests that strong coupling between the Si NPs and the implanted Er atoms (existing as ionized Er^{3+} in SiO_2) effectively enables the Si NPs to pump the Er. The excitation cross section of the Er increases in the presence of Si NPs compared to Er excitation in the pure SiO_2. In the presence of a Si NP, the

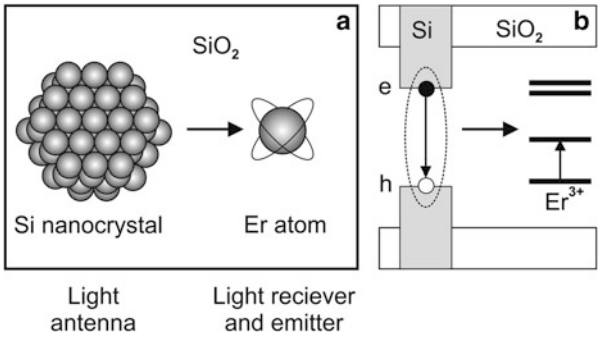

Fig. 4.57 Schematic Er excitation model, showing (**a**) a Si NP and an Er^{3+} ion embedded in SiO_2, and (**b**) the electronic band structure of Si NP doped SiO_2 and the Er energy levels (adapted from [284])

wavefunction of an electron–hole pair ("exciton") in a Si NP can couple to a nearby Er^{3+} at a distance of ~1 nm in SiO_2, as shown schematically in Fig. 4.57a.

An optically generated exciton (dotted line) confined in the Si NP will recombine nonradiatively and excite Er^{3+} from the ground state to the first excited state (Fig. 4.57b). The excited Er ions radiatively decay emitting photons at a wavelength of $\lambda = 1.536$ μm as shown in Fig. 4.56. Silica-based materials containing Si NPs and Er synthesized by ion beams enable the fabrication of a new class of miniature waveguide amplifiers as proposed by Polman [284].

More information about device applications of Si NPs and toward their microelectronic chip-based uses, the reader can find in the two books of Koshida [285] and Pavesi and Turan [286]. In these books alternative fabrication techniques for Si NPs are also described, namely plasma-enhanced chemical vapor deposition (PECVD) and physical vapor deposition (PVD) by sputtering or evaporation producing substoichiometric (or Si-rich) SiO_x (with $x < 2$) layers.

In microelectronics memory architectures charge storage devices for high-density, low-voltage, low-power, and fast write/erase data storage are needed to meet the International Technology Roadmap for Semiconductors (ITRS) requirements in the future. At present, two types of charge trapping memories are used: the polysilicon-blocking oxide–nitride-tunneling oxide-silicon (SONOS) memory, including the nitride read-only memory (NROM), and the nanocrystal floating-gate memory as proposed by Tiwari et al. [274]. A nanocrystal floating-gate memory consists of single-transistor memory-cell structures in which the conventional poly-Si floating-gate (FG) is replaced by Si NPs as isolated charge trapping centers as shown in Fig. 4.58.

The main advantage of the Si nanocrystal-based multidot floating gate memory is, however, the isolation of the Si NPs from each other that allows to reduce reliability constraints arising from charge leakage and hence improving reliability. As shown in Fig. 4.58a,b possible conduction paths originating from oxide defects, either process or operation related, have only a very local effect and cannot lead to a complete discharging of the distributed NC floating gate layer. As a result, the injection oxide thickness between the NPs and the transistor channel can be reduced to <5 nm. At these distances, electrons can tunnel by direct electron tunneling at

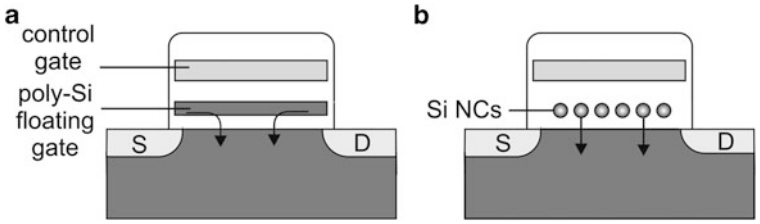

Fig. 4.58 Schematic buildup of (**a**) a poly-Si floating-gate memory cell, and (**b**) a nanocrystal floating-gate memory cell

Table 4.5 Implantation and annealing conditions at Si NP synthesis in thin gate oxides for memory applications

IBS process parameters	Values
SiO_2 thickness (nm)	5–30
Si^+ ion energy (keV)	1–15
Si^+ ion fluence (cm^{-2})	5×10^{15}–5×10^{16}
Si excess at implanted profile peak (at.%)	10–50
Annealing temperature (°C)	950–1,150
Annealing time (min)	0.5–30
Annealing ambient	N_2, $N_2 + O_2$, Ar, vacuum

low gate voltages into the Si NPs. Thicker injection oxides would require charging by defect generating Fowler–Nordheim tunneling (hot electron injection) at higher gate voltages. The last processes are known to limit the memory endurance upon repeated write and erase cycles which is not the case for direct tunneling.

IBS by low energy ion implantation into thin gate oxides allows the formation of a multidot floating gate layer made of Si NCs at a location from the SiO_2/Si interface (transistor channel) that can be tailored for DRAM-like (volatile) or EEPROM-like (nonvolatile) memory applications. Typical implantation and annealing conditions for the formation of Si NP containing gate oxides are summarized in Table 4.5.

Using very low ion energies of $E < 5$ keV (typically 1 keV) promises several advantages for the fabrication of Si NP memories: (1) Shallow and narrow depth profiles of Si excess are achieved. Phase separation is expected to result in a thin layer of Si NCs embedded in the SiO_2. (2) The depth position of the NC layer should be easily controllable by the ion energy and the total amount of Si contained in the NPs by the ion fluence, while the annealing temperature determines the mean NC size. (3) Little ion damage at the SiO_2/Si interface is expected due to the low ion energy; irradiation damage created within the SiO_2 is largely recovered during annealing. The ion energy at Si NP synthesis is one of the critical parameters in relation with the thickness of the gate oxide because after full processing the injection distance between the Si NC layer and the transistor channel can be too small preventing true nonvolatile memory operation. In this case only a DRAM-like

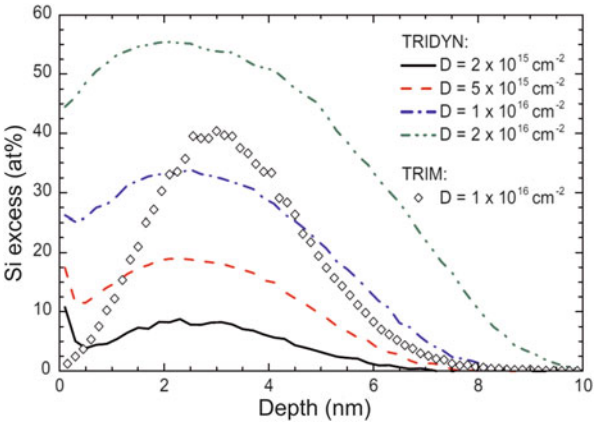

Fig. 4.59 Depth profiles of Si excess for 1 keV Si^+ implantation into SiO_2 calculated by TRIDYN in comparison with TRIM [270]

volatile memory transistor operation with fast programming and erasing at low electric fields (write/erase voltage $<+10$ V/-10 V), which ensures a high endurance, will be possible. The formation of well depth-localized layers of Si (and Ge) NPs for different implantation and annealing conditions given in Table 4.5 and their applications in nonvolatile (EEPROM-like) memory devices has been successfully achieved [287–291].

For a typical example of Si NP synthesis by ion implantation into thin (<10 nm) gate oxide, Fig. 4.59 shows the Si excess depth profiles for 1 keV Si^+ implantation. The ion fluence increases from 1×10^{15} cm^{-2} up to 2×10^{16} cm^{-2}.

As can be seen the Si excess increases for higher Si^+ ion fluences, while the profile broadens considerably due to ion beam mixing, sputtering, and swelling. The slight Si enrichment at the target surface is observed as the result of preferential O sputtering. For comparison, a Si implantation profile calculated by TRIM has been added to Fig. 4.59, which is much sharper than the corresponding TRIDYN profile. Accordingly, the Si peak concentration is significantly overestimated by TRIM and the profile broadening observed by TRIDYN calculations cannot be described by TRIM. Therefore, TRIDYN simulations are required to predict a correct profile for high-fluence implantation. With the given initial Si excess distribution phase separation can be modeled by KMC simulations the result of which is shown in Fig. 4.60.

The Si atoms in Fig. 4.60 are colored according their coordination to other Si atoms. The red color corresponds to atoms with no bonds to neighboring Si excess atoms, while blue indicates fully coordinated atoms. The first chart on the left-hand side depicts the as-implanted SiO_2. The Si excess atoms are dispersed in the oxide with a distribution tail reaching almost up to the SiO_2/Si interface. Bonds between neighboring Si atoms have not yet formed (indicated by the red color). In the first stage of annealing, small Si NCs form rapidly and are visible as tiny (green) dots. With increasing annealing time the NC density visibly decreases and the average

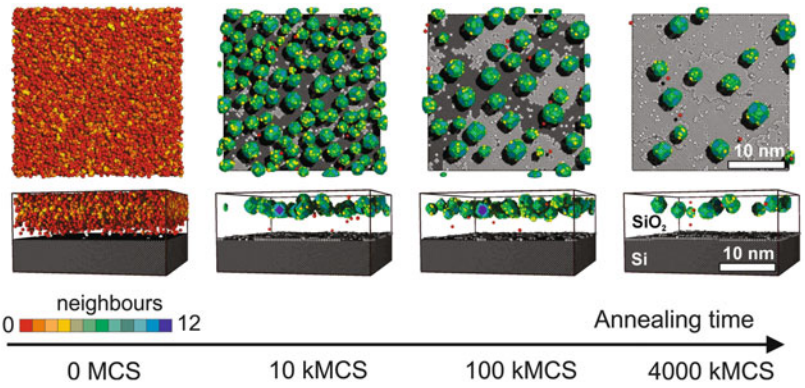

Fig. 4.60 Results of a KMC simulation (*top view* and *cross sections*) for 1 keV Si^+ implantation into 8 nm thick SiO_2 on silicon. At a fluence of 2×10^{15} cm^{-2}, Si NCs form during annealing and dissolve with increasing annealing time due to Si loss to the absorbing SiO_2/Si interface [270]

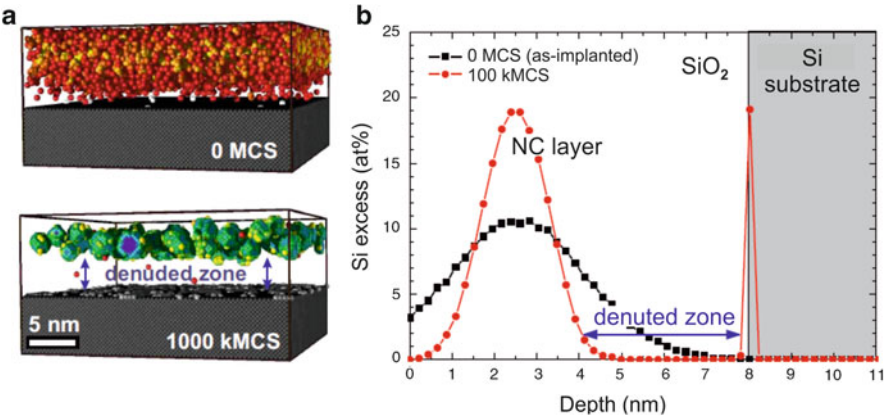

Fig. 4.61 Formation of a denuded zone free of NC at the SiO_2/Si interface during phase separation as predicted by KMC simulations. (**a**) Two KMC simulation snapshots (*cross section view*) are shown for 1 keV Si^+ implantation into 8 nm thick SiO_2 to a fluence of 2×10^{15} cm^{-2}. The first one refers to the as-implanted case while the second was taken after 100 kMCS. (**b**) Corresponding Si excess depth profiles

size of the NCs increases. This behavior of phase separation is important for NC size and density control in fabrication of nonvolatile NC memories. Finally, long-lasting annealing (right chart) leads to a considerable amount of Si loss to the absorbing SiO_2/Si interface. Si atoms attached there are colored in light gray, and it is apparent that a complete Si monolayer has grown epitaxially onto the silicon substrate. The SiO_2/Si interface acts as a strong sink for diffusing Si atoms, and therefore leads to a NC-depleted zone parallel to the interface as shown in Fig. 4.61. This denuded zone will serve as tunneling oxide in the NC memory and isolates the NC from the transistor channel.

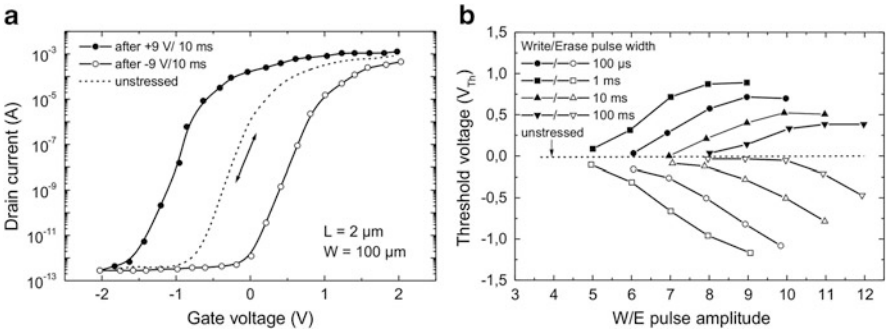

Fig. 4.62 (**a**) Transfer characteristic for Si NP floating-gate nMOS transistor. (**b**) Threshold voltage shift versus write/erase voltages for different pulse durations [289, 290]

At charge injection during the write pulse, electrons have to overcome the barrier by Fowler–Nordheim tunneling or by quantum mechanical direct electron tunneling. In both cases, the width of the injection oxide critically determines the memory properties as writing speed required for charging of the NCs and charge retention. The ion energy and oxide thickness can directly be used to control the distance between Si NCs and the Si/SiO_2 interface. Furthermore, the width of the denuded zone is influenced by the annealing time. For the nonvolatility Si NC memory under normal read and retention conditions, the thickness of the injection oxide has to remain larger than 4 nm [292, 293]. In order to accomplish this target, Si NC n-channel MOSFETs have been fabricated using 1 keV Si^+ implantation to a fluence of 2×10^{16} cm^{-2} into 7 nm thick SiO_2. Subsequent annealing has been done in diluted O_2 atmosphere (N_2/O_2) at 950 °C for 30 min. Swelling due to oxidation has lead to a total oxide thickness of 14 nm. A typical transfer characteristic (drain current I_D versus gate voltage V_G) of such a transistor is shown in Fig. 4.62a.

The threshold voltage shift V_{th} resulting from applied write/erase pulses is plotted in Fig. 4.62b as a function of the pulse amplitude. At 100 ms pulse duration, write/erase pulse amplitudes of ±6 V are high enough to achieve a threshold voltage shift of +0.5 and −0.25 V, respectively. However, shorter pulses require progressively higher write and erase voltages. At 100 µs more than 10 V must be applied to get comparable threshold voltage shifts. Endurance measurements plotted in Fig. 4.63a do not indicate a degradation of the tunneling oxide at this voltage after 10^6 write and erase cycles, and the threshold voltage window does not close after more than 10^4 s waiting time (see Fig. 4.63b), i.e., negligible charge is lost during this period.

However, temperature activated retention measurements reveal a much faster charge loss at elevated temperatures (150 °C), which is not observed in competing memory technologies, e.g., in SONOS type memories using either Si_3N_4 or oxynitrides as a charge trapping layer.

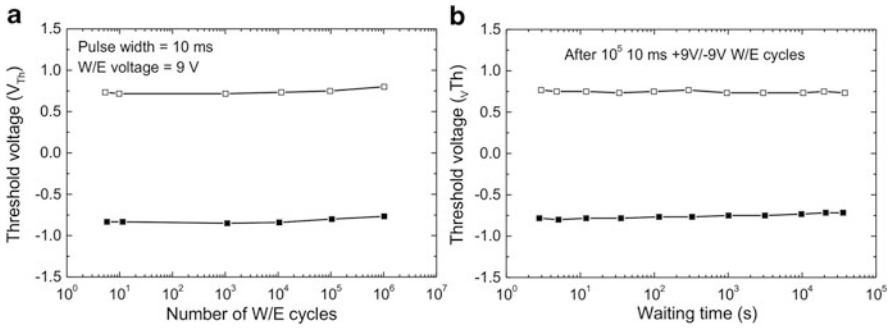

Fig. 4.63 (**a**) Endurance and (**b**) data retention characteristics of a Si NP floating-gate nMOS transistor. The endurance was measured using +9/−9 V write/erase pulses of 10 μs duration. The charge retention has been measured at room temperature after 10^5 write/erase cycles [289, 290]

Low energy IBS of Si NCs in thin gate oxides seems to be a simple technique being advantageous over more complex SiO_x deposition approaches (e.g., CVD). In principle the NC synthesis can be tuned with four process parameters only: the ion fluence Φ and ion energy E controlling the buildup of a supersaturated solid solution of excess Si in the SiO_2 and the annealing time t_A and annealing temperature T_A affecting the NC phase separation. Unfortunately, the situation is much more complex and additional process parameters influence the Si NC formation at low energy IBS. Some of these factors are:

- *Charge neutralization*, which is necessary to prevent a charge buildup at the isolating SiO_2 surface and charge breakdowns through the thin oxide (oxide damage) during implantation [294]
- *Contamination of the SiO_2 by impurities* (e.g., carbon or boron) during ion implantation, sputtered from the mechanical implanter parts or coming from the residual gas atmosphere [290]
- *Absorption of humidity* in the ion-damaged SiO_2 after the sample has been exposed to air [268]
- *Wafer cleaning* (standard RCA and Piranha wet cleaning) affecting the topmost SiO_2 [290]
- *Partial oxidation of implanted Si* during annealing either by residual humidity from the annealing ambient or by humidity that has penetrated before into the damaged oxide [268, 290]
- *Oxide swelling*, which appears after low energy IBS. It could result from various effects such as ion sputtering (negative swelling), incorporation of implanted material, Si oxidation, changed SiO_2 density, or defect creation [290, 295]
- *Reactive annealing ambient* (e.g., N_2/O_2 mixture), which reduces the amount of implanted Si by oxidation but on the other hand improves electrical properties due to the better curing of oxide defects [288]

Irradiation-based concepts for synthesis of Si NCs based on ion beam mixing of interfaces [296] could deliver in particular an alternative to low energy IBS that eliminates external influences on the NC formation at phase separation. For that

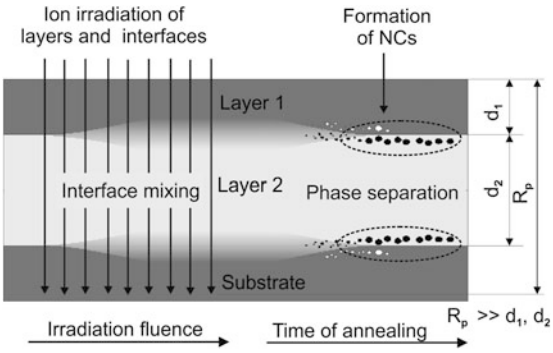

Fig. 4.64 Scheme of ion beam-induced self-alignment of a NC δ-layer near a layer/substrate interface by ion irradiation through the interface and subsequent thermal treatment leading to the phase separation in the ion mixed nonstoichiometric near-interface layer through precipitation and Ostwald ripening of NCs

purpose, the complete transistor gate stack (gate oxide and poly-Si gate electrode) is irradiated by Si ions and will be described in the following chapter.

4.4 Ion Beam Mixing of Interfaces

Although there are possibilities to tailor the mean NC size (mainly by variation of ion fluence, annealing temperature, and time) at conventional IBS, the possibilities for tailoring the NC size distribution by the variation of ion implantation parameters are rather limited. Ion irradiation not only causes supersaturation and damage to the substrate but also affects the interface between a thin layer and the substrate or interfaces between thin stacked layers. As schematically shown in Fig. 4.64 primary energetic ions produce collisional cascades which cause substantial interface mixing leading to nonstoichiometric and nonstable phases near the interface.

Subsequent annealing restores the interface region rapidly via spinodal decomposition. However, the tails of the mixing profiles do not reach the recovered interfaces by diffusion, thus, phase separation proceeds via nucleation and growth of NCs near the interface. The competition between interface restoration and nucleation self-aligns nearly monodispersive δ-layers of NCs in proximity to the interface. Self-organization of a δ-layer of Ge NCs in SiO_2 has been found [262, 297] close to the Si/SiO_2 interface after appropriate Ge^+ implantation into a SiO_2 layer on a Si substrate. The NC δ-layers were found when the following conditions were fulfilled: (1) a negligibly small amount of ions is implanted in the Si/SiO_2 interface region, and (2) the cascade of energetic O and Si recoils produced by primary collisions initiate a few displacements per atom (dpa) in the Si/SiO_2 region. Different contributions to the self-organization of NC δ-layers have been described and investigated by kinetic MC simulations and reaction–diffusion equations [298]. As an example, the positioning of a Ge-NC δ-layer near the SiO_2/Si interface without Ge^+ implantation into this region is shown in Fig. 4.65. The Ge^+ implantation ($E = 350$ keV, $D = 5 \times 10^{16}$ cm^{-2}) into a 500 nm thick SiO_2 layer was carried out in such a way that the maximum of the implanted profile ($R_p = 211$ nm)

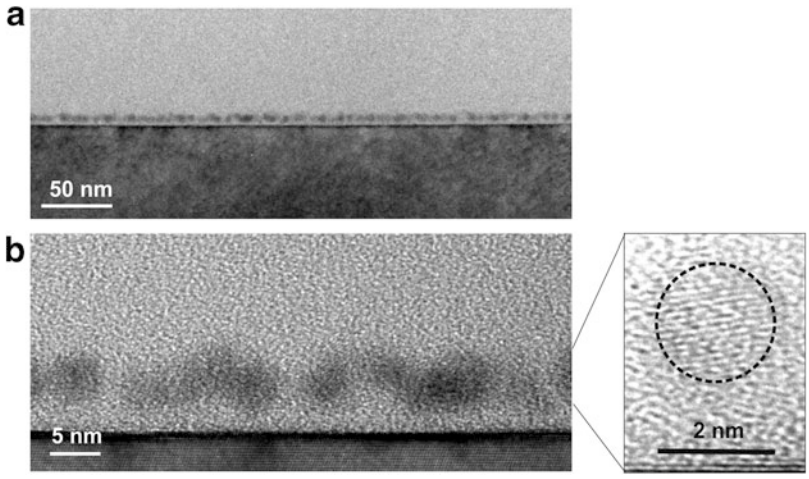

Fig. 4.65 Formation of NCs at flat interfaces under ion irradiation: (**a**) XTEM image overview of a Ge NC δ-layer next to the SiO_2/Si interface; (**b**) HRTEM cross-sectional image of an individual Ge NC with resolved <111> crystal lattice planes of the nanocrystal

is located far away from the SiO_2/Si interface. The Ge concentration in the tail of the implanted profile reaching the interface is below 0.5 at.% and can be neglected.

After annealing of this sample no Ge NCs have been observed near the interface. Ion irradiation (Si^+, $E = 450$ keV, $D = 5 \times 10^{15}$ cm^{-2}, $R_p \approx 720$ nm) through the SiO_2/Si interface before or after Ge^+ implantation in SiO_2 induces a self-aligned δ-layer of Ge NCs as shown in Fig. 4.65. In the ion mixed nonstoichiometric SiO_x ($x < 2$) layer during annealing (1,000 °C, 1 h), tiny Si precipitates form to which Ge atoms attach during diffusion towards the Si substrate. The miscible Ge/Si precipitates grow with increasing annealing time forming nearly pure Ge NCs with a denuded zone of ~3 nm in between the NC layer and the substrate.

Ion irradiation not only affects flat interfaces but also curved interfaces of embedded NCs [298–300]. Thus, NC atoms can be mixed out by recoils of collisional cascades into the surrounding matrix. If these atoms are mobile in the host matrix, their steady state concentration is given by the detailed balance of detachment and attachment processes at the NC interface. The attachment of impurity atoms at the NC interface is mainly a thermally activated process whereas detachment of atoms from NCs can be thermally activated or caused by displacements of the collisional cascade. At higher irradiation temperature, the thermally activated detachment dominates and at low-temperature detachment of NC atoms becomes temperature independent, i.e., detachments are governed by ion beam mixing. An analytical model of the steady state of a NC under ion irradiation, which includes ion beam mixing at interfaces of NCs and impurity diffusion in the host matrix was developed and checked using kinetic lattice Monte Carlo simulations by Heinig et al. [298]. Based on this model a new method of re-assembling of a given NC size distribution using ion-induced "inverse Ostwald

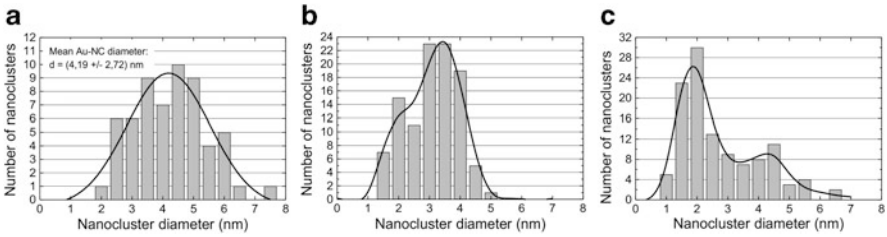

Fig. 4.66 Evolution of the size distribution of Au NCs formed by 330 keV Au^+ implantation with a fluence of 2×10^{16} cm^{-2} and annealing at 1,000 °C for 1 h in dry O_2 (**a**), under subsequent 4.5 MeV Au^+ irradiation of 5×10^{15} cm^{-2} at 190 °C target temperature (**b**), and 1×10^{16} cm^{-2} at 200 °C target temperature (**c**)

ripening" (IOR) was predicted, which should allow even the formation of monodispersive NC distributions. An experiment has been performed [300] in order to prove the predictions for IOR. In a 480 nm thick SiO_2 layer, Au NCs were synthesized by Au^+ implantation ($E = 330$ keV, $\Phi = 2 \times 10^{16}$ cm^{-2}, $R_p = 102$ nm) and subsequent annealing at 1,000 °C for 1 h in dry oxygen. The evaluation of high resolution XTEM images showed that the mean NC diameter d_{NC} in the depth region ($R_p \pm 15$ nm) was 4.2 nm with a FWHM of 2.7 nm (Fig. 4.66a).

The same sample was after it irradiated with 4.5 MeV Au^+ ions at 200 °C with a flux density of 3.9×10^{11} $cm^{-2}s^{-1}$ to study the evolution of the initial NC size distribution under ion irradiation. 4.5 MeV Au^+ ions had a projected range of $R_p = 1.06$ μm and they came to rest deep in the Si substrate, i.e., no Au^+ ions were deposited in the region of the initial Au NC depth distribution. The mean size of Au NCs decreases with increasing fluence of 5×10^{15} cm^{-2} and 10×10^{15} cm^{-2} (see Fig. 4.66b, c, respectively). Furthermore, an increase of the NC density and a decrease of the width of the size distribution with increasing ion fluence were found. This experimental result is in good agreement with theoretical predictions. A quantitative comparison fails due to the lack of reliable values of diffusivity and solubility of Au in SiO_2.

The approach for ion irradiation induced self-alignment of Si NCs near SiO_2/Si interfaces also has been applied to the fabrication of nonvolatile multidot floating gate memory devices [296]. For this application a MOS-like Si/SiO_2/Si structure was selected and submitted to Si^+ ion irradiation to mix the interfaces of this layer stack. Thus, sandwiched between the stable phases of SiO_2 and Si, unstable nonstoichiometric SiO_x ($x < 2$) phases are formed. Annealing restores the upper and lower SiO_2/Si interfaces by spinodal decomposition. However, the tails of the Si atom mixing profiles do not reach the recovered interfaces by diffusion, thus, phase separation proceeds via nucleation and growth of Si NCs in SiO_2. The competition between interface restoration and nucleation self-aligns δ-layers of Si NCs in SiO_2 along the two interfaces. This self-alignment of δ-layers of Si NCs with the SiO_2/Si interfaces has been predicted by atomistic computer simulations [301] and is shown in Fig. 4.67.

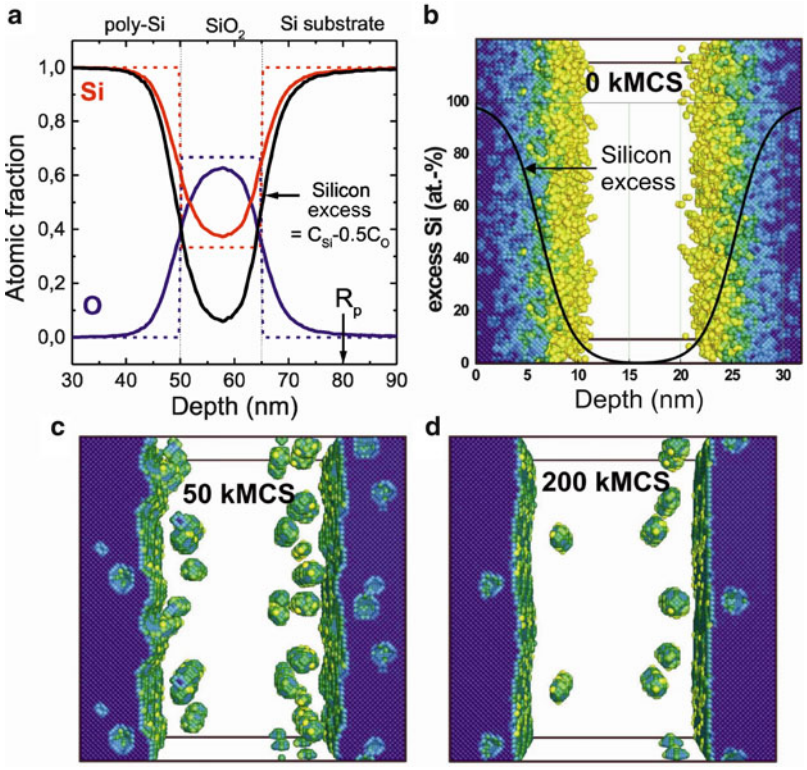

Fig. 4.67 Self-aligned Si NC formation by ion irradiation of SiO_2/Si interfaces: (**a**) TRIDYN results of Si ion irradiation ($E = 50$ keV, $\Phi = 1 \times 10^{16}$ cm^{-2}) through a layer stack of 50 nm poly-Si, 15 nm SiO_2, into the Si substrate. KLMC simulation snapshots referring (**b**) to the as-irradiated state, (**c**) to the early state of phase separation, and (**d**) to a later stage

As shown in Fig. 4.67 the Si precipitates in SiO_2 have developed to Si NC δ-layers which are aligned with the SiO_2/Si interfaces. The mean Si NC diameter is 2 nm and the mean distance from the interfaces is 2 nm, too. In each δ-layers, the Si NC areal density is in the order of 10^{12} cm^{-2}. This prediction has been verified experimentally by energy filtered transmission electron microscopy (EFTEM) [302]. As can be seen in Fig. 4.68, bright and dark areas are visible in dark and white regions of the SiO_2 layer, respectively.

These spherical regions refer to Si NCs in the oxide. Accordingly, the Si NCs are separated from the SiO_2/Si interfaces by a mean distance of 3 nm, i.e., they are aligned in a δ-layer at each interface. The mean diameter of the NCs was estimated to be 3 nm. These morphological features are in accordance with the KLMC simulation predictions from [301].

For memory device fabrication, the ion irradiation-based concept for synthesis of Si NCs experiments was carried out on 150 mm (100)Si wafers covered with a 15 nm thermally grown SiO_2 layer and a 50 nm poly-Si layer deposited by LPCVD

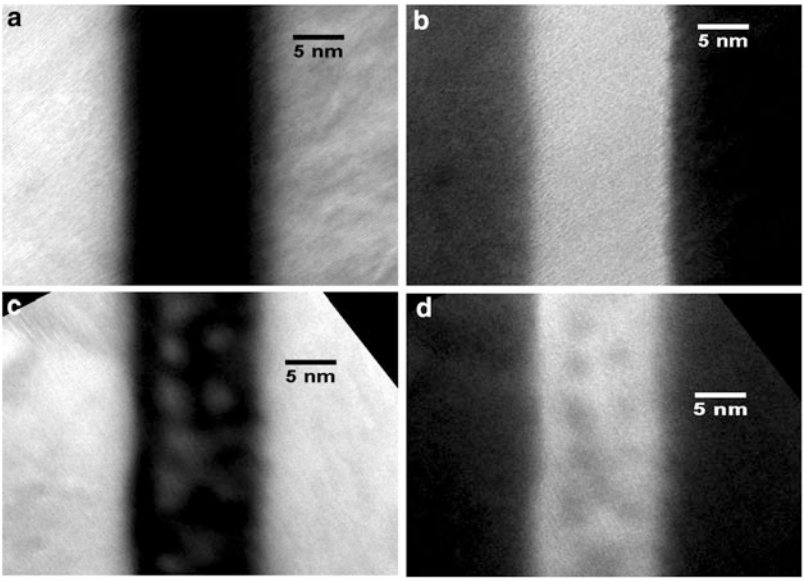

Fig. 4.68 Energy-filtered (X)TEM images of the poly-Si/SiO_2/Si structure: (**a**, **b**) referring to the as-deposited state and (**c**, **d**) after Si^+ ion irradiation ($E = 50$ keV, $\Phi = 7 \times 10^{15}$ cm^{-2}) and postirradiation annealing ($T = 1{,}050$ °C, $t = 120$ s) [302]. In EFTEM images (a,c) recorded with electrons of an energy loss between 14 and 18 eV the Si substrate and the poly-Si layer appear bright – in contrast to dark SiO_2 regions. For an energy loss window between 20 and 36 eV, the Si substrate and the poly-Si layer appear dark, the SiO_2 regions however bright (b,d).

on top of the SiO_2 layer. The upper poly-Si layer was used as a capping layer to prevent any influence of contaminants from ambient and annealing atmosphere (mainly humidity) on the NC formation process in the thin gate oxide [268]. The poly-Si/SiO_2/Si stack was irradiated with 50 keV Si^+ ions at fluences in the range of 3×10^{15}–1×10^{16} cm^{-2}. After ion irradiation a highly n^+-doped and 250 nm thick poly-Si gate was deposited onto the irradiated stack. Subsequently, the samples were annealed (RTA) at different temperatures (950–1,100 °C) and times (5–180 s) and further processed for the fabrication of n-channel MOSFETs in a standard 0.6 μm CMOS process line. Electrical measurements of memory properties show that devices exhibit significant memory windows at low gate voltages. Devices with a memory window of about 0.5 V for write/erase voltages of –7 V/+7 V and a programming time of $t_{pp} = 10$ ms have been achieved. In terms of memory window and transistor characteristics, an ion irradiation fluence of (5–7) $\times 10^{15}$ Si^+ cm^{-2} and annealing at $T_A = 1{,}050$ °C for $t_A = 30$ s appear as promising conditions for devices fabrication (see Fig. 4.69a). The memory window can be increased by annealing at higher temperatures ($T = 1{,}100$ °C) and/or for longer times (>120 s) proceeding to further phase separation Si NC formation. As shown in Fig. 4.69b, in this case a large stable memory window of $\Delta V_{th} \sim 3$ V can be achieved.

No degradation in memory windows was observed for NC memory devices after 10^7 write/erase cycles with $V_{pp} = +7$ V/−7 V, $t_{pp} = 1$ ms programming conditions

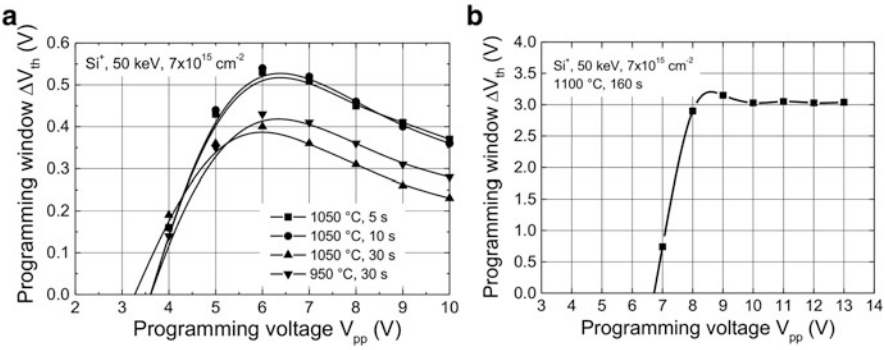

Fig. 4.69 Memory window ΔV_{th} versus programming voltage V_{pp} (pulse length $t_{pp} = 10$ ms) of n-channel MOSFETs with self-aligned Si NCs in the gate oxide. Si^+ irradiation was performed at an ion energy of 50 keV and a fluence of 7×10^{15} cm^{-2}: (**a**) for low thermal budget at different RTA annealing parameters; (**b**) for high thermal budget and annealing at $T = 1{,}100$ °C for 160 s

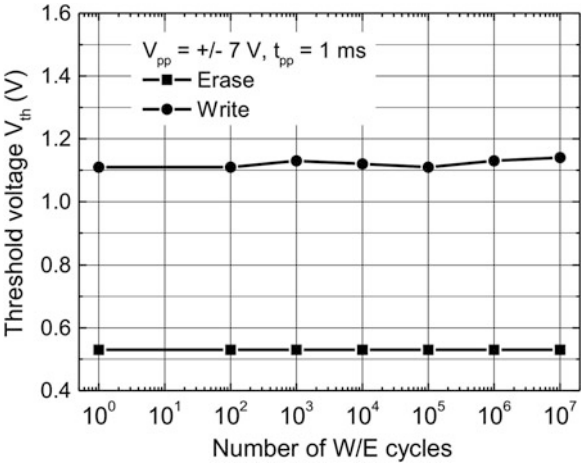

Fig. 4.70 Endurance characteristics of nMOSFETs obtained with write/erase voltages of $V_{pp} = \pm 7$ V and pulses of $t_{pp} = 1$ ms. The sample was irradiated with 50 keV Si^+ ions at a fluence of 7×10^{15} cm^{-2} and annealed at 1,050 °C for 30 s

(Fig. 4.70), which means that the fabricated memory devices exhibit a superior endurance. It was found that data retention time tested at 85 °C is too low for EEPROM application (100 days at room temperature and 8 h at 85 °C). The fabricated nMOS devices exhibit maximum memory windows at low gate voltages indicating that the charge storage nodes are located near to the Si/SiO_2 interface. This implies the possibility of direct charge carrier tunneling into Si NCs during low programming voltages. The lowering of the programming window at programming voltages $V_{pp} > 6$ V (Fig. 4.69a) can be explained by trap-assisted tunneling

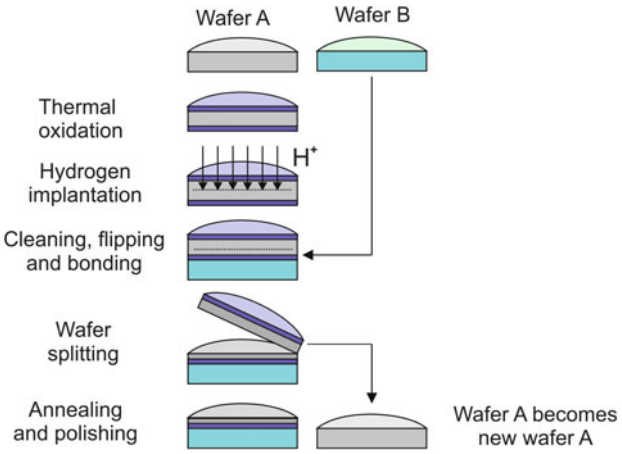

Fig. 4.71 Schematic process flow of SOI wafer fabrication by Smart Cut based on hydrogen implantation, wafer bonding, layer splitting, and final wafer polishing. Wafer A can be reused as substrate for SOI processing

through the gate insulator. Besides retention, all electric parameters of the devices fulfill current requirements to nonvolatile memory devices. The low data retention might be explained by direct re-tunneling of charge carriers to the channel which could be a common problem of multidot floating-gate memories.

4.5 Ion Beam Slicing of Thin Layers (Smart-Cut for SOI and Solar Cells)

High fluence of inert gases or hydrogen can be used for exfoliation of thin layers of crystalline materials to be placed on any kind of substrates (dielectric, glass, plastic, quartz, amorphous silicon, crystalline semiconductor, etc.). This technology, called "Smart Cut" (or Ion Cut), was developed at LETI Laboratories, Grenoble, France, in 1991 and involves the implantation of H^+ ions into silicon. Among the SIMOX process (see Sect. 4.3.1) the Smart Cut process is mostly used for SOI wafers production. SOI wafers made by Smart Cut technology possess less defects in the top Si device layer compared to SOI wafers made by SIMOX. As shown in Fig. 4.71 the Smart Cut process is based on the principles of ion implantation and wafer bonding [303–305].

This process requires two starting silicon wafers (A—seed wafer and B—handle wafer) to produce the SOI wafer. The first step is the thermal oxidation of wafer A. The oxide layer with a thickness in the range of some tens of nanometer until some micrometer will become the buried oxide (BOX) in the final SOI wafer. High-fluence ion implantation of light ions (H^+, He^+) through the SiO_2 into the underlying silicon substrate forms a damaged layer at and around the projected ion range

R_p. After that wafer A is bonded to wafer B, forming the substrate of the final SOI wafer. The bonded wafer pair is subsequently heated so that the wafers split along the gas-implanted plane. The removed portion of the wafer A will now become substrate for another smart cut wafer. The Smart Cut SOI wafer is now annealed at high temperature, after that polished and ready for device processing. The main process parameters are the following:

- High-fluence ion implantation (H^+) through the SiO_2 layer forms the layer for later cutting. The ion fluence is in the range of 3.5×10^{16}–1×10^{17} cm^{-2}. At this stage microcavities or micro bubbles are formed at R_p, the size and density of which depend on the implanted fluence, implantation energy, fluence rate, and implantation temperature. The thickness of the Si layer to be splitted later can be tailored in the range from 0.1 μm up to 13.5 μm by selecting corresponding ion energies between 10 keV and 1 MeV, respectively.
- Hydrophilic bonding of the implanted wafer to a handle wafer (either bare or SiO_2 capped) at room temperature [306]. The handle wafer plays a key role as a stiffener and provides the bulk silicon under the BOX layer in the SOI structure. Before bonding the two wafers are cleaned by a modified RCA cleaning procedure to remove particles, contaminants, and to form hydrophilic surfaces on both wafers. The bonded wafer pair undergoes a heat treatment at ~200 °C to form a strong chemical bond at the bond interface between the wafers.
- Two-step thermal treatment of the joined wafer pair leads to splitting. The first annealing is carried out typically at 400–600 °C during which the implanted hydrogen ions diffuse within the implanted layer (defect-enhanced diffusion) forming H_2 gas bubbles of high internal pressure. The evolution of these bubbles proceeds via Ostwald ripening. Finally, with increasing annealing time the bubbles coalesce leading to crack propagation along the plane of the bubble network leaving a thin monocrystalline Si layer on the surface of the carrier wafer on top of the thermal grown SiO_2 layer. The subsequent high-temperature annealing step is typically performed at 1,100 °C for 2 h to remove any silanol groups from the bonding interface and to achieve a high quality SiO_2/Si interface.
- Final chemical mechanical polishing (CMP) of the Si top layer (about 50–100 nm) of the SOI structure is carried out to remove micro-roughness and surface defects. Standard parameters of the micro-roughness and the Si layer thickness uniformity are 0.15 nm (RMS) and ±10 nm, respectively [307]. For modern integrated circuit applications (e.g., processors), the thickness of the top Si device layer can be further reduced up to some tens of nanometer.

The defect formation during H^+ implantation and the coarsening (Ostwald ripening) of H_2 microcavities has been intensively investigated and is schematically illustrated in Fig. 4.72. It was shown by TEM investigations that the defective region of the implanted profile (mostly around R_p) contains small platelet-like microcavities with dimensions of about 10 nm long and about 1 nm thick. They appear mostly aligned parallel to the surface, i.e., in a (100)-oriented Si crystal lattice plane. After implantation, the nucleation stage of the cavities is not completed and, for example, at 500 °C an annealing time of ~5 min is required

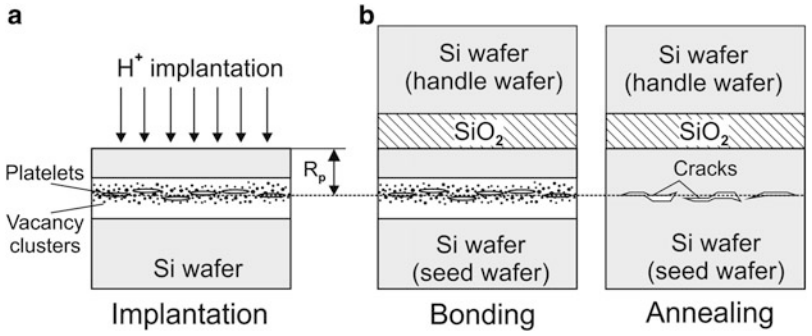

Fig. 4.72 (**a**) Formation of defects (vacancies, vacancy clusters) and H_2 filled microcavities/bubbles during H^+ implantation around R_p in the seed wafer. (**b**) Formation of crack network in the seed wafer during annealing of the bonded wafer pair

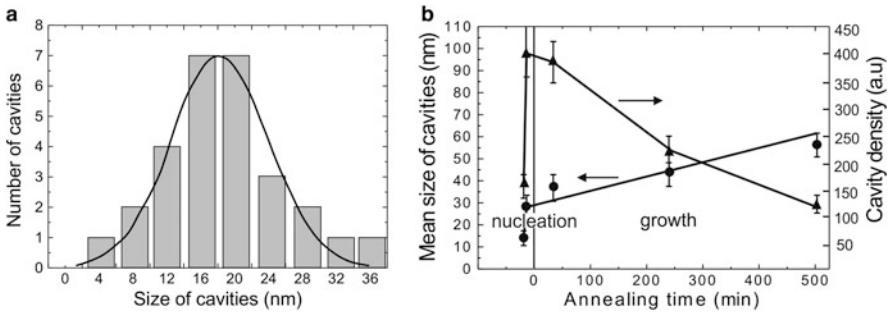

Fig. 4.73 Typical initial distribution of the cavity size (**a**) and (**b**) their evolution in size and density as a function of annealing time at $T_A = 500$ °C (taken from [304])

for coarsening of the cavities [304]. As usually observed in the Ostwald ripening stage, the microcavities grow in size and reduce in density, as shown in Fig. 4.73.

The splitting time has been experimentally measured and varies from a few seconds to some hours sensitively depending on the annealing temperature but also on implantation conditions (ion fluence and energy), Si material properties (doping concentration), and bonding parameters. Remarkably, two temperature ranges with different activation energies for splitting have been identified. In the high-temperature range ($T_A > 530$ °C), an activation energy of $E_a \approx 0.5$ eV is obtained which is comparable with the activation energy of 0.48 eV for atomic hydrogen diffusion in silicon. Therefore, it is assumed that in the high-temperature range splitting is controlled by H diffusion. In the low-temperature range ($T_A < 500$ °C), the activation energy is higher [$E_a = (2.2–2.5)$ eV] and assumed as the sum of two activation energies involving hydrogen diffusion (0.48 eV) and dissociation of Si–H bonds. The dissociation of Si–H bonds greatly depends on experimental conditions. The transition temperature between low- and high-temperature regimes was observed at ≈550 °C [308].

Table 4.6 Smart Cut wafer material properties and process parameters

Wafer parameter	Values
Wafer diameter	$\leq$300 mm
Si device layer thickness	50–100 nm
Si device layer thickness uniformity	$\pm$0.5 nm
BOX layer thickness	100 nm–3 μm
BOX layer thickness uniformity	$\pm$0.1 nm
Surface roughness	0.15 nm
Dislocation density	~100 cm^{-2}
BOX pipe (pinhole) areal density	Non
BOX dielectric electric field breakdown	$>5 \times 10^6$ V cm^{-1}
Implantation parameters	Standard Smart Cut
H^+ ion energy	20–200 keV
H^+ ion fluence	~5×10^{16} cm^{-2}
Implantation temperature	RT–350 °C
Annealing process	500 + 1,100 °C (N_2, Ar)

The thickness of the cleaved Si layer measured by cross-section SEM and TEM imaging is somewhat smaller than the depth R_p of the implanted H profile [309, 310]. As can be obtained from SRIM calculations, the maximum of the H concentration peak is somewhat deeper than the maximum of the damage profile which supports this observation. The results are consistent with the proposed mechanism of preferential H microcavity and bubble formation in the depth region where the highest concentration of defects (damage) is induced by the implantation process.

The Smart Cut process used for mass production significantly lowers the production costs of SOI wafer fabrication, since the H^+ (or He^+) ion fluence is one order of magnitude lower compared to oxygen fluence for SIMOX. The gas implantation can be carried out at room temperature using standard high current ion implantation tools. Compared to the SIMOX process, where high temperatures of $T_A > 1{,}200$ °C and special annealing tools are necessary, at Smart Cut the heat treatment for wafer splitting proceeds in standard furnaces. The material properties for standard Smart Cut SOI wafers together with the corresponding process parameters of H^+ ion implantation for ULSI CMOS circuits are summarized in Table 4.6.

Due to the flexibility of the Smart Cut process it has been used, for example, in crystalline SiC structures which have enabled it to be bonded onto silicon substrate [311]. For other semiconductor materials, the process has been used successfully, for example in Ge [312], GaAs [313], GaN [314], InP [315], and in other materials, e.g., in ferroelectric $BaTiO_3$ (BTO) crystals [316].

The cutting process based on H^+ implantation exhibits an effective and economical method of transferring thin materials layers from bulk substrates onto another substrate material to achieve hetero-material integration. This advantage of the Smart Cut process recently became an interesting technology in the fabrication of thin film solar cells, where thin layers of high quality crystalline semiconductor

materials are transferred and bonded to glass and/or other photovoltaic materials (http://www.sigen.com). Nevertheless, the Smart Cut process has not yet been applied to solar cell mass production. The thickness of the transferred layer is defined by the penetration depth of the H^+ ions which for conventional microelectronic applications is typically <1 μm. Applying high-fluence, high energy implantation of H^+ ions in the energy range of (1–4) MeV, the exfoliation of silicon layers with thicknesses of (15–150) μm, respectively, will be possible. This thickness range represents the thickness gap between thin film solar cells (a-Si, a-Si/μc-Si, CIGS, typically <15 μm thick) and conventional single- or polycrystalline Si solar cells (typically >150 μm thick). The introduction of the Smart Cut process into solar cell fabrication requires electrostatic accelerators supplying H + ions in the MeV ion energy range, which are still too expensive for cost-effective production.

4.6 Ion Beam Erosion, Sputtering, and Surface Patterning (Ripples and Dots)

Surface patterning by ion beam erosion represents nanoscale surface morphologies spontaneously developing from uniform ion bombardment of an initially flat surface in a nonequilibrium self-organization process. Ion beam erosion is routinely used in surface analysis, depth profiling, surface cleaning, and micromachining [317]. Depending on the chemical–physical properties of the eroded substrates and the erosion conditions, it is possible to create ordered submicron, nanoscale surface features like dots and ripples. Highly ordered ripple and dot patterns are observed at erosion with different ions on the surfaces of various substrates, for example of crystalline semiconductors (e.g., Si, Ge, GaSb, and InP), amorphous glasses and thermally grown SiO_2, single-crystalline (e.g., Cu, Ag) and polycrystalline metals (e.g., Ag, Au, Pt). Some elected examples of patterned semiconductor and SiO_2 surfaces are shown in Fig. 4.74.

In Fig. 4.74a–c the direction of the incident ion beam is marked by the arrow. The ion irradiation conditions at off-normal beam direction in Fig. 4.74a–c were the following: (a) Kr^+ ions, $E = 1.2$ keV, $\Phi = 2.2 \times 10^{18}$ cm^{-2}, angle of incidence 15° with respect to the surface normal; (b) Xe^+ ions, $E = 2$ keV, $\Phi = 6.7 \times 10^{18}$ cm^{-2}, angle of incidence 5°; (c) Ar^+ ions, $E = 1$ keV, $\Phi = 1 \times 10^{18}$ cm^{-2}, angle of incidence 45°. In Fig. 4.74d the ion irradiation was carried out at normal incidence with Ar^+ ions at low energy of $E = 0.42$ keV and a fluence of $\Phi = 4 \times 10^{18}$ cm^{-2}.

Ion erosion-induced nanodots, in general, are observed on some materials only during normal incidence of the ion beam onto the substrate surface. In the case of surface ripples, depending upon the off-normal ion beam angle of incidence, ripples with wave vectors either parallel or perpendicular to the beam direction are observed in semiconductors, metals and dielectric materials, and for different and mostly used ion species including Ar^+, Kr^+, and Xe^+. Most results indicate that ripple patterns appear only within a limited range of angles of incidence, which vary between 30° and 70°. However, in contrast to usual observations, Ziberi et al.

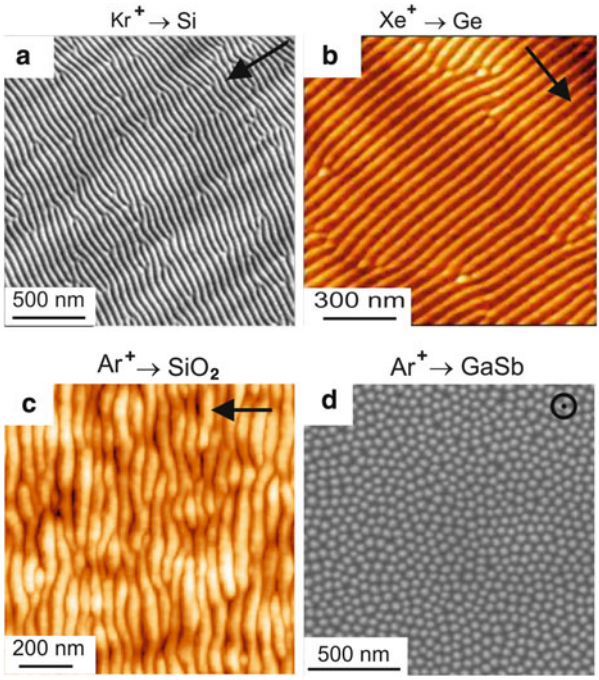

Fig. 4.74 AFM imaged surface pattern induced by ion beam erosion on various substrates. (**a**) ion-eroded (111)Si surface [318]. (**b**) ion-eroded (001) Ge surface from [319]. (**c**) Ion-eroded SiO_2 surface from [320]. (**d**) Hexagonal ordered nanodots with dot size ≈50 nm on GaSb fabricated by normal-incidence ion beam erosion [321]

[319] found that highly ordered ripples occur on 2 keV Xe^+ ion-eroded Si and Ge surfaces at smaller angles of incidence from 5° to 30° (see Fig. 4.74b). They report, that ripple patterns disappear and the surface gets smoothed between 30° and 60°, and evolve again on the surface at incidence angles above 60°. In most cases at incidence angles below a critical angle, which is ~(70–75)°, ripples perpendicular to the ion beam projection on the surface are formed. This critical angle depends mainly on the substrate material, ion species, and ion energy. At incidence angles larger than this critical angle, ripples parallel to the ion beam projection on the surface are formed (see, for example, [322]). Besides the ion beam direction the main process parameters affecting the features of surface pattern are the ion mass, the ion energy, the ion flux and fluence, and the substrate temperature during irradiation. A comprehensive overview about ripple formation under various ion irradiation conditions was published by Chan and Chason [323].

Most experimental studies show that the amplitude of perpendicular-mode ripples and dots increases exponentially with the time up to saturation with increasing fluence. The amplitude saturation may be related to nonlinear effects that become effective after a certain erosion time. At room temperature the ripple wavelength is, in general, not affected by the ion fluence, whereas for samples heated to $T \geq 400$ °C an increase of the wavelength with increasing ion fluence and ion flux was found [324]. At low temperatures, the ripple wavelength is

independent of sample temperature and increases with the ion energy. At higher temperatures, the ripple wavelength λ scales with the following Arrhenius law

$$\lambda \propto (1/T^{1/2}) \exp(-E_\lambda/2kT) \tag{4.11}$$

with T the sample temperature and E_λ an activation energy with values in the range of 0–1.7 eV depending on experimental conditions (e.g., ion mass, ion flux, ion energy) [323].

Furthermore, the wavelength λ is inversely proportional to the square root of ion energy $(E)^{1/2}$. The ripple evolution on heated surfaces and metallic substrates where the crystallinity remains under ion irradiation is more sensitive to the ion flux and ion fluence than on ion beam-amorphized surfaces. Additionally, the ripple and nanodot formation can be significantly influenced by other conditions at high-fluence ion irradiation, for example, by possible deposition of metal contaminants co-sputtered by the incident ion beam from the sample surrounding. As reported in [325, 326] under ion bombardment with Ar^+ ions at normal incidence, the co-deposition of metals can trigger the formation of dot arrays on Si surfaces, which cannot be observed under clean conditions. For example, ion beam erosion experiments performed in ultrahigh vacuum and taking care that the ion beam hits the Si(001) surface only, no ion beam-induced pattern forms on Si for incident angles $\leq 45^\circ$ with respect to the surface normal using 2 keV Kr^+ and fluences of $\approx 2 \times 10^{18}\,\mathrm{cm}^{-2}$ [327]. Therefore, pattern formation at normal or small off-axis ion beam incidence may be substantially influenced by metal impurities coming from broad beam ion sources or which are deposited by sputtering from the target holder surrounding the sample. Ion beam properties, like angle divergence and energy distribution of the ions also significantly influence the evolution and features of surface pattern, which was investigated, for example by Ziberi et al. [328].

Summarizing published studies, focused and unfocused ion beams with varying diameters from tens of nm (FIB) up to ~(1–20) cm (broad beam ion sources) have been used. Though mostly low energies (up to 2 keV) are used, higher ion energies of (4–50) keV for self-organization of surface pattern have also been applied. The wavelength of the ripples λ ranges over two orders of magnitude from several micrometers to several decades nanometers, depending on ion beam parameters and intrinsic materials properties. For example, on semiconductor surfaces (Si and Ge), these surface patterns are nanometer-scale structures, typically with a peak-to-valley amplitude between 0 and 10 nm and a periodicity between 30 and 300 nm. Recently, very regular surface pattern of dots and ripples with an unusual high aspect ratio (amplitude-to-wavelength ratio) of about one were observed at ion irradiation of Ge surfaces with heavy Bi cluster ions [329, 330].

There exist some theoretical models that try to explain the resulting surface topography during ion irradiation. Nevertheless, a complete understanding of the physical processes has not been achieved yet. At present it is widely accepted that the reason for the spontaneous buildup of a self-organized regular pattern is the competition between surface roughening induced by sputter removal of atoms and

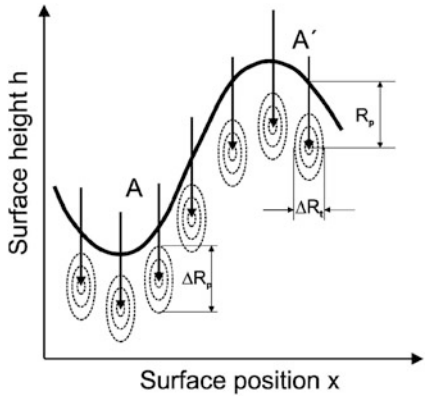

Fig. 4.75 Scheme of the ion erosion-driven Sigmund-instability of planar surfaces. The ellipses contours represent the iso-energy contours of energy deposition. R_p, ΔR_p, and ΔR_t are the projected ion range, the longitudinal and transversal ion straggling, respectively

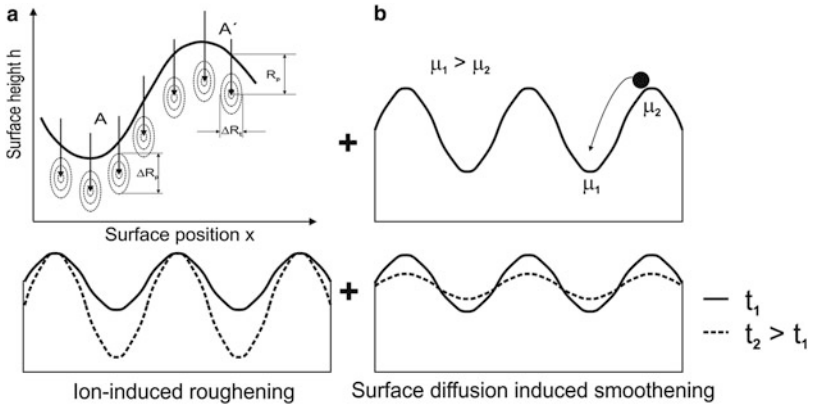

Fig. 4.76 Formation of periodically modulated ripple structures. (**a**) Ion induced roughening due to higher sputter yield at regions of positive surface curvature. (**b**) Surface smoothing by surface migration (diffusion) of atoms transporting material from negative curvature to positive curvature regions

diffusive surface smoothing mechanisms. Most theoretical explanations are based on the Bradley and Harper (BH) erosion-smoothing mechanism [331]. In this continuum model a linear continuum equation is used, which describes the surface topography as a continuous function, and the atomic near-surface structure is not considered to provide a physical understanding of associated atomistic mechanisms.

The BH model describing the sputter morphology evolution and the main features of ripple formation is based on the sputter theory developed by Sigmund [27, 332], which relates the erosion rate to the energy deposition onto the surface by sputtering. As shown in Fig. 4.75 the energy deposition with ellipsoidal shape differently depends on the local surface curvature—it takes place closer to the

surface at convex areas than of concave areas. Thus, the average energy and also the erosion rate are larger in points with positive curvature (A) than in those with negative curvature (A'). Obviously, the surface becomes unstable and the initial surface roughness gets amplified. According to the BH model the curvature dependent erosion rate induced surface roughening competes with opposite processes of smoothing the surface, which leads to the formation of periodically modulated ripple structures, as schematically shown in Fig. 4.76.

In general, the BH model successfully predicts some experimental observations such as ripples orientation, and the exponential growth of the amplitude at short ion irradiation times. However, at long erosion times, the ripples amplitude saturates and this fact cannot be explained by this model. Another implication of BH model is that the wavelength of the ripples should decrease for increasing ion energy, but at room temperature the opposite effect has been experimentally observed. Furthermore, the BH model implies that flat surfaces would remain flat due to the absence of valleys and hills. However, experimental observations show that under ion bombardment, in many cases, different types of structures evolve on initially flat surfaces. To overcome these problems more generalized continuum theories (higher order extensions of the BH equation) have been developed taking into account, for example:

- Nonlinear effects related to the incidence angle dependent sputtering yield which are responsible for the surface roughness saturation with time [333]
- Ion-induced effective surface diffusion (ESD) as a relaxation mechanism [334]
- Stabilizing effect of ion impact induced lateral mass redistribution to offset the BH destabilizing erosive mechanism at low angles [335]
- Other nonlinearities and higher order terms into a most general nonlinear equation [336]
- Re-deposition of eroded material during sputtering onto the surface [337]

However, to explain the self-organization of nanostructures due to ion erosion, more complex mechanisms responsible for the morphological evolution on different material surfaces must be taken into account. Moreover, during the ion bombardment the surface of the substrate is far from equilibrium and many atomistic surface processes become effective. Therefore, atomistic models, based on kinetic Monte Carlo (KMC) and Molecular Dynamic (MD) simulations can give additional useful information about the physical mechanisms behind the macroscopic surface pattern formation (see, for example, [338] and [339], respectively). It has been shown by KMC simulations that the combination of curvature-dependent sputtering based on the Sigmund model with thermally activated surface defect diffusion can produce surface patterns similar to those predicted by the BH theory. The results of MD simulations which take into account the surface mass re-arrangement caused by finite atomistic crater rims can explain, for example, the experimental observation of ripple amplitude saturation, which cannot be accurately predicted by the BH model or any other known numerical or analytical model for the sputter erosion surface instability.

Nowadays, ion-induced nanopatterns become interesting for various technological applications. By controlling the surface pattern down to the nanoscale, the

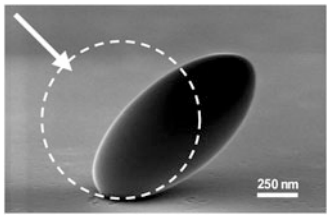

Fig. 4.77 Silica particle on silicon after irradiation with 4 MeV Xe^+ ions to a fluence of 4×10^{14} cm^{-2} at 90 K. The ion beam direction indicated by the *arrow* was tilted 45° from the surface normal. The initially spherical silica particle is indicated by the *dashed circle* [344]

structure and properties of thin films deposited on these surfaces can be tuned. For example, nanostructured ripple surfaces can be used as templates for the growth of thin metal films with predefined magnetic anisotropy [340]. In addition, the self-organized alignment of physical-vapor deposited metal nanoparticle chains or arrays of metallic nanowires with anisotropic optical properties, e.g., dichroitic plasmonic properties, have been recently demonstrated [341].

4.7 Ion Beam Shaping of Nanomaterials

The controlled anisotropic deformation of nanomaterials (e.g., NPs) by their irradiation with high energy ion beams is usually called "ion beam shaping." The energy loss of heavy high energy ions (>2 MeV) in the target is dominated by electronic stopping S_e. Due to the large mass difference between the ion and the electrons, the ion track remains roughly straight and the target atoms around the ion track are electronically excited. The energy in the electronic subsystem is subsequently transferred to the atomic subsystem by means of electron–phonon coupling, resulting in a local lattice temperature which can exceed several thousands of Kelvin [342, 343]. This can lead to the formation of a cylindrically shaped molten ion track with a typical diameter of several nanometers. These processes, called thermal spike model, can therefore induce structural changes in the target material such as amorphization, defect generation, and structural transformations, and finally macroscopic, anisotropic deformation of micro- and nanoscale objects as a result of microscopic processes occurring in the ion track (thermal spike) of individual ion impacts.

Anisotropic deformation of colloidal particles and nanoparticles assembled on a surface or embedded in insulating materials by MeV heavy ion irradiation has been intensively studied in recent years. As shown in Fig. 4.77 the deformation of micrometer-sized colloidal silica ensembles on Si surfaces by irradiation with 0.3–4 MeV Xe^+ ions was employed to change their spherical shape into oblate spheroids [345–347].

Under MeV ion irradiation amorphous silica NPs change their shaping rate into oblate ellipsoids depending on the ion energy and irradiation temperature. The final shaping anisotropy is determined by the ion fluence and the deformation increases with ion fluence and is independent of the ion flux. Size aspect ratios as large as ten

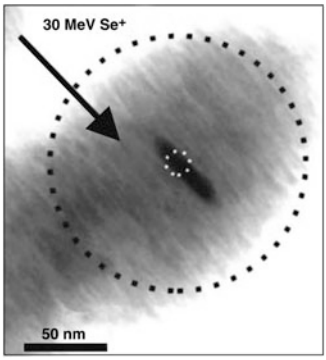

Fig. 4.78 Core–shell particle with a 14 nm-diameter Au core and a 72 nm-thick silica shell after 30 MeV Se^+ ion irradiation at an incidence angle of 45° (*indicated by the arrow*) at a fluence of 2×10^{14} cm^{-2}. The original *spherical shape* of the Au core and the silica shell are indicated by *white* and *black dashed circles*, respectively [351]

have been achieved. It was also found that small silica NPs (~40 nm) show less deformation than large particles (~1,000 nm). The deformation characteristics, expansion in the direction perpendicular to the ion beam and the shrinkage in the direction parallel to the ion beam with remaining constant particle volume, are explained by the viscoelastic thermal spike model of Trinkaus and Klaumünzer [348, 349]. Ion beam modified colloidal ensembles as photonic crystals and colloidal masks are of great interest due to their unique nano- or microstructures with distinct optical properties [350].

Many investigations show that the deformation characteristics for metallic NPs are quite different compared to amorphous silica particles. In [351, 352], for example, core/shell particles with a Au core of 14 nm diameter surrounded by a 72 nm thick silica shell were irradiated with 30 MeV Si^+ ions at a fluence of 2×10^{14} cm^{-2} (see Fig. 4.78).

The observed deformation of the silica shell was consistent with the anisotropic deformation described earlier. However, the Au core has deformed into rods with dimensions of 6 by 38 nm with the major axis along the direction of the ion beam and the minor axis perpendicular to it. Size aspect ratios up to nine were observed for the Au nanorods. Experiments with Au core/silica glass shell NPs have shown that the Au core particle only deforms when the silica shell surrounding the particle is thicker than a critical thickness of ~30 nm. This different deformation behavior of the metallic NP is attributed by the authors to the in-plane mechanical stress in the silica shell acting on the radiation-softened Au core.

Similar ion beam shaping of crystalline metallic NPs was observed, for example, for Co [353], Pt [354], Ag [355], and extensively investigated for Au NPs embedded in silica glass or in thermally grown SiO_2 [352, 356, 357]. As an example, Fig. 4.79 shows a typical shape transformation from spherical NPs with an original diameter of ≈20 nm and embedded in SiO_2 (Fig. 4.79a) into Au nanorods (or nanowires) aligned parallel to the direction of the ion beam.

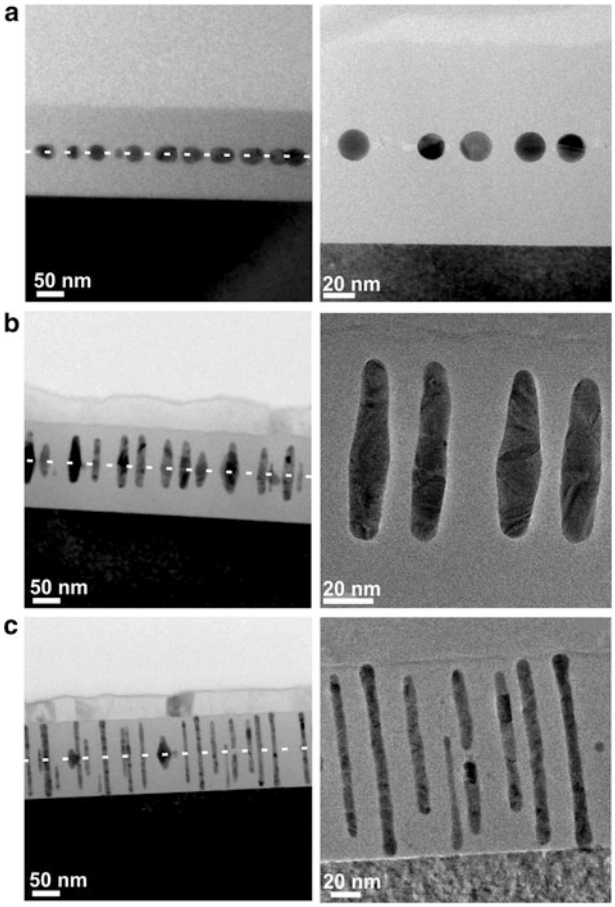

Fig. 4.79 Ion beam shaping of nearly monodispersive spherical Au NPs with a mean diameter of ≈20 nm using 38 MeV I^{7+} ions: (**a**) Au NPs embedded nearly in the middle of a 130 nm thick SiO_2 layer, (**b**) Au particle elongation after irradiation with a fluence of 1×10^{14} cm^{-2}, and (**c**) Au nanorod formation after irradiation with an ion fluence of 2.5×10^{14} cm^{-2}. The *dashed line* indicates the depth plane in which the initial NPs were located

The elongation progressively increases with increasing ion fluence as shown in Fig. 4.79b, c. The Au NPs have been irradiated with 38 MeV I^{7+} ions with a fluence of 1×10^{14} cm^{-2} (Fig. 4.79b) and 2.5×10^{14} cm^{-2} (Fig. 4.79c) leading first to prolate-like nanorods with a length of ≈72 nm, a width of ≈15 nm, and an aspect ratio of about 5 and to pronounced nanowires with a length of ≈140 nm, a width of ≈8 nm, and an aspect ratio of about 17, respectively.

The deformation of spherical Au NPs into nanorods does not follow the visco-elastic thermal spike model and other mechanisms must be the reason. Compared to amorphous insulators it is noteworthy that crystalline metals or freestanding metallic NPs do not deform under high energy ion irradiation, which is ascribed to the

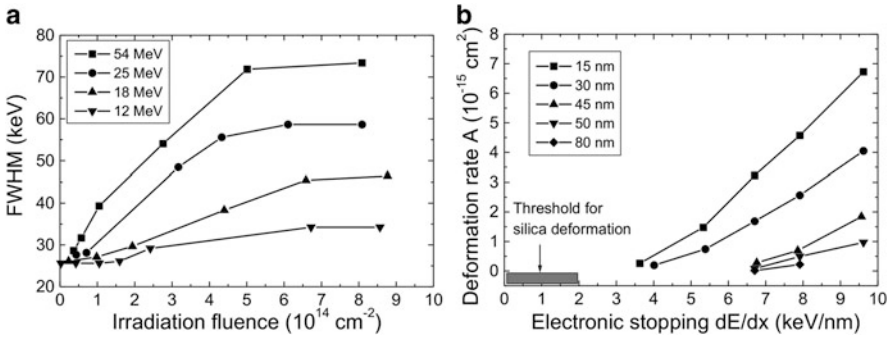

Fig. 4.80 (**a**) Au peak width (FWHM) measured by RBS, representing the Au nanorod size versus fluence for 15 nm Au NPs embedded in SiO_2 under Ag^+ ion irradiation at different ion energies. (**b**) Deformation rate A as a function of electronic stopping S_e in SiO_2 for Au NPs with different diameter of (15–80) nm irradiated with Ag^+ ions [358]

absence of ion track formation due to the large electron mobility of metals, and to fast recrystallization that restores the original state of the material. Thus, the formation of nanorods must be a result of processes that affect both the metal and the surrounding silica matrix and cannot be attributed only to the in-plane mechanical stress in the surrounding silica matrix acting on the radiation-softened Au NP. The shaping behavior of crystalline metallic NPs (e.g., Au) in dependence on ion fluence Φ and deposited energy by electronic energy loss $S_e(x)$ has been investigated in detail by Dawi et al. [358].

The results show the existence of two thresholds, an energy loss threshold (Fig. 4.80a) and a fluence threshold (Fig. 4.80b) for metallic NP elongation, which depend on both NP size and electronic stopping power S_e (ion mass and energy) of the incoming ions. As can be concluded from Fig. 4.80a the energy loss thresholds for elongation of Au NPs with (15–30), (40–50), and 80 nm diameter are around 3.5, 5.5, and (7–8) keV nm^{-1}, respectively. In general, the data from irradiations with different kinds of ions and at different ion energies indicate that a mean threshold of (4–8) keV nm^{-1} in the electronic energy loss can be expected above which deformation of the metallic NPs occurs. In comparison, the electronic energy loss threshold for amorphous NPs (e.g., silica) is much lower and in the range of $S_e \approx$ (0.1–1.8) keV nm^{-1}. The deformation rate A(cm^2) of the NPs in Fig. 4.80a is defined as the relative differential RBS Au peak width change dE per unit fluence dΦ, $A = (1/E)(dE/d\Phi)$. Taking into account the first data points (above the threshold) of the relative change of the Au RBS peak FWHM versus fluence, and defining $dE/d\Phi$ as the slope of the linear width increase, A can be plotted versus the electronic energy loss S_e in the SiO_2 matrix. In general, the ion fluence threshold depends on the ion mass and energy and decreases with increasing ion energy and ion mass. With increasing NP size the fluence threshold for NP deformation increases. Typical values of the fluence threshold for metallic NP deformation can be expected in the range between 5×10^{13} and 5×10^{14} cm^{-2}.

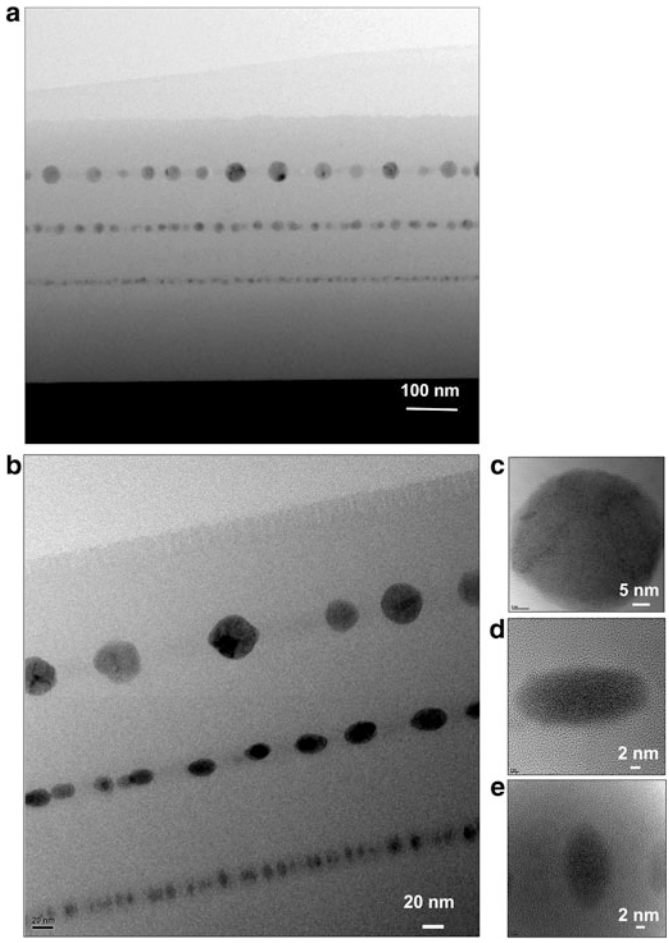

Fig. 4.81 Cross-section (X)TEM image of the as prepared sample with Ge NPs with different sizes of 8, 18, and 37 nm from top to down (**a**). Overview image (**b**) and high-resolution images (**c**–**e**) of the sample after irradiation with 38 MeV I^{7+} ions at a fluence 1×10^{14} cm^{-2}. The largest Ge nanoparticles remain spherically and consist of a mixture of polycrystalline and amorphous regions (**c**). The oblate (**d**) and rod-like (**e**) Ge particles are completely amorphous

Thermal spike calculations of the temperature elevation around the NP are in correlation with the increase of the deformation rate with increasing ion track radius, i.e., with increasing electronic stopping power of the incoming ions. For the deformation of metallic NPs embedded in a silica matrix, two possible mechanisms for deformation can be considered: (1) The nanoparticle responds to the stress field generated in silica by ion tracks squeezing the NP by the surrounding matrix (indirect mechanism). (2) The ion track overlaps with both the NP and the silica matrix, giving rise to transient gradients (chemically, thermally, mechanically) acting on the involved metal atoms of the NP (direct mechanism). In experiments for metallic NP deformation (elongation) in SiO_2, the energy loss

by electronic stopping is higher than the threshold for silica deformation and in-plane stress fields in the silica matrix are always present.

Contrarily to ion beam shaping of metallic NPs embedded in silica, the deformation of crystalline semiconducting Ge NPs evolves with shrinking of the NP in the ion beam direction and expanding perpendicular to the direction of the ion beam which was experimentally observed by Schmidt et al. [359, 360]. As shown in Fig. 4.81 at given irradiation conditions (38 MeV I^{7+} ions at a fluence 1×10^{14} cm^{-2}) the deformation and the shape depend on the size of the spherical Ge NPs.

The largest Ge nanospheres in the top layer kept spherical (cf. Fig. 4.81c), whereas medium-size Ge spheres in the middle layer became oblates (cf. Fig. 4.81d), and smaller ones, in the bottom layer, shaped rod-like (cf. Fig. 4.81e). The high-resolution cross-section (X)TEM image in Fig. 4.81c shows that the large unshaped spherical Ge nanoparticles are in a mixed polycrystalline and amorphous state. The oblate and rod-like Ge particles in Fig. 4.81d, e, respectively, reveal a completely amorphous structure. At a higher fluence of $\approx 5 \times 10^{14}$ cm^{-2} the larger Ge NPs of Fig. 4.81c become smaller, obviously due to partial ion-induced Ge dissolution into SiO_2. These Ge NPs reduced in size start to deform too. This effect was also observed during irradiation of metallic NPs embedded in silica, for example in [357].

At present, the different shape evolution of metal (Au, Ag, Pt, etc.) and semiconductor (Ge) NPs is not yet fully understood. One possible approach for the physical description accounts for the well-known in-plane stress generated by ion tracks in the surrounding silica matrix and for ion tracks overlapping with the NPs the electronic energy relaxation in the whole nanoparticle.

Molten SiO_2 tracks are expected if the energy of electronic stopping in SiO_2 per length unit exceeds the threshold of $dE_{el}/dx > 2$ keV nm^{-1}. In most cases the molten track diameter is small compared to the nanoparticle diameter. The interaction of the molten tracks with the nanoparticles seems to dissolve some material from the NPs in the SiO_2 matrix [357, 359], which has been not yet considered by the model. Whereas in SiO_2 the deposited electronic stopping energy relaxes within a rather confined volume into the phonon system leading to narrow molten tracks, in metals and in Ge the electronic energy relaxes in larger volumes, here we assume in the melts if the following relation is fulfilled:

$$\frac{dE_{NP}^{el}}{dx} \cdot L_{NP} \geq \frac{4\pi}{3} \cdot R_{NP}^3 \cdot H_{NP}^{melting} \cdot \rho_{NP}, \tag{4.12}$$

where L_{NP} is the length of the ion track in the nanoparticle, R_{NP} is the radius of the nanoparticle, $H_{NP}^{melting}$ is the heat of melting, and ρ_{NP} is the density of the NP. Thus, for a given electronic stopping power a spherical nanoparticle melts under the condition that

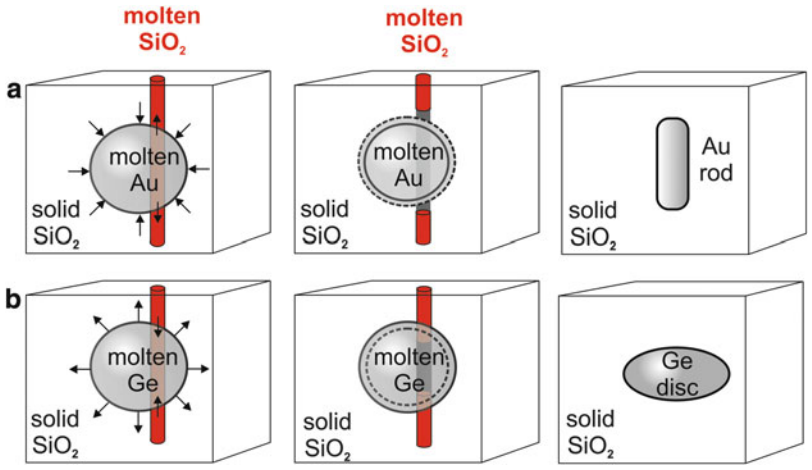

Fig. 4.82 Scheme of different deformation for metal (Au) and semiconducting (Ge) NPs proposed by Heinig (private communication). (**a**) NP elongation in direction of the ion beam direction due to the expansion of the molten metal into the molten SiO_2 track. (**b**) NP shrinking in direction of the ion beam due to the contraction of the molten semiconductor material

$$R_{\mathrm{NP}}^{\max} \leq \sqrt{\frac{3 \cdot \mathrm{d}E_{\mathrm{NP}}^{\mathrm{el}}/\mathrm{d}x}{2\pi \cdot H_{\mathrm{NP}}^{\mathrm{melting}} \cdot \rho_{\mathrm{NP}}}}. \tag{4.13}$$

where melting of NPs is restricted to $L_{NP} \leq 2{\cdot}R_{NP}$. If we set both sides of (4.13) equal we find the largest spherical NP with radius $R_{\mathrm{NP}}^{\max}$ which can be molten by electronic stopping. For example, in the case of 38 MeV I^{7+} ion irradiation the electronic stopping power in Ge is $\mathrm{d}E_{\mathrm{el}}/\mathrm{d}x = 7.7\ \mathrm{keV\ nm^{-1}}$ and we get a maximum particle radius of $R_{\mathrm{NP}}^{\max} \approx 16\,\mathrm{nm}$, which means that Ge particles with smaller sizes will be molten. This estimated size threshold for melting is in agreement with the experimentally found shaping of the three different nanosphere sizes (Ge NPs of 9 nm radius are shaped, whereas NPs of 18.5 nm radius remain spherically, see Fig. 4.81c). The particle radius of 18.5 nm for the largest Ge nanoparticles is above the threshold of $R_{\mathrm{NP}}^{\max} \approx 16\,\mathrm{nm}$. It should be noted that below the shaping threshold, which can be assumed to be $R_{\mathrm{NP}}^{\max}$, two shaping modes have been identified (Fig. 4.81d, e): NPs with radii being much larger than the molten track diameter shape into disks, whereas rod-like shaping is found for NPs with radii comparable with the molten ion track radius. It appears that both are necessary for Ge NP shaping with swift heavy ions, molten tracks in SiO_2, and molten Ge NPs.

The following driving forces for tailoring of NP size distributions, shapes, and anisotropies of nanoparticles by high energy heavy ions can be assumed: (1) the materials dependent electronic stopping power, (2) the volume change of the silica matrix and the NPs upon melting, (3) the asymmetric hydrodynamic flow due to stress field hysteresis, (4) the far-from-equilibrium steady-state solubilities, and (5) the strongly anisotropic diffusion coefficients. One of the most striking effects upon melting of the NPs as schematically shown Fig. 4.82 is its volume change $\pm\Delta V/V_{\mathrm{s}}$

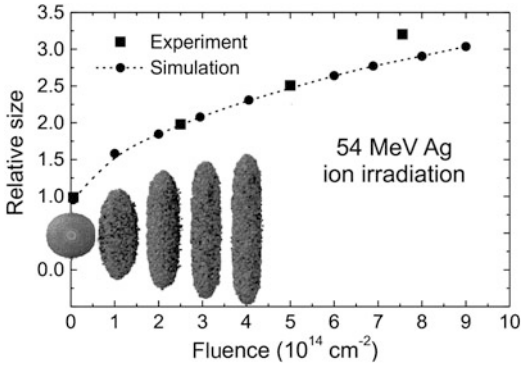

Fig. 4.83 KLMC simulation of the Au nanoparticle deformation. The relative particle size $l/2R_0$ is shown as function of the fluence for 54 MeV Ag^+ ion irradiation. l is the length of the Au rod and R_0 is the radius of the initially spherical Au NP. The insets show the simulated Au NP shapes after irradiation with 1×10^{14}, 2×10^{14}, 3×10^{14}, and 4×10^{14} cm^{-2} (Heinig KH, private communication)

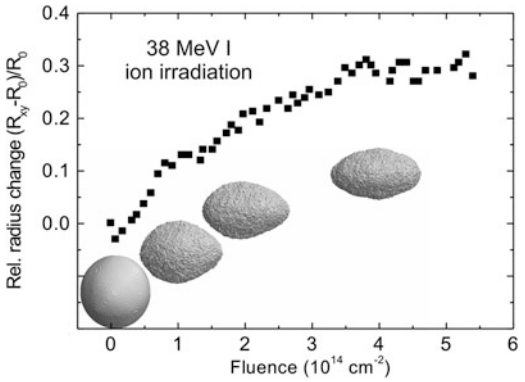

Fig. 4.84 KLMC simulation of the Ge nanoparticle deformation. Shown is the relative particle radius change $(R_{xy}–R_0)/R_0$ as a function of the fluence for 38 MeV I^{7+} ion irradiation. Here, R_{xy} is the larger radius of the oblate spheroid and R_0 is the radius of the initially spherical Ge NP. The insets show the simulated Ge nanoparticle shapes after irradiation with fluences of 1×10^{14}, 2×10^{14}, and 4×10^{14} cm^{-2} [360]

with V_s the solid state volume, for example, contraction by ≈ -5 % for Ge or expansion by about $\approx +5$ % for Au.

When the NP melts it is forced to expand (Au) or to reduce (Ge) its volume. Because it is embedded in SiO_2 a high tensile stress is built up. During the extremely short melt periods of 10...100 ps, this stress can relax only partly via the molten SiO_2 track, not via the solid SiO_2 matrix. Thus, the intersection interfaces between molten SiO_2 and molten Au moves outward and the molten Ge moves into the NP to allow for the molten Au expansion and for the molten Ge contraction, thereby reducing the tensile stress. Within a few tens of picoseconds the molten NPs cool down, reaching due to the extreme cooling rate a strongly

under-cooled liquid state. From that state it re-solidifies suddenly without a chance of re-contraction (Au) or re-expansion (Ge) in the track, which is now solid. Thus, after melting and re-solidification of NPs in SiO_2 a hysteresis of the volume change appears. In the proposed model, this hysteresis is assumed to be the driving force for NP shaping into rods or disks. Based on this model kinetic Monte Carlo simulations described in [195] have been carried out taking into account spatio-temporal temperature profiles of the molten tracks, the volume change of the silica matrix and the NPs upon melting, and the temperature-dependent solubility and diffusivity of the NP material in molten silica surrounding the NP. Two examples of KLMC simulation results for the deformation behavior during high energy ion irradiation of Au and Ge nanoparticles are shown in Figs. 4.83 and 4.84, respectively.

KLMC simulation results in Fig. 4.83 are compared with experimental results taken from [358] for the irradiation of Au NPs with 54 MeV Ag ions for different fluences. The simulation was performed for an Au NP size of 15 nm, a track radius of 4.5 nm, and a minimum track length L_{NP} inside the NP of $R_0/2$. The insets in Fig. 4.83 show the side views of the NPs at the positions of corresponding fluences. The transformation of the spherical Au NPs into elongated nanorods agrees very good with the relative size change experimentally observed by Davi et al. [358] (see experimental data in upper curve in Fig. 4.80b). Assuming that ~1 % of the Au NP volume change upon melting and subsequent shrinking during resolidification is pressed into each ion track the simulation results nicely fit the experimental data.

The simulation in Fig. 4.84 was performed for a Ge NP size of 16 nm, a track radius of 3.8 nm, and a minimum track length L_{NP} of $R_0/2$. The insets of Fig. 4.84 show the side views of NPs at the positions of the fluence which they experienced. The shaping agrees nicely with the experimentally found shapes (see Fig. 4.81b, d), even the required fluences agree. The saturation of shaping at high fluences seen in Fig. 4.84 results from the minimum track length L_{NP}, because too flat Ge NPs will be no longer molten. The model works only for NPs being larger than the track radius, and therefore small Ge NPs becoming elongated (Fig. 4.81e) cannot be modeled. Additionally, a fluence-dependent dissolution of Ge NPs has been observed experimentally which decreases the size of initially not deforming NPs until they shrink below the critical size of (4.12). Afterwards they get a prolate shape too.

The striking agreement between the experiments and the KLMC simulations suggests that the driving force for ion beam shaping is inherently included in the model for atomistic simulations. Finally, the task to identify the microscopic physical origin of driving forces of ion beam shaping remains difficult. Nevertheless, the main behavior of ion beam shaping not only for metal but also for Ge nanoparticles can be satisfyingly described. The experimentally observed growth of very long (~200 nm) Au nanowires at the expense of shorter ones [357] requires an Au transport through the silica matrix which has been also considered in KLMC simulation of ion beam shaping, and a preferred growth of longer nanowires has been observed too (Heinig KH, private communication). Subsequent ion tracks which overlap with the volume of former tracks enable the dissolved Au to diffuse away from the NP, and gold can diffuse track by track from one nanoparticle to another. As the driving force for the preferred Au diffusion from shorter Au

nanorods to longer ones some kind of Ostwald ripening has been identified and KLMC simulations reproduce nicely that experimental finding. The driving force identified so far is related to a strong anisotropy of the mean Au diffusion along the ion track and perpendicular to the track into the surrounding silica matrix.

From application point of view, especially metal nanoparticles (Au, Ag, Cu) are studied extensively, because their near-field and far-field optical response promise, for example, nanophotonic applications for subwavelength light guiding in nanoparticle chains, plasmonic light sources, plasmon lasers, enhanced LEDs, and enhanced solar cells. For these purposes nanorods and nanowires are of special interest since their plasmon resonance frequencies can be tuned over a wide range by varying the aspect ratio and length of the nanoparticles.

4.8 Ion Beam Processing of Other Materials

Ion implantation is a unique technique to modify the near-surface region of a wide range of solid materials independently of many of the constraints associated with conventional processing methods. In most cases materials, such as metals and most semiconductors, are rather insensitive to the electronic part of the energy deposition. Other materials, for example insulating and dielectric materials such as ionic solids, alkali and silver halides, dielectric glasses, and amorphous materials, are quite sensitive to the energy deposited in their electronic systems. The high sensitivity of these materials to ion irradiation makes them particularly attractive for ion beam modification.

Besides the wide application of ion implantation and ion beam synthesis in the semiconductor industry, ion beam methods found application, for example, to the synthesis and modification of metal-nitride layers in metal alloys, and the modification of polymers, insulating optical materials and ceramics. Two general ion beam processing methods are widely used for surface modification of nonsemiconductor materials: scanned or broad beam ion implantation, in which the ion beam is directed toward mostly planar substrate surfaces, and plasma immersion implantation, where the ions hit the surface of nonplanar, three-dimensional, workpieces from all directions. The ion beam treatment is designed to modify only the surface properties of materials without changing their bulk properties. Some of the surface properties that can be modified by ion beam processing are hardness, fatigue, toughness, adhesion, wear, friction, corrosion oxidation, dielectric properties, magnetic properties, superconductivity, resistivity, and catalysis.

4.8.1 Ion Implantation into Metals

The first application of ion implantation into metals was reported in 1969 by Dearnaley [361], who addressed the possibility of improving mechanical and corrosion behavior of steels that are of relevance to the metal processing industry. Ion implantation into metals has shown remarkable improvement in properties, for example, of nitrogen-implanted alloy steels and of nitrogen-implanted aluminum tools for machining high-temperature alloys. An extended overview of ion implantation into metals the reader can find in [362]. Plasma immersion ion implantation (PIII) has introduced another set of opportunities for metal surface treatment by ions and a rapid increase of PIII facilities which are now commercially available. The PIII treatment of metals introduced by Conrad et al. [363] in 1986 can achieve advantages over directed beam implantation. The effects of implanting nitrogen into metal surfaces previously or simultaneously enriched, for instance with carbon and/or boron by vapor deposition which is known as ion beam-assisted deposition (IBAD), also have been found application to metals.

As demonstrated in many studies (see, for example, [364–368]) ion implantation can modify the surface-sensitive mechanical (wear, friction, hardness, adhesion, fatigue) and chemical (corrosion, oxidation, electrochemistry, catalysis) properties of steels. For example, fatigue life has been extended by as much as a factor of two, the coefficient of sliding resistance can be reduced by as much as a factor of 100, the surface hardness can be increased by 2–3 times, and the wear resistance increased by a significant amount. Studies have concentrated on the use of nitrogen ions, but the use of C^+, B^+, Ti^+, and Mo^+ ions has also shown promising results. Today the PSII processing is already used in large-scale manufacturing, such as of automotive parts. A very useful application of this process is in the ion implantation of medical prostheses based on Ti alloys (e.g., Ti6Al4V). For instance, artificial hip joints with complicated shapes have been implanted with nitrogen ions for wear and hardness improvement to increase the lifetime of such devices [369].

N^+ is the most common ion used for metallurgical applications and causes pegging of microcracks, filling of lattice spaces in crystalline structures of the polycrystalline material, and chemical reactions to form nitride compounds, giving new lattice properties. One example is N^+ ion implantation of different austenitic stainless steels (e.g., DIN 1.4301 or AISI 304) with high chromium content where a substantial increase in hardness by converting Cr in the near-surface layers to chromium nitride and a wear improvement (reduction factor) up to a factor of 30 have been achieved. Improvements by B^+ and C^+ implantation into steels have been also reported. These improvements are explained in analog to metallurgical boridizing and carburizing of metal surfaces to form metal-boride and -carbide phases. N^+ ion implantation alone or combined N^+/C^+ implantations are also applied to mold steels which are usually made from FeCr ferritic stainless steels with higher carbon content (e.g., Cr12MoV, X36CrMo17, or X155CrVMo12.1) [370, 371]. These materials do not withstand high-temperature thermal processing, often suffering significant distortions or significant decrease of hardness at temperatures

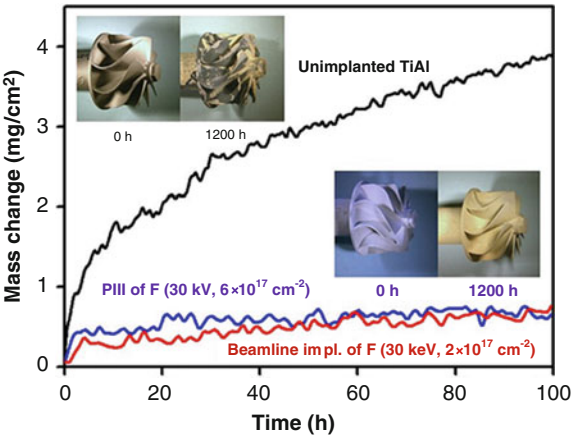

Fig. 4.85 Comparison of the oxidation behavior of γ-TiAl before and after processing by BLII and PIII with F^+ ions. Insets: As-received (untreated) turbo-charger rotor (*top left*). Exposure in air at 1,050 °C for 100, 600, and 1,200 h. The same rotor after fluorine treatment (*bottom right*). Exposure in air at 1,050 °C for 100, 600, and 1,200 h

above (200–300) °C. Ion implantation can substantially improve the surface properties with negligible distortion or oxidation effects, and induce high surface hardnesses (~1,100–2,000 Vickers hardness) resulting in substantial increases in tool lifetimes [372]. For injection and extrusion screws used, for example, in molten plastic pumps ion implantation produces a low friction, wear-resistant surface on the screw and allied components. Interesting industrial applications of N^+ ion beam processing of metals are, for example, in manufacturing of steel knives for cutting meat, plastic, paper, or rubber for which a life improvement by a factor of four to seven could be reached. Compared to other ion applications, for example, to tooling the field of medical implants, such as steel knives was advancing more quickly. This is because ion implantation appears to be the only surface modification technique that can successfully harden titanium alloy's surface (e.g., Ti/6AI/4V) without compromising surface finish, dimensionality, or cosmetic appearance.

Other examples are titanium alloys (titanium aluminides) which are used as light weight materials where ion implantation (PIII) can help to improve substantially materials properties under harsh environmental conditions. Despite of their good mechanical properties they cannot be applied yet, for example, in aero engines due to their insufficient oxidation resistance at temperatures above roughly 800 °C. Using implantation of halogens, especially F^+ ions, into the subsurface zone of the TiAl components the oxidation behavior of TiAl alloys can be improved significantly [373–376]. For turbine blades, as examples for real TiAl components, PIII implantation of F^+ ions extracted from a Ar/CH_2F_2-RF-plasma (400 W, 500–750 Hz) by negative pulses of −30 kV, 10 ms using a total number of 1×10^6 pulses was carried out leading to a retained fluorine dose of $\approx 6 \times 10^{17}$ cm^{-2}. The investigations showed an increased high-temperature oxidation resistance after PIII treatment due to the formation of thin protective alumina layer on the surface in contrast to a fast growing, nonprotective thick mixed oxide layer (TiO_2/Al_2O_3) on untreated samples during high-temperature

oxidation in air. The formation of a growing Al_2O_3 layer is promoted by the fluorine. This so-called fluorine effect leads to the preferential intermediate formation of gaseous aluminum fluorides at elevated temperatures if the fluorine content at the surface is being kept within a certain concentration range. These fluorides are then converted into solid Al_2O_3 due to the high oxygen partial pressure of the high-temperature environment forming protective pure Al_2O_3. The thin Al_2O_3 surface layer is not be damaged by high-temperature corrosion and is stable even under thermocyclic conditions and in wet and aggressive environments which are typical for technical high-temperature applications [377, 378].

Fig. 4.85 shows an example for improvement of high-temperature oxidation resistance of TiAl alloys by plasma-immersion ion implantation (PIII) and beamline ion implantation (BLII) of fluorine ions. The curves for mass change versus time representing the oxidation behavior were measured by thermogravimetric analysis (TGA) and studied during thermocyclic exposure. The ion beam treated samples (red and blue curve) show a significant lower mass gain (higher oxidation resistance) than the untreated sample (black curve). After optimization of implantation parameters for the F^+ ion PIII the same good TGA results compared to optimum beamline implantation of fluorine (25 keV, 2×10^{17} cm^{-2}) were found. In this case, the PIII parameters were the following: pulse length 10 ms, bias voltage 30 kV, RF power 400 W, frequency 750 Hz, 1×10^6 pulses, gas flow CH_2F_2/Ar = 15/5 sccm. The retained fluorine fluence was 6×10^{17} cm^{-2}. For comparison, the upper left and bottom right insets in Fig. 4.85 show the change of turbine rotor tools during high-temperature exposure before and after ion treatment, respectively.

For other Al alloys and Al, the improvement of tribological properties by the formation of an aluminum nitride surface layer has been also demonstrated using low energy (1–10 keV) N^+ ion implantation into heated samples. AlN exhibits high hardness and wear resistance as well as significantly enhanced corrosion resistance. The kinetics of aluminum ion beam nitriding has been intensively investigated by Telbizova et al. [379–381]. It was shown that a thin stoichiometric nitride layer is formed at the aluminum surface by diffusion of aluminum atoms from the bulk underlying the AlN layer. An inhomogeneous AlN layer may form if the process of ion beam nitriding is limited by Al diffusion rather than by N^+ ion supply. At otherwise identical conditions, an increased sample temperature will result in a more homogeneous nitride layer.

The ion implantation into metals and metal alloys is continuing to develop in different metallurgical areas. Ions other than nitrogen are increasingly used, for example, rare earth elements such as yttrium to produce high lubricity and corrosion-resistant surfaces. These developments of ion implantation will continue to extend the options to use moderate temperature processing methods while still achieving improved surface properties for increasing tool life. Ion implantation in metals becomes an important and promising technique for surface nanomodification, especially in case of ultra precision tools where the depth of modification

should be in range of 30–100 nm. Important advantage of this technique is the fact that surface dimensions are not changed after implantation. This is especially important for ultra precision tools where the subsequent dimension correction would be extremely difficult.

4.8.2 Ion Implantation into Polymers

Conventional ion beam implantation has been introduced to modify the surface properties of polymers, giving an improvement in such qualities as hardness, conductivity, and biocompatibility. Plasma immersion ion implantation (PIII) as an alternative method has the advantages of high implantation rates and conformal treatment of three-dimensional polymer or plastic surfaces. Ion beam treatments modify the outermost surfaces of polymers without affecting their bulk properties. The ion beam processing of polymers has led to dramatic improvements in their hardness. For example, after implantation, the surfaces of some polymers may become harder than stainless steel, although the process may actually be a result of carbonization of the polymer rather than by the synthesis of new compounds by implantation itself. Physical and chemical effects appearing during ion implantation into polymers are described more in detail in [382].

The effects of ion implantation in the energy range from several keV to MeV on polymers have been widely reported. The energy release of fast ions in polymers produces pronounced changes in their chemical and physical properties associated with the breaking and rearrangement of the original chemical bonds. Changing the ion fluence three main modifications in polymers can be distinguished: (1) at low ion fluences (~10^{14} cm^{-2}) cross-linking between chains and chain scissions is observed; (2) with increasing ion fluence ($\geq 10^{15}$ cm^{-2}) the original polymer structure is heavily damaged and exhibit properties close to those of hydrogenated amorphous carbon; (3) at very high fluences (~10^{16} cm^{-2}) graphitization of the material occurs [383].

In contrast to ion irradiation of semiconductors and metals in polymers, the electronic stopping (S_e) and nuclear stopping (S_n) act simultaneously and both are responsible for the change of their properties. It has been assumed that a complete modification of irradiated polymer already occurs in the single-ion track, forming a graphitized ion track due to the so-called linear energy transfer [LET—energy deposited per unit ion path length (eV nm^{-1})]. The successive overlap of many ion tracks with increasing ion fluence induces a complete change of chemical bonds of the material. Thus, characteristic saturation fluences for each combination of ion mass and energy are observed. The results of differently generated chemical effects, such as modification of functional groups, destruction of the aromaticity, formation of a three-dimensional compacted network, depend not only on the implantation parameters (total deposited energy, electronic stopping S_e, nuclear stopping S_n, and ion fluence) but also upon the chemical composition and structure of polymers [384, 385].

A particularity during ion irradiation of polymers is that various gaseous molecular species are released, for example hydrogen and less abundant heavier molecules which are scission fragments. Cross-linking occurs when free dangling ion or radical pairs on neighboring molecular chains join. Mechanical, physical, and chemical property changes in polymers are determined by the magnitude of cross-linking and scission. Cross-linking enhances the mechanical stability (increase of hardness, improvement of wear, and starch resistance) and decreases the in-diffusion and solubility of chemical solvents while scission degrades mechanical strength and increases dissolution of polymers in solvents. The electrical conductivity and optical density increase by ion irradiation due to the formation of cross-links and conjugated double and triple bonds in the polymer. Furthermore, the charge carrier mobility can be increased by cross-linking which facilitate the transport of charge carriers across molecular chains of the polymer. Additionally, ion irradiation induces changes in the electronic structure and induces defects such as anions and radicals (donors) and cations (acceptors). Thus, electrons can be excited by visible light, and colour changes occur because of increased light absorbance. With increasing ion fluence more energetic blue light is absorbed first and the color changes from pale yellow to reddish brown and eventually to a dark color. At very high ion fluences, a metallic luster appears because light is scattered by electrons similar to the effect of free electrons in metals. Industrial application examples are:

- The fabrication of conductive integrated circuit trays using N^+ or Ar^+ ion implantation into modified poly-phenylene oxides to prevent IC failure caused by static electricity
- The fabrication of scratch, UV absorbent and oxygen penetration protected transparent polymers by N^+, C^+, or He^+ ion implantation for sun caps, goggles, cosmetic bottles, touch screens, etc.

The application of ion beams to polymer modification can be roughly classified into three main fields: (1) surface modification of mechanical, chemical, and electrical properties mostly by noble gas and metal ion implantation, (2) modification of optical properties by nitrogen and noble gas ion implantation, and finally, (3) synthesis of polymer composite materials containing metal NPs by implanting metal ions, which is motivated by potential optical applications, such as magnetooptic data storages and nonlinear optical devices [386]. The nonlinear optical properties of polymer composites containing metal NPs, for example Ag NPs in PMMA, are based on the dependence of their refractive index on incident light intensity. The metallic NPs embedded in a polymer which exhibit an enhancement of local electromagnetic field enhancement stimulates the linear optical absorption of metal NPs (surface plasmon resonance, SPR). Between suitable dielectric materials (e.g., SiO_2, Al_2O_3, MgO) for embedding metallic NPs, polymers will be of increasing interest.

Mainly noble gas and nitrogen ion, but also metal ion (Ag, Cu, Fe, Cr, Pt, Pd, W, Ti, etc.), halogen ion (F, Cl), and silicon ion implantations have been investigated. For polymer modification the selected ion energies are in the medium energy range (30–500 keV) and relatively high fluences in the range from 10^{14} to 10^{17} cm^{-2} are

implanted. The large number of different polymers and the change of their properties by ion implantation/irradiation cannot be described considerably in the frame of this chapter.

4.8.3 Ion Implantation into Insulating Optical Materials

Ion implantation is one of the most effective techniques for alteration of optical properties including reflectivity, absorption, luminescence, and refractive index in a large number of insulating optical materials [238, 387]. The ion beam-induced optical properties are closely dependent on ion species, ion energy, and ion fluence. Mostly investigated insulating optical materials are noncrystalline glasses, nonlinear optical crystals, photorefractive crystals, and laser crystals. The ion implantation in optical crystals is mainly focused on the investigation and optimization of ion-implanted planar and channel waveguides because optical waveguide structures are the most fundamental parts of integrated optical circuits in the field of modern optical communication. Recent activities in this field of research and development have been reviewed by Chen et al. [388, 389]. It is evident that until now, ion implantation has been used to produce waveguide structures in more than 100 optical materials, including glasses, inorganic crystals, semiconductors, and organic materials (e.g., PMMA).

Ion irradiation (H^+, He^+, Ar^+, etc.) induced defects and compaction of the glass network in different *glasses* lead to an increase of the refractive index (RI) by a few percent [390]. Implanting chemically active ions (e.g., N^+, Li^+) into fused silica (SiO_2) the RI can be increased significantly, for example from 1.46 to 1.96 with increasing Li^+ ion fluence [391]. *Fused silica* is widely used in the manufacture of optoelectronic devices because the coupling between fused silica and optical fibers is much easier resulting from the small difference between their RIs. Different planar waveguides have been produced in fused silica by high energy ion implantation of light (e.g., H^+, 0.5–1.0 MeV, ~10^{16}–10^{17} cm^{-2}) and heavy (C^+, 2–3 MeV, ~1×10^{15} cm^{-2}) ions. *Amorphous silicate and phosphate glasses* are important optical materials due to their good mechanical performance, high chemical stability, and very high transparency in the infrared wavelength region. Rear earth doped (e.g., Nd^{3+} and Er^{3+}) glasses have been extensively used as hosts of waveguide amplifiers and waveguide lasers with RIs tailored by high energy ion irradiation (e.g., O^+, ~5 MeV, ~1×10^{15} cm^{-2}).

For optical waveguide applications, the change of the refractive index n by ion implantation/irradiation has been intensively investigated in *crystalline optical materials*. In these insulating covalent crystals (e.g., niobates), the value of n is linked with the bond polarizability α of the lattice ions and the material density (volume) via the Lorentz–Lorenz expression:

$$\left(\frac{\Delta n}{n}\right) = \left(\frac{(n^2-1)\cdot(n^2+2)}{6n^2}\right)\cdot\left(\frac{\Delta V}{V}+\frac{\Delta\alpha}{\alpha}+F\right), \tag{4.14}$$

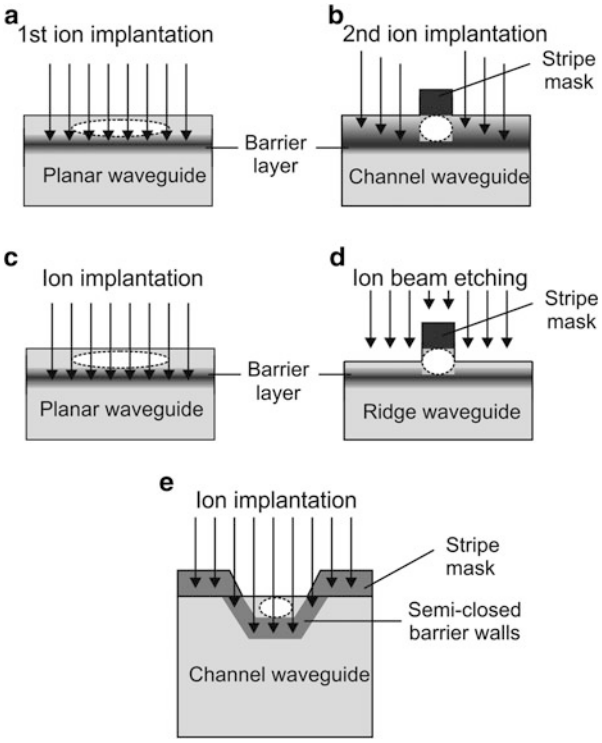

Fig. 4.86 Ion beam processing for barrier-confined waveguides. (**a**) Planar waveguide on the sample surface formed by single implantation step to create a buried vertical barrier wall; (**b**) channel waveguides produced by multiple ion energy implantations to build the side barrier walls with a stripe mask; (**c**) vertical barrier-confined planar waveguide; (**d**) selective etching of the planar waveguide surface regions by patterned etching; (**e**) ion implantation with stripe masks of wedged cross sections, constructing trapezoid cross-section channel waveguides confined by closed barrier walls inside the substrate

where the value of F accounts for the ion beam-induced structural changes of composition, lattice structure, density, and stress of the insulator material. Materials crystallinity implies an efficient packing density of lattice ions and therefore radiation damage, and finally amorphization, reduces the density and then the RI is reduced, for example in $LiNbO_3$, the RI can be lowered up to 10 % by ion irradiation [392].

In the development of integrated optics for communications and signal processing, the control of the RI in a lithographically patterned and well-defined region of the surface or in a buried region is essential. The prerequisite for optical devices is the definition of optical waveguiding paths which result from the trapping of light in a region of high refractive index. Ion implantation in insulating materials always changes the refractive index and, depending on the target material and the ion processing, can either increase or reduce the value of RI. Therefore, if the RI is raised the ion implantation is made into the guiding region. Alternatively, if the RI is decreased, ion irradiation is used to implant the regions adjacent to the guide. Hence, for optically active devices it may be preferable to reduce the index of the regions which act as waveguide boundaries, and so to preserve the optimum crystal quality within the guide. Different waveguide structures have been proposed and realized combining photolithographic patterning, etching, and ion implantation/

irradiation. The ion beam processing for the fabrication of planar, channel, and ridge waveguides is schematically shown in Fig. 4.86.

By optimization of ion implantation and, if necessary, annealing parameters most of these implanted materials show good light guiding properties with acceptably low loss and only minor degradation of bulk crystal properties.

In the majority of cases, the ion implantation in waveguide technology is carried out by high energy (0.5–5 MeV), light ion implantation (H, He), and sometimes by heavy ion implantation (C, O, P, Si, etc.). The light ion implantation requires higher fluences of 10^{15}–10^{16} cm^{-2} than the heavy ion implantation to form the waveguide structure. In some materials, fluences of only ~10^{13} cm^{-2} are sufficient for the heavy ion-implanted waveguide formation. Usually, when high energy H^+ and He^+ ions are implanted into optical crystal substrates, an optical barrier with a lower RI compared to the substrate will be formed, leaving a nearly undisturbed region between the optical barrier and the substrate surface. In the case of heavy ions implanted into the optical crystal, the electronic energy loss S_e is strong enough to change the optical properties in the near-surface region. This change surely weaks the birefringence of the implanted region, resulting in the increase of the RI. The confinement of light in this type of waveguides relies on the enhanced RI layer so that they are sensitive to light polarization direction.

References

1. Furukawa S, Matsumura H, Ishiwara H (1972) Theoretical considerations on lateral spread of implanted ions. Jpn J Appl Phys 11:134
2. Ryssel H, Ruge I (1978) Ion implantation. Akademische Verlagsgesellschaft Geest & Portig K.-G, Leipzig
3. Gibbons JF (1968) Ion implantation in semiconductors – part I: range distribution theory and experiments. Proc IEEE 56:295
4. Ziegler JF, Biersack JP, Littmark U (1985) The stopping and range of ions in matter. Pergamon, New York
5. Maes H, Vandervorst W, van Overstraten R (1981) Impurity profiles of implanted ions in silicon. In: Wang FY (ed) Impurity doping processes in silicon. North-Holland, Amsterdam, p 443, Ch. 7
6. Gibbons JF, Mylroie S (1973) Estimation of impurity profiles in ion implanted amorphous targets using joined half-Gaussian distributions. Appl Phys Lett 22:568
7. Hofker WK (1975) Implantation of boron in silicon. Philips Res Rep Suppl no. 8, pp 1–126
8. Tasch AF, Shin H, Park C et al (1989) An improved approach to accurately model shallow B and BF_2 implants in silicon. J Electrochem Soc 136:810
9. Tasch AF, Yang SH, Morris SJ (1995) Modeling of ion implantation in single-crystal silicon. Nucl Instrum Methods Phys Res B 102:173
10. Zhang H, Gao M, Xu L et al (2008) United Gauss-Pearson-IV distribution model of ions implanted into silicon. Solid State Ionics 179:832
11. Posselt M (1994) Crystal-Trim and its application to investigations on channeling effects during ion implantation. Radiat Eff Def Solids 130–131:87
12. Möller W, Eckstein W (1984) TRIDYN – a TRIM simulation code including dynamic composition changes. Nucl Instrum Methods Phys Res B 2:814
13. Wolf S, Taylor RN (2000) Silicon processing for the VLSI Era, vol. 1: process technology, 2nd edn. Lattice Press, Sunset Beach, CA, p 375

14. Klein K, Park C, Tasch AF et al (1991) Analysis of the tilt and rotation angle dependence of boron distributions implanted into <100> silicon. J Electrochem Soc 138:2102
15. Roy K, Mukhopadhyay S, Mahmoodi-Meimand HS (2003) Leakage current mechanisms and leakage reduction techniques in deep-sub micrometer CMOS circuits. Proc IEEE 91:305
16. Klein KM, Park C, Tasch AF (1991) Modeling of cumulative damage effects on ion-implantation profiles. Nucl Instrum Methods 59–60:60
17. Posselt M, Schmidt B, Murthy CS et al (1997) Modeling of damage accumulation during ion implantation into single-crystalline silicon. J Electrochem Soc 144:1495
18. Simonton R Tash AL (1996) Channeling effects in ion implantation into silicon. In: Ziegler J (ed) Ion implantation science and technology. Ion Implantation Technology Co., pp 293–390
19. Gibbons JF (1972) Ion implantation in semiconductors – part II: damage production and annealing. Proc IEEE 60:1062
20. Morehead FF, Crowder BL, Title RS (1972) Formation of amorphous silicon by ion bombardment as a function of ion, temperature, and dose. J Appl Phys 43:1112
21. Meyer JW, Erikson L, Davies JA (1970) Ion implantation in semiconductors. Academic, New York
22. Harris JS (1971) The effects of dose rate and implantation temperature on lattice damage and electrical activity in ion- implanted GaAs. In: Ruge I, Graul J (eds) Ion implantation in semiconductors. Springer, Berlin, pp 157–167
23. Westmoreland JE, Marsh OJ, Hunsperger RG (1970) Lattice disorder produced in GaAs by 60-keV Cd ions and 70-keV Zn ions. Radiat Eff 5:245
24. Haskell JD, Grant WA, Stephens GA, Whitton LJ (1971) The influence of various parameters on radiation damage in GaP. In: Ruge I, Graul J (eds) Ion implantation in semiconductors. Springer, Berlin, pp 193–198
25. Krimmel EF, Pfleiderer H (1973) Implantation profiles modified by sputtering. Rad Eff 19:83
26. Teichert J, Bischoff L, Hessey E et al (1996) Cobalt disilicide interconnects for micromechanical devices. J Micromech Microeng 6:272
27. Sigmund P (1969) Theory of sputtering. I. Sputtering yield of amorphous and polycrystalline targets. Phys Rev 184:383
28. Winterbon KB, Sigmund P, Sanders JB (1970) Spatial distribution of energy deposited by atomic particles in elastic collisions. Mat Fys Medd Dan Vid Selsk 37(14):1–73
29. Colligon JS (1961) Ion bombardment of metal surfaces. Vacuum 11:272
30. Anderson HH, Bay HL (1975) Heavy-ion sputtering yield of silicon. J Appl Phys 46:1919
31. Behrisch R (ed) (1981) Sputtering by ion bombardment. Springer, Berlin
32. Malherbe JB (1994) Sputtering of compound semiconductor surfaces. I. Ion-solid interactions and sputtering yields. Crit Rev Solid State Mater Sci 19:55
33. Malherbe JB (1994) Sputtering of compound semiconductor surfaces. II. Compositional changes, radiation-induced topography and damage. Crit Rev Solid State Mater Sci 19:128
34. Heera V, Prokert F, Schell L et al (1997) Density and structural changes in SiC after amorphization and annealing. Appl Phys Lett 70:3531
35. Bischoff L, Teichert J (1998) Focused ion beam sputtering of silicon and related materials. Research report, FZR-217, Research Center Rossendorf, pp 25–32
36. Philipp P, Bischoff L (2011) Investigations of conducting nano-structures on ta-C films made by FIB lithography. Nucl Instrum Methods Phys Res B. doi:10.1016/j.nimb.2011.08.057
37. Andersen HH (1979) The depth resolution of sputter profiling. Appl Phys 18:131
38. Schwarz SA, Helms CR (1979) An ion knock-on mixing model with application to Si-SiO_2 interface studies. J Vac Sci Technol 16:781
39. Chu WK, Müller H, Mayer JW, Sigmon TW (1974) Residual disorder in Si from oxygen recoils in annealed "through-oxide" arsenic implants. Appl Phys Lett 25:297
40. Sigmon TW, Chu WK, Müller H, Mayer JW (1975) Enhanced residual disorder in silicon from recoil implantation of oxygen and nitrogen by arsenic implants through dielectric layers. In: Namba S (ed) Ion implantation in semiconductors. Plenum Press, New York, pp 633–639
41. Muline RA, Cullis AG (1975) Residual defects in Si produced by recoil implantation. Appl Phys Lett 26:551

42. Petkov MP, Chen CM, Atwater HA et al (2000) A relation between surface oxide and oxygen-defect complexes in solid-phase epitaxial Si regrown from ion-beam-amorphized Si layers. Appl Phys Lett 76:1410
43. Liu HL, Gearhart SS, Booske JH, Cooper RF (2000) Recoil implantation method for ultrashallow $p(^{+})$/n junction formation. J Appl Phys 87:1957
44. Shao L, Lu X, Jin J et al (2000) Depth profiles of high-energy recoil implantation of boron into silicon. Mater Res Soc Symp 610:B6.8.1
45. Nastasi M, Mayer JW (1994) Ion beam mixing in metallic and semiconductor materials. Mater Sci Eng R Rep 12:1
46. Tsaur BY, Lau SS, Liau ZL, Mayer JW (1979) Ion-beam-induced intermixing of surface layers. Thin Solid Films 63:31
47. Mayer JW, Lau SS (1983) Ion beam mixing. In: Poate JM, Foti G, Jacobson DC (eds) Surface modification and alloying by laser, ion, and electron beams. Plenum, New York, p 241
48. Matteson S, Paine BM, Grimaldi MG et al (1981) Ion beam mixing in amorphous silicon I. Experimental investigation. Nucl Instrum Methods 182–183:43
49. Heinig KH, Hohmuth K, Klabes R et al (1982) Flash lamp annealing of ion implanted silicon. Radiat Eff Def Solids 63:115
50. Heinig KH, Klabes R, Woittennek H (1980) A description of the laser-induced annealing and diffusion behaviour of implanted silicon crystals. Radiat Eff 47:157
51. Appleton BR, Celler GK (eds) (1982) Laser and electron beam interactions with solids. Elsevier North Holland, New York
52. Shima A (2006) Laser annealing technology and device integration challenges. In: 14th IEEE international conference on advanced thermal processing of semiconductors – RTP 2006, pp 11–14
53. Friedrich D, Bernt H, Hanssen H et al (2007) Laser annealing of power devices. In: 15th IEEE international conference on advanced thermal processing of semiconductors – RTP 2007, pp 263–269
54. Paetzel R, Brune J, Simon F et al (2010) Activation of silicon wafer by excimer laser. In: 18th IEEE international conference on advanced thermal processing of semiconductors – RTP 2010, pp 98–102
55. Chen S, Wang X, Thompson M (2010) Characterization of dopant activation, mobility and diffusion in advanced millisecond laser spike annealing. In: 18th IEEE international conference on advanced thermal processing of semiconductors – RTP 2010, pp 66–70
56. Cohen RL, Williams JS, Feldman LC, West KW (1978) Thermally assisted flash annealing of silicon and germanium. Appl Phys Lett 33:751
57. Bomke HA, Berkowitz HL, Harmatz M et al (1978) Annealing of ion-implanted silicon by an incoherent light pulse. Appl Phys Lett 33:955
58. Lue JT (1980) Arc annealing of BF_2^{+} implanted silicon by a short pulse flash lamp. Appl Phys Lett 36:73
59. Fiory AT (2001) Rapid thermal annealing. In: Buschow KHJ et al (eds) Encyclopedia of materials: science and technology. Permagon, Elsevier Science, Amsterdam, pp 8009–8017
60. Kamgar A (1989) Rapid thermal processing of silicon. In: Watts RK (ed) Submicron integrated circuits. Wiley Interscience, New York
61. Roozeboom F, Parekh N (1990) Rapid thermal processing systems: a review with emphasis on temperature control. J Vac Sci Technol B 8:1249
62. Fair RB (ed) (1993) Rapid thermal processing: science and technology. Academic, New York
63. Roozeboom F (ed) (1996) Advances in rapid thermal and integrated processing. Klewer, Dordrecht
64. Sze SM (2002) Semiconductor-device-physics-technology, 2nd edn. Wiley, New York
65. Krynitzky J, Suski J, Ugniewski S (1977) Laser annealing of arsenic implanted silicon. Phys Lett A 61:181
66. Celler GK, Poate JM, Kimerling LC (1978) Spatially controlled crystal regrowth of ion implanted silicon by laser irradiation. Appl Phys Lett 32:464

67. Skorupa W, Gebel T, Yankov RA, Paul S et al (2005) Advanced thermal processing of ultra-shallow implanted junctions using flash lamp annealing. J Electrochem Soc 152:G436–G440
68. Gebel T, Voelskow M, Skorupa W et al (2002) Flash lamp annealing with millisecond pulses for ultra-shallow boron profiles in silicon. Nucl Instrum Methods Phys Res B 186:287
69. Gelpey J, Elliott K, Camm D (2002) Advanced annealing for sub-130 nm junction formation. In: 201st electrochemical society meeting, symposium Q1, rapid thermal and other short-time processing technologies III, May 12–17, 2002, p 735
70. Peuse B, Miner G, Yam M, Elia C (1998) Advances in RTP temperature measurement and control. Mater Res Soc Symp Proc 525:71
71. Singh R (1988) Rapid isothermal processing. J Appl Phys 63:R59–R114
72. Nguyenphu B, Fiory AT (1999) Wafer temperature measurement in a rapid thermal processor with modulated lamp power. J Electron Mater 28:1376
73. Hauf M, Balthasar H, Merkl C, Müller S, Streibel C (1999) Emissivity compensated wafer temperature measurement using intensity-modulated lamp light. In: Roozeboom F et al (eds) Advances in rapid thermal processing. Electrochemical Society, Pennington, NJ, pp 383–390
74. Schietinger C, Adams B, Yarling C (1991) Ripple technique: a novel non-contact wafer emissivity and temperature method for RTP. Mater Res Soc Symp Proc 224:23
75. Saito S, Shishiguchi S, Mineji A, Matsuda T (1998) Ultra shallow junction formation by RTA at high temperature for short heating cycle time. Mater Res Soc Symp Proc 532:3
76. Hebb J, Shajii A (1999) Temperature measurement, uniformity, and control in a furnace-based rapid thermal processing system. In: Roozeboom F et al (eds) Advances in rapid thermal processing. Electrochemical Society, Pennington, NJ, pp 375–382
77. Timans P, Sharangpani R, Thakhur RPS (2000) Rapid thermal processing. In: Nishi Y (ed) Handbook of semiconductor manufacturing technology. Decker, New York
78. Lau SS, Mayer JW, Tseng W (1980) Handbook of semiconductors. North-Holland, Amsterdam
79. Kannan VC, Casey D (1977) Two-step annealing of arsenic-implanted <111> silicon. Appl Phys Lett 31:721
80. Michel AE, Rausch W, Ronsheim PA (1987) Implantation damage and the anomalous transient diffusion of ion-implanted boron. Appl Phys Lett 51:4487
81. Sedwick TO, Michel AE, Deline VR, Cohen SA (1988) Transient boron diffusion in ion-implanted crystalline and amorphous silicon. J Appl Phys 63:1452
82. Fair RB (1990) Point defect charge-state effects on transient diffusion of dopants in Si. J Electrochem Soc 137:667
83. Cowern NEB, Jansen KTF, Jos HFF (1990) Transient diffusion of Ion-implanted B in Si: dose, time, and matrix dependence of atomic and electrical profiles. J Appl Phys 68:6191
84. Jaraiz M, Gilmer GH, Poate JM, de la Rubia TD (1996) Atomistic calculations of ion implantation in Si: point defect and transient enhanced diffusion phenomena. Appl Phys Lett 68:409
85. Suzuki K (2003) Model for transient enhanced diffusion of ion-implanted boron, arsenic, and phosphorous over wide range of process conditions. Fujitsi Sci Technol J 39:138
86. Jones KS, Rozgonyi GA (1993) Extended defects from ion implantation and annealing. In: Fair RB (ed) Rapid thermal processing science and technology. Academic, Boston
87. Talwar S, Wang Y, Gelatos C (2000) Laser thermal processing (LTP) for fabrication of ultra-shallow, hyper-abrupt, highly activated junctions for deca-nanameter MOS transistors. Electrochemical Society Symposium Proceedings PV 2000-9 95
88. Tichy RS, Elliott K, McCoy S, Sing D (2001) Annealing of ultra-shallow implanted junctions using arc-lamp technology: achieving the 90 nm node. In: Proceedings of 9th international conference on advanced thermal processing of semiconductors – RTP 2001, pp 87–93
89. Talwar S, Markle D, Thompson M (2003) Junction scaling using lasers for thermal annealing. Solid State Technol 46:83
90. Borland JO, Matsuda T, Sakamoto K (2002) Shallow and abrupt junction formation: paradigm shift at 65-70 nm. Solid State Technol 45:79
91. Borland JO (2007) 32 nm node USJ implant and annealing options. 15th IEEE international conference on advanced thermal processing of semiconductors – RTP 2007, p 181

92. Mayer JW, Lau SS (1990) Electronic materials science. Integrated circuits in Si and GaAs. Macmillan, New York, pp 183–222
93. Simonton RS, Class W, Erokhin Y et al (2000) In: Nishi Y, Doehring R (eds) Handbook of semiconductor manufacturing technology. New York, Decker
94. Borland JO, Kawski J (1998) Triple well applications profit from MeV implant technology. Semicond Int 21:67
95. Venkatesan S, Lutze JW, Laga C, Taylor WJ (1995) Device drive current degradation observed with retrograde channel profiles. Tech Dig IEDM-95:419–422
96. Parrill TM, Namaroff MJ (1999) Ion implantation productivity for advanced applications. Eur Semicond 1999:44
97. Taur Y, Ning TH (1998) Fundamentals of modern VLSI devices. Cambridge University Press, New York, NY
98. Hori A, Mizuno B (1999) CMOS device technology toward 50 nm region-performance and drain architecture. IEDM Technical Digest International, Washington, DC, pp 641–644
99. Rodder M, Amerasekera A, Aur S, Chen IC (1994) A study of design/process dependence of 0.25 μm gate length CMOS. International electron devices meeting. Technical Digest International, San Francisco, CA, pp 71–74
100. Osborn CM (1990) Formation of silicided, ultra-shallow junctions using low thermal budget processing. J Electron Mater 19:67
101. Schaber H, Criegern RV, Weitzel I (1985) Analysis of polycrystalline silicon diffusion sources by secondary ion mass spectrometry. J Appl Phys 58:4036
102. Aoyame T, Suzuki K, Tashiro H et al (1995) Effect of fluorine on boron diffusion in thin silicon dioxides and oxynitride. J Appl Phys 77:417
103. Murakami T, Kuroi T, Kawasaki Y et al (1997) Application of nitrogen implantation to ULSI. Nucl Instrum Methods Phys Res B 121:257
104. Colombeau B, Smith AJ, Cowern N et al (2004) Electrical deactivation and diffusion of boron in preamorphized ultrashallow junctions: interstitial transport and F co-implant control. Technical Digest IEEE IEDM (2004) p. 971
105. Ota K, Shugihara K, Sayama H et al (2002) Novel locally strained channel technique for high performance 55 nm CMOS. Technical Digest IEEE IEDM (2002) p. 27
106. Hazdra P, Vobecky J, Galster N (2000) A new degree of freedom in diode optimization: arbitrary axial lifetime profiles by means of ion irradiation. ISPSD 2000, May 22–25, Toulouse, France
107. Hazdra P, Brand K, Rubes J, Vobecky J (2001) Local lifetime control by light ion irradiation: impact on blocking capability of power P-i-N diode. Microelectron J 32:449
108. Hazdra P, Vobecky J, Brand K (2002) Optimum lifetime structuring in silicon power diodes by means of various irradiation techniques. Nucl Instrum Methods Phys Res B 186:414
109. Nakano Y, Ishiko M, Tadano H (2002) Deep level centers in silicon introduced by high-energy He irradiation and subsequent annealing. J Vac Sci Technol B 20:379
110. Hazdra P, Brand K, Vobecky J (2001) Effect of defects produced by MeV H and He ion implantation on characteristics of power silicon P-i-N diodes. In: Proceedings of 11th international conference on ion implantation technology 2000, IEEE Press, p 135
111. Hazdra P, Komarnitskyy V (2007) Local lifetime control in silicon power diode by ion irradiation: introduction and stability of shallow donors. IET Circuits Devices Syst 1:321–326
112. Vobecky J, Hazdra P, Homola J (1996) Optimization of power diode characteristics by means of ion irradiation. IEEE Trans Electron Devices 43:2283
113. Ronsisvalle C, Enea V, Abbate C (2011) Effects of back-side He irradiation on MOS-GTO performances. In: Proceedings of 23rd international symposium on power semiconductor devices and ICs (ISPSD) 2011, May 23–26, IEEE Press, San Diego, CA, pp 144–147
114. Deboy G, Marz M, Stengl JP et al (1998) A new generation of high voltage MOSFETs breaks the limit of silicon. Technical Digest IEDM 98, San Francisco, CA, p 683

115. Lorenz L, Deboy G, Knapp A, März M (1999) COOLMOS – a new milestone in high voltage power MOS. Proceedings of ISPSD 1999, Toronto, pp 3–10
116. Saggio M, Fagone D, Musumeci S (2000) MDmesh™: innovative technology for high voltage power MOSFETs. Proceedings of ISPSD 2000, Toulouse, p 65
117. Meijer J, Burchard B, Ivanova K et al (2004) High-energy ion projection for deep ion implantation as a low cost high throughput alternative for subsequent epitaxy processes. J Vac Sci Technol B 22:152
118. von Borany J, Friedrich M, Rüb M et al (2005) Application of ultra-high energy boron implantation for superjunction power (CoolMOS) devices. Nucl Instrum Methods Phys Res B 237:62
119. Rüb M, Bär M, Deboy G et al (2004) 550V superjunction 3.9 Ohmmm^2 transistor formed by 25 MeV masked boron implantation. Proceedings of ISPSD 2004, Kitakyushu, Japan, p 455
120. Schmidt B, Schubert D (1986) Siliciumsensoren. Akademie-Verlag, Berlin
121. Reichel H et al (1989) Halbleitersensoren: Prinzipien, Entwicklungsstand, Technologien, Anwendungsmöglichkeiten. Expert Verlag, Ehningen bei Böblingen
122. Sze SM (1994) Semiconductor sensors. Wiley, New York
123. Lutz G (1999) Semiconductor radiation detectors: device physics. Springer, Berlin
124. Hartmann F (2009) Evolution of silicon sensor technology in particle physics. STMP 231. Springer, Berlin
125. Spieler H (2005) Semiconductor detector systems. Oxford University Press, Oxford
126. Lecrosnier D, Pelous G, Amouroux C et al (1975) Optimization of avalanche silicon photodiodes. Technical digest – international electron devices meeting, Washington, DC, p 595
127. Ripoche G, Harari J (2009) Avalanche photodiodes. In: Decoster D, Harari J (eds) Optoelectronic sensors. ISTE Ltd., London, pp 80–87
128. Kemmer J (1980) Fabrication of low noise silicon radiation detectors by the planar process. Nucl Instrum Methods 169:499
129. Kemmer J, Burger P, Henck R, Heijne E (1982) Performance and applications of passivated ion-implanted silicon detector. IEEE Trans Nucl Sci NS-29:733
130. Kemmer J (1990) Advanced concepts for semiconductor nuclear radiation detectors. Nucl Instrum Methods B 45:247
131. Radeka V, Rahek V, Rescia P et al (1989) Implanted silicon JFET on completely depleted. IEEE Trans Electron Devices Lett ED-10:91
132. Strüder L (1989) Recent developments in semiconductor detectors and on-chip electronics. Nucl Instrum Methods A 283:387
133. Caywood JM, Mead CA, Mayer JW (1970) Influence of carrier diffusion effects on window thickness of semiconductor detectors. Nucl Instrum Methods 79:329
134. Kanno I (1987) Models of formation and erosion of a plasma column in a silicon surface-barrier. Rev Sci Instrum 58:1926
135. von Borany J, Schmidt B, Grötzschel R (1996) The application of high energy ion implantation for silicon radiation detectors. Nucl Instrum Methods Phys Res A 377:514
136. von Borany J, Beyer V, Schmidt B, Schnabel B (2003) A novel silicon detector for energetic electrons with improved linearity characteristics. Microelectron Eng 67–68:140
137. Deutscher M (1989) Ein Justierdetektor für Elektronenformstrahlen. Habilitations-schrift, Teil D, AdW der DDR
138. Seibt W, Sundström KE, Tove PA (1973) Charge collection in silicon detectors for strongly ionizing particles. Nucl Instrum Methods 113:317
139. Finch EC, Asghar M, Forte M (1979) Plasma and recombination effects in the fission fragment pulse height defect in a surface barrier detector. Nucl Instrum Methods 163:467
140. Hellings G, Mitard J, Eneman G et al (2009) High performance 70-nm germanium pMOSFETs with boron LDD implants. IEEE Electron Device Lett 30:88
141. Jones R, Thomas S, Bharatan S et al (2002) Fabrication and modeling of gigahertz photodetectors in heteroepitaxial Ge-on-Si using a graded buffer layer deposition by low

energy plasma enhanced CVD. Proceedings of international electron devices meeting (IEDM), 2002, p 793
142. Simoen E, Satta A, D'Amore A et al (2006) Ion-implantation issues in the formation of shallow junctions in germanium. Mater Sci Semicond Process 9:634
143. Brunco DP, De Jaeger B, Eneman G et al (2008) Germanium MOSFET devices: advances in materials understanding, process development, and electrical performance. J Electrochem Soc 155:H552
144. Satta A, Simoen E, Clarysse T et al (2005) Diffusion, activation, and recrystallization of boron implanted in preamorphized and crystalline germanium. Appl Phys Lett 87:172109
145. Hellings G, Wuendisch C, Eneman G et al (2009) Implantation, diffusion, activation, and recrystallization of gallium implanted in preamorphized and crystalline germanium. Electrochem Solid State Lett 12:H417
146. Chui CO, Kulig L, Moran J, Tsai W, Saraswat KC (2005) Germanium n-type shallow junction activation dependences. Appl Phys Lett 87:091909
147. Posselt M, Schmidt B, Anwand W et al (2008) Implantation into preamorphized germanium and subsequent annealing: Solid phase epitaxial regrowth, P diffusion, and activation. J Vac Sci Technol B 26:430
148. Wündisch C, Posselt M, Schmidt B et al (2009) Millisecond flash lamp annealing of shallow implanted layers in Ge. Appl Phys Lett 95:252107
149. Satta A, Simoen E, Duffy R et al (2006) Diffusion, activation, and regrowth behavior of high dose P implants in Ge. Appl Phys Lett 88:162118
150. Janssens T, Huyghebaert C, Vanhaeren D et al (2006) Heavy ion implantation in Ge: dramatic radiation induced morphology in Ge. J Vac Sci Technol B 24:510
151. Darby BL, Yates BR, Rudawski NG et al (2011) Insights for void formation in ion-implanted Ge. Thin Solid Films 519:5962
152. Kögler R, Mücklich A, Skorupa W et al (2007) Vacancies in high energy ion implanted SiGe. J Appl Phys 101:033508
153. Holland OW, Appleton BR, Narayan J (1983) Ion implantation damage and annealing in germanium. J Appl Phys 54:2295
154. Huber H, Assmann W, Karamian SA et al (1997) Void formation in Ge induced by high energy heavy ion irradiation. Nucl Instrum Methods Phys Res B 122:542
155. Nitta W, Taniwaki M, Hayashi Y, Yoshiie T (2002) Formation of cellular defect structure on GaSb ion-implanted at low temperature. J Appl Phys 92:1799
156. Romano L, Impellizzeri G, Tomasello MV et al (2010) Nanostructuring in Ge by self-ion implantation. J Appl Phys 107:084314
157. Wilson IH (1982) The effects of self-ion bombardment (30–500 keV) on the surface topography of single-crystal germanium. J Appl Phys 53:1698
158. Ghaly M, Nordlund K, Averback RS (1999) Molecular dynamics investigations of surface damage produced by kiloelectronvolt self-bombardment of solids. Philos Mag A 79:795
159. Kim JC, Cahill DG, Averback RS (2005) Surface defects created by 20 keV Xe ion irradiation of Ge(111). Surf Sci 574:175
160. Herrmannsdoerfer T, Heera V, Ignatchik O et al (2009) Superconducting state in a gallium-doped germanium layer at Low temperatures. Phys Rev Lett 102:217003
161. Zhou S, Bürger D, Mücklich A et al (2010) Hysteresis in the magnetotransport of manganese-doped germanium: evidence for carrier-mediated ferromagnetism. Phys Rev B 81:165204
162. Sealy BJ (1988) Ion implantation doping of semiconductors. Int Mater Rev 33:38
163. Wesch W, Götz G (1986) Rapid annealing of ion-implanted GaAs. Physica Status Solidi A 94:745
164. Pearton SJ, Poate JM, Sette F et al (1987) Ion implantation in GaAs. Nucl Instrum Methods Phys Res B 19/20:369
165. Dodadalapur A, Streetman BG (1990) Implantation in InP-the role of stoichiometric imbalances. Electrochem Soc Symp Proc 90–13:66

166. Rao MV (1992) Rapid thermal annealing of ion-implanted InP, InGaAs, and InSb. Proc SPIE 1595:108
167. Pearton SJ, Chakrabarti UK (1992) Novel dry etch chemistries for InP and related compounds. In: Katz A (ed) Indium phosphide and related materials: processing, technology and devices. Artech House, Norwood, MA, pp 420–426
168. Rao MV (1993) Ion implantation in III–V compound semiconductors. Nucl Instrum Methods Phys Res B 79:645
169. de Souza JP, Sadana DK (1992) Ion implantation in gallium arsenide MESFET technology. IEEE Trans Electron Devices ED-39:166
170. Rao MV, Nadella RK, Holland OW (1992) Elevated temperature 3 MeV Si and 150 keV Ge implants in InP:Fe. J Appl Phys 71:126
171. Rao MV, Nadella RK (1990) Be^+/P^+, Be^+/Ar^+, and Be^+/N^+ coimplantations into InP:Fe. J Appl Phys 67:1761
172. Gill SS, Sealy BJ (1986) Review of rapid thermal annealing of ion implanted GaAs. J Electrochem Soc 133:2590
173. Pearton SJ, Jalali B, Abernathy CR et al (1992) Isolation properties and experimental ranges of high energy ions in GaAs and InP. J Appl Phys 71:2663
174. Vellanki J, Nadella RK, Rao MV (1993) Highly conductive buried n^+ layers in lnP:Fe created by MeV energy Si, S, and Si/S implantation for application to microwave devices. J Electron Mater 22:73
175. Pearton SJ, Zolper JC, Shul RJ, Ren F (1999) GaN: processing, defects, and devices. J Appl Phys 86:1
176. Zolper JC (1997) Ion implantation in group III-nitride semiconductors: a tool for doping and defect studies. J Cryst Growth 178:157
177. Wilson RG, Zavada JM, Cao XA et al (1999) Redistribution and activation of implanted S, Se, Te, Be, Mg, and C in GaN. J Vac Sci Technol A 17:1226
178. Cao XA, Abernathy CR, Singh RK et al (1998) Ultrahigh Si^+ implant activation efficiency in GaN using a high-temperature rapid thermal process system. Appl Phys Lett 73:229
179. Kucheyev SO, Williams JS, Pearton SJ (2001) Ion implantation into GaN. Mater Sci Eng R Rep 33:51–107
180. Cao XA, Pearton SJ, Dang GT (2000) Creation of high resistivity GaN by implantation of Ti, O, Fe, or Cr. J Appl Phys 87:1091
181. Neudeck PG (1994) Progress towards high temperature, high power SiC devices. Institute of Physics Conference Series 141: Compound Semiconductors, pp 1–6
182. Rao MV (2003) Maturing ion-implantation technology and its device applications in SiC. Solid State Electron 47:213
183. Choyke WJ, Matsunami H, Pensl G (2004) Silicon carbide recent major advances. Springer, Berlin
184. Handy EM, Rao MV, Holland OW et al (2000) Al, B, and Ga ion-implantation doping of SiC. J Electron Mater 29:1340
185. Capano MA, Ryu S, Melloch MR et al (1998) Dopant activation and surface morphology of ion implanted 4H- and 6H-silicon carbide. J Electron Mater 27:370
186. Handy EM, Rao MV, Jones KA (1999) Effectiveness of AlN encapsulant in annealing ion-implanted SiC. J Appl Phys 86:746
187. Wirth H, Panknin D, Skorupa W, Niemann E (1999) Efficient p-type doping of 6H-SiC: Flash-lamp annealing after aluminum implantation. Appl Phys Lett 74:979
188. Reiss S, Heinig KH (1994) Ostwald ripening during ion beam synthesis – a computer simulation for inhomogeneous systems. Nucl Instrum Methods Phys Res B 84:229
189. Goodrich FC, Rusanov AI (eds) (1981) The modern theory of capillarity. Akademie Verlag, Berlin
190. Ostwald W (1897) Studien über die Bildung fester Körper. 1. Abhandlung: "Übersättigung und Überkaltung". Z Phys Chem 22:289
191. Lifshitz LM, Slyozov VV (1961) The kinetics of precipitation from supersaturated solid solutions. J Phys Chem Solids 19:35

192. Wagner C (1961) Theorie der Alterung von Niederschlägen durch Umlösen (Ostwald-Reifung). Z Electrochem 65:581
193. Reiss S, Weber R, Heinig KH, Skorupa W (1994) Experimental study and modeling of structure formation in buried layers at ion beam synthesis. Nucl Instrum Methods Phys Res B 89:337
194. Strobel M (1999) Modeling and computer simulations of ion beam synthesis of nanostructures. Ph.D. dissertation, University of Technology, Dresden, Germany
195. Strobel M, Heinig KH, Möller W (2001) Three-dimensional domain growth on the size scale of the capillary length: effective growth exponent and comparative atomistic and mean-field simulations. Phys Rev B 64:245422
196. Schmitz G, Haasen P (1992) Decomposition of an AlLi alloy – the early stages observed by HREM. Acta Metallurgica et Materialia 40:2209
197. Calderon HA, Voorhees PW, Murray JL, Kostorz G (1994) Ostwald ripening in concentrated alloys. Acta Metallurgica et Materialia 42:991
198. Mazzoldi P, Arnold GW, Battaglin G et al (1994) Peculiarities and application perspectives of metal-ion implants in glasses. Nucl Instrum Methods B 91:478
199. Atwater HA, Shcheglov KV, Wong SS et al (1994) Ion beam synthesis of luminescent SI and GE nanocrystals in a silicon dioxide matrix. Mater Res Soc Symp Proc 316:409
200. Mantl S (1992) Ion beam synthesis of epitaxial silicides: fabrication, characterization and applications. Mater Sci Rep 8:1
201. Zuhr RA, Magruder RH, Anderson TA, Wittig JE (1994) Nanosize metal alloy particle formation in AG and CU sequentially implanted silica. Mater Res Soc Symp Proc 316:457
202. Zhu JG, White CW, Budai JD et al (1995) Growth of Ge, Si, and SiGe nanocrystals in SiO_2 matrices. J Appl Phys 78:4386
203. White CW, Budai JD, Zhu JG et al (1995) Compound semiconductor nanocrystals formed by sequential ion implantation. Mater Res Soc Symp Proc 358:169
204. White CW, Budai JD, Zhu JG et al (1996) Ion beam synthesis and stability of GaAs nanocrystals in silicon. Appl Phys Lett 68:2389
205. Christoloveanu S (1989) Advanced silicon on insulator materials: processing, characterization and devices. In: Harbeke G, Schulz MJ (eds) Semiconductor silicon. Springer, Berlin, pp 223–249
206. Colinge JP (1997) Silicon-on-insulator technology: materials to VLSI, 2nd edn. Kluwer, Boston, pp 32–44, Chapter 2
207. Celler GK, Cristoloveanu S (2003) Frontiers of silicon-on-insulator. J Appl Phys 93:4955
208. Reeson KJ (1987) Fabrication of buried layers of SiO_2 and Si_3N_4 a using ion beam synthesis. Nucl Instrum Methods Phys Res B 19–20:269
209. Hatzopoulos N, Bussmann U, Robinson AK, Hemment PLF (1991) Buried insulator formation by nitrogen implantation at elevated temperatures. Nucl Instrum Methods Phys Res B 55:734
210. Zhang E, Yi W, Chen J et al (2005) Research on the effect of nitrogen implantation doses on the structure of separation by implantation of oxygen and nitrogen. Smart Mater Struct 14: N42
211. Maydell-Ondrusz EA, Wilson IH (1984) A model for the evolution of implanted oxygen profiles in silicon. Thin Solid Films 114:357
212. Jäger HU, Hensel E, Kreissig U et al (1985) A model for the oxidation of silicon by high dose oxygen implantation. Thin Solid Films 123:159
213. Jäger HU (1986) Model investigations of the oxidation of silicon by high dose implantation. Nucl Instrum Methods Phys Res B 15:748
214. Jäger HU (1987) Improved modeling of oxygen depth profiles in high dose oxygen-implanted silicon. Phys Stat Sol (a) 103:K75
215. Nakashima S, Katayama T, Miyamura Y et al (1994) Thickness increment of buried oxide in a SIMOX wafer by high-temperature oxidation. In: Proceedings of IEEE International SOI Conference (1994), pp 71–72

216. Kawamura K, Deai H, Morikawa Y et al (1996) Gate oxide integrity on ITOX-SIMOX wafers. In: Proceedings of IEEE International SOI Conference (1996), pp 162–163
217. Maszara WP, Bennett J, Boden T et al (1997) Low dose SIMOX and impact of ITOX process on quality of SOI film. In: Proceedings of IEEE International SOI Conference (1997) pp 18–19
218. Dong Y, Chen M, Chen J et al (2004) Patterned buried oxide layers under a single MOSFET to improve the device performance. Semicond Sci Technol 19:L25
219. White AE, Short KT, Dynes RC et al (1987) Mesotaxy: single-crystal growth of buried $CoSi_2$ layers. Appl Phys Lett 50:95
220. White AE, Short KT (1988) Synthesis of buried oxide and silicide layers with ion beams. Science 241:930
221. White AE, Short KT, Dynes RC et al (1989) Mesotaxy: synthesis of buried single-crystal silicide layers by implantation. Nucl Instrum Methods Phys Res B 39:253
222. Mantl S, Jebasinski R, Hartmann D (1991) The effect of dose on the growth of buried $CoSi_2$ layers in (111) and (100) Si produced by ion implantation. Nucl Instrum Methods Phys Res B 59–60:666
223. Van Ommen A, Bulle-Lieuwma CWT, Ottenheim JJM, Theunissen AML (1990) Ion beam synthesis of heteroepitaxial Si/$CoSi_2$/Si structures. J Appl Phys 67:1767
224. Hensel JC, Tung RT, Poate JM, Unterwald FC (1984) Electrical transport properties of $CoSi_2$ and $NiSi_2$ thin films. Appl Phys Lett 44:913
225. Vanheilemont J, Bender H, Wu MF et al (1993) Implantation temperature dependent distribution of $NiSi_2$ formed by ion beam synthesis in silicon. Appl Phys Lett 62:2795
226. Hsu JY, Liang JH (2005) An investigation of annealing effect on forming nickel disilicide by ion beam synthesis. Nucl Instrum Methods Phys Res B 241:543
227. Liang JH, Chao DS (2001) Formation of tungsten silicide films by ion beam synthesis. Surf CoatTechnol 140:116
228. White AE, Short KT, Maex K et al (1991) Exploiting Si/$CoSi_2$/Si heterostructures grown by mesotaxy. Nucl Instrum Methods Phys Res B 59–60:693
229. Radermacher K, Mantl S, Dieker C, Lüth H (1991) Ion beam synthesis of buried α-$FeSi_2$ and β-$FeSi_2$ layers. Appl Phys Lett 59:2145
230. Homewood KP, Reeson KJ, Gwilliam RM et al (2001) Ion beam synthesized silicides: growth, characterization and devices. Thin Solid Films 381:188
231. Golanski A, Christie WH, Galloway MD et al (1991) Ion beam induced diffusion and crystallization in high-dose Er implanted Si. Nucl Instrum Methods Phys Res B 59–60:444
232. Hogg SM, Vantomme A, Wu MF, Langouche G (2000) Electrical properties of rare earth silicides produced by channeled ion beam synthesis. Microelectron Eng 50:211
233. Bischoff L, Heinig KH, Teichert J, Skorupa W (1996) Submicron $CoSi_2$ structures fabricated by focused ion beam implantation and local flash lamp melting. Nucl Instrum Methods Phys Res B 112:201
234. Hausmann S, Bischoff L, Teichert J (1998) Dose rate effects in focused ion beam synthesis of cobalt disilicide. Appl Phys Lett 72:2719
235. Akhmadaliev C, Schmidt B, Bischoff L (2006) Defect induced formation of $CoSi_2$ nanowires by focused ion beam synthesis. Appl Phys Lett 89:223129
236. Heinig KH (1984) Effects of transient local melting on semiconductor surfaces. In: Proceedings of international conference on energy pulse modification of semiconductors and related materials, EPM '84. Dresden, p 265
237. Calvo P, Claverie A, Cherkashin N et al (2004) Thermal evolution of 113 defects in silicon: transformation against dissolution. Nucl Instrum Methods Phys Res B 216:173
238. Buchal C, Withrow SP, White CW, Poker DB (1994) Ion implantation of optical materials. Annu Rev Mater Sci 24:125
239. Meldrum A, Haglund RF, Boatner LA, White CW (2001) Nanocomposite materials formed by ion implantation. Adv Mater 13:1431

240. Heinig K, Müller T, Schmidt B et al (2003) Interfaces under ion irradiation: growth and taming of nanostructures. Appl Phys A Mater Sci Process 77:17
241. Skorupa W, Rebohle L, Gebel T (2003) Group-IV nanocluster formation by ion-beam synthesis. Appl Phys A Mater Sci Process 76:1049
242. Mazzoldi P, Mattei G (2007) Some aspects of ion implantation technique in nanostructured materials. Phys Stat Sol (a) 204:621
243. Flytzanis C, Hache F, Klein MC et al (1991) Nonlinear optics in composite materials. In: Wolf E (ed) Progress in optics, vol 29. North-Holland, Amsterdam, pp 321–411
244. Magruder RH, Kinser DL, Wittig JE, Zuhr RA (1992) Structure property relationships of nanometer-size metal clusters in glasses. Proc SPIE 1761:180
245. Magruder RH, Haglund RF, Yang L et al (1994) Physical and optical properties of Cu nanoclusters fabricated by ion implantation in fused silica. J Appl Phys 76:708
246. Hosono H, Fukushima H, Abe Y et al (1992) Cross-sectional TEM observation of copper-implanted SiO_2 glass. J Non Cryst Sol 143:157
247. Matsunami N, Hosono H (1993) Colloid formation effects on depth profile of implanted Ag in SiO_2 glass. Appl Phys Lett 63:2050
248. Matsumi N, Hosono H (1993) Anomalous fringe pattern of Ag colloid in phosphate glasses by implantation. Nucl Instrum Methods Phys Res B 80/81:1233
249. Mazzoldi P, Tramontin L, Boscolo-Boscoletto A et al (1993) Substrate effects in silver-implanted glasses. Nucl Instrum Methods Phys Res B 80/81:1192
250. Magruder RH, Yang L, Huglund RF et al (1993) Optical properties of gold nanocluster composites formed by deep ion implantation in silica. Appl Phys Lett 62:1730
251. White CW, Zhou DS, Budai JD, Zuhr RA (1994) Colloidal Au nanoclusters formed in fused silica by MeV ion implantation and annealing. Mater Res Soc Symp Proc 316:499
252. Strobel M, Heinig K, Möller W (1999) Ion beam synthesis of gold nanoclusters in SiO_2: computer simulations versus experiments. Nucl Instrum Methods Phys Res B 147:343
253. Fukumi K, Chayahara A, Kadono K et al (1994) Gold nanoparticles ion implanted in glass with enhanced nonlinear optical properties. J Appl Phys 75:3075
254. KimerIing LC, Kolenbrander KD, Michel J, Palm J (1996) Light emission from silicon. Solid State Phys 50:333
255. Walters RJ, Kalkman J, Polman A et al (2006) Photoluminescence quantum efficiency of dense silicon nanocrystal ensembles in SiO_2. Phys Rev B 73:132302
256. Pavesi L, Dal Negro L, Mazzoleni C et al (2000) Optical gain in silicon nanocrystals. Nature 408:440
257. Conibeer G, Green M, Corkish R et al (2006) Silicon nanostructures for third generation photovoltaic solar cells. Thin Solid Films 511–512:654
258. Alfond TL, Theodore ND (1994) Backscattering and electron microscopy study of mega-electron volt gold implantation into silicon. J Appl Phys 76:7265
259. Wendler E, Herrmann U, Wesch W, Dunken HH (1996) Structural changes and Si redistribution in Si^+ implanted silica glass. Nucl Instrum Methods Phys Res B 116:332
260. Zhu JG, White CW, Budai JD, Withrow SP, Chenb Y (1995) Growth of Ge, Si, and SiGe nanocrystals in SiO_2 matrices. J Appl Phys 78:4386
261. von Borany J, Grötzschel R, Heinig KH et al (1997) Multimodal impurity redistribution and nanocluster formation in Ge implanted silicon dioxide films. Appl Phys Lett 71:3215
262. Heinig KH, Schmidt B, Markwitz A et al (1999) Precipitation, ripening and chemical effects during annealing of Ge^+ implanted SiO_2 layers. Nucl Instrum Methods Phys Res B 148:969
263. Markwitz A, Schmidt B, Matz W et al (1998) Microstructural investigation of ion beam synthesised germanium nanoclusters embedded in SiO_2 layers. Nucl Instrum Methods Phys Res B 142:338
264. Oswald S, Schmidt B, Heinig KH (2000) XPS investigation with factor analysis for the study of Ge clustering in SiO_2. Surf Interface Anal 29:249
265. Borodin VA, Heinig KH, Schmidt B (1998) Modeling of Ge nanocluster evolution in ion-implanted SiO_2 layer. Nucl Instrum Methods Phys Res B 147:286

266. Tiwari S, Rana F, Chan K et al (1995) Volatile and non-volatile memories in silicon with nano-crystal storage. IEEE International Electron Devices Meeting Technical Digest, p 521
267. Devine RAB (1994) Macroscopic and microscopic effects of radiation in amorphous SiO_2. Nucl Instrum Methods Phys Res B 91:378
268. Schmidt B, Grambole D, Herrmann F (2002) Impact of ambient atmosphere on as-implanted amorphous insulating layers. Nucl Instrum Methods Phys Res B 191:482
269. Claverie A, Bonafos C, Ben Assayag G et al (2006) Materials science issues for the fabrication of nanocrystal memory devices by ultra low energy ion implantation. Defect Diffus Forum 258–260:531
270. Müller T, Heinig KH, Möller W (2002) Materials science issues for the fabrication of nanocrystal memory devices by ultra low energy ion implantation. Appl Phys Lett 81:3049
271. Müller T, Heinig KH, Möller W et al (2004) Multi-dot floating-gates for nonvolatile semiconductor memories: their ion beam synthesis and morphology. Appl Phys Lett 85:2373
272. Brongersma ML, Polman A, Min MS et al (1998) Tuning the emission wavelength of Si nanocrystals in SiO_2 by oxidation. Appl Phys Lett 72:2577
273. Skorupa W, Rebohle L, Gebel T (2003) Group-IV nanocluster formation by ion-beam synthesis. Appl Phys A 76:1049
274. Tiwari S, Rana F, Hanafi H et al (1996) A silicon nanocrystals based memory. Appl Phys Lett 68:1377
275. Fu Y, Dutta A, Willander M, Oda S (2000) Carrier conduction in a Si-nanocrystal-based single-electron transistor – I. Effect of gate bias. Superlattices Microstruct 28:177
276. Lopez M, Garrido B, Bonafos C (2001) Model for efficient visible emission from Si nanocrystals ion beam synthesized in SiO_2. Nucl Instrum Methods Phys Res B 178:89
277. Iwayama TS, Hama T, Hole DE, Boyd IW (2002) Optical and structural properties of encapsulated Si nanocrystals formed in SiO_2 by ion implantation. Surf Coat Technol 158–159:712
278. Cheylan S, Elliman RG (1999) The effect of ion dose and annealing ambient on room temperature photoluminescence from Si nanocrystals in SiO_2. Nucl Instrum Methods Phys Res B 148:986
279. Bonafos C, Columbeau B, Altibelli A et al (2001) Kinetic study of group IV nanoparticles ion beam synthesized in SiO_2. Nucl Instrum Methods Phys Res B 178:17
280. Linnros J, Lalic N, Galeckas A, Grivickas V (1999) Analysis of the stretched exponential photoluminescence decay from nanometer-sized silicon crystals in SiO_2. J Appl Phys 86:6128
281. Kik PG, Brongersma ML, Polman A (2000) Strong exciton-erbium coupling in Si nanocrystal-doped SiO_2. Appl Phys Lett 76:2325
282. Kik PG, Polman A (2000) Exciton–erbium interactions in Si nanocrystal-doped SiO_2. J Appl Phys 88:1992
283. Kik PG, Polman A (2001) Exciton–erbium energy transfer in Si nanocrystal-doped SiO_2. Mater Sci Eng B 81:3
284. Polman A (2002) Photonic materials: teaching silicon new tricks. Nat Mater 1:10
285. Koshida N (ed) (2006) Device applications of silicon nanocrystals and nanostructures. Springer, Berlin
286. Pavesi L, Turan R (2010) Silicon nanocrystals: fundamentals, sythesis and applications. Wiley-VCH, Weinheim
287. von Borany J, Gebel T, Stegemann KH (2002) Memory properties of Si^+ implanted gate oxides: from MOS capacitors to nvSRAM. Solid State Electron 46:1729
288. Normand P, Kapetanakis E, Dimitrakis P et al (2003) Effect of annealing environment on the memory properties of thin oxides with embedded Si nanocrystals obtained by low-energy ion-beam synthesis. Appl Phys Lett 83:168
289. Dimitrakis P, Kapetanakis E, Tsoukalas D et al (2004) Silicon nanocrystal memory devices obtained by ultra-low-energy ion-beam synthesis. Solid State Electron 48:1511

290. Normand P, Kapetanakis E, Dimitrakis P et al (2004) Nanocrystals manufacturing by ultra-low-energy ion-beam-synthesis for non-volatile memory applications. Nucl Instrum Methods Phys Res B 216:228
291. Beyer V, von Borany J, Klimenkov M, Müller T (2009) Current-voltage characteristics of metal-oxide-semiconductor devices containing Ge or Si nanocrystals in thin gate oxides. J Appl Phys 106:064505
292. Compagnoni CM, Ielmini D, Spinelli AS (2003) Study of data retention for nanocrystal Flash memories. In: Proceedings of the 41st annual international reliability physics symposium, pp 506–512
293. Tiwari S, Wahl JA, Silva H et al (2000) Small silicon memories: confinement, single-electron, and interface state considerations. Appl Phys A 71:403
294. Normand P, Dimitrakis P, Kapetanakis E et al (2004) Processing issues in silicon nanocrystal manufacturing by ultra-low-energy ion-beam-synthesis for non-volatile memory applications. Microelectron Eng 73–74:730
295. Carrada M, Cherkashin N, Bonafos C et al (2003) Effect of ion energy and dose on the positioning of 2D-arrays of Si nanocrystals ion beam synthesised in thin SiO_2 layers. Mater Sci Eng B 101:204
296. Schmidt B, Heinig KH, Röntzsch L et al (2006) Ion irradiation through SiO_2/Si interfaces: non-conventional fabrication of Si nanocrystals for memory applications. Nucl Instrum Methods Phys Res B 242:146
297. von Borany J, Grötzschel R, Heinig KH et al (1999) The formation of narrow nanocluster bands in Ge-implanted SiO_2-layers. Solid State Electron 43:1159
298. Heinig KH, Müller T, Schmidt B, Strobel M, Möller W (2003) Interfaces under ion irradiation: growth and taming of nanostructures. Appl Phys A 77:17
299. Heinig KH, Schmidt B, Strobel M, Bernas H (2001) inverse ostwald ripening and self-organization of nanoclusters due to ion irradiation. Mater Res Soc Symp Proc 650:R9.6/O14.6
300. Schmidt B, Heinig KH, Mücklich A (2001) Evolution of ion beam synthesized Au nanoclusters in SiO_2 under ion irradiation. Mater Soc Symp Proc 647:O11.20
301. Röntzsch L, Heinig KH, Schmidt B (2004) Experimental evidence of Si nanocluster δ-layer formation in buried and thin SiO_2 films induced by ion irradiation. Mater Sci Semicond Process 7:357
302. Röntzsch L, Heinig KH, Schmidt B et al (2005) Direct evidence of self-aligned Si nanocrystals formed by ion irradiation of Si/SiO_2 interfaces. Phys Stat Sol (a) 202:R170
303. Bruel M (1995) Silicon on insulator material technology. Electron Lett 31:1201
304. Aspar B, Bruel M, Moriceau H (1997) Basic mechanisms involved in the Smart-Cut® process. Microelectron Eng 36:233
305. Bruel M (1996) Application of hydrogen ion beams to Silicon on Insulator material technology. Nucl Instrum Methods Phys Res B 108:313
306. Tong QY, Gösele U (1999) Semiconductor wafer bonding: science and technology. Wiley, New York
307. Bruel M, Aspar B, Auberton-Herve AJ (1997) Smart-Cut: a new silicon on insulator material technology based on hydrogen implantation and wafer bonding. Jpn J Appl Phys 36:1636
308. Aspar B, Lagahe C, Moriceau H et al (1998) Kinetics of splitting in the Smart-Cut^R process. Proc IEEE Int SOI Conf 1998:137–138
309. Nastasi M, Mayer JW (2006) Ion implantation and synthesis of materials. Springer, Berlin, p 152
310. Tesmer JR, Nastasi M (eds) (1995) Handbook of modern ion beam analysis. Materials Research Society, Pittsburgh, PA
311. Di Cioccio L, Leitec Y, Letertre F et al (1996) Silicon carbide on insulator formation using the Smart Cut process. Electron Lett 32:1144

312. Akatsu T, Deguet C, Sanchez L et al (2006) Germanium-on-insulator (GeOI) substrates – a novel engineered substrate for future high performance devices. Mater Sci Semicond Process 9:444
313. Jalaguier E, Aspar B, Pocas S et al (1998) Transfer of 3 in GaAs film on silicon substrate by proton implantation process. Electron Lett 34:408
314. Tauzin A, Akatsu T, Rabarot M et al (2005) Transfers of 2-inch GaN films onto sapphire substrates using Smart Cut^{TM} technology. Electron Lett 41:668
315. Moriceau H, Fournel F, Aspar B et al (2003) New layer transfers obtained by the Smart Cut process. J Electron Mater 32:829
316. Izuhara T, Gheorma IL, Osgood RM et al (2003) Single-crystal barium titanate thin films by ion slicing. Appl Phys Lett 82:616
317. Carter G (2001) The physics and applications of ion beam erosion. J Phys D Appl Phys 34:R1
318. Ziberi B, Frost F, Höche T, Rauschenbach B (2005) Ripple pattern formation on silicon surfaces by low-energy ion-beam erosion: experiment and theory. Phys Rev B 72:235310
319. Ziberi B, Frost F, Rauschenbach B (2006) Formation of large-area nanostructures on Si and Ge surfaces during low energy ion beam erosion. J Vac Sci Technol A 24:1344
320. Keller A, Facsko S, Möller W (2009) The morphology of amorphous SiO_2 surfaces during low energy ion sputtering. J Phys Condens Matter 21:495305
321. Facsko S, Dekorsy T, Koerdt C et al (1999) Formation of ordered nanoscale semiconductor dots by ion sputtering. Science 285:1551
322. Carter G, Nobes MJ, Paton F et al (1977) Ion bombardment induced ripple topography on amorphous solids. Radiat Eff Defects Solids 33:65
323. Chan WL, Chason E (2007) Making waves: kinetic processes controlling surface evolution during low energy ion sputtering. J Appl Phys 101:121301
324. Brown AD, Erlebacher J (2005) Temperature and fluence effects on the evolution of regular surface morphologies on ion-sputtered Si(111). Phys Rev B 72:075350
325. Ozaydin G, Ozcan AS, Wang YY (2005) Real-time X-ray studies of Mo-seeded Si nanodot formation during ion bombardment. Appl Phys Lett 87:163104
326. Zhou J, Facsko S, Lu M, Möller W (2011) Nanopatterning of Si surfaces by normal incident ion erosion: influence of iron incorporation on surface morphology evolution. J Appl Phys 109:104315
327. Macko S, Frost F, Ziberi B et al (2010) Is keV ion-induced pattern formation on Si(001) caused by metal impurities? Nanotechnology 21:085301
328. Ziberi B, Frost F, Tartz M (2008) Ripple rotation, pattern transitions, and long range ordered dots on silicon by ion beam erosion. Appl Phys Lett 92:063102
329. Bischoff L, Pilz W, Schmidt B (2011) Amorphous solid foam structures on germanium by heavy ion irradiation. Appl Phys A 104:1153
330. Bischoff L, Heinig KH, Schmidt B et al (2012) Self-organization of Ge nanopattern under erosion with heavy Bi monomer and cluster ions. Nucl Instrum Methods Phys Res B 272:198–201
331. Bradley RM, Harper JME (1988) Theory of ripple topography induced by ion bombardment. J Vac Sci Technol A 6:2390
332. Sigmund P (1973) A mechanism of surface micro-roughening by ion bombardment. J Mater Sci 8:1545
333. Cuerno R, Barabasi AL (1995) Dynamic scaling of ion-sputtered surfaces. Phys Rev Lett 74:4746
334. Makeev MA, Barabasi AL (1997) Ion-induced effective surface diffusion in ion sputtering. Appl Phys Lett 71:2800
335. Carter G, Vishnyakov V (1996) Roughening and ripple instabilities on ion-bombarded Si. Phys Rev B 54:17647
336. Makeev MA, Cuerno R, Barabasi AL (2002) Morphology of ion-sputtered surfaces. Nucl Instrum Methods Phys Res B 197:185

337. Munoz-Garcia J, Castro M, Cuerno R (2006) Nonlinear ripple dynamics on amorphous surfaces patterned by ion beam sputtering. Phys Rev Lett 96:086101
338. Chason E, Chan WL (2009) Kinetic Monte Carlo simulations compared with continuum models and experimental properties of pattern formation during ion beam sputtering. J Phys Condens Matter 21:224016
339. Kalyanasundaram N, Freund JB, Johnson HB (2009) A multiscale crater function model for ion-induced pattern formation in silicon. J Phys Condens Matter 21:224018
340. Liedke MO, Liedke B, Keller A (2007) Induced anisotropies in exchange-coupled systems on rippled substrates. Phys Rev B 75:220407(R)
341. Oates TWH, Keller A, Noda S, Facsko S (2008) Self-organized metallic nanoparticle and nanowire arrays from ion-sputtered silicon templates. Appl Phys Lett 93:063106
342. Toulemonde M, Dufour C, Wang Z, Paumier E (1996) Atomic and cluster ion bombardment in the electronic stopping power regime: a thermal spike description. Nucl Instrum Methods Phys Res B 112:26
343. Toulemonde M, Costantini JM, Dufour C (1996) Track creation in SiO_2 and $BaFe_{12}O_{19}$ by swift heavy ions: a thermal spike description. Nucl Instrum Methods Phys Res B 116:37
344. Snoeks E, van Blaaderen A, van Dillen T et al (2000) Colloidal ellipsoids with continuously variable shape. Adv Mater 12:1511
345. Vossen DLJ, de Dood MJA, van Dillen T et al (2000) Novel method for solution growth of thin silica films from tetraethoxysilane. Adv Mater 12:1434
346. Snoeks E, van Blaaderen A, van Dillen T et al (2001) Colloidal assemblies modified by ion irradiation. Nucl Instrum Methods Phys Res B 178:62
347. van Dillen T, Polman A, van Kats CM, van Blaaderen A (2003) Ion beam-induced anisotropic plastic deformation at 300 keV. Appl Phys Lett 83:4315
348. Trinkaus H, Ryazanov AI (1995) Viscoelastic model for the plastic flow of amorphous solids under energetic ion bombardment. Phys Rev Lett 74:5072
349. Klaumünzer S (2004) Ion hammering of silica colloids. Nucl Instrum Methods Phys Res B 215:345
350. van Dillen T, van Blaaderen A, Polman A (2004) Shaping colloidal assemblies. Mater Today 7:40
351. Roorda S, van Dillen T, Polman A et al (2004) Aligned gold nanorods in silica made by ion irradiation of core–shell colloidal particles. Adv Mater 16:235
352. Penninkhof JJ, van Dillen T, Roorda S et al (2006) Anisotropic deformation of metallo-dielectric core–shell colloids under MeV ion irradiation. Nucl Instrum Methods Phys Res B 242:523
353. D'Orleans C, Stoquert JP, Cerruti C et al (2003) Anisotropy of Co nanoparticles induced by swift heavy ions. Phys Rev B 67:220101(R)
354. Giulian R, Kluth P, Araujo LL et al (2008) Shape transformation of Pt nanoparticles induced by swift heavy-ion irradiation. Phys Rev B 78:125413
355. Penninkhof JJ, Polman A, Sweatlock LA et al (2003) Mega-electron-volt ion beam induced anisotropic plasmon resonance of silver nanocrystals in glass. Appl Phys Lett 83:4137
356. Mishra YK, Singh F, Avasthi DK et al (2007) Synthesis of elongated Au nanoparticles in silica matrix by ion irradiation. Appl Phys Lett 91:063103
357. Dawi EA, Rizza G, Mink MP et al (2009) Ion beam shaping of Au nanoparticles in silica: particle size and concentration dependence. J Appl Phys 105:074305
358. Dawi EA, Vredenberg AM, Rizza G, Toulemonde M (2011) Ion-induced elongation of gold nanoparticles in silica by irradiation with Ag and Cu swift heavy ions: track radius and energy loss threshold. Nanotechnology 22:215607
359. Schmidt B, Mücklich A, Röntzsch L, Heinig KH (2007) How do high energy heavy ions shape Ge nanoparticles embedded in SiO_2? Nucl Instrum Methods Phys Res B 257:30
360. Schmidt B, Heinig KH, Mücklich A, Akhmadaliev C (2009) Swift-heavy-ion-induced shaping of spherical Ge nanoparticles into disks and rods. Nucl Instrum Methods Phys Res B 267:1345

361. Dearnaley G (1969) Ion bombardment and implantation. Rep Prog Phys 32:405
362. Ashworth V, Grant WA, Procter RPM (1982) Ion implantation into metals. Franklin Book Co., Elkins Park, PA
363. Conrad JR, Radtke JL, Dodd RA et al (1987) Ion bombardment and implantation. J Appl Phys 62:4591
364. Dearnaley G (1983) Applications of ion implantation in metals. Thin Solid Films 107:315
365. Picraux ST (1984) Ion implantation in metals. Annu Rev Mater Sci 14:335
366. Dimigen H, Kobs K, Leutenecker R et al (1985) Wear resistance of nitrogen-implanted steels. Mater Sci Eng 69:181
367. Dearnaley G (1994) Historical perspective of metal implantation. Surf CoatTechnol 65:1
368. Dearnaley G (1990) Ion beam modification of metals. Nucl Instrum Methods Phys Res B 50:358
369. Hirvonen JK (1989) Ion beam processing for surface modification. Annu Rev Mater Sci 19:401
370. Kliauga AM, Pohl M, Klaffke D (1998) A comparison of the friction and reciprocating wear behaviour between an austenitic (X 2 CrNiMo 17 13 2) and a ferritic (X 1 CrNiMoNb 28 4 2) stainless steel after nitrogen ion implantation. Surf CoatTechnol 102:237
371. Thorwarth G, Mändl S, Rauschenbach B (2000) Plasma immersion ion implantation of cold-work steel. Surf CoatTechnol 125:94
372. Woolley E (1997) Surface hardening by ion implantation. Materials World 5:515
373. Schumacher G, Dettenwanger F, Schütze M et al (1999) Microalloying effects in the oxidation of TiAl materials. Intermetallics 7:1113
374. Donchev A, Gleeson B, Schütze B (2003) Thermodynamic considerations of the beneficial effect of halogens on the oxidation resistance of TiAl-based alloys. Intermetallics 11:387
375. Donchev A, Kolitsch A, Schütze M, Yankov R (2009) Plasma-immersion-ion-implantation of fluorine to protect TiAl-components against high-temperature oxidation. Plasma Process Polym 6:434
376. Neve S, Masset PJ, Yankov RA (2010) High temperature oxidation resistance of fluorine-treated TiAl alloys: chemical vs. ion beam fluorination techniques. Nucl Instrum Methods Phys Res B 268:3381
377. Masset PJ, Yankov R, Kolitsch A, Schütze M (2010) Comparison of fluorination treatments to improve the high temperature oxidation resistance of TiAl alloys in SO_2 containing environments. Mater Sci Forum 638–642:1374
378. Donchev A, Kolitsch A, Schütze M, Yankov R (2011) Combined Al- plus F-treatment of Ti-alloys for improved behaviour at elevated temperatures. Mater Corros 62:695
379. Telbizova T, Parascandola S, Prokert F (2001) Ion nitriding of Al: growth kinetics and characterisation of the nitride layer. Surf CoatTechnol 142–144:1028
380. Telbizova T, Chevolleau T, Möller W et al (2001) Nitrogen incorporation and loss during ion nitriding of Al. Nucl Instrum Methods Phys Res B 184:347
381. Möller W, Parascandola S, Telbizova T et al (2001) Surface processes and diffusion mechanisms of ion nitriding of stainless steel and aluminium. Surf CoatTechnol 136:73
382. Fink D (2004) Fundamentals of ion-irradiated polymers. Springer, Berlin
383. Calcagno L, Foti G (1991) Ion irradiation of polymers. Nucl Instrum Methods B 59–60:1153
384. Marletta G (1990) Chemical reactions and physical property modifications induced by keV ion beams in polymers. Nucl Instrum Methods Phys Res B 46:295
385. Lee EH (1999) Ion-beam modification of polymeric materials – fundamental principles and applications. Nucl Instrum Methods Phys Res B 151:29
386. Stepanov AL (2010) Synthesis of silver nanoparticles in dielectric matrix by ion implantation: a review. Rev Adv Mater Sci 26:1
387. Townsend PD (1987) Optical effects of ion implantation. Rep Prog Phys 50:501
388. Chen F, Wang XL, Wang KM (2007) Development of ion-implanted optical waveguides in optical materials: a review. Opt Mater 29:1523

389. Chen F (2008) Construction of two-dimensional waveguides in insulating optical materials by means of ion beam implantation for photonic applications: fabrication methods and research progress. Crit Rev Solid State Mater Sci 33:165
390. Bayly AR (1973) Optical properties of ion bombarded silica glass. Radiat Eff 18:111
391. Standley RD, Gibson WM, Rodgers JW (1972) Properties of ion-bombarded fused quartz for integrated optics. Appl Optics 11:1313
392. Wie DTY, Lee WW, Blom LR (1975) Large refractive index change induced by ion implantation in lithium niobate. Appl Phys Lett 25:329