Quick SPICE-Based Heat Transfer Estimator for QFN Packages on Multilayer PCB

Giovanni Mezzina(✉), Alberto F. Brunetti, Cataldo L. Saragaglia, Giuseppe Spadavecchia, and Daniela De Venuto

Politecnico di Bari, Dip. di Ingegneria Elettrica e dell'Informazione, Bari, Italy
giovanni.mezzina@uni-hannover.de

Abstract. The thermal design of Printed Circuit Boards (PCBs) is paramount for compact sensing applications featuring power-hungry on-board computing devices and to enhance devices lifespan. Traditionally, PCB thermal analysis use complex software tools with fluid dynamics or finite element (FEM) solvers, however, they are time-consuming. It limits rapid prototyping. This paper addresses this issue by introducing an automated tool for quick simulation of heat transfer in PCBs, focusing on cases involving quad-flat no-lead (QFN) packages. The tool aims to reduce simulation time and facilitate the design process for faster prototyping. The tool proposed in this study translates the thermal behavior of the PCB into an equivalent resistive network, which adjusts to the composition of the metal, dielectric, and solder mask in the analyzed regions. It incorporates image processing algorithms to identify thermal connections and reconstruct multi-layer structures, even with irregularly shaped metal areas. Simulation tests on a PCB sample demonstrated that the proposed tool provides results comparable (<2 °C within an area that can achieve up to 24.6 cm^2 from QFN) with a professional FEM thermal analysis software but 91.16x faster.

Keywords: PCB · Thermal Design · Heat Flow · QFN · Conduction

1 Introduction

The continuous advancements in integrated circuits (ICs) miniaturization have resulted in a significant increase in the density of Printed Circuit Boards (PCBs). These latter, on the other hand, in line with scientific and commercial demands, have progressively reduced in size while requiring the integration of a high number of interfaces and on-board computational capabilities [1–4]. In this context, the utilization of power-hungry electronic components prone to overheating, such as CPUs, GPUs, FPGAs, and voltage regulators, made the proper thermal design of PCBs crucial [1, 2]. This aspect, which was often underestimated, overlooked, or addressed retrospectively, is gaining paramount importance. The reasons behind this trend are manifold: (i) the presence of heat-sensitive devices; (ii) the increased risk of failure and reduced lifespan of components exposed to heat; (iii) the derating of power dissipation as junction temperatures rise; (iv) the decrease in electrical performance associated with die overheating [5, 6]. This aspect is also

© The Author(s), under exclusive license to Springer Nature Switzerland AG 2024
C. Ciofi and E. Limiti (Eds.): SIE 2023, LNEE 1113, pp. 204–213, 2024.
https://doi.org/10.1007/978-3-031-48711-8_24

important, especially in applications that involve the use of heat-sensitive sensors located on the small PCB near to “hot” ICs (e.g., temperature, optical, pressure, and gas sensors) [7, 8]. The study of the thermal influence of power-hungry ICs on the surrounding components depends on the preferred heat transfer process: (i) heat conduction in solids, (ii) heat convection in fluids and gases, and (iii) heat generated by radiation. Specifically, in the context of thermal analysis of PCBs, the heat transfer process depends on the packages used for the ICs. Most of the currently employed packages favor conduction as a fundamental method of heat transfer. Miniaturization has led to the widespread use of packages called Quad-Flat-No-Lead (QFN) and similar [9, 10]. These packages offer the advantage of small footprints, excellent heat conduction properties from the die to the exposed pad (EP) located on the component’s bottom, and good electrical signal integrity as the EP is typically connected to the ground. Nevertheless, since heat is transferred from the die to the PCB through the EP, accurate modeling of the thermal behavior of the board is necessary.

The current state of common practice relies on the utilization of two methods for thermal analysis of Quad Flat No-Lead (QFN) packages: Computational Fluid Dynamics (CFD) with conjugate heat transfer (CHT) analysis and the Finite Element Method (FEM). These methods have demonstrated high accuracies in predicting heat transfer mechanisms and, for this reason, they have been integrated into widely used scientific and commercial simulators (e.g., COMSOL, ANSYS, etc.) [11]. Besides the substantial cost associated with these tools, the simulators employ adaptive and iterative algorithms for the volumetric fragmentation (e.g., meshing) of the domain under analysis. This process proves to be extremely time-consuming even for coarse fragmentations, theoretically designed to be quicker. Consequently, incorporating a feedback step into the workflow concerning multi-layer PCB design or the design of cooling devices like heatsinks becomes challenging. In this context, a few state-of-the-art solutions have been proposed. OnSemi, in [2], has presented a solution for the rapid estimation of heat transfer in PCBs incorporating QFN packages by establishing an electrical equivalent of the thermal behavior of the board. Specifically, they designed a resistive network employing an approach named axisymmetric. This method is constrained to modeling the PCB region beneath the EP and employs a coordinate transformation from Cartesian to radial, assuming the copper planes into inner layers to be rectangular or square. Additionally, this method fails to achieve accurate estimations when the copper polygons, as frequently occurs, exhibit irregular profiles, disregarding the substantial lateral thermal resistance of the dielectric within the inner layers when interspersed with splits in the planes. Authors in [12] devised a solver that analyzes gerber files pixel-by-pixel, associating with each a system of fluid dynamics equations across six principal directions. The system demonstrated good accuracy when juxtaposed with CFD tools; nonetheless, given the substantial number of pixels composing a set of gerber files describing a multi-layer PCB, the computational burden becomes excessively high to implement a quick estimator.

In this context, the present paper introduces an automated tool for heat transfer estimation in a multi-layer PCB embedding QFNs. The primary strength of the design lies in its ability to generate a heatmap of the board within a few seconds (<10 s for up to 32 layers), allowing real-time feedback for appropriate placement of heat-sensitive

components around power-hungry QFN ICs. This is made possible by an automated PCB feature extraction system based on an image processing algorithm applied to gerber files. This algorithm simplifies heat diffusion paths by considering the relative presence of metal and dielectric/solder mask in the analyzed areas, even in presence of irregular metal polygon shapes. Lastly, through analysis of the stack-up's CSV file, the system can derive a resistive network netlist that describes the thermal equivalent in the electrical domain. A SPICE simulation on the extracted resistive network is ultimately conducted, providing a steady-state thermal measurement.

2 The Proposed System

Figure 1 illustrates the detailed workflow of the proposed tool, which consists of four main phases: Initialization, Thermal Path Analysis, Resistive Network Modeling, and SPICE Simulation.

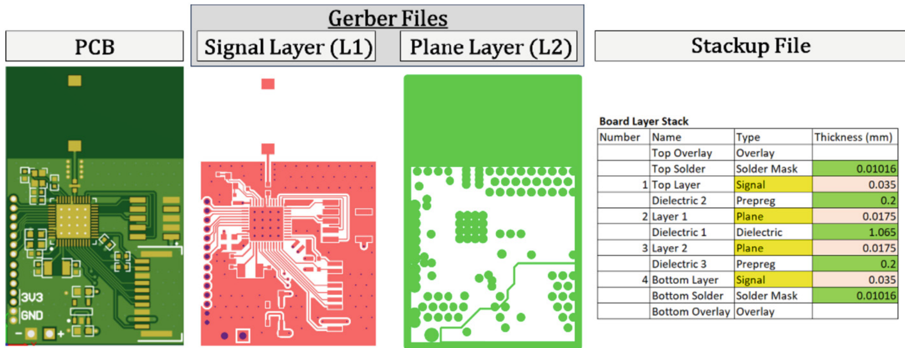
Initialization	Thermal Path Analysis	Resistive Network Modelling	SPICE Simulation
• Gerbers and Stackup Extraction • DUT Definition	• Test Area Fragmentation • Element Composition	• IC Area Resistive Network Model • Radial Resistive Network Model • Equivalent Circuit	• Netlist definition (.cir) • Simulation choice

Fig. 1. Overall workflow of the proposed tool

2.1 Phase 1: Initialization

During the initialization phase, the user must load, via a dedicated Graphical User Interface (GUI), the: (i) gerber files with.JPG extension or Altium standard extensions; and (ii) the stack-up file in.CSV format.

An illustration of gerber files (two out of four layers) and a stack-up table for a sample PCB is shown in Fig. 2. During this phase, the layer and interposed dielectric thicknesses are extracted from the stack-up file. From the individual gerber files, photosensitive masks are determined, indicating the areas where metal will be present. In this context, during initialization, the user is prompted to define the metal (e.g., Copper [Cu]) and the dielectric (e.g., FR4) to be modeled. As can be noticed from Fig. 2, there are two types of layers in the stack-up file: signal and plane layers. A signal layer is realized through a positive mask, where colored areas correspond to metallic zones. Plane layers are negative masks, where white areas correspond to metal regions. Once materials are defined and the plane layers are converted into positive masks, the GUI enables the user, via a point-and-click system, to select the Device Under Test (DUT) through the *assembly* layer. This selection serves the purpose of automatically defining the EP area.



Board Layer Stack

Number	Name	Type	Thickness (mm)
	Top Overlay	Overlay	
	Top Solder	Solder Mask	0.01016
1	Top Layer	Signal	0.035
	Dielectric 2	Prepreg	0.2
2	Layer 1	Plane	0.0175
	Dielectric 1	Dielectric	1.065
3	Layer 2	Plane	0.0175
	Dielectric 3	Prepreg	0.2
4	Bottom Layer	Signal	0.035
	Bottom Solder	Solder Mask	0.01016
	Bottom Overlay	Overlay	

Fig. 2. Overview of gerbers (2 out of 4 layers) and stack-up files to be uploaded in the automatic tool. For the sake of example, the Gerber files section distinguishes between Signal and Plane layers.

Currently, tool permits to select only QFN ICs for the analysis; however, the generality of the here presented method will allow easy integration of various IC package families.

2.2 Phase 2: Thermal Path Analysis

During the Thermal Path Analysis phase, the tool initially partitions the test area (defined by the user through a point-and-click system) into two types of elements, namely IC Elements and Radial Elements. The first element (i.e., IC Element) is derived from the QFN's landing pattern. It encompasses the entire volume beneath an octagonal area inscribing the QFN's EP. Figure 3 depicts an example of an IC Element area (on an outer layer) obtained from the landing pattern. The octagon is further subdivided into eight sub-elements of triangular shape, one for each simplified propagation direction. From each of these eight propagation directions, a cascade of Radial Elements is realized, as schematized in Fig. 3.

Once the elements are defined (Test Area Fragmentation), the process moves on to defining their physical composition. This phase, referred to as Element Composition in Fig. 1, aims to analyze the percentage of metal and dielectric (inner layers) or solder mask (outer layers) along the propagation direction within the analyzed element. For this purpose, the image processing algorithm implemented by the tool extracts all elements as subsets of pixels [13]. Subsequently, within each element, three possible areas are identified along the propagation direction, denoted as $n_{px1..3}$. The interval n_{px1} represents the number of pixels from the origin of the frame, defined by the propagation source (e.g., first column on the left in Fig. 3), to the first pixel belonging to the metal mask. If the frame starts with at least one pixel of the metal mask, $n_{px1} = 0$. The interval n_{px2} corresponds to the number of pixels within the area ranging from the column containing the first pixel of the metal mask to the column containing the last "metallic" pixel. Finally, like n_{px1}, n_{px3} represents the number of pixels within the interval between the column containing the last pixel of the metal mask and the last column of the analyzed frame. $n_{px3} = 0$ if the last column contains pixel from metal mask. The number of pixels belonging to the metal

mask divided by the total number of pixels in the n_{px2} area determines the percentage used to subsequently extract the equivalent resistive model. The complementary value represents the percentage of dielectric or solder mask. Irregular-profile masks are, thus, simplified as shown in Fig. 3 as a combination of rectangles. This simplification offers the advantage of reducing computational complexity by avoiding the analysis of conduction effects on individual pixels while preserving information concerning the thermal path along metallic areas (low thermal resistivity) or regions with high thermal resistivity (e.g., dielectric) that impede heat flow.

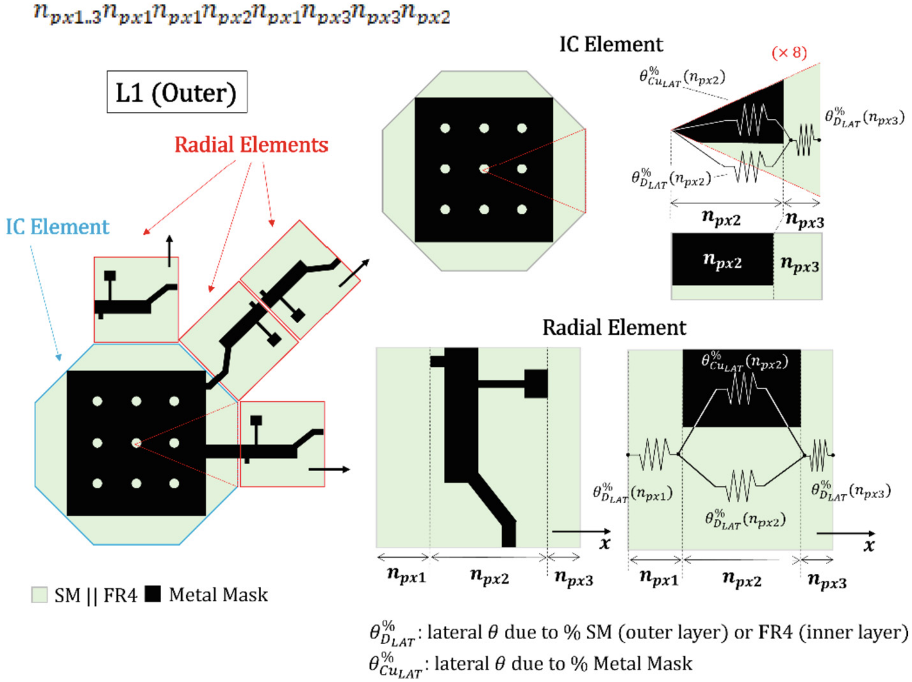


Fig. 3. Demonstrative schematization of Test Area Fragmentation and Element Composition Phases. The figure reports the equivalent resistive network for coplanar heat transfer process.

2.3 Phase 3: Resistive Network Modelling

Once the representation of the PCB layers has been simplified by redefining the elements as depicted in Fig. 3, the tool proceeds to extract the resistive network for the thermal equivalent. Figure 3 illustrates the equivalent coplanar circuit (layer containing metal) for an ith layer belonging to both the IC Elements and Radial Elements stacks. The resistive network is derived using a combination of formulas for extracting the thermal resistance of a parallelepiped:

$$\theta = \left(\frac{1}{\lambda_{mat}} \cdot l\right)/A \tag{1}$$

where λ_{mat} is the thermal conductivity of the analyzed material (e.g., Cu, Soldermask, FR4); l is the length along the x-axis of the metal or dielectric parallelepipeds in coplanar resistances and the thickness of the dielectric in the vertical modeling of the board (Fig. 4); A equals the cross-sectional area of the parallelepiped along the direction of analysis of the resistor, in accordance with Ohm's law.

It is necessary to specify that once the coplanar sections are extracted, the system also generates the model for the equivalent vertical thermal resistance, considering the dielectric interposed between the layers. The model and an example stack are shown in Fig. 4. Particular attention is devoted to the vertical modeling of the IC Elements section. In this case, the presence of a certain number of thermal vias in the EP is accounted for by inserting the thermal resistance related to the N thermal vias in parallel with $\theta_{FR4_h}^{L_{i\to i+1}}$. This thermal resistance will be extremely low, predominating in the parallel configuration. Consistent with existing literature [1–17], this is indeed considered the preferred heat transfer path in QFN packages.

Further details regarding the formulas employed for modeling the resistive network can be found in the previous work [14].

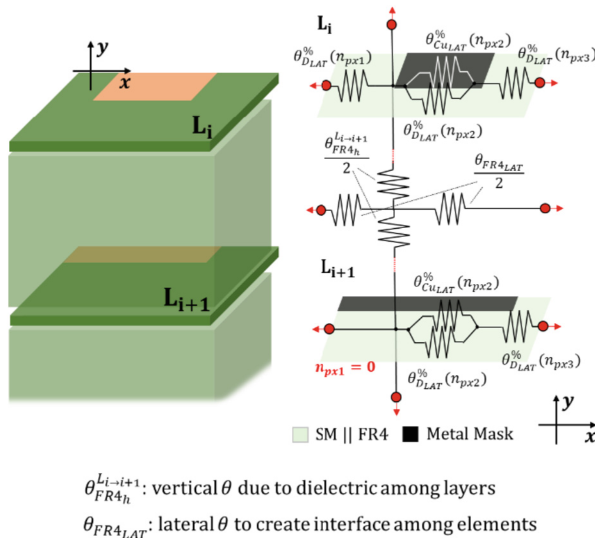


Fig. 4. Vertical Modelling of PCB elements focused on two subsequent layers L_i and L_{i+1}

2.4 Phase 4: SPICE Simulation

Once the resistive model describing the PCB has been finalized, the user is prompted to input three parameters, which are obtainable from the IC's datasheet: (i) the junction-board or die-EP thermal resistance, θ_{J-EP} (the solder paste thermal resistance can be added for more precise estimation); (ii) the thermal resistance between the junction and the top of the case, θ_{J-T} (typically 20–50 °C/W for plastic mold, default 40 °C/W); (iii)

the parameter h or heat transfer coefficient (sometimes film coefficient) for determining the θ_{ex} for heat exchange interface between a body and the surrounding air. Additionally, it is possible to request the insertion of a heatsink thermal resistance, $\theta_{Heatsink}$, if the preliminary study of its effect is desired.

Once all the necessary parameters are provided, the tool will automatically generate a netlist file with a. cir extension. This netlist file will report the equivalent thermal resistance of the PCB as a passive network, $\theta_{tool-PCB}$, , the previously defined ambient thermal resistances as the electric counterpart, the power to be dissipated (P_D) represented as a DC current generator, and the ambient temperature (T_A) through a DC voltage generator. The netlist will include a bias point simulation, corresponding to a steady-state thermal analysis. Currently, the extracted.cir file has been tested with Pspice A/D integrated in OrCAD 17.4. Optionally, the system allows for conducting parametric simulations for the design of cooling devices based on the power to be dissipated, P_D, or to define the range of dissipable power based on commercial heatsink thermal resistances, $\theta_{Heatsink}$.

Figure 5.a presents a simplified version of the implemented equivalent circuit, while Fig. 5.b provides an example of a netlist and the output file of the bias point analysis.

3 Experimental Results

To provide an overview of the accuracy and speed performance of the here-proposed estimator, the system has been validated through comparison with a professional heat transfer analysis tool (i.e., Ansys 2023 r1).

3.1 Sample PCB Characteristics

The sample board used for comparison is the power supply module of a more general PCB used in railway applications [2, 15]. This power supply module integrates a Power Management IC with QFN package capable of providing 4 switching and a linear output channel, overall dissipating 1W in the worst-case. The QFN's EP size is 5.6 mm × 5.6 mm, which determines the extraction pitch of the Radial Elements for modelling. The test board has the following dimensions: 51 mm × 44 mm, thickness 1.43 mm. The PCB has 10 layers of which 2 (connected to ground) are dedicated to dissipation. The thickness of all layers of the board is ½ oz (~18 μm, 35μ m with finishing on outer layer). The IC is placed on the top (L1) of the test board.

3.2 Estimation Tool Performance

The validation of the proposed tool has been carried out by considering six points for the calculation of the radial elements located along each of the four main axes, identified in Fig. 6 as the x-axis, y-axis, diag-1, and diag-2 (red points - Fig. 6). The points have been set equidistantly with a step size of d = 5.6 mm (EP side length). The central point, at a distance of 0 mm from the junction, corresponds to the evaluation coordinates of the IC Element (yellow point - Fig. 6). A total of 25 points per layer have been extracted (250 points for 10 layers).

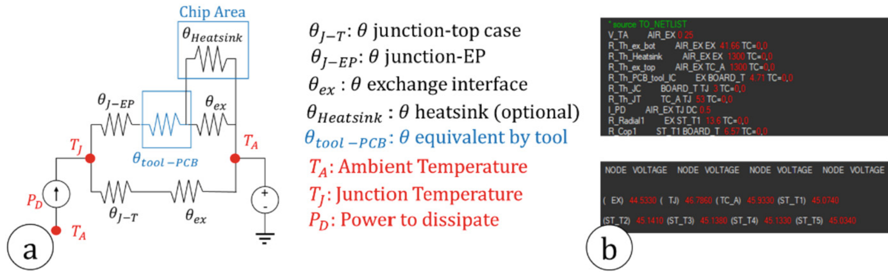


Fig. 5. SPICE Simulation. (a) Simplified equivalent electrical circuit; (b) Netlist and bias point output demonstrative snapshots.

In the Ansys environment, each assessment point has been instrumented with temperature probes, and a Steady-State Thermal analysis has been performed using convection parameters and material selections in line with what was defined for the developed estimator. For the calculation, an adaptive mesh was generated with automatic shaping and manually optimized element sizing to minimize the skewness parameter.

Figure 6 presents on the left a graphical representation of the analyzed points, with an isometric view of the top layer (L1). On the right side of Fig. 6, the upper subplot displays the mean of the absolute value of the difference between the measurements conducted using Ansys (FEM_T) and the estimations generated by the proposed tool ($Model_T$), as a function of the distance from the junction. The graph includes error bars with the upper limit indicating the maximum error incurred and the lower limit representing the minimum mismatch between the measurements.

The four lower subplots are instead dedicated to specific errors along each single direction.

Overall, the simulation results in Fig. 6 showed that the estimator exhibits an average error <1 °C within an area of 7.1 cm^2 and <3 °C within an area of 12.5 cm^2 considering the layer 1 (L1 (top)). The results improve on the widely and uniformly distributed ground layers (L2 and L9), where the estimation error remains below 2 °C for an area of 24.63 cm^2. Presumably, this is due to the greater uniformity of the copper polygon that cover the whole PCB area with a few splits mainly due to vias. It is in contrast to the outer layers that are significantly irregular and heterogeneous due to traces and components.

To assess the computation timing, the thermal analyses with Ansys software and the developed estimator have been conducted on a PC with an Intel Xeon® E-2104G processor - 3.20 GHz, and 32 GB of RAM. The Ansys analysis needed 494.88 ms for the PCB sample meshing and 271.81 s for the temperature analysis, totaling 766.69 s. The analysis using the estimator necessitated 5.25 s for the resistive network modelling and 3.16 s for the bias point calculation with the SPICE simulator, resulting in a total of 8.41 s (91.16 times faster).

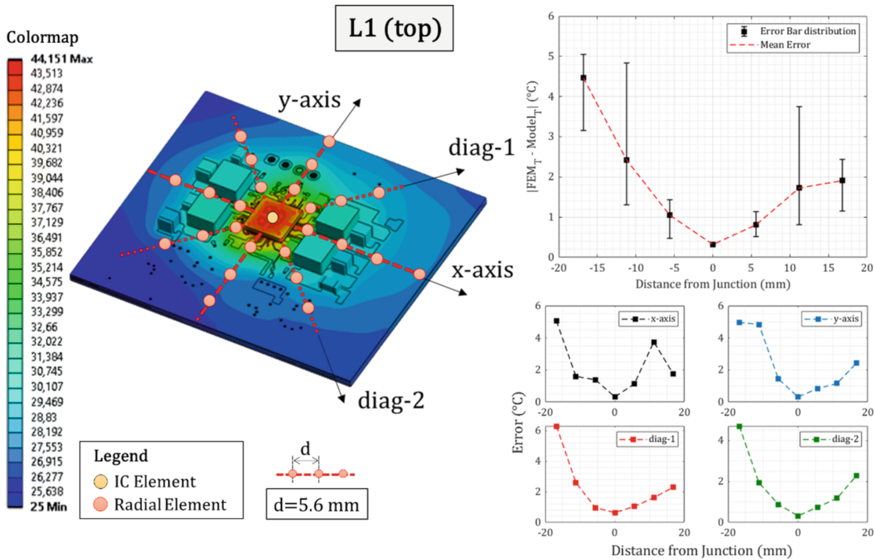


Fig. 6. Sample PCB analysis. Isometric top view of sample board to identify assessment points location. Upper subplot: Comparison between Ansys-based measurements and tool-based ones along x and y axes, diag-1 and diag-2. Bottom subplots: error graphs along main directions.

4 Conclusions

A real-time automated tool for modeling heat transfer in a PCB with QFNs has been presented. This tool employs a novel approach to define and employ resistive networks to depict PCB heat flow. Notably, it adapts to irregular copper layer shapes, critical limitation for most of quick estimators at the state of the art but really common in PCB design. The tool autonomously extracts data from Gerber and stack-up files, including copper-dielectric ratios and thermal connections. It offers crucial support for designers by aiding components placement to enhance sensing accuracy and heat-sensitive components lifespan. Tested on a 10-layer sample PCB, the model yielded precise temperature predictions, with <3 °C deviations compared to Ansys in an area of 12.5 cm^2 around the IC, but drastically reducing simulation time (~90 times). The achieved results are promising from the perspective of developing pseudo real-time analysis tools for the thermal behavior of electronic boards. Prospectively, it can provide feedback during the design phase, thereby preventing errors in heat-sensitive components placements and incorrect design choices (e.g., layer thicknesses, plane splits, etc.), improving electronic devices lifespan.

References

1. Otaki, D., Nonaka, H., Yamada, N.: Thermal design optimization of electronic circuit board layout with transient heating chips by using Bayesian optimization and thermal network model. Int. J. Heat Mass Transf. **184**, 122263 (2022)

2. Shen, Y., et al.: Thermal modeling and design optimization of PCB vias and pads. IEEE Trans. Power Electron. **35**(1), 882–900 (2019)
3. De Venuto, D., Mezzina, G.: Spatio-temporal optimization of perishable goods' shelf life by a pro-active WSN-based architecture. Sensors **18**, 2126 (2018). https://doi.org/10.3390/s18072126
4. De Venuto, D., Annese, V.F., Defazio, G., Gallo, V.L., Mezzina, G.: Gait analysis and quantitative drug effect evaluation in Parkinson disease by jointly EEG-EMG monitoring. In: 2017 12th International Conference on Design & Technology of Integrated Systems In Nanoscale Era (DTIS), pp. 1–6. Palma de Mallorca, Spain (2017). https://doi.org/10.1109/DTIS.2017.7930171
5. Dede, E.M., et al.: Thermal design, optimization, and packaging of planar magnetic components. IEEE Trans. Compon., Packag. Manufact. Technol. **11**(9), 1480–1488 (2021)
6. Xu, S., Xunbo, L.: Analysis on thermal reliability of key electronic components on PCB board. In: 2011 International Conference on Quality, Reliability, Risk, Maintenance, and Safety Engineering. IEEE (2011)
7. Kasemsadeh, B., Heng, A., Ashara, A.: Application Report SNOA967A. Temperature sensors: PCB guidelines for surface mount devices. Texas Instrument (2019)
8. Neiser, A., et al.: Placement of embedded temperature sensors in a printed circuit board for a manufacturing process. In: 2015 38th International Spring Seminar on Electronics Technology (ISSE). IEEE (2015)
9. Chang, C.-L., Hsieh, Y.-Y.: Thermal analysis of QFN packages using finite element method. In: 5th International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, 2004. EuroSimE 2004. Proceedings of the. IEEE (2004)
10. Hollstein, K., et al.: Thermal analysis of the design parameters of a QFN package soldered on a PCB using a simulation approach. Microelectron. Reliab. **120**, 114118 (2021)
11. Sanjitha, K., Panduranga, V., Mallesh, S.: Thermal analysis of different components on the PCB using ANSYS software. In: Gunjan, V.K., Suganthan, P.N., Haase, J., Kumar, A. (eds.) Cybernetics, Cognition and Machine Learning Applications. Algorithms for Intelligent Systems. Springer, Singapore (2023). https://doi.org/10.1007/978-981-19-1484-3_17
12. Zhang, Y., Bagnoli, P.E.: A modeling methodology for thermal analysis of the PCB structure. Microelectron. J. **45**(8), 1033–1052 (2014)
13. Mezzina, G., De Venuto, D.: RGB and 3D-segmentation data combination for the autonomous object manipulation in personal care robotics. In: 2021 16th International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS), pp. 1–6. Montpellier, France (2021). https://doi.org/10.1109/DTIS53253.2021.9505128
14. Mezzina, G., Brunetti, A.F., Saragaglia, C.L., Matarrese, G., De Venuto, D.:Automatic tool for real-time estimation of QFN-related heat transfer in multi-layer PCB by using SPICE simulations. In: 2023 9th International Workshop on Advances in Sensors and Interfaces (IWASI), pp. 177–182. Monopoli (Bari), Italy (2023). https://doi.org/10.1109/IWASI58316.2023.10164511
15. De Venuto, D., Ohletz, M.J., Riccò, B.: Digital window comparator DfT scheme for mixed-signal ICs. J. Electron. Test. **18**, 121–128 (2002). https://doi.org/10.1023/A:1014937424827
16. De Venuto, D., Ohletz, M.J.: On-chip test for mixed-signal ASICs using two-mode comparators with bias-programmable reference voltages. J. Electron. Test. **17**, 243–253 (2001). https://doi.org/10.1023/A:1013377811693
17. Blagojevic, M., Kayal, M., Gervais, M., De Venuto, D.: SOI hall-sensor front end for energy measurement. IEEE Sens. J. **6**(4), 1016–1021 (2006). https://doi.org/10.1109/JSEN.2006.877996