

A K_a-Band Ultra-Low Power GaAs MMIC LNA

Shikha Sharma[®], Sergio Colangeli^(⊠)[®], Patrick Longhi[®], Walter Ciccognani[®], Antonio Serino[®], and Ernesto Limiti[®]

University of Roma Tor Vergata, via del Politecnico 1, 00133 Roma, Italy colangeli@ing.uniroma2.it

Abstract. In this paper, a low-noise amplifier (LNA) having ultra-low voltage is presented, intended for active antenna SATCOM applications. The amplifier is composed of three common-source stages with inductive source degeneration and is realized in a 0.1 μ m GaAs process provided by United Monolithic Semiconductors (UMS). The proposed LNA can operate at a sub-Volt supply voltage (nominally 0.7 V, but even lower if some performance degradation is accepted). The LNA provides a gain of 26 dB and a noise figure below 1.6 dB across an operative band from 27 to 31 GHz, while consuming only 18.9 mW. The output third-order intercept point is 13.8 dBm at 29 GHz and the saturated output power is 3.8 dBm. The LNA survived repeated input power sweeps up to 5 dBm and a 24 h stress test at -7 dBm without degradation. Chip size is 2.3×1.4 mm².

Keywords: GaAs \cdot K_a band \cdot Low Noise Amplifier \cdot MMIC \cdot Ultra-low power

1 Introduction

 K_a -band active antennas play a crucial role in satellite communication systems, providing both high-capacity data links and the possibility of multiple-beam cover-age. Due to the use of hundreds of modules, low-noise amplifiers with very low power consumption are critical for increasing energy efficiency. However, it is highly challenging to achieve satisfactory performance from K_a -band LNAs (basically, low noise figure, high gain, high linearity) at operating points featured by very low drain voltage. Many studies on GaAs LNAs with noise figures (NF) ranging from 1.5 to 2 dB in K/K_u and near-by bands have been published in the literature [1,7,8,11,14]. In this paper, an ultra-low power LNA is presented, designed, and fabricated in United Monolithic Semiconductor's 0.1 μ m GaAs pHEMT process (commercial name: PH10-10). Although optimized for gain and noise figure, the LNA also exhibits interesting performance as to linearity and survivability. See Table 1 for a framing of this work in the state of the art.

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Ref.	f	L_g	G	ΔG	NF	Size	P_{DC}
	[GHz]	[nm]	[dB]	[dB]	[dB]	$[\mathrm{mm}^2]$	[mW]
[14]	20-24	70	18	± 0.6	1.2	2×1.5	115
[14]	26.5 - 31.5	70	18	± 0.6	1.5	3×1.2	115
[7]	23-43	100	21	± 2	2-2.4	31×31	118.4
[8]	22-34	150	14.3	± 1.5	1.75	1×0.54	24
[11]	18-40	150	11	± 0.5	3.6	2.4×2.1	220
[1]	21.5 - 50	100	22.5	± 2.5	3-4.5	2.5×1	36
This work	27-31	100	26	± 0.1	1.5	2.3×1.4	18.9

 Table 1. State of art overview for GaAs LNAs in comparable bands.

2 Design

The adopted 0.1 μ m GaAs pHEMT process is featured by a typical cutoff frequency (f_T) of 130 GHz and has an optimal transistor drain-source voltage (V_{DS}) of 2.5 V. Thus, the Foundry's PDK model is not guaranteed at sub-Volt VDS. As a consequence, a multi-bias small-signal and noise transistor model was extracted in house for V_{DS} in the neighborhood of 0.7 V. The model is comprised of a smallsignal equivalent circuit [3,5] equipped with equivalent noise temperatures [12].

The designed LNA consists of three $4 \times 30 \ \mu\text{m}$ active stages. The gate bias is almost zero ($V_{GS} = -0.02 \text{ V}$), corresponding to a drain current density of 75 mA/mm (9 mA per stage) at the nominal supply of $V_{DS} = 0.7 \text{ V}$. All stages are in common-source configuration, with appropriately selected, stagedependent inductive degenerations, as explained next.



Fig. 1. Micro-photograph of the realized MMIC LNA. The overall chip size is of $2.3 \times 1.4 \text{ mm}^2$, but the actual length is 0.2 mm shorter.

In particular, the first two stages are conceived as a simultaneously conjugatematched pair which minimizes the noise measure [6] and therefore, virtually, also the noise figure. This is achieved in practice by following the procedure outlined in [2] and reprised in [9,14]. The third stage is basically a simultaneously conjugate-matched one, so that he overall chain is also simultaneously conjugatematched and low-noise [4]. Of course, the baseline design with ideal elements underwent appropriate tuning and optimization through the subsequent design steps, i.e., when introducing real elements and EM simulations.

For reasons of compatibility with other cells in the reticule, the fabricated LNA occupies an area of $2.3 \times 1.4 \text{ mm}^2$, but the actual length is 0.2 mm shorter. The fabricated LNA is shown in Fig. 1.



Fig. 2. Input (left) and output (right) matching matching of three samples (continuous curves) versus updated model (dashed curve).



Fig. 3. Left: Gain and noise figure of three samples (continuous curves) versus updated model (dashed curve). Right: Noise figure of two samples (markers) versus model, with actual and perfectly matched source termination.

3 Characterization

After fabrication, the MMIC LNA has been extensively characterized on wafer with respect to small-signal, noise figure, power curves, intermodulation, and survivability.

Figure 2 presents the simulated and measured matching under nominal operating conditions, whereas the gain and noise figure are shown in Fig. 3. The LNA achieves a 26-dB small-signal flat gain across the whole band-width (27–31 GHz). The measured noise figure, is 1.5 dB in average across the operating bandwidth, with a lowest value of 1.4 dB at 30 GHz and a maximum of 1.6 dB at 27 GHz.

Notice that the small-signal campaign both on the LNA and on a large set of test structures has been vital in order to carry out a thorough reverse engineering of the design. In particular, two main conclusions were drawn from this activity:

- The EM-simulated S-parameters of the passive structures were found to suffer from nonnegligible phase discrepancies from measurements when applying transmission line offsets, even if these were duly removed through calibrated ports with shifted reference planes. This issue, however, basically disappears when using calibrated ports with zero-length shifts.
- The S-parameters of the degenerated active devices resulted much more sensitive than expected on the parameters of the degenerations themselves. Also, some differences were observed between the devices from the samples used for modeling and those in the LNA's foundry run, especially in terms of gain. In this case, comparisons were made both on non-degenerated and degenerated transistors.

By updating the EM simulations and device models accordingly, the agreement between simulations and measurements is very satisfactory, as can be seen from Fig. 2 and Fig. 3-left.



Fig. 4. Left: Intermodulation test. Right: Measured third-order intercept points versus frequency.

Third-order measurements were also taken, with a tone spacing of 100 MHz. The measured frequency components versus input power are shown in Fig. 4-left for both lower and upper sides and at three nominal frequencies (lower, center and upper frequency). For better clarity, the intercept points versus nominal frequency are then shown in Fig. 4-right for the lower and upper sides separately. The measured output intercept points are quite flat versus frequency and average at OTOI = 13.8 dBm at center frequency.



Fig. 5. Left: Gain compression test. Right: Measured output power at 1-dB gain compression versus frequency.

Finally, gain compression and stress tests were carried out with a similar test bench, namely, after removing one of the two tones and amplifying the remaining one up to a maximum nominal level, due to hardware limitations, of -5 dBm. The measured output power at 1-dB gain compression point is approximately -2 ± 0.5 dBm over frequency, associated with a flat gain: see Fig. 5.

Another important aspect of LNA's for SATCOM applications is their survivability to possible nearby interferers. When this aspect is specifically addressed, the go-to solution is the use of off-chip or (if available) on-chip limiters [15], which, however, entail a significant increase in noise figure; alternatively, GaN technology can be adopted in place of GaAs since it is inherently more robust and allows specific protection techniques [13,16], although at the cost of higher noise figure and/or power consumption [10,16]. Notice that the proposed design is GaAs-based and devoid of any protection mechanism in addition to the LNA.

To assess survivability, two different test conditions were devised, namely a short-term stress and a long-term stress. The former consisted in applying an input power sweep from -35 dBm to -5 dBm with 1 dB step, each level being maintained for 5 s. Notice that the final level corresponds to 16 dB gain compression for this MMIC. Also, the sweep was applied three times, obtaining a good retracing of the same curve.

The long-term stress consisted in applying an input power fixed at -7 dBm for 24 h, while monitoring the output power and the total gate and drain currents. Figure 6-left reports the sequence of a short-term stress test, the long-term stress test and an additional short-term stress test performed to double check that the LNA's behavior did not show degradations. In addition, Fig. 6-right shows the

monitored values of I_G and I_D during the long-term stress. The former falls below the quantization error of the ammeter while the latter remains constant throughout the whole test.



Fig. 6. Left: Power measurements before, during and after stress. Right: Measured gate and drain currents during the stress.

4 Conclusion

An ultra-low voltage (0.7 V) MMIC LNA targeting active antenna SATCOM applications was presented in this contribution, designed and realized in a European, commercial 0.1 µm GaAs process provided by UMS. Although the amplifier is composed of three active stages, it occupies less than $2.3 \times 1.4 \text{ mm}^2$ and achieves remarkable performance in an operative band from 27 to 31 GHz while consuming as low as 18.9 mW.

Measured gain is 26 dB and a noise figure below 1.6 dB. The output thirdorder intercept point is around 14 dBm and the saturated output power is about 4 dBm. The LNA survived repeated input power sweeps up to 5 dBm and a 24 h stress test at -7 dBm without degradation.

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