Characterization of PIN Diode for T-R Radar Limiter Design at X-Band

Giovanni Collodi[1(✉)], Maria Fancelli[1], Monica Righini[1], Roberto Galassi[2], Luigi Volpi[3], Enrico Vetrano[2], and Alessandro Cidronali[1]

[1] Dipartimento Ingegneria dell Informazione - DINFO, Università degli Studi di Firenze, Via S. Marta N. 3, 50139 Firenze, Italy
{giovanni.collodi,maria.fancelli,monica.righini, alessandro.cidronali}@unifi.it
[2] Pasquali Microwave System srl, Via Del Palazzo Dei Diavoli, 124/B, 50142 Firenze, Italy
info@pasquali-ms.it
[3] RTW srl, Via Agostino Bassi, 5, Pisa, Italy
https://www.pasquali-microwavesystems.com, https://www.rtw.it/

Abstract. This paper introduces a new characterizing method for packaged PIN diodes. The method is specifically oriented to the design of microwave transmitting-receiving (TR) radar limiters in steady-state operating conditions. Characterization were carried out at X-band in both ON ($V_{bias} = 10\,\mathrm{V}$) and OFF ($V_{bias} = 0\,\mathrm{V}$) PIN diode bias states, and varying its position inside a WR90 waveguide based test JIG. The effects of the JIG as well as the diode package parasitics have been de-embedded from the experimental data by means of a accurate EM simulations. The resulting extracted PIN diode Y parameters represent the basis to develop of a PIN diode lumped element model. The model has been adopted to predict the steady state TR limiter performances across X-band.

Keywords: Device modeling · TR limiter · Microwave electronics

1 Introduction

TR Limiters are usually employed in radar systems to protect the high sensitive receiver from undesired large input signal, thus relaxing the linearity specifications of radar receivers, [1,2]. Typical Transmitter-Receiver (TR) limiters make use of PIN diodes in order to implement a voltage-controlled resistors. The ability showed by such devices to manipulates large amounts of RF power, making use of low DC excitation is fundamental in TR limiters [3]. PIN diodes based TR limiter configurations are well known and the principle of operation is largely discussed in literature [4,5]. The accurate characterization of PIN across the operative bandwidth is crucial for accurate TR limiter design.

Basically a TR limiter consists in a waveguide with one or more resonant cavities. Each of them incorporate a PIN diode mounted on a structure, the

C. Ciofi and E. Limiti (Eds.): SIE 2023, LNEE 1113, pp. 93–101, 2024.
https://doi.org/10.1007/978-3-031-48711-8_11

post, that allows to change the position of the diode inside the corresponding cavity [6]. Each of the series of posts and diodes became a RF short circuit when the diode enter in ON state, at a frequency which depends upon the post length, thus the diode position within the cavities; conversely, in the OFF state the diodes shouldn't affect the signal propagation across the waveguide. In this paper we present a method to characterize the intrinsic portion of a PIN diode, for its use in predicting the operative frequency of the limiter on the basis of the post length. The PIN diode is considered embedded in a WR90 waveguide, with the contribution of the waveguide de-embedded by means of electromagnetic simulations. The method is suitable for estimation of the TR limiter operation across the X-band in both the OFF and ON steady states.

The anlystical treatment for the diode extraction, the electromagnetic simulations and the experimental results are presented in the paper.

2 Intrinsic PIN Diode Characterization

One of the main issue in limiter design consist in the availability of an accurate model of the PIN diode. In the past year many linear and non linear model were proposed. Some of them were physically based, while other were fully behavioral. Among the others, some interesting approaches were illustrated in [7–9]. All these methods are aimed to describe the whole discrete PIN diode, included in its package. On the contrary the method proposed in the present paper is oriented to the identification of the intrinsic portion of a discrete PIN diode, for a better prediction of the limiter operating frequency as function of the diode in the waveguide cavity. The accurate geometrical description of the diode is obtained by means of a series of microscopic measurements. The mechanical characterization of the intrinsic part of the diode is necessary for the correct identification of the intrinsic diode model. The intrinsic part of the PIN diode corresponds to the Silicon die as illustrated in Fig. 1, which describes the internal structure of the diode adopted in this work. The Silicon die is bonded to the cathode through a couple wire. This approach enables to include all package parasites within the EM simulation as well as the effect of the interaction of the package with the JIG structure.

The intrinsic portion of the diode is described by means its S- Parameter Matrix $S_{diode}\,(V_{bias}, \omega)$ where ω and V_{bias} correspond, respectively, to the whole X-band radial frequency and to the ON and OFF state bias. For the S_{diode} identification we follows the de-embedding approach introduced in [10]. The procedure is schematically described in Fig. 2. The latter enables the identification of the $S\,(1 \times 1)$ matrix describing the intrinsic portion of the diode. The procedure make use of the $S\,(2 \times 2)$ matrix obtained by VNA measurements while the effect of both the JIG and the diode package are described by an $S\,(3 \times 3)$ matrix obtained by a accurate EM simulations as described in Fig. 3.

The de-embedding method implemented in the present work is described by the (1) and the (2).

$$S_{(1\times1)} = M^{-1}, \tag{1}$$

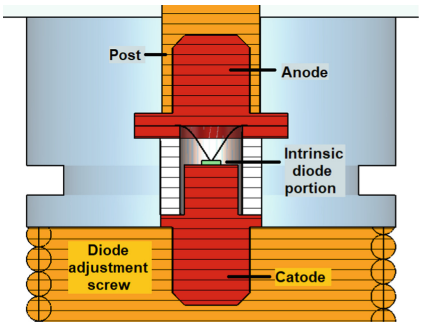

Fig. 1. Accurate interior mechanical description of the discrete PIN diode under test (from CST EM simulator)

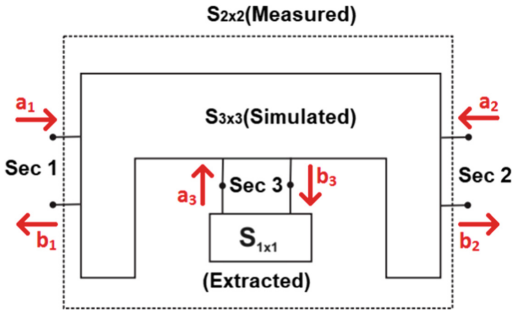

Fig. 2. Schematic description of the de-embedding method implemented for the extraction of $Y_{diode}\,(V_{bias}, \omega)$.

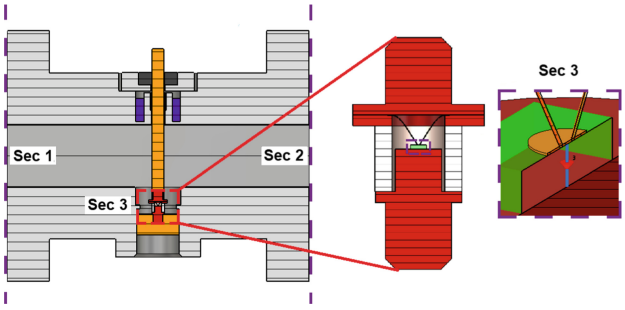

Fig. 3. Schematic of the EM simulated Test JIG used to extract the intrinsic PIN diode S parameter description.

where M is a (1×1) matrix obtained starting from the (2×2) measured S matrix and the and the (3×3) simulated S matrix.

$$\mathbf{M} = [S_{31}\ S_{32}\ S_{33}] \cdot \begin{bmatrix} [\mathbf{A} - \mathbf{G}]^{-1} \cdot \mathbf{D} \\ 1 \end{bmatrix}, \tag{2}$$

where:
$\mathbf{A}$ = Measured S-paramenter matrix
$\mathbf{G}$ = (2×2) minor of the simulated (3×3) S matrix.
$\mathbf{D}$ = (2×1) column vector of the 3rd column of the (3×3) S matrix.
$[S_{31}\ S_{32}\ S_{33}]$= 3rd row of the simulated (3×3) S matrix.

3 Test JIG and Measurements

A test JIG was designed to both enable the measurements for the de-embedding procedure and to verify the predictive performance of the model, it is based on a WR90 waveguide and emulates the limiter operation across the X-band. The JIG was developed using the full-3D EM simulator CST as illustrated in Fig. 3. The prototype of the designed JIG is illustrated in Fig. 4.

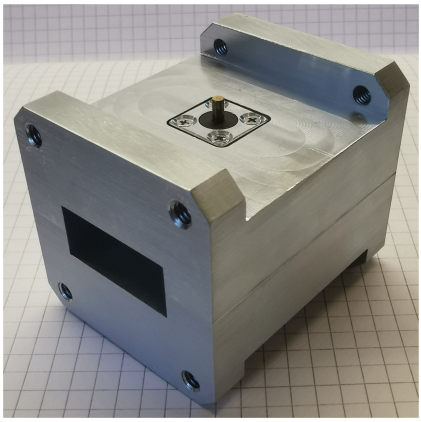

Fig. 4. Experimental test JIG for the PIN diode extraction and model validation; this part emulates the limiter operation across X-band.

A measurement set-was implemented as illustrate in Fig. 5, by means of a VNA calibrated on WR90 waveguide standards. By the test JIG, the PIN diode was polarized in both ON and OFF condition (Vd = 10 V and Vd = 0 V) using an external power supply. A set of S-parameter broadband measurements were carried out, considering 9 different diode positions within the JIG, for both the ON and OFF diode state.

Six out of the nine double set of measured data were used in the de-embedding procedure to extract the corresponding $S\,(1 \times 1)$ matrix, describing the intrinsic

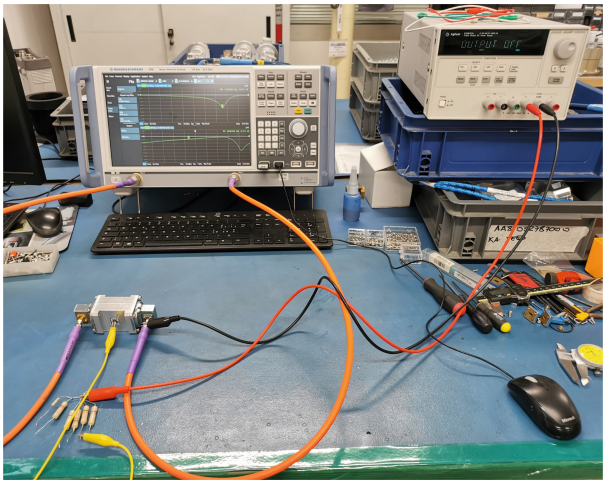

Fig. 5. Experimental measurement set-up for PIN diode extraction and model validation across X-band.

portion of the diode while the remaining three sets of measures were used to validate the model.

4 Intrinsic PIN Diode Modeling

The procedure to extract the intrinsic PIN diode circuital model in the ON and OFF condition makes use of the corresponding six $S\,(1 \times 1)$ matrix, extracted from the measures obtained varying the position of the diode inside the JIG. As the diode is polarized in the same state (same Vd) in the all the six ON and six OFF position, it seems reasonable to expect the extracted matrices to be equal. On the contrary these S matrix slightly differ one each other due to numerical noise and higher order effect not taken into account by the model description of Sect. 2. As a consequence the $S\,(1 \times 1)$ representative of the ON and OFF states were calculated as average value of the six extracted one.

The extraction of the components included in the circuital model was based on the averaged intrinsic matrix, extracted for the six screw positions, which are depicted in Fig. 7 for both the ON and OFF state. The implemented circuital model was based on a very simple topology, which is the same for both the two states. The latter is based on a series inductance, L, followed by a parallel R, C circuit. The proposed topology is illustrated in Fig. 6. The components value were calculated by means of a best fitting procedure and lead to the values illustrated in Table 1. Comparison between the ON and OFF model and the averaged ON and OFF $S\,(1 \times 1)$ matrices are shown in Fig. 7. The latter highlight a good agreement between the extracted intrinsic average S parameter and the one obtained with the intrinsic model.

Results illustrated in Table 1, show that the inductance is almost constant in both the states, while the capacitance and resistance undergo a significant change from ON to OFF (from 3.8 to 0.17 pF and from 8 to 1100 Ω respectively).

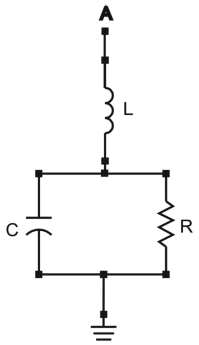

Fig. 6. Circuit model topology of the intrinsic PIN diode, the catode is considered connected to ground.

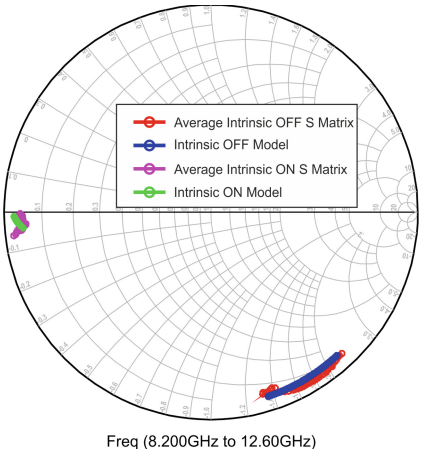

Fig. 7. Comparison between averaged extracted intrinsic diode data and simulated one by circuit of Fig. 6.

5 Experimental Results

The three sets of measures, which correspond to different diode depths into the waveguide, in both the ON and OFF condition, not included in the diode

Table 1. ON and OFF model value.

Component	ON State	OFF State
R	8 Ω	1100 Ω
L	0.08 nH	0.09 nH
C	3.8 pF	0.17 pF

characterization phase, were used to validate the model. To this aim three corresponding EM simulations of the JIG considering the different position of the screw in the post within the WR90 guide were carried out and used in conjunction with the extracted circuital model for the ON and OFF described in the previous section. The aims were to predict the behavior of the limiter in these specific screw positions. Results of this simulations are illustrated in Fig. 8 in comparison with measured data at the corresponding screw position within the limiter. Figure shows on the left the OFF state while on the right the ON state.

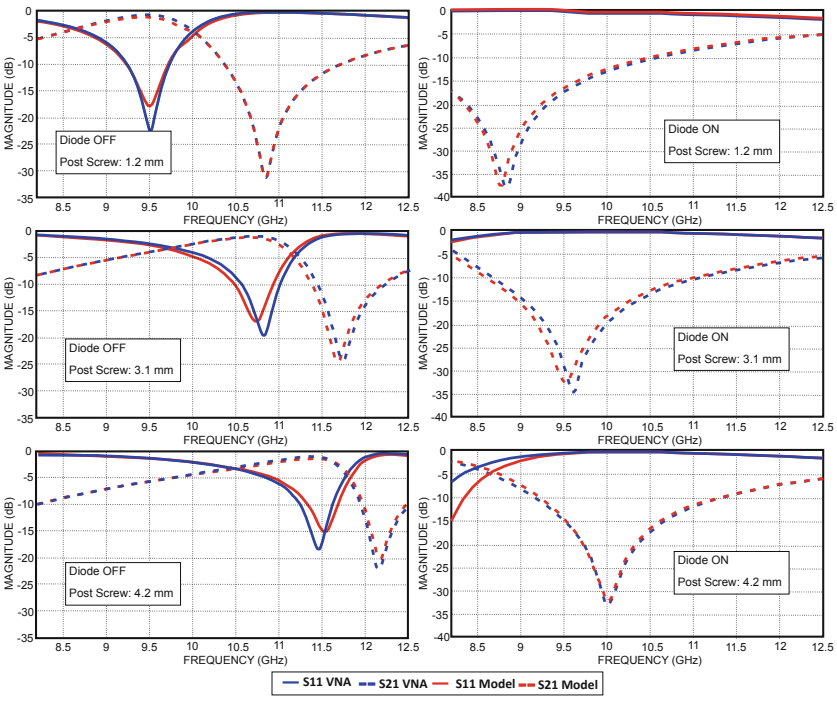

Fig. 8. Comparison between measurement and simulated data, in terms of S11 (continuos) and S21 (dashed) for different diode positions and for both OFF state: left column, ON state: right column.

6 Conclusion

In the present paper a procedure to extract the intrinsic PIN diode lumped element model was presented. The method is based on the optimization of a mathematical technique aimed at the identification of the intrinsic portion packaged diode. The approach enable a simple and fast modeling of the PIN Diode die as shown by the corresponding model which uses only three lumped elements for both ON and OFF state. The effects of parasites due to the package are absorbed by the EM simulation of the JIG which includes an accurate description of the diode mechanics. This approach shows advantage both in the intrinsic extrapolation procedure as well as in the prediction of the structure behavior across the whole X-band. The illustrated results highlight an optimum matching between measurements and simulation.

References

1. Cidronali, A., et al.: System level analysis of millimetre-wave GaN-based MIMO radar for detection of micro unmanned aerial vehicles. In: Photonics and Electromagnetics Research Symposium - Spring (PIERS-Spring), Rome, vol. 2019, pp. 438–450 (2019)
2. Cidronali, A., Pagnini, L., Collodi, G., Passafiume, M.: A highly linear Ka-Band GaN-on-Si active balanced mixer for radar applications. IEEE Trans. Circuits Syst. I Regul. Pap. **69**(11), 4453–4464 (2022)
3. Wang, Z., Cao, H., Zhang, C.: Research on the influence of PIN diode on limiter performance in power limiter. In: 7th IEEE International Symposium on Microwave, Antenna, Propagation, and EMC Technologies (MAPE). Xi'an, vol. 2017, pp. 220–223 (2017)
4. Madany, Y.M., Miligy, A.F.: Investigation and design of microwave waveguide power limiter (MWPL) for communication and radar applications. In: 2015 International Conference on Electromagnetics in Advanced Applications (ICEAA), Turin, pp. 1621–1624 (2015)
5. Drozdovskaia, L., Drozdovski, N.: Simple microwave waveguide passive power limiter. In: 1998 IEEE Asia-Pacific Conference on Circuits and Systems. Microelectronics and Integrating Systems. Proceedings, Chiang Mai, pp. 683–686 (1998)
6. Wang, D., Gao, L., Zheng, S., Deng, F., Hou, D.: Investigation on the pulse characteristics of RF/microwave limiter based on multistage PIN diodes and Schottky diodes. In: Proceedings of 2014 3rd Asia-Pacific Conference on Antennas and Propagation, Harbin, pp. 1366–1369 (2014)
7. Strollo, A.G.M.: A new SPICE model of power P-I-N diode based on asymptotic waveform evaluation. IEEE Trans. Power Electron. **12**(1), 12–20 (1997)
8. Nazir, M.U., Kashif, M., Ahsan, N., Malik, Z.Y.: PIN diode modelling for simulation and development of high power limiter, digitally controlled phase shifter and high isolation SPDT switch. In: Proceedings of 2013 10th International Bhurban Conference on Applied Sciences and Technology (IBCAST), Islamabad, pp. 439–445 (2013)

9. Caverly, R.H., Quinn, M.J.: Time domain modeling of PIN control and limiter diodes. In: 1999 IEEE MTT-S International Microwave Symposium Digest, Anaheim, vol. 2, pp. 719–722 (1999)
10. Cidronali, A., Collodi, G., Vannini, G., Santarelli, A.: A new approach to FET model scaling and MMIC design based on electromagnetic analysis. IEEE Trans. Microw. Theory Tech. **47**, 900–907 (1999)