A 0.94 V Dynamic Bias Double Tail Comparator for High-Speed Applications in 5 nm Technology

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Abstract. The necessity of efficient comparators in modern ADCs calls for new two-stages topologies that overcome the Strongarm limitations in terms of common-mode offset and gain dependency. The latest fashion is represented by dynamic bias integrators coupled with low power and low noise latches. The dynamic bias significantly reduces the overall power consumption, a feature which the second stage has to maintain; also, a CMOS implementation is usually adopted to gain more robustness. Starting from the comparator with dynamic floating inverter amplifier [1], a new structure has been derived and explained. The architecture has been simulated in 5 nm FinFET technology and compared to the state-of-the-art for very stringent power, noise and speed targets. Nonetheless, the proposed topology matches various applications thanks to its multiple degrees of freedom which allow the designer plenty of room for further improvements. The continuously scaling technology will favour this CMOS dynamic bias implementation even more.

Keywords: StrongARM · Dynamic Bias · Comparator

1 Introduction

1.1 Analog-to-Digital Converters (ADCs) for Serial Links

In modern communications, speed and efficiency are the key features and the motivations behind the present work. Nowadays, serial data are transferred at 56 Gb/s [2] or even higher rates. This requires extensive equalization that can only be achieved in the digital domain. As a result, high-speed ADCs are key components of serial data receivers. Such great speed may be obtained only through at least 64 time-interleaved Successive Approximation Register (SAR) converters. The single SAR should be carefully designed as its power, speed and resolution greatly affects the overall performance. In a typical SAR the most energy-hungry block is the comparator [3]. The aim of this article is to present a power optimized comparator for high-speed applications.

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Table 1. Comparator targets.

Targets		
Decision Time	t_{DEC}	$\approx$ 10ps
Charge in a period	Q	<2fC
Noise	N_i	<2 mV
Integrator Gain	A_V	$\in$ [6, 9]

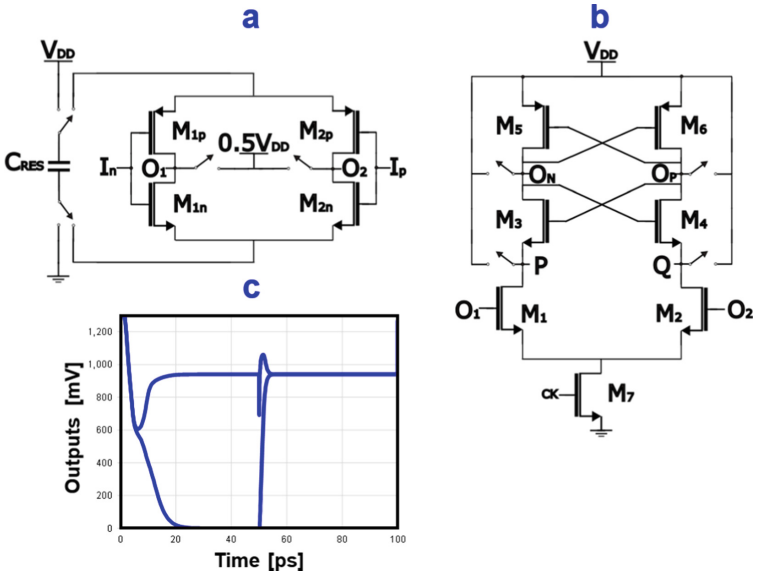

Fig. 1. **a** Dynamic Floating Inverter Amplifier, **b** Strongarm, **c** Tang Comparator Outputs

1.2 Comparator Targets

As explained in Sect. 1.1, analog-digital converters represent a bottleneck regarding the overall performance of the entire receivers. This scenario imposes stringent targets in terms of speed [4], noise and energy consumption. For this work, the target specifications of Table 1 have been adopted. Combining these three metrics a Figure of Merit (1) can be defined, i.e. a single number which allows to rank different topologies based on their efficiency at first glance. This FoM [5] fairly evaluates the time needed to perform a comparison, the charge consumed in a clock period (T) and the noise produced in the process [1]. The smaller FoM will guarantee the higher efficiency.

$$\mathrm{FoM} = t_{DEC} * Q * N_i^2 \tag{1}$$

$$t_{DEC} = t\,(\mathit{differential\ output} = 0.5 * V_{DD}) \tag{2}$$

$$Q = I_{SUPPLY}\,dt \tag{3}$$

$$Nt = \sqrt{N_{o,integrator} + \frac{No,\ latch}{A^2_{V,integrator}}} \tag{4}$$

Technology. It is important to remark that 5 nm technology has been used for this work. Such scaled technology node is necessary due to successive digital processing required for signal equalization. Topology considerations are linked to the adopted technology. Complementary (CMOS) structures are more suited for Finfet [6] with respect to much older technology nodes, e.g. 90nm or similar, where it would be preferable to adopt nmos implementations, such as the dynamic bias integrator of [7].

2 Comparator Topologies Overview

2.1 Strongarm (SA)

Strongarm [8] is one of the most popular comparator implementations thanks to its extreme simplicity and efficiency. As shown in Fig. 1b, the integrator ($M_{1,2}$) and the latch ($M_{3–6}$) are implemented with the minimum number of transistors and the whole architecture has only one stage. This compactness guarantees both velocity and reduced energy consumption, while the noise is further reduced by the cascode enhanced gain. Unfortunately, the one-stage approach presents major drawbacks as both the offset and the gain heavily depend on the input common mode. These flaws may be overcome by construction with a two-stage comparator [1].

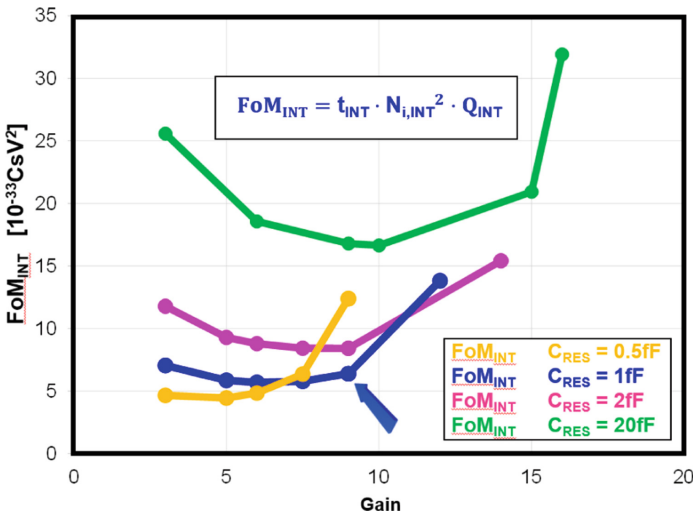

Fig. 2. Integrator FoM for different sizing of C_{RES}.

2.2 Dynamic Floating Inverter Amplifier Comparator (Tang)

A two-stage approach allows to overcome the common mode dependency, whereas a CMOS implementation is preferrable in the adopted technology.

The need for low power comparators requires dynamic biasing, a technique for reducing the energy consumption by improving the transistors transconductance over current ratio [7]. These three features point to the Tang comparator, shown in Fig. 1.

Dynamic Floating Inverter Amplifier. This first stage—Fig. 1a—is a dynamic bias CMOS integrator providing all the advantages of an independent power domain [1] thanks to the capacitive supply offered by the reservoir capacitor (C_{RES}). This capacitance is charged between ground and V_{DD} during a reset phase, then it supplies the inverters ($M_{1p,1n}$ and $M_{2p,2n}$) through a charge sharing mechanism. Once the transistors size has been chosen, the sizing of the reservoir allows to control speed, power and gain [1]. The bigger the reservoir, the greater the gain and the charge consumption, whereas the time will be shortened. A simple way out of these trade-offs is to select a certain gain range and then to look for the minimum integrator figure of merit—Fig. 2, which accounts for the integration time, the charge and the noise of the first stage.

Strongarm as Second Stage. The Strongarm presents not only a latch, but also an additional amplifier ($M_{1,2}$), therefore Tang comparator relies on two integrators and a latch in only two stages. As stated in 2.1, this topology has excellent characteristics in terms of noise and power thanks to the gradual turning on of its transistors. SA performance as second stage may be further optimized by adding a small delay at the tail (M_7) so to allow the first integrator to produce a bigger gain. An effective delay should increase the integrator gain without an excessive degradation of the decision time, so as to improve the FoM. Hence, the required delay should be extremely low, in the order of fraction of ps. In this work such delay has been implemented by changing the threshold of the tail transistors. If an older technology is employed, the same delay can be realized through some logic ports on the clock path or resetting the drain of M_7 at V_{DD}.

3 Proposed Comparator

3.1 Double Tail Comparator

In this work a further optimization of Tang comparator is proposed, the Double Tail, Fig. 3. Once understood that delaying the Strongarm turning on brings significant advantages in terms of power, gain and noise, a delayed Tang comparator may seem the most straightforward approach. Nonetheless, the SA presents a major flaw when used as second stage: this circuit is reset at V_{DD}, but its input voltages (O_1, O_2) are expected to be around $0.5*V_{DD}$. Consequently, designing a reset network at half the supply seems more convenient in terms of noise and power.

A second improvement is the additional tail (M_8) which cuts the power consumption of $M_{5,6}$. Also this additional tail is delayed through the threshold voltage. Such delay should match the delay of the lower tail (M_{TAIL}) to maximize the power efficiency of this circuit, which is named “double tail” after these two fets turning on the structure.

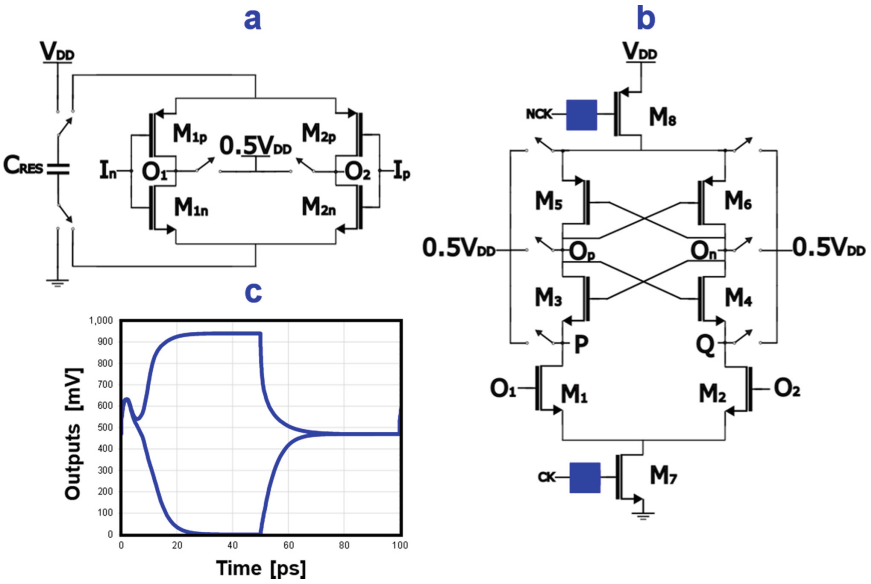

Fig. 3. **a** Dynamic Floating Inverter Amplifier, **b** Double Tail Latch, **c** Outputs of Double Tail Comparator.

The main strength of the Double Tail is maintaining the SA advantages while improving the noise and power efficiency at the cost of a slight delay in the overall decision time, as shown in Fig. 3c. As previously explained, the delay should be kept reasonable compared to the total decision time. The easiest way to estimate the optimal delay is to look at the minimum FoM in a certain decision time range.

4 Conclusion

4.1 State of the Art Comparison

In order to validate the Double Tail topology in a fair comparison, the state of the art has been considered, redesigned in 5nm and simulated through Cadence Virtuoso to meet the given targets. The results are reported in Table 2. Note that the SA is still one of the most performing comparators thanks to its one-stage implementation.

4.2 Final Considerations

The Double Tail comparator stands out as the most efficient topology for the given targets as it employs a low power dynamic bias integrator coupled with a latch which is equally optimized for energy minimization.

This topology suits different applications thanks to the two main degrees of freedom, i.e. the reservoir capacitor in the first stage and the tunable delays in the second. The gain and noise performance may be further improved by stacking the integrator transistors or the tails.

Table 2. Comparator topologies simulated in 5 nm TSMC technology.

Topologies	Decision time charge noise	FoM
Strongarm [8]	9.63ps 1.596fC 2.58 mV	$102.31*10^{-33}CsV^2$
Elzakker [9]	10.89ps 2.411fC 2.37 mV	$147.48*10^{-33}CsV^2$
Bindra [7]	13.40ps 1.249fC 2.52 mV	$106.28*10^{-33}CsV^2$
Tang [1]	10.47ps 1.631fC 2.93 mV	$146.60*10^{-33}CsV^2$
Delayed tang	11.89ps 1.726fC 2.34 mV	$112.37*10^{-33}CsV^2$
Double tail	10.77ps 1.588fC 2.22 mV	$84.29*10^{-33}CsV^2$

Future Work

A further clarification should be added: this work was meant to be built inside a given system where two clock signals (Ck and Nck) and a half supply reference ($0.5*V_{DD}$) had been already employed, therefore the double tail topology required no additional circuitry. Whenever such conditions are not met, the nmos solution mentioned in the "technology" paragraph would represent the most advisable choice.

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