Multi-Chip 3D Integrated Micro-System Based on Microwave Multilayer

Cheng Yang, Zhenghu Zhu, Mengjie Hu, Chao Zhao, and Xu Long

Abstract 3D integrated vertical interconnection technology is an effective way to realize miniaturization, lightweight and high integration of electronic RF system. This paper introduces and verifies a hybrid interconnection structure that combines multiple types of chip stacking and flip chip welding in detail. The vertical interconnection of multiple types of chips and substrates is realized through two assembly methods of lead bonding and flip chip bonding. Finally, multiple active chips and passive devices are high-density integrated in a 60 mm × 60 mm × 1.5 mm active link volume. Compared with the traditional 2D packaging structure, the hybrid interconnection structure can reduce the packaging volume by more than 40% and increase the interconnection density by more than 2 times, effectively meeting the target requirements of miniaturization, functional diversification and rapid response of electronic system equipment.

Keywords Multi-chip stacking · 3D integrated · Micro system

1 Introduction

With the continuous development of military electronic equipment towards miniaturization, lightweight, multi-function and high reliability, the microelectronic packaging industry is also facing new technical challenges. Currently, the density of traditional planar hybrid integration has approached the limit [1, 2], and three-dimensional heterogeneous integration vertical interconnection technology can improve the integration density significantly, which is of great significance for achieving miniaturization and lightweight equipment [3, 4]. Among them, chip stacking [5–7] and flip chip welding technology [8, 9] are an important technical implementation approach

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in three-dimensional heterogeneous integration technology. As a transmission port for receiving and transmitting electronic signals, RF components can achieve system integration and reduce the size and weight of products through multi chip stacking and flip chip welding technology significantly.

According to the product characteristics of RF components in a certain project, a hybrid interconnection structure combining multiple types of chip stacking and flip chip bonding was designed. Through simulation analysis, system structure optimization and other means, three-dimensional integration technologies such as high-density vertical interconnection of the microsystem were developed, key technologies such as traditional multi-chip planar interconnection, high-density and reliable flip chip bonding were broke, the technical pain points and difficulties in miniaturization, lightweight and high integration of electronic countermeasures RF microsystems were solved, the performance and reliability of products were improved, a hybrid interconnected microsystem with ultra wideband and high density integration was developed to reduce system volume while improving its interconnection density.

2 Microsystem Architecture Design

Based on the index requirements of RF components in the project, a three-dimensional multi-layer heterogeneous structure micro system was designed, including chips of digital and microwave functions. The chips of RF and digital functions in the micro system can achieve miniaturization, lightweight, and integration of RF micro systems through chip stacking and flip chip welding. The 3D heterogeneous integration scheme includes three parts: traditional circuits, multi-chip stacked circuits, and multifunctional SIP based micro bump technology on silicon. The multi-chip stack circuit improves the traditional mature RF channel scheme by stacking some chips to improve the integration of the circuit, providing control signals for amplifying and detecting circuits and frequency conversion circuits; The multifunctional SIP assembles a multifunctional RF chip onto a silicon based RDL substrate by flip flopping. The specific layout diagram is shown in Fig. 1, the structural schematic diagram is shown in Fig. 2, and the functions and materials of each chip are shown in Table 1.

3 Process Plan Design and Implementation

3.1 Multi Type Chip Stacking Scheme

The commonly chip types used in RF systems include limiters, filters, amplifiers, geophones, single pole switches, mixers etc. The traditional assembly method of MCM is to assemble and package multiple bare chips and components on the same

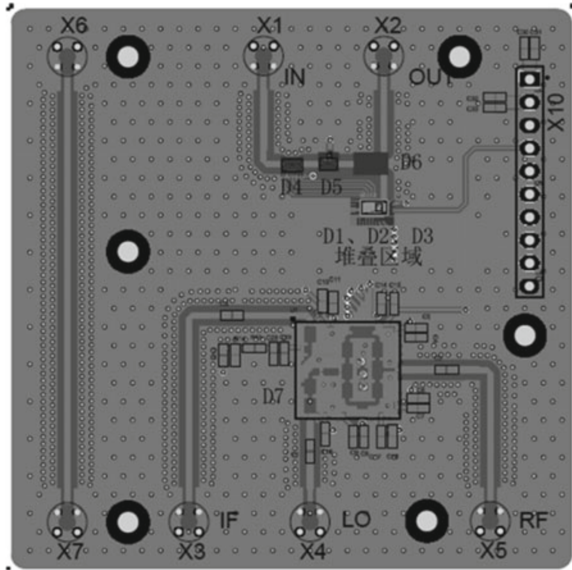

Fig. 1 RF microsystem layout

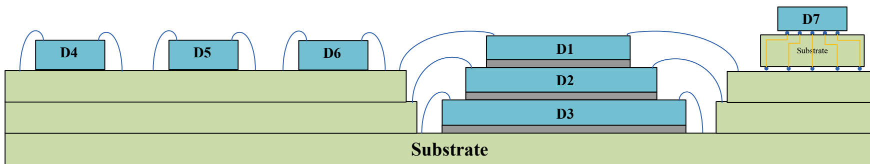

Fig. 2 Schematic diagram of RF microsystem structure

Table 1 Classification of chip functions and materials

Die	Function	Material
D1	Microwave	GaAs
D2	Digital	GaAs
D3	Digital	Si
D4	Microwave	GaAs
D5	Microwave	GaAs
D6	Microwave	GaAs
D7	Microwave	GaAs

interconnect substrate. The assembly dimension is two-dimensional, and the interconnect density is low. Multi chip stacked die technology is an important packaging method to realize miniaturization, high density, high-speed interconnection and multi-functional integration. It shortens the interconnection length, improves integration and obtains smaller overall dimensions significantly, which can meet the

requirements of the micro system such as miniaturization, lightweight and high reliability in this project. Therefore, the success of multi-chip stacking directly determines the quality of microsystem interconnection.

Chip stacking should adopt different stacking methods according to different packaging requirements. Currently, there were three main methods of chip stacking, including: pyramid chip stacking, dislocation chip stacking, and alternating chip stacking.

Combining the product characteristics and technical specifications of the microsystem, this article uses a pyramid type chip stack to achieve high-density vertical interconnection of three layers of chips. Chips with microwave and digital functions in RF microsystems were stacked in a vertical direction through chip-on-chip layer stacking, and the chips with the substrate were interconnected through wire bonding. Finally, three-dimensional integration of chips with different materials and functions was realized. When designing a chip stack structure, it was considered that directly stacking chips on top of microwave chips would have an unpredictable impact on the microwave performance of the system. In the stack structure, microwave chips D1 were placed on the top layer, and digital chips D2 and D3 were sequentially stacked below D1. The specific process flow of multi-layer chip stacking is shown in Fig. 3.

Due to the relatively thin thickness and weak stress resistance of stacked chips, it is necessary to reduce stress during chip placement to avoid chip bending. The adhesive between the chips not only plays a bonding role, but also plays a role in buffering stress. A thicker adhesive layer can solve the stress problem well, but it will affect the quality of the patch when the adhesive layer is too thick. During the assembly process, it is necessary to control the thickness of the adhesive layer to reduce stress reasonably; The curing conditions of the patch adhesive also have a significant impact on the stress. Too high curing temperature is not conducive to

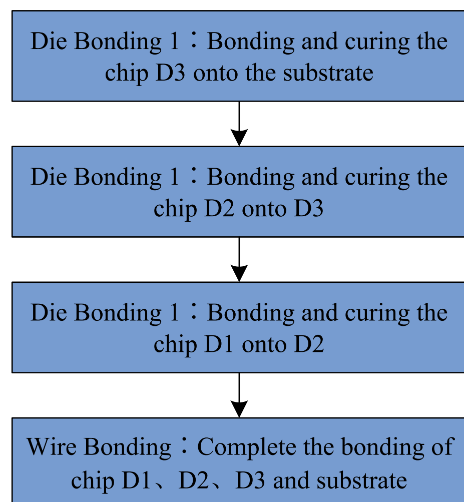

Fig. 3 Multichip stacking process flow chart

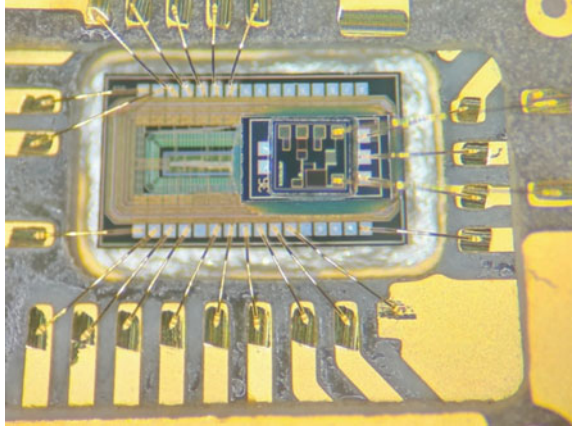

Fig. 4 Physical image of multiple types of chip stack

stress relief. When the patch adhesive is cured, it is necessary to reduce the stress by lowering the temperature and extending the time. Therefore, it is necessary to optimize the thickness and curing conditions of the adhesive to ensure the quality of multi chip stacking when stacking chips.

The physical photos of the final stacked multiple types of chips are shown in Fig. 4.The stack structure has three layers. The chips order are D1, D2, and D3 from top to bottom. The chip stack structure improves the integration density of the system and reduces the corresponding volume by one-third.

3.2 Flip Welding Scheme

In the microsystem, D7 is a transceiver module based on the FO process, with a solder bump of Sn63Pb37 at the bottom and solder ball diameter was 200 μ m. The method of flip chip welding is used to realize its cascade with the microwave substrate.

Flip chip welding is the method of aligning chips and substrates that need to be interconnected using dedicated flip chip welding equipment, and then welding to form intermetallic compounds to achieve interconnection. The commonly welding methods include reflow soldering and hot press soldering. Compared to reflow soldering, hot-press soldering can realize shorter connection paths, smaller contact resistance and better warpage. Therefore, the method of hot-press welding is used for flip chip welding of D7 in this article. In order to achieve good flip chip welding results, it is necessary to coat the substrate with flux or pre-treatment with the same temperature gradient solder paste before flip chip, and then complete the interconnection through the optimized flip chip bonding process.

Because of low interlayer height and high solder ball density, it is difficult to clean the flux between the solder balls after flip chip welding of D7. And the residual flux can affect the long-term reliability of the system. Therefore, it is necessary to

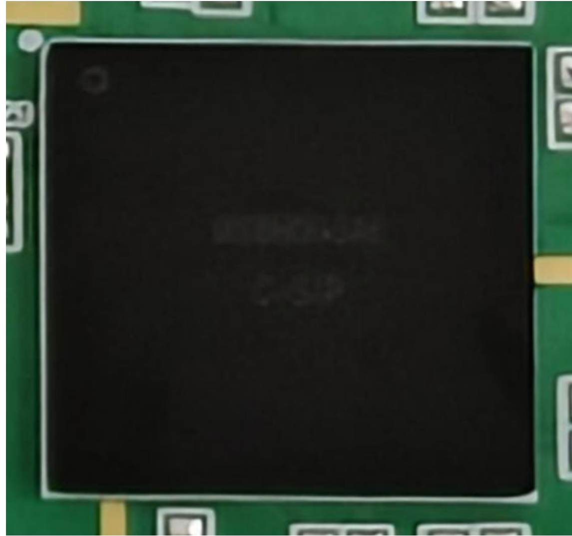

Fig. 5 Physical image of multiple types of chip stack

obtain better cleaning ability by setting reasonable cleaning parameters to thoroughly remove the residual flux.

The physical image of D7 after flip chip welding is shown in Fig. 5.After flip welding, the interconnection between D7 and substrate were changed from gold wire bonding to solder bumps which shortening the interconnection path and improving the integration density.

3.3 Microsystem Integration Scheme

The integration scheme of the microsystem is as follows: Firstly, the surface mounted resistive and capacitive devices are welded on the microwave substrate using solder of Sn96.5Ag3Cu0.5; Secondly, the Sn63Pb37 solder balls on the D7 chip are connected to the microwave substrate in a high-density cascade through flip chip soldering; After completing the stacking of D1, D2 and D3 multi-chips, the remaining bare chips are bonded and fixed to the corresponding electrical interconnection positions through conductive adhesive, complete wire bonding; Finally, the connector is manually welded to the substrate to complete the assembly of the microsystem. The entire process assembly process is shown in Fig. 6.

The finished rendering of the microsystem is shown in Fig. 7, with a final size of approximately 60 mm $\times$ 60 mm $\times$ 1.5 mm. Compared to traditional 2D packaging structures, this hybrid interconnect structure can realize package volume reduction of more than 40%, interconnect density increase of more than twice et al., and improve the volume, size and integration density of RF systems effectively.

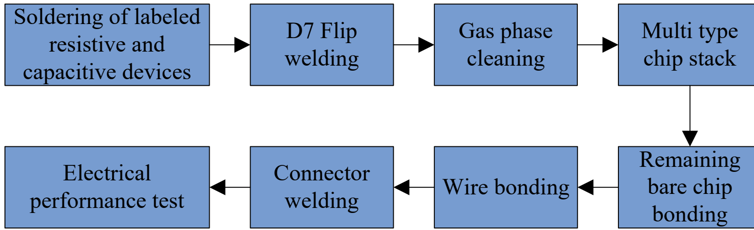

Fig. 6 Process assembly flow chart

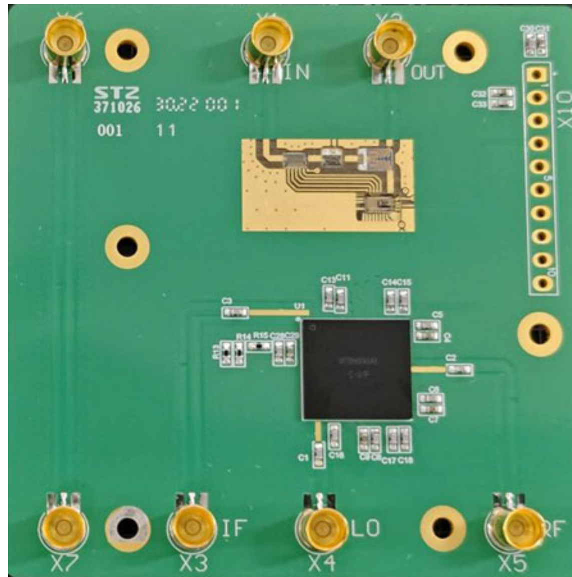

Fig. 7 Physical diagram of microsystem

4 Conclusion

This paper designed a hybrid interconnection structure that combined multiple types of chip stacking and flip chip soldering. Through reasonable process design, multiple active chips and passive devices were integrated into a single 60 mm × 60 mm × 1.5 mm active link volume with high-density, high-density vertical interconnection integration of multiple types of chips, chipsets and multi-layer microwave substrates has been realized. Compared with traditional 2D packaging structures, this hybrid interconnection structure can realize packaging volume reduction of more than 40%, interconnect density increase of more than twice et al., and meet the target requirements of miniaturization, functional diversification and rapid response of electronic system equipment. It also provides a design idea for miniaturization and high integration solutions of the same type of RF systems.

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