Manufacturing of Silicon Solar Cells and Modules

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Abstract

To get from cell making to module making requires proper preparation of pristine wafers to be physically and electrically connected in series to achieve the rated output of a PV module. This chapter highlights the "silicon wafer to PV module" journey, with all pertinent steps of optically and electrically augmenting each wafer explained in details. The steps of connecting, co-firing and testing of the modules are also given.

1 Introduction

Silicon-based solar cells (and consequently modules) still dominate the PV market (more than 85%) compared to other commercially available thin film and third-generation photovoltaics. Apart from the obvious reasons of well-established silicon manufacturing processes developed originally for microprocessors, the abundance of silicon as silicon oxide in Earth's crust is another reason. However, not any "sand" is appropriate for wafer-building purposes. Quartz is a crystalline form of silicon oxide that can be harvested with less chances of containing contaminants within the collected aggregate. These quartz particles, available in Unimin's mines near Charlotte, North Carolina, can be described as ultra-pure compared to their silica counterparts available elsewhere in the world (Beiser 2018).

Terrestrial photovoltaic made from silicon starts as p-type monocrystalline Czochralski (Cz) silicon substrates. But due to the lower cost of multi-crystalline (mc) silicon, in the 1980s mc silicon wafers rose as a potential candidate to replace single-crystalline (sc) ones. On the other hand, their lower metallurgical quality due to the presence of defects in the form of grain boundaries has precluded achieving efficiencies similar to those of Cz, so that both technologies shared a rather constant and equal figure of merit ($/W). With progress in silicon manufacturing technologies, a monocrystalline solar cell made a gradual comeback since the mid-2000s, as evident from Fig. 1. The high efficiencies of such cells as well as their aesthetic presence (since they are a darker shade of the usual blue of multi-crystalline-Si cells) made consumers and producers cause an increase in demand for monocrystalline modules.

On the other hand, the production of mc-Si has not slowed down either. As mentioned before, after 2007, the market has been presented with new opportunities in the Chinese market. The manufacturing processes' yield and economics have yet again tipped the scale towards the multi-crystalline side. The mass production of such p-doped wafers not only enhanced their figure of merit, but also drove many wafer-making companies around the world out of business, such as Al Mulk holding who used to manufacture solar panels in the United Arab Emirates and currently the focused on installing them (UAE-based Mulk Holdings International pens JV agreement to enter US market 2021). This is clearly shown in Fig. 2 which demonstrates a clear advantage for mc-Si that has only been cemented in the years after (Miles et al. 2007).

Apart from economic aspects that are necessary for manufacturing firms to survive, there are various interrelated

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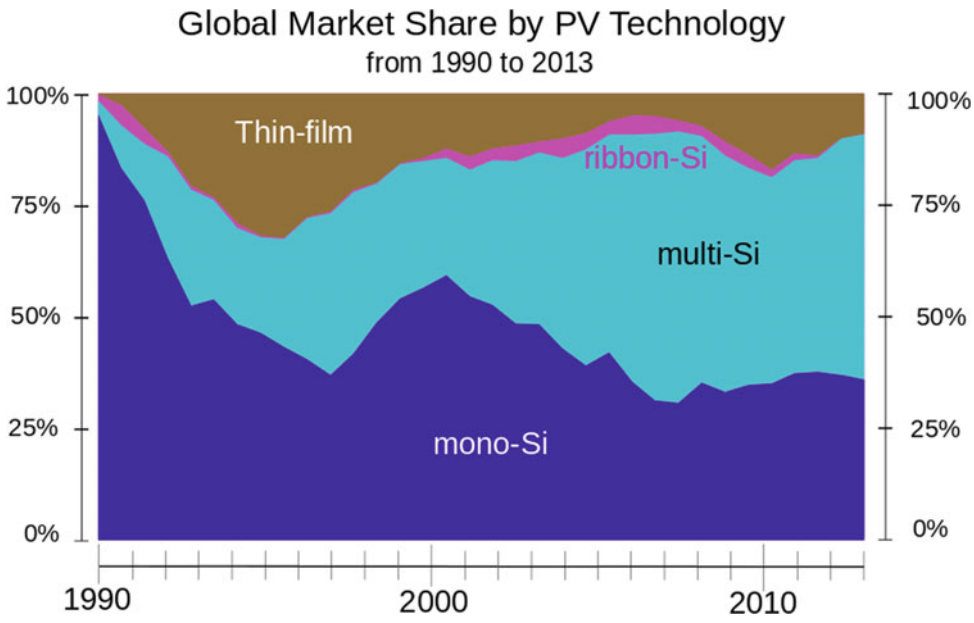


Fig. 1 Global market share of PV technologies (https://commons.wikimedia.org/wiki/File:Global_Market_Share_by_PV_Technology_from_1990_to_2013.svg)

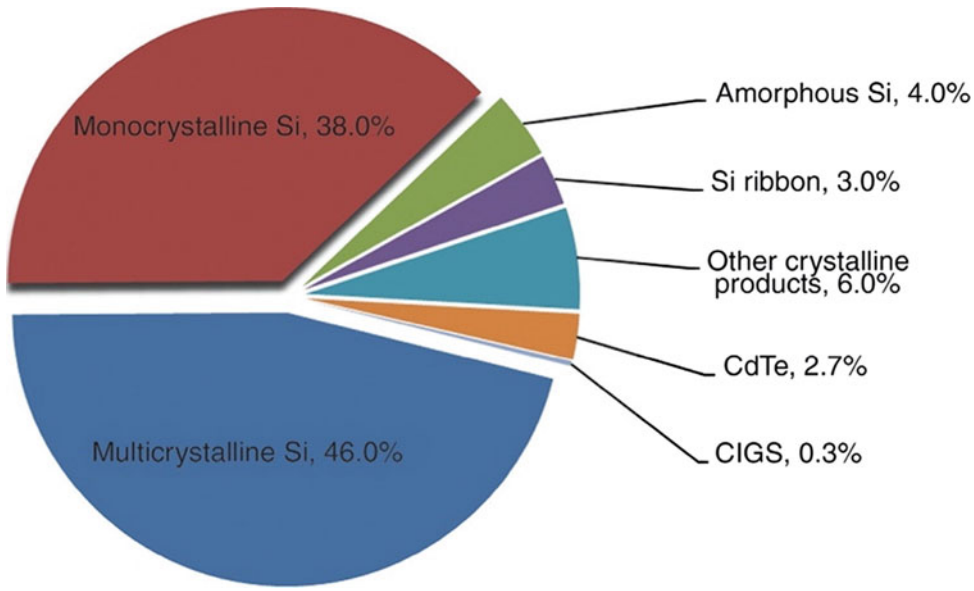


Fig. 2 Solar cell technologies contribution in 2006 (Miles et al. 2007)

parameters that are crucial to arrive at a functioning final product. The manufacturing process must integrate physical properties of the materials to their electrical performance, stability and optical performance in order to guarantee the reliability of produced solar cells. These cells will be electrically connected, encapsulated and installed, which also necessitates proper testing procedure before their dispatch to customers. The properties needed can thus be subdivided into surface and bulk properties as will be explained in the following sections.

2 Silicon Bulk Properties

The bulk properties of silicon solar cells are controlled by selecting a material that has the appropriate bandgap, selectively doping it to allow smooth movement of carriers without causing any undesirable recombination and reducing avoidable losses such as reflection or high sheet resistance as well as low carrier mobility. These main parameters are explained below.

2.1 Bandgap Selection and Tuning

Monocrystalline Si semiconductors have an indirect and a direct bandgap of EG = 1.17 eV (exactly in the middle of the solar radiation) and 3 eV, respectively, at STC conditions. Two electron–hole pairs generation events are possible, however rather rare, caused by high-energy (low wavelength) UV photons. At longer wavelength than visible range (Vis: ~380 to 800 nm), any incident solar radiation causes the formation of excess charge carrier absorption that overshadows desired band-to-band generation and separation. In other words, care must be taken in operating silicon solar cells away from their designated wavelength range.

2.2 Carrier Concentration

The intrinsic carrier concentration links the imperfections and the disequilibrium of the crystal lattice to the potential voltage generation. At high carrier densities caused by excessive doping, the band structure is altered, which exposes more charge carriers and increases the effective intrinsic concentration. Moreover, the quality of the targeted regions (doped) is inversely related to the doping level. Although it is intuitive that having more carriers would mean better electron/hole diffusion within the material towards the contacts as seen in Fig. 3, too many carriers available is likely to slow the diffusion due to the crowding of similarly charged species that tend to generate repulsive forces. The reader is reminded at this point that the solar cell has two processes that should proceed in equilibrium, the first is the electron diffusion (through carriers) through the bulk of the material and the second is the electron motion outside of the cell and through the selected electrical load.

2.3 Recombination

The timeframe for a photogeneration event, their separation and transportation to respective side of the solar cell can be measured on a femto-second scale. Characterization and observation equipment capable of pursuing such processes are either economically unavailable or require extensive retrofitting to allow the observation of how electron/hole pairs are generated and how to coerce them to separate and follow the desired path to allow the cell to operate at highest quantum efficiency. Usually, recombination within the structures of Si semiconductors is governed by defects and grain boundaries are described as Shockley–Read–Hall (SRH) lifetimes and can be described by avoidable and nonavoidable recombination. The associated lifetime τ (defined with respect to the diffusion length L, which is a small portion of the solar cell overall thickness) increases for good quality materials. Remember that:

1. At higher concentrations, Auger recombination becomes more prominent (a nonavoidable recombination). Excitonic effects have also been noted to intensify Auger coefficients at high or near-high (moderate) carrier densities.
2. Band-to-band direct recombination, although a base mechanism for electron–hole pair recombination, is insignificant quantitatively. It is still nonavoidable recombination but has lower effect than Auger because it requires high-energy conversion levels.

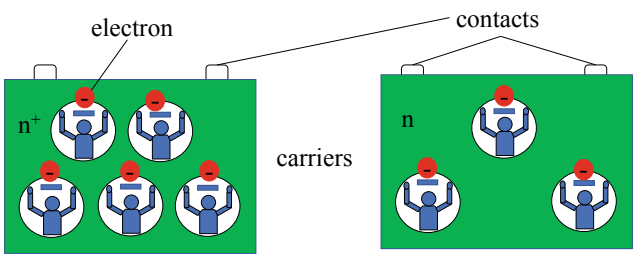


Fig. 3 High concentration of carriers (n+) compared to ideally doped n-type regions

2.4 Electron Mobility

Electrons possess mobilities that are almost triple those of holes at low or near-low (moderate) concentrations. Note that scattering caused by defects and carrier-carrier scattering are highly manifested at higher doping densities and high injected materials, respectively.

2.5 Surface Contacts

To allow electrons to reach the intended electrical load, they need to diffuse from their generated locations through available carriers to the contacts (see Fig. 3). Contacts form an interconnected network to connect the electrical circuit consisting of the solar cell and the electrical load, which are scaffolded on top of the Si solar cell surface. Even though these contacts are essential for charge carrier extraction, they cause shading as they cover 5–10% of the area exposed to incident solar radiation. Another issue is the increased series resistance as the interface between the contact and the bulk silicon material is not perfect. All the while the charge separation has to be planned to minimize recombination and slow diffusion rates which reduces the overall efficiency (through fill factor reductions) of the solar cell.

As will be explained later, a heavily doped region (n^+, $n^{+}{}^{+}$, p^+ or p^{++}) under each of the contacts is added and would act like a conveyor belt to pump electrons or holes towards the contact in the n-region or the back-surface field, respectively. This allows the majority carries to permeate and reach the targeted contact at a low voltage loss (but with significant resistance). The flow of minority carriers (electrons in P-regions and vice versa) is best described as the surface recombination velocity (SRV) or *S for short*. Usually, the surface recombination velocity is high ($S = 10^6$ cm s^{-1}) and is limited only by thermal diffusion.

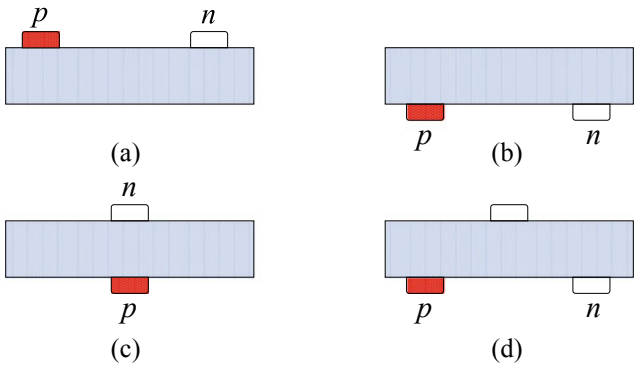


Fig. 4 Permutations of contacts placed on wafers

3 Crystalline Silicon Solar Cells

Considering the previous discussion, there are certain parameters that can be identified to augment the overall efficiency of the cell by focusing on the optimization of said parameters. Thus, the following are four cardinal rules to minimize avoidable losses:

1. Reflection events are attenuated and minimized to low levels using light trapping techniques.
2. Minimum recombination is allowed: Only Auger and radiative recombination mechanisms are accounted for.
3. Ideal contacts exhibiting no shading or series resistance losses.
4. No recombination losses while charge carriers are transported across the thickness of the cell (flat carrier profile).

Champion efficiency cells use intrinsic material to regulate and reduce the Auger recombination as well as free-carrier absorption. This cell is less than 100 μm thick, which is a trade-off between the required absorption and minimal nonavoidable expected recombination. Considering the thermodynamical limit, a 29% maximum efficiency is obtained under STC conditions.

3.1 Cell Contact Design

If contacts are placed on the top of the cell, it would intuitively satisfy rule #4 placing them as close as possible to photogeneration events. On the other hand, this will cause shading and thus the violation of rule #1, as shown in Fig. 4a.

To avoid such complications, contacts can be placed at the bottom of the cell, as in Fig. 4b which theoretically guarantees a high efficiency (23%) but might require altering doping concentration on the top because since the holes are lighter than electrons. The latter fact suggests that the best solution is to put the contact per face as in Fig. 4c which is simpler. Minority carriers (electrons in P-substrates) in the substrate are usually extracted at the front (top) face, given that their low density hinders their collection probability. The diffusion length represents the maximum material thickness a charge carrier can cross before it is depleted (recombined). On the other hand, majority of carriers with their high diffusion length can travel all the way to the back surface for simpler collection. Several designs implemented minority carrier extraction contacts at both the front and back of cells for higher utilization of photogeneration events, as shown in Fig. 4d.

3.2 PERL and Commercial Cells

The passivated emitter rear locally diffused (or PERL for short) solar cells harbour efficiencies bordering 25% under STC, due to the implementation of novel micro-electronic techniques (Magsi 2014). The term "passivated emitter" relates to the formed high-quality oxide at the front surface of the cell that attenuates the phenomenon of charge carrier recombination in that region and improves the overall efficiency. The rear is locally diffused only at the metal contacts, to prevent recombination and retain a good electrical contact. This will be presented in detail later in this chapter.

Both laboratory-level solar cells with nearly 25% efficiency shown in Fig. 5a and commercially available ones have efficiency levels of 16% (for multi-Si) and 17% (for mono-Si) as shown in Fig. 5b. These cells display the contacting structure of one contact per face. The cell performance is shown in Table 1.

4 Conventional Solar Cell Manufacturing

The following sections will focus on most important parameters for solar cell building and how to optimize each in order to arrive at a device that functions optimally.

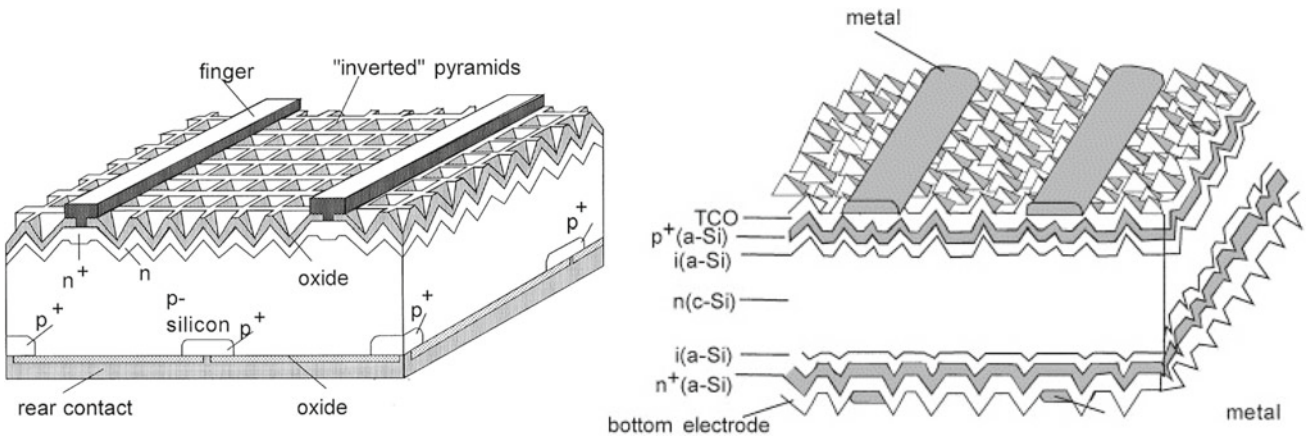


Fig. 5 **a** PERL versus **b** commercial solar cells (Green et al. 2001) (with permission 5364101367492)

Table 1 Cell performance (Bai et al. 2020)

Cell type	Ideal parameters (calculations)	Passivated emitter rear locally diffused solar cell (PERL)	Industrial solar cells' average parameters
Size, cm^2	–	4	225
Thickness, µm	80	450	250
Sheet resistance, Ωcm	Intrinsic	0.5	1
Short circuit current density, Acm^{-2}	0.0425	0.0422	0.034
Open circuit voltage, V	0.765	0.702	0.600
Fill factor, FF	0.890	0.828	0.740
Efficiency, %	28.8	24.7	15.0

4.1 Substrate Selection

Monocrystalline Cz-Si or float zone (FZ-Si) material shows the highest industrial performances with no defects in the form of grain boundaries, where there are light contamination levels of both metallic and oxygen, nitrogen and carbon (O, N, C) impurities, which leads to durable SRH lifetimes ($\sim$1 ms), however still short of the Auger limit. Magnetic Czochralski (MCz) processing of the silicon material harbours less concentrations of oxygen than sole Cz-Si and thus providing the base for higher efficiency solar cells (less O_2 = less SiO_2 = less defects = long lifetime = high efficiency). The process is, however, prohibitively expensive.

With better production economics and manufacturing technologies, commercially established photovoltaic cells are based on block/ribbon MC-Si P-substrates. Moreover, crystal defects including grain boundaries, lattice dislocations and metal impurities are more prominent than Cz or Fz because of lesser time for precipitation and gettering due to the rather rapid solidification of monocrystalline silicon. As a result, the lifetime within multi-crystalline silicon is understandably lower. This, however, can be mitigated by applying various modifications and additions to the manufacturing process that would diminish the potent metallurgical effects. For example, using gettering techniques is known to reduce contaminant impurities resulting in less dominance of avoidable lifetime reducers. This can be achieved by adding getters. In a gettering process, a sacrificial region is formed, able to trap impurities that reduce the lifetime of charge carriers in such a way that no adverse effects are borne on the device being manufactured, or at least where they are accessible and conveniently etched off. However, due to the high concentration of impurities, this deems the getter region as "electrically dead", which adversely affects the UV response of the manufactured device.

4.2 Doping Level and Type

Controlling the doping level can control the recombination and the series resistance. A suitable doping level is determined after an optimization process considering the structure of the cell and the governing recombination mechanism.

Boron doped (P-Substrates) hold the champion efficiency for laboratory scale cells as well as lucrative low costs for industrial applications. Such substrates harbour high Auger limiting charge carrier lifetimes; however with higher SRH recombination, higher doping levels are achieved to decrease the density of charge carriers (increase the rate of recombination), at a given voltage, while this is compensated by the reduction of the lifetime. The series resistance is also reduced at high doping levels, which is prominent in thick cells and affects the electron transport to the back surface of the cell. 1016 cm^{-3} doping levels are present in industrial cells. Point contact cells have achieved high efficiencies, however, with both low (PERL cells—1 Ωcm) and high substrate resistivities.

4.3 Cell Thickness

In cells with high diffusion lengths with respect to the device thickness, surface recombination arises as a severe issue: if the surface recombination speed (S) is higher than diffusion length/device thickness ratio for minority carriers ($\sim$250 cm s^{-1} for high performing cells), decreasing the thickness of a given cell for a given voltage increases the recombination. Although thin cells absorb less light (due to penetration depth), this can be countered by light trapping techniques. Moreover, thinner cells require more expensive feedstock material, which increases the cost and hinders the ability to industrialize thin cells. Also, technologically evolved wafering methods allow processing of very thin, large-area substrates with least breakage rates, which otherwise could lead to a large scrap fraction due to breakages during processing and transporting between processing stations. It should be mentioned here that light trapping and surface recombination are limiting factors on imposing cell thickness. With the addition of a BSF (rear passivation), the typical thickness for a solar cell has been normalized to be 200 μm which is compatible with minority carrier lifetimes.

4.4 Front Surface

A grid of metallic fingers is used at the forefront of solar cells to gather the rather segregated photogenerated charge carriers. An optimization process must be carried out between the transparency of the front surface of the cell and the series resistance as there is a trade-off between the two factors, in order to produce thick, conductive metal fingers with low series (contact) resistance. These two requirements are important, but they have an inverse relationship. Contacts carry electrons from the cell bulk to the external load, but they reduce transparency and reduce series resistance.

Thin fingers in the range of $\sim$15 μm are obtained for lab-scale solar cells using physical evaporation or photolithography processes. The choice of materials for these thin metal fingers should consider good conductivity, manufacturability as well as good compatibility (low interfacial resistance) with the bulk silicon. Material combinations such as Ti/Pd/Ag are suitable with n-type silicon producing high conductivity. Nickel possesses these characteristics but is not amenable for mass production. Nickel plating of laser-carved grooves results in 40 μm deep and 20 μm wide fingers. Laser-grooved buried grid, previously used in highest efficiency, does not suffer from coarse metallization techniques or high shading and resistance losses.

100 μm wide lines based on screen-printed silver pastes are utilized in commercially available cells. Laser-grooved, buried grids are usually used in highest efficiency since it does not suffer from coarse metallization techniques or high shading and resistance losses, but it would complicate the manufacturing process and increase production time of a cell.

4.5 Homogenous Emitters

Under the metal lines of the contacts, the substrate benefits from heavy doping (n^+ or n^{++}) to make the contact selective and decrease recombination. Think of a conveyor belt that pulls electrons or holes to the contact. The doped region of the emitter (called emitter and has to be as thin as possible to reduce possibility of the recombination of the recently generated electron/hole pairs) covers the top surface of the solar cell offering minority carriers a gateway to be collected by the metallic contact fingers as shown in Fig. 6.

The challenge that remains for exposed surfaces that are electronically conductive is that they allow recombination to occur before the electron is transported into the external load. This highlights the importance of having passivated emitters, where the emitter (n-region) is thin and subjects minority carriers to high surface recombination velocities which results in poor collection of the generated charge carries in that region.

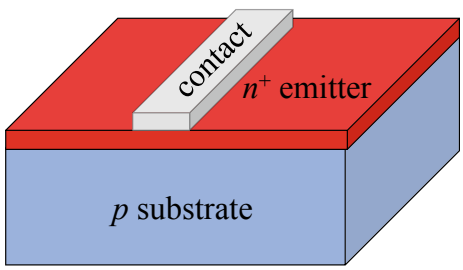


Fig. 6 Heavily doped (n^+) emitter layer underneath contact finger

Thin and highly *n*-doped regions surrounding the interface with the contacts (and only there) act as a pump for charge carriers while allowing the surface to be passivated as shown in Fig. 7. Lowering the doping levels in the bulk has a positive effect on the charge collection efficiency of the emitter to avoid wide-scale heavy doping and its undesirable effects. This localized higher concentration doping lowers the sheet resistance and diminishes recombination at the metallic interface by increasing the depth of the emitter. If charge carriers are said to be collected at the top surface of the solar cell, this gives away that the thickness of the emitter is less than the diffusion length of the minority carriers, which further implies a high SRV. Recombination can be further mitigated by making the interface between the emitter and the finger narrower than the finger by using laser grooving. The emitter can be made as deep as 1 μm, enhancing the contact conductance.

Further improvement involves enhancing the diffusion in different regions since requirements are so different yet can be discretized. For example, Fig. 8 depicts a strongly doped *n*-type emitter (n^{++}) and thick region right underneath the fingers surrounded by a thin and lightly doped (n^{+}) area right underneath the passivating layer.

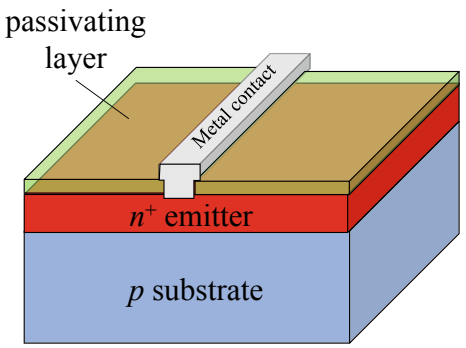


Fig. 7 Adding a passivating layer on top of emitter to ensure surface passivation

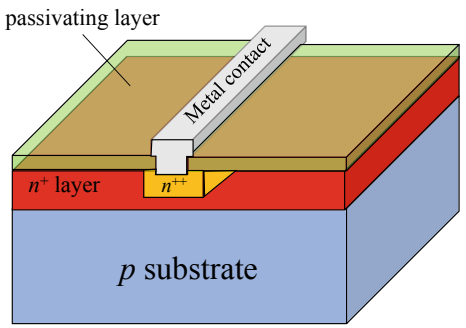


Fig. 8 Adding a heavily doped n^{++} layer right underneath the contact to enhance electron diffusion

These "selective emitters" need complicated photolithographic processing. These point emitters work best in concentrating applications (more than one sun). Small cross-section metal finger reduces series resistance.

4.6 Heterojunction Solar Cell Structure

Although it is a trait of third-generation solar cells, a transparent electrode fully covered solar cell front surface with a middle amorphous silicon layer reduces the interface recombination levels and a screen-printed grid helps with the lateral conductance. The topology of such layout is shown in Fig. 9.

Highly doped emitter decreases the contact resistance, and the layer can be buried at a shallower region so that it is not pierced during the metal finger firing and co-firing which can potentially short-circuit the junction. Moreover, metal fingers must be spaced apart to keep shading losses in order, which means that emitter and lateral conductance must also be high.

5 Industrial Cells

Commercial phosphorus-doped emitters can boast surface concentrations over 10^{19} cm^{-3} and are 0.4 μm deep, along with 60 Ωcm sheet resistance. The highly doped region harbours a high level of getter and precipitated foreign materials (due to heavy phosphorous doping) resulting in an electrically dead layer, where the collection of short wavelength photons is improbable, with a large intrinsic current density. SiN_x suits the purpose of surface passivation which allows for screen-printed cells to incorporate selective emitters.

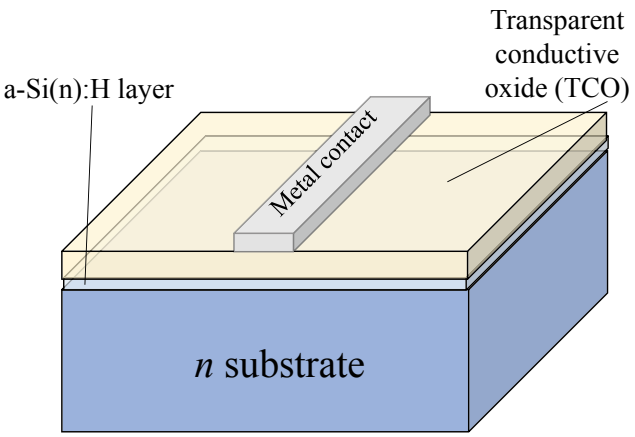


Fig. 9 Topology of a heterojunction solar cells

5.1 Back Surface Field

The back-surface field (BSF) is the hole collector. It needs not to be transparent like the emitter and thus is usually made of a thin layer of metal (preferably gold). The BSF can take advantage of a p^+ layer in order to decrease contact recombination for cells with $w < L$.

Most commercial cells can boast a screen-printed or thermally evaporated aluminium BSF with a subsequent silver (Ag) or an Ag–Al solid solution electrode. The contact can cover the whole surface and need not be in the form of a contact finger and can cover the entire back surface with a reflective layer that can assist in reflecting unabsorbed solar radiation and allow the cell a second chance to use it. An example of the back-surface field is shown in Fig. 10.

5.2 Cell Size Effects

Although larger size solar cells allow for more W/m^2 of solar irradiance absorption, working with such cells has many disadvantages from operational point of view (larger size allows more recombination events and longer distance to reach contacts which will decrease efficiency). It is known that the area of a given cell determines the device's end efficiency in lab-scale cells. And since the emitter region is contoured by masking or etching, the effective edge of the emitter is located at a respectable distance from cell's edge, which reduces recombination, as surface edges act as a hub for surface recombination that negatively affects high diffusion length devices.

Cell sizes preferred by the industry usually 12.5 × 12.5 cm or 15.6 × 15.6 cm are the norm. Apart from manufacturability issues, increasing the size of a given cell, increases the spacing between the charge carrier collection terminals, thus increasing joule losses. The electric resistance of the metal fingers is proportional to the quadratic power of its length. The mitigation of the resulting series resistance happens at cost of increased shading as increasing the number of terminals connected to the busbars, decreases the distance that charge carriers have to cross from the metal fingers connected to them. Another deciding factor comes from the manufacturing process of the original silicon ingot. Cz silicon is limited by the surface tension of the silicon growing around the seed crystal during production.

5.3 Cell Optics

The efficiency of a cell largely varies depending on how much incident solar radiation it can absorb. Not only due to intrinsic parameters, such as the material bandgap, but also external factors such as the surface condition of the cell. Ideally, cells must optically absorb photons from the whole spectral range of the hemisphere. For uniformity and comparison of different solar cells, a standard spectral distribution of an air mass (AM) is 1.5 and 0.1 W cm^{-2} is used. Global incident irradiation is considered at 25 °C. Metal grid shading propels the level of optical losses in non-encapsulated cells. Various solutions have been both proposed and implemented to mitigate shading losses by deploying shaped fingers with a prismatic top. Industrial scale cells harbour an optical loss of the order 7% while lab-scale cells are much lower.

Next comes the losses due to direct reflection, which can amount to as much as 30% of the incident radiation for bare silicon in air due to its high refractive index. This necessitates the utilization of an anti-reflection coating (ARC) on top of the emitter. This works exactly like ARC layers on spectacles, where light will reflect off the glasses and affect communication quality if others cannot see one's eyes, as shown in Fig. 11. Adding the ARC to the emitter will prevent reflection at the outset and allow the cell the opportunity to absorb light. This reflectance can be attenuated and

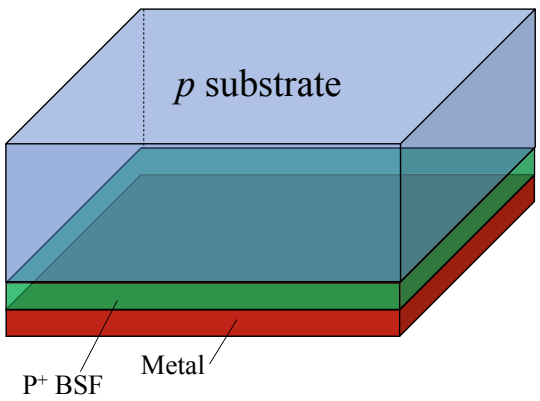


Fig. 10 Topology of the back-surface field (BSF)

Fig. 11 Spectacles **a** without anti-reflection coating (ARC) and **b** with ARC (https://www.allaboutvision.com/lenses/anti-reflective.htm)

can reach up to zero reflection, by utilizing a non-absorbing layer on top of the Si substrate surface with a different refractive index (nARC).

Snell law states that reflection is minimal when the thickness of the layer of a certain material is an odd multiple of quarter of the free space wavelength. Adding a thin layer of a dielectric material decreases the level of reflection due to effective interference effects which would help enhance cell output. In other cases, reflection increases up to the value of ARC, however never above it. ARC is usually at a refraction value calculated by taking the average of the refraction index of air and the targeted material (Si in this case) at 600 nm, where SiN_x is a viable material to be used at 2.4 refraction index, usually deposited by plasma enhanced chemical vapour deposition (PECVD).

5.4 Texturing of Cell Surface

Texturing exposes metallurgical planes or introduces random topological markings that scatter incident radiation within the material, as shown in Fig. 12. Chemically etched textures are utilized in both laboratory and industrial scale devices (silicon solar cells), with the addition of ARC, which reduces the optical reflection to desirable levels. Texturing can be done chemically (base or acid), mechanically or using photolithography techniques. In the case of acid etching, fine features are obtained of the inverted pyramids with a much more controllable geometry using photolithographic techniques. Thus, photons incident on the inverted pyramids (textured surface) are still normal to the cell in question.

5.5 Light Trapping

Silicon surface is only capable of weakly absorbing photons with low energy and high wavelength. Hence, unless the internal reflectance of the silicon is large, most of the photons will break out of the surface. In order to achieve high reflectance events, light trapping techniques are utilized. These events allow the cell material multiple chances at absorbing the light as it bounces back from the back-surface field or as it interacts with quantum-scale materials. Quantum dots made from special materials distributed near the surface of the cell are nano-scale material that amplify incident radiation via quantum-based interactions. These interactions are based on the dual nature of the light. Once the light hits the material quantum dots, it starts to vibrate/resonate and the light will be amplified. The BSF can turn into practical back mirrors since metals are good reflectors. Oxide structures such as Si–oxide–metal structure are able to produce large reflectance due to the optimization of the interference effects especially when it is etched, exposing the family of planes such as {111} or {001}. Light trapping improves the absorption of the wafer by increasing its effective thickness. In the case of one-side isotropic illumination in the geometrical optics regime, the maximum enhancement factor is calculated from knowing the refractive indices of silicon and air as follows:

$$F = 4\left(\frac{n_{\mathrm{Si}}}{n_{\mathrm{air}}}\right)^2 \tag{1}$$

This means that each wave will resonate for fifty times within the cell thickness before escaping (remember that $n_{\mathrm{Si}} = 3.5$ and $n_{\mathrm{air}} = 1$). Due to high contest of absorption by free carriers at long wavelength, the improvement in the photogeneration will not be high.

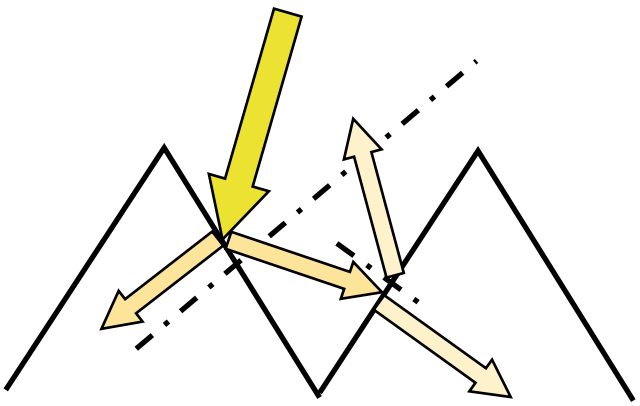


Fig. 12 Texturing effects on incident solar radiation causing multiple reflections within the material

6 Module Manufacturing Processes Overview

The quality of a solar photovoltaic module is a direct result of meticulous processing of individual solar cells. After the production of the wafer as per the discussion in the previous chapter, as well as the enhancement opportunities discussed above, a solar cell becomes ready to be incorporated into a module, where it is connected in series and in parallel to other cells. Figure 13 shows a general sequence of manufacturing processes to arrive at a quality solar cell.

6.1 Starting Materials and Processes

Solar-grade Cz-Si ingots are sliced into round wafers that are trimmed to a pseudo-square shape. The starting material can also consist of MC-Si square wafers with nominal

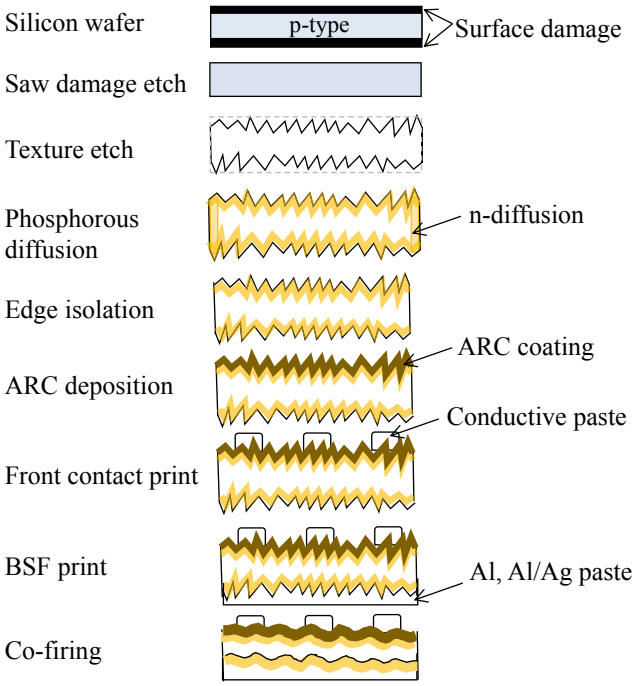


Fig. 13 Sequential manufacturing processes of a silicon solar cell

dimensions: 12.5 × 15.6 cm, a thickness: 180–200 μm (less is better) and standard doping of p-type (boron) to a resistivity 0.5–6 Ωcm. The diagram of Fig. 14 shows the general sequence of processes.

6.2 Saw Damage Removal

Sawing operations usually utilize abrasive materials (discs, wires, etc.) that are sure to leave the surface of wafers with an extensive damage and debris that is stuck to the outer rims of the wafer. This diminishes the quality of the surface region and renders the wafer incapable of reliably hosting further layers and/or causes the wafer to fracture during processing.

This issue can be fixed in an acidic or alkaline bath, where 10 μm are etched off from each face. The wafers are placed in Teflon tapes that are submerged in tanks with a solution subjected to concentration and temperature regulation. Alkaline etches are advantageous to their acidic counterparts, due to their less hazardous waste. Nevertheless, acidic solutions are recommended for multi-crystalline material as they result in an isotropic structure.

6.3 Texturing

Texturing is used for cleaning and also to introduce a surface structure that allows light trapping. This can be done with chemical (acid/base), physical (plasma or laser) or mechanical etching.

6.3.1 Chemical Texturing

Potassium hydroxide (KOH) etching is applied for monocrystalline material as they form microscopic pyramids. However, pyramid size must be optimized as it affects the optical properties. For instance, sufficiently small pyramids tend to cause high reflection, whereas large ones tend to obstruct contact formation. This is shown in Fig. 15 (Al-Husseini and Lahlouh 2017), where the random-sized pyramids preclude omnidirectional reflections, promoting light reflection into the materials.

The shape and size of the pyramids as well as texturing coverage and adequate pyramid size depend on many factors including temperature, solution mixing and wafer residence time in the chemical bath. Practical bath parameters call for 5% KOH concentration at 80 °C for 15 min. Alcohol is usually added to enhance the wettability of the silicon surface, in turn enhancing the homogeneity of the solution. Anisotropic texture consisting of alkaline solutions is applied to multi-crystalline wafers; however, it yields extremely poor results. A drawback of alkaline etching is the existence of steps between grains, that can interrupt the subsequent screen-printing of metal contacts.

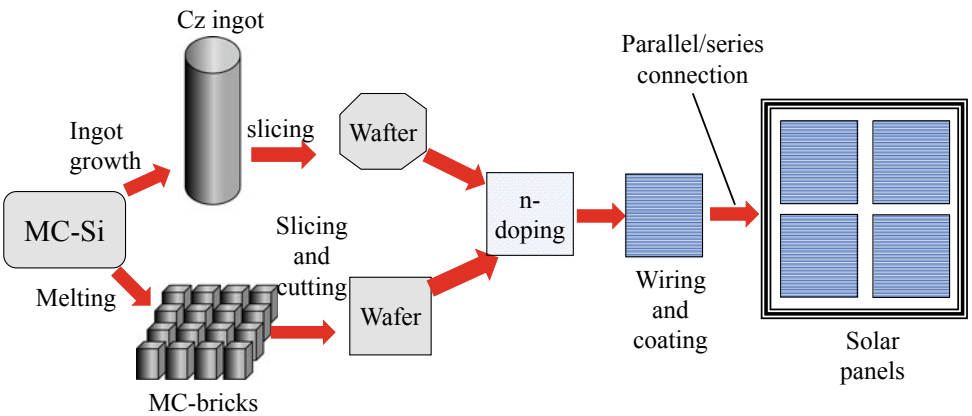


Fig. 14 General sequence of silicon wafer-to-module processing

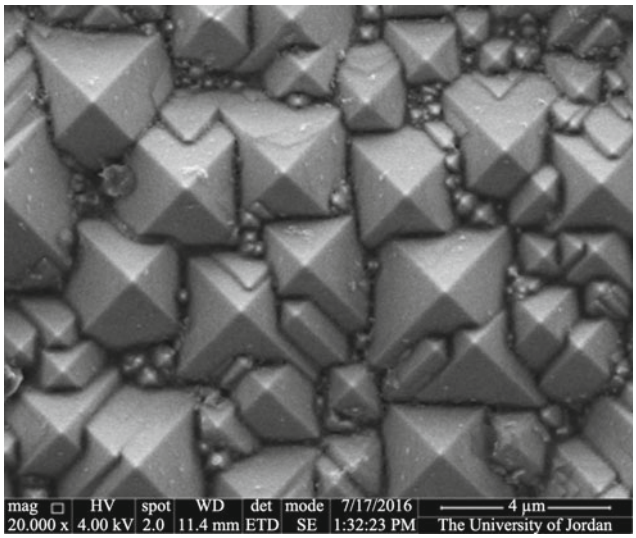


Fig. 15 Using KOH to texturize a silicon wafer results in random-sized pyramids (https://scialert.net/fulltext/?doi=jas.2017.374.383)

An acid can also be used, which results in an inverted pyramid structure that is preferred to ones resulting from alkaline texturing. But these pyramids require subsequent photolithographic patterning, that is a major disadvantage due to the compatibility complications with industry and process automation.

Nitric and hydrofluoric acids along with suitable additives present a more convenient method of etching, known as isotropic etching, which gives results similar to the one shown in Fig. 16.

This treatment results in uniformly distributed etch pits of 1–10 µm diameter. This can cause homogeneous reflectance over the surface of the wafer and the lack of steps between grains. The acidic chemical attack produces a porous silicon layer before the etching process comes to halt. This is typically done in an alkaline solution. The acidic texturing results in a gain of short-circuit current of the order of 5–7%, but the acidic bath suffers from quick depletion of solution and exothermic effects, on top of environmental and health issues that accompany acid handling. This calls for a process predesign, involving automated wet benches that are able to manage the temperature of the etching solution and an automated process to refill the chemicals.

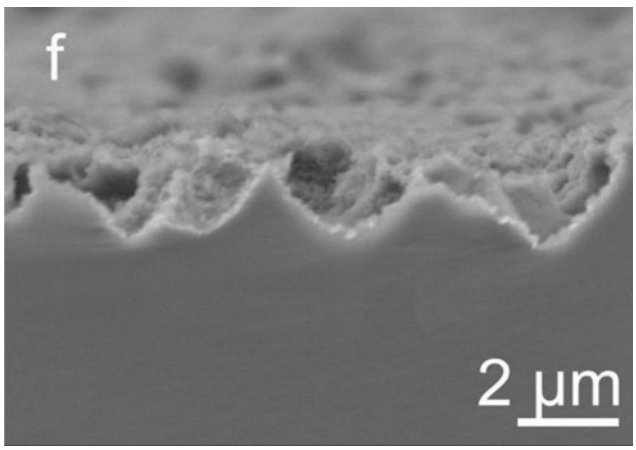


Fig. 16 Inverted pyramids produced by Hydrofluoric (HF) acidic etching of silicon (Gao et al. 2018)

6.3.2 Plasma Texturing

Reactive ion etching (RIE) is a dry isotropic etching process that results in dense, porous and inclined and dimensionally limited pits usually less than 1 µm. The process is a texturization of silicon in a halogen plasma. The incorporation of these pits increases short-circuit current in the range of 10% compared with anisotropic textures as shown in Fig. 17 (Addonizio et al. 2019).

In order to create better regular features, RIE can be combined with a masking layer. However, the chemicals have the potential to elevate the severity global warming which is a disadvantage for industrial commercialization. Another disadvantage is the low process output data.

6.3.3 Mechanical Texturing

This process uses abrasive claws to mechanically introduce V-grooves about 50 µm deep on the Si wafers. The process is conducted through a traditional dicing saw, with a subsequent base etching to polish the surface and rid it of residue materials and saw damage. The average reflectivity is in the variety of 6–8%; in addition, the efficiency gains of 5% (relative) are obtained following encapsulation. Metal fingers (contacts) are screen printed in line with the etched grooves, on the unaltered regions.

Table 2 compares reflectivity gains at different wafer processing stages using texturing techniques discussed above (Macdonald et al. 2004).

6.4 Phosphorus Diffusion

Phosphorous diffusion refers to adding the *n*-type layer to the conventionally p-doped starting wafer. Solid-state diffusion can only take place at high temperature and a controlled atmosphere of the intended dopant. Two processes are available: either a batch process in a quartz furnace or a continuous process in a belt furnace.

6.4.1 Quartz Furnace

A quartz furnace with wafers placed in quartz boats offers material compatibility and thus low contamination that can result due to handling in noncompatible or metallic boats or furnace. An atmosphere rich with phosphorus can be

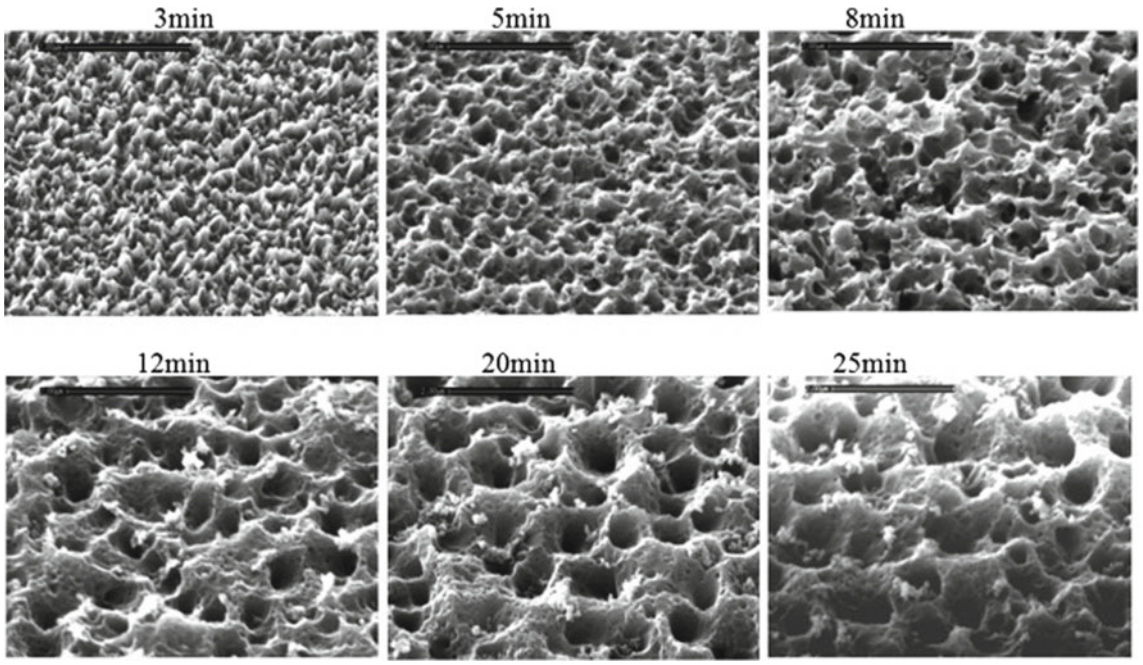
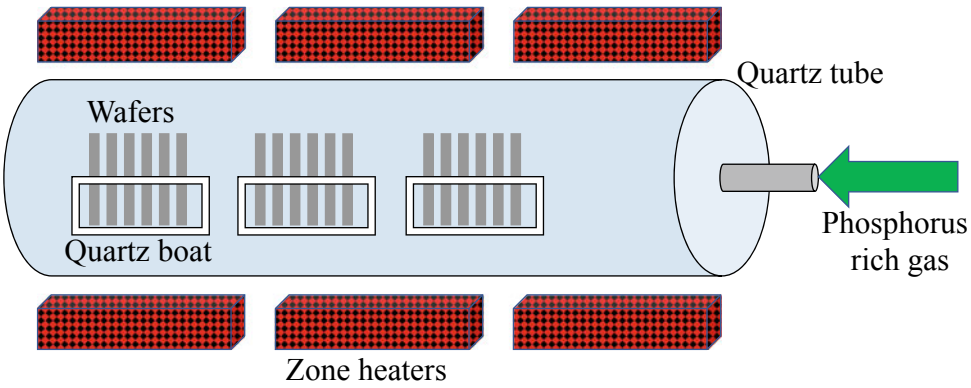


Fig. 17 Pyramids used by plasma (RIE) at different processing times (Addonizio et al. 2019) (with permission 5364110390101)

Table 2 Reflectivity of MS-Si with different texturing techniques (Macdonald et al. 2004) (with permission 5364160034473)

Reflectivity (%)	Alkaline texturing	Acidic texturing	Plasma texturing
Bare	34.4	27.6	11.0
With SiN ARC	9.0	8.0	3.9
With ARC and encapsulation	12.9	9.2	7.6

Fig. 18 Quartz tube furnace



supplied by bubbling N_2 through liquid $POCl_3$ (which has to be handled with care) before injecting it into the furnace, as shown in Fig. 18.

Tubes are generally exposed and function at atmospheric pressure, but operating at low pressures improves the uniformity and throughput. The furnace temperature ramping and heat treatment protocol are easily adjusted and controlled. Durations between 20 and 30 min at temperatures above 800ºC are typical to the treatment. Advantages of quartz furnace include the sovereignty of Si atoms with low to almost no foreign metallic impurities high throughput is achievable since simultaneous substrates can be used in a single batch. Commercial furnaces can consist of stacks of four tubes to further enhance process throughput.

6.4.2 Belt Furnace

This furnace is a continuous process type, with phosphorus source supplied to one or both wafer faces. The temperature

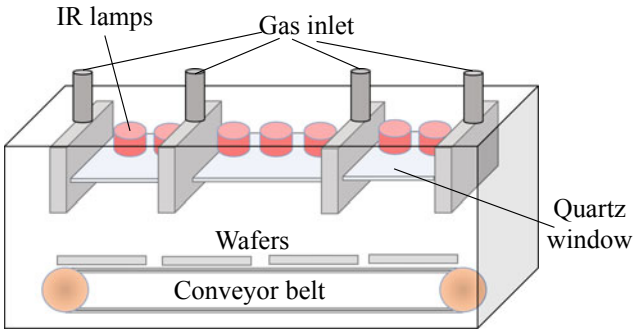


Fig. 19 Belt furnace

control (fast heat ramp up or down) can be achieved through infrared (IR) heated zones. Dopant sources can deposit using many methods such as screen printing, spinning-on, spraying-on, by CVD or by vapourization. The temperature cycle experienced by the wafer will be an exact replica of the furnace heater temperature profile along the conveyer belt, with the time frame control via speed controls. A depiction of a belt furnace is shown in Fig. 19.

Some disadvantages of the belt furnace are ambient air intrusion as well as the belt material being a potential source of metallic impurities. The main obvious advantage of such a process is the amenable automation and the capability to apply various temperature profiles for rapid heating and cooling.

7 Cell Optical Enhancements

After a desired single-faced phosphorous diffusion, a parasitic junction formed on the surface and also at the edges which causes a multitude of problems (leading to low shunt resistance) and should be removed. This layer of amorphous phosphosilicate glass usually undergoes an etching process in dilute HF as it will delay the succeeding processing steps.

Usually, titania (TiO_2) is employed to create the anti-reflection coat as it possesses an optimum refractive index for encapsulated cells. This can be done via many processes, such as atmospheric pressure chemical vapour deposition (APCVD), spin coating or screen printing. Nowadays, hydrogenated silicon nitride (SiN:H) films are the most advantageous choice, as they associate anti-reflection with bulk and surface passivation, it also is a distant cousin of silicon, which enhances material and precursor compatibility. SiN:H can be deposited using chemical deposition CVD (fast, high-quality solid material) and plasma-enhanced CVD (PECVD), which requires low-pressure and low temperature (<500 °C) processing.

7.1 Chemical Vapour Deposition (CVD)

Chemical vapour deposition process is used to produce good quality solid substrates. The substrate is placed in the path of one or more volatile precursors, which react and decompose on the substrate surface as shown in Fig. 20.

In general, CVD is a reliable process, but there could be a lot of wasted materials as the mixed gaseous precursors rely on process parameters (flow rate, substrate temperature, concentration, etc.) to achieve the required deposition on the substrate. This is depicted in Fig. 21a as the conventional CVD process proceeds with limited control over the rate and quantity of which the gas molecules are interacting with the substrates. In Fig. 21b, a CVD-enhancing process such as plasma, radio waves or thermal wire has been added to impose lateral forces on the molecules, hence forcing them to deposit on the surface.

The plasma-enhanced chemical vapour deposition (PECVD) is favoured to other low-pressure CVD as it occurs at low temperatures ($T < 500$ °C). The process induces hydrogenation, that is very beneficial for silicon.

For the ARC layer deposition, amorphous silicon nitride films are created by PECVD. A successive thermal step is required to activate hydrogenation; industrially, the previously mentioned firing step is sufficient. The process is depicted in Fig. 22. One issue arises which is the elaborate

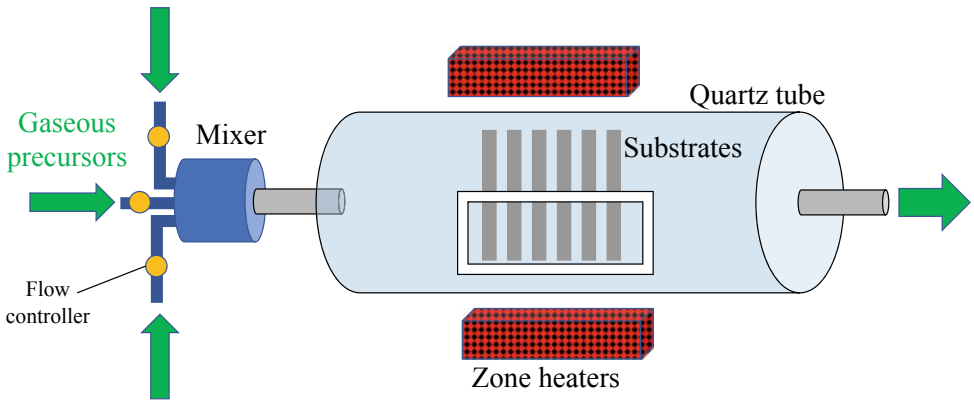


Fig. 20 A depiction of the CVD process

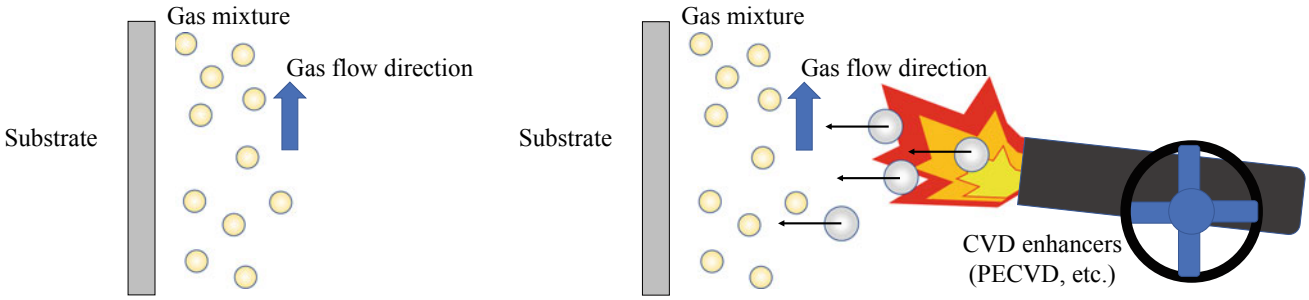


Fig. 21 **a** CVD and **b** enhanced CVD processes

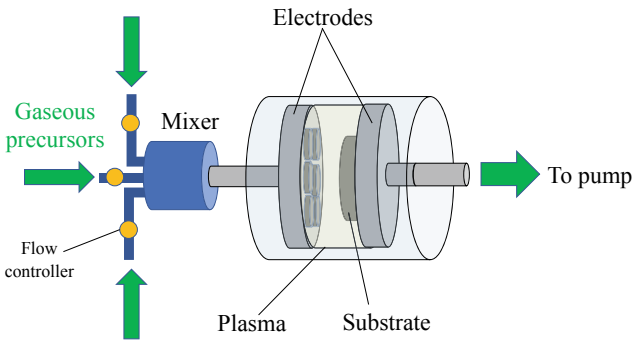


Fig. 22 PECVD process

control over process parameters, such as applied voltage across electrodes, as well as the distance between them. These parameters affect the thickness and quality of the deposited films.

The three important surface properties (ARC, bulk and surface passivation) are interconnected and cannot be altered independently; hence, optimization of all the processing parameters such as temperature, power and frequency of plasma excitation, and gas flow rate is a must. To decouple the plasma from the CVD process, two operational routes are available: (Sect. 7.2) direct PECVD (high frequency: 13.56 MHz, low frequency: 10–599 kHz) and (Sect. 7.3) Remote PECVD.

7.2 Direct PECVD

In this method, the wafers are situated in the plasma caused by the excitation of the processing gases by the electromagnetic field. Hence, the bulk is efficiently passivated, but surface passivation is not achieved properly as a result of the severe effects of long exposure of the wafers to the aggressive plasma. Furthermore, the surface passivation worsens as the wafers are exposed to UV light. The process is shown in Fig. 23 (Aberle 2001).

7.3 Remote PECVD

Wafers are situated away from where the plasma forms as shown in Fig. 24. The setup has an advantage similar to batch-type direct PECVD as wafers are fed continuously and there is no direct contact between the substrates and the plasma; thus, surface damage is avoided but surface passivation is enhanced, whereas bulk passivation reduced.

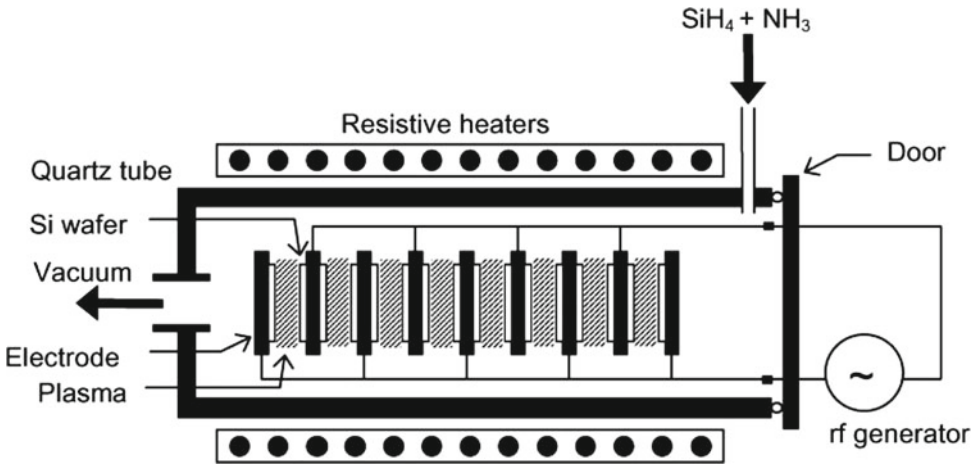


Fig. 23 Direct-plasma batch reactor for the simultaneous PECVD deposition of SiN onto many Si wafers (Aberle 2001) (with permission 5364110735212)

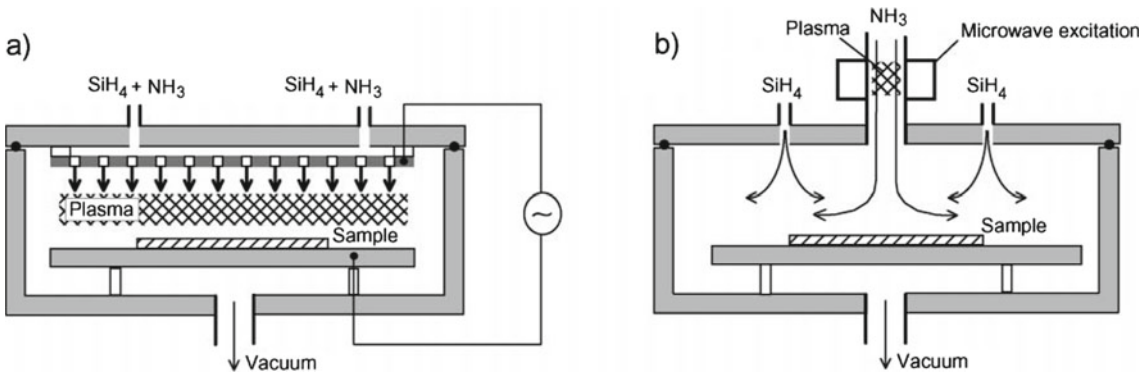


Fig. 24 Deposition of SiN in **a** a direct-plasma reactor and **b** a remote-plasma reactor using microwave excitation (Aberle 2001) (with permission 5364110735212)

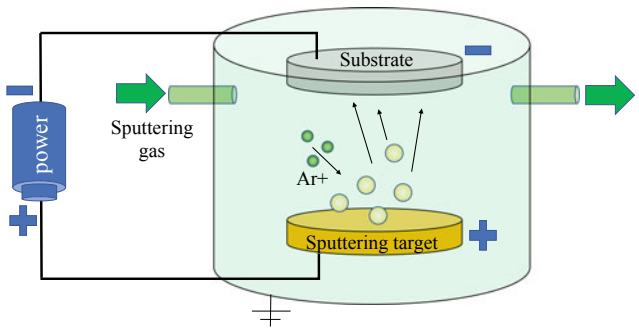


Fig. 25 Depiction of the sputtering process

7.4 Sputtering Techniques

Sputtering process takes place when atoms are ejected from a solid target material due to bombardment of the target by energetic particles. If vacuum is generated and maintained, these atoms flow from the positive (high voltage) target to the negative (low voltage) desired substrate and land on its surface. The reader should pay attention that the "target" refers to the source material that will be deposited on the substrate, which is not called a target although it appears to be one. The process is shown in Fig. 25.

8 Front Contact Print and Dry

The process of adding contact fingers to the solar cell is a delicate task. The resulting metallization allows effective electron harvesting but should not impede reception of solar radiation. There are general requirements for the front metallization material, and they include:

1. low electric resistance (related to contacts).
2. low bulk resistivity.
3. suitable contact dimensions (width and heigh aspect ratio).
4. surface stickiness and adhesion.
5. compatibility with subsequent encapsulating or ARC materials.
6. solderability.

The ideal contact metal is selected based on its resistivity, price and availability, making silver a very valuable option. Copper possesses similar characteristics as silver, but it does not qualify for conventional processes such as screen printing. This is mainly due to the diffusivity of copper during heat treatments which will contaminate the silicon wafer. In addition, screen printing is the de facto process of adding front contacts on silicon wafers.

8.1 Screen Printing

Screen printing does not live up to the advantages presented by vacuum physical evaporation for first three requirements mentioned above. Screen printing is utilized to adhere a paste composing of silver powder to the front face of the wafer in a mesh pattern that is used to deposit the fingers and associated busbars. The presence of solvents in the paste gives it a viscous liquid nature; the solvents can be easily evaporated in a furnace at around 250 °C and the dried paste is ready for further processing.

Automatic screen printers are available and allow nonstop operation with high throughput. The automatic screen printers can hold wafers from packs, shelf-like or a belt line. Those wafers are then situated with adequate accuracy under the screen, and once printed, they are delivered to the belt line. A sample silk screen showing contact finger pattern is shown in Fig. 26.

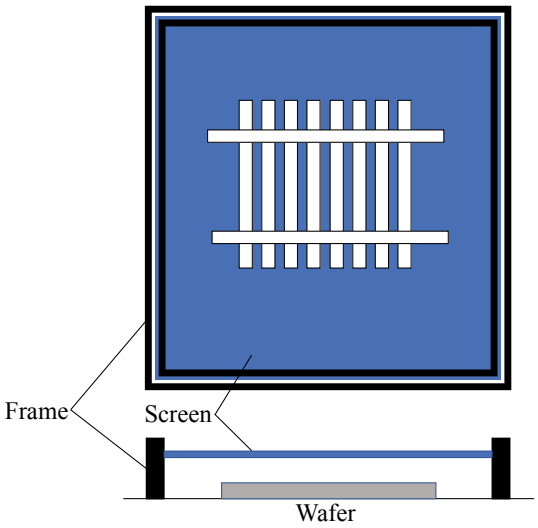


Fig. 26 Silk screen with contact finger pattern pre-inscribed

8.1.1 Screen Printing Process

The front contact of a solar cell requires a fine and thick layer. In order to achieve that through screen printing, wires must be quite thin and compact. Moreover, the reticule's opening has to be sufficiently greater in diameter than the largest grain available in the paste. A schematic of the process is shown in Fig. 27. At the start of the process, the screen and wafer are separated by a distance referred to as the snap-off. Subsequent to dispensing the paste, pressure is applied on the squeegee that is manufactured from metal or rubber. Once pressure is applied, the screen and wafer are in contact. The squeegee is then swept across the screen spreading the paste during the process. This continues until an opening is present where the paste would fill it and adheres to the wafer. The paste will stay in the opening even after the squeegee passes and the screen is retuned.

8.1.2 Paste Properties

The paste carries active material to wafer surface. There are some general components for the paste as follows:

1. Organic solvents: carrying the active materials and providing required paste viscosity.
2. Binders: usually organic, allow agglomeration of active material particle.
3. Conducting material: 10 μm fine silver or aluminium powder (or both). This material is the contact material and makes up around 80% of the paste weight.
4. Glass frit: scratches the surface for more intimate contact laying. Make up to 10% of the weight and consists of powder of metal oxides with low melting point and high reactivity.

8.1.3 Process Parameters

The amount of paste determines the thickness of the screen material, emulsion, open area of fabric and printed line width. For instance, it is essential for the paste to have a low viscosity to fill all the volume permitted by the fabric and emulsion without any voids. Nevertheless, the fluid must also not seep off the surface when the printing process is completed. The snap-off distance, pressure applied on the screen and the velocity of the squeegee are the vital factors that control the printing process.

9 Back Surface Field Deposition

The back-surface field (BSF) layer can be simply achieved by doping the back region of a p-type wafer with the use of screen printing an aluminium paste. The BSF layer is formed as a result of the dissolvement and the epitaxial recrystallization of silicon in aluminium during cooling subsequent to

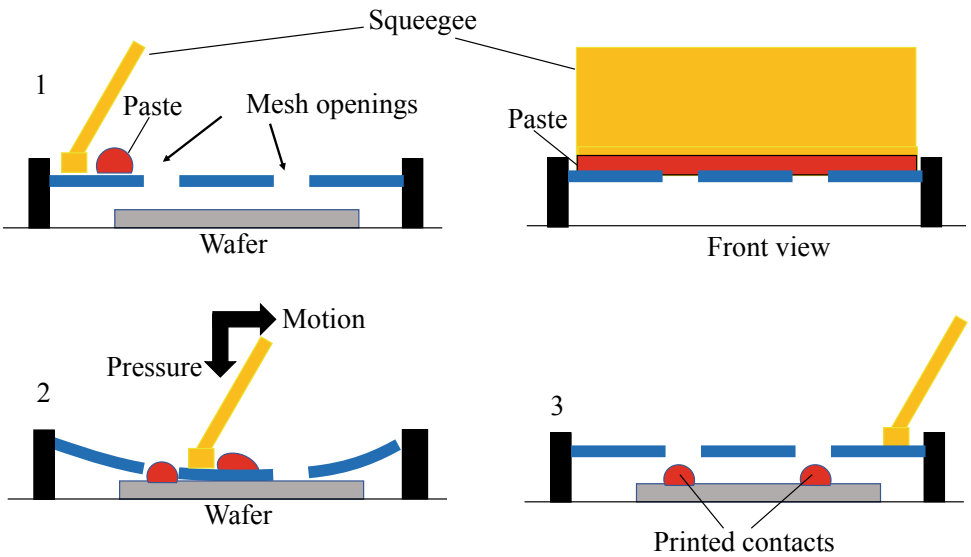


Fig. 27 Steps of the screen-printing process

the firing step. However, soldering onto Al contacts is impossible, so it is recommended to use silver and aluminium paste to print busbars.

10 Drying and Co-Firing

The series resistance is decreased by obtaining a good conductor. This is achieved by burning off the organic components of the paste, and by sintering the metallic grains together. The metallic grains ought to form an indistinguishable interface with the preceding silicon layer. The back paste must penetrate the BSF to reach the base during firing. The thermal profiles and composition of the pastes must go under a well-controlled optimization process to adhere to the requirements and standards.

11 Testing and Sorting

Efficiency (I-V) tests are conducted under simulated STC conditions using a solar simulator with certified standard output of irradiance intensity and spectrum, with the aid of a temperature control mechanism, where a flash lamp is capable of providing the required illumination as shown in Fig. 29. The test machine or sun simulator exposes modules to a burst of bright (1000 W/m^2) light with a duration in microseconds from a xenon lamp.

Devices are categorized according to their performance, and devices that do not fall into any level of efficiency or performance bin are disposed of.

The manufacturer typically arranges the cells in different classes depending on the current achieved at a constant voltage close to the maximum power point. Subsequently, the modulus will be manufactured to match the cells of the same class in order to eliminate mismatch losses. Solar cells within a module must have a maximum of a 5% current variation for a single bin (category), to ensure a stable operation of the assembled modules.

12 Module Making

The final step after individual cell testing is their assembly in a module. The cells are electrically connected in series to increase the output voltage, relative to sole solar cells. The cells are encapsulated and furnished with various ancillary and performance-enhancing components such as bypass diodes, connections, a junction box, cabling, front glass and finally glass or a polymer (Tedlar in particular) on the rear surface of the module. The utilization of these components offers physical sturdiness for the module and protection of contacts from weather elements (e.g. humidity, dust and elevated temperature) that cause losses and deteriorate the performance over time (Ayang et al. 2018).

Silicon solar cells are electrically connected together by a ribbon, which is a thin copper tape deposited with a tin alloy. The cells are typically immersed in a clear encapsulant that serves as a binder between the different layers of the PV panel. Ethylene–vinyl acetate (EVA) is most commonly used for encapsulation purposes due to its manufacturability and electric insulation. It is transparent and supplied in rolls that are cut into the required shapes and sizes. The deposition takes place via a vacuum thermal treatment, transforming the polymer layers into a translucent gel that coalesces on the cells by heating it at temperatures up to 150 °C (Şahin and Okumuş 2016; Ecoprogetti 2014). The EVA is placed on a frame of aluminium or stainless steel and protected with clear glass on the front side to finalize the lamination process (Şahin and Okumuş 2016).

The frame is the final piece that is installed in a PV module assembly. It is typically made of anodized aluminium and serves to guarantee the robustness of individual panels as well as the functional and reliable linkage to other photovoltaic modules.

A line of sealant is deposited around the panel walls and along the frame to isolate the side of the panels from rain and dust accumulation. Silicon is the most commonly employed material for this intent, though a specific sealing tape is occasionally utilized. A fully assembled PV module is shown in Fig. 28.

There are also frameless modules and special plastic solutions provided for unique applications. These solutions often include the deployment of rear-side glued supports and modules with glass-glass technology for transparent rooftop installations (Ecoprogetti 2014; Swart 2018).

As explained previously, the current generated through the photovoltaic reactions is collected by the metallic top contacts that enable electron flow and collection. Busbars are directly connected to outer leads. Whereas fingers in narrower metallization zones collect current for transfer to the busbars (https://www.pveducation.org/pvcdrom/top-contact-design).

A junction box is placed on the back of the PV module and provides lead wires as an outer connection to provide connection to other PV modules, charge controllers, batteries or inverters. It covers the shadow protection diodes, to prevent the generation of hotspots due to mismatched individual cells' output currents, as well as the cables that incorporate the panels in the field (Ecoprogetti 2014).

Bypass diodes are connected in parallel within the PV module, as opposed to blocking diodes that are connected in series (https://www.sunwize.com/tech-notes/pv-module-bypass-diodes-what-are-they-and-what-do-they-do/), and deliver an alternate current during shading or deficiency of

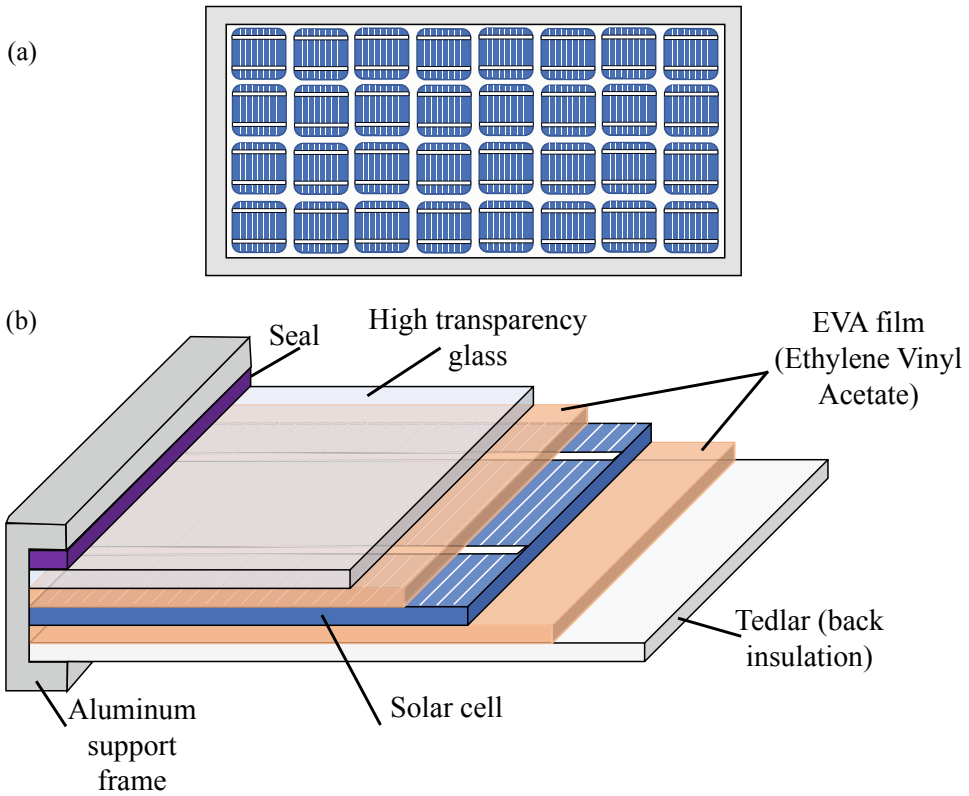


Fig. 28 Fully Assembled PV Module **a** Top view, **b** cross-section view

Fig. 29 Flash test of assembled PV panel (Findlay 2022)

cell or panel. In general, diodes are devices that allow the flow of current in a specific direction. The installation of the diodes can either be in the module junction box or incorporated directly into the module.

The assembled modules, similar to their unit cells, are exposed to a flash test to obtain their I-V characteristics which indicate their overall performance as seen in Fig. 29. Modules are also subjected to light-soaking (exposition to illumination for a long period of time) to verify their resistance to light-induced deterioration.

References

Aberle AG (2001) Overview on SiN surface passivation of crystalline silicon solar cells. Sol Energy Mater Sol Cells 65(1):239–248. https://doi.org/10.1016/S0927-0248(00)00099-4

Addonizio ML, Antonaia A, Fusco L (2019) Plasma etched c-Si wafer with proper pyramid-like nanostructures for photovoltaic applications. Appl Surf Sci 467–468:143–150. https://doi.org/10.1016/j.apsusc.2018.10.078

Al-Husseini AM, Lahlouh B (2017) Silicon pyramid structure as a reflectivity reduction mechanism. J Appl Sci 17(8):374–383. https://doi.org/10.3923/jas.2017.374.383

Anti-Reflective Coating for Eyeglasses—Worth The Money? https://www.allaboutvision.com/lenses/anti-reflective.htm. Accessed 8 Aug 2022

Ayang A, Wamkeue R, Ouhrouche M, Saad M (2018) Faults diagnosis and monitoring of a single diode photovoltaic module based on estimated parameters. In: 2018 IEEE electrical power and energy conference, EPEC 2018.https://doi.org/10.1109/EPEC.2018.8598308

Bai Q, Yang H, Cheng X, Wang H (2020) Recombination parameters of the diffusion region and depletion region for crystalline silicon solar cells under different injection levels. Appl Sci 10(14):4887. https://doi.org/10.3390/app10144887

Beiser V (2018) The ultra-pure, super-secret sand that makes your phone possible. In: Wired magazine

Ecoprogetti (2014) What is the raw material that composes a photovoltaic module? https://ecoprogetti.com/the-structure-of-photovoltaic-module/

Findlay S (2022) Flash testing high capacity solar. https://www.winaico.com.au/blog/flash-testing-high-capacity-solar

Gao K et al (2018) Fabrication of black silicon by Ni assisted chemical etching. Mater Res Express 5(1). https://doi.org/10.1088/2053-1591/aaa1fb

Global Market Share by PV Technology from 1990 to 2013. https://commons.wikimedia.org/wiki/File:Global_Market_Share_by_PV_Technology_from_1990_to_2013.svg. Accessed 9 Aug 2022

Green MA, Zhao J, Wang A, Wenham SR (2001) Progress and outlook for high-efficiency crystalline silicon solar cells. Sol Energy Mater Sol Cells 65(1):9–16. https://doi.org/10.1016/S0927-0248(00)00072-6

Honsberg C, Bowden S, Top contact design. https://www.pveducation.org/pvcdrom/top-contact-design

Macdonald DH et al (2004) Texturing industrial multicrystalline silicon solar cells. Sol Energy 76(1):277–283. https://doi.org/10.1016/j.solener.2003.08.019

Magsi K (2014) Bio-inspired photon absorption and energy transfer for next generation photovoltaic devices. Stony Brook University

Miles RW, Zoppi G, Forbes I (2007) Inorganic photovoltaic cells. Mater Today 10(11):20–27. https://doi.org/10.1016/S1369-7021(07)70275-4

Şahin ME, Okumuş HI (2016) Physical structure, electrical design, mathematical modeling and simulation of solar cells and modules. Turk J Electromech Energy 10680

Silicon Pyramid Structure as a Reflectivity Reduction Mechanism. https://scialert.net/fulltext/?doi=jas.2017.374.383. Accessed 8 Aug 2022

Sunwize, PV module bypass diodes—what are they and what do they do?" https://www.sunwize.com/tech-notes/pv-module-bypass-diodes-what-are-they-and-what-do-they-do/

Swart AJ (2018) Analyzing the performance of identical PV modules in a semi-arid region over a 2-year period. In: International conference on multidisciplinary research, pp 94–108

UAE-based Mulk Holdings International pens JV agreement to enter US market (2021) Arabian Business. https://www.arabianbusiness.com/industries/construction/467119-uae-based-mulk-holdings-international-inks-deal-with-park-international-investments-silver-heights-real-estate