# Silicon Feedstock and Ultra-Refinement

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**Abstract**

This chapter focuses on obtaining and refining silicon under the stringent requirements of the photovoltaic manufacturing industry. Starting with the carbothermal process; a well-established manufacturing process of silicon, other processes such as chemical vapor deposition for further silicon refinement are also introduced and their history discussed. Doping processes are also important so these are also discussed in detail.

## 1 The Carbothermal Refinement Process

Silicon is one of the most abundant elements in the Earth's crust, as it exists in the silica or the silicon oxide ($SiO_2$) form. Silicon is an essential element in many industries, mainly the microprocessor and solar photovoltaic cells and modules. Pure silicon has to be extracted (reduced) from its oxide form then ultra-refined in order to be useful in aforementioned industries. In addition to the production of solar grade silicon, metallurgical grade silicon is obtained by acquiring the hyper-pure (more than 99.9999999% pure) silicon form. The hyper-pure form is obtained by devising processing technologies for removing oxygen atoms that are connected to the silicon grain. This allows arriving at what is known as "metallic silicon" that is around 96% pure. Further refinement of the silicon allows doping it with selected elements to control its electric and electronic behavior. This allows for the production of the semiconductor grade silicon and other devices that have become indispensable for everyday life. Silicon refinement for acquiring metallurgical grade silicon is carried out by a carbothermic process. This process involves placing the $SiO_2$ material in a compatible quartz crucible and subjecting it to energy to break the Si/O bonds. Supplying energy in the form of heat helps in breaking the Si-$O_2$ bonds, but the amount of heat has to be in the range of 159.8 J/g (melting point of silica), which is substantial and challenging to provide. Thus, an innovative method similar to the one used to extract aluminum from bauxite (aluminum oxide ore) that allows for breaking the Si/O bond is utilized. As will be explained later, the carbothermal process breaks the $SiO_2$ bonds, and hence a reduction reaction takes place, whereas the carbon atoms replace silicon in bonding with the $O_2$ atoms resulting in elemental Si as shown in Fig. 1. A crucible containing the $SiO_2$ is placed within an arc furnace, with retractable graphite electrodes acting as both an electricity conductor and also as a source of pure carbon for the reaction. Once the electric circuit is closed, the graphite electrodes (positive terminal) are lowered enough toward the raw materials of silicon oxide and carbon, and an arc is generated. This arc provides the energy as well as the carbon required for the reaction to proceed. This is the reason behind the name "arc furnace". The furnace is also utilized to initially heat the carbon (around 1500–2000 ºC), then to supply the required amount of energy through the electric arc to break the $SiO_2$ bonds.

The following chemical reaction represents the carbothermal process:

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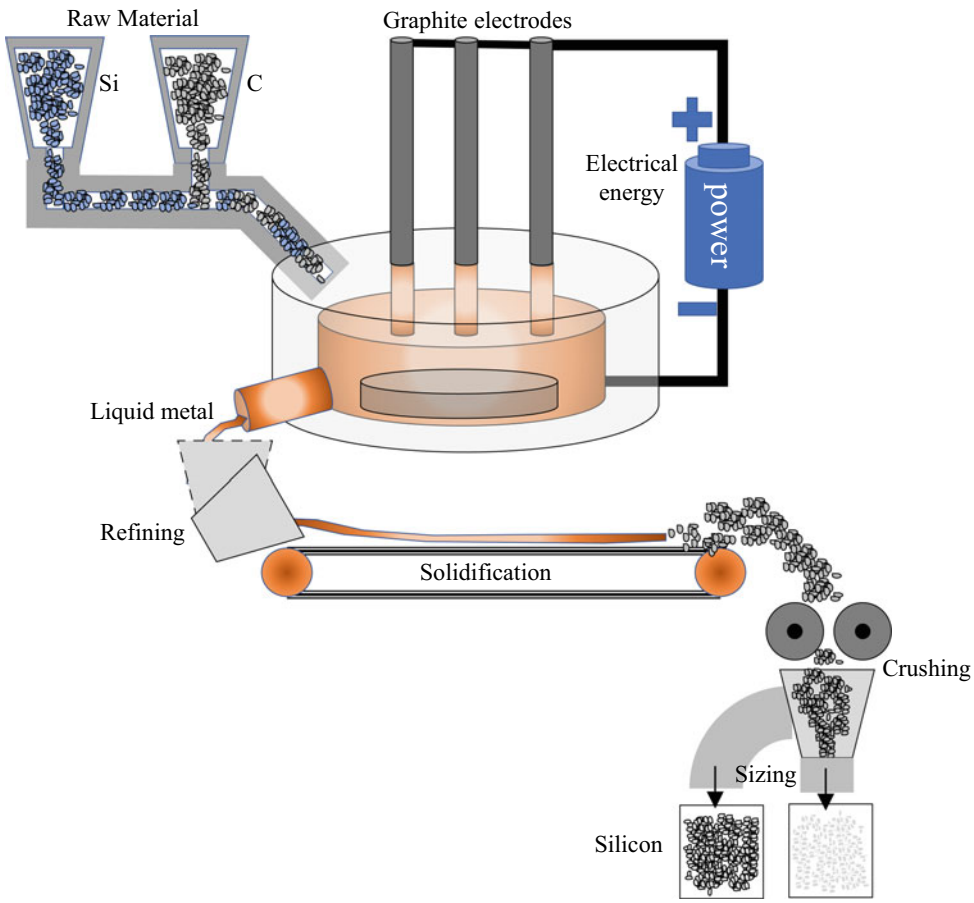



**Fig. 1** Carbothermic process of metallurgical silicon refinement

$$SiO_2 + C \xrightarrow{\text{energy}} Si + CO_2 + \text{heat} \quad (1)$$

It is evident that elemental silicon is obtained after breaking the $SiO_2$ bond, carbon dioxide results as well as heat. This heat can and should be recovered by attaching a regenerative cycle to the setup shown in Figure 1. Silicon issues from the crucible in liquid form, however upon pouring and crushing it, chunks of metallic Si are obtained with a purity level of $\sim$96%.

## 2 Silicon Ultra-Refinement

Further refinement to the silicon leads to the production of solar grade silicon (SOG-Si). As a result, the level of purity of the Si should increase from 96% to 99.99999% (5–7 nines succeeding the decimal point). To achieve such purity, specialized processes under pristine environmental control have to be used. This strict environmental control is applied to personnel as well, and thus, it is quite common to see people in full hazmat suits handling silicon and making it ultra-pure.

In general, there are two routes for carrying out the silicon purification and ultra-refinement: (i) chemical metallurgical purification of trichlorosilane in Siemens reactor or silane in fluidized bed reactor and (ii) electrochemical refinement, involving the dissolution of quartz in fluoride and three-layer electro-refining Si. In both cases, chunks of metallic silicon are digested chemically into a gas then deposited on a substrate that is made of a single crystal silicon material called the "seed crystal". This approach benefits from the strong cohesive forces between similar materials. The silicon processing is shown in Fig. 2.

The chemical route utilizes trichlorosilane ($SiHCl_3$) gas to carry the silicon material and decomposes it (deposits it) on the seed crystal. The gas results from the chemical reaction between the silicon chunks and hydrochloric acid in the presence of hydrogen. Silane gas ($SiH_4$) can also be used, but it is less reactive than when chlorine is added from the reaction with HCl. Silane, dichlorosilane, or trichlorosilane are then used to deposit silicon in either the Siemens process or the fluidized bed reactor. These two processes are well developed and have historically been used to produce ultrapure silicon mainly for microchips and microprocessors for the PC industry. The processes fall under the umbrella of chemical vapor deposition (CVD), a process class that is essential for solar cell making. It is a chemical process that produces high-quality and high-performance solid materials.

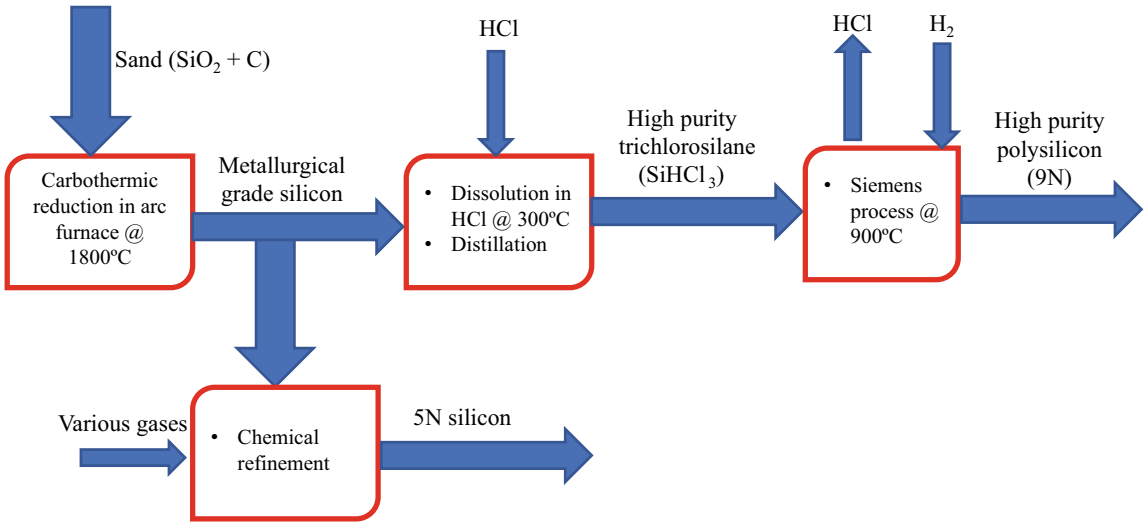



**Fig. 2** From sand to high-purity silicon

The inputs of the CVD process are gasses, including carrier gasses that will carry the silicon to the substrates. The silicon chunks will first be dissolved with hydrochloric acid (HCl) and carried by hydrogen to the heated substrates. The substrates are added and heated into the tubes that are made up of quartz as shown in Fig. 3 Quartz is a very hard material that is at the same time transparent and heat resistant; hence, it is recommended to utilize it as the designated material of the tube.

Hydrochloric acid dissolves the silicon, which allows the formation of either dichlorosilane ($SiH_2Cl_2$) or trichlorosilane ($SiHCl_3$) gases. Hydrogen carries the $SiHCl_3$ gas through the tube to the substrates. The gasses then come into contact with the heated substrates that are placed within the tube, and the gasses decompose and cover the substrates with silicon. Afterward, a stream of hydrogen is inserted through the tube in order to bond with the chloride. This in return produces HCl gas, which can be collected, recycled, and reused. In general, the CVD process can incorporate any number of gasses which pass through the tube, and the gasses interact with each other and with the silicon. The silicon is then transported by a carrier gas to the substrates. The substrates are originally made of pure silicon that act as the seed particle which initiates the process of acquiring refined silicon. The carried silicon and gasses are then decomposed onto the silicon substrates. Extra hydrogen flows through the tube to react with chloride and leave the pure silicon on the substrates. The interaction between the hydrogen and the chloride results in the production of HCl gas. The seed particle, made up of pure silicon, can either be manufactured by hand or through a special process.

On an environmental consciousness note, the amount of $CO_2$ produced and energy utilized in the arc furnace to break the $SiO_2$ bond is high. Moreover, the production of highly refined silicon does not only require large amounts of energy, but also excessive amounts of HCl acid. Thus, every 4 tons of acid produces 1 ton of silicon. Hence, it is evident that the extensive usage of water, energy, and acids hinders the production of solar cells. The real problem lies in the difference between the amount of energy utilized into

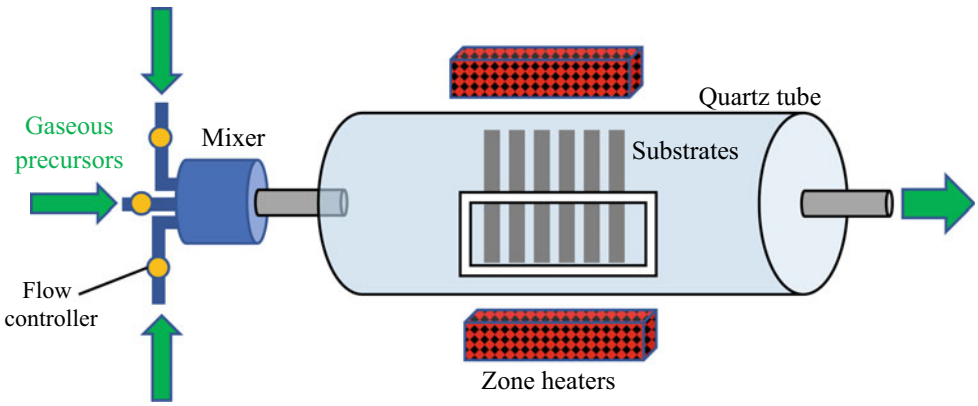



**Fig. 3** CVD setup for obtaining highly pure solar grade and semiconductor grade silicon

building the solar cells and the energy produced by the cells. It was found that the amount of energy produced by the module over its lifetime of approximately 25 years will not cover the amount of energy that went into building them. For this reason, it is necessary to search for more efficient ways, that are both environmentally friendly and not energy intensive, to produce PV modules. The current processes to produce PV modules are energy intensive, wasteful, produce excessive amounts of $CO_2$ emissions and involve the utilization of chemicals and acids.

## 2.1 Siemens Process

One of the oldest techniques for silicon making, it is basically a CVD technique. It starts with metallurgical silicon with 96% purity as input material from the arc furnace and ends with ultrapure silicon. By injecting hydrochloric (HCl) acid to dissolve the silicon, trichlorosilane ($SiHCl_3$) gas is generated.

Throughout this process, seed silicon rods made up of highly pure silicon are added as substrates. Hydrogen is added to interact with the chloride in the $SiHCl_3$ gas and isolate the silicon, resulting in the formation of HCl gas. Silicon accumulates on top of the silicon seed rods. Once the process is over, the deposited Si is removed and collected. Figure 4 demonstrates the Siemens process to purify silicon. The following chemical reactions represent the process of first dissolving silicon with HCl, then acquiring the $SiHCl_3$ gas and excess hydrogen. The chemical reaction also shows that the $SiHCl_3$ and hydrogen gasses produce pure silicon and excess HCl gas.

$$Si + 3HCl \xrightarrow{\text{yields}} SiHCl_3 + H_2 \quad (2)$$

$$SiHCl_3 + H_2 \xrightarrow{\text{yields}} Si + 3HCl \quad (3)$$

## 2.2 Fluidized Bed Reactor Process

In addition to the Siemens process, chemical metallurgical silicon refinement can also be carried out by the fluidized bed reactor (FBR). The FBR is an old process that does not utilize large quantities of hydrogen or HCl gasses to react with silane gas that is injected from the bottom of the reactor. The FBR process was found to compensate for the drawbacks of the Siemens process. The Siemens process is a non-continuous process that disturbs the continuity of the process to collect and obtain pure silicon. In contrast, the FBR process is a continuous process that does not need to stop to collect the produced silicon. To obtain pure silicon, silane (SiH4) gas with silicon particles and hydrogen can be readily injected through the reactor, as shown in Fig. 5.

Unlike the Siemens process, the FBR process does not initially require dissolving the silicon with HCl to obtain the $SiHCl_3$ gas, instead silane gas with silicon particles can be directly inserted into the reactor. As soon as the gas enters, it decomposes on tiny little seeds, made of pure silicon. Once enough silicon is collected on the seeds, bigger granules form and sink to the bottom of the reactor, where they are regularly removed from the process. Consequently, the silicon is obtained without the need to discontinue the process at any occurrence. Compared to the conventional rod reactor (Siemens process), the FBR consumes as little as 10% of the electricity for a matched output. The reduction in the electricity utilization is attributed to the heat loss bypass due to the heated gas/cold silicon seed surface interface reaction. Moreover, the FBR process suits the rapidly expanding photovoltaic industry by producing less-expensive polysilicon.

# 3 Monocrystalline Silicon Production

The Siemens and the FBR processes assist in acquiring high-purity chunks of silicon grains with irregular shapes. These shapes, however, are not suitable to be readily utilized

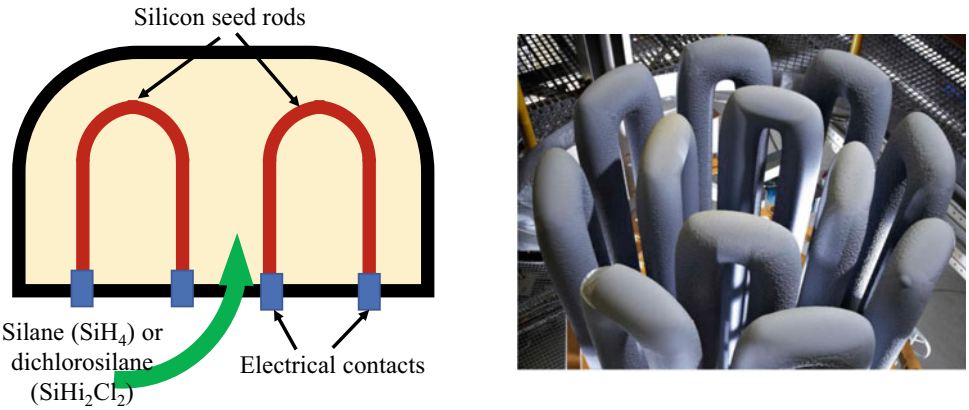



**Fig. 4** Siemens process for polysilicon purification and refinement **a** the Siemens chamber or bell and **b** polysilicon rods ready to be broken into silicon chunks (Polysilicon Production 2023)

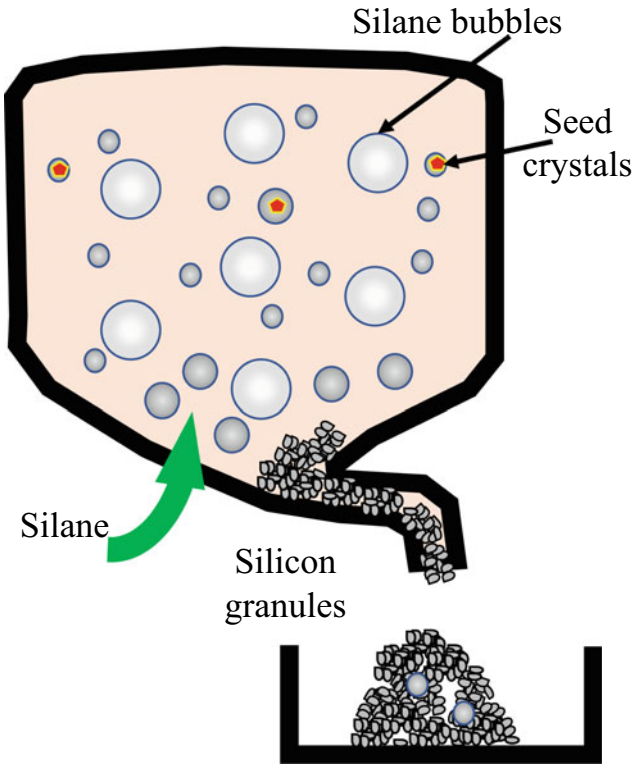



**Fig. 5** A schematic of the process of silicon purification and refinement via a fluidized bed reactor

in making solar cells. The silicon grains need to be melted and solidified again to facilitate the process of making silicon wafers. The purity of chunks of silicon grains can be shaped into monocrystalline or multi-crystalline silicon wafers through specific processes. Two processes are used for the production of ultrapure ingots of monocrystalline silicon. These processes are (i) the Czochralski (Cz) process and (ii) the float zone (Fz) process.

## 3.1 The Czochralski Process

Jan Czochralski, a Polish scientist, invented the self-titled technique "The Czochralski Process" in 1916, while studying the different rates at which metals crystalize. This process is used to produce a single crystal "monocrystal" of semiconductors, metals, and salts. This process is used to this day due to its simplicity to control the crystallization rates of semiconductors, such as silicon (What does Czochralski Process Mean? 2023). The Cz-Si is the Czochralski-Silicon process that started producing monocrystalline silicon which is still more expensive than the polycrystalline silicon, as it requires directional solidification and patient workers to produce them. The process is carried out by first melting the high-purity, semiconductor-grade silicon chunks in a crucible at 1425 ºC, usually made of quartz, into homogenous molten silicon. By adding precise amounts of dopant impurity atoms, such as boron and phosphorus, the produced silicon can be altered to become p or n-type, respectively, with varied electronic properties. Then, a seed crystal mounted on a rod that is precisely oriented is dipped into the molten silicon. As the silicon starts to crystalize around the seed crystal, the rod is controllably pulled out while being rotated to collect more silicon through its ascension. The temperature gradients, rod pulling rate, and rotation speed are precisely controlled to extract a large single-crystal cylindrical ingot of silicon. To prevent issues such as immature crystallization and the formation of grain boundaries, the process is undertaken in an inert atmosphere of argon, or in an inert chamber made out of quartz. Figure 6 shows the process of the Czochralski-Silicon method to acquire monocrystalline silicon, and the picture shown in the figure is taken in the Science Museum in London (a highly recommended visit if you are in London: https://www.sciencemuseum.org.uk/).

The Cz-Si process results in oxygen-rich silicon wafers. Oxygen impurities ultimately lower the minority carrier lifetime (a concept which will be discussed later) and reduce the voltage, current, and efficiency of solar cells. There are various sources of oxygen impurities, such as the atmosphere and the seed crystal. Additionally, oxygen impurities are active at higher temperatures, which results in temperature-sensitive wafers, and hinders the quality of any following processes. To address this issue, an alternative method, the float zone method, was introduced.

## 3.2 Float Zone Process

The float zone (Fz-Si) is an alternative to the Cz method for single crystal making. The process produces high-purity silicon wafers with extremely low concentrations of oxygen and carbon impurities. Nevertheless, the float zone method has high concentrations of nitrogen impurities that are intentionally added to aid in controlling the microdefects. Most importantly, nitrogen impurities are added to enhance the mechanical strength of the silicon wafers. The float zone method is similar to the Cz-Si procedure; however, it does not pull the seed crystal, instead it involves casting the molten silicon and then applying a strong magnetic field to induce heat within the ingot. The induction coil is mobile and moves either up or down the ingot while being wrapped around it. The magnetic effects induce heat and is applied to the cast silicon regions, or zones, which results in multiple float, or molten, zones. As the induction coil moves up, the float zones carry the impurities and move up simultaneously, leaving behind a big grain of monocrystalline range. With

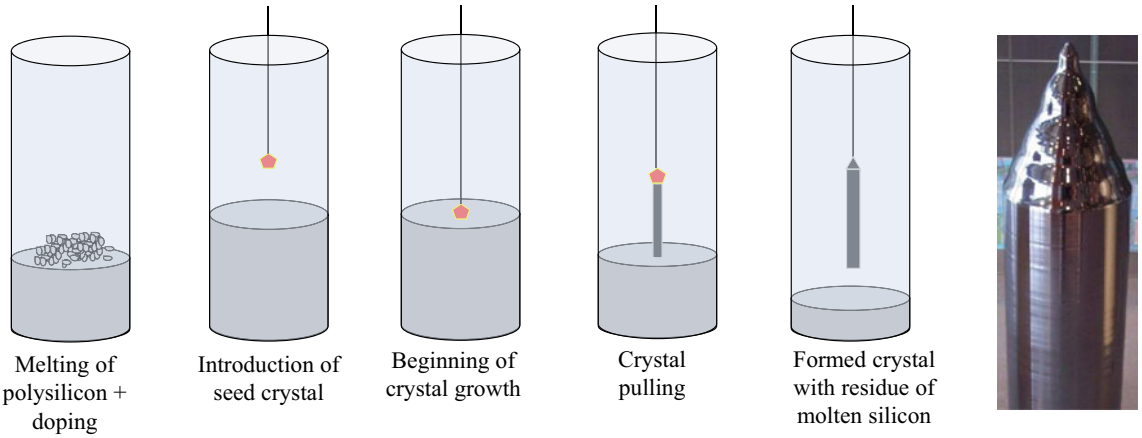



**Fig. 6** Process of obtaining monocrystalline silicon through the Czochralski-Silicon method. The photo is a Cz grown ingot displayed in the Science Museum of London (Silizium and für die Waferherstellung 2023)

the continuation of the upward coil motion, the monocrystalline range enlarges simultaneously. At the end of the process, all the excess parts of the casted silicon, including the molten zones and impurities, are cut, leaving behind a monocrystalline silicon wafer with extremely low impurities. In the float zone method, the surface tension of the silicon limits the sizes of the monocrystalline wafers. Most sizes of monocrystalline wafers do not exceed 20 cm. Additionally, the shape of the monocrystalline is heavily influenced by the float zone and the coil size. For instance, as the float zone or the coil size increases, most of the cast silicon starts to melt, consequently, the monocrystalline shape cannot be formed. Figure 7 details the several stages associated with the float zone method for producing monocrystalline silicon. Figure 8 shows a close-up of the process as well as a picture of the coil in action.

Both the Cz and the Fz processes have their own merits and drawbacks. The quality and the budget available for each process are important selection parameters. A summary of the pros and cons of each is given in Table 1.

The Cz-Si process and the float zone method both produce monocrystalline silicon crystals. Monocrystalline silicon is manufactured and produced due to its high efficiency; however, it is rather expensive. On the other hand, multi-crystalline silicon is more cost-effective to produce; however, most of the produced multi-crystalline silicons have low efficiencies and highly visible grains and grain boundaries.

## 4 Multi-crystalline Silicon (MS-Si) Production Processes

Multi-crystalline silicon is produced by two processes, either (i) directional solidification or (ii) ribbon growth.

*Directional solidification*

This process controls the direction of heat loss from the silicon melt in a crucible. It is carried out by initially placing highly pure silicon into a silicon nitrate ($Si_3N_4$)-coated crucible, made of quartz. Two filaments, containing a seed crystal made up of pure silicon, are dipped into the crucible. The filaments are pulled back to obtain the accumulated silicon around the exterior walls of the filaments. After obtaining the multi-crystalline silicon, the silicon block is cut by a metallic wire, then diced and sliced into thin wafers. Upon acquiring the thin silicon wafers, the wafers are properly washed and prepared. Total growth times range between 20 and 30 hours producing large half-ton ingots. Figure 9 presents the process of directional solidification for producing multi-crystalline silicon.

### 4.1 String Ribbon Process

In this process, there is no double crucible setup as in the directional solidification technique. A seed crystal with wire filaments are dipped into a molten silicon crucible made of quartz as shown in Fig. 10a. In a process that depends on cohesive forces and surface tension, a thin sheet of silicon is formed akin to the formation of a soap bubble on a special frame (see Fig. 10b). This method saves post-processing steps as the wafer is produced to the required dimensions, but it is slow and requires complex control, intense labor involvement, and training.

### 4.2 Ribbon Growth Technique

In contrast to directional solidification, ribbon growth reduces the waste induced from post-processing steps, such

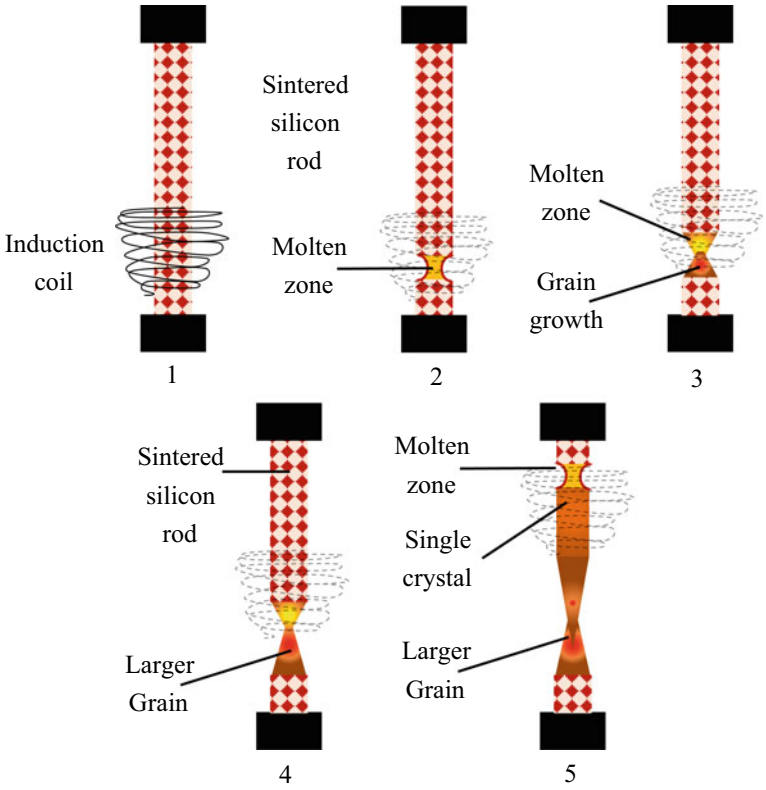



**Fig. 7** Several stages incorporated in the float zone method for obtaining monocrystalline silicon

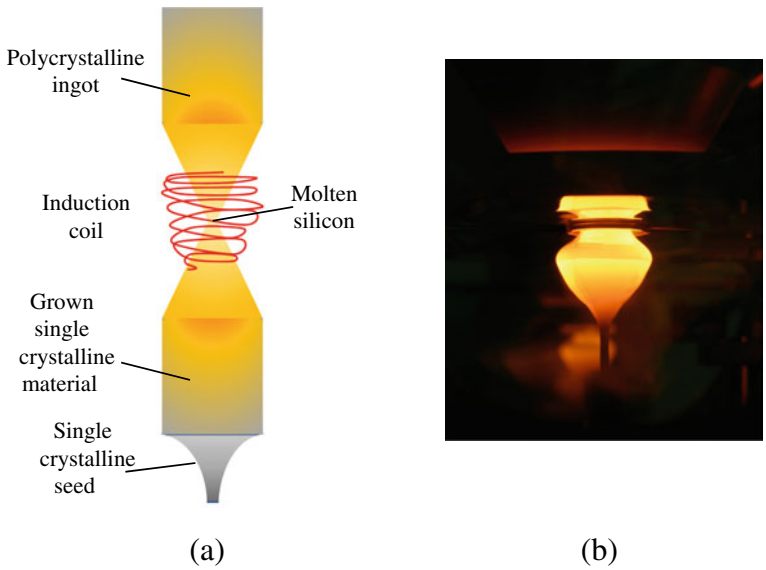



**Fig. 8** **a** A close-up of the float zone process and **b** a picture of the induction coil around the cast silicon ingot (Si-crystal floatingzone 2023)

**Table 1** Comparison between Cz and float zone

| | Cz technique | Float zone technique |
|---|---|---|
| Advantages | • Allows big crystal diameters (~46 cm)<br>• Lower production cost | • Low-impurity concentration<br>• Dopant concentration in the final crystal is homogenous |
| Disadvantages | • Higher impurities (oxygen and carbon) from quartz and graphite crucibles<br>• Low homogeneity of axial and radial dopant concentrations due to oscillations | • More expensive than Cz<br>• Crystal diameter limited to ~20 cm |

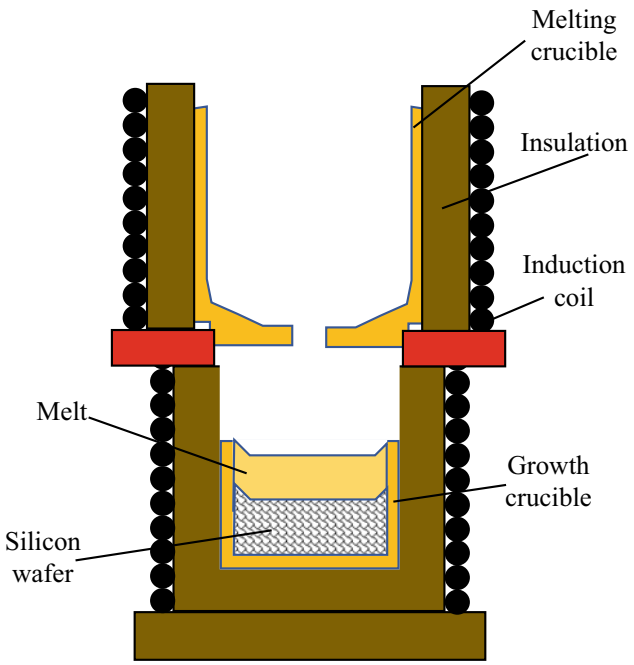



**Fig. 9** Directional solidification

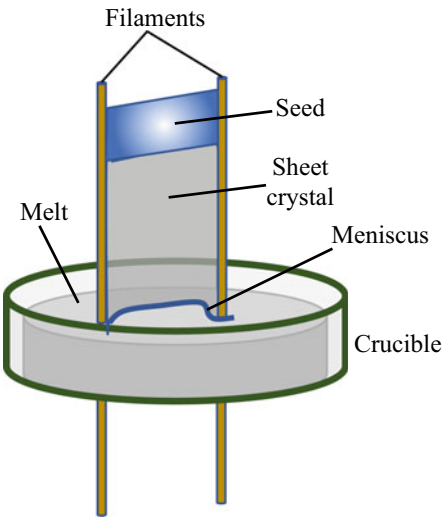
as slicing and dicing, just like string ribbon process. Ribbon growth is another alternative to produce multi-crystalline silicon wafers from molten silicon in less than an hour. In this method, the molten silicon is poured into a dye. A substrate is placed underneath the dye to shape the thickness of the multi-crystalline silicon wafer. Hence, the thickness of the produced multi-crystalline silicon depends on the speed of the moving substrate. Ribbon growth produces thin multi-crystalline wafers without the need of slicing or dicing the wafers; this in return reduces waste. Nevertheless, other post-processing steps, such as cleaning and polishing, are still necessary. The produced multi-crystalline wafers are made of doped silicon; thus, they tend to be extremely fragile. For this reason, the wafers need to be contained within an insulating, anti-reflective material, such as glass, this in return seals the wafers from water, humidity, or other impurities. Figure 11 shows the production of multi-crystalline silicon wafers by utilizing the ribbon growth method. The process is similar to road marking technique, where hot thermoplastic paint is applied through a machine with a shaping dye that holds the hot paint, while a dye opening applies a homogenous thickness of paint that depends on the size and speed of the dye.

### 4.3 Comparison Between Bulk Process and Ribbon Growth

In general, bulk processes produce a lot of waste of virtually nonrecyclable material. As can be seen from Fig. 12, bulk silicon processing requires 1–2 days to start producing wafers that utilize 30–50% of the starting ultrapure silicon. The rest must go through the refinement process one more time. On the other hand, ribbon or string grown silicon requires less than an hour for the first wafer to appear. But the process is slow and requires intensive trained labor intervention. Figure 13 lists the main steps for each process (bulk and ribbon), with less steps for the latter.

## 5 Silicon Post-processing

Post-processing of the produced ingots from the CZ or the float zone methods is both time consuming and extremely wasteful. Post-processing of the ingots is carried out to




a

b

**Fig. 10** **a** Production of multi-crystalline silicon through the string ribbon method and **b** similarity of soap bubble adhesion to the filaments (Soap-Bubble Shapes 2023)

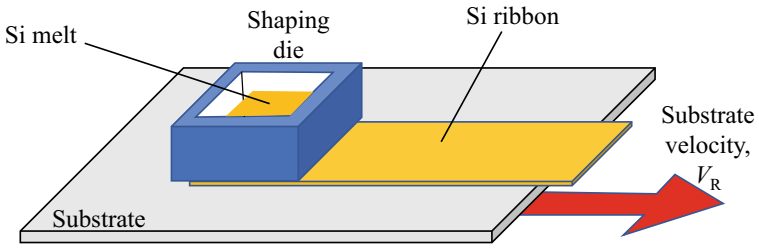



**Fig. 11** Ribbon growth method for obtaining multi-crystalline silicon, where $V_R$ is the speed of the moving substrate

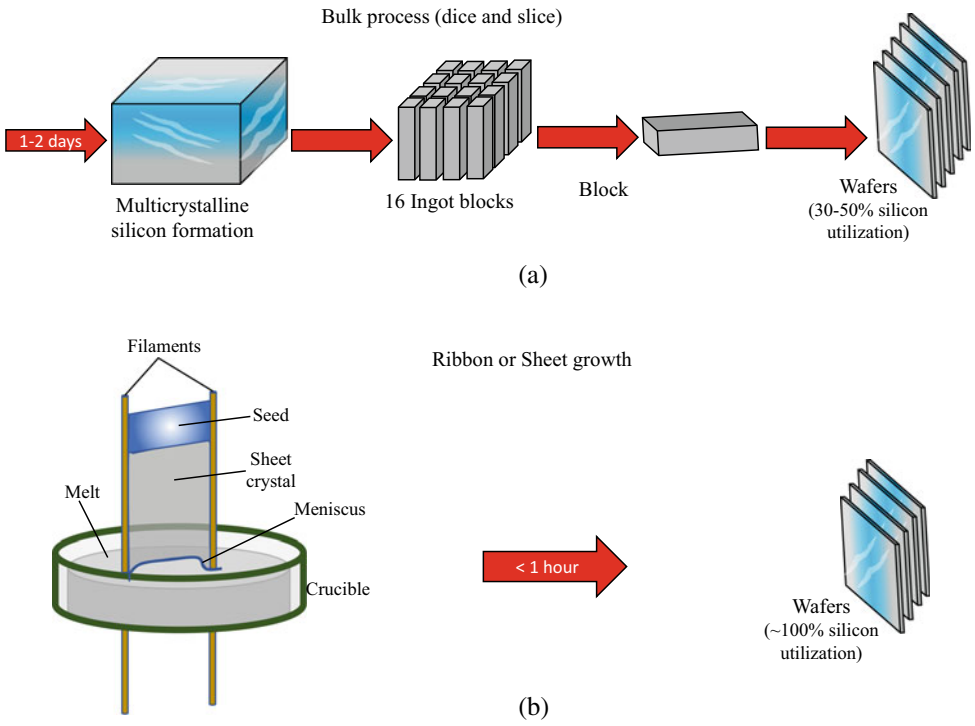



**Fig. 12** Process comparison of **a** bulk silicon wafer production and **b** ribbon or sheet grown silicon

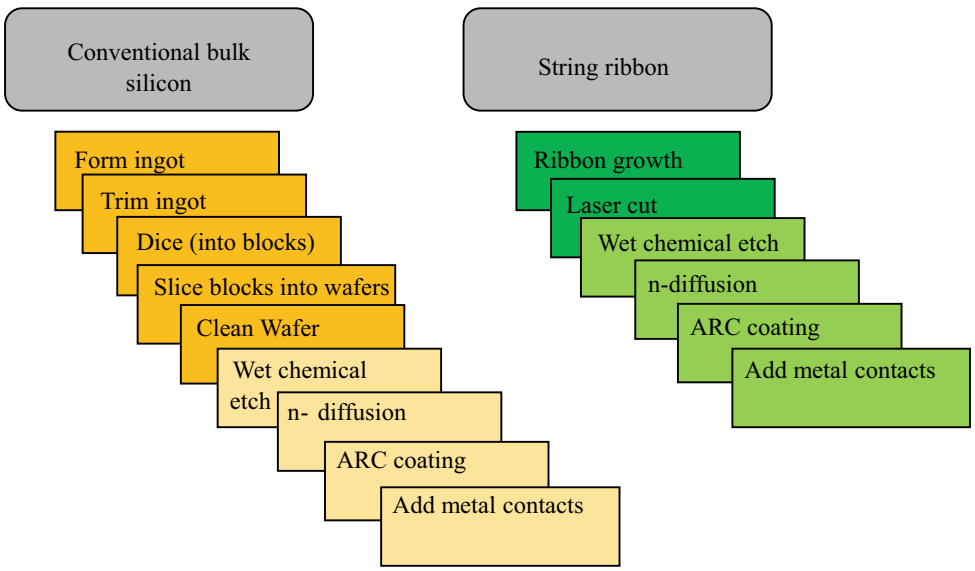



**Fig. 13** Main steps for bulk silicon and string ribbon processes

convert mono-crystalline silicon into thin either mono or multi-crystalline wafers. Figure 14 shows the steps required to arrive at the wafer, which starts either with a Cz monocrystalline ingot, or as a MS-Si from a silicon melt in a quartz crucible. The silicon is allowed to solidify (into MS-Si), is diced into blocks (16 is a conventional number); then it is sliced with either a saw or diamond-tipped metallic wire (just like country bread is cut into slices) for wafers to be produced.

The silicon from Cz comes in the form of cylinders. These cylinders are diced either by an inner diameter sawing or a wire saw. As can be seen in Fig. 15a, the wafer is sliced using an inner diameter sawing technique, in which the cutting edge of the circular blade is embedded with diamond splinters. A better idea is to use a wire saw that cuts the wafer with several parallel wires. This will minimize the induced wastes from dicing, as shown in Fig. 15b. Try using unscented floss to cut a cake instead of using a knife and you will appreciate how low the waste (stuck to the knife) is. The wire is made up of steel with a diameter of 100–200 μm and a speed of 10 m/s.

The first step is grinding, which involves decreasing the diameter of the ingots using either the CZ or FZ method with the aim of making them more workable and cutting them into shorter cylinders. Grinding also adds certain features to the formed cylinders to distinguish the p-type from the n-type material. This is shown in Fig. 16.

Once the wafers have been diced, they are lapped on both sides in attempt to eliminate any surface debris that could have been fractured as a result of the slicing process, as well as to thin the wafer to the desired thickness. Figure 17 demonstrates a schematic view of a wafer lapping machine. After the required thickness of thin wafers has been obtained, they are etched using either KOH (a base) or $HNO_3$/HF (an acid) to remove any damaged surfaces.

The wafers are then polished to remove any excess acids/bases left on the wafers. Super-flat, mirrored surface with minimum surface roughness wafers are attained after polishing. Once the wafers have been polished, they go through a cleaning process with ultra-pure chemicals, which gets rid of the polishing agents and ensures that the wafers do not contain any residuals. Etching, polishing, and cleaning are categorized as finishing processes that are responsible for adding small features on the surface of the wafers to indicate the type of interaction the wafers have with the incoming solar radiation. These small features are also known as the miller indices, or exposed planes, which are shown in Fig. 18.

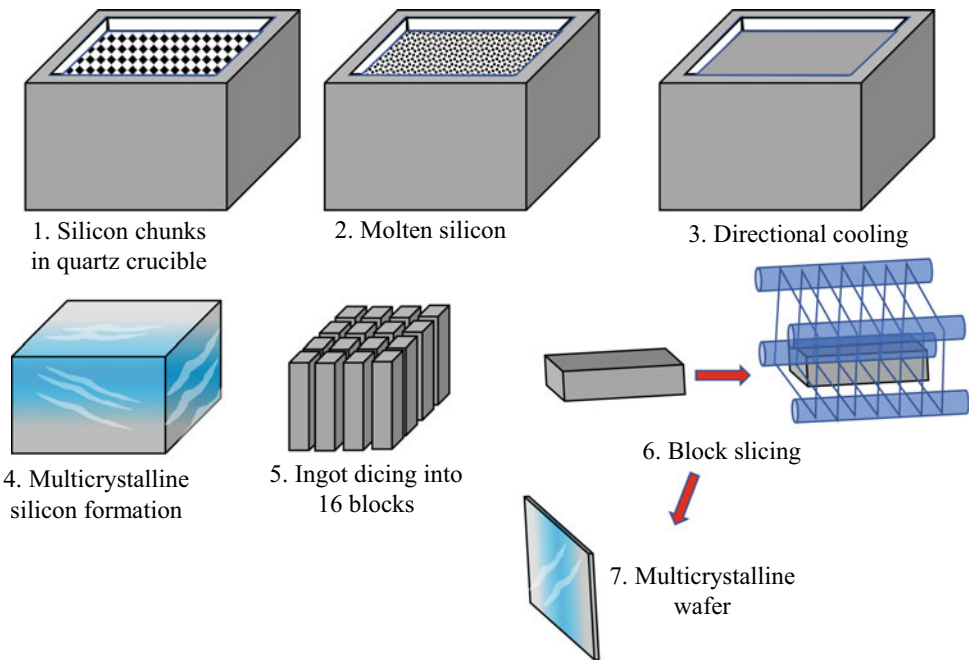



**Fig. 14** Main steps of producing wafers from bulk silicon production

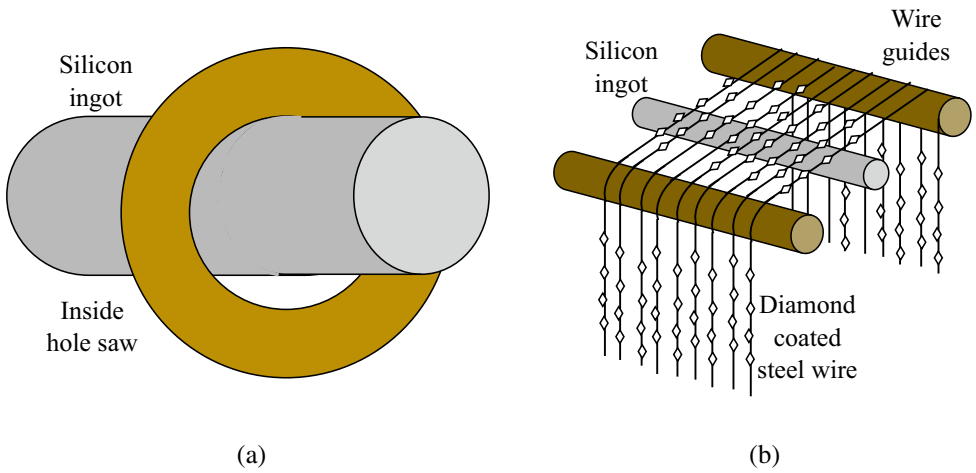



**Fig. 15** **a** Using an inner saw reduces the broken edges and provides better control over the cut and **b** diamond-coated steel wires allow lower waste from the slicing operation

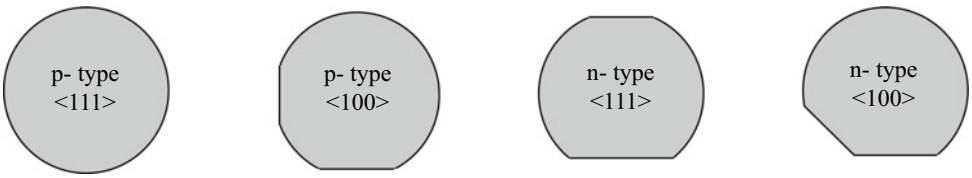



**Fig. 16** Adding different features to the wafer to distinguish doping status and exposed crystallographic planes

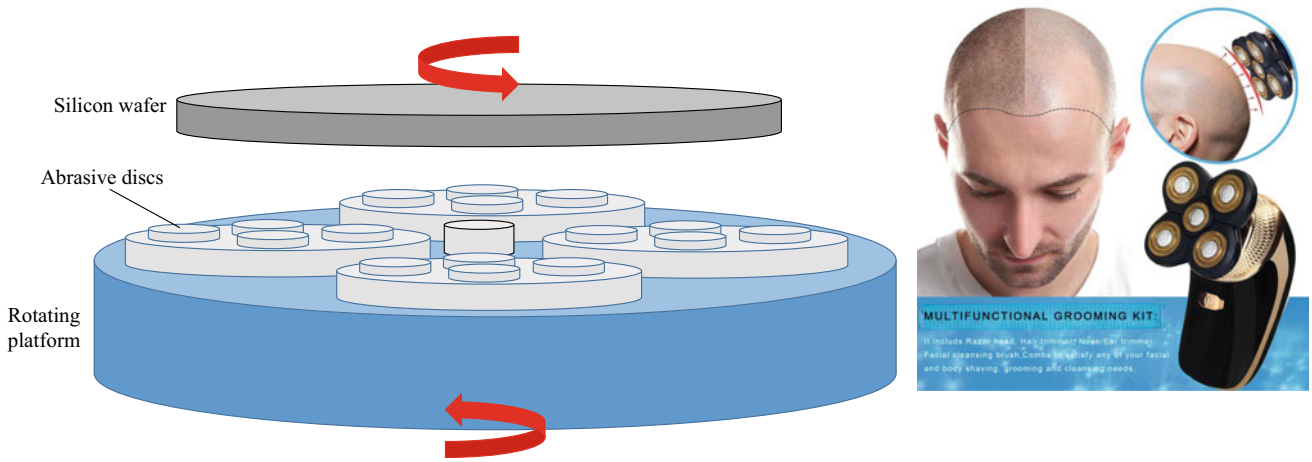



**Fig. 17** Schematic of a wafer lapping machine and its similarities with electric shaver razor (DOTSOG in this case)

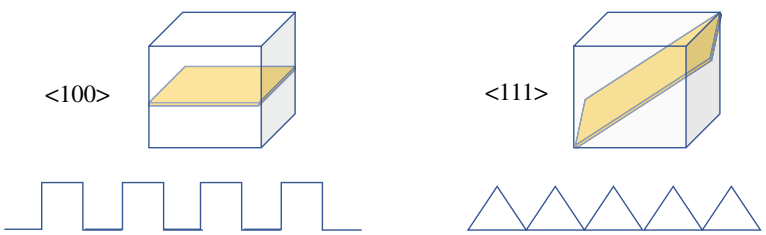



**Fig. 18** Crystallographic plane families that are exposed according to silicon wafer etching

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