Chapter 3
ABB's Recent Advances in Solid-State Circuit Breakers

Li "Lisa" Qi, Xiaoqing Song, Thorsten Strassel, and Antonello Antoniazzi

1 Introduction

The need of easing and making the integration of distributed energy resources from renewables more effective is driving a new resurgence of DC in power distribution, which this time is feasible and convenient due to the recent developments in power electronics. On the other hand, DC power distribution raises tough challenges in terms of circuit protection, as fault current can be extremely large and growing at extremely high rate that conventional protection devices, e.g., electromechanical circuit breakers, cannot cope with. A viable solution to such protection needs is given by solid-state circuit breakers (SSCBs), exploiting the latest development of power semiconductor technology, such as low-losses IGCTs and WBG FET devices.

At present, a satisfactory technology fitting all SSCB applications has not yet emerged, but different design solutions are possible matching the various power ratings.

This chapter presents ABB's recent investigations on SSCBs based on optimized Si IGCTs, looking for the best fit for high power SSCBs, for rated currents in the range of kAs and rated voltage from 1 kV and up, and on presently available SiC FET devices, more suited for lower power SSCBs. The design of such SSCBs is

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discussed, from the selection of the power semiconductor device to the requirements for the gate drive circuit, the cooling system, the voltage clamping, and the protection control.

Finally, some application cases of SSCBs in DC microgrids and in DC power system for marine vessels are highlighted, with specific focus on the motivation for using SSCBs instead of conventional protection devices.

2 Solid-State Circuit Breakers

The interruption process and functions of components in a SSCB are briefly explained in this section. Section 3.6 gives theoretical analysis using IGCT-based SSCB as an example.

The conceptual diagram of a solid-state circuit breaker (SSCB) and the main functional units are illustrated in Fig. 3.1. Low on-state loss semiconductor devices ensure high efficiency at conducting condition and fast current interruption in case of faults. Differently from the application in power converters, switching losses are not relevant for SSCBs, possibly leading to different device designs and optimization. Several semiconductor devices can be connected in series and/or parallel to meet SSCB’s voltage and current requirements. Bidirectional power flow is typically controlled through arranging devices in antiparallel or in antiseries, as only a few 4-quadrants inherently symmetric devices (e.g., GaN HEMT) exist. Moreover, one can distinguish between turn-on only device (as thyristors) and turn-off devices (as MOSFETs, IGBTs, IGCTs). While thyristors or triacs could be used in AC applications, turn-off semiconductor devices are used more frequently in SSCBs

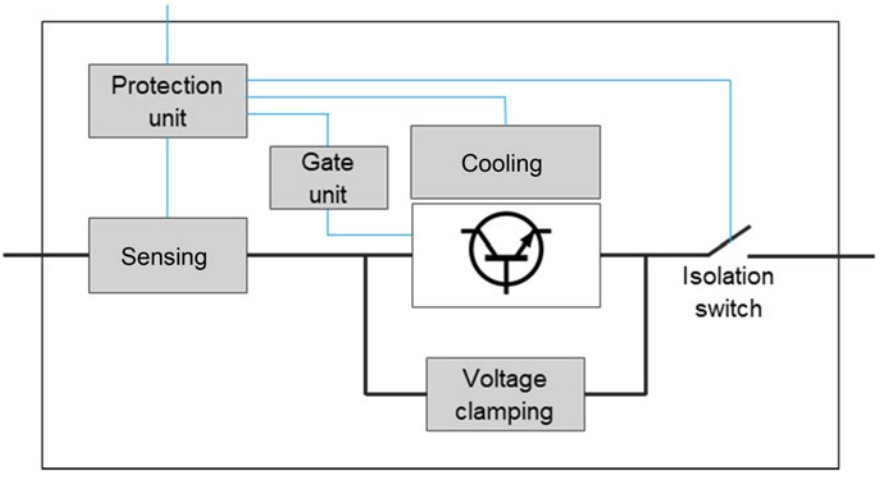


Fig. 3.1 Conceptual block diagram of a typical SSCB

for reasons of fault current limiting or for DC interruption. A SCCB concept has to take these device characteristics into account and compensate potential drawbacks to match the application needs. Sections 3 and 4 describe two SSCB architectures based on different semiconductor devices.

A voltage clamping circuit (e.g., a Metal Oxide Varistor (MOV)) is used to limit the temporary overvoltage when the semiconductor switches are turned off and to absorb the inductive energy of the grid, which could be a challenge especially in connection with large current limiting inductive elements. A cooling system, e.g., a heat sink with or without fans, or liquid-cooled cold plates for high power devices, keeps the temperature of the junction in the safe area. Due to safety requirements, e.g., in case of maintenance, a mechanical contact system is used to provide air-gap galvanic isolation. The protection unit controls the power semiconductor device, through the gate unit, and the isolation switch, providing protection functions, including fault detection, location, and protection coordination, as well as auxiliary functions such as measurement and communication.

Different designs of these functional units are described in the following sections.

3 Design and Development of IGCT-Based SSCBs

3.1 Selection of Semiconductor Devices

High power Silicon Integrated Gate-Commutated Thyristors (IGCTs) are good candidates for fully controllable bidirectional SSCBs, in particular for high power applications, with large rated current in the range of 1 kA+ and rated voltage in the upper end of the LVDC range. Most typical IGCT is asymmetrical (A-IGCT) and requires a diode in series to block the reverse voltage; alternated configurations with the diode in parallel to the IGCT are not suitable for bidirectional switching. Reverse Blocking IGCT (RB-IGCT) has been optimally designed to provide very low conduction losses and both forward and reverse blocking capability [2, 3]. The electrical characteristics of the selected RB-IGCT are the following:

Forward blocking voltage:	2500 V
Reverse blocking voltage:	−2500 V
Voltage drop (&1000 A):	0.9 V

Figure 3.2 shows the topologies of bidirectional switching blocks based on antiparallel A-IGCT and RB-IGCT, whereas the conduction loss profiles of bidirectional switching blocks based on A-IGCTs, RB-IGCTs, and IGBTs are compared in Fig. 3.3. The low conduction loss achieved with the optimized RB-IGCT up to 3000 A confirms that it is an appropriate choice for SSCB applications.

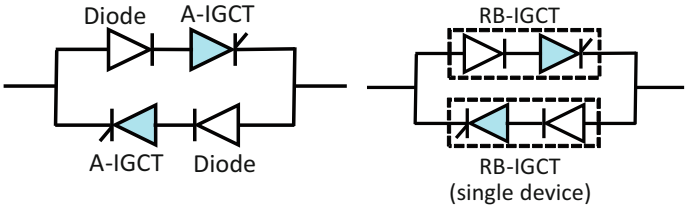


Fig. 3.2 A-IGCTs and RB-IGCTs for bidirectional switching [4]

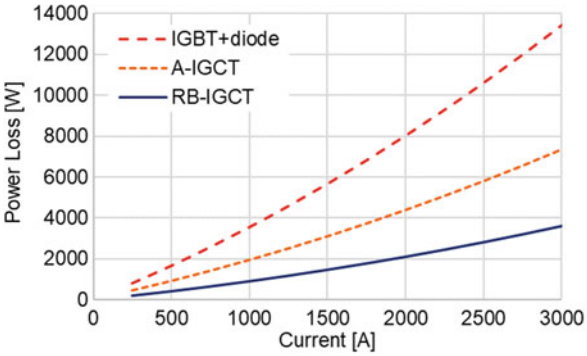


Fig. 3.3 Conduction loss profile of A-IGCT, RB-IGCT, and IGBT bidirectional switches [4]

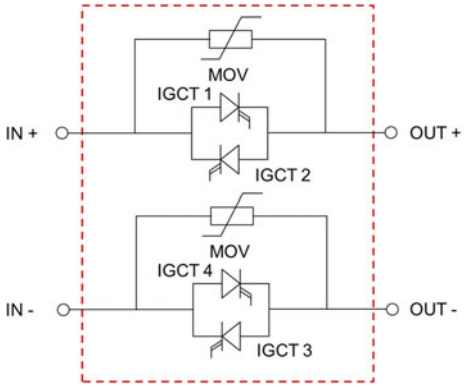


Fig. 3.4 Circuit diagram of a two-pole RB-IGCT SSCB (the isolation switch is omitted) [4]

A two-pole SSCB can be built using two RB-IGCT switches on the positive and the negative conductor, as illustrated in Fig. 3.4. The efficiency of such two-pole RB-IGCT SSCB, as given in Fig. 3.5, is higher than 99.9% for currents up to 1500 A. More antiparallel switches can be connected in parallel for higher nominal currents.

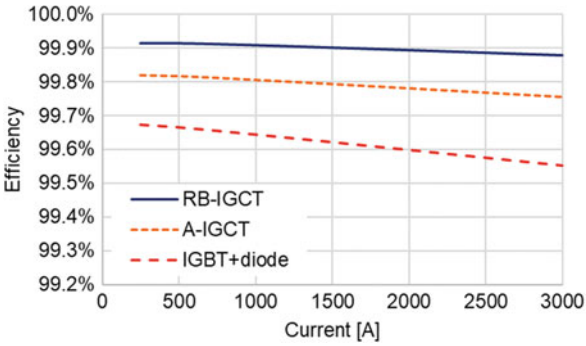


Fig. 3.5 Efficiency profile of the two-pole SSCB using RB-IGCT, A-IGCT, and IGBT [4]

3.2 Voltage Clamping

After an RB-IGCT SSCB is turned off, the energy accumulated in the system inductance needs to be dissipated to avoid the resulting overvoltage can damage the semiconductor device. This energy dissipation is achieved by a MOV, which is a nonlinear device providing high impedance at "low" voltage level, i.e., at the system voltage, and low impedance at "high" voltage level, i.e., at the max. allowed voltage. In this way, the MOV only conducts a very low leakage current at the normal operating voltage and clamps the voltage to a level that does not damage the RB-IGCTs when they are turned off to interrupt the fault current. The detailed description of the interruption sequence can be found later in Sect. 3.6.

Figure 3.6 shows the voltage-current characteristics of the selected MOV for the RB-IGCT SSCB, with a diameter of 108 mm and a thickness of 7.3 mm, corresponding to a residual voltage of 2180 V at 5000 A and a leakage current smaller than 1 mA at 1 kV; the maximum energy capacity is 10.7 kJ (95 J/cm^3). Thanks to the low inductance of the clamping circuit connecting the MOV, the overvoltage peaks are limited below the RB-IGCT's maximum blocking voltage of 2500 V. The MOV has been protected in a sealed packaging to withstand harsh environmental conditions.

3.3 Cooling and Mechanical Design

Due to RB-IGCT's relatively low losses, both air cooling and liquid cooling are suitable even for this high-power SSCBs. It is commonly known air-cooled systems tend to be bulkier than liquid-cooled systems, but they eliminate the need for auxiliary components such as heat exchangers, external coolant connections, etc. which are typically not considered in the comparison. One implementation of an air-cooled RB-IGCT SSCB is described in the following.

To improve the power density of the circuit breaker, despite the condition to use air to dissipate the losses, a two-phase cooling system was selected. Pulsating Heat

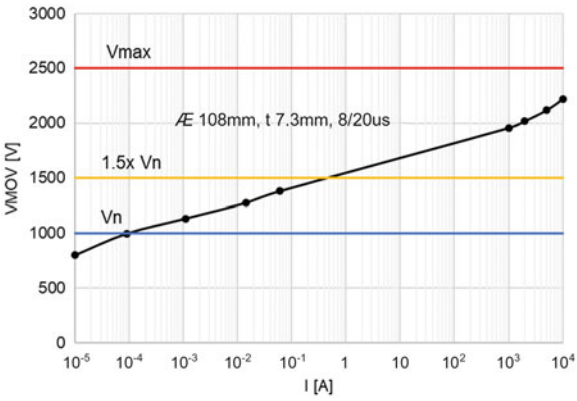


Fig. 3.6 Voltage-current characteristics of the MOV of the RB-IGCT SSCB [4]

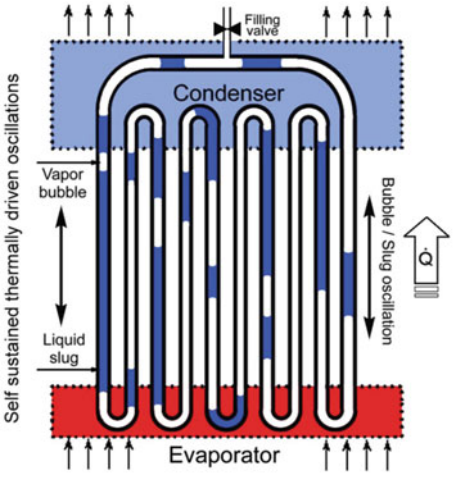


Fig. 3.7 Schematic of a pulsating heat pipes with the three different sections: evaporator, adiabatic, and condenser [7]

Pipes (PHPs) have been preferred over thermosyphons as they offer orientation-free performance, whereas thermosyphons’ efficiency is reduced when tilted. Independence from orientation is required in some applications, e.g., for shipboard systems due to the roll and pitch of the ships. PHPs have been demonstrated [6] and a schematic diagram is shown in Fig. 3.7 [7], and a customized PHP was designed to meet the unique requirements of the RB-IGCT SSCB [4, 8].

RB-IGCTs are puck-type devices that enable cooling on both surfaces. Furthermore, each pole requires two antiparallel RB-IGCTs. The stack was designed so that the RB-IGCTs (in blue) and the MOV (in grey) are in mechanical series while being in electrical parallel as illustrated in Fig. 3.8. This design allows active cooling of the MOV from the adjacent PHPs (in green), which is beneficial in case of fast repetitive interruption operations of the breaker, when the MOV needs to dissipate relatively large energy. This layout also permits a small amount of heat to be conducted through the MOV and dissipated by the up/downstream PHPs.

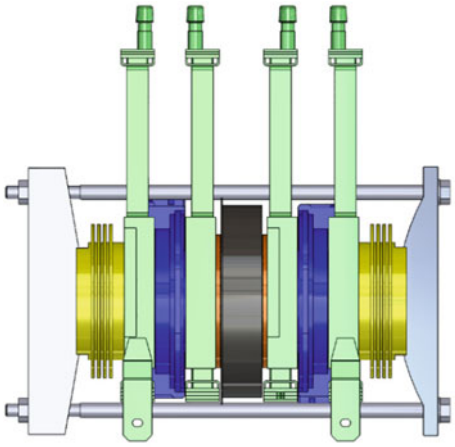


Fig. 3.8 Mechanical layout of one pole of the RB-IGCT SSCB [6]

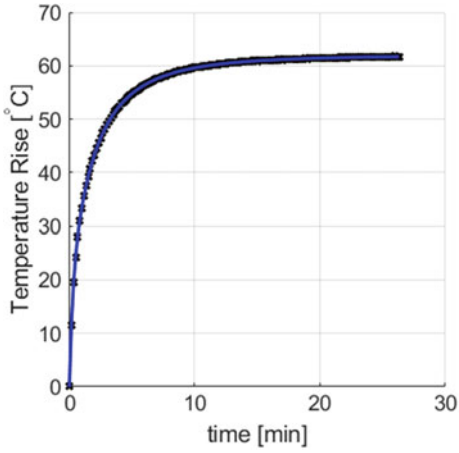


Fig. 3.9 Baseplate temperature rise of test article during 1500 A heat run [4]

Referring to Fig. 3.8, air is flowing in a duct (not shown) across the condensers of the PHPs. As the two condensers are in series in the air flow, thermal stacking may occur. This is not an issue in steady state, as only one IGCT is conducting at any moment, whereas transient thermal stacking, when the direction of conduction is inverted, can be more significant and requires additional margin in the design of the heat sinks. A heat run of the SSCB at 1500 A constant current is shown in Fig. 3.9. Finally, in bipolar circuit breakers, the gate units of the IGCTs on the two poles are interleaved to minimize the overall footprint of the SSCB.

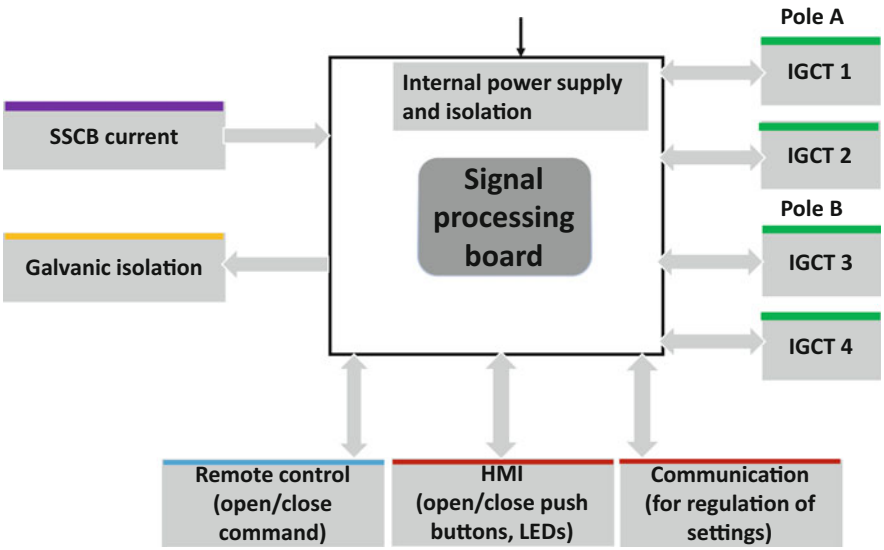


Fig. 3.10 Trip unit control board architecture

3.4 Control and Auxiliary System

In order to implement multiple functions of a SSCB (measurement, protection, control, monitoring, and communication), a microcontroller board was developed, which architecture is illustrated in Fig. 3.10. The trip-unit is designed to handle:

- The current sensor
- The galvanic isolation switch
- Control signals to the RB-IGCTs
- Feedback signals from the RB-IGCTs gate drivers
- The HMI panel with command buttons and indicators
- Interlock signals between different SSCBs
- Communication signal for status monitoring and tuning of the SSCB settings

The RB-IGCT gate drivers are controlled by fiber optics signal from the control board. An interlock signal is also travelling through fiber optic cables between the upstream and downstream SSCBs to allow protection coordination for selectivity. The measurement from the current sensor is processed by a signal conditioning circuit on the control board before being sent to the microcontroller.

The isolation switch provides galvanic isolation via air-gap, so that the SCCB ensures the same electrical safety for maintenance as electromechanical circuit breakers. The operation of the isolation switch is coordinated with the control of RB-IGCTs, to ensure arc-free operation at zero current by means of proper closing and opening sequences:

- Closing: the galvanic-isolation switch closes first, and then the ON signal is sent to the RB-IGCTs.
- Opening: the RB-IGCTs are turned-off first, and then the galvanic-isolation switch opens.

One primary function of the control board is to measure the current for short circuit and overload protection. A shunt resistor made of Manganin, chosen for its low temperature coefficient of resistance and long-term stability, was adopted for current measurement of the RB-IGCT SSCB. The shunt resistance value was selected to be 15 μΩ and can cover both the nominal current of 1500 A and overcurrent exceeding 5000 A.

When the time derivative of the fault current is large, the current measurement is affected by significant error due to the non-negligible stray inductance on the measuring path. The voltage measured by the microcontroller ADC (Analog Digital Conversion) is the sum of the actual voltage drop on the shunt resistance $R_{\text{shunt}} \cdot i_{\text{actual}}$ and the bias from the stray inductance $L_{\text{shunt}} \cdot \frac{di_{\text{actual}}}{dt}$, where R_{shunt} is the shunt resistance, L_{shunt} is the parasitic inductance, and i_{actual} is the actual current. The effect on the measured current i_{meas} is given in (3.1).

$$i_{\text{meas}} = i_{\text{actual}} + \frac{L_{\text{shunt}} \frac{di_{\text{actual}}}{dt}}{R_{\text{shunt}}} \tag{3.1}$$

Therefore, to reduce the measurement error, the stray inductance should be kept minimum or as low as possible.

A dedicated auxiliary power supply was developed to guarantee both the correct current profile and timing requested at start-up (34 V – 1 A steady, 8 A peak), and the insulation level to account for allowable system transient voltage level and the SSCB opening.

3.5 Experimental Validation

A test circuit for the RB-IGCT SSCB is illustrated in Fig. 3.11. Because of the ultrafast fault-current rising and response time of the device, the test circuit was designed to provide high current for less than 1 ms. Therefore, the test circuit can be implemented by an LC circuit with a capacitor bank and an adjustable air core inductance to emulate system inductance. The capacitance is sized to provide sufficiently high fault energy and short circuit current (e.g., current peak higher than 5 kA or more); the inductance L_{sys} can be adjusted from 30 to 200 μH to perform tests at different fault-current derivatives. Figure 3.12 shows the experimental setup of the short circuit test circuit. To perform the short circuit test, the capacitor bank is first pre-charged to 1 kV voltage by a High Voltage (HV) Low Current (LC) power supply, and then the power supply is disconnected and the RB-IGCT SSCB is closed.

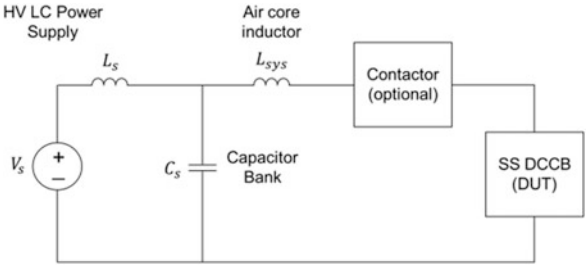


Fig. 3.11 Test circuit for the RB-IGCT SSCB [1]

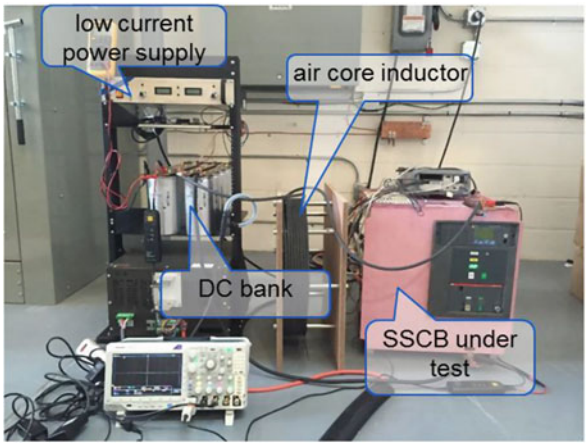


Fig. 3.12 Experimental setup of the test circuit [1]

Figure 3.13 shows the SSCB current and voltage from the short circuit testing when the system inductance is equal to 65 μH. After the circuit is closed, the fault is first detected at ~180 μs, and then the RB-IGCTs turn off within 5 μs. The fault current is limited and commutated to the MOV. The MOV dissipates the inductive energy and reduces the fault current to zero in ~190 μs. The overall breaking time, from the fault occurrence until the fault current goes to zero, is ~370 μs. Figure 3.14 illustrates the short circuit test results with the system inductance increased to 140 μH. As the fault current takes longer time to reach the threshold, the fault detection time is longer, and the RB-IGCTs are turned-off at ~390 μs. Similarly, as the stored energy is higher, it takes longer time (~ 370 μs) to discharge it across the MOV. The total breaking time is ~760 μs. Note that RB-IGCTs turn-off time, from the detection of the fault to the commutation of the current on the clamping circuit, is not affected by L_{sys}.

Protection coordination between two SSCBs was also tested with the test circuit in Fig. 3.15. The overcurrent threshold was set to 3 kA for the upstream SSCB CB1, and to 2 kA for the downstream SSCB CB2; therefore, at short circuit faults, CB2 is supposed to interrupt the fault current before CB1 takes any action. Figure 3.16 presents the current and voltages on CB1 and CB2 from one test with the system inductance adjusted to 200 μH: the voltage on CB2 raises when this SSCB opens and is then clamped by its MOV, whereas voltage on CB1 remains zero as this SSCB

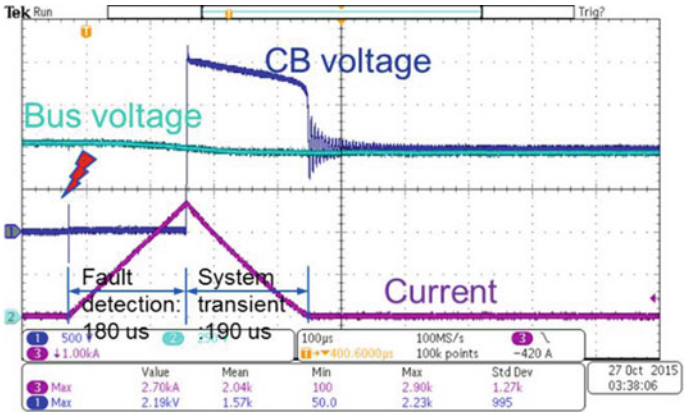


Fig. 3.13 Short circuit test result with low system inductance (65 µH) [1]

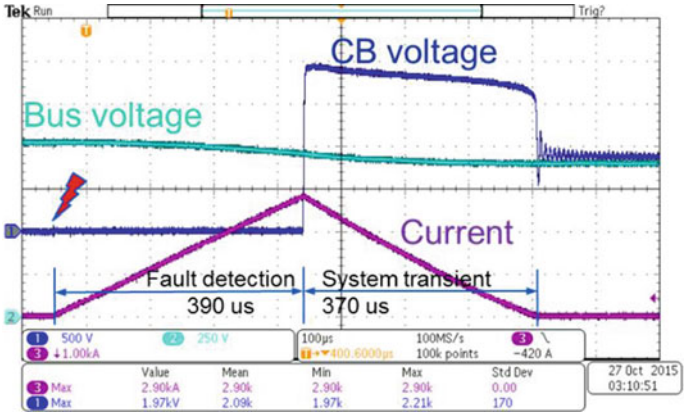


Fig. 3.14 Short circuit test result with high line inductance (140 µH) [1]

stays closed. Selectivity can be more difficult to achieve at higher current derivative. To avoid unwanted tripping of the upstream breaker CB1, when the trip unit in the downstream breaker CB2 sends the turn-off command to the RB-IGCT, it also sends an interlocking signal to CB1 blocking its false tripping.

ABB has unveiled a commercial solid-state circuit breaker, named SACE Infinitus, based on RB-IGCT technology, with rated voltage 1000 V and rated current 2500 A, employing a liquid cooling system [27].

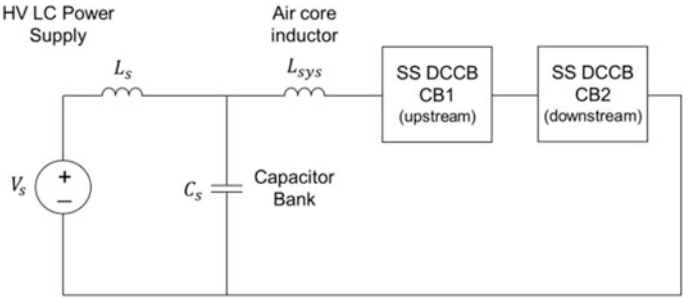


Fig. 3.15 Test circuit for protection coordination between two IGCT SSCBs [1]

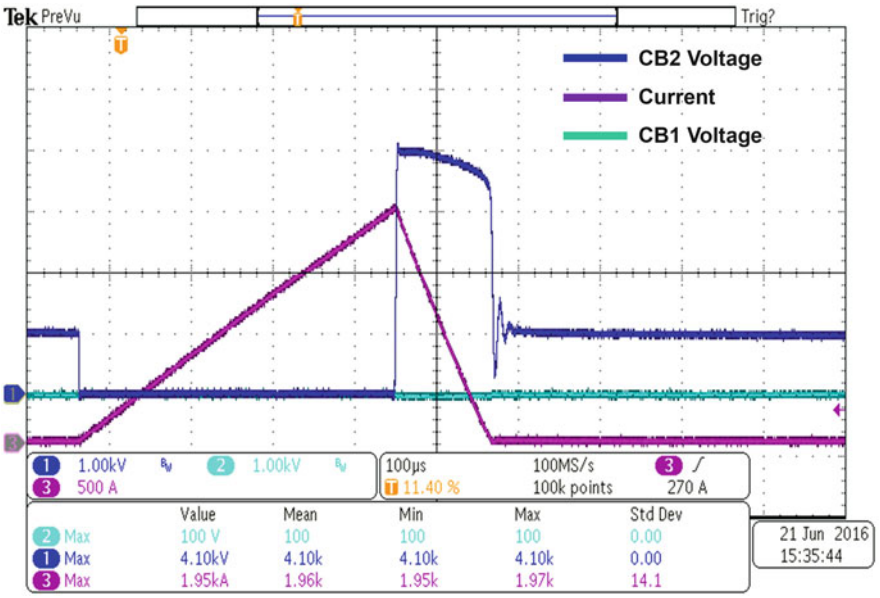


Fig. 3.16 Protection coordination test results [1]

3.6 Model-Based Design

SSCB breaker design is a tedious process and involves multiple components. A model-based design provides deep insights into the SSCB protection process and theoretical foundation for selecting parameters of each component inside the breaker. SSCB can be employed for overcurrent protection, to prevent consequent damages in grids where fault energy and current can be high. In DC applications, fault current can have large *di*/*dt* and rapidly rise to peak value within a few microseconds. Additionally, overcurrent and thermal limit of semiconductors on DC fault path are much lower than traditional power system equipment and devices.

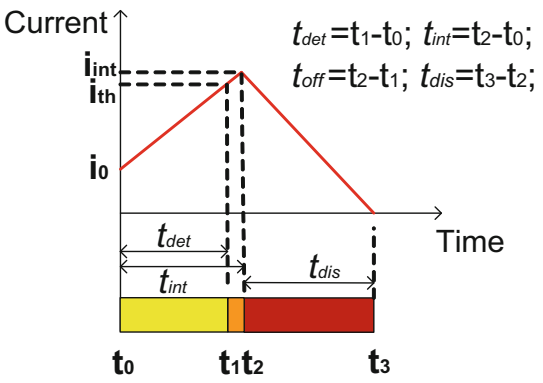


Fig. 3.17 Decomposition of a complete SSCB protection process [5]

Once a fault is detected, SSCB can react with ultrafast turnoff speed to interrupt DC current before it reaches dangerously high magnitude. Maximum allowable *di/dt* indicates the maximum rate of rise of the fault current the SSCB can interrupt in low-inductance grid (or low-inductance faults), while minimum *di/dt* gives indication on the maximum energy the SSCB can handle in high-inductance grid (or high-inductance faults). Proper system design can help reach a compromise for SSCB between required protection speed and energy dissipation.

The critical current rate of rise *di/dt* which can be handled by the circuit breaker is a more relevant indicator of the short circuit interruption performance of a SSCB than its breaking capacity, i.e., the maximum prospective current that it is capable of breaking, typically used for electromechanical circuit breakers.

The time decomposition of a complete protection process by a SSCB is illustrated Fig. 3.17. Considering ultrafast fault interruption speed by SSCBs, the DC fault current can be approximated as a linearly increasing current before the fault interruption. The protection starts from t_0 when the current is i_0. When the fault current increases to its threshold value i_{th}, the fault is detected and the fault detection time is t_{det}. t_{off} is the SSCB opening delay. i_{int} is the peak fault current after all delays in fault location and breaker opening. The fault interruption time is t_{int}. After the fault interruption, the fault current starts to decrease. t_{dis} is the energy dissipation time of the MOV.

The equivalent circuits during the complete SSCB DC fault protection process are illustrated in Fig. 3.18. R_{eq} and L_{eq} are equivalent system resistance and inductance. During the fault interruption and energy dissipation, the DC fault current flows through the semiconductor switch and MOV, respectively. When the switch is on, its resistance is combined into R_{eq}. When the MOV is on, it is approximated as a voltage source and a resistor, whose values V_{mov} and R_{mov} are derived from the linearization of its voltage-current characteristics at the SSCB's interruption current.

Equations (3.2) and (3.3) describe the two equivalent circuits at fault interruption and energy dissipation. The interruption time and the fault peak can be approximated by (3.4) and (3.5). The dissipation time and energy can be calculated from (3.6) and (3.7). Equations (3.6) and (3.7) are complex and difficult to see major impacting factors. Because of the high fault-current derivative, the voltage drops at the fault

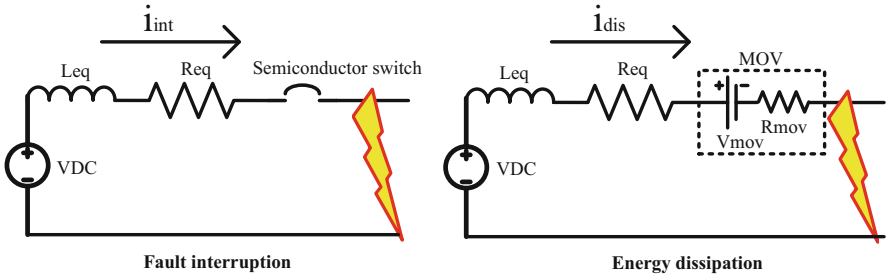


Fig. 3.18 Equivalent circuits during a SSCB protection [1]

resistance are much smaller than the drop on the fault inductance. If R_{eq} and R_{mov} are ignored from (3.6) and (3.7), then the dissipation time and energy can be estimated by (3.8) and (3.9). From (3.8) and (3.9), the energy dissipation time becomes longer with higher system inductance or with lower MOV clamping voltage. The dissipated energy is higher with higher inductance and higher clamping voltage.

$$V_{DC} = R_{eq} i_{intp} + L_{eq} \frac{di_{intp}}{dt} \tag{3.2}$$

$$V_{DC} = R_{eq} i_{dis} + L_{eq} \frac{di_{dis}}{dt} + V_{mov} + R_{mov} i_{dis} \tag{3.3}$$

$$t_{int} \approx \frac{i_{th} - i_0}{\frac{V_{DC}}{L_{eq}}} + t_{off} \tag{3.4}$$

$$i_{int} \approx i_{th} + \frac{V_{DC}}{L_{eq}} (t_{off}) \tag{3.5}$$

$$t_{dis} \approx -\frac{L_{eq}}{R_{eq} + R_{mov}} \ln \left(-\frac{V_{DC} - V_{mov}}{(R_{eq} + R_{mov}) i_{int} - V_{DC} + V_{mov}} \right) \tag{3.6}$$

$$\begin{aligned} E_{dis} \approx & \left(V_{mov} \frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} + R_{mov} \left(\frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} \right)^2 \right) t_{dis} \\ & + R_{mov} \left(i_{int} - \frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} \right)^2 \frac{e^{-2 \frac{R_{eq} + R_{mov}}{L_{eq}} t_{dis}} - 1}{-2 \frac{R_{eq} + R_{mov}}{L_{eq}}} \\ & + \left(i_{int} - \frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} \right) \left(V_{mov} + 2 R_{mov} \frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} \right) \frac{e^{-\frac{R_{eq} + R_{mov}}{L_{eq}} T_{dis}} - 1}{-\frac{R_{eq} + R_{mov}}{L_{eq}}} \end{aligned} \tag{3.7}$$

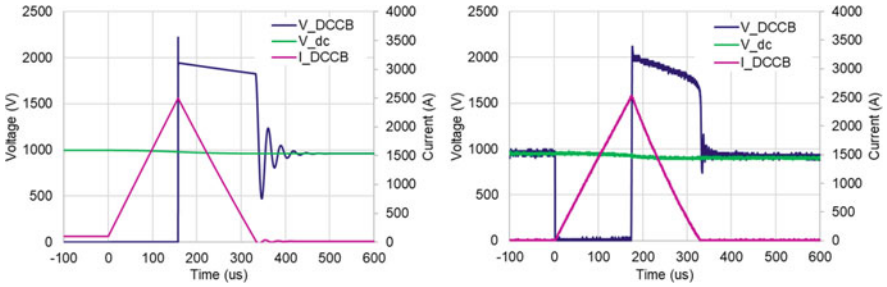


Fig. 3.19 Side-by-side comparison of simulated and experimental short circuit test results of RB-IGCT SSCB [6]

$$T_{\text{dis}} \approx \frac{L_{\text{eq}} i_{\text{int}}}{V_{\text{mov}} - V_{\text{DC}}} \tag{3.8}$$

$$E_{\text{dis}} \approx \frac{1}{2} \frac{L_{\text{eq}} {i_{\text{int}}}^2 V_{\text{mov}}}{V_{\text{mov}} - V_{\text{DC}}} \tag{3.9}$$

The equivalent circuits in the DC protection can be simulated in Matlab/Simulink. Figure 3.19 compares the simulation results and the experimental results when the system inductance is equal to 65 μH. The simulation results are quite close to the experimental results except some differences in the MOV performance. The errors are expected since the nonlinear characteristics of the MOV are approximately by a linear circuit (a reactance behind a voltage source) within its dominant operation zone. In this simulation, V_{mov} and R_{mov} are set to 1952 and 0.0282, respectively [6].

The above equations can be used to interpret and analyze the interactions between the protected DC system and the SSCB-based DC protection. The time delay t_{off} normally is quite small and thus can be neglected. From (3.4) and (3.9), the fault-interruption time and energy-dissipation time are proportional to the system inductance. This has been verified by the previous experimental test results. In the experimental validation, two different system inductance values 65 and 140 μH are used. Because the fault interruption time and energy dissipation time are linearly increasing with the inductance value, the breaking time for 140 μH is roughly doubled compared to the time for 65 μH. If the system inductance is low, the fault detection needs to be completed within short time frame, which is more challenging. From (3.8) and (3.9), the MOV dissipation time and energy are linearly increasing with the system inductance. The SSCB dissipates less energy and the fault current

is reduced to zero faster. On the other hand, the fault interruption time, energy dissipation time, and energy are all in reverse proportional to the DC system voltage. If the system voltage is high, the allowed fault detection time is short, but the energy to be dissipated is lower, and thus it takes less time for the SSCB to dissipate the energy.

4 Design and Development of SSCBs Based on SiC Unipolar Devices

IGCTs have very low conduction voltage drops at high current levels, thanks to the strong conductivity modulation in the thyristor type semiconductor switches, making them a good candidate for high current SSCBs. However, IGCTs do not fit very well with low current SSCBs, because of their low-current behaviors. The forward voltage, indeed, does not tend to zero at very low current but to a minimum value (~0.5 V for the RB-IGCT described in the previous section) dependent on its design.

Semiconductor devices with resistive characteristics, such as MOSFETs, fit very well for such application, in particular those based on Wide Bandgap (WBG) semiconductors that offer lower conduction resistances and higher voltages.

Table 3.1 summarizes and compares some key properties of 4H-SiC and GaN WBG materials compared with Silicon [9]. SiC and GaN have ~3× larger bandgap compared to conventional Si. Because of their larger bandgap, GaN and SiC can withstand ~10× larger breakdown electric field, resulting in devices with higher (>10 times) blocking voltage and lower (>300 times) conduction resistances compared to silicon devices.

Equation (3.10) shows the ideal specific resistances of the unipolar power semiconductor resistances with different blocking voltages [10].

$$R_{\text{on\_sp,ideal}} = \frac{4\,\text{BV}^2}{\varepsilon_S \mu {E_{\text{br}}}^3} \tag{3.10}$$

where BV is the blocking voltage of the power devices, ε_S is the semiconductor permittivity, μ is the electron mobility, and E_{br} is the breakdown electric field. Substituting the semiconductor properties into (3.10), it can be seen that the SiC-based power semiconductor devices could achieve ~300× lower conduction resistances compared to the Si-based power devices as shown in (3.11).

Table 3.1 Semiconductor material properties

Semiconductor materials	Si	GaN	4H-SiC
Bandgap (eV)	1.1	3.4	3.3
Electron mobility ($\text{cm}^2\text{v}^{-1}\ \text{s}^{-1}$)	1400	1200	1000
Breakdown electric field (MV/cm)	0.3	3.3	2.5

$$R_{\text{on\_SiC}} \approx \frac{1}{300} R_{\text{onSi}} \tag{3.11}$$

As conduction losses are the major contribution to the SSCB power losses, SiC and WBGs strongly reduce SSCB power losses and heat dissipation, also making cooling a lot easier.

4.1 SiC JFET vs. SiC MOSFET

The two most common types of SiC power devices are Junction Field Effect Transistor (JFET) and Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET). At device level, the main difference between the two is that JFETs are usually depletion-mode devices that are normally-on, which means they can conduct current when no voltage is applied at gate, while MOSFETs are mostly enhancement-mode devices that are normally off, meaning they are in blocking mode at zero gate voltage.

In terms of conduction losses, SiC JFETs are deemed to have lower specific resistance compared with SiC MOSFET. Figure 3.20 shows the simplified device structure of the SiC JFET and SiC MOSFET. For SiC JFET, the majority resistances include the JFET region resistance (R_{JFET}), drift region resistance (R_{Drift}), and substrate resistance (R_{sub}), while the SiC MOSFET device structure has additional channel resistance (R_{Ch}) as shown in (3.13).

$$R_{\text{on\_JFET}} = R_{\text{JFET}} + R_{\text{Drift}} + R_{\text{Sub}} \tag{3.12}$$

$$R_{\text{on\_MOSFET}} = R_{\text{Ch}} + R_{\text{JFET}} + R_{\text{Drift}} + R_{\text{Sub}} \tag{3.13}$$

Without channel resistances, the SiC JFETs can achieve lower specific resistance compared to SiC MOSFETs. Depending on the channel mobility and voltage rating, the channel resistance (R_{Ch}) could take up to 30% of the total resistances [10], which means SiC JFETs have potentials to achieve up to 30% lower resistances compared to SiC MOSFETs at certain voltage levels.

However, the absence of the inversion channel in SiC JFETs also leads to higher temperature coefficient of on-resistance compared to SiC MOSFETs. The channel resistance usually has negative temperature coefficient due to the higher electron mobility at elevated temperatures while the JFET region resistance, drift region resistance, and substrate resistance all have positive temperature coefficient. In SiC JFET, there is no inversion channel to offset the positive temperature coefficient of the JFET, drift layer and substrate, leading to a higher overall temperature coefficient [11].

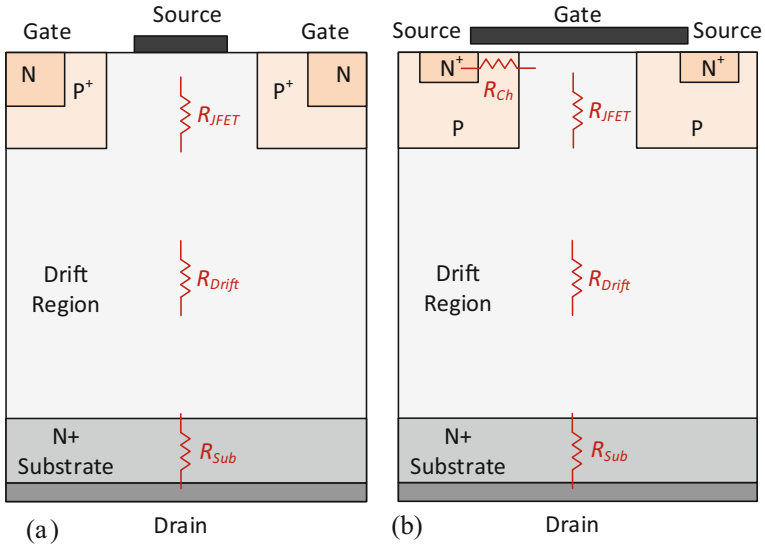


Fig. 3.20 Simplified device structure and major resistances of SiC JFETs and SiC MOSFETs. (**a**) SiC JFET; (**b**) SiC MOSFET

4.2 A Low Resistance SiC JFET Module

Figure 3.21 shows an example of a low resistance SiC JFET module, developed by ABB [12]. By paralleling four SiC JFET dies in parallel, the fabricated SiC JFET module has 4.2 mΩ total resistance from drain terminal to source terminal. The packaging of this SiC JFET module was carefully considered and designed to achieve a lower parasitic inductance and high temperature operation. For example, instead of soldering, the dies were sintered to direct bonded copper (DBC) with silver paste to withstand higher temperature. Two 10 mil aluminum (Al) wire bonds were used to connect source of the SiC JFETs to the DBC traces.

To better understand and optimize the packaging, the parasitic resistance of the module (such as DBC trace resistance, solder resistance, terminal resistance, bond wire resistance, contact resistance as shown in Fig. 3.22a) as well as the SiC chip on-state resistance are measured. Figure 3.22b shows the resistance distribution of the fabricated SiC JFET module. It is found that the bond wire and contact resistance contribute significantly to the module resistance. The total resistance of the wire bonding is 0.85 mΩ, consisting of 0.37 mΩ wire bond to chip source metallization contact resistance, 0.23 mΩ wire bond to DBC contact resistance, and 0.25 mΩ Al wire equivalent resistance. It is important to further optimize wire bonding to achieve low module resistances.

4.3 Reverse Conduction and Reverse Blocking Characteristics of SiC JFETs

While the forward conduction and blocking characteristics of the SiC JFETs are well known and tested, the 3rd quadrant characteristics including the reverse conduction and reverse blocking characteristics are often neglected and rarely studied. The SiC JFET's 3rd quadrant characteristics need to be better understood for bidirectional SSCB application, which requires to conduct and interrupt bidirectional currents.

Figure 3.23 shows the reverse conduction characteristics of the SiC JFETs compared with its forward conduction characteristics, all tested at room temperature with −2 V to +2 V gate voltages. At 1 ~ 2 V gate voltages, the reverse conduction resistances have similar values with forward conduction. When a slightly negative gate voltage (e.g., −2 V) is applied, the SiC JFET will saturate at a lower current during forward conduction, while reverse conduction demonstrates no saturation at much higher current levels (up to 50 A). An explanation of this phenomenon can be found in [13].

Figure 3.24 shows the tested SiC JFET's reverse blocking characteristics with gate voltages varying from 0 V to −10 V. The SiC JFET has no reverse blocking capability, even with very negative gate voltages (e.g., −10 V). With a more negative gate voltage (<−4 V), the reverse conduction voltage drop will also increase. The relationship between the negative gate bias voltage and the reverse conduction voltage can be found in [13].

4.4 Cooling System Design

Although the SiC power devices can achieve much lower conduction resistances compared to the Si counterparts, one remaining design challenge of SiC-based SSCBs is the cooling system, because of the still high power losses compared

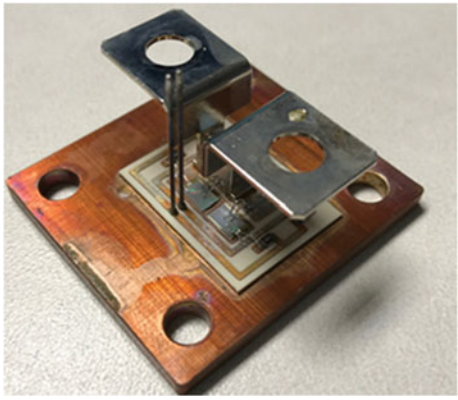


Fig. 3.21 The in-house developped low resistance (4.2 mΩ) SiC JFET module picture [12]

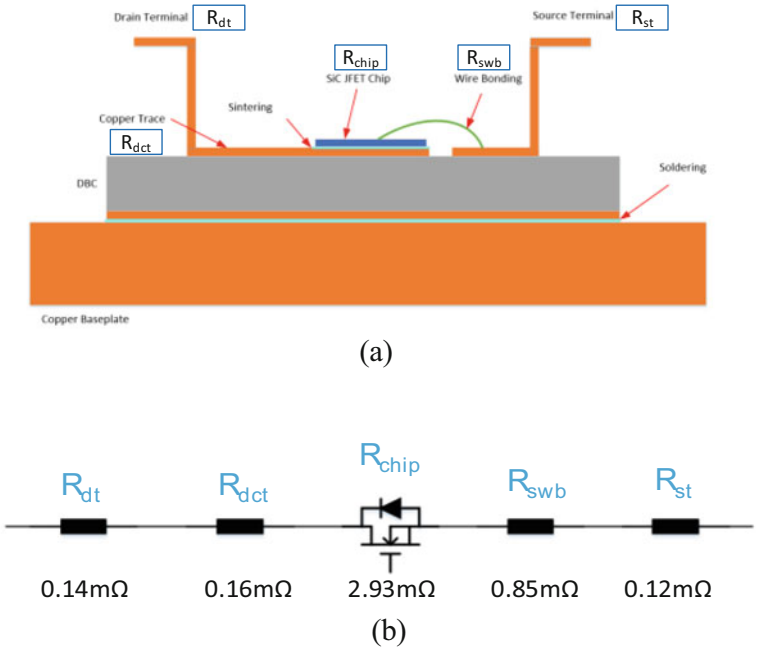


Fig. 3.22 The distribution of parasitic resistances of the fabricated SiC JFET module. (**a**) The constituent resistance of the SiC JFET package; (**b**) the measure value of the parasitic resistances [12]

to conventional mechanical breakers. For example, power losses for a typical electromechanical 250 A MCCB are around 5 W, while they are 5 times larger or more for a SSCB.

SiC power devices usually have small chip sizes and compact module design to reduce parasitic capacitances and inductances, which is beneficial for higher frequency operation in power converters. In addition, such modules can only be cooled through the baseplate, whereas in IGCTs the heat can be extracted from both sides. These pose an additional challenge in designing the cooling system that shall be able to manage higher heat flux. Heat pipes or vapor chambers can be used to distribute the heat over a larger heat sink. Figure 3.25 illustrates the cooling options for SSCBs, considering both the overall power to be dissipated and the heat flux across the heat exchange surface.

Thermal design is especially challenging when considering the overload condition. For example, in a standard Type C trip curves for electro-mechanical breakers, the breaker needs to withstand overload current, such as four times the nominal current ($4\times I_N$) for at least 1 s, $3\times I_N$ for 2 s and $2\times I_N$ for 6 s. During the overload conditions, significant amount of heat in SSCBs is generated, for example, under $4\times I_N$, at least $16\times$ more losses are generated and need to be dissipated effectively.

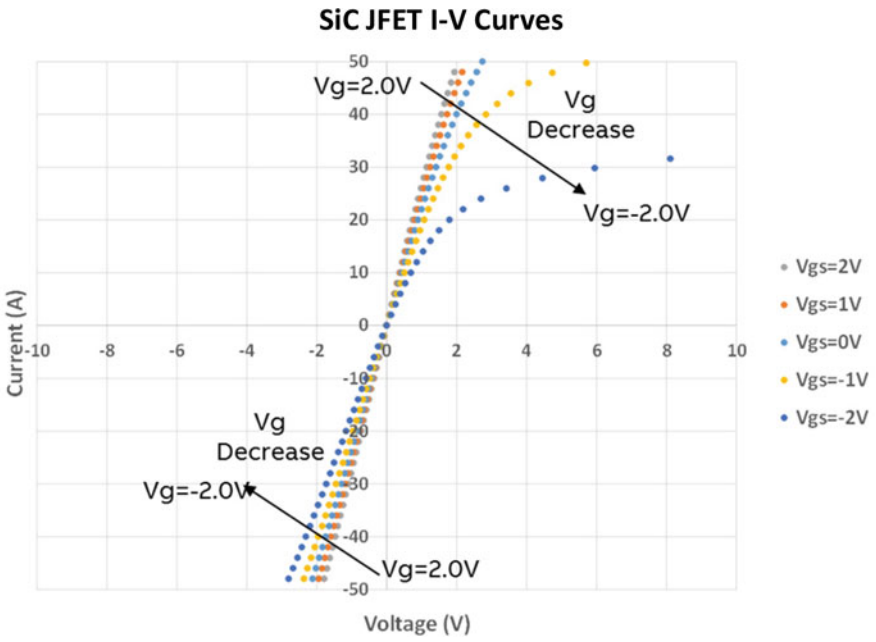
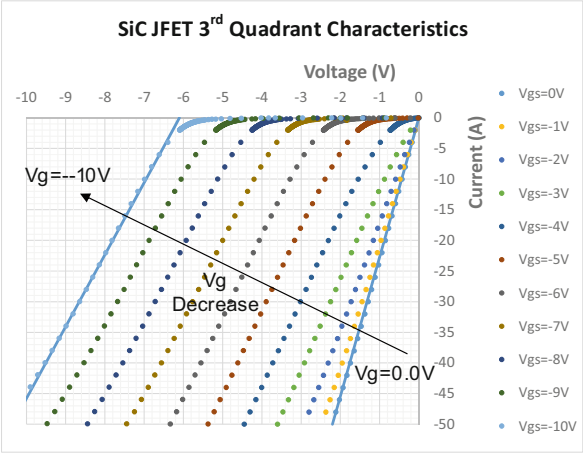


Fig. 3.23 Comparison of the SiC JFET forward conduction and reverse conduction characteristics with different gate voltages [13]

Fig. 3.24 SiC JFET reverse blocking characteristics with gate voltages varying from 0 V to −10 V [13]



(Gate threshold Voltage: -5V)

Different ways can be used to handle such overload conditions, like derating the semiconductor device adequately to lower the loss or optimizing the cooling system design (e.g., larger heat-sink sizes, liquid cooling instead of forced air convection, etc.). The first approach will lead to a significant cost increase due to the high prices

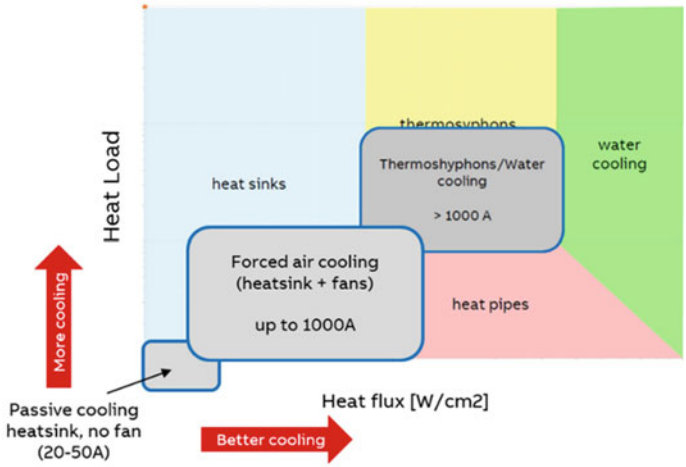


Fig. 3.25 Cooling options for solid-state circuit breakers

of semiconductor devices, whereas the second is more cost-effective in most cases. However, constraints from different applications need to be considered, such as form-factor, noise-levels, maintenance, etc., which can reduce design choices and the performance achievable from the thermal system.

One interesting method to address the large heat dissipation under overload conditions is the adoption of a phase-change material (PCM). The latent heat of the phase change process of the material allows it to absorb significant amount of energy for a relatively small change in temperature. This provides an increased thermal capacitance (lower transient thermal impedance) in the thermal network, which can help to reduce the case temperature and in turn, the junction temperature of the device. A material with phase-transition temperature slightly higher than the steady-state operating temperature of the breaker under nominal current shall be selected, to ensure that it is activated only when an overload occurs.

Figure 3.26 shows one design example of the PCM-based heat sink to address the overload conditions. In HS2, the PCM was filled at the bottom of the fins to provide less thermal resistance during normal conditions. Both HS1 and HS2 temperature rise quickly under the overload current. After the PCM in the HS2 is activated at ~50 °C, a slower temperature rise compared to the heat sink without PCM (HS1) can be found in Fig. 3.27. This is because PCM is adding thermal mass to the cooling system to provide greater system time constant and slow down the temperature rise to the thermal surge. The PCM performs as a reservoir to absorb the transient heat surge during overload, which can enhance the safety for the wide band-gap devices.

As shown in Fig. 3.27, the PCM takes portion of the heat sink fins and increases the thermal resistance of the network. The steady-state temperature of HS2 under overload current is higher than that of HS1. To avoid the temperature further rising,

Fig. 3.26 HS1 is the heat sink without any PCM, HS2 is the same heat sink with 1/3 fin filled with PCM [14]

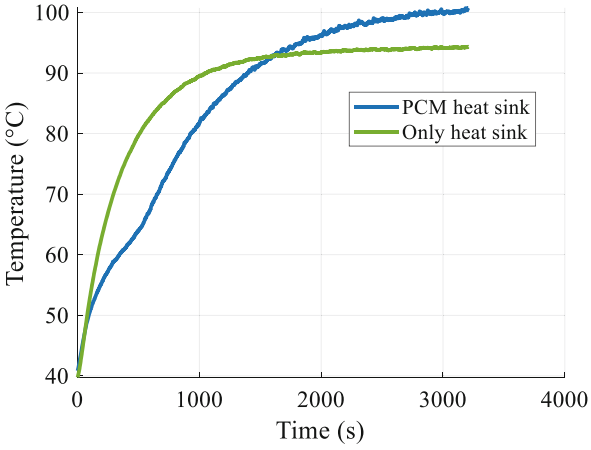


Fig. 3.27 Testing results for two heat sinks HS1 (only Heat Sink) and HS2 heat sink (filled with 1/3 PCM) under overload conditions [14]

the SSCB should interrupt the overload current promptly, and optimization of the PCM heat sink should be performed based on the overload conditions of the breaker.

4.5 Voltage Clamping Circuit Selection

Besides the power semiconductor devices and the affiliated cooling system, the voltage clamping circuit is also critical for SSCBs and HCBs. It has two functions: (a) to clamp the transient voltage across the power semiconductor devices and avoid over-voltage damage and (b) to absorb the residual energy left in the system parasitic inductances after semiconductor switches turn-off.

Different types of voltage clamping circuit can be used, including metal oxide varistors, transient voltage suppression diodes, snubber circuits, etc. In this section, those solutions are reviewed, and their advantages and limitations briefly summarized.

1.5mm x 3mm	7~25mm disc	60mm disc	60mm disc
Surface mount	Through hole	Press Pack	Screw Mount
< 120V V_{NDC}	< 1.2kV V_{NDC}	< 3.5kV V_{NDC}	< 3.5kV V_{NDC}
< 500A surge current	< 10kA surge current	< 70kA surge current	< 70kA surge current
< 2.5J absorb energy	< 480J absorb energy	< 10kJ absorb energy	< 10kJ absorb energy

Fig. 3.28 Overview of MOVs available on the market, in terms of size, DC nominal voltage range, maximum surge current, and maximum energy absorbing capability [15]

4.5.1 Metal Oxide Varistor (MOV)

Figure 3.28 shows an overview of the MOVs on the market, and it can be seen that MOVs have various package types (from small surface-mount to big screw-mount). The MOVs have advantages of wide voltage ranges (up to 3.5 kV DC operating voltage per device) and huge surge current or energy absorbing capabilities. Also, the MOV has bidirectional current/voltage capability and more cost-effective compared to other voltage clamping components, like TVS diodes.

During the SSCB current interruption phase within the MOV, a sharp voltage spike (V_{pk}) usually appears at the voltage waveform at the initial voltage clamping transient of the MOV. This peak of the voltage spike needs to be lower than the blocking voltage of the semiconductor device; otherwise, an overvoltage damage of the semiconductor device could happen. When the SSCB is in standby mode (semiconductor switch OFF and galvanic isolation switch closed), the MOV withstands the system DC bus voltage, generating some leakage current. The maximum system DC bus voltage the MOV can withstand is defined as its maximum operating voltage (V_{op}). The leakage current through the MOV needs to be low enough to avoid the overheat damage of the MOV due to too much losses generated. The leakage current also needs to meet the requirements from standards (e.g., UL 489I sets requirement for SSCB’s max leakage current in stand-by mode.)

One important index to evaluate the voltage clamping solution is the ratio between peak clamping voltage and maximum operating voltage (V_{pk}/V_{op}). Lower V_{pk}/V_{op} is preferred to achieve higher voltage utilization rate of the solid-state (SS) devices, and the SSCB can operate at a higher DC bus voltage for a certain voltage class of the semiconductor device (e.g., 1200 V). V_{pk}/V_{op} depends on the SSCB design and requirements, and on the MOV’s size. For example, a 20 mm disc MOV is tested with $V_{pk}/V_{op} = 1.61$ at 150A interruption current and a 10 mm disc MOV’s

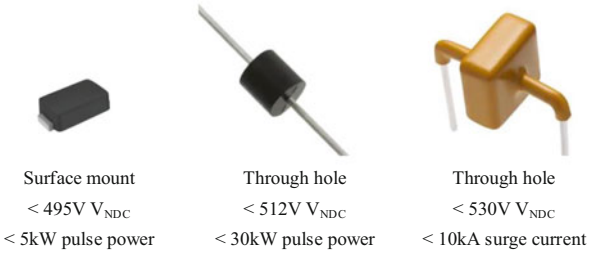


Fig. 3.29 Survey of TVS diodes in terms of package, maximum DC nominal voltage, maximum pulse power, or surge current capability [15]

$V_{pk}/V_{op} = 1.81$ at 120 A interruption current. In general V_{pk}/V_{op} for MOV is in the range 1.6 ~ 2.2.

To be noted that when selecting the MOV some voltage margin needs to be considered, because the semiconductor device could see higher voltage than the MOV's peak clamping voltage. When the current is commutating from the semiconductor device to MOV, the *di/dt* generates extra voltage drop across the loop inductance between the semiconductor device, which is also applied to the semiconductor devices.

4.5.2 Transient Voltage Suppression (TVS) Diode

Another commonly used voltage clamping solution is TVS diodes, which work like an avalanche diode but can achieve enhanced peak current and energy handling capability. Both unidirectional and bidirectional TVS diodes are available.

Figure 3.29 exhibits a few commercially available TVS diodes from one manufacturer. Compared to MOVs, TVS diodes have limited voltage range (<530 V for single device) and limited peak current capability (with only small surface-mount and through-hole package devices available). To achieve higher voltage rating or absorbing higher energy, the series connection or parallel connection of TVS diodes is needed. TVS diodes are also more expensive compared to MOV for similar absorbing energy and voltage requirements.

Figure 3.30 shows the TVS diode V-I trajectory during the voltage clamping process. One interesting phenomenon is noticed that after the TVS diode reaches a peak clamping voltage, its voltage drops to a level even lower than its nominal voltage [15]. For example, a 430 V nominal voltage TVS diode is tested and demonstrates ~540 V peak voltage, and then the voltage decreases to ~340 V (called static clamping voltage). The TVS diode's maximum DC operating voltage should be determined by its static clamping voltage (340 V), rather than its nominal voltage (430 V), and the V_{pk}/V_{op} ratio for the tested TVS diode is calculated as 540 V/340 V = ~1.59, which is slightly lower than MOVs. Some margin needs to be added when selecting the TVS diodes because of the parasitic loop inductances between the TVS diodes and the semiconductor devices.

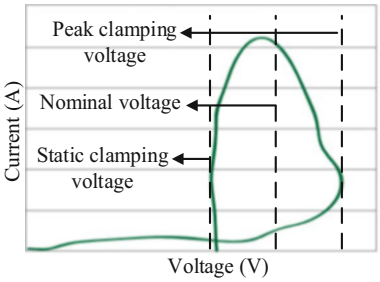


Fig. 3.30 TVS diode V-I trajectory during the voltage clamping process

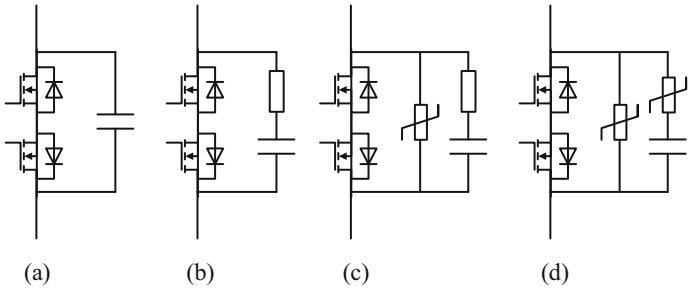


Fig. 3.31 Capacitor based clamping circuits: (**a**) only capacitor as snubber circuit; (**b**) RC based snubber circuit; (**c**) RC snubber in parallel with MOV; (**d**) MOV and capacitor in series based snubber circuit in parallel with another MOV [15]

4.5.3 Capacitor-Based Voltage Clamping Circuit

Capacitor-based snubber circuits are another option for voltage clamping in SSCBs. One beneficial feature of that solution is they control *dv*/*dt* at turn-off, reducing the turn-off stresses on the semiconductor device during fault current interruption.

Figure 3.31 shows some different types of snubber circuits. Capacitor-based snubbers in Fig. 3.31a are the simplest case, but they have the issue of current oscillations after turn off. To address this, more complex designs have been like the RC snubber (Fig. 3.31b), RCD snubber, etc., which can quickly suppress the oscillation by selecting the right damping resistors.

To reduce the size of the capacitor in the RC snubber, a MOV can be added in parallel as in Fig. 3.31c. The MOV has the function of absorbing the energy and clamping the voltage, while the RC snubber limits the turn-off *dv*/*dt*, increasing the current turn-off capability of the semiconductor device. A different solution, with the resistor replaced by a MOV as shown in Fig. 3.31d, was proposed in [16] to speed up the dampening of LC resonance. More details and comparison between the different snubber circuits can be found in [15, 16].

4.6 Design of the Gate Driver and the Protection Unit

The main requirement in designing the gate driver unit for SSCBs is that enough voltage must be provided to the gate of the power semiconductor device in order to turn-on or turn-off the current, ensuring the lowest on-state resistance and reliable current interruption. Different from the power electronics converters, fast-switching speed (e.g., high switching *dv*/*dt* and *di*/*dt*) is not crucial in SSCBs because of limited switching times, indeed sometimes a lower switching speed is preferred to reduce the overvoltage stress across the semiconductor switches.

The protection unit is intended to monitor the current and send out the tripping signal to the gate driver circuit when a fault occurs. In some cases, the characteristics of the power semiconductor devices (like the voltage drop) could be used for sensing the current, eliminating the need of additional current sensors and saving cost.

All the gate driver circuits, sense and trip electronics, etc. are powered by auxiliary power supplies, which usually need to be electrically isolated from the main power circuit.

In addition to the lower on-state resistance, because of their normally-on behavior SiC JFETs do not need auxiliary power supply when in conduction mode. However, they still need negative gate-source potential to turn off and stay off. Such behavior can be exploited to simplify the design of passive SSCBs not requiring isolated auxiliary power supply, sensors, and digital electronics, in which the power for turning off the JFET is drawn from the fault energy itself by means of a pick-up circuit. The design of the protection circuit for such SiC JFET-based SSCB is presented in this section.

Figure 3.32 shows the fundamental concept of a passive SSCB. The pick-up circuit shall be designed to draw enough power for the gate drivers in the different fault scenarios that can occur in DC circuits: overload, bolted (low impedance) short circuit (high *di*/*dt*), and high impedance short circuit (low *di*/*dt*).

The overload fault occurs when the load current increases above the nominal current value and stays there for extended period of time. This fault increases the losses and in terms the temperature of the elements that are carrying the fault current. To protect the system from this type of fault, a positive temperature coefficient (PTC) resistor is connected in series between two JFETs as shown in Fig. 3.32. The PTC resistor offers very low resistance during normal operation, up to the nominal current, but above nominal current the heat generated inside PTC increases its resistance. If the overload current lasts long enough, the PTC can become highly resistive (in the order of MΩ), causing a high voltage drop across the PTC. This voltage is usually more than enough to turn-off the power JFETs. Therefore, by using correct timing and gate driving circuit, the maximum voltage across PTC can be kept below the safe values, and the fault current can be interrupted.

In case of short circuit, the fault impedance affects the rate of the fault current increase (the *di*/*dt*). In low-impedance faults, the fault current can increase at rate as large as 100 A/μs or higher, whereas the rate can be of the order of 1 A/μs in high-

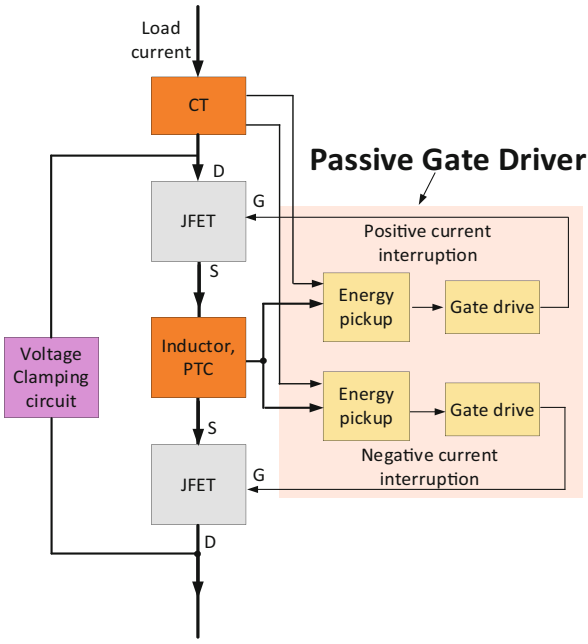


Fig. 3.32 Functional circuit block diagram of a SiC JFET-based SSCB with passive gate driver

impedance short circuits. Such different behaviors require different energy pick-up circuits.

To handle high *di/dt* faults, an inductor *L* is connected in series with the SiC JFETs to sense the fault. The voltage across the series inductor L can instantly achieve or exceed the required gate voltage to turn-off the fault current, and can directly be applied to the JFETs gate.

For low *di/dt* faults, as the voltage across the inductor L would be too low for turning-off the JFETs, a current transformer (CT) is added in the main current path. This current transformer produces no output in case of normal operation’s steady currents but during transient, such as high or low *di/dt* faults, it produces current in the secondary winding that is used to charge a capacitor and provide the voltage for the gate driver circuits.

Figure 3.33 shows the short circuit tripping curve of a SSCB prototype in which the CT is used to sense the low *di/dt* current from 0.15 to 0.8 A/μs, and the series-connected inductor *L* is designed to sense the high di/dt current from 0.8 A/μs and above. The short-circuit fault up to 9 A/μs *di/dt* is tested and validated.

The design of the pick-up circuit, the inductor, and the current transformer can be tuned to adjust the tripping curve in order to match the requirements, considering that the inductor and the CT are also part of the main circuit and can influence the overall system behavior, this can limit the flexibility.

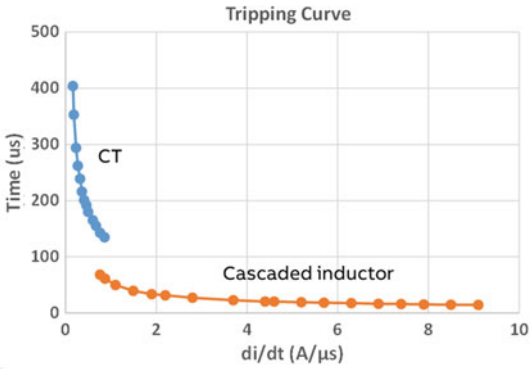


Fig. 3.33 Tripping curve (tripping time vs. *di/dt*) of the SiC JFET-based SSCB under short circuit faults

5 Application Cases for SSCBs

Tackling climate change is one of the key challenges of this century. To contain global warming within 1.5 °C above pre-industrial levels, society needs to cut net emissions to zero by 2050 latest.

This target can be achieved without dramatic social consequences only if the energy system is radically transformed. Fossil fuels that today power cities and industries shall be replaced with clean, decarbonized electricity from renewable sources, and energy wastes shall be minimized [17].

DC addresses all requirements of this energy transformation, but for its massive deployment some issues have to be solved, one of which is the need for fast and selective protection.

As DC grids typically have low inductance and resistance, and large capacitors at the DC bus terminals that contribute to fault currents, short-circuit faults can result in ultrafast transients with high currents that can cause severe damage to power electronic converters and sensitive loads. In addition, discharge of capacitors can result in voltage dips of the DC bus, with consequent temporary shutdown of the installation, which is not acceptable for most applications. Thus, advanced protection schemes that quickly identify faults and fast circuit breakers are needed, able to clear faults before the current reaches a dangerous level and the voltage drops below the shut-down value. Smart SSCBs perfectly fit this application [18]. This also confirms that the maximum admissible rate of rise of the current, i.e., the maximum *di/dt* of the fault current which a circuit breakers can interrupt, is the key performance parameter for SSCBs, more relevant than the maximal prospective current value typically used for conventional circuit breakers.

A large number of application cases for the DC grids of the future are explored in literature and by demonstration projects, and their maturity has been increasing and is still increasing significantly. The ease of integration of distributed generation from renewable sources, typically operating in DC, batteries and energy efficient loads (LED, VSDs, ...), together with other advantages makes DC fit very well with microgrids [19]. The efficiency of AC and DC power distribution in commercial

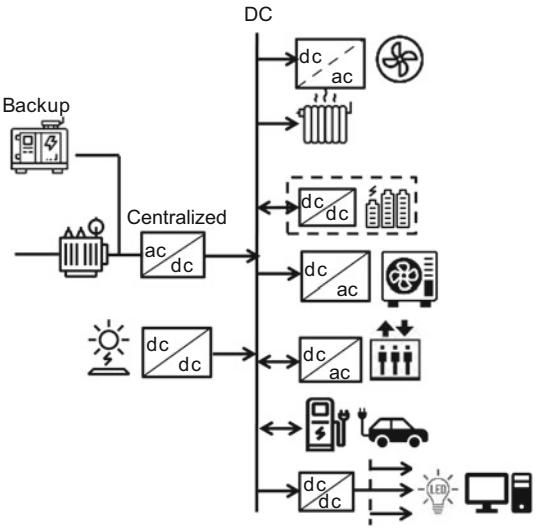


Fig. 3.34 DC microgrid for commercial and residential buildings

and residential buildings has been compared in several studies. DC is most likely to be more efficient in buildings with high local PV generation and storage capability, in which the energy being exchanged with the public AC grid is low [20], as the percentage of PV energy dissipated in conversion is lower because of the lower number of conversion stages [21] (Fig. 3.34).

The Current/OS foundation has been developing a set of rules for DC power distribution in multi-sources installations, including residential and commercial buildings, street-lighting, and EV-charging installations, with the intent of ensuring safety, reliability, and interoperability of equipment from different vendors. The rules have been validated in some pilot installations [25]. Current/OS rules require use of SSCBs to reduce short circuit current and energy, and risk of arc-flash and electric-shock in high-safety zones distributed in living spaces.

The German research project DC-Industrie has proven the feasibility of DC grids in industrial context that can potentially reduce the energy consumption by about 6–10% [22]. The saving mainly results from the ease of recovery of power from drives during braking that would be typically wasted in AC as regenerative drives are significantly more expensive. The DC-Industrie power distribution architecture consists of DC sectors, i.e., groups of DC components (loads, generators, or storage) forming a functional unit, connected to the DC bus through a solid-state circuit breaker (Fig. 3.35). Use of ultrafast solid-state circuit breaker is crucial to ensure reliable and selective protection, i.e., to avoid that a fault in a DC sector causes the shutdown of the plant.

DC power distribution has been gaining momentum in marine vessels, where the ABB’s Onboard DC Grid™ architecture has proven to enable fuel savings up to 27% [23, 24]. Here, as shown in Fig. 3.36, a bus tie breaker connects the two starboard and portside sections; this typically allows an optimal and redundant usage of the

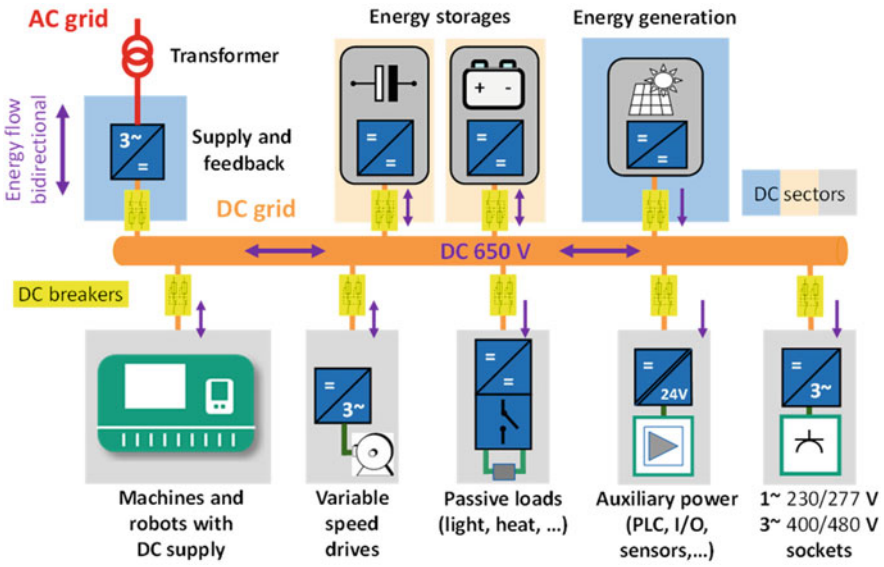


Fig. 3.35 Industrial DC microgrid according to DC-Industrie (© DC-INDUSTRIE & ZVEI) [26]

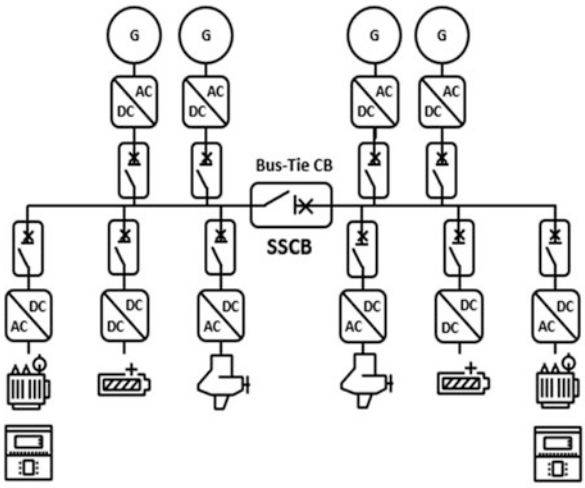


Fig. 3.36 Example of a DC distribution grid in a marine vessel with SSCB as bus-tie circuit breaker [27]

power generators. If a fault occurs, the sections must be protected by the circuit breaker to prevent a total outage and ensure service continuity by disconnection of the faulty section. In situations that are too challenging for traditional technology due to the high and fast rising (in milliseconds) short circuit currents in DC shipboard power systems, SSCB technology can excel. For example, SSCBs can quickly limit the fault current from generators and converter capacitors. SSCB can limit the short circuit currents to a few kA, avoiding damages to healthy sections

and unwanted trips especially of fuses, thus providing a supreme resilience to the system. In terms of system design, with a slower DCCB as the DC tie breaker, the generator capacity should be restricted to satisfy the fault tolerance of the converter and the DCCB. Fast DCCB, such as SSCB, is crucial to alleviate the design constraint of system capacity, and thus Onboard DC Grid™ is applicable to small and large vessels.

Improved LVDC protection by SSCB can be also a relevant enabler for cost-effective solutions for the integration of renewables in the existing AC grid. Energy storage systems are deployed for different use cases like frequency regulation or deferral of power line upgrades. In the case of large-scale battery energy storage systems (BESS) in the range of megawatt power (MW) and energy capacities of megawatthours (MWh), the (LV) battery banks are typically connected via a DC bus to an DC/AC bi-directional converter via a step-up transformer to the distribution or transmission grid. Depending on the use case, the energy storage needs to be sized in order to support from 15 min to 6 h of full converter power. But with larger energy storage size, i.e., with a larger number of battery banks, the short circuit current in case of faults can rise to couple of 100 kAs at very fast rise times. As traditional protection run there into the limits of technology performance, an upper limit for battery banks to a single converter is set. But for cost-effectiveness, the total installed converter power should not exceed the requirements of the point of common connection to the grid. The need which stems for this desired independent scaling of converter power and energy capacity, to create larger DC buses, can only be fulfilled if SSCBs are deployed for fault current protection.

Finally, for the integration of high-power electric vehicle infrastructure (EVCI) to the AC grid, the addition of energy storage systems is expected to become a must in many situations. Fleets of electric cars, light trucks, and buses which are used to supply cities and metropolitan areas will increase the stress on the distribution grids, especially at vehicle depots or in industrial zones. The DC coupling of such an energy storage system to the charger system will lead to challenges of short circuit handling as described before and of ensuring a high availability to keep operations running. The deployment of SSCB protection for this application seems to be as well very promising from the economical aspect.

Even though the adaption of DC offers a wide range of benefits for the integration of renewables, solid-state circuit breakers could be in principle also beneficial as retrofit in the AC distribution. One of the challenges of grid protection to future distribution grid protection with high penetration of DER (Distributed Energy Resource) is difficulty in protection coordination because of changing fault current levels and directions. The conventional AC distribution protection devices, such as fuses and reclosers, are no longer used and need to be upgraded to smart devices for intelligent protection algorithms to be deployed. This upgrade process will take huge efforts in money and time to be implemented. At the transitional stage of limited interconnection of DERs in distribution grid, an alternative solution could be to install SSCBs at the proper locations in distribution grids to allow fast interruption of fault contributions from these DERs. In this way, the original distribution protection scheme can still work, and a cost-effective solution, instead

of expensive upgrade of whole distribution protection, can temporarily solve the challenge to meet requirements of protection selectivity and coordination.

6 Concluding Remarks

Solid-state circuit breakers are not a drop-in replacement of the traditional electromechanical devices. Their ultrafast interruption is a key enabler for new DC power distribution models that can improve energy efficiency and ease integration of distributed energy resources. On the other hand, higher cost, larger footprint, due to the reuired cooling and air-gap isolation, and limited overload capacity make them less competitive for application in which electromechanical circuit breakers fit the job.

The different technical challenges that need to be addressed in the design of a SSCB have been briefly discussed in this chapter, starting from the selection of the power semiconductor device to the design of the cooling system and the voltage clamping circuit.

The power semiconductor device shall be selected in order to minimize conduction losses, whereas switching losses are obviously less relevant for this application. This means that devices optimized for power converters, in particular for mid-frequency applications, might not be optimal for SSCBs, and the other way round. Today, it seems there is not a device fitting the whole application spectrum. Silicon Reverse-blocking Integrated Gate-Commutated Thyristors (RB-IGCTs), offering low power losses at large currents (from several hundred Amps and larger), are the most effective solution for high power SSCBs, with rated currents in the range of kAs and rated voltage from 1 kV and up, but scaling down this technology for lower power SSCBs is difficult because of their non-linear behavior at low current. Silicon Carbide devices such as MOSFETs and JFETs seem a good fit for such smaller SSCBs due to the low on-state resistance. In particular, normally-on SiC JFETs offer the possibility to design passive SSCBs that nearly mimics the behavior of thermomagnetic CBs without the need of current sensors and digital control.

The design of the cooling system strongly impacts the SSCB footprint and the installation constraints. Whereas liquid cooling is typically required for high power converters and SSCBs based on IGBTs, having power losses of the order of several kW, with lower losses RB-IGCTs air-cooled SSCBs are possible, that are much simpler to install, by using dual-phase thermosyphons to displace the heat from the hot semiconductor device to a forced-air heat sink.

Thermal aspects during current interruption are also challenging, in particular in overload or short circuit. The cooling system in this case plays a minor role here, as turn-off is so short to be adiabatic. Differently from electromechanical circuit breakers, where the arc chamber combines the functions of switching off the current and dissipating the fault energy, in SSCBs the fault energy is dissipated through the clamping circuit. This makes Metal Oxide Varistors (MOVs) more suitable for SSCBs than snubbers typically used in power converters, as they have

much better dissipation capability. However, MOVs impose tough constraints on the power semiconductor device, as the SSCB’s maximum operational voltage shall not exceed 0.5–0.6 the blocking voltage of the semiconductor device, depending of the design; or, equivalently, the semiconductor device shall have a blocking voltage 1.6–2.2 times the system voltage. Such design constraints can be eased replacing MOVs with Transient Voltage Suppressing (TVS) diodes, but at the price of higher costs and much lower energy dissipation capability. Hybrid circuits including MOVs and other components offer an improved property mix, but are more complex.

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