Power Systems

Isik C. Kizilyalli
Z. John Shen
Daniel W. Cunningham *Editors*

Direct Current Fault Protection

Basic Concepts and Technology Advances

Springer

Power Systems

Electrical power has been the technological foundation of industrial societies for many years. Although the systems designed to provide and apply electrical energy have reached a high degree of maturity, unforeseen problems are constantly encountered, necessitating the design of more efficient and reliable systems based on novel technologies. The book series Power Systems is aimed at providing detailed, accurate and sound technical information about these new developments in electrical power engineering. It includes topics on power generation, storage and transmission as well as electrical machines. The monographs and advanced textbooks in this series address researchers, lecturers, industrial engineers and senior students in electrical engineering.

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Preface

Electricity, in its predominant form of alternating current (AC), is at the heart of modern civilization. However, direct current (DC) electricity is re-emerging, long after losing the *War of Currents* over a century ago. DC inherently offers higher transmission efficiency, better system stability, better match with modern electrical loads, and easier integration of renewable and storage resources than AC. DC power is gaining traction in high-voltage (HVDC) or medium-voltage (MVDC) grids, DC data centers, photovoltaic farms, electric vehicle charging infrastructures, shipboard, and aircraft power systems. However, fault protection must be provided that can simultaneously meet the efficiency, response time, lifetime, and cost requirements of the future DC grids.

The lack of effective DC fault protection technology remains a major barrier for the DC paradigm shift. Interruption of DC currents is extremely difficult due to the lack of current zero crossings which are naturally available in AC power systems. Intensive research has been conducted to address this critical need in the past 20 years. Numerous technical papers and patents have been published on the subject of solid-state and hybrid circuit breakers, including several comprehensive review or survey papers on different technical aspects of DC fault interruption techniques. However, no comprehensive book is available on this important technical topic. This book attempts to bridge this gap and cover the basic concepts and recent technology advances in the field of DC fault protection.

The book is organized in five parts with a total of 20 chapters contributed from the invited field experts around the world who are actively engaged in DC fault protection research and development. It is intended for researchers, engineers, and graduate students in the field of fault protection, DC power systems, power electronics, and power systems in general.

In *Part I—Introduction*, the readers are provided with a brief overview on DC power systems and DC fault protection technology. Chapter 1, "Introduction," highlights the benefits of DC power over conventional AC power and the emerging markets for DC power. Chapter 2, "Overview of Direct Current Fault Protection Technology," provides an overview of DC fault scenarios, fault detection, and fault interruption technologies. A new unified classification of various DC fault

interruption methods, including simple mechanical means, solid state circuit breaker (SSCB), hybrid circuit breaker (HCB), converter-based breakerless protection, and fault current limiter (FCL), are introduced, based on the fundamental topology and operation principle. Their advantages and disadvantages for different DC applications are discussed.

In *Part II—Solid State Circuit Breakers*, we include seven chapters to showcase different approaches and considerations in designing SSCBs.

Chapter 3, "ABB's Recent Advances in Solid-State Circuit Breakers," provides an overview of ABB's recent development of SSCBs based on Si IGCTs for kA/kV ratings, and lower power SSCBs based on SiC FETs. SSCB design considerations, such as power semiconductor device, gate drive circuit, cooling system, voltage clamping circuit, and protection control are discussed.

Chapter 4, "iBreaker: WBG-Based Tri-Mode Intelligent Solid-State Circuit Breaker," introduces a new class of intelligent SSCBs using wide-bandgap (WBG) semiconductors. The iBreaker concept explores the use of WBG switching devices in low-voltage (up to 1000 V), mΩ-resistance SSCB designs and new converter-based topologies and control techniques beyond the conventional ON/OFF operation to integrate intelligent functions. Two iBreaker design examples, one rated at 380 V/20 A and based on GaN switches for data center applications and the other rated at 750 V/250 A and based on SiC switches for hybrid electric aircraft applications, are discussed to highlight the iBreaker design methodology and functionality.

Chapter 5, "T-Type Modular DC Circuit Breaker (T-Breaker)," introduces a T-Breaker concept that has a scalable modular structure with locally integrated energy storage devices. It offers a strong capability in limiting fault current, high tolerance to control signal mismatch during breaking events, and ancillary functions including power flow control, power quality improvement, and transient stability enhancement.

Chapter 6, "Soft Turn-Off Capacitively Coupled SSCBs for MVDC Applications," discusses a capacitive coupled transient current commutation technique for designing SSCBs. Applying transient current commutation in SSCBs allows soft turn-off of the main semiconductor switch during DC current interruption. Eliminating the transient stress on the semiconductor switches and mitigating the gate voltage oscillations are two significant benefits, which help to enhance the long-term reliability and lifetime of the SSCBs.

Chapter 7, "Review of Z-Source Solid-State Circuit Breakers," provides a review on a special class of SSCBs using thyristors as the main static switch, the Z-source circuit breakers. Z-source SSCBs automatically respond to a fault without requiring fault sensing circuitry. The basic principle of operation is described, followed by popular design variations in the literature. Z-source breakers with coupled inductors are then illustrated. The incorporation of the Z-source breaker into power converters is also discussed. Examples of buck and boost converters with built-in Z-source breakers are presented.

Chapter 8, "Medium Voltage High Power Density Solid-State Circuit Breaker for Aviation Applications," presents the key design challenges for medium voltage

SSCBs related to hybrid electric aviation applications. The technical approaches to address such challenges, including extremely high specific power density, high efficiency, reliability, and high-altitude insulation capability, are explained in detail with a 2 kV/1.2 kA SSCB example design.

Chapter 9, "Light-Triggered Solid-State Circuit Breaker for DC Electrical Systems," by Sandia National Labs describes the design, simulation, and characterization of a novel SSCB approach using a light-triggered commutating switch combined with a cascaded normally-on WBG transistor circuit. Simulations of the various parts of the breaker and their predicted behavior in various system designs drives a first hardware demonstration. Circuit breaker voltage and current timing diagrams illustrate the interplay between different parts of the breaker to demonstrate sensitivity of the timing. The good match between measured performance and predicted behavior allows for realizing scaled up future designs.

In *Part III—Hybrid Circuit Breakers*, we include five chapters to illustrate different HCB schemes with vastly different operating principles.

Chapter 10, "ABB's Recent Advances on Hybrid DC Circuit Breakers," introduces two types of HCBs recently developed at ABB. The first type is a hybrid fault current limiting circuit breaker (FLCB) under the term PowerFul CB which naturally commutates the fault current from a mechanical breaker to a parallel semiconductor path. A current interruption capability of more than 11 kA at a DC voltage of 5 kV with an interruption time less than 2 ms is demonstrated. The second type is a low-voltage active resonant zero-crossing HCB that demonstrates a current interruption capability of 2000 A at a DC voltage of 1650 V with an interruption time of roughly 4 ms.

Chapter 11, "Hybrid Circuit Breakers with Transient Commutation Current Injection," introduces a 6 kV/1 kA HCB based on a power electronically modulated Transient Commutation Current Injection (TCCI) concept. The TCCI circuit in the parallel electronic path remains in a standby mode with near zero power loss under normal conditions but can rapidly generate a well-regulated counter current to force the fault current in the primary mechanical path to zero or near zero, and therefore facilitate current commutation from the mechanical to the electronic path. The TCCI circuit then ensures a near-zero voltage and a small high-frequency AC ripple current condition for the main mechanical contacts to separate without forming an arc. Exhibiting ultra-low on-state resistance by virtue of having no semiconductors in the primary current path, the topology achieves minimal on-state losses and greater than 99.97% efficiency. The HCB design also employs a specially designed high-speed actuator/vacuum contactor combination enabling sub-millisecond interruption as well as a modular MVDC power electronic interrupter (PEI) design in the electronic path.

Chapter 12, "Efficient DC Interrupter with Surge Protection (EDISON)," introduces another HCB design based on counter current injection. EDISON consists of multiple submodules of IGBTs and MOVs, a fault current commutation circuit (FC3), and a fast mechanical switch (FMS) which is controlled by a piezoelectric actuator. Supercritical CO_2 is used as the switching medium to enable high dielectric strength at unprecedented short contact travel, combined with outstanding heat

transfer and low viscosity. Furthermore, EDISON introduces a new topology with no semiconductors in the main current path. Commutation of the current to the fault current commutation branch is achieved by the FC3 voltage source, which substantially reduces steady-state losses.

Chapter 13, "535 kV/25 kA Hybrid Circuit Breaker Development," introduces a 535 kV/25 kA active resonant-type HCB developed by Tsinghua University for the Zhangbei flexible DC transmission project in China, one with the highest voltage and power ratings ever reported. All subsystems of the HCB are described and key technical issues are analyzed. Testing and field deployment of the HCB engineering prototype are discussed.

Chapter 14, "Ultra-Fast Resonant Hybrid DC Circuit Breaker," introduces another active resonant-type HCB for MVDC applications. The HCB uses a resonant current source made of a power electronic H-bridge in series with a resonant inductor capacitor tank to generate artificial current zero crossings in the mechanical switch.

In *Part IV—Other Fault Protection Topics*, we include four chapters to cover several important topics related to DC fault protection.

Chapter 15, "Gas Discharge Tubes for Power Grid Applications," provides an overview on the potential benefits of gas discharge tube switches and circuit breakers as an enabling technology for medium- to high-voltage direct current power systems. High-voltage, high-power gas tubes are a recent development in a long line of proven gaseous electronic devices for power conversion and transmission systems that include thyratrons and mercury-arc rectifiers and valves. In their present state of development, they are best suited for high-voltage (up to 500 kV), moderate-current (up to 1000 A) applications. Electrical opening and closing times are both fast (<5 μs) and the devices are compact and amenable to high-temperature operation. The device capabilities and critical design criteria are discussed. The key technical challenges to make gas tubes viable in various electric power system applications are also outlined.

Chapter 16, "Converter-Based Breakerless DC Fault Protection," provides a brief overview of breakerless fault protection based on different converter topologies and control techniques. A breakerless MVDC architecture for a shipboard power system is also introduced and the advantages of the breakerless approach are discussed. A comparison between the breaker-based and breakerless approaches is discussed.

Chapter 17, "DC Fault Current Limiters and Their Applications," provides a brief overview of DC fault current limiters (FCLs), including directly installed DC reactors, superconducting FCL, and power electronic FCL. The technical requirements of FCL as well as the parameter configuration methods are analyzed in detail. A classification of these FCL methods based on fundamental topology and operation principle is introduced with an extensive reference list.

Chapter 18, "Eliminating SF_6 from Switchgear," provides a brief overview of SF_6 use in medium- and high-voltage gas-insulated electrical equipment and the outsized environmental impact of SF_6 as the worst greenhouse gas for global warming that has prompted a decades-long search for alternative gases and gas mixtures.

In *Part V—Future Outlook*, we include two chapters which provide a technical and economic future outlook of DC fault protection and MVDC power systems.

Chapter 19, "Fundamental Challenges and Future Outlook," outlines the fundamental challenges in the existing SSCB and HCB solutions. Conventional SSCBs use transistors in an undesirable way—continuously dissipating power except during infrequent fault interruption throughout their service life. Conventional HCBs offer a relatively long interruption time that is limited by the finite amount of force applied to the mechanical contacts. Innovative solutions are needed to overcome these fundamental limitations for future DC grids. This chapter introduces a new series-type hybrid circuit breaker (S-HCB) concept as an example to stimulate other new fault interruption ideas. The S-HCB conducts its load current through metal wires instead of semiconductor switches and curtails its fault current to near zero throughout the entire opening process of a series mechanical switch. It offers the low on-resistance of conventional mechanical contacts for normal operation and μs-scale fault interruption speed which is even faster than the fast-acting SSCBs.

Chapter 20, "Techno-Economic Aspect and Commercialization of MVDC Power Systems," covers a study of the medium-voltage direct current (MVDC) market, including the value proposition, market and segment opportunities, channels and barriers to entry, and speed of adoption. A variety of existing and promising MVDC markets are evaluated in renewable energy generation (PV and wind), grid distribution including emerging microgrid systems, transportation domains as well as commercial and industrial sectors. A regulatory framework is introduced, with guidelines and standards that will help shape emerging MVDC markets.

This is the first book that comprehensively covers the basic concepts and recent technology advances in the field of DC fault protection. Our goal is to help the readers quickly learn the state of the art of DC fault protection, appreciate the distinct advantages and disadvantages of different technical approaches in terms of efficiency, speed, complexity, lifetime, and cost for different voltage and current ranges, and inspire new innovations. We believe that this book will provide useful information to researchers in both academia and industry.

Finally, we would like to express our gratitude to all the chapter contributors. This book would not be possible without their devoted efforts. This book was inspired by the exemplary work performed by researchers supported through ARPA-E's CIRCUITS Program and later the BREAKERS Program, the latter focusing exclusively on novel MVDC circuit breaker technologies. We would also like to thank the staff at Springer, in particular Michael McCabe and Olivia Ramya Chitranjan, for their help and support.

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About the Editors

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Part I
Introduction

Chapter 1
Introduction

Isik C. Kizilyalli, Daniel W. Cunningham, and Z. John Shen

Electricity delivered by alternating current (AC) has a long and colorful history [1]. This method, which alternates the flow of electricity back and forth many times per second, has dominated the transmission and distribution system in the world for over a century. AC proliferation has been driven by the ease and lower cost of voltage conversion as compared to direct current (DC). However, DC electric power offers several benefits over AC, reducing system power losses due to improved electrical conductivity and utilizing fewer power cables with higher power carrying capacity (as shown in Table 1.1) [2, 3]. In addition, controlling of DC electric power could be easier since frequency and phase synchronization requirements are eliminated.

There are a few examples of high voltage DC transmission projects around the world, which boast lower costs and a smaller physical footprint by avoiding additional power conversion equipment while supporting higher transmission efficiency. At lower voltages (i.e., <1 kV), simpler controls and fewer conversion stages have made DC microgrids an appealing option for datacenters, industrial facilities, and office blocks [4]. This is due to the fact many of the services commonly connected to microgrids, such as energy storage, renewables, electric vehicle charging, and consumer devices, all operate on DC platforms.

There is a tremendous opportunity to extend the benefits of DC power to medium voltage (MV) markets, particularly in electric grid distribution (i.e., 3.3–100 kV) where MVDC provides several promising characteristics in the same way that HVDC does for high voltage grid transmission. DC has improved efficiency due

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Table 1.1 Transmission benefits of DC versus AC

	DC	AC
Overhead line loss[a]	3.5%	6.7%
Cables required	2	3
Power capacity[b]	1.4	1

[a]Per 1000 km
[b]For the same wire size and insulation as AC

to a lack of reactive power losses, skin effects, and corona losses. DC also exhibits greater power delivery capacities compared to AC. The effective value of AC current and voltage has a root mean square (RMS) relationship, which is approximately 70% of peak. Since AC distribution cables still need to be sized for peak current, this creates an inherent benefit via greater power delivery with the same sized DC cable or line. Expansion of MVDC distribution would make connecting a growing portfolio of DC energy consumers and producers much less complex since the distribution systems are connecting to an increasingly DC world: 50% of electricity runs through DC devices today [5]. Currently DC networks are typically a collection of point-to-point interconnections, but a multi-point DC mesh network would allow for greater diversification of generation, frequency response, and energy arbitrage and would increase grid resiliency. As the MVDC market matures, meshed DC distribution and large-scale grid integration of renewables and storage are expected to grow, driven by higher efficiency and flexible system operation.

There remains, however, a significant technology gap in the safety and protection mechanisms required to mitigate potentially damaging faults in MVDC systems. Circuit breakers, current limiters, and fault detection mechanisms are essential to grid resiliency in a number of ways: sectioning the grid during a fault; preventing damage to wiring, power electronics, and other important assets; and restoring power to the grid after a fault is cleared. Since, unlike AC, DC does not exhibit natural current zero-crossings (the result of alternating the flow of electricity back and forth), novel methods for fault isolation have to be developed to safely bring the fault current to zero [6].

In addition, the fast reduction of current (di/dt) needed to mitigate the potentially damaging arc in DC circuits can eventually create a large overvoltage (V) in the system, especially when the inductance (L) of the load is large [7]. This risk is largely avoided for AC systems, since transformers and generators can handle high fault currents (20×–40× nominal current) for much longer periods of time (>100 ms), which minimizes the associated overvoltage. Three main types of circuit breakers are being used in the LVDC and HVDC markets: mechanical circuit breakers (MCBs), solid-state circuit breakers (SSCBs), and hybrid circuit breakers (HCBs). All circuit breakers feature a parallel surge arrestor, typically a metal oxide varistor (MOV), to conduct and absorb any residual energy stored in the line inductance after a fault, if needed [8, 9].

MCBs use a mechanical switch in combination with an arc interruption mechanism (e.g., vacuum, SF_6, oil) to clear faults. MCBs feature low on-state resistance

and power losses (<0.01% loss), but suffer from lifetime concerns due to arcing and, at least historically, slow switching speeds. In addition, MCBs are limited up to 3 kV applications due to technical challenges in breaking high voltage arcs without a zero-crossing. Since switching speeds and arc elimination are lower risk for AC systems, MCBs are used for AC circuit breakers [8, 9]. SSCBs use semiconductor devices, including integrated gate-commutated thyristors (IGCTs) and integrated insulated-gate bipolar transistors (IGBTs), as the switching medium. SSCBs do not generate arcs and have much faster switching speeds in the range of <100 μs, leading to lower maximum fault currents [8]. This makes them ideal for applications where the circuit breakers are located in close proximity to the equipment being protected, e.g., in electric vehicle battery packs [10]. However, the high on-state conduction losses (>0.3% conduction loss, up to 30% of the losses of a voltage source converter station [11]) and capital costs are the main drawbacks for this technology. Conduction losses are due to the on-state device resistance. These losses result in a significant amount of heat generation, and a cooling system (either liquid or air) is often required to prevent overheating and ensure semiconductor stability [12]. HCBs are capable of delivering fast switching speeds (response times of <2 ms), while still keeping power losses low (<0.01% loss). HCBs typically have three parallel branches: a normal, low on-resistance operation branch which contains a load commutation switch and mechanical switch; a main breaker branch which is formed by stacking several semiconductor switches; and an energy dissipation branch which typically consists of surge arresters. When a fault occurs, the commutation switch shifts the current to the main breaker. The mechanical switch will open under zero current once the current has been completely commutated, thus avoiding arc creation. Then the main breaker will be turned off, and the remaining fault current will be dissipated by the surge arresters. Table 1.2 provides a comparison summary among all three types of DC circuit breakers based on five key performance metrics. Since there is no clear winner, it becomes a tradeoff in selections based on applications. Typically for low voltage applications, we see MCBs being used while in high voltage applications both

Table 1.2 Tradeoffs between all DC circuit breaker types

	Mechanical circuit breaker	Solid state circuit breaker	Hybrid circuit breaker	Ideal Mvdc circuit breaker
Efficiency	✓	✗	✓	✓
Response time	✗	✓	✗	✓
Scalability (voltage)	✗	✓	✓	✓
Cost	✓	✗	✗	✓
Lifetime	✗	✓	✓	✓

SSCBs and HCBs are selected. Interestingly, for MV applications, all five key metrics are critical enough that the selection of breaker types becomes even more challenging.

The challenge of leveraging HVDC or LVDC for MVDC circuit breakers is as follows. The complexity of existing HVDC circuit breakers (HCB or SSCB), driven by a large number of semiconductor devices and associated cooling infrastructure, makes it difficult to scale down to MVDC levels without substantial compromises in operational efficiency and cost. Conversely, scaling up from LVDC (conventionally MCB) to MVDC is also difficult because of arcing concerns: at higher voltage levels, arcing becomes a significant hazard. As a result, development in MVDC circuit breaker technologies (and MVDC distribution applications) has been challenging. Currently, MVDC circuit breakers are only available for lower voltage (<3 kV), low power (<3 MW) applications, and are primarily limited to the rail sector [13–16].

While circuit protection protocols in AC systems are very advanced, with IEEE standards implemented for many grid, ship, and rail systems, there is minimal commercially available products and limited documentation to define the performance requirements for MVDC circuit breakers. To bridge this gap metrics were established in the ARPA-E Building Reliable Electronics to Achieve Kilovolt Effective Ratings Safely (BREAKERS) program [17] shown in Table 1.3.

In order to enable circuit protection for MVDC applications in renewable collection, offshore oil and gas distribution, electrification of transportation, high energy physics, nuclear fusion, and other applications, the metrics in BREAKERS program targeted medium voltage circuit breakers rated between 1 and 100 kV, with instantaneous power levels between 1 and 200 MW. Circuit breaker efficiencies above 99.97%, through low conduction losses, are currently realized in HCBs at LVDC and HVDC levels, but have not yet been delivered for MVDC applications. A fast response time, where the response time is defined as the instant from when the breaker receives the trip order to the instant when the current has been lowered to approximately zero, limits the maximum fault current protecting DC power conversion and equipment, and enables fast electricity recovery. Combining low loss with aggressive circuit breaker response times would lead to advances in

Table 1.3 BREAKERS program technical metrics

ID	Category	Target
1.1	Rated voltage	1 kV DC $\geq$ V $\geq$ 100 kV DC
1.2	Rated power[a]	$\geq$1 MW
1.3	Efficiency	$\geq$99.97%
1.4	Response time	$\leq$500 μs
1.5	Lifetime	$\geq$30,000 cycles, $\geq$30 years
1.6	Nuisance trips	$\leq$0.1%
1.7	Power density[a]	$\geq$60 MW/m^3
1.8	Cooling	Passive or forced air[b]

[a]Instantaneous power

[b]Power consumed for any active cooling must be included while measuring breaker efficiency

circuit breaker design with application to existing LVDC and HVDC applications as well. Targets for nuisance trips were included to increase circuit breaker reliability and lifetime. Nuisance trips are unwarranted circuit breaker trips with either no electrically based reason for the trips, or, the breaker deems there to be a fault when one does not exist. Faster fault detection mechanisms could lead to a greater percentage of nuisance trips, resulting in unnecessary outages and avoidable situations. Finally, as medium voltage becomes more popular in the transportation sector and for off-shore applications, circuit breaker size and volume will become important factors in the design. Therefore, power density should be maximized to deliver a compact and modular product for these applications. The requirement for utilization of passive or forced air cooling for heat dissipation is from the fact cooling water is generally not available where MVDC circuit breakers would be installed. Additionally, it pushes innovations in thermal management and packaging that can reduce system-level weight, complexity, and cost in transportation and stationary applications relative to liquid cooled systems.

In summary, there is a significant technology gap in the safety and protection mechanisms required to mitigate potentially damaging faults in DC systems. This lingering risk of electrical fault scenarios (e.g., shorts and overloads) remains a primary hurdle preventing the growth of DC markets. In AC networks, electricity alternates direction periodically, naturally providing a "zero crossing" where no current flows, which allows electrical faults to easily be extinguished. DC networks, on the other hand, deliver power without zero crossings, which greatly increases the likelihood of electrical arcs in conventional circuit breakers, making them useless in fault scenarios. Advances in MVDC safety and protection hardware will create an opportunity for greater use of DC on the electric grid enabling significant efficiency improvements. This will transform how electricity is delivered and managed across the entire power grid from generation to the end user resulting in improved capacity and greater grid resiliency. Furthermore, other MVDC applications, such as subsea oil and gas production, offshore wind, and nuclear fusion, will derive from the emergence of safe and reliable electrical DC power networks.

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Chapter 2
Overview of Direct Current Fault Protection Technology

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1 Introduction

Fault protection remains a major obstacle for the widespread adoption of inherently advantageous DC power in applications ranging from high-voltage DC (HVDC) transmission to medium-voltage DC (MVDC) and low-voltage DC (LVDC) distribution. DC fault protection is critically important for the reliable operation of these DC power systems and generally comprises the detection, location, interruption, and isolation of short circuit faults of pole-to-pole (P-P) and pole-to-ground (P-G) types. A pole-to-pole fault occurs when the positive and negative power lines are shorted and typically exhibits a low short circuit impedance. It is the most severe fault type in DC power networks and often introduces an exceedingly high fault current within a very short time period. A pole-to-ground fault occurs when either the positive or negative power line is shorted to ground, often caused by lightning and component failure. The impact of a P-G fault depends on the specific grounding scheme used by the DC power system and can be harmful too. Other DC fault types, such as high-impedance ground and arc faults, although of importance, are not discussed in this book because of their relatively low fault current level in comparison to short circuit faults.

While HVDC technologies have been increasingly adopted by the utility industry, MVDC and LVDC are still limited to only a few special applications despite the advantages they offer. Like in any AC grid, a fundamental requirement for a DC grid

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is the ability to interrupt the fault current and isolate the faulty part from the rest of the network. To minimize disruption to grid operation, it is critically important to offer DC protection schemes that can detect, discriminate, and isolate DC faults at high speeds with full selectivity. Furthermore, global DC protection standards and guidelines need to be developed to facilitate the widespread adoption of DC power systems.

Fault interruption is arguably the most important and challenging aspect of DC fault protection. DC fault interruption techniques, such as DC circuit breakers, must isolate a short circuit fault quickly and selectively in conjunction with DC fault detection and location techniques. Because of the absence of natural zero current crossing and the low reactance nature of DC grids, it is much more difficult to develop cost-effective and reliable fault interruption solutions for DC systems than traditional AC systems. Furthermore, modern DC power systems generally comprise a large number of semiconductor-based power electronic converters which offer limited fault ride-through capability. For example, commonly used IGBTs (Insulated Gate Bipolar Transistors) can only withstand a short circuit current of 3–4 times the nominal rating for no more than 10 μs. In comparison, AC transformers and switchgears using bulky copper and iron elements can sustain a short circuit current of 30–40 times the nominal rating for more than hundreds of milliseconds. This huge difference in electro-thermal capacity mandates a much faster fault interruption in emerging DC grids than traditional AC grids.

Numerous technical papers and patents have been published on various types of DC fault interruption techniques in the past two decades, truly reflecting the high interest level on the subject from industry and academia alike. Several survey papers are already available to offer excellent reviews on different aspects of DC fault interruption, including fault protection in MVDC and LVDC [1–6] and HVDC [7–10] power systems, solid-state circuit breakers (SSCBs) [11], thyristor-based SSCBs [12–14], hybrid circuit breakers (HCBs) [15], fault current limiters (FCLs) [16], and converter-based breakerless fault protection [17]. However, these survey or review papers tend to cover technical publications under a specific category and/or focus on the detailed technical features or subsystems. There is considerable inconsistency in the use of technical terms, definitions, or classifications among the authors. Thus, there is a need for a high-level comprehensive and comparative overview and unified classification of all relevant DC fault interruption techniques based on fundamental topology and operation principle beyond secondary implementation details. The inherent strengths and weaknesses of the major fault interruption techniques need to be compared and evaluated objectively for a wide range of DC power applications beyond the claims in the original publications.

This chapter intends to bridge this gap by providing a unified classification and comparison of most, if not all the DC fault interruption technologies in the literature after a brief review on DC fault current analysis. The purpose is to help the readers quickly learn about the exciting but sometimes confusing research field of DC fault protection and appreciate the inherent advantages and disadvantages of each approach in comparison to other competing solutions in terms of efficiency, speed, complexity, lifetime, and cost for different voltage and current ratings. While this

chapter cites some of the most important and/or representative publications on the fault protection concepts in its reference list, the readers are encouraged to find more comprehensive reference lists in the review or survey papers [1–17].

2 DC Fault Current Analysis

Understanding and analyzing short circuit fault currents is the first step of formulating an appropriate fault protection strategy. A DC fault current typically comprises two parts: an initial capacitive discharge transient current and a subsequent static fault current supplied by the power sources. Figure 2.1 shows a DC system in a ring configuration. At faults, the DC system has fault currents from the AC sources and DC sources, namely, AC synchronous generators, induction motors, batteries, and converter capacitors. The fault currents from various AC and DC sources collectively define fault characteristics, such as fault peak and time constants. Ultimately, the DC fault features determine DC protection design requirements on protection devices, fault detection and location methods, and protection coordination.

Different types of fault sources and their corresponding DC fault current calculation are summarized as follows.

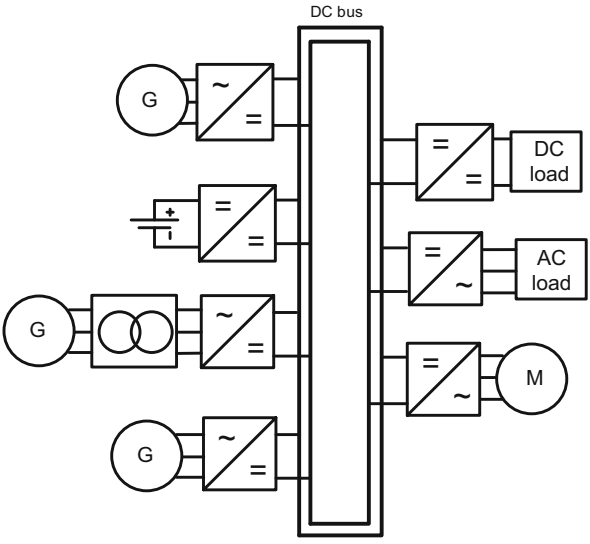

Fig. 2.1 A notional DC power system in a ring configuration

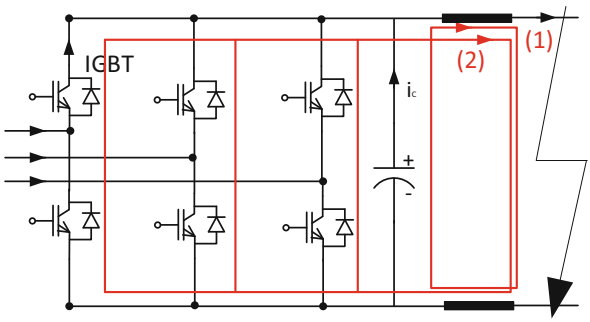

Fig. 2.2 Fault current paths of the capacitor of a two-level AC/DC rectifier [19]

2.1 Fault Current from Capacitors

Converters are used widely in DC systems. Converter capacitors not only provide energy reservoir for the power flowing out of converters but also smooth DC system voltage. At DC faults, the converter capacitor discharging is uncontrollable and could contribute high fault currents within a few microseconds. The capacitor discharging can lead to system wide undervoltage tripping of equipment. The high discharging current may also cause mechanical damages to equipment because of high electromagnetic stress.

Besides power supply interruption and mechanical damages, the rapidly increasing capacitor discharging current may also damage converter semiconductors. Figure 2.2 illustrates two stages of DC fault current development of a two-level AC/DC rectifier and their corresponding fault paths. At the first stage, the DC fault current appears as the capacitor discharging current to the fault location in fault path (2.1). Once the capacitor voltage reaches zero, the converter diodes turn on. At the second stage, the DC fault current flows through the freewheeling diodes of the rectifier as indicated by fault path (2.2). Figure 2.3 shows the fault current paths of a boost converter. Similarly, the capacitor first discharges at a DC fault according to fault current path (2.1); then, the fault current flow through the freewheeling diodes of the boost converter in fault current path (2.2). In both Figs. 2.2 and 2.3, if the distance between the converter to the fault location is short, the capacitor voltage quickly drops to zero and, at the same time, the DC fault current already increases to a very high value when the fault currents start to flow through the converter. Therefore, the high fault current may destroy the freewheeling diodes due to the violation of their thermal limits. If this thermal violation is foreseen, the converter design should avoid this damage, which normally requires oversize of the converter and thus results in some increase in capital cost. Similar fault paths exist in a conventional buck converter. However, the fault current through the diodes is limited by the buck converter output filter, and thus the risk of thermal violation of the diodes is much reduced.

Depending on the relationship between the discharging resistance R, inductance L, and capacitance C, the capacitor discharging current i_{cap} can be either a DC

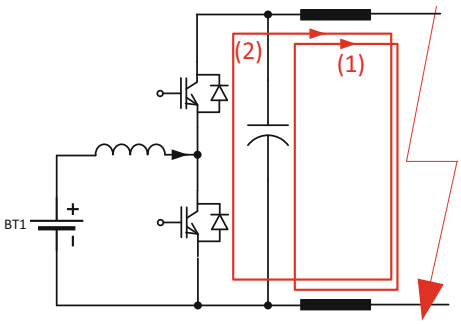

Fig. 2.3 Fault current paths of the capacitor of a boost converter [19]

current calculated by (2.1) or a decaying AC oscillating current calculated by (2.2). V_0 is the capacitor voltage before the discharging. The capacitor voltage v_{cap} can be calculated from (2.3) and (2.4). To avoid the undervoltage tripping, the DC fault should be interrupted before the capacitor voltage drops below its undervoltage threshold. If the capacitor voltage is allowed to drop to zero, to avoid possible damages to the converter freewheeling diodes, the fault current should be interrupted before the thermal limits of the diodes are reached. For the oscillating capacitor discharging current, the DC voltage drops to zero at time equal to $\frac{\pi-\beta}{\omega}$ according to (2.4). The freewheeling diodes start conducting at this moment, and the DC fault i_f can be estimated by (2.5). It starts from the capacitor discharging current value derived from (2.2) at time equal to $\frac{\pi-\beta}{\omega}$ and decays with time constant τ, which is the ratio between the total inductance and resistance on the fault path (2.2). Assuming exactly same freewheeling diodes, the total resistance includes two thirds of each diode's on-state resistance and the diodes of each phase take one third of the total DC fault current. In real systems, if the capacitor voltage is allowed to be negative, the commutation process is complex, and the accurate diode current waveforms can be obtained from detailed time domain simulations.

$$i_{\text{cap}}(t) = \frac{1}{L}\frac{V_0}{p_1 -' p_2}\left(e^{p_1 t} - e^{p_2 t}\right), \quad \text{if} \quad R > 2\sqrt{\frac{L}{C}}. \tag{2.1}$$

$$i_{\text{cap}}(t) = \frac{V_0}{\omega L} e^{-\delta t} \sin(\omega t), \quad \text{if} \quad R \leq 2\sqrt{\frac{L}{C}}. \tag{2.2}$$

$$v_{\text{cap}}(t) = \frac{1}{LC}\frac{V_0}{p_1 -' p_2}\left(\frac{1}{p_1}e^{p_1 t} - \frac{1}{p_2}e^{p_2 t}\right), \quad \text{if} \quad R > 2\sqrt{\frac{L}{C}}. \tag{2.3}$$

$$v_{\text{cap}}(t) = \frac{V_0 \omega_0}{\omega} e^{-\delta t} \sin(\omega t + \beta), \quad \text{if} \quad R \leq 2\sqrt{\frac{L}{C}}. \tag{2.4}$$

$$i_f(t) = i_{\text{cap}} \left(\frac{\pi - \beta}{\omega} \right) e^{-\left(t - \frac{\pi-\beta}{\omega}\right)/\tau}, t > \frac{\pi - \beta}{\omega}. \tag{2.5}$$

where $\omega_0 = \frac{1}{\sqrt{LC}}$, $\delta = \frac{R}{2L}$, $\omega = \sqrt{\omega_0^2 - \delta^2}$, $p_{1,2} = -\delta \pm \sqrt{\delta^2 - \omega_0^2}$, $\beta = \arctan \frac{\omega}{\delta}$.

2.2 *Fault Current from Batteries*

Batteries can contribute DC fault currents unrestrictedly through conventional DC/DC boost converters or directly to fault locations. Figure 2.4 illustrates the fault current path of a battery contributing through the freewheeling diode of a conventional boost converter. The battery DC fault current can rise to a high value within a few milliseconds, which can cause damages to the power devices and equipment on the path.

The battery DC fault current i_{Batt} rises to its peak and steady state after a transient process as indicated in (2.6). The steady-state fault magnitude is determined by battery voltage V_{Batt} and its fault resistance R. The fault current rising time constant τ is the ratio of the fault inductance L to R. Conventionally, at three times of its rising time constant, the fault current is considered to rise to a value close to ~95% of its peak value.

$$i_{\text{Batt}}(t) = \frac{V_{\text{Batt}}}{R} \left(1 - e^{-t/\tau}\right) \tag{2.6}$$

where $\tau = \frac{L}{R}$.

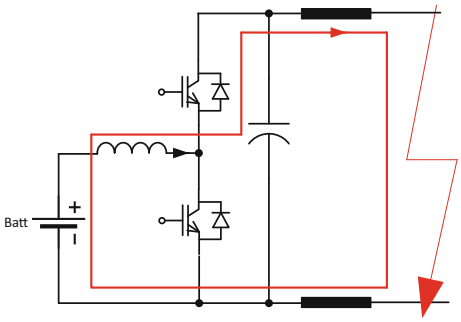

Fig. 2.4 Fault current path of a battery contributing through a boost converter

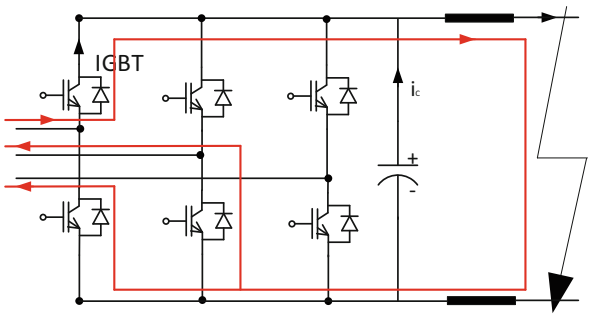

Fig. 2.5 Fault current path of an AC source through a two-level AC/DC rectifier

2.3 *Fault Current from AC Sources*

Depending on converter topology, active switches may or may not appear on DC fault path. If IGBTs (Insulated Gated Bipolar Transistor) are on the fault paths, they should be turned off quickly to avoid damages because of their low thermal limits. If semiconductors with high thermal limits are used, such as IGCTs (Integrated Gate Commutated Thyristor), they can be controlled to limit DC fault currents at higher level, which allows reliable fault detection and protection coordination. However, these converters with active switches on fault path normally have relatively higher cost. For many low-cost converters, such as two-level AC/DC rectifiers, there are no active switches on its fault path to interrupt or limit DC fault current.

An AC source contributes to fault current through the freewheeling diodes of a conventional two-level AC/DC rectifier. At steady state, the fault paths from AC side to DC side are shown in Fig. 2.5. The DC fault current waveform thus appears as the envelope of the three phase fault currents of the AC source. The DC fault peak is determined by the first peak of the three phase fault currents, which occurs around half cycle or ~8 ms/~10 ms of 60 Hz/50 Hz systems. The high fault current from the AC source can damage the freewheeling diodes of its associated AC/DC rectifier and other equipment on the fault path.

Considering the worst fault scenario where the fault occurs at voltage peak, the generator AC fault current i_{gen} and its derivative can be calculated by (2.7). In direct and quadrature (dq) reference frame, E_{q0} is generator internal voltage in q-axis. L_{ad} and $L_{\delta\text{s}}$ are armature and leakage inductance of the stator winding in d-axis. L_D is generator damping winding inductance. L_{d}'' and L_{q}'' are generator stator sub-transient inductances in d- and q-axis. r_{f} and r_{s} are generator field winding and stator winding resistances. It should be noted that the generator frequency f_s can vary during its operation. From (2.12), if the generator frequency is lower, the fault current peak is higher, but the time to reach the fault peak is longer.

$$i_{\text{gen}}(t) = -I''_{\text{gen}} e^{-t/\tau''_d} \cos\left(2\pi f_s t\right) + I''_{\text{gen}} e^{-t/\tau_a} \tag{2.7}$$

where $I''_{\text{gen}} \approx \frac{E_{q0}}{2\pi f_s L''_d}$, $\tau''_d \approx \frac{L_f + \frac{1}{1/L_{\text{ad}}+1/L_{\delta s}+1/L_D}}{r_f}$, $\tau_a \approx \frac{\left(\frac{1}{0.5\left(1/L''_d+1/L''_q\right)}\right)}{r_s}$.

AC motors can also contribute DC fault currents through the freewheeling diodes of their interfacing DC/AC inverters before the remaining flux of the motors disappears. Similar to the AC generator fault current, the AC motor fault current i_{m} at the worst fault scenario can be obtained from (2.8). L_{s}, L_{m}, and L_{r} are motor inductances. R_{r} and R_{s} are motor resistances.

$$i_{\text{m}}(t) = -I'_{\text{m}} e^{-t/\tau_r} \cos\left(2\pi f_s t\right) + I'_{\text{m}} e^{-t/\tau_s}. \tag{2.8}$$

where $I'_{\text{m}} \approx \frac{E}{2\pi f_s L'}$, $L' = L_{\text{S}} + \frac{L_{\text{m}} L_{\text{r}}}{L_{\text{m}}+L_{\text{r}}}$, $L = L_{\text{S}} + L_{\text{m}}$, $\tau_{\text{r}} \approx \frac{L'}{R_{\text{r}}}$, $\tau_{\text{s}} \approx \frac{L}{R_{\text{s}}}$.

More generally, an AC grid, instead of an AC generator, is connected to a DC system. The AC grid can be represented by a three-phase voltage source behind impedance; its AC fault current i_{AC} can be estimated as (2.9). The total source resistance R_{s} and inductance L_{s} includes the AC transformer resistance and inductance. The commutation resistance of the AC/DC rectifier should also be added into the total resistance R_{s}. V_{s} and L_{s} are the AC source internal voltage and total inductance. If the DC fault location is far away from the AC source and its rectifier, then the total DC line resistance R_{line} should also be included into the calculation.

$$i_{\text{AC}}(t) = I_{\text{F}} \sin\left(2\pi f_s t - \phi\right) + \left(i_0 + I_{\text{F}} \sin\left(\phi\right)\right) e^{-t/\tau} \tag{2.9}$$

where $I_{\text{F}} = \frac{V_{\text{S}}}{\sqrt{\left(R_s+\frac{2}{3}R_{\text{line}}\right)^2+X_s^2}}$, $\phi = \arctan\left(\frac{2\pi f_s L_{\text{s}}}{R_s+\frac{2}{3}R_{\text{line}}}\right)$, $\tau = \frac{L_{\text{s}}}{R_s+\frac{2}{3}R_{\text{line}}}$.

If the harmonics caused by the three-phase AC fault currents are ignored, the DC fault current can also be estimated from as (2.10) and (2.11) according to IEC 61660 [18]. The DC fault current after the AC/DC rectifier first rises to its peak i_{peak} at t_{peak} and then eventually settle down to a steady-state value i_{k}, which can be derived from (2.9). Time constants τ_1 and τ_2 are rising and decaying time constants, respectively. i_{peak}, t_{peak}, i_{k} can be derived from (2.1), (2.2), (2.3), (2.4), (2.5), (2.6), (2.7), (2.8), and (2.9). IEC61660 gives equations to calculate τ_1, and τ_2.

$$i_1(t) = i_{\text{peak}} \frac{1 - e^{-\frac{t}{\tau_1}}}{1 - e^{-\frac{t_{\text{peak}}}{\tau_1}}}, 0 \le t \le t_{\text{p}} \tag{2.10}$$

$$i_2(t) = i_{\text{peak}} \left[\left(1 - \frac{i_{\text{k}}}{i_{\text{peak}}}\right) e^{-\frac{t-t_{\text{peak}}}{\tau_2}} + \frac{i_{\text{k}}}{i_{\text{peak}}}\right], t_{\text{p}} \le t \tag{2.11}$$

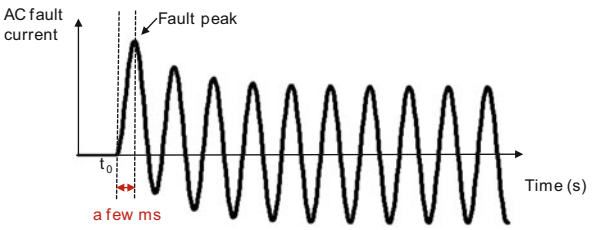

Fig. 2.6 Example AC fault current waveform

2.4 *Salient Features of DC Fault Currents*

Some example fault currents in AC and DC systems are illustrated in Figs. 2.6 and 2.7, respectively. The approximated DC fault current from batteries using (2.10) is given. In IEC 61660, (2.10) and (2.11) are also used to approximate the DC fault current waveforms from batteries, which results in rising to a peak and then reducing to its steady-state value. From (2.6), the battery fault current rises to a high value close to its peak and final stead-state value within a short time frame. A compromise of the two curves could be a more accurate battery DC fault current, which needs further experimental validation. Compared to the AC fault current, the DC fault currents have two distinguished characteristics:

1. There are no consistent 50 Hz/60 Hz zero-crossings in DC fault currents
2. The fault current rising speed of DC capacitors and batteries is much faster than AC fault currents.

The two salient features impose completely different design requirements on DC protection devices and methods from AC.

1. Because of non-zero crossing in DC fault currents, traditional electromagnetic AC circuit breakers cannot be directly employed as DC circuit breakers.
2. The required speed for DC fault detection, identification, and isolation is much faster than their AC counterparts.

The current derivative *di/dt* and the time to fault peak t_{peak} are crucial to define required speed and other protection requirements for DC circuit breakers and protection methods. From (2.1), (2.2), (2.3), (2.4), (2.5), (2.6), (2.7), (2.8), (2.9), (2.10), and (2.11), the DC fault current derivative of different types of sources can be calculated by (2.12), (2.13), (2.14), (2.15), (2.16), and (2.17). At zero current derivative, the fault currents reach their maximum values. The time to fault peak of the capacitor fault currents thus can be calculated as (2.18) and (2.19). And the fault peak can be calculated by (2.20) and (2.21).

$$\frac{di_{\text{cap}}}{dt} = \frac{1}{L}\frac{V_0}{p_1 -' p_2}\left(p_1 e^{p_1 t} - p_2 e^{p_2 t}\right), \quad \text{if} \quad R > 2\sqrt{\frac{L}{C}}. \tag{2.12}$$

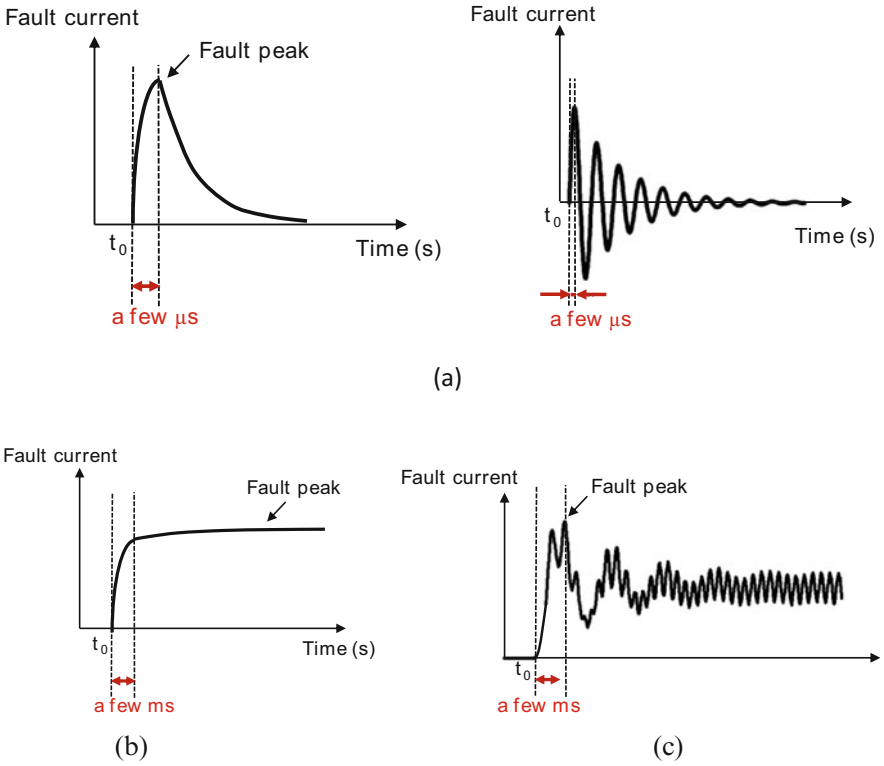

Fig. 2.7 Example DC fault current waveforms from various sources. (**a**) Capacitor (Left: $R > 2\sqrt{\frac{L}{C}}$; Right: $R \leq 2\sqrt{\frac{L}{C}}$) (**b**) Battery (**c**) AC source

$$\frac{di_{\text{cap}}}{dt} = -\delta \frac{V_0}{\omega L} e^{-\delta t} \sin(\omega t) + \frac{V_0}{L} e^{-\delta t} \cos(\omega t), \quad \text{if} \quad R \leq 2\sqrt{\frac{L}{C}}. \tag{2.13}$$

$$\frac{di_{\text{Batt}}}{dt} = \frac{V_{\text{Batt}}}{L} e^{-t/\tau} \tag{2.14}$$

$$\frac{di_{\text{gen}}}{dt} = \frac{I''_{\text{gen}}}{\tau''_{\text{d}}} I''_{\text{g}} e^{-t/\tau''_{\text{d}}} \cos\left(2\pi f_s t\right) + 2\pi f_s I''_{\text{gen}} e^{-t/\tau''_{\text{d}}} \sin\left(2\pi f_s t\right) - \frac{I''_{\text{gen}}}{\tau_{\text{a}}} e^{-t/\tau_{\text{a}}} \tag{2.15}$$

$$i_{\text{am}}(t) = \frac{I'_{\text{m}}}{\tau_{\text{r}}} e^{-t/\tau_{\text{r}}} \cos\left(2\pi f_s t\right) + 2\pi f_s I'_{\text{m}} e^{-t/\tau_{\text{r}}} \sin\left(2\pi f_s t\right) - \frac{I'_{\text{m}}}{\tau_{\text{s}}} e^{-t/\tau_{\text{s}}}. \tag{2.16}$$

Table 2.1 Initial fault current, time to fault peak, and initial current derivatives [20]

	DC sources			AC sources	
	Capacitor		Battery	Generator	Motor
	$R > 2\sqrt{\frac{L}{C}}$	$R \le 2\sqrt{\frac{L}{C}}$			
i at $t \to 0$	$\frac{V_0}{L}t$	$\frac{V_0}{L}(1-\delta t)\,t$	$\frac{V_{DC}}{L}t$	$\left(\frac{I''_g}{\tau''_d} - \frac{I''_g}{\tau_a}\right)t$	$\left(\frac{I'_m}{\tau_r} - \frac{I'_m}{\tau_s}\right)t$
t_{peak}	$\frac{\ln(p_2/p_1)}{p_1-p_2}$	$\sim \frac{\pi}{2\omega}$	$\sim 3\frac{L}{R}$	$\sim \frac{T_s}{2}$	$\sim \frac{T_s}{2}$
di/dt at $t \to 0$	$\frac{V_0}{L}$	$\frac{V_0}{L}$	$\frac{V_{DC}}{L}$	$\frac{I''_g}{\tau''_d} - \frac{I''_g}{\tau_a}$	$\frac{I'_m}{\tau_r} - \frac{I'_m}{\tau_s}$

$$i_{AC}(t) = 2\pi f_s I_F \cos\left(2\pi f_s t - \phi\right) - \frac{i_0 + I_F \sin(\phi)}{\tau} e^{-t/\tau} \tag{2.17}$$

$$t_{peak} = \frac{\ln(p_1/p_2)}{p_1 - p_2}, \quad \text{if} \quad R > 2\sqrt{\frac{L}{C}}. \tag{2.18}$$

$$t_{peak} = \frac{\beta}{\omega}, \quad \text{if} \quad R \le 2\sqrt{\frac{L}{C}}. \tag{2.19}$$

$$i_{f_{peak}}(t) = \frac{1}{L}\frac{V_0}{p_1 -' p_2}\left(e^{p_1 t_{peak}} - e^{p_2 t_{peak}}\right), \text{if} \quad R > 2\sqrt{\frac{L}{C}} \tag{2.20}$$

$$i_{f_{peak}}(t) = \frac{V_0}{\omega L} e^{-\delta t_{peak}} \sin\left(\omega t_{peak}\right), \text{if} \quad R \le 2\sqrt{\frac{L}{C}} \tag{2.21}$$

Especially, for ultrafast solid-state circuit breakers, the initial fault currents, the times to fault peak, and the initial current derivatives are valuable variables to develop technical requirements for DC breakers and DC fault detection, location, and protection coordination methods. These initial variables derived from (2.12), (2.13), (2.14), (2.15), (2.16), (2.17), (2.18), and (2.19) are summarized in Table 2.1. Examples of using these variables for designing solid-state circuit breaker and various DC protection methods can be found in [19, 20].

Within a very short time frame after fault occurrence, the initial current derivatives can be approximated as constant values and the initial fault currents are considered linearly increasing with time. This linear approximation in DC fault current behavior is useful to estimate design parameters for solid-state circuit breakers. Their time to peak is quite different and analyzed as follows:

1. Considering a fault location close to its source, then the capacitor discharges in oscillation waveforms if resistance is very low. The fault peak occurs at $\pi/2$, and the time to peak of capacitors is $\pi/2$ divided by the angular speed ω. The time to peak of capacitor discharging thus can be as low as a few microseconds.

2. Because the battery DC fault current derivative decreases to ~5% of its initial value at three times of the rising time constant, the time to peak of batteries is approximately equal to three times of the rising time constant. This time to peak is related to the ratio between the total inductance and resistance, including the battery internal resistance, on the fault path. The time to peak of batteries can be up to a few milliseconds.
3. For the AC sources, since the fault currents develop as the envelope of three-phase fault currents, they reach fault peak at approximately half cycle of the AC system time constant. The time to peak of AC sources is related to system frequency and equal to ~8 ms/~10 ms for 60 Hz/50 Hz systems.

2.5 DC Fault Current Analysis of High Impedance Faults

In Sects. 2.1, 2.2, and 2.3, the fault current analysis was conducted at low fault impedance. Fault impedance has high impacts on DC fault features, such as reduced fault peaks, increased fault time constants, etc. With one source contributing to a DC fault, the fault resistance can be added as a part of the total resistance on the fault path to calculate DC fault voltages and currents. The equations in Sects. 2.1, 2.2, and 2.3 need to be updated with the fault resistance accordingly.

If multiple sources contribute fault current to one fault location, the fault current is the summation of weighted fault currents from all available sources during fault. Figure 2.8 shows fault circuit of two equivalent DC sources, VDC1 and VDC2, at a high impedance fault. R_{eq} and L_{eq} are the equivalent resistance and inductance from one DC source to the fault location. R_f is the fault resistance. Numbers 1 and 2 indicate the variables associated with VDC1 and VDC2, respectively. Equations (2.20) and (2.21) describe the fault current i_{f1} and i_{f2} from two sources. Because of the high fault resistance, the fault current from one source is impacted by the fault current from other sources. From the two equations, the fault current from one source can be derived if the fault current from the other source and the fault resistance are known. In real systems, VDC1 and VDC2 could be measured DC voltages by protection devices. Equations (2.22) and (2.23) indicate that remote sensing and measurement could be required to accurately estimate fault currents at high impedance fault. Equation (2.24) can be used to calculate the fault current i_{f1} with given circuit parameters, including R_f.

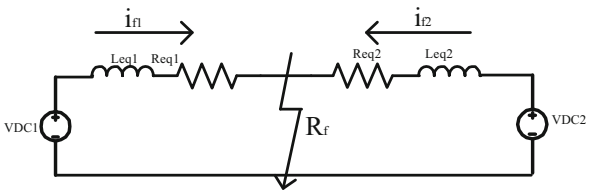

Fig. 2.8 High impedance DC faults with two sources

$$v_{\mathrm{DC1}} = L_{\mathrm{eq1}} \frac{di_{\mathrm{f1}}}{dt} + R_{\mathrm{eq1}} i_{\mathrm{f1}} + R_{\mathrm{f}} \left(i_{\mathrm{f1}} + i_{\mathrm{f2}}\right) \tag{2.22}$$

$$v_{\mathrm{DC2}} = L_{\mathrm{eq2}} \frac{di_{\mathrm{f2}}}{dt} + R_{\mathrm{eq2}} i_{\mathrm{f2}} + R_{\mathrm{f}} \left(i_{\mathrm{f1}} + i_{\mathrm{f2}}\right) \tag{2.23}$$

$$i_{\mathrm{f1}}(\mathrm{s}) = \frac{v_{\mathrm{DC1}}(\mathrm{s})}{\mathrm{SL}_1 + R_1 + \frac{R_{\mathrm{f}}(\mathrm{SL}_2 + R_2)}{\mathrm{SL}_2 + R_2 + R_{\mathrm{f}}}} - \frac{v_{\mathrm{DC2}}(\mathrm{s})}{\mathrm{SL}_2 + R_2 + \frac{R_{\mathrm{f}}(\mathrm{SL}_1 + R_1)}{\mathrm{SL}_1 + R_1 + R_{\mathrm{f}}}} \frac{R_{\mathrm{f}}}{\mathrm{SL}_1 + R_1 + R_{\mathrm{f}}} \tag{2.24}$$

In above equations, the fault resistance R_{f} is considered as a known variable. In reality, R_{f} usually is an unknown variable and needs to be derived in order for accurate fault detection and location. In practical applications, multiple voltage and current measurements can be used to estimate the fault resistance. Equations (2.25), (2.26), and (2.27) describe the fault circuit from VDC1 at three different time instants $t1$, $t2$, and $t3$. As described before, the current measurements of both i_{f1} and i_{f2} at multiple time instants are needed. The current derivatives can be derived by directly measuring from the circuit or indirectly calculating from the current measurements. Equation (2.28) is the matrix format of (2.25), (2.26), and (2.27). Not only the fault resistance but also the fault location thus can be derived by solving (2.28). If there are more measurements available, least square regression can be used to optimally estimate and improve estimation accuracy.

$$v_{\mathrm{DC1},t1} = L_{\mathrm{eq1}} \frac{di_{f1,t1}}{dt} + R_{\mathrm{eq1}} i_{f1,t1} + R_{\mathrm{f}} \left(i_{f1,t1} + i_{f2,t1}\right) \tag{2.25}$$

$$v_{\mathrm{DC1},t2} = L_{\mathrm{eq1}} \frac{di_{f1,t2}}{dt} + R_{\mathrm{eq1}} i_{f1,t2} + R_{\mathrm{f}} \left(i_{f1,t2} + i_{f2,t2}\right) \tag{2.26}$$

$$v_{\mathrm{DC1},t3} = L_{\mathrm{eq1}} \frac{di_{f1,t3}}{dt} + R_{\mathrm{eq1}} i_{f1,t3} + R_{\mathrm{f}} \left(i_{f1,t3} + i_{f2,t3}\right) \tag{2.27}$$

$$\begin{bmatrix} v_{\mathrm{DC1},t1} \\ v_{\mathrm{DC1},t2} \\ v_{\mathrm{DC1},t3} \end{bmatrix} = \begin{bmatrix} \frac{di_{f1,t1}}{dt} & i_{f1,t1} & i_{f1,t1} + i_{f2,t1} \\ \frac{di_{f1,t2}}{dt} & i_{f1,t2} & i_{f1,t2} + i_{f2,t2} \\ \frac{di_{f1,t3}}{dt} & i_{f1,t3} & i_{f1,t3} + i_{f2,t3} \end{bmatrix} \begin{bmatrix} L_{\mathrm{eq1}} \\ R_{\mathrm{eq1}} \\ R_{\mathrm{f}} \end{bmatrix} \tag{2.28}$$

3 DC Fault Detection and Identification

A DC fault must be identified and located in a timely and reliable way in order to prevent any damage to the power network. Due to the fast rate of change of the dc fault current and restricted thermal limit of semiconductors, fault detection and

identification present significant technical challenges in protection reliability and speed. The final DC fault current at any location in a DC system is a weighted summation of all fault currents contributed from different sources at different locations inside a DC network. Therefore, the final fault current is a superimposition of the fault currents from all sources. The DC fault current waveform and its characteristics are closely related to DC network topology and line parameters. A DC fault current estimation method of a distributed DC network was introduced in IEC 61660 [18], and an improved method was developed to generalize the DC fault calculation into a meshed DC network and improve the estimation accuracy [21].

DC fault current can be detected and identified by different methods and technologies. Depending on the location of measurements, local measurement-based and communication-based methods can be applied. Local measurement and communication-based methods can be further classified according to variables used in the DC fault detection. Typical local measurement-based methods include overcurrent, current derivative, under voltage, and distance. These fault protection methods are non-unit protection and can respond to both in-zone and out-of-zone faults if protection thresholds are reached. The most common communication-based fault detection method is differential protection. It is a unit protection and only activated to in-zone faults.

Most of the aforementioned fault detection methods are extended from conventional fault detection methods of AC systems into DC. AC fault current increases in the form of sinusoidal waveform with inherent 50/60 Hz system frequency. Table 2.1 in Sect. 2 gives the equations to estimate the DC current from different sources. DC fault currents by capacitors and batteries increase rapidly given the DC line inductance is normally low. In principle, the conventional AC fault detection methods are revised significantly to accommodate fast protection speed requirement in DC fault detection to prevent service interruptions or damages to components. Essentially, instead of fault voltages and currents at steady-state used in AC fault detection, fault voltages and currents at initial transients are used for DC fault detection. The current derivative-based protection is rarely used as a primary fault detection method in AC. However, it can be used as a primary protection method in DC because current derivatives at DC faults are substantially high due to low inductance. Stringent synchronization and high sampling rate are crucial for the accurate and reliable fault detection using current derivative-based DC fault detection.

Each fault detection technique has advantages and disadvantages in terms of reliability, speed, sensitivity, selectivity, and implementation complexity [1, 19, 20, 22]. It should be noted that the previously mentioned non-unit DC fault detection methods normally can effectively handle DC faults with low fault impedance. However, fault impedance has high impact on DC fault detection. If there is high fault impedance in the fault path, the fault resistance should be included into the fault current calculations as described in Sect. 2. The detection thresholds of non-unit fault detection methods should be adjusted accordingly to include the impacts by high fault impedance. As given in Sect. 2.5, a high impedance fault with fault current contributions from multiple sources, local measurement protection no longer can find fault impedance and thus accurately detect DC faults. Remote sensing and

communication would be needed for estimating fault impedance and location. Unit protection has the advantage of being much less dependent on fault impedance. High fault impedance can reduce DC fault increasing speed and increase time to reach fault peak. Therefore, the speed requirement on DC fault detection at high impedance fault can be relaxed, which is beneficial to communication-based differential protection. With reasonable cost increase of a reliable communication scheme, high speed differential protection may be used as primary protection for DC microgrids. Communication delays should be kept minimal since they slow down protection response speed. Reliable high bandwidth communication and strict synchronization are must-haves for sample-based differential protection. Depending on the specific needs of a DC system to be protected, the final selection of a proper DC fault detection method could be a hybrid one combining multiple DC fault detection techniques.

4 DC Fault Interruption Technologies

The objective of DC fault interruption technologies is to quickly and safely isolate the faulty part from the healthy part of a DC network while preventing damages to the system. It is a critical building block of any DC power systems and has become a subject of intensive research and development over the past decades.

AC power systems typically use mechanical circuit breakers to establish an electric arc and take advantage of the natural zero crossing of AC current for extinguishing it. The interruption capability and speed of those mechanical circuit breakers are sufficient for most AC applications. The first challenge of DC fault current interruption with respect to AC is the intrinsic absence of current zero crossings in DC power systems which makes it difficult to extinguish the arc of any mechanical circuit breakers. The second challenge is that DC power systems typically have significantly less reactance than AC leading to much faster rise of the fault current, and thus require a response time of a few milliseconds or less in comparison to tens of millisecond for AC circuit breakers. The third challenge is that the residual electromagnetic energy of a DC power system, proportional to the loop inductance and the square of the fault current at the moment of interruption, must be dissipated during the interruption process. In some HVDC systems this energy can be as high as tens of megajoules.

DC fault interruption forces the fault current to zero and forms a complete air-gap or galvanic isolation of the fault from the system. It must have the key features such as low conduction loss, fast response, galvanic isolation, high reliability, long lifetime, and low cost. A new unified classification of various DC fault interruption technologies based on fundamental topology and operation principle instead of secondary technical features is provided in Fig. 2.9. It is divided into five categories: mechanical circuit breaker (MCB), solid-state circuit breaker (SSCB), hybrid circuit breaker (HCB), converter-based protection (breakerless), and fault current limiter (FCL). Each category will be further subdivided into several subcategories based

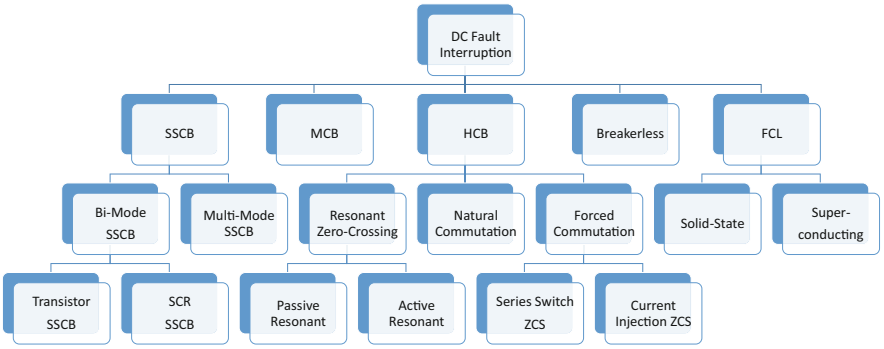

Fig. 2.9 A unified classification of DC fault interruption technologies based on fundamental topology and operation principle, including mechanical circuit breaker and fuse (MCB), solid-state circuit breaker (SSCB), hybrid circuit breaker (HCB), converter-based protection (breakerless), and fault current limiter (FCL)

on the second-order features. The operating principle, advantages, disadvantages, and practical applications of each of the DC fault interruption technologies will be discussed in this section. They will be compared for a wide range of voltage and current ratings at the end of this chapter.

4.1 Mechanical Circuit Breaker

Mechanical circuit breaker (MCB) is a very mature technology that has been widely used in AC grids for near a century. In an MCB, two metal contacts close or open a circuit with mechanical forces such as electromagnetic, thermal-magnetic, spring action, and others. The conduction loss of an MCB is determined by the contact resistance of the metal contacts and ranges from a few $\mu\Omega$ to tens of $m\Omega$ depending on its current rating. MCB offers the lowest power loss among all the fault interruption technologies. Its voltage rating is determined by the physical gap and dielectric media between the contacts, ranging from hundreds of volts for an open-air mold-case circuit breaker (MCCB) to tens of kV for a vacuum interrupter or hundreds of kV for a sulfur hexafluoride (SF_6) high-voltage circuit breaker. The arc voltage between the two contacts during opening counters the power supply voltage and helps reduce the fault current. The wide voltage and current ratings, ultralow conduction loss, and cost effectiveness make MCB an ideal choice for most AC applications since the breaking arc can be extinguished at the naturally occurring current zero crossings. However, MCBs take a relatively long time, in the order of tens to hundred milliseconds, to interrupt a fault, thus are not suitable for DC applications which require a faster response time. Furthermore, MCBs interrupt the fault current through the generation and extinction of electric arc which degrades their lifetime and reliability over time.

Classical AC MCBs can be adapted for certain DC applications after significant voltage and/or current derating. Dedicated DC MCBs with special arc quenching techniques can also be designed for DC applications up to kV/kA ratings, such as DC railway and traction systems. However, MCB is generally not a viable or cost-effective option for most DC power systems considering their limited arc quenching capability, lifetime, and response time. Note that an MCB with a parallel LC resonant circuit can generate artificial current zero crossings through the metal contacts and considerably improves its DC fault interruption capability. Unlike in many other publications, this solution is listed under the HCB category in the classification of Fig. 2.9 and will be discussed later in this section.

Fuse is another widely used fault interruption technology at a relatively low cost and therefore briefly discussed in this section. A fuse is usually made of a fuse link surrounded by a heat absorbing material to extinguish the arc during the interruption of the fault current. It can be used in both AC and DC systems. However, in an AC grid, the natural zero-crossing of the current is able to assist the fuse in quenching the arc, while in a DC system, the fuse needs to be able to absorb the arc energy by itself entirely as there is no zero-crossing available. Consequently, a DC fuse offers significantly lower fault interruption capability than a similar AC fuse. Fuses are commonly used for DC traction, battery protection, mining, and other DC applications with an operating voltage up to 4000 V. The fundamental drawback of fuses is their one-time use nature which does not allow reclosing of the circuit after a momentary short circuit fault. Furthermore, their interruption time is similar to that of MCBs and therefore not suitable for DC applications subject to fast-rising fault currents. They are often used in DC systems as the backup protection in case the primary protection measure fails to interrupt the fault current.

4.2 Solid-State Circuit Breakers

A solid-state circuit breaker (SSCB) essentially uses power semiconductor devices, such as MOSFET, IGBT, IGCT, or thyristor, to close and open a circuit loop. Figure 2.10 shows a conceptual block diagram and switching waveforms of a generic SSCB. Additional gate driver, cooling system, voltage clamping circuit, fault detection circuit, and auxiliary power supply are needed for SSCB operation. During normal operation, the power semiconductor device stays in ON-state. The gate driver unit applies appropriate bias voltage or current to the power semiconductor gate terminal to keep it in a low-resistance ON-state. The fault detection circuit continuously monitors the load current either in an analog mode or a digital mode with a high sampling rate. If an overcurrent condition is detected, the control electronics turn OFF the power semiconductor device through the gate driver. When the power semiconductor device is turned OFF, the residual electromagnetic energy in the system inductance generates a transient overvoltage across the power semiconductor switch, which is eventually limited by the voltage clamping circuit such as a metal-oxide-varistor (MOV). Once the MOV absorbs all

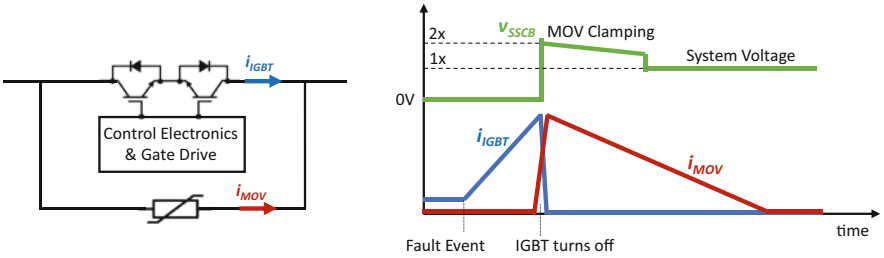

Fig. 2.10 A notional circuit diagram and switching waveforms of SSCB using bidirectional IGBT switch as an example

the residual system energy and the system current is driven to zero, both the power semiconductor and MOV are in a high impedance state, and the voltage across the circuit breaker reaches the system bus voltage. Chapter 3 of this book describes a 1 kV/1.5 kA rated SSCB example that uses reverse-blocking IGCTs as the static switch. It exhibits a power loss under 3 kW and a response time of several hundred μs (line inductance dependent). Chapters 4, 5, 6, 7, 8, and 9 of this book introduce a few other SSCB examples with each offering distinct design features.

SSCBs offer several distinct advantages. First, they offer a response time several orders of magnitude faster than that of conventional MCBs. Note that the SSCB response time (typically tens to hundreds of μs) is largely dictated by the MOV energy absorption time since the semiconductor devices can complete the switching action within a few μs. Second, unlike MCBs which rely on contact separation for current interruption, semiconductor devices can interrupt the fault current without arcing. This translates into a greatly increased operation lifetime. Finally, thanks to the extremely fast current interruption capability, SSCBs can limit the fault current and let-through energy to a relatively low level, allowing downsizing of power cables and other system components.

The main disadvantage of SSCBs is their high ON-state conduction power loss and the associated active cooling requirement, which significantly increase the size, weight, cost, and complexity of the power system. In comparison to the μΩ-mΩ contact resistance of MCBs, power semiconductor devices typically have an ON-resistance several orders of magnitude higher, depending on the device type and voltage rating. Silicon IGBTs offer a voltage rating of 600–6500 V and a current rating up to 1 kA for a single discrete device or power module. For example, a discrete 1200 V IGBT typically offers a minimum equivalent ON-resistance of 15–20 mΩ. ICGTs offer a voltage rating of 2500–6500 V and a current rating up to 2 kA with roughly 20–50% less ON-resistance than IGBTs. Thyristors (also known as silicon-controlled rectifiers or SCRs) offer a voltage rating up to 12 kV and a current rating up to 6 kA with an equivalent ON-resistance even lower than that of IGCTs. Silicon power MOSFETs offer an ON-resistance in the mΩ range for a voltage rating under 100 V and become a viable LVDC device option. However, the ON-resistance of silicon power MOSFETs increases dramatically with its voltage

rating, making them unsuitable for a voltage rating over 300 V. It is worth noting that active cooling techniques, such as forced air or liquid cooling, are generally required for a power loss more than several tens of watts in an SSCB design, resulting in a penalty in weight, size, complexity, and reliability. High-power SSCBs usually require active cooling provisions while low-power SSCBs may be passively cooled. On a separate note, the switching speed of these semiconductor devices is not as a critical factor for SSCB designs as for conventional power converter designs. This is simply because the switching of an SSCB tends to be an infrequent event and the total fault interruption time is mainly determined by the much longer MOV energy absorption time.

During the past decade, wide bandgap (WBG) semiconductor devices, such as silicon carbide (SiC) MOSFETs and gallium nitride (GaN) transistors, have become commercially available and attracted attention for potential SSCB applications. WBG transistors offer significantly lower specific ON-resistance than their silicon counterparts, and provide a possibility for low-loss and passively cooled SSCB designs. Chapter 4 of this book describes a GaN-based 380 V/20 A SSCB design with a total ON-resistance of 10 mΩ and a total power loss of 4 W without requiring any active cooling provision. Chapters 5 and 6 of this book describe several SiC-based SSCB topologies while Chap. 9 also introduces several WBG-based SSCB schemes. However, it should be pointed out that the WBG devices currently are 3–5 times more expensive than silicon and their faster switching characteristics generally do not benefit SSCB applications. Furthermore, while high-voltage WBG devices such as 20 kV SiC IGBTs were previously reported, they are yet to become commercially available. In the near future, WBG-based SSCBs are most likely limited to relatively low power systems (e.g., under 1000 V and/or 100 A).

Conventional SSCBs typically have two operating states (thus referred to as bi-mode SSCBs in Fig. 2.9): ON-state for conducting normal current and OFF-state for interrupting fault current. The bi-mode SSCBs offer very limited flexibility to deal with complex operating scenarios such as inrush currents. The inrush current, often the initial charging current for the large input capacitor of an electrical load during startup, can be many times of the nominal current and difficult to distinguish from a true short circuit fault current. The inrush current may cause nuisance tripping of circuit breakers. Innovative solutions beyond the conventional ON/OFF SSCB configuration need to be developed to integrate intelligent functions with minimal cost penalty.

Chapter 4 of the book describes a new intelligent SSCB that operates in three states (thus referred to as the multi-mode SSCB in Fig. 2.9). In addition to the ON and OFF states, the so-called tri-mode SSCB can operate in a distinct PWM Current Limiting (PWM-CL) state with a moderate overcurrent for a short period of time to facilitate intelligent functions such as soft startup, fault authentication, fault location, and selective coordination. The tri-mode SSCB will switch from the PWM-CL to the OFF state if it deems the overcurrent condition to be a true short circuit fault rather than a startup scenario after a short time period. Switching-mode buck topologies along with a variable frequency PWM control method are adopted to replace the simple bi-mode SSCB ON/OFF switch configuration to optimize

both soft-start and other fault protection functions. Other multi-mode SSCB design examples include operating the power MOSFET of the SSCB in a saturation mode to limit the inrush current or using different converter topologies. The T-Breaker concept introduced in Chap. 5 also offers multiple operation modes.

For bi-mode SSCBs, there are two different types of power semiconductor devices that can be used as the main static switch: fully controllable transistors (e.g., MOSFET, IGBT, and IGCT) and semi-controllable thyristors (SCRs). Transistors can be turned ON and OFF by a gate control signal and easily adopted in an SSCB design. Although IGCTs are essentially a special type of thyristors, they are placed under the transistor category here because of their full gate controllability.

In comparison to IGBTs, thyristors offer considerably higher power rating (up to 12 kV or 6 kA), lower conduction loss, and superior surge current capability (up to 100 kA) because they are fabricated on an entire silicon wafer (up to 150 mm in diameter) which are sandwiched in a pressure contact package. For those reasons, thyristors are good candidate for high-power SSCB designs. However, thyristors can be turned on by a gate control signal but must be turned off by either natural or forced commutation, making them more difficult to use in DC applications. Special auxiliary commutation circuits are needed to turn them off in DC power networks due to the lack of current zero crossing. Various SCR-based SSCB topologies are reviewed in [12]. The main drawbacks of the SCR-based SSCBs include relatively long current interruption time and the use of bulky capacitors. A special type of SCR-based SSCBs termed the Z-source SSCB was developed in recent years, which has the advantage of autonomous fast current interruption. A Z-source SSCB has a LC impedance network (the Z-source network). When there is a critical short circuit fault, the inductor current remains relatively constant for a short time period, and the capacitors provide a transient current path, creating a current zero-crossing in the SCR. The SCR commutates off after current reaches zero, and the short circuit fault is isolated from the power source. The commutation of the SCR does not need the OFF command from the control circuits, enabling a fast fault interruption speed. Chapter 7 of this book describes the basic concept of the Z-source SSCB and several design variants. The limitations of the Z-source SSCBs include their difficulty of protecting against overload or high impedance short circuit faults with low *di/dt* as well as the complexity in realizing bidirectional capability.

4.3 Hybrid Circuit Breakers

Hybrid circuit breakers (HCBs) combine the advantages of MCB (low loss) and SSCB (arcless interruption) and offer a viable solution for DC fault interruption.

Figure 2.11 shows the notional circuit diagrams of several HCB types. A classical HCB generally comprises of a mechanical path to conduct the normal load current, a parallel electrical or electronic commutation path to carry the current under a fault condition, and a parallel voltage clamping circuit (e.g., MOV). The mechanical path, mainly comprising of a mechanical switch or breaker, offers low ON-resistance

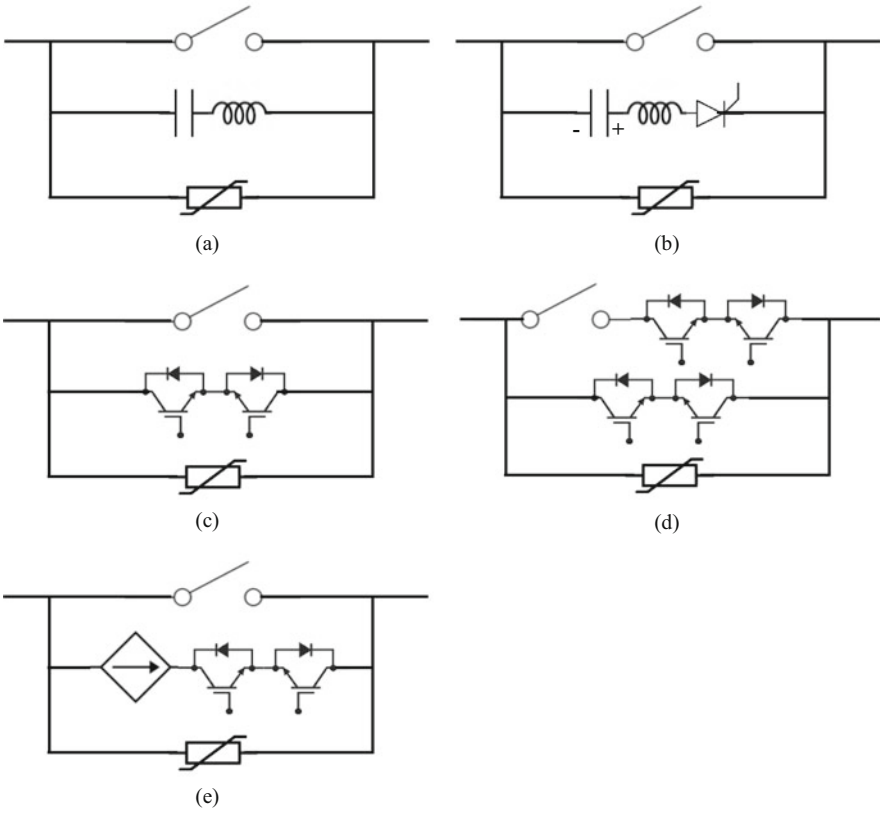

Fig. 2.11 Notional diagrams of various types of HCBs: (**a**) passive resonant type, (**b**) active resonant type, (**c**) natural commutation type, (**d**) series-switch ZCS commutation type, and (**e**) counter-current injection ZCS commutation type

comparable to that of MCB during normal operation. The parallel commutation path, comprising of passive or active circuit elements, creates artificial current zero crossing or forces the current to zero completely in the mechanical path under a short circuit fault condition, aiding the opening of the mechanical switch with significantly suppressed arcing or no arcing at all. After the mechanical switch fully opens, the parallel voltage clamping circuit absorbs the residual electromagnetic energy in the circuit.

HCBs can be classified into three subcategories. The first HCB subcategory is termed resonant zero-crossing HCB in this chapter. Under this subcategory, the parallel commutation circuit is essentially a *LC* resonant circuit. Upon the detection of a fault condition, the mechanical breaker opens and generates a switching arc. Subsequently, a current oscillation is generated between the commutation *LC* circuit and the switching arc, creating artificially current zero crossings through the mechanical breaker. These current zero crossings aid to extinguish the arc and

eventually commutate the fault current into the resonant circuit. The capacitors in the resonant circuit will be eventually charged. The resonant circuit can be of either passive or active type. A passive resonance circuit (Fig. 2.11a) only uses *L* and *C* components and exploits the negative differential resistance of the arc, which interacts with the *LC* circuit to excite a divergent current oscillation that is superimposed to the fault current. The oscillation grows until it ultimately exceeds the fault current, creating zero crossings. Passive resonant commutation circuit is the simplest scheme in terms of component count for DC fault interruption. The active resonance concept (Fig. 2.11b) is similar to the passive method, but the capacitors in the *LC* branch are precharged and a semiconductor switch (e.g., SCR) is typically used to initiate the injection of the capacitor discharge current. The active scheme allows faster operation and higher interruption capability than the passive one, due to the fact that it reduces the time for the current oscillation to grow. On the other hand, more active components and more complex control are needed in the active resonance schemes. Passive resonant zero-crossing HCBs can typically interrupt a fault current up to a few kA within 10–20 ms while the active type resonant zero-crossing HCBs can interrupt up to tens of kA within a few milliseconds. Chapter 10 of this book describes a low-voltage active resonant zero-crossing HCB that demonstrates a current interruption capability of 2000 A at a DC voltage of 1650 V with an interruption time of roughly 4 ms. Chapter 13 of this book describes a high-power active resonant zero-crossing HCB that demonstrates a current interruption capability of 25 kA at a DC voltage of 535 kV with an interruption time less than 3 ms [23]. Chapter 14 of this book describes yet another MVDC active resonant zero-crossing HCB scheme.

The second HCB subcategory is termed natural-commutation HCB. Under this subcategory, the commutation circuit is simply a semiconductor switch in parallel to the mechanical path (Fig. 2.11c). Upon the detection of a fault condition, the mechanical breaker opens and generates a switching arc. The arc voltage subsequently forces the fault current to commutate to the parallel semiconductor switch as it provides a less resistive path, resulting in the extinguishment of the arc itself. The semiconductor switch conducts the fault current for a period of time (typically 10–20 ms) until the mechanical breaker fully opens and regains its voltage blocking capability. The semiconductor switch then turns off and forces the MOV to clamp the transient voltage surge. Chapter 10 of this book describes a natural commutation HCB that demonstrates a current interruption capability of more than 11 kA at a DC voltage of 5 kV with an interruption time less than 2 ms. The natural commutation HCB scheme offers a very simple solution to extend the DC fault interruption capability of common mechanical circuit breakers. However, there are several limitations. First, the current commutation is facilitated by the arc produced across the contacts of the MCB, which results in contacts wear and a degraded lifetime. Second, the arc voltage across the mechanical contacts has a limited range, thus limiting this scheme to low- or medium-voltage applications. Third, the semiconductor switching device must conduct an excessively large fault current for a relatively long time (typically a few milliseconds) during the interruption process, leading to a significant cost and size penalty.

The third HCB subcategory is termed zero-current-switching (ZCS) forced-commutation HCB. In case of a fault, the current through the mechanical path is simply forced to zero either by turning off a lower-voltage series semiconductor switch (also known as the load commutation switch or LCS as shown in Fig. 2.11d) or by injecting a well-controlled counter current (Fig. 2.11e). Once the fault current is completely commutated from the mechanical path into the parallel commutation path, the mechanical switch can open arclessly under a zero-current condition. During the interruption process, the electronic path needs to carry the fault current until the mechanical switch fully opens and regains its full voltage blocking capability. At that instant the electronic path turns off and forces the MOV to clamp the transient voltage surge. ABB reported an LCS-type ZCS HCB that demonstrated a current interruption capability of 9 kA at a DC voltage over 80 kV with an interruption time less than 2 ms [24]. Chapter 11 of this book describes a counter-current injection type of ZCS commutation HCB that demonstrates a current interruption capability of 1 kA at a DC voltage of 6 kV with an interruption time of 0.5 ms. Chapter 12 of this book describes a similar ZCS commutation concept but with different power ratings and choice of the mechanical switch. The ZCS forced-commutation HCB scheme offers fast and arc-free fault interruption, long service lifetime, and low conduction loss (especially for the counter current injection type), and can be adopted in medium- to high-voltage DC power systems. Design complexity and cost are among its disadvantages.

4.4 Breakerless Fault Protection

The cost, size, and weight factors of the various DC circuit breakers mentioned above seriously limit their adoption in DC power systems. The concept of breakerless or converter-based protection thus becomes an attractive option for DC grids facilitated by power electronic interfacing converters, such as the naval shipboard power systems [17]. Those DC grids already have a large number of power converters to control and regulate normal power flows. It would be highly advantageous to use the same power converters to provide fault protection without using standalone circuit breakers, which would often compete with the main power converters in size, weight, and cost. Some power converter topologies, such as thyristor rectifier, dual-active bridge, and full-bridge modular multi-level converter (FB-MMC), inherently offer fault blocking capability. For example, the FB-MMC topology can block the DC terminal capacitance discharge into the short fault and maintain full control over the DC fault current while maintaining full charge of the sub-module DC capacitors. The FB-MMC topology provides bi-directional current control under either ac- and dc-side short circuit faults and offers significant advantages in fault protection. Fault-blocking or fault-tolerance capability can also be added to other converter topologies including the common two-level inverters with additional components and power loss. But the associated cost and efficiency penalty is likely only a fraction of that of a stand-alone DC breaker since the

existing hardware resources of the power converter, such as sensing and control as well as thermal management, are shared for the additional fault-blocking function. The breakerless protection concept is an ideal option for point-to-point DC power transmission with a fault-blocking power converter at each end of the transmission line. However, this cost-effective fault protection concept might not be universally applicable for all DC power architectures because not all power cables are directly controlled by a power converter. It is worth noting that DC circuit breakers and fault-blocking power converters can be combined in an optimal way to provide a cost-effective protection solution. Chapter 16 of this book provides a comprehensive overview of the breakerless protection concept.

4.5 Fault Current Limiters

The perspective or let-through fault current in a DC power system often exceeds the interrupting capability of the existing circuit breakers used. This is especially true in case of power system upgrade or reconfiguration. The purpose of a fault current limiter (FCL) is to limit the fault current magnitude to an acceptable level by inserting additional impedance so the downstream circuit breakers only need to interrupt a smaller perspective fault current [12]. The term fault current limiter or fault current limiting is sometimes used to describe fast-acting circuit breakers in the literature, causing confusion among the readers. In this book, an FCL is strictly defined as a protective device that limits rather than completely interrupts the fault current as in the case of a true circuit breaker.

Application of FCLs is a viable approach to reduce the fault current. Under normal operating conditions, an FCL retains low impedance so that the power flow is unaffected. In the event of a fault, however, the impedance of the FCL rapidly increases so the fault current rises to a lower peak value (e.g., three to five times the nominal load current) and at a lower *di/dt* rate, which can be safely interrupted by the existing CBs. Use of FCLs in DC power grids can significantly relax the current interruption requirement on various types of DC circuit breakers. FCLs may be classified by their principle of operation and key technological components used. Generally, FCLs can be implemented with passive nonlinear elements, inductive devices, vacuum switches, as well as using semiconductor and superconductor technologies. Superconducting and solid-state fault current limiters are two main FCL types for DC applications. In a superconducting FCL [25], the resistance or inductance of the superconducting element can change dramatically in the event of an excessive fault current. In a solid-state FCL, the increase in resistance or inductance is facilitated by a semiconductor switching circuit. Chapter 17 of this book provides a comprehensive overview of FCLs and their applications in DC power systems.

5 Concluding Remarks

This chapter briefly reviews fault currents from various types of DC sources, different fault detection technologies, and a wide variety of fault interruption technologies. A comparison of the fault interruption technical solutions in terms of advantages, disadvantages, and most suitable applications is summarized in Table 2.2.

Mechanical circuit breakers (MCBs) are a mature fault interruption technology offering low loss and cost. It is the standard solution for conventional AC power systems over the full voltage and current spectrum. With significant voltage/current derating, MCBs may also be used in some DC power systems. However, their distinct disadvantages of slow response (typically more than 20 ms), limited DC interruption capability, poor service lifetime due to arc erosion, and high let-through fault current limit their usage in modern DC power grids.

Solid-state circuit breakers (SSCBs) offer very fast response to faults (typically hundreds of microseconds), arc-free fault interruption, long service lifetime, and low let-through fault current and energy. However, their greatest weakness is the high ON-state power loss and the associated requirement for active cooling (liquid or forced air), leading to a large cost and complexity penalty. It is most likely that SSCBs provide a viable solution for relatively low power LVDC or MVDC systems (e.g., under 1 kV or 100 A). It becomes increasingly difficult to extend the SSCB concept into the high-power space as the DC voltage and current increase. It should be mentioned that low-loss passively cooled SSCBs are a viable and competitive solution for many LVDC applications (e.g., 380 V and 50 A). SSCBs are also considered as a fault protection solution for AC power applications, including 600 V/100 A fast-acting smart AC circuit breakers.

Hybrid circuit breakers (HCBs) combine the advantages of MCB and SSCB and offer a low loss, arc-free or arc-lite fault interruption, reasonable service lifetime, and moderate response time (1–3 ms). Their disadvantages include high cost and complexity as well as slower response than SSCBs. HCBs are expected to provide a viable solution for a wide range of high-power MVDC to HVDC power grids where moderate fault response is acceptable. However, it would be difficult for the existing HCB schemes to deal with the fast-rising fault current in some low-impendence DC power networks.

Fault current limiters (FCLs) limit the fault current magnitude to a manageable level so the interruption requirement for the downstream circuit breakers can be relaxed. FCLs and various types of circuit breakers may work together to offer an optimal protection solution in certain high-power MVDC to HVDC power grids, especially in case of system upgrade or reconfiguration. Note FCLs alone will not be able to isolate the fault.

Converter-based breakerless protection may offer a more cost-effective solution than other circuit breakers for certain DC grids with a large number of interfacing power converters. One of such examples is a point-to-point power transmission with a power converter at each end of the power line. However, one big challenge of the

Table 2.2 Comparison of different DC fault protection technologies

Technology	Advantages	Disadvantages	Applications
Mechanical Circuit Breaker (MCB)	Mature technology, low cost, low loss	Very slow (>20 ms), poor DC interruption capability, poor lifetime, high let-through fault current	Traditional AC power systems or limited DC applications with significant power deratings
Solid-State Circuit Breaker (SSCB)	Very fast (<0.1 ms), arc-free operation, long lifetime, low let-through fault current, low system stress	High loss, high cost, active cooling often required	LVDC or MVDC low-power DC systems or AC power systems that mandate ultrafast response
Hybrid Circuit Breaker (HCB)	Low loss, moderate speed (1–3 ms), arc-free or arc-lite operation, good lifetime	Moderate speed, high cost, high complexity	MVDC or HVDC high-power systems that accept moderate response
Fault Current Limiter (FCL)	Moderate power loss, natural response, relaxed CB requirements	Additional loss and cost, need separate CBs to isolate faults	High-power DC or AC power systems; grid capacity upgrade
Converter-based Breakerless Protection (Breakerless)	Adding fault-blocking capability to basic converters with small cost and efficiency penalty, more cost effective than standalone CBs	Applicable only to certain DC grids with a high level of converter controls	DC or AC power grids with a large number of interfacing converters (e.g., point-to-point power transmission)

converter-based solution is to ensure minimum fault impacts required by protection selectivity.

There is no single fault interruption technology that is universally optimal for all use scenarios. It is likely that two or more of the technologies will be used in combination in a power grid. The selection of appropriate fault interruption technology for a particular DC application is an extremely complex task which involves many design trade-off factors and mandates far more rigorous deliberation than the overly simplified summary here.

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Part II
Solid State Circuit Breakers

Chapter 3
ABB's Recent Advances in Solid-State Circuit Breakers

Li "Lisa" Qi, Xiaoqing Song, Thorsten Strassel, and Antonello Antoniazzi

1 Introduction

The need of easing and making the integration of distributed energy resources from renewables more effective is driving a new resurgence of DC in power distribution, which this time is feasible and convenient due to the recent developments in power electronics. On the other hand, DC power distribution raises tough challenges in terms of circuit protection, as fault current can be extremely large and growing at extremely high rate that conventional protection devices, e.g., electromechanical circuit breakers, cannot cope with. A viable solution to such protection needs is given by solid-state circuit breakers (SSCBs), exploiting the latest development of power semiconductor technology, such as low-losses IGCTs and WBG FET devices.

At present, a satisfactory technology fitting all SSCB applications has not yet emerged, but different design solutions are possible matching the various power ratings.

This chapter presents ABB's recent investigations on SSCBs based on optimized Si IGCTs, looking for the best fit for high power SSCBs, for rated currents in the range of kAs and rated voltage from 1 kV and up, and on presently available SiC FET devices, more suited for lower power SSCBs. The design of such SSCBs is

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discussed, from the selection of the power semiconductor device to the requirements for the gate drive circuit, the cooling system, the voltage clamping, and the protection control.

Finally, some application cases of SSCBs in DC microgrids and in DC power system for marine vessels are highlighted, with specific focus on the motivation for using SSCBs instead of conventional protection devices.

2 Solid-State Circuit Breakers

The interruption process and functions of components in a SSCB are briefly explained in this section. Section 3.6 gives theoretical analysis using IGCT-based SSCB as an example.

The conceptual diagram of a solid-state circuit breaker (SSCB) and the main functional units are illustrated in Fig. 3.1. Low on-state loss semiconductor devices ensure high efficiency at conducting condition and fast current interruption in case of faults. Differently from the application in power converters, switching losses are not relevant for SSCBs, possibly leading to different device designs and optimization. Several semiconductor devices can be connected in series and/or parallel to meet SSCB’s voltage and current requirements. Bidirectional power flow is typically controlled through arranging devices in antiparallel or in antiseries, as only a few 4-quadrants inherently symmetric devices (e.g., GaN HEMT) exist. Moreover, one can distinguish between turn-on only device (as thyristors) and turn-off devices (as MOSFETs, IGBTs, IGCTs). While thyristors or triacs could be used in AC applications, turn-off semiconductor devices are used more frequently in SSCBs

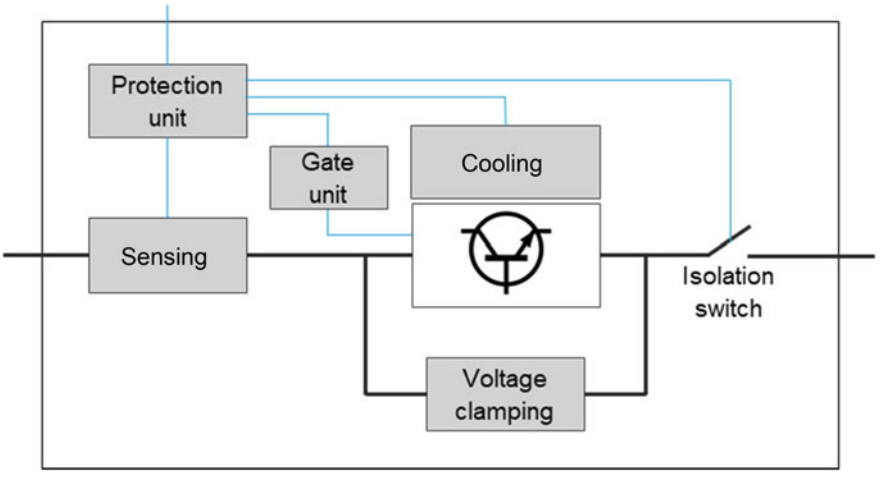

Fig. 3.1 Conceptual block diagram of a typical SSCB

for reasons of fault current limiting or for DC interruption. A SCCB concept has to take these device characteristics into account and compensate potential drawbacks to match the application needs. Sections 3 and 4 describe two SSCB architectures based on different semiconductor devices.

A voltage clamping circuit (e.g., a Metal Oxide Varistor (MOV)) is used to limit the temporary overvoltage when the semiconductor switches are turned off and to absorb the inductive energy of the grid, which could be a challenge especially in connection with large current limiting inductive elements. A cooling system, e.g., a heat sink with or without fans, or liquid-cooled cold plates for high power devices, keeps the temperature of the junction in the safe area. Due to safety requirements, e.g., in case of maintenance, a mechanical contact system is used to provide air-gap galvanic isolation. The protection unit controls the power semiconductor device, through the gate unit, and the isolation switch, providing protection functions, including fault detection, location, and protection coordination, as well as auxiliary functions such as measurement and communication.

Different designs of these functional units are described in the following sections.

3 Design and Development of IGCT-Based SSCBs

3.1 Selection of Semiconductor Devices

High power Silicon Integrated Gate-Commutated Thyristors (IGCTs) are good candidates for fully controllable bidirectional SSCBs, in particular for high power applications, with large rated current in the range of 1 kA+ and rated voltage in the upper end of the LVDC range. Most typical IGCT is asymmetrical (A-IGCT) and requires a diode in series to block the reverse voltage; alternated configurations with the diode in parallel to the IGCT are not suitable for bidirectional switching. Reverse Blocking IGCT (RB-IGCT) has been optimally designed to provide very low conduction losses and both forward and reverse blocking capability [2, 3]. The electrical characteristics of the selected RB-IGCT are the following:

Forward blocking voltage:	2500 V
Reverse blocking voltage:	−2500 V
Voltage drop (&1000 A):	0.9 V

Figure 3.2 shows the topologies of bidirectional switching blocks based on antiparallel A-IGCT and RB-IGCT, whereas the conduction loss profiles of bidirectional switching blocks based on A-IGCTs, RB-IGCTs, and IGBTs are compared in Fig. 3.3. The low conduction loss achieved with the optimized RB-IGCT up to 3000 A confirms that it is an appropriate choice for SSCB applications.

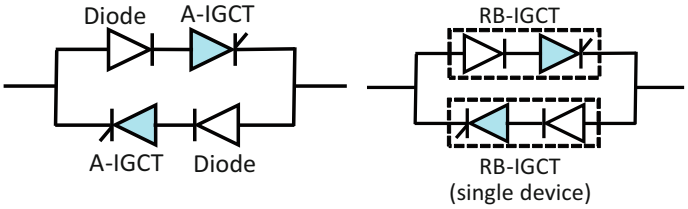

Fig. 3.2 A-IGCTs and RB-IGCTs for bidirectional switching [4]

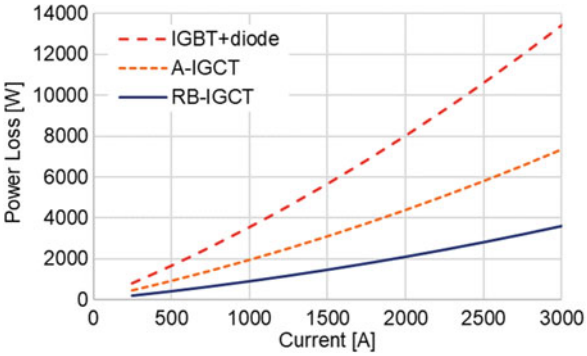

Fig. 3.3 Conduction loss profile of A-IGCT, RB-IGCT, and IGBT bidirectional switches [4]

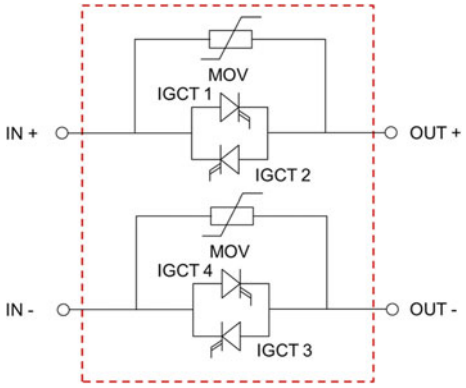

Fig. 3.4 Circuit diagram of a two-pole RB-IGCT SSCB (the isolation switch is omitted) [4]

A two-pole SSCB can be built using two RB-IGCT switches on the positive and the negative conductor, as illustrated in Fig. 3.4. The efficiency of such two-pole RB-IGCT SSCB, as given in Fig. 3.5, is higher than 99.9% for currents up to 1500 A. More antiparallel switches can be connected in parallel for higher nominal currents.

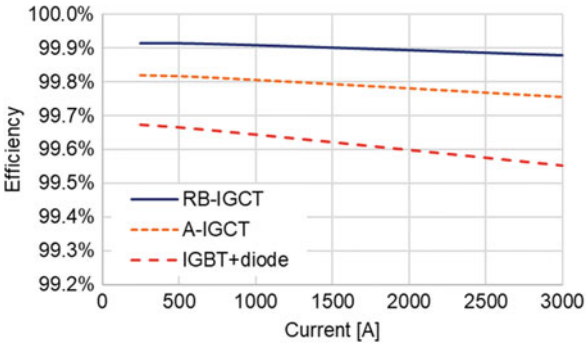

Fig. 3.5 Efficiency profile of the two-pole SSCB using RB-IGCT, A-IGCT, and IGBT [4]

3.2 Voltage Clamping

After an RB-IGCT SSCB is turned off, the energy accumulated in the system inductance needs to be dissipated to avoid the resulting overvoltage can damage the semiconductor device. This energy dissipation is achieved by a MOV, which is a nonlinear device providing high impedance at "low" voltage level, i.e., at the system voltage, and low impedance at "high" voltage level, i.e., at the max. allowed voltage. In this way, the MOV only conducts a very low leakage current at the normal operating voltage and clamps the voltage to a level that does not damage the RB-IGCTs when they are turned off to interrupt the fault current. The detailed description of the interruption sequence can be found later in Sect. 3.6.

Figure 3.6 shows the voltage-current characteristics of the selected MOV for the RB-IGCT SSCB, with a diameter of 108 mm and a thickness of 7.3 mm, corresponding to a residual voltage of 2180 V at 5000 A and a leakage current smaller than 1 mA at 1 kV; the maximum energy capacity is 10.7 kJ (95 J/cm^3). Thanks to the low inductance of the clamping circuit connecting the MOV, the overvoltage peaks are limited below the RB-IGCT's maximum blocking voltage of 2500 V. The MOV has been protected in a sealed packaging to withstand harsh environmental conditions.

3.3 Cooling and Mechanical Design

Due to RB-IGCT's relatively low losses, both air cooling and liquid cooling are suitable even for this high-power SSCBs. It is commonly known air-cooled systems tend to be bulkier than liquid-cooled systems, but they eliminate the need for auxiliary components such as heat exchangers, external coolant connections, etc. which are typically not considered in the comparison. One implementation of an air-cooled RB-IGCT SSCB is described in the following.

To improve the power density of the circuit breaker, despite the condition to use air to dissipate the losses, a two-phase cooling system was selected. Pulsating Heat

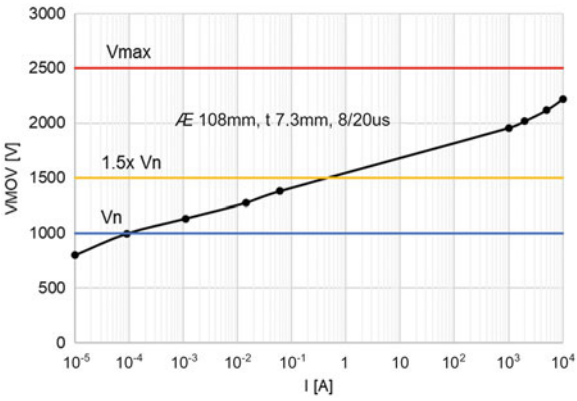

Fig. 3.6 Voltage-current characteristics of the MOV of the RB-IGCT SSCB [4]

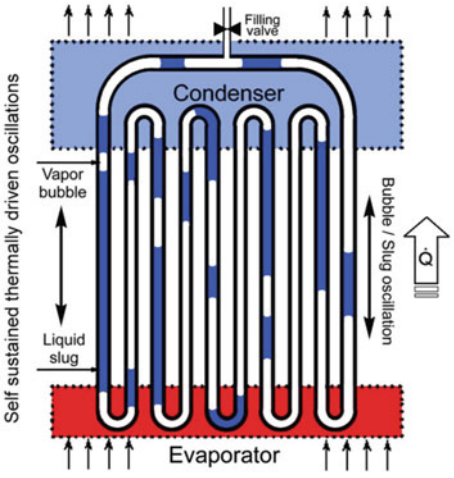

Fig. 3.7 Schematic of a pulsating heat pipes with the three different sections: evaporator, adiabatic, and condenser [7]

Pipes (PHPs) have been preferred over thermosyphons as they offer orientation-free performance, whereas thermosyphons’ efficiency is reduced when tilted. Independence from orientation is required in some applications, e.g., for shipboard systems due to the roll and pitch of the ships. PHPs have been demonstrated [6] and a schematic diagram is shown in Fig. 3.7 [7], and a customized PHP was designed to meet the unique requirements of the RB-IGCT SSCB [4, 8].

RB-IGCTs are puck-type devices that enable cooling on both surfaces. Furthermore, each pole requires two antiparallel RB-IGCTs. The stack was designed so that the RB-IGCTs (in blue) and the MOV (in grey) are in mechanical series while being in electrical parallel as illustrated in Fig. 3.8. This design allows active cooling of the MOV from the adjacent PHPs (in green), which is beneficial in case of fast repetitive interruption operations of the breaker, when the MOV needs to dissipate relatively large energy. This layout also permits a small amount of heat to be conducted through the MOV and dissipated by the up/downstream PHPs.

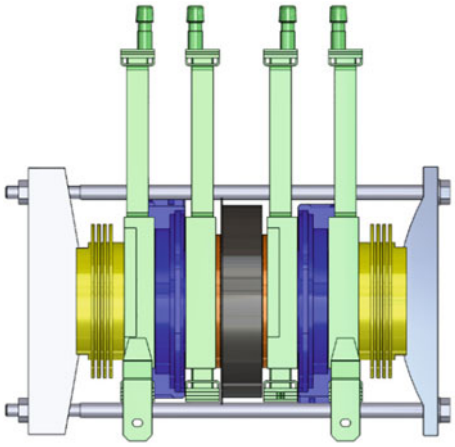

Fig. 3.8 Mechanical layout of one pole of the RB-IGCT SSCB [6]

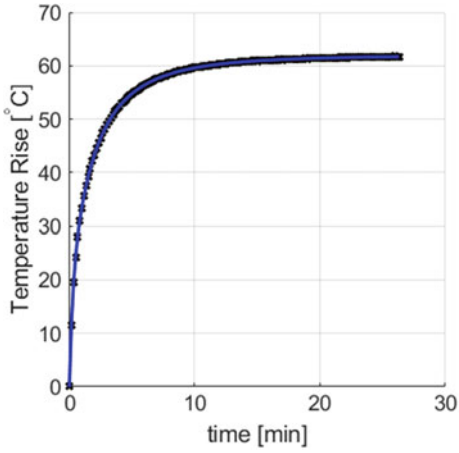

Fig. 3.9 Baseplate temperature rise of test article during 1500 A heat run [4]

Referring to Fig. 3.8, air is flowing in a duct (not shown) across the condensers of the PHPs. As the two condensers are in series in the air flow, thermal stacking may occur. This is not an issue in steady state, as only one IGCT is conducting at any moment, whereas transient thermal stacking, when the direction of conduction is inverted, can be more significant and requires additional margin in the design of the heat sinks. A heat run of the SSCB at 1500 A constant current is shown in Fig. 3.9. Finally, in bipolar circuit breakers, the gate units of the IGCTs on the two poles are interleaved to minimize the overall footprint of the SSCB.

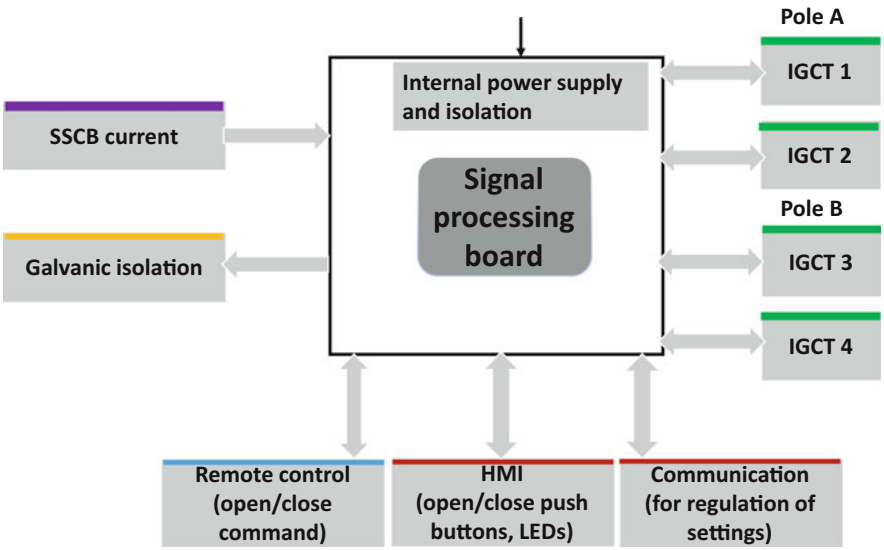

Fig. 3.10 Trip unit control board architecture

3.4 Control and Auxiliary System

In order to implement multiple functions of a SSCB (measurement, protection, control, monitoring, and communication), a microcontroller board was developed, which architecture is illustrated in Fig. 3.10. The trip-unit is designed to handle:

- The current sensor
- The galvanic isolation switch
- Control signals to the RB-IGCTs
- Feedback signals from the RB-IGCTs gate drivers
- The HMI panel with command buttons and indicators
- Interlock signals between different SSCBs
- Communication signal for status monitoring and tuning of the SSCB settings

The RB-IGCT gate drivers are controlled by fiber optics signal from the control board. An interlock signal is also travelling through fiber optic cables between the upstream and downstream SSCBs to allow protection coordination for selectivity. The measurement from the current sensor is processed by a signal conditioning circuit on the control board before being sent to the microcontroller.

The isolation switch provides galvanic isolation via air-gap, so that the SCCB ensures the same electrical safety for maintenance as electromechanical circuit breakers. The operation of the isolation switch is coordinated with the control of RB-IGCTs, to ensure arc-free operation at zero current by means of proper closing and opening sequences:

- Closing: the galvanic-isolation switch closes first, and then the ON signal is sent to the RB-IGCTs.
- Opening: the RB-IGCTs are turned-off first, and then the galvanic-isolation switch opens.

One primary function of the control board is to measure the current for short circuit and overload protection. A shunt resistor made of Manganin, chosen for its low temperature coefficient of resistance and long-term stability, was adopted for current measurement of the RB-IGCT SSCB. The shunt resistance value was selected to be 15 μΩ and can cover both the nominal current of 1500 A and overcurrent exceeding 5000 A.

When the time derivative of the fault current is large, the current measurement is affected by significant error due to the non-negligible stray inductance on the measuring path. The voltage measured by the microcontroller ADC (Analog Digital Conversion) is the sum of the actual voltage drop on the shunt resistance $R_{\text{shunt}} \cdot i_{\text{actual}}$ and the bias from the stray inductance $L_{\text{shunt}} \cdot \frac{di_{\text{actual}}}{dt}$, where R_{shunt} is the shunt resistance, L_{shunt} is the parasitic inductance, and i_{actual} is the actual current. The effect on the measured current i_{meas} is given in (3.1).

$$i_{\text{meas}} = i_{\text{actual}} + \frac{L_{\text{shunt}} \frac{di_{\text{actual}}}{dt}}{R_{\text{shunt}}} \tag{3.1}$$

Therefore, to reduce the measurement error, the stray inductance should be kept minimum or as low as possible.

A dedicated auxiliary power supply was developed to guarantee both the correct current profile and timing requested at start-up (34 V – 1 A steady, 8 A peak), and the insulation level to account for allowable system transient voltage level and the SSCB opening.

3.5 Experimental Validation

A test circuit for the RB-IGCT SSCB is illustrated in Fig. 3.11. Because of the ultrafast fault-current rising and response time of the device, the test circuit was designed to provide high current for less than 1 ms. Therefore, the test circuit can be implemented by an LC circuit with a capacitor bank and an adjustable air core inductance to emulate system inductance. The capacitance is sized to provide sufficiently high fault energy and short circuit current (e.g., current peak higher than 5 kA or more); the inductance L_{sys} can be adjusted from 30 to 200 μH to perform tests at different fault-current derivatives. Figure 3.12 shows the experimental setup of the short circuit test circuit. To perform the short circuit test, the capacitor bank is first pre-charged to 1 kV voltage by a High Voltage (HV) Low Current (LC) power supply, and then the power supply is disconnected and the RB-IGCT SSCB is closed.

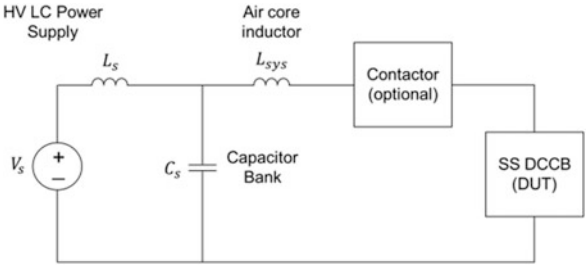

Fig. 3.11 Test circuit for the RB-IGCT SSCB [1]

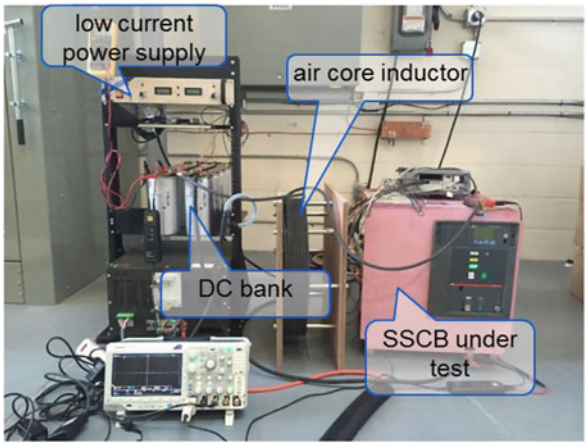

Fig. 3.12 Experimental setup of the test circuit [1]

Figure 3.13 shows the SSCB current and voltage from the short circuit testing when the system inductance is equal to 65 μH. After the circuit is closed, the fault is first detected at ~180 μs, and then the RB-IGCTs turn off within 5 μs. The fault current is limited and commutated to the MOV. The MOV dissipates the inductive energy and reduces the fault current to zero in ~190 μs. The overall breaking time, from the fault occurrence until the fault current goes to zero, is ~370 μs. Figure 3.14 illustrates the short circuit test results with the system inductance increased to 140 μH. As the fault current takes longer time to reach the threshold, the fault detection time is longer, and the RB-IGCTs are turned-off at ~390 μs. Similarly, as the stored energy is higher, it takes longer time (~ 370 μs) to discharge it across the MOV. The total breaking time is ~760 μs. Note that RB-IGCTs turn-off time, from the detection of the fault to the commutation of the current on the clamping circuit, is not affected by L_{sys}.

Protection coordination between two SSCBs was also tested with the test circuit in Fig. 3.15. The overcurrent threshold was set to 3 kA for the upstream SSCB CB1, and to 2 kA for the downstream SSCB CB2; therefore, at short circuit faults, CB2 is supposed to interrupt the fault current before CB1 takes any action. Figure 3.16 presents the current and voltages on CB1 and CB2 from one test with the system inductance adjusted to 200 μH: the voltage on CB2 raises when this SSCB opens and is then clamped by its MOV, whereas voltage on CB1 remains zero as this SSCB

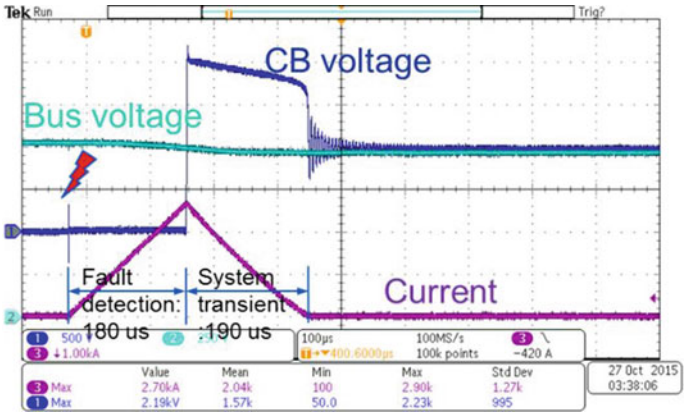

Fig. 3.13 Short circuit test result with low system inductance (65 µH) [1]

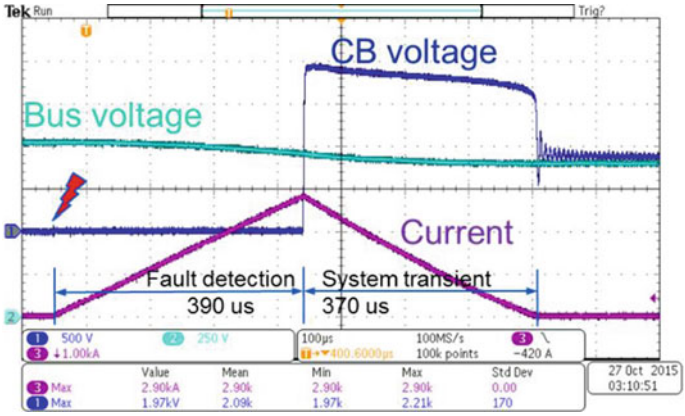

Fig. 3.14 Short circuit test result with high line inductance (140 µH) [1]

stays closed. Selectivity can be more difficult to achieve at higher current derivative. To avoid unwanted tripping of the upstream breaker CB1, when the trip unit in the downstream breaker CB2 sends the turn-off command to the RB-IGCT, it also sends an interlocking signal to CB1 blocking its false tripping.

ABB has unveiled a commercial solid-state circuit breaker, named SACE Infinitus, based on RB-IGCT technology, with rated voltage 1000 V and rated current 2500 A, employing a liquid cooling system [27].

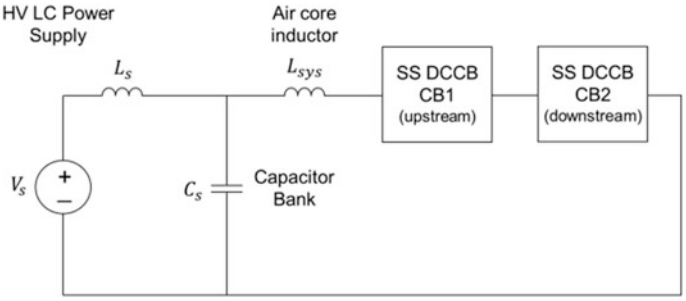

Fig. 3.15 Test circuit for protection coordination between two IGCT SSCBs [1]

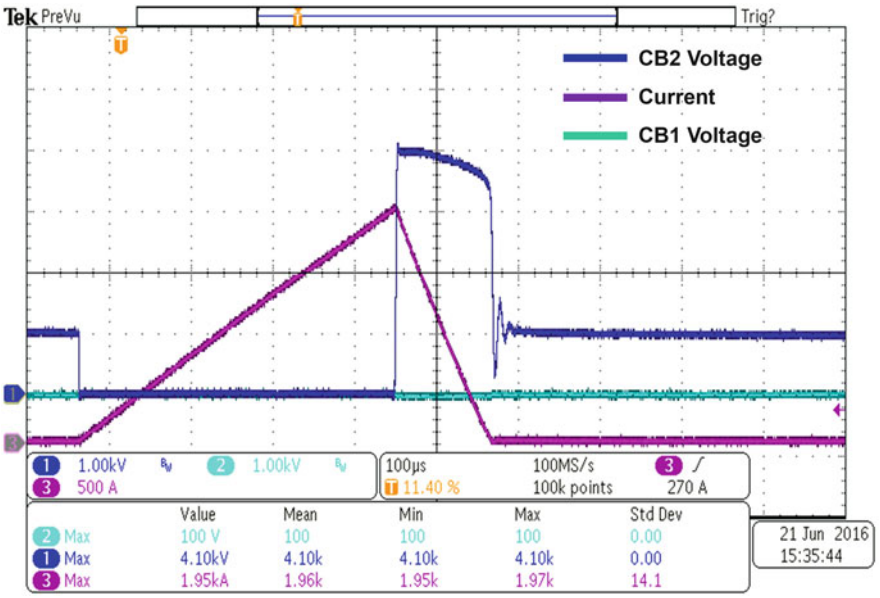

Fig. 3.16 Protection coordination test results [1]

3.6 Model-Based Design

SSCB breaker design is a tedious process and involves multiple components. A model-based design provides deep insights into the SSCB protection process and theoretical foundation for selecting parameters of each component inside the breaker. SSCB can be employed for overcurrent protection, to prevent consequent damages in grids where fault energy and current can be high. In DC applications, fault current can have large *di*/*dt* and rapidly rise to peak value within a few microseconds. Additionally, overcurrent and thermal limit of semiconductors on DC fault path are much lower than traditional power system equipment and devices.

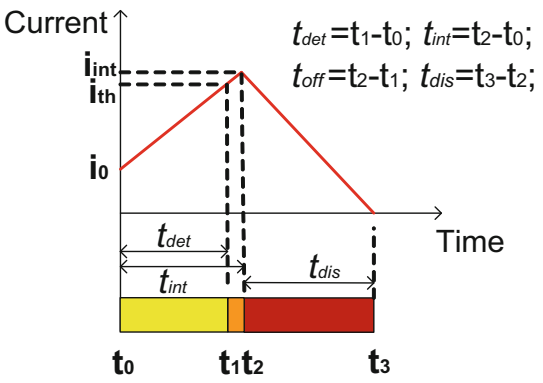

Fig. 3.17 Decomposition of a complete SSCB protection process [5]

Once a fault is detected, SSCB can react with ultrafast turnoff speed to interrupt DC current before it reaches dangerously high magnitude. Maximum allowable *di/dt* indicates the maximum rate of rise of the fault current the SSCB can interrupt in low-inductance grid (or low-inductance faults), while minimum *di/dt* gives indication on the maximum energy the SSCB can handle in high-inductance grid (or high-inductance faults). Proper system design can help reach a compromise for SSCB between required protection speed and energy dissipation.

The critical current rate of rise *di/dt* which can be handled by the circuit breaker is a more relevant indicator of the short circuit interruption performance of a SSCB than its breaking capacity, i.e., the maximum prospective current that it is capable of breaking, typically used for electromechanical circuit breakers.

The time decomposition of a complete protection process by a SSCB is illustrated Fig. 3.17. Considering ultrafast fault interruption speed by SSCBs, the DC fault current can be approximated as a linearly increasing current before the fault interruption. The protection starts from t_0 when the current is i_0. When the fault current increases to its threshold value i_{th}, the fault is detected and the fault detection time is t_{det}. t_{off} is the SSCB opening delay. i_{int} is the peak fault current after all delays in fault location and breaker opening. The fault interruption time is t_{int}. After the fault interruption, the fault current starts to decrease. t_{dis} is the energy dissipation time of the MOV.

The equivalent circuits during the complete SSCB DC fault protection process are illustrated in Fig. 3.18. R_{eq} and L_{eq} are equivalent system resistance and inductance. During the fault interruption and energy dissipation, the DC fault current flows through the semiconductor switch and MOV, respectively. When the switch is on, its resistance is combined into R_{eq}. When the MOV is on, it is approximated as a voltage source and a resistor, whose values V_{mov} and R_{mov} are derived from the linearization of its voltage-current characteristics at the SSCB's interruption current.

Equations (3.2) and (3.3) describe the two equivalent circuits at fault interruption and energy dissipation. The interruption time and the fault peak can be approximated by (3.4) and (3.5). The dissipation time and energy can be calculated from (3.6) and (3.7). Equations (3.6) and (3.7) are complex and difficult to see major impacting factors. Because of the high fault-current derivative, the voltage drops at the fault

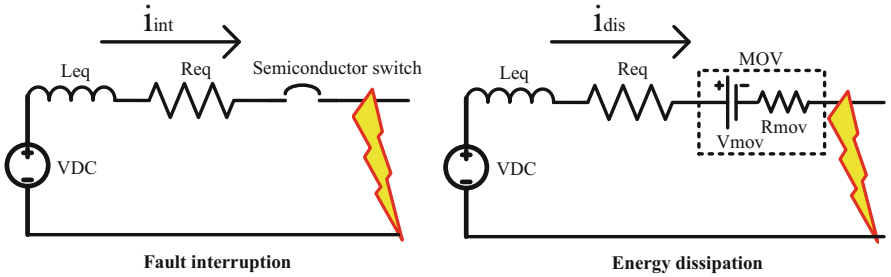

Fig. 3.18 Equivalent circuits during a SSCB protection [1]

resistance are much smaller than the drop on the fault inductance. If R_{eq} and R_{mov} are ignored from (3.6) and (3.7), then the dissipation time and energy can be estimated by (3.8) and (3.9). From (3.8) and (3.9), the energy dissipation time becomes longer with higher system inductance or with lower MOV clamping voltage. The dissipated energy is higher with higher inductance and higher clamping voltage.

$$V_{DC} = R_{eq} i_{intp} + L_{eq} \frac{di_{intp}}{dt} \tag{3.2}$$

$$V_{DC} = R_{eq} i_{dis} + L_{eq} \frac{di_{dis}}{dt} + V_{mov} + R_{mov} i_{dis} \tag{3.3}$$

$$t_{int} \approx \frac{i_{th} - i_0}{\frac{V_{DC}}{L_{eq}}} + t_{off} \tag{3.4}$$

$$i_{int} \approx i_{th} + \frac{V_{DC}}{L_{eq}} (t_{off}) \tag{3.5}$$

$$t_{dis} \approx -\frac{L_{eq}}{R_{eq} + R_{mov}} \ln \left(-\frac{V_{DC} - V_{mov}}{(R_{eq} + R_{mov}) i_{int} - V_{DC} + V_{mov}} \right) \tag{3.6}$$

$$\begin{aligned} E_{dis} \approx & \left(V_{mov} \frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} + R_{mov} \left(\frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} \right)^2 \right) t_{dis} \\ & + R_{mov} \left(i_{int} - \frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} \right)^2 \frac{e^{-2 \frac{R_{eq} + R_{mov}}{L_{eq}} t_{dis}} - 1}{-2 \frac{R_{eq} + R_{mov}}{L_{eq}}} \\ & + \left(i_{int} - \frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} \right) \left(V_{mov} + 2 R_{mov} \frac{V_{DC} - V_{mov}}{R_{eq} + R_{mov}} \right) \frac{e^{-\frac{R_{eq} + R_{mov}}{L_{eq}} T_{dis}} - 1}{-\frac{R_{eq} + R_{mov}}{L_{eq}}} \end{aligned} \tag{3.7}$$

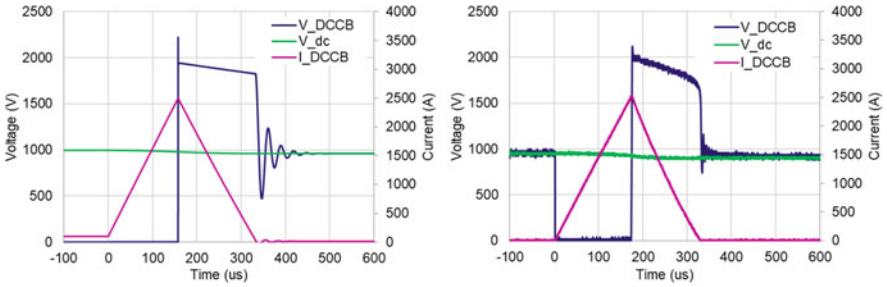

Fig. 3.19 Side-by-side comparison of simulated and experimental short circuit test results of RB-IGCT SSCB [6]

$$T_{\text{dis}} \approx \frac{L_{\text{eq}} i_{\text{int}}}{V_{\text{mov}} - V_{\text{DC}}} \tag{3.8}$$

$$E_{\text{dis}} \approx \frac{1}{2} \frac{L_{\text{eq}} {i_{\text{int}}}^2 V_{\text{mov}}}{V_{\text{mov}} - V_{\text{DC}}} \tag{3.9}$$

The equivalent circuits in the DC protection can be simulated in Matlab/Simulink. Figure 3.19 compares the simulation results and the experimental results when the system inductance is equal to 65 μH. The simulation results are quite close to the experimental results except some differences in the MOV performance. The errors are expected since the nonlinear characteristics of the MOV are approximately by a linear circuit (a reactance behind a voltage source) within its dominant operation zone. In this simulation, V_{mov} and R_{mov} are set to 1952 and 0.0282, respectively [6].

The above equations can be used to interpret and analyze the interactions between the protected DC system and the SSCB-based DC protection. The time delay t_{off} normally is quite small and thus can be neglected. From (3.4) and (3.9), the fault-interruption time and energy-dissipation time are proportional to the system inductance. This has been verified by the previous experimental test results. In the experimental validation, two different system inductance values 65 and 140 μH are used. Because the fault interruption time and energy dissipation time are linearly increasing with the inductance value, the breaking time for 140 μH is roughly doubled compared to the time for 65 μH. If the system inductance is low, the fault detection needs to be completed within short time frame, which is more challenging. From (3.8) and (3.9), the MOV dissipation time and energy are linearly increasing with the system inductance. The SSCB dissipates less energy and the fault current

is reduced to zero faster. On the other hand, the fault interruption time, energy dissipation time, and energy are all in reverse proportional to the DC system voltage. If the system voltage is high, the allowed fault detection time is short, but the energy to be dissipated is lower, and thus it takes less time for the SSCB to dissipate the energy.

4 Design and Development of SSCBs Based on SiC Unipolar Devices

IGCTs have very low conduction voltage drops at high current levels, thanks to the strong conductivity modulation in the thyristor type semiconductor switches, making them a good candidate for high current SSCBs. However, IGCTs do not fit very well with low current SSCBs, because of their low-current behaviors. The forward voltage, indeed, does not tend to zero at very low current but to a minimum value (~0.5 V for the RB-IGCT described in the previous section) dependent on its design.

Semiconductor devices with resistive characteristics, such as MOSFETs, fit very well for such application, in particular those based on Wide Bandgap (WBG) semiconductors that offer lower conduction resistances and higher voltages.

Table 3.1 summarizes and compares some key properties of 4H-SiC and GaN WBG materials compared with Silicon [9]. SiC and GaN have ~3× larger bandgap compared to conventional Si. Because of their larger bandgap, GaN and SiC can withstand ~10× larger breakdown electric field, resulting in devices with higher (>10 times) blocking voltage and lower (>300 times) conduction resistances compared to silicon devices.

Equation (3.10) shows the ideal specific resistances of the unipolar power semiconductor resistances with different blocking voltages [10].

$$R_{\text{on\_sp,ideal}} = \frac{4\,\text{BV}^2}{\varepsilon_S \mu {E_{\text{br}}}^3} \tag{3.10}$$

where BV is the blocking voltage of the power devices, ε_S is the semiconductor permittivity, μ is the electron mobility, and E_{br} is the breakdown electric field. Substituting the semiconductor properties into (3.10), it can be seen that the SiC-based power semiconductor devices could achieve ~300× lower conduction resistances compared to the Si-based power devices as shown in (3.11).

Table 3.1 Semiconductor material properties

Semiconductor materials	Si	GaN	4H-SiC
Bandgap (eV)	1.1	3.4	3.3
Electron mobility ($\text{cm}^2\text{v}^{-1}\ \text{s}^{-1}$)	1400	1200	1000
Breakdown electric field (MV/cm)	0.3	3.3	2.5

$$R_{\text{on\_SiC}} \approx \frac{1}{300} R_{\text{onSi}} \tag{3.11}$$

As conduction losses are the major contribution to the SSCB power losses, SiC and WBGs strongly reduce SSCB power losses and heat dissipation, also making cooling a lot easier.

4.1 SiC JFET vs. SiC MOSFET

The two most common types of SiC power devices are Junction Field Effect Transistor (JFET) and Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET). At device level, the main difference between the two is that JFETs are usually depletion-mode devices that are normally-on, which means they can conduct current when no voltage is applied at gate, while MOSFETs are mostly enhancement-mode devices that are normally off, meaning they are in blocking mode at zero gate voltage.

In terms of conduction losses, SiC JFETs are deemed to have lower specific resistance compared with SiC MOSFET. Figure 3.20 shows the simplified device structure of the SiC JFET and SiC MOSFET. For SiC JFET, the majority resistances include the JFET region resistance (R_{JFET}), drift region resistance (R_{Drift}), and substrate resistance (R_{sub}), while the SiC MOSFET device structure has additional channel resistance (R_{Ch}) as shown in (3.13).

$$R_{\text{on\_JFET}} = R_{\text{JFET}} + R_{\text{Drift}} + R_{\text{Sub}} \tag{3.12}$$

$$R_{\text{on\_MOSFET}} = R_{\text{Ch}} + R_{\text{JFET}} + R_{\text{Drift}} + R_{\text{Sub}} \tag{3.13}$$

Without channel resistances, the SiC JFETs can achieve lower specific resistance compared to SiC MOSFETs. Depending on the channel mobility and voltage rating, the channel resistance (R_{Ch}) could take up to 30% of the total resistances [10], which means SiC JFETs have potentials to achieve up to 30% lower resistances compared to SiC MOSFETs at certain voltage levels.

However, the absence of the inversion channel in SiC JFETs also leads to higher temperature coefficient of on-resistance compared to SiC MOSFETs. The channel resistance usually has negative temperature coefficient due to the higher electron mobility at elevated temperatures while the JFET region resistance, drift region resistance, and substrate resistance all have positive temperature coefficient. In SiC JFET, there is no inversion channel to offset the positive temperature coefficient of the JFET, drift layer and substrate, leading to a higher overall temperature coefficient [11].

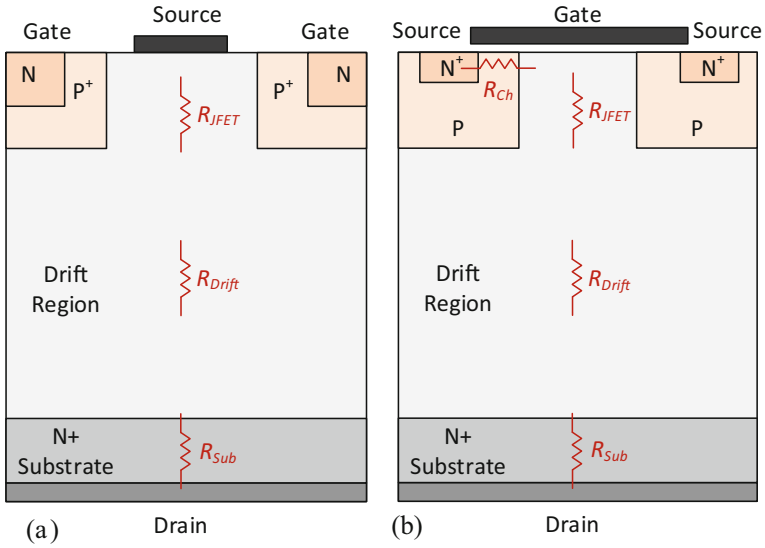

Fig. 3.20 Simplified device structure and major resistances of SiC JFETs and SiC MOSFETs. (**a**) SiC JFET; (**b**) SiC MOSFET

4.2 A Low Resistance SiC JFET Module

Figure 3.21 shows an example of a low resistance SiC JFET module, developed by ABB [12]. By paralleling four SiC JFET dies in parallel, the fabricated SiC JFET module has 4.2 mΩ total resistance from drain terminal to source terminal. The packaging of this SiC JFET module was carefully considered and designed to achieve a lower parasitic inductance and high temperature operation. For example, instead of soldering, the dies were sintered to direct bonded copper (DBC) with silver paste to withstand higher temperature. Two 10 mil aluminum (Al) wire bonds were used to connect source of the SiC JFETs to the DBC traces.

To better understand and optimize the packaging, the parasitic resistance of the module (such as DBC trace resistance, solder resistance, terminal resistance, bond wire resistance, contact resistance as shown in Fig. 3.22a) as well as the SiC chip on-state resistance are measured. Figure 3.22b shows the resistance distribution of the fabricated SiC JFET module. It is found that the bond wire and contact resistance contribute significantly to the module resistance. The total resistance of the wire bonding is 0.85 mΩ, consisting of 0.37 mΩ wire bond to chip source metallization contact resistance, 0.23 mΩ wire bond to DBC contact resistance, and 0.25 mΩ Al wire equivalent resistance. It is important to further optimize wire bonding to achieve low module resistances.

4.3 Reverse Conduction and Reverse Blocking Characteristics of SiC JFETs

While the forward conduction and blocking characteristics of the SiC JFETs are well known and tested, the 3rd quadrant characteristics including the reverse conduction and reverse blocking characteristics are often neglected and rarely studied. The SiC JFET's 3rd quadrant characteristics need to be better understood for bidirectional SSCB application, which requires to conduct and interrupt bidirectional currents.

Figure 3.23 shows the reverse conduction characteristics of the SiC JFETs compared with its forward conduction characteristics, all tested at room temperature with −2 V to +2 V gate voltages. At 1 ~ 2 V gate voltages, the reverse conduction resistances have similar values with forward conduction. When a slightly negative gate voltage (e.g., −2 V) is applied, the SiC JFET will saturate at a lower current during forward conduction, while reverse conduction demonstrates no saturation at much higher current levels (up to 50 A). An explanation of this phenomenon can be found in [13].

Figure 3.24 shows the tested SiC JFET's reverse blocking characteristics with gate voltages varying from 0 V to −10 V. The SiC JFET has no reverse blocking capability, even with very negative gate voltages (e.g., −10 V). With a more negative gate voltage (<−4 V), the reverse conduction voltage drop will also increase. The relationship between the negative gate bias voltage and the reverse conduction voltage can be found in [13].

4.4 Cooling System Design

Although the SiC power devices can achieve much lower conduction resistances compared to the Si counterparts, one remaining design challenge of SiC-based SSCBs is the cooling system, because of the still high power losses compared

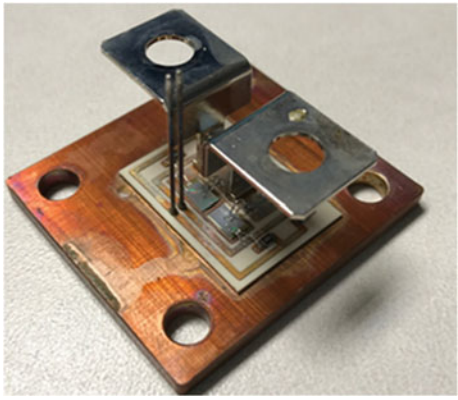

Fig. 3.21 The in-house developped low resistance (4.2 mΩ) SiC JFET module picture [12]

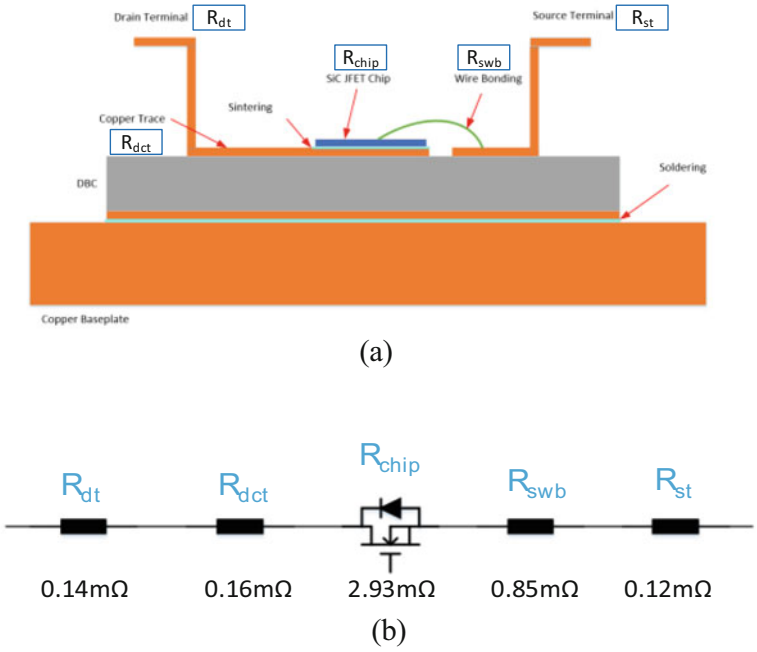

Fig. 3.22 The distribution of parasitic resistances of the fabricated SiC JFET module. (**a**) The constituent resistance of the SiC JFET package; (**b**) the measure value of the parasitic resistances [12]

to conventional mechanical breakers. For example, power losses for a typical electromechanical 250 A MCCB are around 5 W, while they are 5 times larger or more for a SSCB.

SiC power devices usually have small chip sizes and compact module design to reduce parasitic capacitances and inductances, which is beneficial for higher frequency operation in power converters. In addition, such modules can only be cooled through the baseplate, whereas in IGCTs the heat can be extracted from both sides. These pose an additional challenge in designing the cooling system that shall be able to manage higher heat flux. Heat pipes or vapor chambers can be used to distribute the heat over a larger heat sink. Figure 3.25 illustrates the cooling options for SSCBs, considering both the overall power to be dissipated and the heat flux across the heat exchange surface.

Thermal design is especially challenging when considering the overload condition. For example, in a standard Type C trip curves for electro-mechanical breakers, the breaker needs to withstand overload current, such as four times the nominal current ($4\times I_N$) for at least 1 s, $3\times I_N$ for 2 s and $2\times I_N$ for 6 s. During the overload conditions, significant amount of heat in SSCBs is generated, for example, under $4\times I_N$, at least $16\times$ more losses are generated and need to be dissipated effectively.

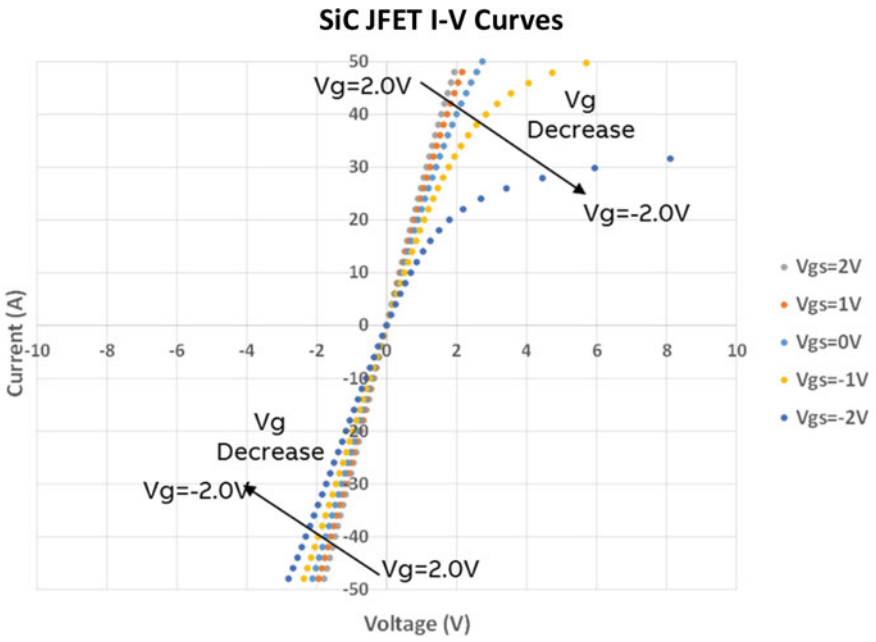

Fig. 3.23 Comparison of the SiC JFET forward conduction and reverse conduction characteristics with different gate voltages [13]

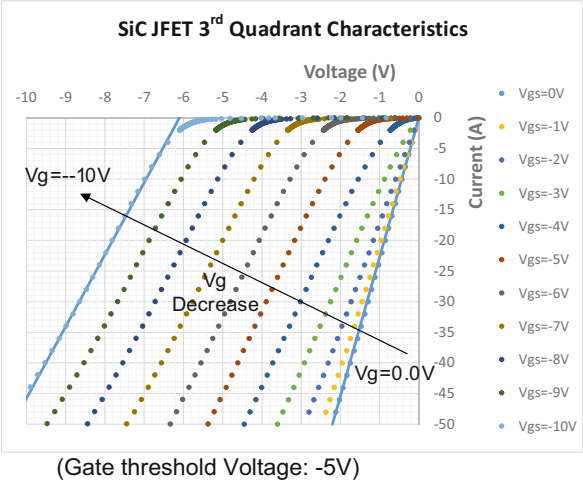

Fig. 3.24 SiC JFET reverse blocking characteristics with gate voltages varying from 0 V to −10 V [13]

Different ways can be used to handle such overload conditions, like derating the semiconductor device adequately to lower the loss or optimizing the cooling system design (e.g., larger heat-sink sizes, liquid cooling instead of forced air convection, etc.). The first approach will lead to a significant cost increase due to the high prices

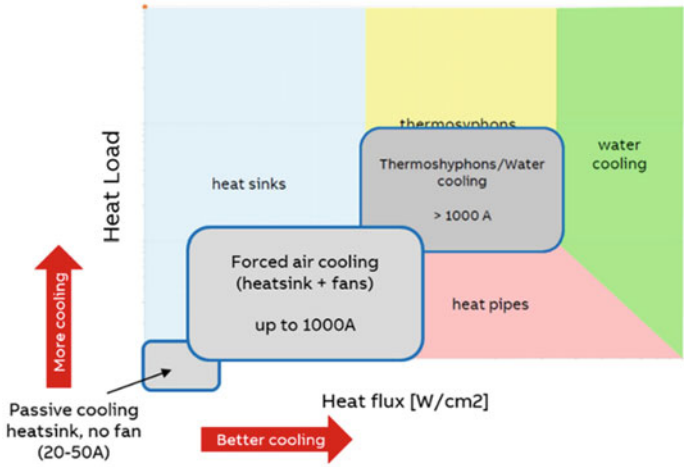

Fig. 3.25 Cooling options for solid-state circuit breakers

of semiconductor devices, whereas the second is more cost-effective in most cases. However, constraints from different applications need to be considered, such as form-factor, noise-levels, maintenance, etc., which can reduce design choices and the performance achievable from the thermal system.

One interesting method to address the large heat dissipation under overload conditions is the adoption of a phase-change material (PCM). The latent heat of the phase change process of the material allows it to absorb significant amount of energy for a relatively small change in temperature. This provides an increased thermal capacitance (lower transient thermal impedance) in the thermal network, which can help to reduce the case temperature and in turn, the junction temperature of the device. A material with phase-transition temperature slightly higher than the steady-state operating temperature of the breaker under nominal current shall be selected, to ensure that it is activated only when an overload occurs.

Figure 3.26 shows one design example of the PCM-based heat sink to address the overload conditions. In HS2, the PCM was filled at the bottom of the fins to provide less thermal resistance during normal conditions. Both HS1 and HS2 temperature rise quickly under the overload current. After the PCM in the HS2 is activated at ~50 °C, a slower temperature rise compared to the heat sink without PCM (HS1) can be found in Fig. 3.27. This is because PCM is adding thermal mass to the cooling system to provide greater system time constant and slow down the temperature rise to the thermal surge. The PCM performs as a reservoir to absorb the transient heat surge during overload, which can enhance the safety for the wide band-gap devices.

As shown in Fig. 3.27, the PCM takes portion of the heat sink fins and increases the thermal resistance of the network. The steady-state temperature of HS2 under overload current is higher than that of HS1. To avoid the temperature further rising,

Fig. 3.26 HS1 is the heat sink without any PCM, HS2 is the same heat sink with 1/3 fin filled with PCM [14]

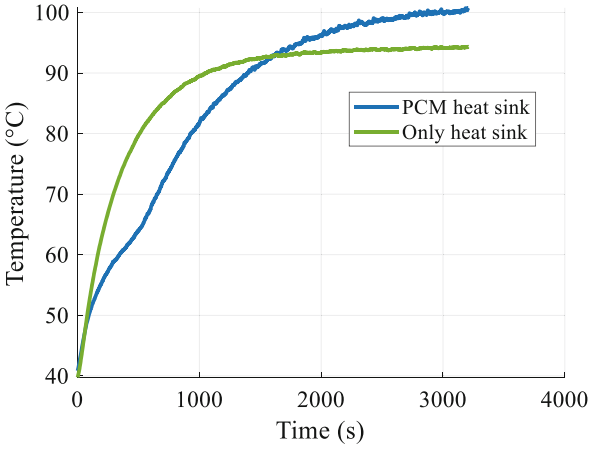

Fig. 3.27 Testing results for two heat sinks HS1 (only Heat Sink) and HS2 heat sink (filled with 1/3 PCM) under overload conditions [14]

the SSCB should interrupt the overload current promptly, and optimization of the PCM heat sink should be performed based on the overload conditions of the breaker.

4.5 Voltage Clamping Circuit Selection

Besides the power semiconductor devices and the affiliated cooling system, the voltage clamping circuit is also critical for SSCBs and HCBs. It has two functions: (a) to clamp the transient voltage across the power semiconductor devices and avoid over-voltage damage and (b) to absorb the residual energy left in the system parasitic inductances after semiconductor switches turn-off.

Different types of voltage clamping circuit can be used, including metal oxide varistors, transient voltage suppression diodes, snubber circuits, etc. In this section, those solutions are reviewed, and their advantages and limitations briefly summarized.

1.5mm x 3mm	7~25mm disc	60mm disc	60mm disc
Surface mount	Through hole	Press Pack	Screw Mount
< 120V V_{NDC}	< 1.2kV V_{NDC}	< 3.5kV V_{NDC}	< 3.5kV V_{NDC}
< 500A surge current	< 10kA surge current	< 70kA surge current	< 70kA surge current
< 2.5J absorb energy	< 480J absorb energy	< 10kJ absorb energy	< 10kJ absorb energy

Fig. 3.28 Overview of MOVs available on the market, in terms of size, DC nominal voltage range, maximum surge current, and maximum energy absorbing capability [15]

4.5.1 Metal Oxide Varistor (MOV)

Figure 3.28 shows an overview of the MOVs on the market, and it can be seen that MOVs have various package types (from small surface-mount to big screw-mount). The MOVs have advantages of wide voltage ranges (up to 3.5 kV DC operating voltage per device) and huge surge current or energy absorbing capabilities. Also, the MOV has bidirectional current/voltage capability and more cost-effective compared to other voltage clamping components, like TVS diodes.

During the SSCB current interruption phase within the MOV, a sharp voltage spike (V_{pk}) usually appears at the voltage waveform at the initial voltage clamping transient of the MOV. This peak of the voltage spike needs to be lower than the blocking voltage of the semiconductor device; otherwise, an overvoltage damage of the semiconductor device could happen. When the SSCB is in standby mode (semiconductor switch OFF and galvanic isolation switch closed), the MOV withstands the system DC bus voltage, generating some leakage current. The maximum system DC bus voltage the MOV can withstand is defined as its maximum operating voltage (V_{op}). The leakage current through the MOV needs to be low enough to avoid the overheat damage of the MOV due to too much losses generated. The leakage current also needs to meet the requirements from standards (e.g., UL 489I sets requirement for SSCB’s max leakage current in stand-by mode.)

One important index to evaluate the voltage clamping solution is the ratio between peak clamping voltage and maximum operating voltage (V_{pk}/V_{op}). Lower V_{pk}/V_{op} is preferred to achieve higher voltage utilization rate of the solid-state (SS) devices, and the SSCB can operate at a higher DC bus voltage for a certain voltage class of the semiconductor device (e.g., 1200 V). V_{pk}/V_{op} depends on the SSCB design and requirements, and on the MOV’s size. For example, a 20 mm disc MOV is tested with $V_{pk}/V_{op} = 1.61$ at 150A interruption current and a 10 mm disc MOV’s

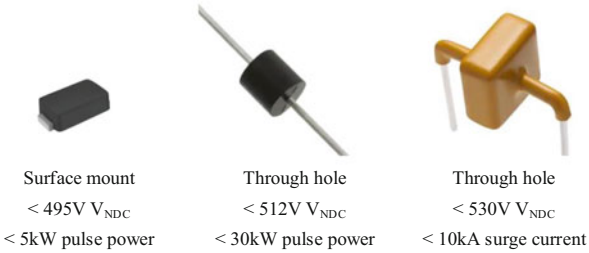

Fig. 3.29 Survey of TVS diodes in terms of package, maximum DC nominal voltage, maximum pulse power, or surge current capability [15]

$V_{pk}/V_{op} = 1.81$ at 120 A interruption current. In general V_{pk}/V_{op} for MOV is in the range 1.6 ~ 2.2.

To be noted that when selecting the MOV some voltage margin needs to be considered, because the semiconductor device could see higher voltage than the MOV's peak clamping voltage. When the current is commutating from the semiconductor device to MOV, the *di/dt* generates extra voltage drop across the loop inductance between the semiconductor device, which is also applied to the semiconductor devices.

4.5.2 Transient Voltage Suppression (TVS) Diode

Another commonly used voltage clamping solution is TVS diodes, which work like an avalanche diode but can achieve enhanced peak current and energy handling capability. Both unidirectional and bidirectional TVS diodes are available.

Figure 3.29 exhibits a few commercially available TVS diodes from one manufacturer. Compared to MOVs, TVS diodes have limited voltage range (<530 V for single device) and limited peak current capability (with only small surface-mount and through-hole package devices available). To achieve higher voltage rating or absorbing higher energy, the series connection or parallel connection of TVS diodes is needed. TVS diodes are also more expensive compared to MOV for similar absorbing energy and voltage requirements.

Figure 3.30 shows the TVS diode V-I trajectory during the voltage clamping process. One interesting phenomenon is noticed that after the TVS diode reaches a peak clamping voltage, its voltage drops to a level even lower than its nominal voltage [15]. For example, a 430 V nominal voltage TVS diode is tested and demonstrates ~540 V peak voltage, and then the voltage decreases to ~340 V (called static clamping voltage). The TVS diode's maximum DC operating voltage should be determined by its static clamping voltage (340 V), rather than its nominal voltage (430 V), and the V_{pk}/V_{op} ratio for the tested TVS diode is calculated as 540 V/340 V = ~1.59, which is slightly lower than MOVs. Some margin needs to be added when selecting the TVS diodes because of the parasitic loop inductances between the TVS diodes and the semiconductor devices.

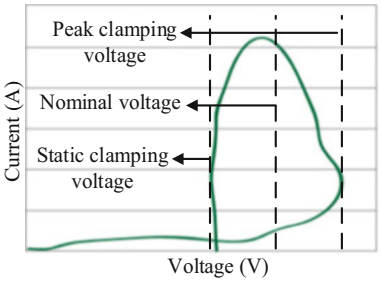

Fig. 3.30 TVS diode V-I trajectory during the voltage clamping process

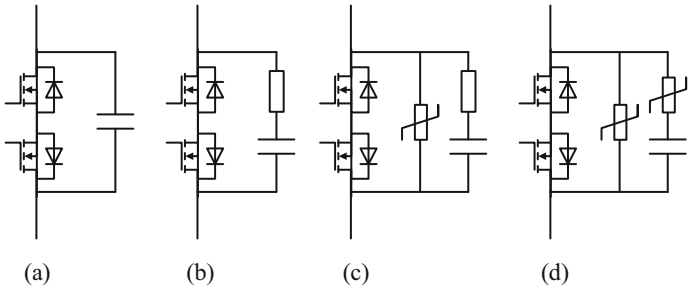

Fig. 3.31 Capacitor based clamping circuits: (**a**) only capacitor as snubber circuit; (**b**) RC based snubber circuit; (**c**) RC snubber in parallel with MOV; (**d**) MOV and capacitor in series based snubber circuit in parallel with another MOV [15]

4.5.3 Capacitor-Based Voltage Clamping Circuit

Capacitor-based snubber circuits are another option for voltage clamping in SSCBs. One beneficial feature of that solution is they control *dv*/*dt* at turn-off, reducing the turn-off stresses on the semiconductor device during fault current interruption.

Figure 3.31 shows some different types of snubber circuits. Capacitor-based snubbers in Fig. 3.31a are the simplest case, but they have the issue of current oscillations after turn off. To address this, more complex designs have been like the RC snubber (Fig. 3.31b), RCD snubber, etc., which can quickly suppress the oscillation by selecting the right damping resistors.

To reduce the size of the capacitor in the RC snubber, a MOV can be added in parallel as in Fig. 3.31c. The MOV has the function of absorbing the energy and clamping the voltage, while the RC snubber limits the turn-off *dv*/*dt*, increasing the current turn-off capability of the semiconductor device. A different solution, with the resistor replaced by a MOV as shown in Fig. 3.31d, was proposed in [16] to speed up the dampening of LC resonance. More details and comparison between the different snubber circuits can be found in [15, 16].

4.6 Design of the Gate Driver and the Protection Unit

The main requirement in designing the gate driver unit for SSCBs is that enough voltage must be provided to the gate of the power semiconductor device in order to turn-on or turn-off the current, ensuring the lowest on-state resistance and reliable current interruption. Different from the power electronics converters, fast-switching speed (e.g., high switching *dv*/*dt* and *di*/*dt*) is not crucial in SSCBs because of limited switching times, indeed sometimes a lower switching speed is preferred to reduce the overvoltage stress across the semiconductor switches.

The protection unit is intended to monitor the current and send out the tripping signal to the gate driver circuit when a fault occurs. In some cases, the characteristics of the power semiconductor devices (like the voltage drop) could be used for sensing the current, eliminating the need of additional current sensors and saving cost.

All the gate driver circuits, sense and trip electronics, etc. are powered by auxiliary power supplies, which usually need to be electrically isolated from the main power circuit.

In addition to the lower on-state resistance, because of their normally-on behavior SiC JFETs do not need auxiliary power supply when in conduction mode. However, they still need negative gate-source potential to turn off and stay off. Such behavior can be exploited to simplify the design of passive SSCBs not requiring isolated auxiliary power supply, sensors, and digital electronics, in which the power for turning off the JFET is drawn from the fault energy itself by means of a pick-up circuit. The design of the protection circuit for such SiC JFET-based SSCB is presented in this section.

Figure 3.32 shows the fundamental concept of a passive SSCB. The pick-up circuit shall be designed to draw enough power for the gate drivers in the different fault scenarios that can occur in DC circuits: overload, bolted (low impedance) short circuit (high *di*/*dt*), and high impedance short circuit (low *di*/*dt*).

The overload fault occurs when the load current increases above the nominal current value and stays there for extended period of time. This fault increases the losses and in terms the temperature of the elements that are carrying the fault current. To protect the system from this type of fault, a positive temperature coefficient (PTC) resistor is connected in series between two JFETs as shown in Fig. 3.32. The PTC resistor offers very low resistance during normal operation, up to the nominal current, but above nominal current the heat generated inside PTC increases its resistance. If the overload current lasts long enough, the PTC can become highly resistive (in the order of MΩ), causing a high voltage drop across the PTC. This voltage is usually more than enough to turn-off the power JFETs. Therefore, by using correct timing and gate driving circuit, the maximum voltage across PTC can be kept below the safe values, and the fault current can be interrupted.

In case of short circuit, the fault impedance affects the rate of the fault current increase (the *di*/*dt*). In low-impedance faults, the fault current can increase at rate as large as 100 A/μs or higher, whereas the rate can be of the order of 1 A/μs in high-

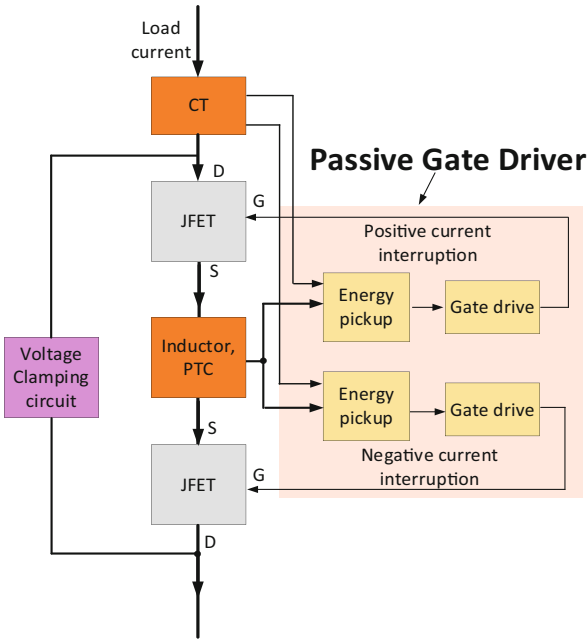

Fig. 3.32 Functional circuit block diagram of a SiC JFET-based SSCB with passive gate driver

impedance short circuits. Such different behaviors require different energy pick-up circuits.

To handle high *di/dt* faults, an inductor *L* is connected in series with the SiC JFETs to sense the fault. The voltage across the series inductor L can instantly achieve or exceed the required gate voltage to turn-off the fault current, and can directly be applied to the JFETs gate.

For low *di/dt* faults, as the voltage across the inductor L would be too low for turning-off the JFETs, a current transformer (CT) is added in the main current path. This current transformer produces no output in case of normal operation’s steady currents but during transient, such as high or low *di/dt* faults, it produces current in the secondary winding that is used to charge a capacitor and provide the voltage for the gate driver circuits.

Figure 3.33 shows the short circuit tripping curve of a SSCB prototype in which the CT is used to sense the low *di/dt* current from 0.15 to 0.8 A/μs, and the series-connected inductor *L* is designed to sense the high di/dt current from 0.8 A/μs and above. The short-circuit fault up to 9 A/μs *di/dt* is tested and validated.

The design of the pick-up circuit, the inductor, and the current transformer can be tuned to adjust the tripping curve in order to match the requirements, considering that the inductor and the CT are also part of the main circuit and can influence the overall system behavior, this can limit the flexibility.

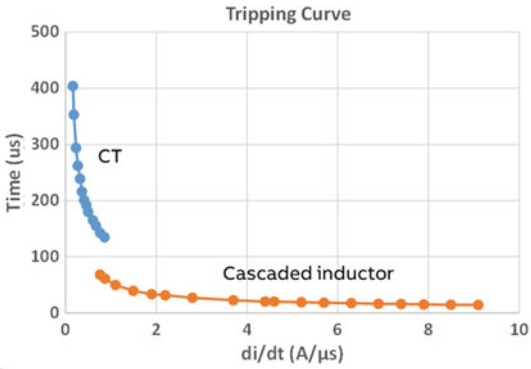

Fig. 3.33 Tripping curve (tripping time vs. *di/dt*) of the SiC JFET-based SSCB under short circuit faults

5 Application Cases for SSCBs

Tackling climate change is one of the key challenges of this century. To contain global warming within 1.5 °C above pre-industrial levels, society needs to cut net emissions to zero by 2050 latest.

This target can be achieved without dramatic social consequences only if the energy system is radically transformed. Fossil fuels that today power cities and industries shall be replaced with clean, decarbonized electricity from renewable sources, and energy wastes shall be minimized [17].

DC addresses all requirements of this energy transformation, but for its massive deployment some issues have to be solved, one of which is the need for fast and selective protection.

As DC grids typically have low inductance and resistance, and large capacitors at the DC bus terminals that contribute to fault currents, short-circuit faults can result in ultrafast transients with high currents that can cause severe damage to power electronic converters and sensitive loads. In addition, discharge of capacitors can result in voltage dips of the DC bus, with consequent temporary shutdown of the installation, which is not acceptable for most applications. Thus, advanced protection schemes that quickly identify faults and fast circuit breakers are needed, able to clear faults before the current reaches a dangerous level and the voltage drops below the shut-down value. Smart SSCBs perfectly fit this application [18]. This also confirms that the maximum admissible rate of rise of the current, i.e., the maximum *di/dt* of the fault current which a circuit breakers can interrupt, is the key performance parameter for SSCBs, more relevant than the maximal prospective current value typically used for conventional circuit breakers.

A large number of application cases for the DC grids of the future are explored in literature and by demonstration projects, and their maturity has been increasing and is still increasing significantly. The ease of integration of distributed generation from renewable sources, typically operating in DC, batteries and energy efficient loads (LED, VSDs, ...), together with other advantages makes DC fit very well with microgrids [19]. The efficiency of AC and DC power distribution in commercial

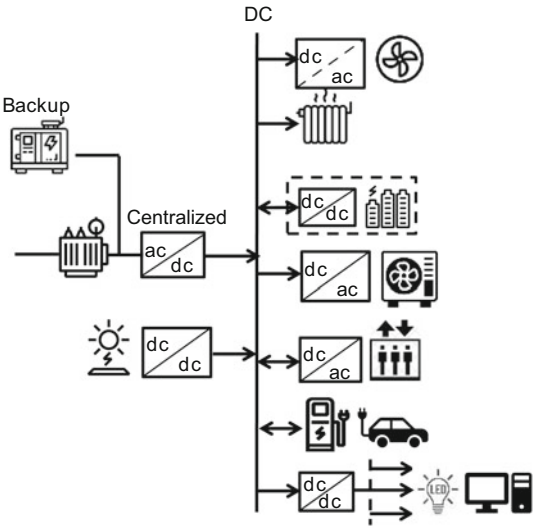

Fig. 3.34 DC microgrid for commercial and residential buildings

and residential buildings has been compared in several studies. DC is most likely to be more efficient in buildings with high local PV generation and storage capability, in which the energy being exchanged with the public AC grid is low [20], as the percentage of PV energy dissipated in conversion is lower because of the lower number of conversion stages [21] (Fig. 3.34).

The Current/OS foundation has been developing a set of rules for DC power distribution in multi-sources installations, including residential and commercial buildings, street-lighting, and EV-charging installations, with the intent of ensuring safety, reliability, and interoperability of equipment from different vendors. The rules have been validated in some pilot installations [25]. Current/OS rules require use of SSCBs to reduce short circuit current and energy, and risk of arc-flash and electric-shock in high-safety zones distributed in living spaces.

The German research project DC-Industrie has proven the feasibility of DC grids in industrial context that can potentially reduce the energy consumption by about 6–10% [22]. The saving mainly results from the ease of recovery of power from drives during braking that would be typically wasted in AC as regenerative drives are significantly more expensive. The DC-Industrie power distribution architecture consists of DC sectors, i.e., groups of DC components (loads, generators, or storage) forming a functional unit, connected to the DC bus through a solid-state circuit breaker (Fig. 3.35). Use of ultrafast solid-state circuit breaker is crucial to ensure reliable and selective protection, i.e., to avoid that a fault in a DC sector causes the shutdown of the plant.

DC power distribution has been gaining momentum in marine vessels, where the ABB’s Onboard DC Grid™ architecture has proven to enable fuel savings up to 27% [23, 24]. Here, as shown in Fig. 3.36, a bus tie breaker connects the two starboard and portside sections; this typically allows an optimal and redundant usage of the

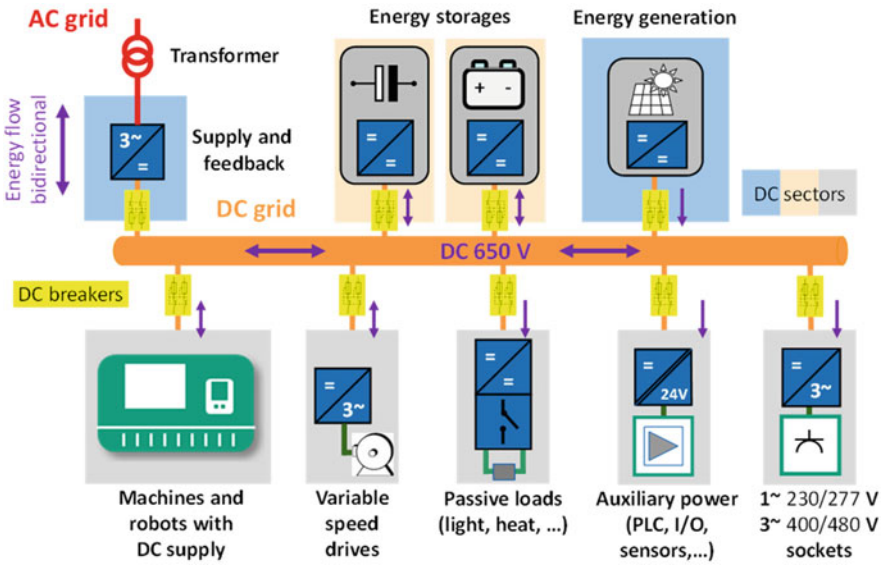

Fig. 3.35 Industrial DC microgrid according to DC-Industrie (© DC-INDUSTRIE & ZVEI) [26]

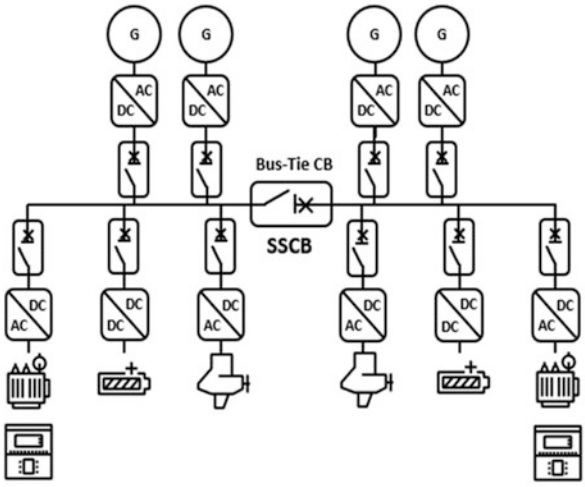

Fig. 3.36 Example of a DC distribution grid in a marine vessel with SSCB as bus-tie circuit breaker [27]

power generators. If a fault occurs, the sections must be protected by the circuit breaker to prevent a total outage and ensure service continuity by disconnection of the faulty section. In situations that are too challenging for traditional technology due to the high and fast rising (in milliseconds) short circuit currents in DC shipboard power systems, SSCB technology can excel. For example, SSCBs can quickly limit the fault current from generators and converter capacitors. SSCB can limit the short circuit currents to a few kA, avoiding damages to healthy sections

and unwanted trips especially of fuses, thus providing a supreme resilience to the system. In terms of system design, with a slower DCCB as the DC tie breaker, the generator capacity should be restricted to satisfy the fault tolerance of the converter and the DCCB. Fast DCCB, such as SSCB, is crucial to alleviate the design constraint of system capacity, and thus Onboard DC Grid™ is applicable to small and large vessels.

Improved LVDC protection by SSCB can be also a relevant enabler for cost-effective solutions for the integration of renewables in the existing AC grid. Energy storage systems are deployed for different use cases like frequency regulation or deferral of power line upgrades. In the case of large-scale battery energy storage systems (BESS) in the range of megawatt power (MW) and energy capacities of megawatthours (MWh), the (LV) battery banks are typically connected via a DC bus to an DC/AC bi-directional converter via a step-up transformer to the distribution or transmission grid. Depending on the use case, the energy storage needs to be sized in order to support from 15 min to 6 h of full converter power. But with larger energy storage size, i.e., with a larger number of battery banks, the short circuit current in case of faults can rise to couple of 100 kAs at very fast rise times. As traditional protection run there into the limits of technology performance, an upper limit for battery banks to a single converter is set. But for cost-effectiveness, the total installed converter power should not exceed the requirements of the point of common connection to the grid. The need which stems for this desired independent scaling of converter power and energy capacity, to create larger DC buses, can only be fulfilled if SSCBs are deployed for fault current protection.

Finally, for the integration of high-power electric vehicle infrastructure (EVCI) to the AC grid, the addition of energy storage systems is expected to become a must in many situations. Fleets of electric cars, light trucks, and buses which are used to supply cities and metropolitan areas will increase the stress on the distribution grids, especially at vehicle depots or in industrial zones. The DC coupling of such an energy storage system to the charger system will lead to challenges of short circuit handling as described before and of ensuring a high availability to keep operations running. The deployment of SSCB protection for this application seems to be as well very promising from the economical aspect.

Even though the adaption of DC offers a wide range of benefits for the integration of renewables, solid-state circuit breakers could be in principle also beneficial as retrofit in the AC distribution. One of the challenges of grid protection to future distribution grid protection with high penetration of DER (Distributed Energy Resource) is difficulty in protection coordination because of changing fault current levels and directions. The conventional AC distribution protection devices, such as fuses and reclosers, are no longer used and need to be upgraded to smart devices for intelligent protection algorithms to be deployed. This upgrade process will take huge efforts in money and time to be implemented. At the transitional stage of limited interconnection of DERs in distribution grid, an alternative solution could be to install SSCBs at the proper locations in distribution grids to allow fast interruption of fault contributions from these DERs. In this way, the original distribution protection scheme can still work, and a cost-effective solution, instead

of expensive upgrade of whole distribution protection, can temporarily solve the challenge to meet requirements of protection selectivity and coordination.

6 Concluding Remarks

Solid-state circuit breakers are not a drop-in replacement of the traditional electromechanical devices. Their ultrafast interruption is a key enabler for new DC power distribution models that can improve energy efficiency and ease integration of distributed energy resources. On the other hand, higher cost, larger footprint, due to the reuired cooling and air-gap isolation, and limited overload capacity make them less competitive for application in which electromechanical circuit breakers fit the job.

The different technical challenges that need to be addressed in the design of a SSCB have been briefly discussed in this chapter, starting from the selection of the power semiconductor device to the design of the cooling system and the voltage clamping circuit.

The power semiconductor device shall be selected in order to minimize conduction losses, whereas switching losses are obviously less relevant for this application. This means that devices optimized for power converters, in particular for mid-frequency applications, might not be optimal for SSCBs, and the other way round. Today, it seems there is not a device fitting the whole application spectrum. Silicon Reverse-blocking Integrated Gate-Commutated Thyristors (RB-IGCTs), offering low power losses at large currents (from several hundred Amps and larger), are the most effective solution for high power SSCBs, with rated currents in the range of kAs and rated voltage from 1 kV and up, but scaling down this technology for lower power SSCBs is difficult because of their non-linear behavior at low current. Silicon Carbide devices such as MOSFETs and JFETs seem a good fit for such smaller SSCBs due to the low on-state resistance. In particular, normally-on SiC JFETs offer the possibility to design passive SSCBs that nearly mimics the behavior of thermomagnetic CBs without the need of current sensors and digital control.

The design of the cooling system strongly impacts the SSCB footprint and the installation constraints. Whereas liquid cooling is typically required for high power converters and SSCBs based on IGBTs, having power losses of the order of several kW, with lower losses RB-IGCTs air-cooled SSCBs are possible, that are much simpler to install, by using dual-phase thermosyphons to displace the heat from the hot semiconductor device to a forced-air heat sink.

Thermal aspects during current interruption are also challenging, in particular in overload or short circuit. The cooling system in this case plays a minor role here, as turn-off is so short to be adiabatic. Differently from electromechanical circuit breakers, where the arc chamber combines the functions of switching off the current and dissipating the fault energy, in SSCBs the fault energy is dissipated through the clamping circuit. This makes Metal Oxide Varistors (MOVs) more suitable for SSCBs than snubbers typically used in power converters, as they have

much better dissipation capability. However, MOVs impose tough constraints on the power semiconductor device, as the SSCB’s maximum operational voltage shall not exceed 0.5–0.6 the blocking voltage of the semiconductor device, depending of the design; or, equivalently, the semiconductor device shall have a blocking voltage 1.6–2.2 times the system voltage. Such design constraints can be eased replacing MOVs with Transient Voltage Suppressing (TVS) diodes, but at the price of higher costs and much lower energy dissipation capability. Hybrid circuits including MOVs and other components offer an improved property mix, but are more complex.

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Chapter 4
iBreaker: WBG-Based Tri-Mode Intelligent Solid-State Circuit Breaker

Z. John Shen, Yuanfeng Zhou, Risha Na, and Ahmad Kamal

1 Introduction

Low-voltage DC power networks (up to 1000 V) such as DC data centers, PV farms, and EV charging infrastructures are gaining tractions in recent years because of their advantages in efficiency, cost, and power quality over the traditional AC power [1–5]. However, protecting these DC power networks from short circuit faults remains a major technical challenge [6–10]. Conventional electromechanical AC circuit breakers must be significantly redesigned or derated for DC applications due to the lack of current zero crossing and the difficulty of extinguishing arcs. With a typically response time of 20–50 ms, they are too slow to interrupt fast-rising DC fault currents. Solid-state circuit breakers (SSCBs) have been under intensive research in recent years to address these challenges, as discussed in other chapters of this book and survey papers such as [11, 12]. An SSCB typically uses power semiconductor devices like IGBTs or IGCTs as the main static switch, which simply switches ON and OFF in response to an overcurrent condition. It typically offers a response time less than several tens of μs to protect the network assets (cables, connectors, power converters, etc.) from excessive electrothermal stress. However, the main disadvantage of SSCBs is their high conduction loss and the need to effectively remove the heat generated during normal on-state operation. Unlike in more sophisticated HVDC or MVDC systems where active cooling (e.g., liquid or forced air) of the SSCBs may be acceptable, SSCBs for low-voltage DC

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power applications (<1000 V) must rely on passive cooling to meet the cost and maintenance-free requirements. It is extremely challenging to limit the on-state power loss of a silicon-based SSCB to a level of several watts that can be dissipated via passive cooling.

Wide bandgap (WBG) semiconductor devices such as SiC or GaN transistors offer a much lower on-resistance and conduction power loss than silicon IGBT or MOSFET for a voltage rating over 600 V, and are highly attractive for SSCB applications [13–16]. While WBG devices are still roughly 3–5 times more expensive than their silicon counterparts, they are expected to follow the classical semiconductor cost reduction learning curve in the future. In particular, GaN HEMT transistors, which are fabricated on low-cost silicon wafers in fully depreciated CMOS fabs, stand a real chance of achieving cost parity with silicon in the near future, as indicated by the fact that 100 V-rated commercial eGaN FETs are already priced comparably to silicon MOSFETs.

Another challenge for the SSCBs is to operate under complex circuit conditions, such as distinguishing between a true short circuit fault current and a load inrush current with both exhibiting similar overcurrent behaviors. The inrush current, often several times of the nominal current, is mostly the initial charging current for the large input capacitor of an electrical load during its startup or plugging-in phase [17]. The inrush current may cause nuisance tripping of circuit breakers or damage the electronic equipment. Conventional electromechanical circuit breakers address this problem by allowing a very high (typically 20–30× of the nominal current) fault current tripping point as well as a wide current-time profile for overcurrent protection, neither being feasible for effective protection of the new DC microgrids. Innovative solutions beyond the commonly used ON/OFF switch configuration need to be developed to integrate intelligent functions with minimal cost penalty.

In this chapter, we will describe a new class of WBG-based intelligent SSCBs, referred to as iBreakers [16], which were developed with the funding support of the US Department of Energy ARPA-E CIRCUITS Program [18]. The iBreaker concept explores the use of WBG switching devices and new converter-based topology and control techniques to integrate intelligent functions. An iBreaker can operate in an ON state for continuous conduction of normal load currents or an OFF state to interrupts fault currents. In addition, it can operate in a distinct PWM Current Limiting (PWM-CL) state with a moderate overcurrent for a short period of time to facilitate intelligent functions such as soft startup, fault authentication, fault location, and selective coordination. The iBreaker will switch from the PWM-CL to the OFF state if it deems the overcurrent condition to be a true short circuit fault rather than a startup scenario after a short time period. Switching-mode buck topologies along with a variable frequency PWM control method are adopted to replace the simple SSCB ON/OFF switch configuration to optimize both soft-start and other fault protection functions. Furthermore, the technique of identifying the fault location on the power cable using the iBreaker hardware/software architecture is discussed in this chapter. While different aspects and design examples were reported by the authors in the past [16, 19–21], this chapter aims at providing a comprehensive overview on the basic concept and general design methodology

of iBreaker. Key design elements will be discussed in detail, including choice of WBG switches, tri-mode operation and topology, combined digital and analog control, and universal hardware/software architecture. Two DC iBreaker design examples are described in this chapter to highlight the design methodology and functionality. The first iBreaker is rated at 380 V/20 A and based on GaN switches for data center applications while the second iBreaker is rated at 750 V/250 A and based on SiC JEFT switches for hybrid electric aircraft applications. Greater than 99.95% transmission efficiency, passive cooling, and μs-scale response time are demonstrated experimentally in both cases.

2 Design Methodology

The general design methodology of iBreaker is discussed in this section. Figure 4.1 shows four key design elements: use of WBG switch for mΩ-range on-resistance, tri-mode operation for integrating intelligent functions, combined digital and analog control for both speed and flexibility, and universal hardware/software architecture for easy commercialization.

2.1 Choice of WBG Devices

One major limitation of today's SSCBs is their high on-resistance in comparison to that of mechanical circuit breakers (typically in a sub-mΩ range). Even if the SSCB conduction loss is insignificant (e.g., <0.5%) comparing to the total transmitted power, self-heating of the SSCB due to the conduction loss can be a serious concern

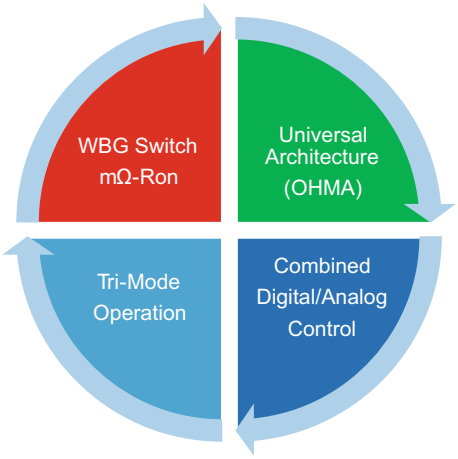


Fig. 4.1 iBreaker design methodology including four key elements: use of WBG switches, tri-mode operation, combined digital and analog control, and universal hardware/software architecture [16]

since maintenance-free passive cooling is highly preferred in low-voltage circuit breaker applications. Silicon IGBTs typically offers a forward voltage drop of 1.5–3.0 V (depending on the voltage and current ratings), and are the most commonly used power semiconductor switch type in SSCBs today. The forward voltage drop of IGBTs translates into an on-resistance of tens to hundreds of mΩ or a power loss of tens to hundreds of watts, too high for passive thermal management. Silicon superjunction MOSFETs up to 650 V typically offer an on-resistance similar to that of IGBTs. In the long run, WBG devices, such as SiC MOSFETs with a specific R_{DSON} of 2–3 mΩ-cm^2 at 1200 V or GaN HEMTs with a specific R_{DSON} of 1–2 mΩ-cm^2 at 650 V, become the only choice to reduce the SSCB on-resistance into the mΩ range for passive cooling operation. Even though these WBG devices are still 3–5 times more expensive than their silicon counterparts, they are expected to follow the classical semiconductor cost reduction learning curve. In particular, GaN HEMT-type devices, fabricated on silicon wafers with an MOCVD-grown epitaxial layer in fully depreciated 6 or 8 inch CMOS fabs, stand a real chance of achieving cost parity with silicon in the near future if the production volume reaches a critical mass. This is indicated by the fact that commercial 100 V eGaN FETs are already in a price range comparable to their silicon MOSFET competition.

2.2 Tri-Mode Operation

A conventional SSCB design for interrupting fault currents is typically comprised of a semiconductor static switch, sensing and control electronics, auxiliary power and communication circuits, and energy absorption components such as MOVs. It typically operates either in the ON (normal) or OFF (fault) state, and has a limited flexibility to deal with complex scenarios such as inrush currents during the startup of an electronic load. In this work, a switching-mode common-inductor bidirectional buck topology is used to replace the simple ON/OFF switch configuration and facilitate a third operating mode of PWM current limiting (PWM-CL) in addition to the basic ON and OFF operation to enhance the flexibility and intelligence of the SSCB. The tri-mode iBreaker will quickly limit an overcurrent to 2–3× of the nominal current within a few microseconds, and conduct a fault authentication process within a preset time window (typically a few milliseconds) while operating at this moderate overcurrent. This will significantly reduce the stress on the wiring and power semiconductor devices, and reduce the current rating and cost of semiconductor switches. The fault authentication algorithm will be discussed later in this chapter. If a short circuit fault condition is confirmed, the iBreaker will transition to the OFF state from the current PWM-CL state. However, if a startup inrush condition is determined, the iBreaker will continue to operate in the PWM-CL state and facilitate a soft start of the load at this limited overcurrent. In addition, the PWM-CL state can accommodate other intelligent functions. One example is to identify the fault location on the downstream cable connecting the load. This function can help expediting the system maintenance process after a

power shutdown due to a fault. It is worth noting that an SSCB topology operating a silicon MOSFET and a freewheeling diode in a pulse (or hiccup) mode was reported to limit the startup inrush current in [9, 10], but it somehow operated the MOSFET continuously in the saturation regime with a very high power dissipation to limit the fault current before shutting it down. A true switching-mode buck topology was simulated and modeled to limit the DC fault current by operating the semiconductor switch in a PWM ("pulse by pulse") mode in [22, 23] while a similar buck topology was experimentally demonstrated in a DC fault current limiter (FCL) [24], but none of these works integrated the type of soft-start and other intelligent functions as demonstrated in this work.

2.3 Combined Digital and Analog Control

Analog control provides extremely fast fault detection and reaction times (typically 1–5 μs) but lacks the flexibility and programmability offered by digital control techniques. On the other hand, the response time of digital control is limited to tens of μs by the clock or interrupt frequency of the DSP or microcontroller used. In the iBreaker designs, a hybrid control approach is adopted to combine digital and analog control to achieve both programmability and μs-scale response time.

2.4 Universal Hardware/Software Architectures

The application environment for circuit breakers is extremely diverse and complex in terms of current and voltage characteristics as well as load and fault conditions. It would be impractical to develop an *iBreaker* product for every application scenario. Instead, a universal hardware/software architecture should be considered to allow the use of one hardware but many control algorithms (OHMA) approach. The proposed OHMA approach will allow circuit breaker manufacturers to develop and support a small number of *iBreaker* products for a wide range of diverse applications, using different software programs optimized for each application scenario.

3 Circuit Topology

A bidirectional common-inductor buck topology is adopted in this work to facilitate the aforementioned tri-mode operation, as shown in Fig. 4.2. In the first GaN-based 380 V/20 A iBreaker design example, the DC bus voltage is set to 380 V and the nominal load current to 20 A. The iBreaker is comprised of a GaN power board (yellow box) and a control circuit board (green box). It is essentially a back-to-

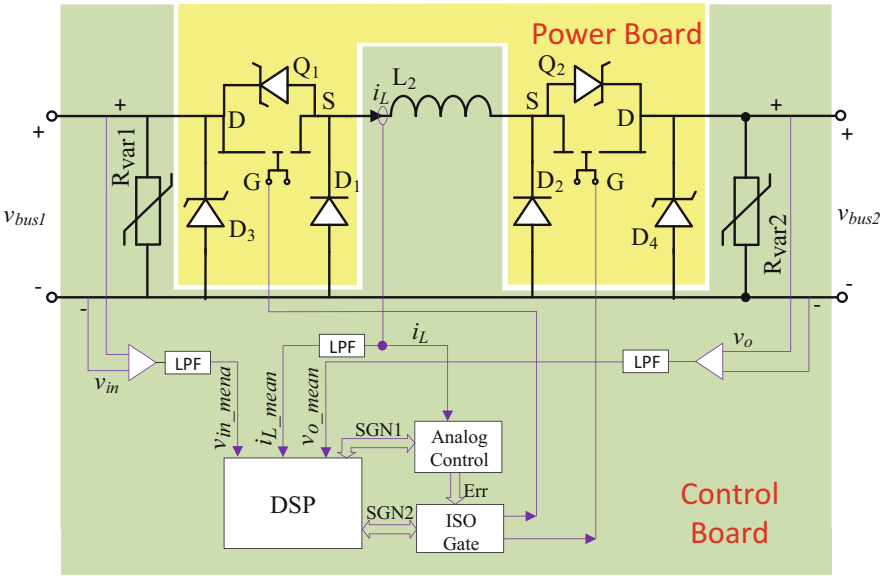


Fig. 4.2 Simplified schematic of a bidirectional iBreaker comprised of a control board (green box) and a power board (yellow box). The iBreaker is essentially a back-to-back buck converter with a shared inductor. The control board has current, voltage, temperature sensors, a DSP, low pass filters (LPFs), and an analog control circuit. Q_1 and Q_2 are the main WBG switches

back bidirectional buck converter with a common inductor, which allows or blocks current flow in either direction between left and right. When current flows from left to right, GaN FET Q_2 remains in the ON state and operates in the 3rd quadrant with a low on-resistance. GaN FET Q_1 also remains in the ON state and operates in the 1st quadrant under normal operation conditions. However, when an overcurrent condition is detected, Q_1, freewheeling diode D_1, and inductor L_2 together form a simple buck converter and operate in a PWM mode to limit the load current to a reasonably low level (e.g., 2× nominal). L_2 also helps limit the fault current rate of change *di/dt* when a short circuit fault occurs. The circuit operates in a similar way when the current flows from right to left since the topology is nearly symmetrical. The following discussion assumes that the current flows from left to right for the sake of simplicity. In one design implementation of the 380 V/20 A iBreaker, five 650 V/25 mΩ GaN FETs (GaN Systems GS66516T) are used in parallel for Q_1 or Q_2 to offer an equivalent on-resistance of 5 mΩ in this study. The iBreaker total on-resistance is 10 mΩ (that of Q_1 and Q_2). The power board also includes several RC snubbers, MOVs, and diodes to ensure safe operation of the iBreaker.

The control board includes several sensors for current/voltage/temperature, a DSP, low pass filters (LPFs), and an analog control circuit. A DSP or MCU (e.g., NUCLEO-L432KC from STMicroelectronics) is used to control the operation of the iBreaker, which has ADC, DAC, PWM, UART, and GPIO modules. Voltage and current sensors are used to constantly monitor the DC bus voltage v_d, node voltage

v_s, and inductor current i_L. Note that only the DC components of v_s, v_d, and i_L are fed to the ADC module of the DSP through the low pass filters. The DSP reads these input signals once in every sampling cycle (e.g., 72 μs), and runs different control programs based on these signals. In addition, an analog control circuit is designed to continuously detect and register overcurrent conditions due to either a short circuit fault or a startup inrush current. The instantaneous inductor/load current i_L before the LPF is constantly compared with a trip threshold I_p, which is the maximum current of the iBreaker set by the DSP (e.g., 40 A or 2× of the nominal rating of 20 A). If i_L is less than I_p, Q_1 will be solely controlled by the DSP. If i_L exceeds I_p, the overcurrent analog control circuit will turn off Q_1 immediately to limit the output current of the iBreaker, and at the same time send an overcurrent status signal to the DSP. The DSP will then initiate a PWM current-limiting (PWM-CL) program and find out the reason behind the overcurrent condition. If it is due to an inrush current, the iBreaker will charge the capacitive load to the DC bus voltage through a PWM operation of the buck converter. The pulse width of v_s is measured using the DSP's capture function when the iBreaker operates in the PWM-CL mode. After the successful startup, Q_1 will stay on. If the soft startup operation cannot increase the load voltage to a preset value close to the DC bus voltage within a specified time period, it is deemed that the overcurrent condition is due to a short circuit fault. Therefore, Q_1 will turn off and remain off.

Combining the flexible DSP with the analog-like overcurrent detection circuit leads to an optimal solution to maintain a μs-scale ultrafast response time while gaining digital programmability for the iBreaker. The iBreaker also draws power from the positive and negative power buses to supply the control electronics through an isolated DC power module. An NTC sensor is used to monitor the switch temperature for over-temperature protection of the iBreaker. A Bluetooth module is also included in the *iBreaker* for wireless communication of status reporting and remote switching functions.

4 Control Strategy

The iBreaker offers three distinct operation states: ON, OFF, and PWM Current Limiting (PWM-CL). The conventional ON state (Q_1 and Q_2 staying ON) allows continuous conduction of normal load currents while the conventional OFF state (Q_1 and Q_2 staying OFF) prohibits any current flow. The third PWM-CL state allows Q_1 or Q_2 depending on the current flow direction to switch in a PWM mode with a limited peak current to distinguish an inrush current from a short circuit fault and/or perform other intelligent functions. In the CL state, the WBG switches at a variable PWM frequency to optimally facilitate a soft startup process. Note that the iBreaker only operates in the CL mode for a short time period (typically several ms), and then exits to either the ON or OFF state depending on the circumstances. Such a tri-mode control strategy is described as an event-driven finite state machine (FSM) in Fig. 4.3.

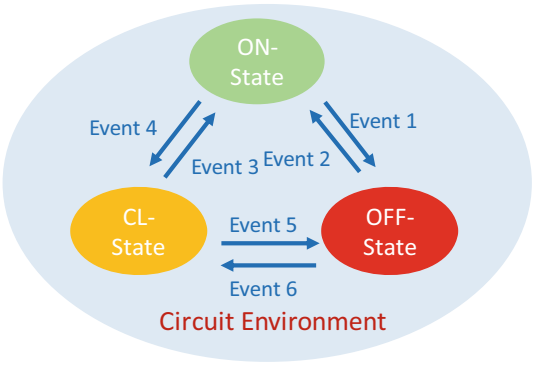


Fig. 4.3 iBreaker tri-mode control strategy

Transitions among the three operation states are driven by events as shown in Fig. 4.3. Event 1 denotes the transition from ON to OFF state. It covers at least one of the following conditions: overload current (but still below the instant overcurrent shutdown threshold I_p) for an extended time period (e.g., 30 seconds); manual or remote shutdown command; or over-temperature. Event 2 covers the transition from OFF to ON state based on manual or remote turn-on command. Event 4 occurs when the load current exceeds the preset overcurrent threshold I_p, due to either a true short circuit fault or a normal inrush current during load startup. The iBreaker will shift from ON to CL state. In the CL state, the DSP will run a soft startup program, and operate the GaN FET with a variable frequency PWM algorithm to be discussed next. The root cause of the overcurrent condition will be determined by a fault authentication program to be discussed next. If it is deemed to be an inrush current, the iBreaker will return to the ON state after successfully charging the input capacitor of the load to the DC bus voltage, as indicated by Event 3. If the overcurrent is due to a short circuit fault, the iBreaker will shift to the OFF state, as indicated by Event 5. In the CL state, the average current through Q_1 is always less than I_p since the PWM duty cycle is less than 100%. The DC source and the power line, if sufficiently designed, will not be subject to thermal overstress since the iBreaker only operates in the CL state for a very short time period (less than a few ms). Event 6 denotes situations such as reclosing of the iBreaker immediately after a short circuit shutdown or a scheduled soft start of a load. The default operating state of the iBreaker is OFF, guaranteed by a large gate-source shorting resistor in the hardware design. The iBreaker will be powered up once being connected to the DC power source, a process taking no more than tens of μs to complete. After initialization, the DSP may choose to turn on Q_1 or keep it OFF depending on the user command. If the iBreaker enters the ON state, its load current i_L will be monitored by both the DPS and the overcurrent analog control circuit. If an overcurrent condition (i.e., i_L exceeding I_p) is detected, the iBreaker will shift to the CL state; otherwise it will remain in the ON state. The iBreaker operating in the CL state will continue its operation if the soft start process is still on-going, or exit to the ON state if the soft start process is finished. However, if the DSP determines

that the startup process cannot be completed as a result of a true short circuit fault, it will transition to the OFF state. Other state shifts from ON to OFF or from OFF to CL can be facilitated by a remote or manual user command.

The DSP continuously monitors the currents and voltages of the iBreaker circuit as shown in Fig. 4.2 with a sampling cycle time of 72 μs. When operating in the CL state, the DSP examines the difference between the DC bus voltage and the output voltage. If the error is less than a preset threshold (e.g., 5 V), the DSP sends the iBreaker to the ON state. Otherwise, the DSP will check next if the soft start process exceeds a preset time limit (e.g., 2 ms), and send the iBreaker to the OFF state if that is the case. Otherwise, the DSP will check next if the load current exceeds the preset overcurrent threshold, and continue the PWM operation at the same PWM frequency if that is the case. Otherwise, the buck converter will operate at a reduced PWM frequency as will be discussed next. The PWM period can be chosen as 4, 6, 8, 12, 18, 24, 36, and 72 μs. For a true soft start, the iBreaker will eventually operate at a PWM frequency of 13.9 kHz (1/72 μs) before exiting to the ON state.

4.1 Variable Frequency PWM Algorithm

Most digital equipment loads have an input filter capacitor in a range of tens of μF [17]. The input capacitance can be as large as thousands of μF in aircraft [25]. When such a load with an input capacitor is powered up by a DC bus, there will be a very large initial inrush current to charge the capacitor. The proposed iBreaker will shift to the PWM-CL state to limit the inrush current and gradually charge the capacitor up to the DC bus voltage. A variable frequency PWM control algorithm is developed to optimize the soft startup process. If the PWM frequency is too low at a certain duty cycle, the energy transferred from the DC source will be completely dissipated on the load resistor without actively charging the parallel capacitor within one PWM cycle. This requirement sets the lower limit for the PWM frequency. On the other hand, if the PWM frequency is too high or the PWM cycle time too small, the DC source cannot transfer sufficient amount of energy to the load within one PWM cycle under the constraint of a finite OFF time for the WBG transistors. This requirement sets the upper limit for the PWM frequency. Note that the upper and lower frequency limits vary with the increasing load voltage (i.e., the buck converter duty cycle).

To successfully charge the input capacitor of an electronic load during the soft start process, the energy transferred from the DC source to the load must be more than the energy dissipated by the load within one PWM cycle. This requirement determines the lower limit for the PWM frequency as

$$f_{\text{pwm}} > \frac{2v_{\text{o}}^2\left(V_{\text{bus}} - v_{\text{o}}\right)}{V_{\text{bus}} L_2 I_{\text{p}}^2 R} \tag{4.1}$$

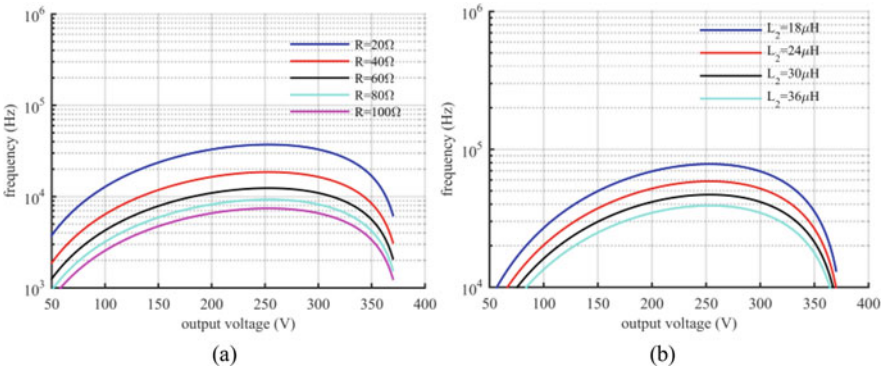


Fig. 4.4 Relationship between the load voltage and minimum PWM frequency for (**a**) a set of different load resistor with a fixed L_2 of 36 μH, and (**b**) a set of different load inductor L_2 with a fixed load resistor of 19 Ω

where V_{bus} is the input bus voltage, v_{o} the output voltage, I_{p} the overcurrent threshold, and L_2 the internal inductor, and R the load resistance.

Figure 4.4 shows the relationship between the minimum PWM frequency and the output (load) voltage for different load resistor R and inductance L_2. For a load resistor R of 100 Ω and 20 Ω with a fixed L_2 of 36 μH, the PWM frequency should be higher than 7.5 kHz and 40 kHz, respectively. A higher PWM frequency is required for a successful soft start if we want to allow a smaller load resistor. Similarly, a higher PWM frequency is required for a lower value of L_2.

On the other hand, a reasonably long PWM cycle time is required for the DC source to transfer sufficient amount of energy to the load side within one PWM cycle considering a finite OFF time for the GaN FETs. A reasonable PWM off time T_{off} sets an upper limit for the PWM frequency

$$T_{\text{off}} = \frac{L_2 I_{\text{p}}^2 R_{\text{rated}}}{2V_{\text{bus}}^2} \tag{4.2}$$

For a rated load resistor of 19 Ω, I_{p} of 40 A, L_2 of 36 μH, and V_{bus} of 380 V, the maximum T_{off} is roughly 4 μs. To guarantee enough margin for a successful soft start, it is better to choose a T_{off} as small as practically possible. WBG devices offer a high switching speed, and allow T_{off} in the range of 1 μs or less. In this work, a fixed T_{off} of 1 μs is selected. Note that the actual PWM off time can be longer than T_{off} because the overcurrent detection and register circuit constantly adjusts the PWM signal from the DSP.

To choose an optimal PWM frequency for the buck converter, Eqs. (4.1) and (4.2) are plotted in the f_{pwm}-v_{o} plane in Fig. 4.5. The red curve is the minimum PWM frequency required to charge up the input capacitor according to Eq. (4.1). The green curve is the maximum PWM frequency according to Eq. (4.2). A PWM frequency between the lower and upper limits needs to be selected for the buck

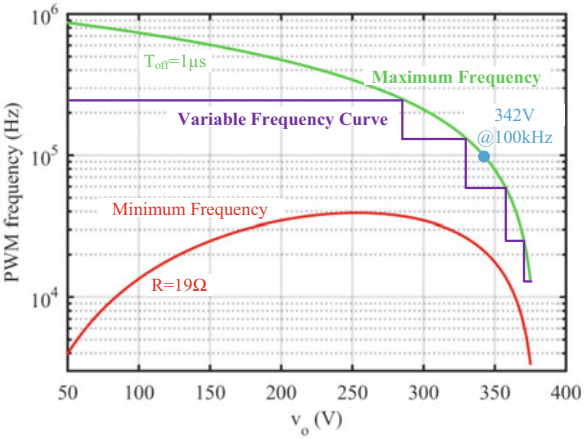


Fig. 4.5 Variable PWM frequency algorithm between the upper and lower limits set by Eqs. (4.1) and (4.2) for a fixed PWM off time of 1 μs

converter. If a fixed PWM frequency of 100 kHz is used, the output voltage would be charged to around 342 V (the blue dot in Fig. 4.5), leaving a large difference of 38 V below Vbus. If the WBG switch turns on at this moment, there would be a large inrush current because of the large voltage difference. It is far more optimal to use a variable PWM frequency algorithm which gradually reduces the PWM frequency as the output voltage v_o increases to approach the DC bus voltage, as indicated by the multistep purple line in Fig. 4.5. When the voltage difference is less than 5 V, the PWM operation can stop and the WBG transistor shifts to the ON state. In practice, the last PWM frequency is usually selected first, which is also the sampling frequency for voltage and current sensing (13.9 kHz or 1/72 μs in this design case as shown in Fig. 4.5). Other PWM frequencies are selected to be multiples of the last PWM frequency to ensure a smooth and easy frequency change. For example, the initial PWM frequency is 18× of the last PWM frequency or 250 kHz in this design case.

4.2 Fault Authentication Methods

After an overcurrent is detected and the iBreaker shifts into the PWM-CL state, the DSP needs to use a fault authentication method to judge whether it is a true short circuit fault or just an inrush current for normal equipment startup. We propose two different fault authentication methods. The first method monitors the output voltage of the iBreaker (i.e., the load voltage v_L) within a preset time window. The time window should be long enough to allow the completion of a soft startup process but short enough to ensure a quick response to a true fault current. Figure 4.6 shows a RC load model used for startup analysis. If the output voltage approaches the bus voltage V_{bus} (within a margin of a few volts) within the predetermined time window, it is deemed to be a normal startup process, and the iBreaker next shifts to the ON

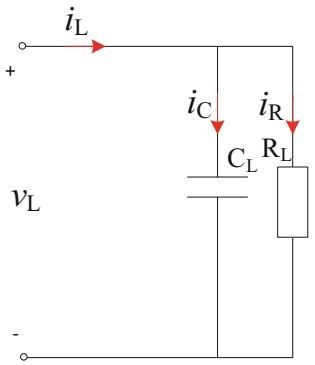


Fig. 4.6 RC load model for startup analysis

state. If the output voltage of the iBreaker does not reach the bus voltage within the predetermined time window, it is deemed to be a short circuit fault, and the *iBreaker* shifts to the OFF state. This is a simple fault authentication method that is easy to implement, but requires prior knowledge on the load resistance and capacitance. Nevertheless, a typical time window of 1–5 ms can cover a wide range of loads with various R and C values.

The second fault authentication method directly measures the rate of change of the load voltage dv_L/dt as shown in Fig. 4.2. If $dv_L/dt > 0$, it is deemed to be an inrush current scenario. Otherwise, it is a short circuit fault. The output or load voltage can be sampled periodically (e.g., every 72 μs) and dv_L/dt can be calculated. The dv_L/dt increment between two consecutive voltage samples is given by

$$\Delta v_L = \frac{I_L}{C_L} e^{-t/(R_L C_L)} \times \Delta t \tag{4.3}$$

where Δt is the sampling time of 72 μs and I_L at 40 A.

Figure 4.7a shows the calculated load voltage change between two consecutive sampling periods as a function of the actual load voltage for different load capacitances and a fixed resistance of 19.5 Ω for startup scenarios. It is evident that the voltage increment between two consecutive sampling periods increases with decreasing load capacitance. For example, for a load capacitance C of 10,000 μF and load resistance R of 19.5 Ω, Δv_L is between 0.1 and 0.3 V. Figure 4.7b shows the calculated load voltage change between two consecutive sampling periods as a function of the actual load voltage for different load resistances and a fixed capacitance of 5 mF for startup scenarios. Δv_L decreases quickly with increasing load voltage for smaller load resistances. Assuming the resolution of ADC in the iBreaker is 12 bits, so the theoretical voltage sampling resolution for a voltage range of 0–500 V is 120 mV. Because of the noise and nonlinearity of the ADC, the actual voltage sampling resolution is usually 2~3 times of the theoretical value, roughly 0.3 V. It is also possible to monitor the load voltage change over more than

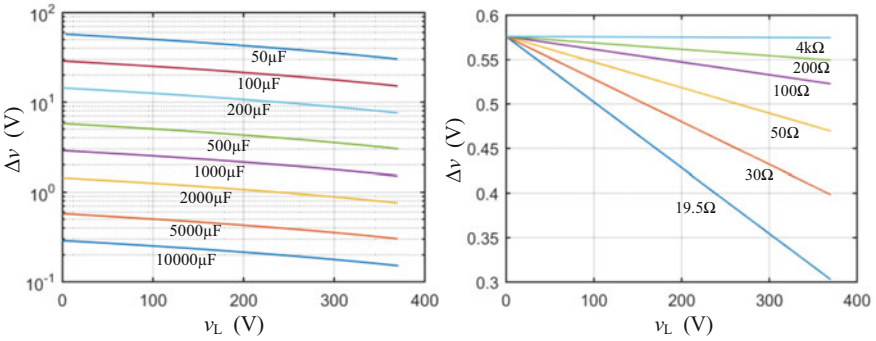


Fig. 4.7 Load voltage increment as a function of the actual load voltage for (**a**) different load capacitances with a fixed resistance of 19.5 Ω and (**b**) different load resistances with a fixed capacitance of 5 mF

two sampling cycles. Comparing to the first method, the second fault authentication method does not require prior knowledge on the load capacitance and resistance.

4.3 Fault Locating Algorithms

It is highly desirable to identify the fault location on the power line in the event of a fault shutdown so that it can be cleared by the maintenance personnel as quickly as possible. A method based on travelling-wave was reported to identify short circuit location in transmission lines in [26]. Other fault location techniques based on power line impedance measurement by injecting small signals were also reported [27, 28]. However, these methods require additional hardware and inevitably increase system cost and complexity. The PWM-CL state of the iBreaker provides an opportunity to locate a fault without any additional hardware and greatly simplifies the troubleshoot process after the fault shutdown [19]. After a fault is authenticated in a PWM-CL mode, a fault locating algorithm can be performed and a special PWM gate control pulses will be sent to the buck converter for a short period (a few ms). Since the power line inductance L_{line} between the iBreaker and the short location can be considered as part of the output inductance of the buck converter, it can therefore be extracted from the converter voltage and current information as

$$L_{\text{line}} = \left[\left(V_{\text{in\_mean}} - V_{\text{o\_mean}}\right) \times t_1 / \left(2I_{\text{p}} - 2I_{\text{L\_mean}}\right)\right] - L_2 \tag{4.4}$$

where $V_{\text{in\_mean}}$ is the averaged input bus voltage, $V_{\text{o\_mean}}$ the averaged output voltage, t_1 the on time of the PWM pulse, I_{p} the overcurrent threshold, $I_{\text{L\_mean}}$ the

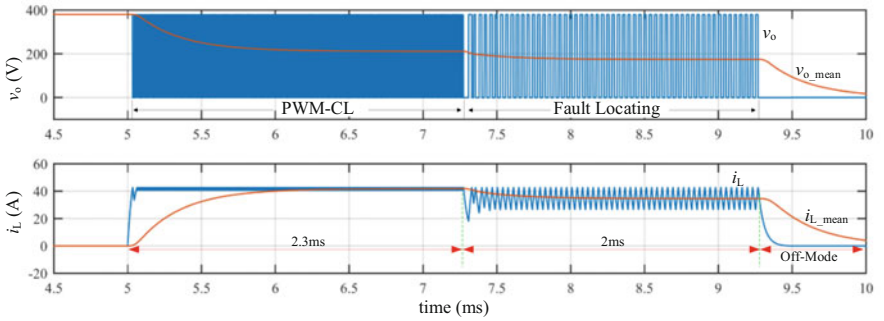


Fig. 4.8 Simulated current and voltage waveforms of the iBreaker responding to a short circuit fault at $t = 5$ ms. It initially operates in a PWM-CL state with an output current limited to 40 A for 2.3 ms. After the fault condition is authenticated at $t = 7.3$ ms, it switches on a fault locating algorithm for about 2 ms. The PWM period for these two current limiting modes is 4 μ and 36 μs, respectively

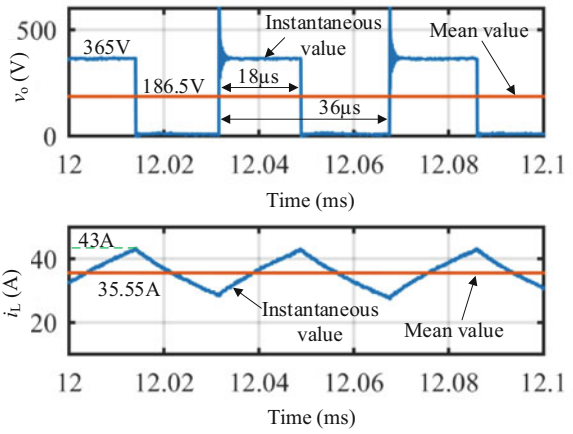


Fig. 4.9 Measured output voltage and current (instantaneous and average) waveforms under short circuit fault with an actual line inductance of 163.8 μH

averaged output or inductor current, and L_2 the internal inductor in Fig. 4.2. The averaged voltages and current values are measured after the low pass filters (LPFs).

The distance between the iBreaker and the fault location can then be calculated based on the per-unit-length inductance value of the power line. The fault locating algorithm is verified by simulation and experiments. Figure 4.8 shows the simulated current and voltage waveforms of the iBreaker responding to a short circuit fault at $t = 5$ ms. It initially operates in a PWM-CL state with a PWM period of 4 μs and an output current limited to 40 A. After the fault condition is authenticated at $t = 7.3$ ms, it switches to a fault locating algorithm with a PWM period of 36 μs for about 2 ms. During this short time period, it extracts the power line inductance and the distance between the fault and the iBreaker. Figure 4.9 shows the measured instantaneous and averaged output voltages and currents for an actual power line

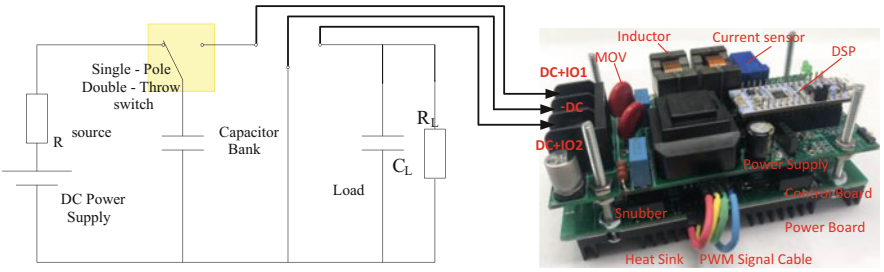


Fig. 4.10 380 V/20 A GaN-based iBreaker prototype in a capacitor discharge testing circuit

inductance of 163.8 μH. The extracted power line inductance using the proposed approach is 161.3 μH, within an error of 1.5%.

5 Design Examples

Two iBreaker design examples are discussed in this section to highlight design methodology and performance.

5.1 380 V/20 A iBreaker for Data Center Applications

The first iBreaker is rated at 380 V/20 A and based on GaN switches for data center applications. Figure 4.10 shows the iBreaker prototype and the capacitor discharge circuit used to characterize its protection functions. The capacitor bank of 2 × 5600 μF is first charged by a DC power supply to 380 V, and then discharged to a RC load through the iBreaker. In the experiment, two types of RC loads are used. Type 1 is a 40 μF capacitor in series with a 2.5 Ω resistor to emulate a normal inrush startup condition. Type 2 is a 2.5 resistor to emulate a short circuit fault condition.

In the 380 VDC/20 A iBreaker prototype, each of Q_1 and Q_2 shown in Fig. 4.2 is made of five paralleled commercial 650 V/60 A/25 mΩ GaN FETs (GaN Systems GS66516T) to offer a total iBreaker on-state resistance of 10 mΩ, which exhibits a total power loss of 4 W and a transmission efficiency of 99.95%. The heatsink pad is on the topside of GS66516T FETs, allowing excellent heat transfer to the heat sink through a thermal interface material (TIM), as shown in Fig. 4.11. The heat generated by the GaN FETs will flow from the junction to case, then PCB board, thermal interface material (TIM), heatsink, and finally to ambient. The thermal resistance $R_{\theta TIM}$ of the thermal interface material is estimated as 1.3 °C/W. The total junction to case thermal resistance $R_{\theta JC}$ of all ten GaN FETs is 0.027 °C/W. The heatsink to ambient thermal resistance $R_{\theta HSA}$ is 4 °C/W. The total on-state power

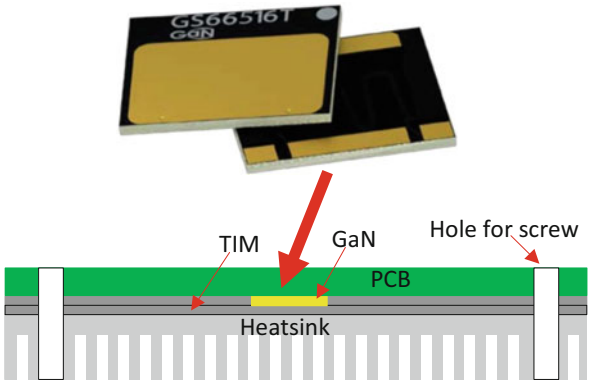


Fig. 4.11 GaN FET (GS66516T) on the 380 V/20 A iBreaker PCB with a heatsink mounted with a TIM pad

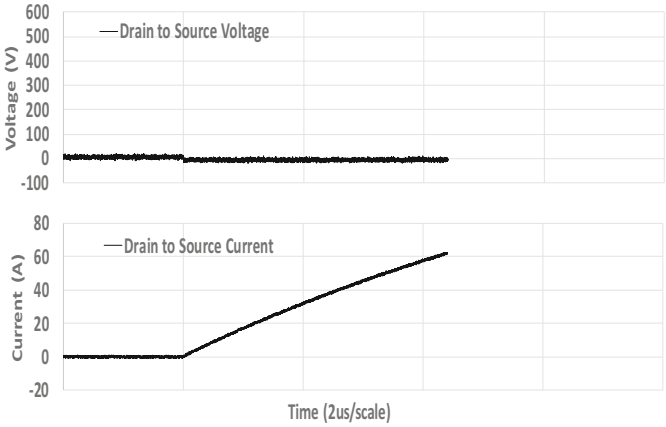
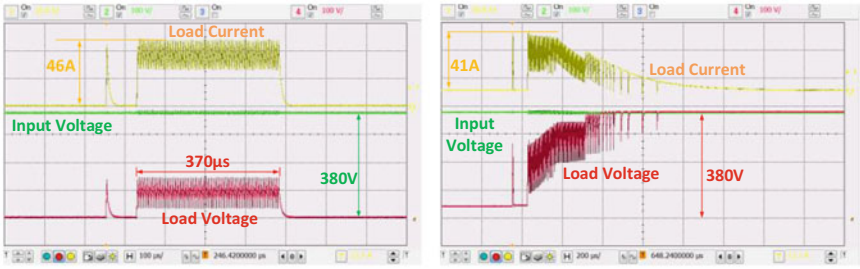


Fig. 4.12 RBSOA characterization of a single 650 V/60 A GaN FET (GS66516T) using a clamped inductive switching circuit. The device safely turns off a current of 68 A with a flyback voltage up to 580 V

loss of the iBreaker is 4 W at the rated current of 20 A and a total on-resistance of 10 mΩ. The junction temperature rise is estimated to be 21.2 °C at room temperature, offering a large margin for safe and reliable operation of the 380 V/20 A iBreaker.

One concern with using GaN FETs in SSCB applications is whether or not they have sufficient Reverse Bias Safe Operating Area (RBSOA) to survive a stressful inductive turnoff with simultaneously occurring high current and high voltage on the device. These GaN FETs are comprehensively characterized to address this concern. Figure 4.12 shows the measured drain voltage and current waveforms of a single GS66516T under a clamped inductive switching RBSOA characterization testing. The single GaN FET can safely turn off a current up to 68 A under a flyback voltage of 580 V, indicating a large safety margin for the intended 380 VDC applications since each of the five parallel GaN FETs only needs to handle 1/5 of the total current (4 A nominal).



(a) Short circuit shutdown (b) Soft-start

Fig. 4.13 Input voltage (green), load voltage (red), and load current (yellow) waveforms of the 380 V/20 A iBreaker responding to (**a**) short circuit fault with a 2.5 Ω resistive load, and (**b**) in-rush current with a 40 µF capacitive load to emulate a soft startup process

Figure 4.13a, b show the input voltage (green), load voltage (red), and load current (yellow) waveforms of the bidirectional 380 V/20 A iBreaker responding to (a) a short circuit fault and (b) an in-rush current, respectively. A load resistor of 2.5 Ω is used to emulate a short circuit fault in Fig. 4.13a. It is observed that the iBreaker initially senses an overcurrent of 46 A, and quickly turns it off within a few µs by the analog control circuit. The iBreaker, however, enters into the PWM-CL state after approximately 100 µs and maintains an average current of about 40 A (2× of the nominal), now controlled by the combined digital and analog circuits. The iBreaker stays in the PWM-CL state for a preset window of 370 µs until the fault authentication algorithm confirms that this is a true fault condition, and shut off at the end. For Fig. 4.13b, a load capacitor of 40 µF is used to emulate a load startup process that induces a large in-rush current. It is observed that the iBreaker operates in the PWM-CL state with a gradually decreasing load current as the load voltage increases, in contrast to the short circuit case of Fig. 4.12a. The load capacitor is fully charged to the input voltage of 380 V with a peak charging current of 41 A after 500 µs. The iBreaker then shifts to the on state at the end.

5.2 750 V/250 A iBreaker for Hybrid Electric Aircraft Applications

The second iBreaker is rated at 750 V/250 A and based on SiC JEFT switches for hybrid electric aircraft applications. To reduce carbon emission and fuel consumption [3], the aviation industry is exploring hybrid electric aircraft (HEA) through propulsion electrification. Depending on the HEA configuration, at least part of the propulsion power is provided by one or more electric motors which are powered by a battery pack. One HEA example is a six-seat commuter aircraft from Ampaire. The parallel-hybrid HEA has a 160 kW electric motor driving a front propeller and a 300 HP internal combustion engine driving a rear propeller [29].

Ampaire estimated 50–70% reduction in fuel consumption and 25–50% reduction in maintenance cost due to electrification of the powertrain [30].

A short circuit fault in an HEA electric system can result in excessive fault current in the power distribution system, and more dangerously in the Li-ion battery itself. Short circuit protection is therefore critically required in all HEA [31, 32]. Currently most HEA adopt the common practice of ground electric vehicles and use a battery contactor module (BCM) to connect the Li-ion battery to the powertrain [33]. The BCM, as shown in Fig. 4.14a, uses two main mechanical contactors for switching the DC current in either direction and a smaller auxiliary contactor to pre-charge the DC link capacitor during startup. Since the mechanical contactors are incapable of interrupting large DC fault currents, a fuse must be connected in series to interrupt excessive fault currents. The contactor/fuse solution typically offers a response time of tens of milliseconds, allowing the fault current to rise to more than ten times of the nominal current and causing excessive stress on the electrical system (battery, cables, or switches). The single-use fuse must be replaced after each short circuit incident, and the mechanical contactors also suffer from limited operation lifetime, both requiring costly maintenance work.

Figure 4.14b illustrates our SiC-based iBreaker battery switching module that offers at least 1000 times faster fault response time, 10 times lower fault current stress, much less maintenance requirement, and significantly improved operation lifetime in comparison to the mechanical contactor solution. The iBreaker comprises of back-to-back connected SiC JFETs with two free-wheeling/TVS diodes and allows or blocks the flow of charging or discharging current from the Li-ion battery pack. It is a simplified asymmetric version of the symmetric bidirectional buck converter topology in Fig. 4.2 with the dedicated common inductor being eliminated. This is because the 750 V/250 A iBreaker will be placed at a fixed location near the Li-ion battery pack and operate in a more predictable manner than the universal iBreaker configuration in Fig. 4.2. For example, the only in-rush current scenario is to pre-charge the DC link capacitor of the propulsion inverter at a known time instance. There is no in-rush charging current in the opposite direction. In the normal discharge or charge mode, both the charge and discharge transistors remain in the on-state. In case the discharge current exceeds a preset threshold (an overcurrent condition), the discharge transistor, the free-wheeling Diode 2, and the power cable form a buck converter and operate in a PWM mode to limit the overcurrent to a predefined value (e.g., 1.5–2× nominal rating). The parasitic inductance of the cable of a few μH is used to regulate the discharge current, saving both space and weight. The Li-ion battery in this HEA application can only be charged by a well-regulated battery charger on the ground (in-flight regenerative charging not allowed), which provides sufficient overcurrent protection. In the unlikely event of overcurrent in a charge mode when the EV charger fails to limit its output current or voltage, both the charge and discharge transistors will turn off completely to provide redundant protection for the battery. There is no need for using a fuse in the power loop. A Hall-effect current sensor along with an analog control circuit is used to sense the charge/discharge current and to detect overcurrent conditions. A microcontroller is used to control the operation of the

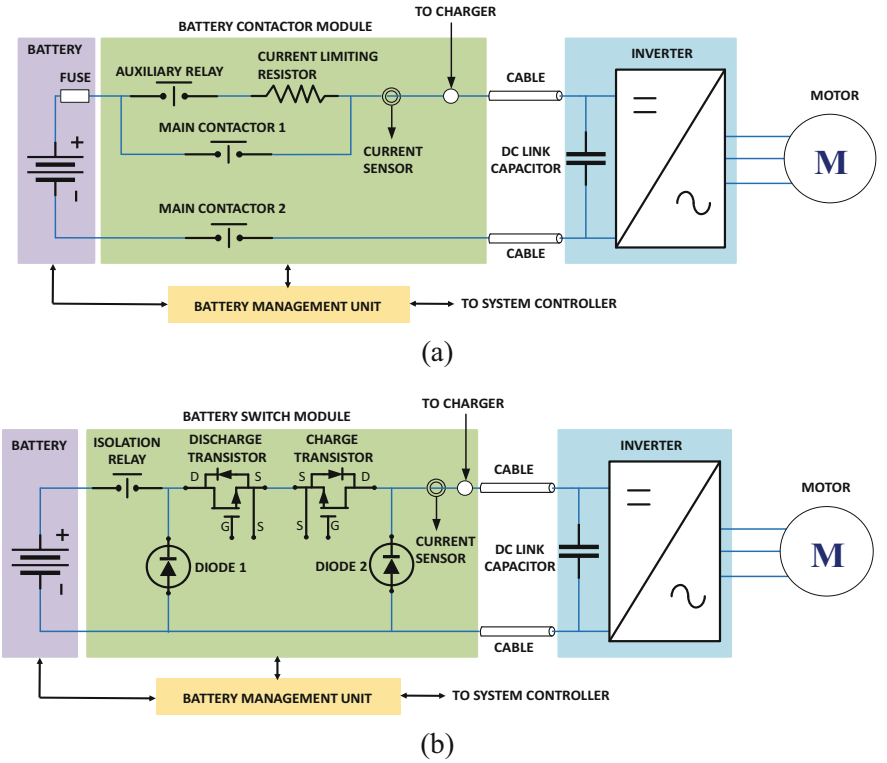


Fig. 4.14 Comparison of (**a**) prior-art contactor/fuse and (**b**) proposed iBreaker battery switching module (BSM) solutions

Table 4.1 HEA BSM design specifications

Specification	Value
Rated voltage	750 V
Nominal current	150 A
Peak current	250 A (~5 min)
Rated power	112.5 kW
Peak power	187.5 kW
Total R_{ON}	<1 mΩ
DC-link capacitor	320 μF

iBreaker and to communicate with the flight system controller of the aircraft and the battery management system (BMS) via CAN bus. To provide galvanic isolation, an isolation relay is included, which only switches under zero-current conditions. The iBreaker is primarily powered by the 24 V secondary power distribution system of the aircraft, but it also has an internal DC/DC converter to draw power directly from the HV Li-ion battery pack as a redundant power supply. The design specifications of the iBreaker are provided in Table 4.1.

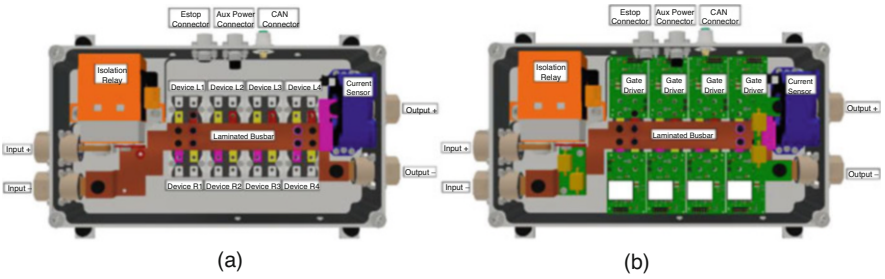


Fig. 4.15 3D model of the HEA iBreaker showing the SiC JFET and diode power modules (**a**) with a laminated busbar interconnection, and (**b**) with the gate driver boards (one for each SiC JFET module)

The iBreaker uses 1200 V/1.8 mΩ SiC JFETs in SOT-227 power module (United SiC's UJ4SC120002SNS). To reduce the conduction resistance of the iBreaker, four SiC power modules are paralleled to form each of the charge and discharge transistors. Figure 4.15 illustrates the 3D rendering of the iBreaker showing the SiC JFET and diode power modules interconnected with a laminated busbar and the gate driver boards (one for each SiC JFET module), respectively. The custom laminated busbar is used to connect all the eight SiC power modules which reduces the total conduction resistance of the iBreaker to merely 0.9 mΩ, comparable to the 0.4 mΩ of the existing mechanical contactor solution. Thus, for a peak current of 250 A the peak power loss of the iBreaker is just 56.25 W compared to 25 W for the existing mechanical contactor solution. The eight power modules are driven by individual gate drivers due to ease of design and debugging of this approach. The eight gate driver boards are screwed on top of each power module to make a robust connection. The gate drivers receive power and input signals from a main controller board, which is placed over the gate drivers. Finally, an 800 V-to-24 V DC/DC converter to provide auxiliary power from the HV battery for the iBreaker is mounted on the controller board with plug in headers.

Figure 4.16 shows the iBreaker (BSM) in the setup of short circuit response testing. A power resistor of 1 Ω is used to emulate a short circuit condition. The short circuit protection function is tested at a voltage level of 750 V, which is the same as the propulsion system of the hybrid aircraft. The waveforms for the iBreaker in response to the short circuit fault are shown in Fig. 4.17. The parasitic inductance of the power cable between the iBreaker and the DC-link capacitor is emulated with a 6.5 μH inductor. The load current shoots up rapidly due to a short condition but is cut off at 350 A by the iBreaker. This 350 A threshold limit is also adjustable through CAN communication. After the initial interruption of the current the BSM enters the PWM-CL state and sends a series of PWM pulses with a fixed frequency of 2 kHz (not shown in Fig. 4.16). As these pulses are to verify a short circuit condition, the current threshold is lowered to 150 A, so as to not inflict needless stress on the entire system. After 25 pulses of 150 A, the iBreaker measures the output voltage, which is not higher than 100 V, indicating that the overcurrent was not due to pre-charging of

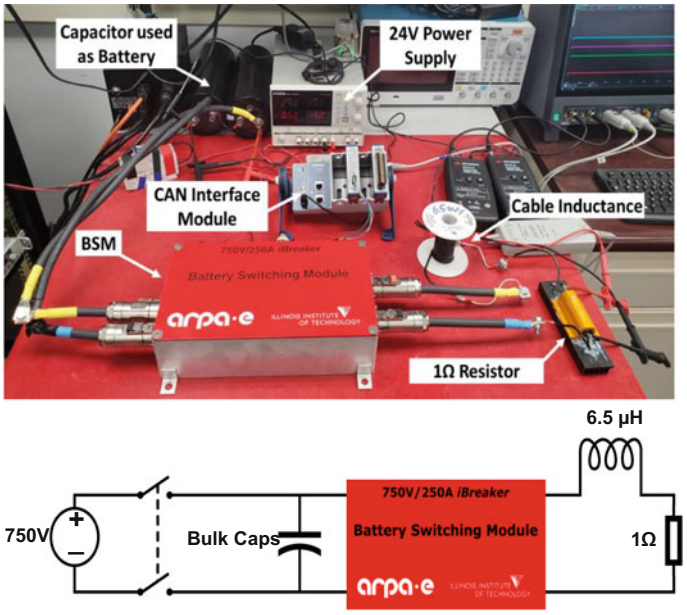


Fig. 4.16 Test setup for iBreaker (BSM) short circuit response

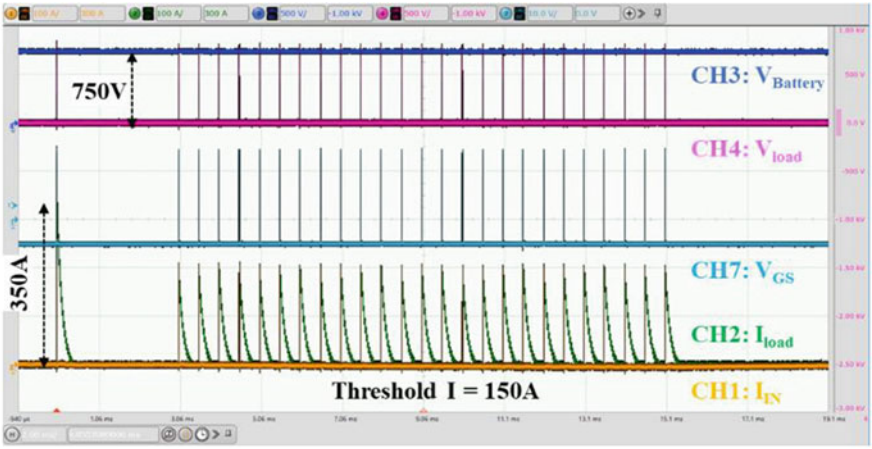


Fig. 4.17 Current and voltage waveforms of iBreaker responding to a short circuit fault

the DC-link capacitor but due to an actual short circuit. Therefore, the BSM turns off and remains off after validation of a short circuit condition. The 100 V and 25 pulse numbers were selected because the value of the DC-link capacitor in the aircraft is known and fixed. These numbers can be modified easily in the control code for different DC-link capacitor values.

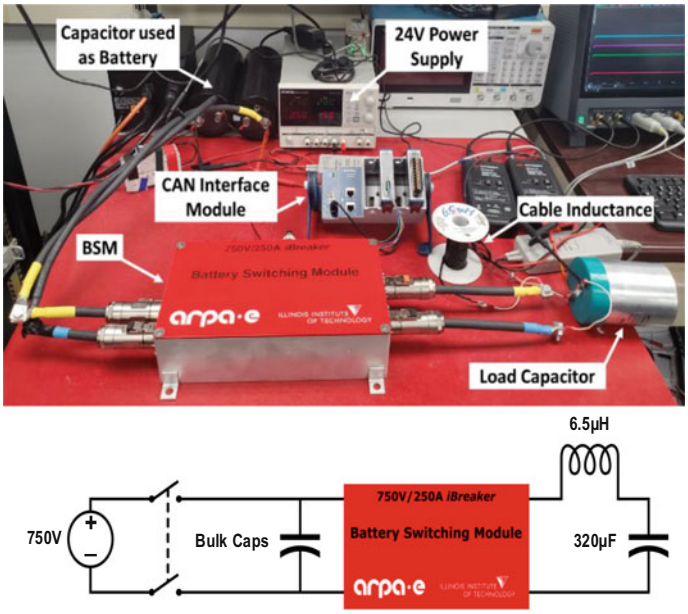


Fig. 4.18 Test setup for iBreaker (BSM) soft-start to pre-charge the DC-link capacitor

The same capacitive discharge circuit is also used to verify the soft-start process of the iBreaker to pre-charge a DC-link capacitor, where the shorting resistor is replaced with a 320 μF capacitor, similarly rated to actual capacitor used on the hybrid aircraft. The circuit diagram is shown in Fig. 4.18. The current and voltage waveforms of the iBreaker during the soft-start process are shown in Fig. 4.19. Similar to the short circuit response, the inrush current of the capacitor load shoots up rapidly but is cut off at 350 A by the iBreaker. After the initial interruption of the inrush current, the iBreaker enters the PWM-CL state and outputs a series of PWM pulses with a peak current of 150 A. After 25 pulses, the iBreaker measures the output voltage, which is significantly higher than 100 V, indicating that the initial overcurrent was due to the inrush current from pre-charging the DC-link capacitor instead of short circuit. Hence, the iBreaker continues outputting the 150 A current pulses to slowly increase the DC-link capacitor voltage. After 120 ms, when the voltage of the DC-link capacitor increases to 730 V (within 20 V of the 750 V bus voltage), the iBreaker enters the ON state and remains on.

Solid-state power controller (SSPC) or solid-state circuit breaker (SSCB) offers an alternative solution of replacing mechanical contactors with power semiconductor devices that offer faster response, lower fault current stress, and less maintenance requirements [34]. However, SSPCs suffer from higher on-state conduction loss and the need for active cooling (e.g., forced air or liquid cooling) [35]. Most of the SSPCs are based on silicon IGBTs or MOSFETs [36–38], but SSPCs based on wide bandgap (WBG) semiconductor devices are recently investigated due to their lower

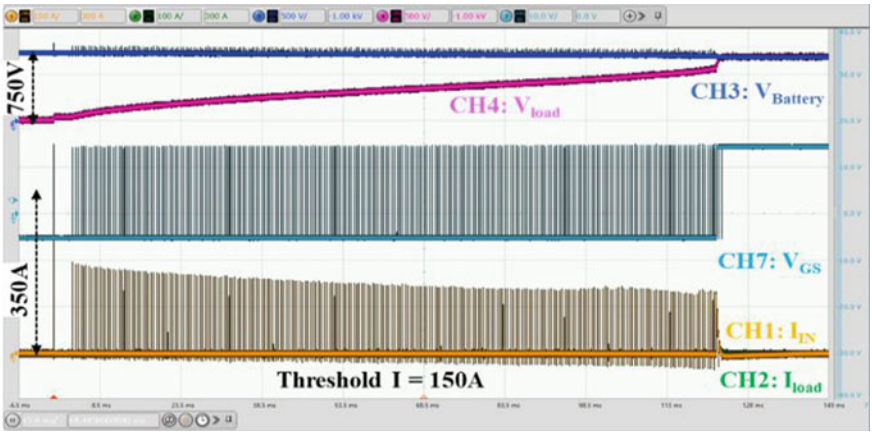


Fig. 4.19 Current and voltage waveforms of iBreaker during a soft-start process to pre-charge the DC capacitor

on-state resistance [39–43]. A major challenge of adopting the MEA-level SSPCs into the HEA powertrain application is to increase their voltage/current/power ratings. This is not a trivial task even with the adoption of low-loss WBG devices since the power level of HEA is considerably higher than MEA. Another SSPC design challenge is to distinguish true fault currents and normal inrush currents during startup since both can reach the same current level. Some SSPCs use a foldback current limiting approach to limit the inrush current by operating the power semiconductor switch in its saturation region [44–49]. However, this would generate excessive amount of heat and potentially device degradation or catastrophic failure. This is especially true for SiC power MOSFETs with their gate oxide integrity still being a subject of intensive research. The iBreaker design concept has proven to be a viable option to address these challenges [50].

6 Concluding Remarks

In this chapter, a new WBG-based intelligent SSCB concept, referred to as iBreaker, is introduced. The iBreaker concept explores the use of WBG switching devices and new converter-based topology and control techniques to integrate intelligent functions. The use of WBG devices allows mΩ-range on-resistance and maintenance-free passive cooling in low-voltage DC power networks. An iBreaker can operate in an ON state for continuous conduction of normal load currents or an OFF state to interrupts fault currents. In addition, it can operate in a distinct PWM Current Limiting (PWM-CL) state with a moderate overcurrent for a short period of time to facilitate intelligent functions such as soft startup, fault authentication,

fault location, and selective coordination. The iBreaker will switch from the PWM-CL to the OFF state if it deems the overcurrent condition to be a true short circuit fault rather than a startup scenario after a short time period. Switching-mode buck topologies along with a variable frequency PWM control method are adopted to replace the simple SSCB ON/OFF switch configuration to optimize both soft-start and other fault protection functions. Greater than 99.95% transmission efficiency, passive cooling, and μs-scale response time are demonstrated experimentally in several design cases.

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Chapter 5
T-Type Modular DC Circuit Breaker (T-Breaker)

Jin Wang, Yue Zhang, Xiao Li, Faisal Alsaif, and Yizhou Cong

1 Introduction

Solid-state circuit breakers (SSCBs) are excellent candidates for protections in dc networks. Compared with the slow breaking time of mechanical circuit breakers (MCBs), SSCBs are able to break fault currents in tens of nanoseconds to microseconds thanks to their high switching speed. The total response time of SSCBs is often limited by the sensing and control circuits rather than semiconductor devices themselves. Traditional SSCBs are built with series and parallel connected silicon devices. They are typically more compact and have longer lifetimes than MCBs due to the elimination of moving parts and arcing.

In recent years, there have been significant efforts on circuit topologies of SSCBs for low-voltage (LV) and medium-voltage (MV) applications [1]. One example is a family of Z-source-based dc circuit breakers (DCCBs) [2–4], where different types of impedance network are coupled with switching devices to allow automatic commutation to break fault currents. The other group of examples is modular circuit configurations. In [5], a hybrid circuit breaker is presented with diode-bridge-based submodules in both the solid-state branch and the low loss path. The proposed CB utilizes the counteracting voltage accumulated on the submodule capacitors to assist the fault current communication from the low loss path to the solid-state branch. In the solid-state branch, the submodule capacitors could also help gate synchronization issues thanks to their voltage clamping capability. Similar concepts are also proposed in [6–10]. Many recently proposed SSCBs have also incorporated current limiting functions, such as the Z-source breaker proposed in [3] and a tri-mode intelligent SSCB presented in [11].

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Though there have been exciting developments of SSCBs, in general, there are still few main challenges faced by SSCBs, especially MV SSCBs. These challenges include the need for bidirectional blocking switches, the stringent requirement on synchronization between switch blocks during fault transients, high cost, low power density, etc.

To match the efficiency of MCBs (>99.97%), a large amount of semiconductor devices is needed to be connected in parallel to achieve low on resistance, which results in high cost and low power density. Also, because of the high efficiency requirement and the constant-on operation, compared to power converters at the same voltage and power ratings, such as motor drives, SSCBs often require more semiconductors. For example, a 200 A 1200 V rated Silicon Carbide (SiC) power module can be used in a 100 A motor drive and still enables a reasonably good peak efficiency (around 99.0%). But if the same 200 A rated SiC power module is used to build SSCBs, to achieve an efficiency higher than 99.97%, the power module must be derated to operate with a nominal current less than 50 A. This means that the utilization of semiconductor switches in SSCBs is not as cost effective as in typical power converters, which leads to higher cost and lower power density. One approach to better utilize the large amount of semiconductor switches in SSCBs and increase the value proposition of SSCBs is to add ancillary functions such as fault current limiting, power flow control, power quality improvements, transient stability improvement, etc.

In this chapter, a scalable modular T-Type solid-state dc circuit breaker (T-Breaker) is introduced [12]. The T-Breaker not only can serve as a highly reliable dc circuit breaker, but also can function as an energy router to realize a wide range of ancillary functions to improve power flow regulation and enhance stability and reliability of dc networks. The derivation of the T-Breaker circuit topology, the operation principles, ancillary functions, and current development status are presented in detail.

2 Derivation and Variations of T-Breaker

2.1 Derivation and Reasoning of the Basic T-Breaker Topology

As illustrated in Fig. 5.1, the T-Breaker topology is derived from traditional SSCBs with series-connected bi-directional switches through three major steps:

Step 1: Rearranging semiconductor switches. The semiconductor switches that are used in conventional SSCBs need to have bidirectional blocking capabilities. However, typical power semiconductor switches, such as Insulated-Gate Bipolar Transistors (IGBTs), Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs), and Integrated Gate-Commutated Thyristors (IGCTs), are unidirectional blocking devices. Therefore, for conventional SSCBs, pairs of head-to-head connected switch pairs are used to form ac switches. In Step 1,

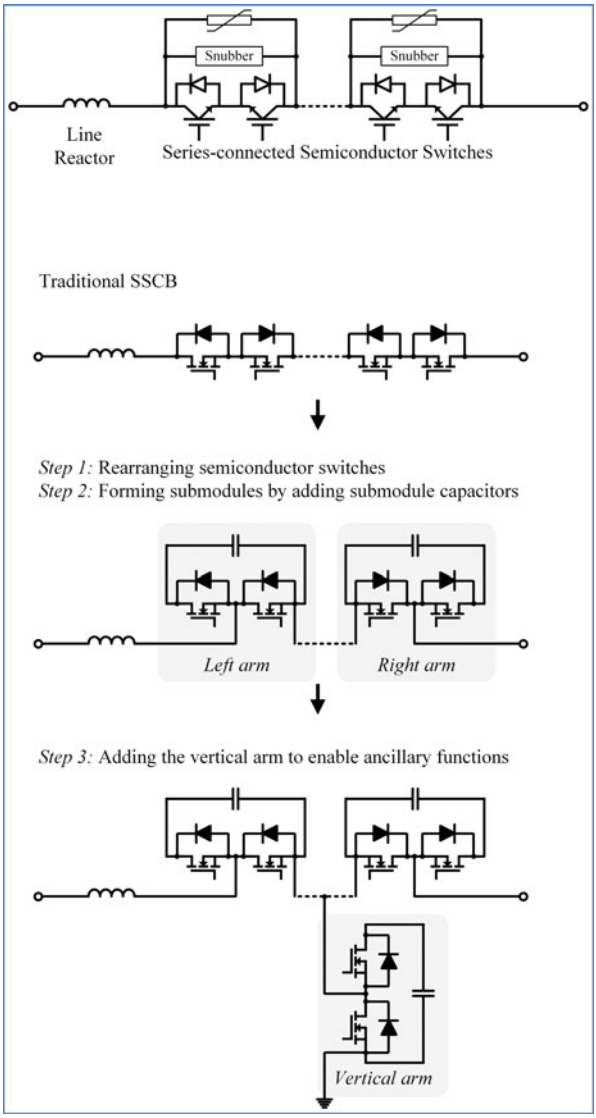


Fig. 5.1 Derivation and reasoning of the basic T-Breaker topology [13]

as shown in Fig. 5.1, the ac switches are decomposed and organized into two separated groups of head-to-toe connected switches. This approach does not increase the on-state loss and enables the utilization of widely available half-bridge power modules, which are commonly used in power converters and motor drives. Thus, high modularity and interoperability can be achieved.

***Step 2: Forming submodules*.** Submodules can be formed by adding energy storage components such as capacitor banks, batteries, super capacitors, etc., in parallel with half-bridge power modules. Metal Oxide Varistors (MOVs) could also be

put in parallel with energy storage elements to extend the fault energy absorption capability. By forming submodules with dedicated energy storage elements, the breaker can:

- Become self-sustainable by harvesting energy from submodule capacitors for gate drives, sensors, control circuits, and other auxiliary circuits [14]
- Be more reliable against misalignments of gate signals for series-connected switches thanks to the submodule capacitor's voltage clamping capability
- Absorb fault energy during current breaking
- Buffer potential high oscillations introduced by high stray inductance of MOVs
- Could inject voltage to the line to realize fault current limiting and ancillary functions

It is worth mentioning that traditional SSCBs often require snubber circuits which can include capacitors. However, the snubber capacitors often have small size and are not meant as energy storage devices. In contrast, the T-Breaker is fundamentally different because large capacitor banks, super capacitors, and batteries are integrated into the submodules not only to absorb energy during breaking events but also provide ancillary functions during normal operation.

Step 3: Adding the vertical arm. The final step is to add the vertical arm to the middle point of the horizontal arms. Like shunt-type Flexible AC Transmission Devices [15, 16], the added vertical arm enables current injection and absorption to and from the power line. Thus, with energy storage devices in both horizontal and vertical arms, the T-Breaker can realize both series and parallel compensations, which makes the T-Breaker an ultimate power conditioning solution for dc networks.

2.2 T-Breaker Topology Variations

The T-Breaker as shown in Fig. 5.1 has a modular structure. In general, all types of circuit building blocks such as half bridges, full bridges, three-level neutral point clamped half bridges and full bridges, T-converters, etc., can be implemented as submodules of a T-Breaker. The generalized system diagram of T-Breaker is shown in Fig. 5.2.

Depending on types of submodules, topologies of T-Breakers can be categorized into two groups: unipolar and bipolar. For example, as shown in Fig. 5.3, for three-level T-Breaker topologies, both the unipolar half bridge and the bipolar full bridge could be utilized. Though the number of submodules in the horizontal arms is different, the total number of switching devices is the same for these two topologies. The major difference between unipolar and bipolar topologies is that bipolar topologies would allow more flexibility on how the voltage from each submodule can be inserted into the dc network.

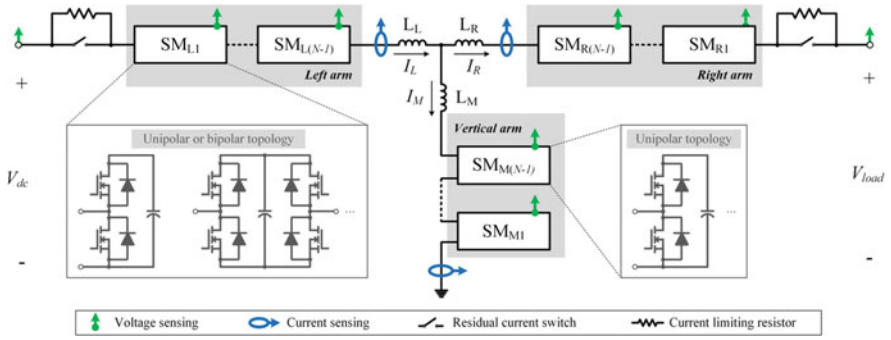


Fig. 5.2 Generalized T-Breaker system diagram

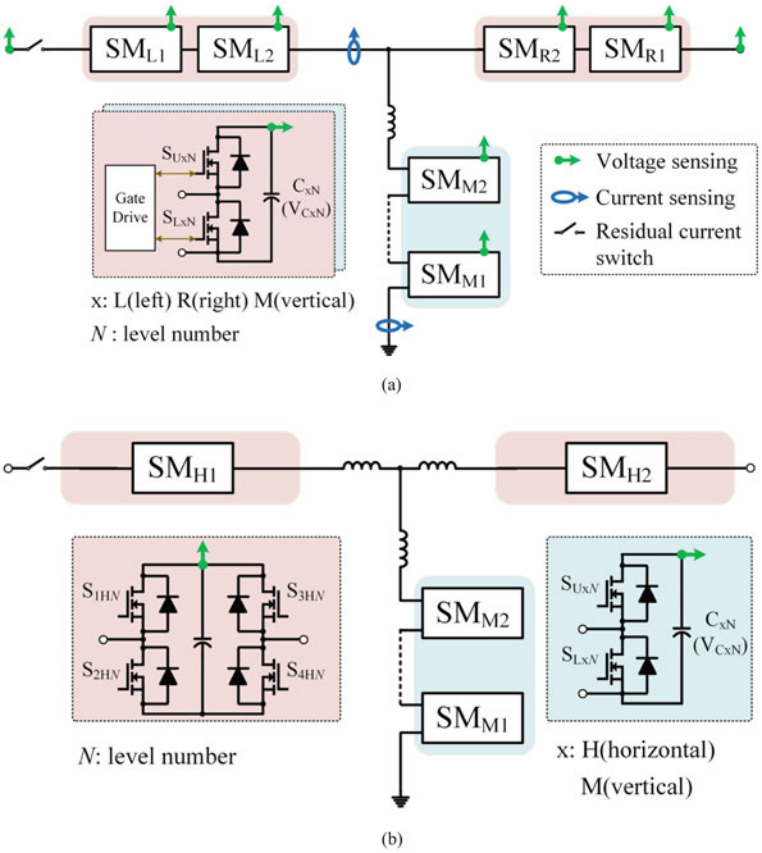


Fig. 5.3 Variations of three-level T-Breaker topologies. (**a**) Three-level half-bridge T-Breaker. (**b**) Three-level full-bridge T-Breaker

3 Normal, Fault Current Limiting and Breaking Operations

3.1 Active Charging of Submodules During Normal Operation

The dc voltage of T-Breaker submodules can be adjustable or optimized for fault current limiting, current breaking, and compensation functions. In general, higher submodule voltage could be beneficial for fault current limiting but could limit the capability of fault energy absorption and introduce high inrush current during series compensation. For the vertical arm, to maintain current regulating capability during shunt compensation, the summation of the submodule voltages needs to be higher than the system dc bus voltage.

Due to the power consumption from auxiliary circuits, bleeding resistors, and the energy drained in compensation operation, submodules' bus voltages can gradually decrease to zero if without active charging. Depending on the location and the topology of submodules, different control schemes can be applied to charge the dc energy storage elements to maintain desired voltage. Since the required charging energy is low, the charging mode only needs to happen at a very low duty ratio during normal operation. Voltage sorting control in classic multilevel converters could also be implemented to ensure voltage balance between all submodules.

For the vertical arm, only unipolar submodule topologies are needed. The submodule voltages are maintained by operating them together like a burst-mode boost converter as illustrated in Fig. 5.4. The phase-shifted pulse-width-modulation (PWM) could be implemented to reduce charging current ripple and disturbance to the load current.

The charging scheme for the horizontal arm depends on the submodule topology. For unipolar topologies, resonant charging procedures can be adopted. As presented in Fig. 5.5a, the vertical arm is bypassed to the ground, while the horizontal arm submodule capacitors are inserted. The benefit of this strategy is its fast speed. However, the charging current is expected to have high amplitude, and the power

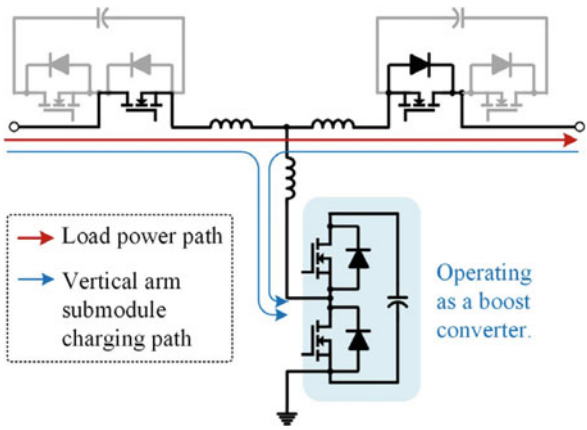


Fig. 5.4 Charging scheme for vertical arm submodules

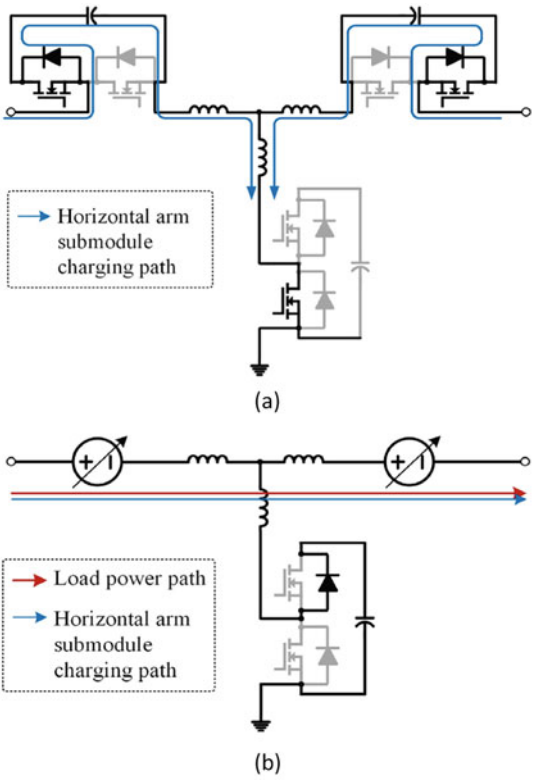


Fig. 5.5 Charging schemes for submodules in horizontal arms. (**a**) Resonant charging with unipolar submodules. (**b**) Active PWM switching charging with bipolar submodules

flow to the load is shortly interrupted. Since the dc load often has its own input capacitors, the very low duty ratio of the interruption will not cause any voltage fluctuation on the load side.

For bipolar submodules, since horizontal arm submodules can be inserted into the power line in both directions, besides resonant charging, active PWM control can be implemented to maintain the submodule voltages. Assuming D (ranging from -1 to 1) is the active-duty cycle of each submodule, when a submodule sees under-voltage or overvoltage, by applying PWM control, an averaged equivalent output voltage of $V_{\text{inj}} = DV_{\text{sub}}$ is injected into the line at the submodule terminals. The amount and the direction of the power flow into each submodule are therefore controlled, and the submodule bus voltage is regulated.

Figure 5.6 shows a SiC-based proof-concept 1-kV, 500-A, 3-level half-bridge unipolar T-Breaker prototype. Test results at normal operation with a 15 A load are shown in Fig. 5.7. With a very small charging duty ratio, the submodule voltage is very well maintained. Though the left arm current has charging pulses, both the source and the load will not see these pulses because of the filter capacitors and the extremely low duty ratio of the charging current.

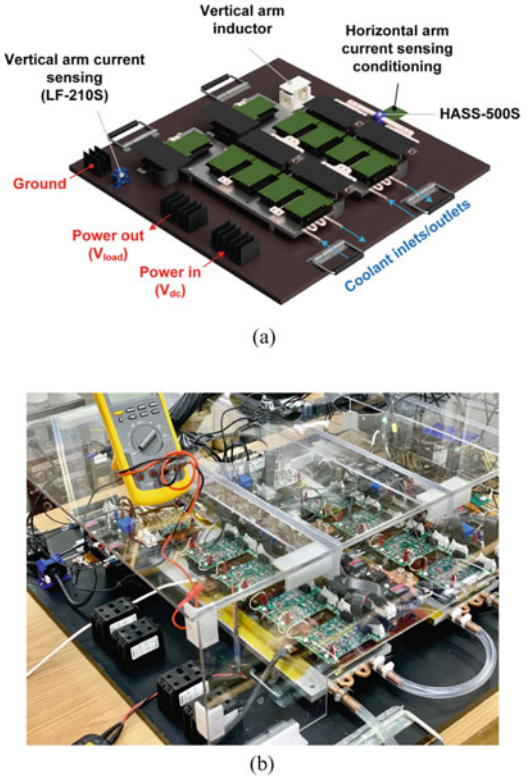


Fig. 5.6 A SiC-based proof-concept 1-kV, 500-A, 3-level half-bridge unipolar T-Breaker prototype. (**a**) 3D-rendering of the 1-kV, 500-A, 3-level half-bridge unipolar T-Breaker prototype. (**b**) Test setup of the 1-kV, 500-A, 3-level half-bridge unipolar T-Breaker prototype

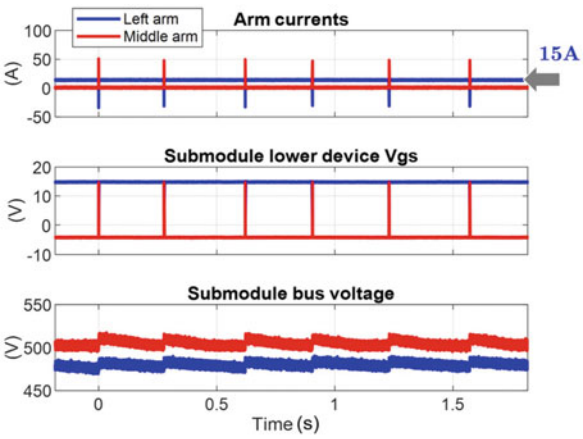


Fig. 5.7 Charging of submodules with low duty ratio

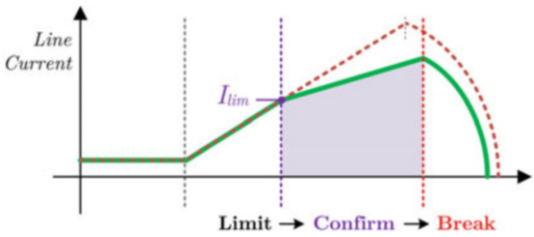


Fig. 5.8 Benefits of fault current limiting

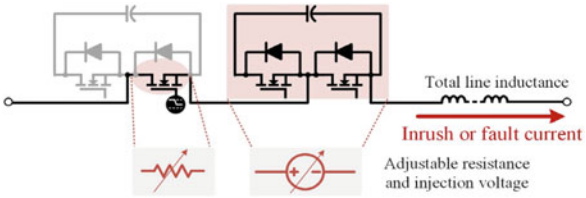


Fig. 5.9 Equivalent circuit of T-Breaker in active current limiting mode

3.2 Fault Current Limiting

During fault conditions, the T-Breaker could act as a Fault Current Limiter (FCL). As shown in Fig. 5.8, if fault current limiting could be implemented after a threshold value (I_{lim}), the breaking current can be reduced, and the confirmation time can be prolonged to avoid false diagnostics.

As shown in Fig. 5.9, the T-Breaker could actively limit line currents in two ways, (a) injecting modulated submodule voltages and (b) driving semiconductor devices into their current-clamping regions, thus equivalently increasing the distribution line impedance.

Scale down fault current limiting tests with voltage injection have been carried out. During the test, the dc system voltage is set as 120 V. The line inductance is set at 51 μH. As shown in Fig. 5.10, when the line current reaches a pre-set value, two submodules are alternatively injected into the line with a 50% duty ratio. The increasing rate of the fault current is effectively reduced.

Additional test results, as summarized in Fig. 5.11, show how the fault current could be regulated. When the duty ratio of the lower device in the submodule is small, which means long submodule voltage insertion time, the fault current could be significantly reduced.

3.3 Fault Current Breaking

With the T-Breaker, fault current breaking can be realized by turning off all the switches at the same time. The half-bridge T-Breaker's fault current breaking commutation is shown in Fig. 5.12a. Assuming fault current flows from left to right, on the left arm, the fault current would shift from the bypassing switch of

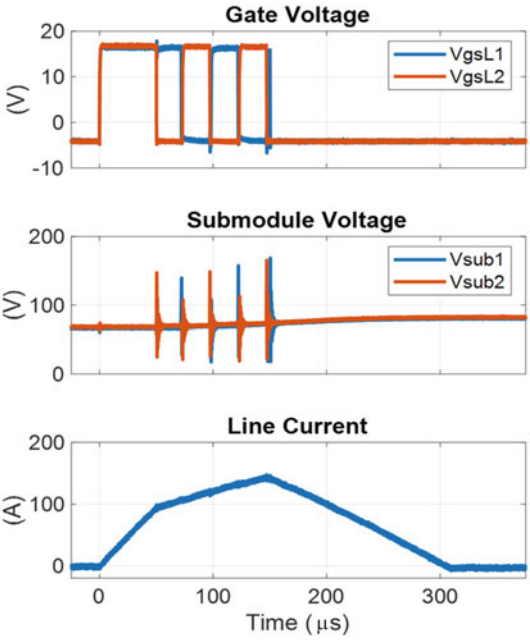


Fig. 5.10 Scale down fault current limiting tests with the 1-kV prototype

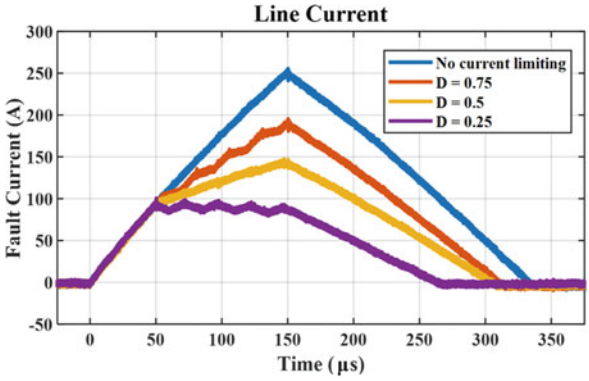


Fig. 5.11 Summary of additional fault current tests that show how the fault current can be regulated

each submodule to the antiparallel diode of the inserting switch. The energy storage devices in the left arm submodules are inserted to absorb fault energy, and their voltages are therefore increasing. On the right arm, the fault current would go through the body diodes of the bypassing switch.

For the bipolar full-bridge T-Breaker, as shown in Fig. 5.12b, energy storage devices in all horizontal arm submodules are inserted to block the fault current and absorb fault energy.

If submodules are only equipped with capacitors without any surge arresters, the breaking current would follow the profile as illustrated in Fig. 5.13. Thus, when a

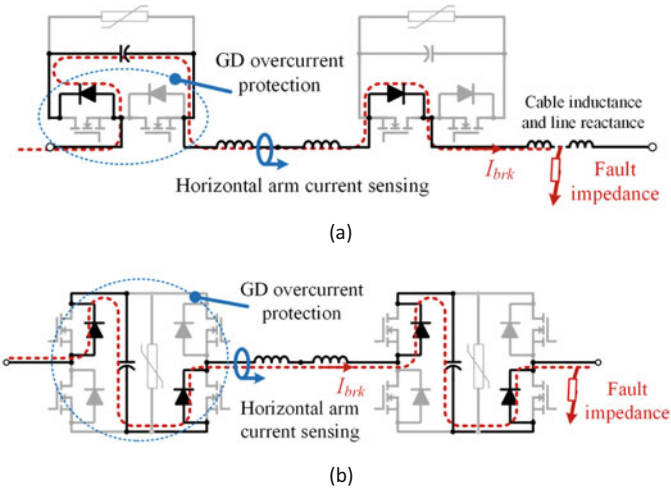


Fig. 5.12 Breaking mode of T-Breakers. (**a**) Breaking current commutation in half-bridge-based T-Breaker. (**b**) Breaking current commutation in full-bridge-based T-Breaker

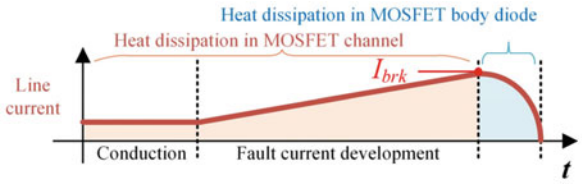


Fig. 5.13 T-Breaker fault current profile

breaking action is initiated at I_{brk}, considering the current loop impedance (R_{flt} and L_{flt}) and the number of inserted submodules (N), the breaking current profile and submodule voltages can be described with Eqs. (5.1) and (5.2), respectively.

Surge protection devices can be added to submodules for their high energy density and their voltage clamping capability. In T-Breakers, the submodule capacitors could absorb a significant amount of fault energy and reduce the energy dissipated in surge protection devices, hence extended breakers' lifetime; the capacitors also can suppress ringing on submodule bus which is introduced by surge protection devices' stray inductance.

$$I_{\text{line}}(t) = I_{\text{brk}} e^{-\frac{R_{\text{flt}}}{2L_{\text{flt}}}t\left[e^{-\sigma t}+\frac{R_{\text{flt}}}{4\sigma L_{\text{flt}}}(e^{\sigma t}+e^{-\sigma t})\right]} \tag{5.1}$$

$$\Delta V_{\text{sub}}(t) = \frac{I_{\text{brk}}}{2\sigma C_{\text{sub}}} e^{-\frac{R_{\text{flt}}}{2L_{\text{flt}}}t\left[e^{\sigma t}-e^{-\sigma t}\right]} \tag{5.2}$$

where $\sigma = \frac{\sqrt{C_{\text{sub}}R_{\text{flt}}^2 - 4L_{\text{flt}}(N-1)}}{2\sqrt{C_{\text{sub}}}L_{\text{flt}}}$.

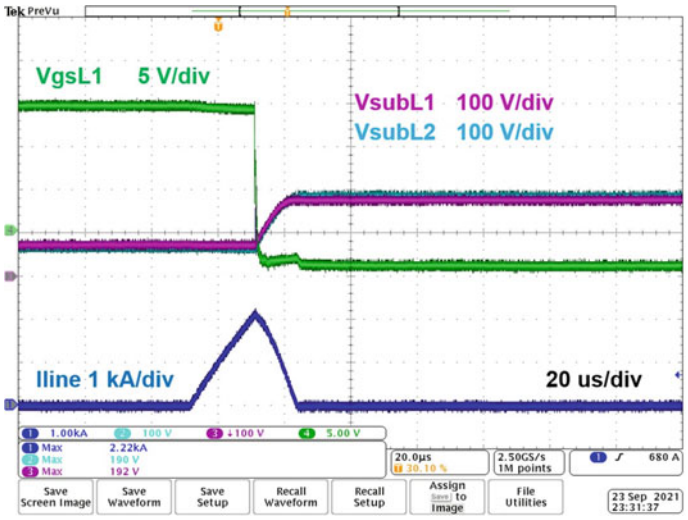


Fig. 5.14 Fault current breaking test waveforms

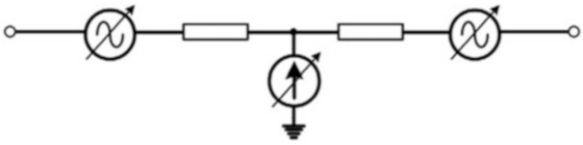


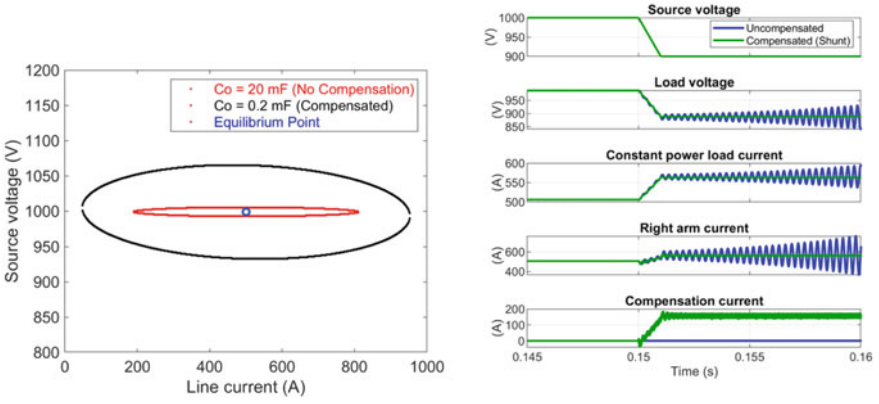
Fig. 5.15 Equivalent circuit of T-Breaker compensation mode

Figure 5.14 shows fault current breaking test waveforms of the 3-level unipolar T-Breaker that is shown in Fig. 5.6. After the breaking event is initiated, voltages on submodule capacitors start to increase until the current eventually reach zero.

4 Transient Stability Enhancement with T-Breaker

T-Breaker could offer ancillary functions similar to series and shunt compensations provided by FACTs devices and custom power devices in ac systems. As shown in the equivalent circuit in Fig. 5.15, with the submodule-based circuit structure, voltage and current can be injected into the power line to enhance power flow control, power quality to the load, and transient stability.

As an example, a comparison study for the abovementioned 1-kV 500-A unipolar T-Breaker prototype has been carried out. In the study, the load is set as a constant power load (CPL); a source voltage sag of 10% is introduced. Region of Attraction (ROA) analysis is performed to show if the system can go back to its equilibrium (stable) or not (unstable). Figure 5.16a shows the comparison between two cases:



(a) (b)

Fig. 5.16 Stability improvement with shunt compensation provided by the T-Breaker. (**a**) Region of attraction comparison. (**b**) Time domain simulation

Case 1: load dc link capacitance is 20 mF, and no compensation is implemented; and *Case 2*: load dc link capacitance is only 0.2 mF while the shunt compensation is enabled. The ROA analysis results show that the shunt compensation can stabilize the system under disturbances with much smaller bus capacitance. This analysis is verified with simulation results as shown in Fig. 5.16b. The simulation results show that when the load side capacitance is only 0.2 mF, without shunt compensation, the system becomes unstable when there is a 10% source voltage sag. At the same condition, the shunt compensation not only made the system stable but also effectively suppressed voltage and current oscillations.

Scaled down tests have also been carried out with the 1-kV 3-level unipolar prototype. During tests, the dc bus voltage is set at 270 V. A constant power load was implemented. Both shunt compensation with the vertical arm and series compensation with horizontal arms have been tested [17].

The shunt compensation was first evaluated against load step change. During the test, the CPL load is first operated at 4 kW, and then the CPL is increased to 6 kW (50% power step). Figure 5.17a shows that without compensation, the system experiences excessive oscillation. Figure 5.17b shows that with compensation, the system stabilizes very quickly.

The shunt compensation was also evaluated against 20% source voltage sag when the CPL load is set at 5 kW. As shown in Fig. 5.18, the shunt compensation can effectively eliminate the system oscillation and make the system more stable.

Series compensation with horizontal arms is also evaluated against source voltage sag. Figure 5.19 shows that with series compensation, when there is a 20% source voltage sag, the series compensation can bring the load voltage to its nominal value and significantly reduce oscillations in the system.

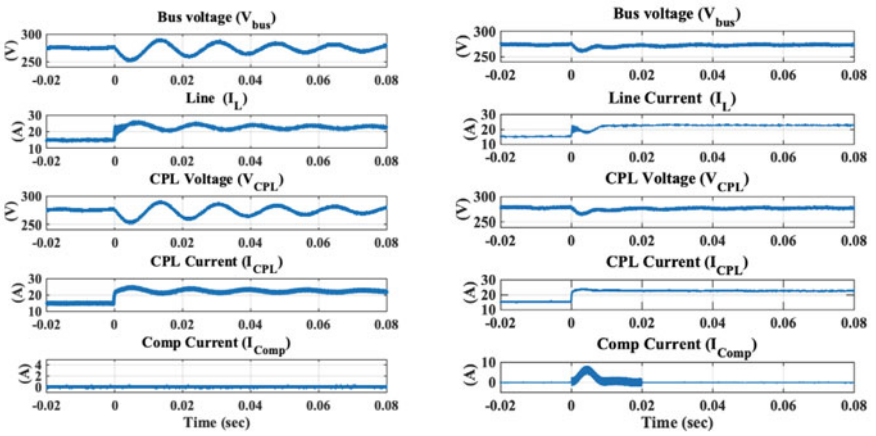


Fig. 5.17 50% step load change test results without and with shunt compensation. (**a**) Without shunt compensation. (**b**) With shunt compensation

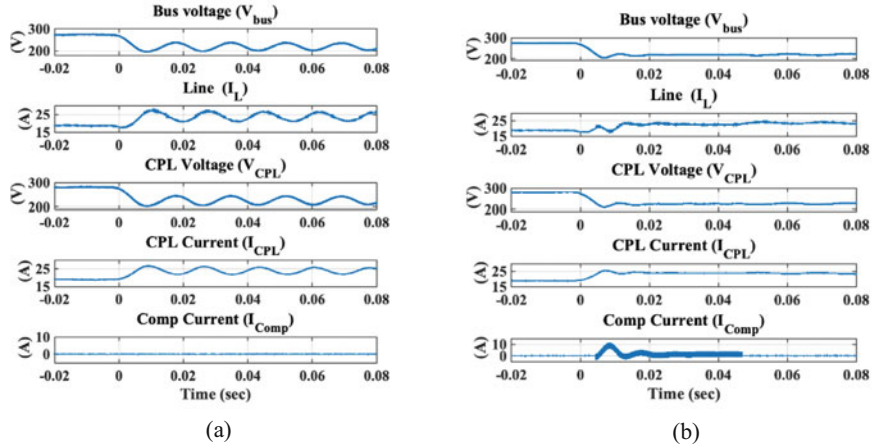


Fig. 5.18 20% voltage sag test results without and with shunt compensation. (**a**) Without shunt compensation. (**b**) With shunt compensation

5 Concluding Remarks

Like ac distribution, future dc distribution will also require reliable circuit breakers and power conditioning circuits that could provide fault protection, power flow control, power quality enhancement, and stability improvements. The T-Breaker introduced in this chapter combines all these required functions into one modular and scalable circuit. The modular structure with integrated energy storage devices

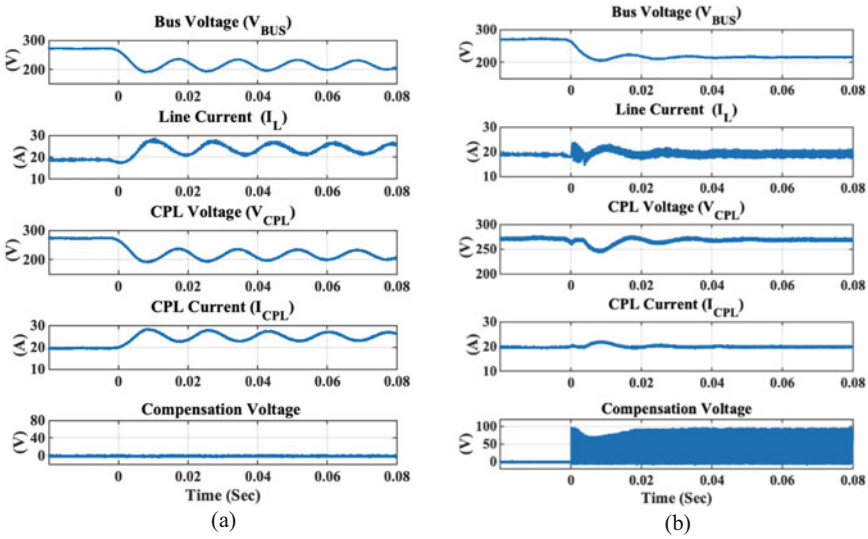


Fig. 5.19 20% voltage sag test results without and with series compensation. (**a**) Without series compensation. (**b**) With series compensation

not only can provide fault current limiting functions and strong immunity to misalignments in the gate control signals but also can be utilized to realize both shunt and series compensations.

The initial prototype and test results have validated all key concepts of the T-Breaker. Full current (500 A) conduction tests and 5 kA breaking tests have also been successfully performed at the Raytheon Technology Research Center. As a result, sponsored by the National Aeronautics and Space Administration (NASA), a 120-V 10-kW Gallium Nitride (GaN)-based T-Breaker prototype is being built to function as an energy router for future dc microgrids on the moon surface [18].

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Chapter 6
Soft Turn-Off Capacitively Coupled SSCBs for MVDC Applications

Fei Lu and Reza Kheirollahi

1 Introduction

Medium-voltage DC (MVDC) systems are growing worldwide [1]. Compared with alternative current (AC) counterparts, DC systems eliminate the need for frequency synchronization and reactive power compensation, facilitate using renewable energies, present potential advantages for integration of distributed generations and energy storage systems, and reduce the number of energy conversion stages [2, 3]. Besides, in recent years, a massive expansion of DC loads such as data centers and electric vehicle charge stations has been reported [4]. This highlights the significance of research in this field for both academia and industry.

However, the progress of MVDC systems faces technical limitations. Among many factors, circuit breakers are under early development [1, 5–7]. On one hand, due to the lack of zero crossing points in DC currents and the low inertia of DC systems, AC circuit breakers are not effective in interrupting large DC currents [8]. On the other hand, downsized versions of high-voltage DC (HVDC) circuit breakers do not lead to compact and efficient topologies [9]. Therefore, it suggests an urgent need to develop reliable, efficient, fast, and compact circuit breakers targeting MVDC applications.

Compared with mechanical and hybrid circuit breakers, SSCBs present remarkable advantages. They benefit from a fast response speed within microseconds, high compactness, and scalability [10–12]. Also, recent developments in wide bandgap semiconductor devices have resulted in more efficient circuit breakers as the result

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of smaller on-state resistance and extended electrical ratings [13, 14]. In contrast, achieving high efficiency in SSCBs leads to an expensive design [13]. According to the survey conducted in [15], most of the design cost of an SSCB is related to solid-state switches. Therefore, the reliability of the solid-state switches in circuit breakers is of great importance.

Energy-absorbing components are inseparable from DC circuit breakers. DC systems include line inductors to slow down the rising rate of short circuit fault currents [16]. The corresponding inductive energy needs to be dissipated during DC current breaking. However, solid-state switches have a limited energy dissipation capability [17]. To overcome this difficulty, energy absorption components are employed. Metal oxide varistors (MOVs), paralleled MOVs, MOV and resistor-capacitor (MOV-RC), and MOV and resistor-capacitor-diode (MOV-RCD) snubbers are commonly used in conjunction with solid-state switches [14].

Passive snubbers have limitations in SSCBs. MOV-based snubbers clamp voltage oscillations well, but they bring extremely high dv/dt across the main switch. MOV-RC and MOV-RCD snubbers overcome this problem as snubber capacitance helps effectively during the transient; MOV-RCD has better current capability compared with the RC snubbers; however, they suffer from a conflict between the response speed and power shock reduction during DC current interruption [18]. That is, increasing the snubber capacitance decreases the power shock on the solid-state switches, but it elongates the reaction time interval in the breakers. The situation is worsened when ultrafast SSCBs aim to be optimally coordinated in DC systems [19].

This chapter deals with the application of auxiliary active injection circuits in eliminating power shock on solid-state switches in SSCBs. Active injection circuits have been reported in mechanical and hybrid breakers to alleviate the arcing problem in mechanical disconnectors during DC current interruption [20–22]. In mechanical breakers, the countercurrent pulse is generated by a resonant LC circuit, and it is controlled by an injection switch. The injection capacitor in the auxiliary branch can be charged by an external charger [22] or through the DC system itself [23]. The former gives the flexibility of adjusting the injected pulse current's amplitude and duration, while the latter benefits from simplicity. The injection capacitor and inductor are chosen regarding the fastness of the main switch S_{m}, the maximum fault current aimed to be interrupted in the system, the maximum voltage value on the injection capacitor, and the power density limitation of the targeted design.

The capacitive coupling interface is also introduced in this chapter, where it helps to enhance reliability in active injection-based breakers. In DC breakers where the auxiliary branch is directly connected to the main branch, they are prone to short circuit faults in the auxiliary injection circuits. This puts the reliability of DC systems at serious risk. To avoid this issue, capacitive couplers are introduced which act as the interface between the main and auxiliary branches and block short circuit fault currents. The operation of MVDC SSCBs based on a capacitive coupling interface will be demonstrated throughout the chapter.

2 Soft Turn-Off Operation in SSCBs

Even though solid-state switches in DC breakers undergo a limited number of switching, they experience large dv/dt and di/dt values. These result in high gate voltage oscillations leading to device failure or false turn-on operation during DC current interruption. MOV-RCD snubber circuits are considerably effective in mitigating the mentioned phenomenon; however, they are not able to fully solve the problem [24, 25].

High power shock on solid-state switches during the dc current interruption is another critical reliability issue. In SSCBs, solid-state switches are responsible for interrupting large DC currents. In this case, depending on fault currents amplitude and the snubber circuits, a relatively large transient power may appear on the solid-state switches [24]. Accordingly, high transient energy produces in the switches during a very short period [18].

This transient energy could be the source of two major separate failures including gate degradation and thermal runaway [26]. These two failures are the result of the fast growth rate of the temperature inside the device. The temperature dynamic and its growth rate are proportional to the transient power and energy in which the device is subjected to. Degradation and thermal runaway temperatures are two distinct boundaries in solid-state switches. The degradation of the gate structure occurs when the surface is exposed to degradation temperature for a sufficient time. This results in partially or entirely losing current conduction capability. In case the temperature reaches the thermal runaway boundary, the drain current increases exponentially followed by a permanent device failure.

Gate voltage oscillations and transient power are current-dependent. Meaning that reducing the current amplitude in solid-state switches during DC current interruption helps to mitigate the pointed challenges. The soft turn-off is a promising solution in this matter [22, 24], which will be elaborated in the following.

Soft turn-off operation refers to the situation in which the DC current in the switch is forced to zero during dc current breaking. To achieve this, active injection circuits with precharge injection capacitors are utilized. The general structure of the presented concept is shown in Fig. 6.1a. The breaker includes three branches connected in parallel: main branch, auxiliary branch, and energy-absorbing branch, illustrated in the following.

The critical current and voltage waveforms of the soft turn-off breaker are shown in Fig. 6.1b. In normal operating mode, the main branch conducts the load current through the main switch S_{m}, and current in the auxiliary and energy-absorbing branch is zero. It is assumed that a short circuit fault occurs at $t = t_0$, and the system current begins to increase. The current interruption process includes three main stages: the current reaction process, soft turn-off operation, and energy absorbing stage.

During the reaction time interval ($t_1 \leq t < t_2$), a countercurrent pulse is created by the auxiliary branch, and it is injected into the main branch to cancel the fault current in the main switch. Next, at $t = t_2$, when the current in the main switch S_{m}

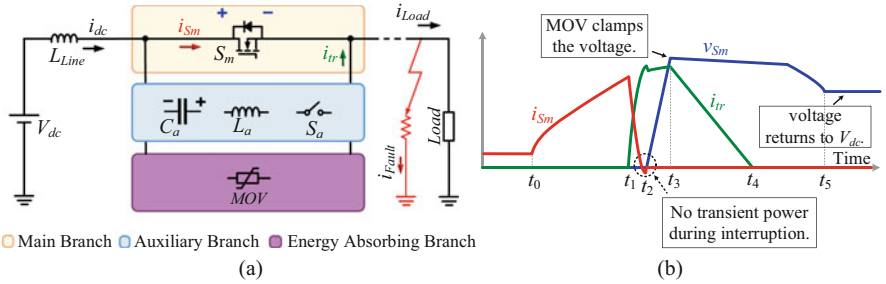


Fig. 6.1 Soft turn-off operation [22]. (**a**) The general structure of active current injection-based SSCBs is shown; the main branch includes solid-state switches; the auxiliary branch consists of injection components, and the energy-absorbing branch involves MOVs (**b**) Corresponding critical current and voltage waveforms (labeled in Fig. 6.1a) are represented

reduces to zero, S_m is triggered to be OFF. Then, the commutated fault current in the auxiliary branch is interrupted, forcing the fault current to the energy-absorbing branch ($t_3 \leq t < t_5$). Finally, the energy-absorbing elements dissipate the stored inductive energy of the line inductor.

The operation of the breaker shown in Fig. 6.1 reveals the soft turn-off during the DC current interruption. First, at the time of turning off the main switch, the current in the main switch is almost zero, which helps to mitigate the gate voltage oscillations. Also, as labeled in Fig. 6.1b, when the voltage across the solid-state switch begins rising, the current in the switch is zero, meaning zero power shock in the solid-state switch. All of these features are effective in enhancing the reliability of the breaker and extending its lifetime [24].

There are two kinds of modularity in the soft turn-off SSCBs. Regarding Fig. 6.2a, multiple solid-state switches can be connected in parallel to achieve higher efficiency and current interruption capability [14]. In this case, to achieve a soft turn-off operation, each solid-state switch is accompanied by its auxiliary and energy storage branches. In addition to simplicity during the design procedure, this kind of modularity results in current scalability, which is highly useful for the future development of DC systems. Also, it is highly effective in addressing any possible glitch between digital signals received by multiple solid-state switches in the main branch. In other words, if one of the switches in the main branch turns off sooner, the provided modularity prevents any damage to other switches due to resulted uneven current distribution.

Figure 6.2b indicates the second type of modularity, where multiple active injection auxiliary branches are connected in parallel to the main branch [22]. The goal is to obtain injection countercurrent pulses with different amplitudes for fault currents under different fault resistances. Each auxiliary branch could involve a unique injection inductor, resulting in a unique injection countercurrent pulse. Modularity can be achieved by activating different combinations of auxiliary branches during DC current interruption. Each auxiliary branch may include its precharge injection capacitor, or all the auxiliary branches can share one injection

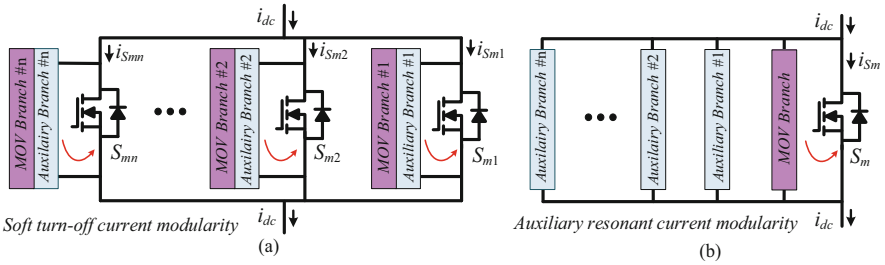


Fig. 6.2 Implementing modularity in soft turn-off SSCBs. (**a**) Each solid-state switch has its auxiliary and MOV branches. (**b**) Modularity in this topology can be achieved by generating countercurrent pulses with adjustable amplitudes and durations

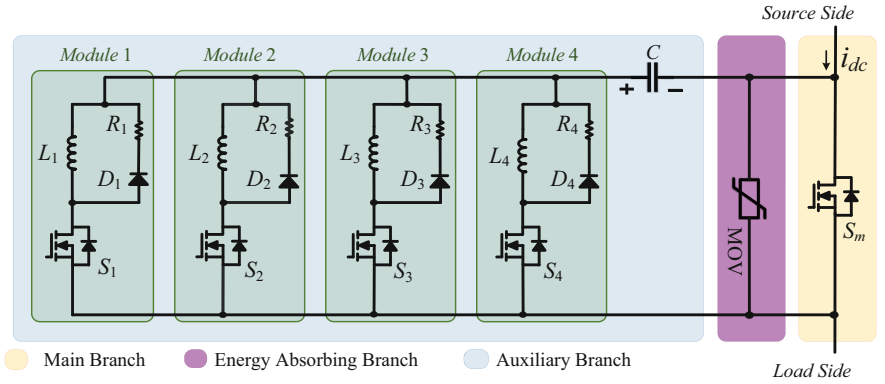


Fig. 6.3 Modular active injection circuits in a soft turn-off SSCB corresponding to Fig. 6.2b [22]. The auxiliary branch includes one injection capacitor; however, multiple injection inductors are connected in parallel. The value of injection inductors is optimized to achieve adjustable pulse currents

capacitor as shown in Fig. 6.3 [22]. For both cases, the SSCB only consists of one MOV branch directly connected in parallel to the main branch.

On the other hand, DC circuit breakers with active injection circuits shown in Fig. 6.1 are prone to short circuits in the auxiliary branch. This practical issue could reduce the reliability of the implemented protection systems and result in safety challenges. Figure 6.4 shows two general structures of DC circuit breakers with auxiliary circuits in DC systems. In Fig. 6.4a, the precharge injection capacitor is fully charged through an external charger; while in the topology of Fig. 6.4b, the injection capacitor is charged by the DC system itself controlled by a charging switch.

In both structures of Fig. 6.4, the potential failures are shown [27]. In Fig. 6.4a, the short circuit failure path creates its way through the injection inductor L_a, the injection switch S_a, and the external charger V_{Ch}-S_{Ch}. In such a short circuit failure, the circuit breaker is bypassed, leaving the DC system without protection. In the

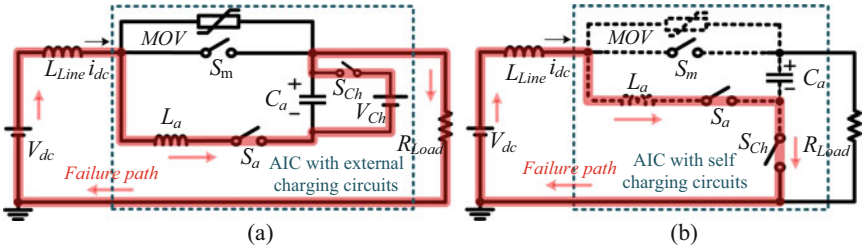


Fig. 6.4 Potential short circuit failures in active injection circuit-based circuit breakers [27]. (**a**) A short circuit may occur through the external charging converter, bypassing the circuit breaker and leaving the DC system without any protection. (**b**) Short circuit failure may occur through the injection switch S_{ch}, resulting in a short circuit in the DC link

second scenario of Fig. 6.4b, the failure path leads to a short circuit close to the DC source; the fault is created through the injection inductor L_a, the injection switch S_a, and the charging switch S_{Ch}. Although a residual current mechanical disconnector can separate the circuit breakers from the DC source during the OFF-state, it is not practical when multiple SSCBs are in the DC systems [28, 29]. Therefore, solving the problem inside the circuit breakers is more effective.

3 Capacitively Coupled Soft Turn-Off SSCBs

A capacitive couple-based interface is a promising solution to prevent the potential failures described in Fig. 6.4. The general topology is shown in Fig. 6.5a [27]. The auxiliary branch is connected to the main branch through two coupling capacitors. The couplers allow the transient pulse currents during DC current interruption, but they prevent short circuit faults in the case of any failure. The coupling capacitance is in the range of hundreds of nano-Farad, which can be easily built using couplers with enough airgap for the sake of voltage isolation. As the capacitance is low, it does not reduce the power density of the final design.

Regarding Fig. 6.5, a few points can be highlighted below:

1. As coupling capacitors are in the range of hundreds of nano-Farad, the injected pulse current during DC current interruption should be short with sufficient flat-top profile (Δt_β in Fig. 6.5b) to achieve soft turn-off operation.
2. The auxiliary branch is completely isolated from the DC power system; in this case, an external charger is used to charge the injection capacitor C_a in the auxiliary branch.
3. When the main switch S_m is ON, the voltage across the coupling capacitors is almost zero. During the turn-off process, coupling capacitors share the DC bus voltage. Also, overshoot voltages across the couplers can be clamped as will be further described in the section.

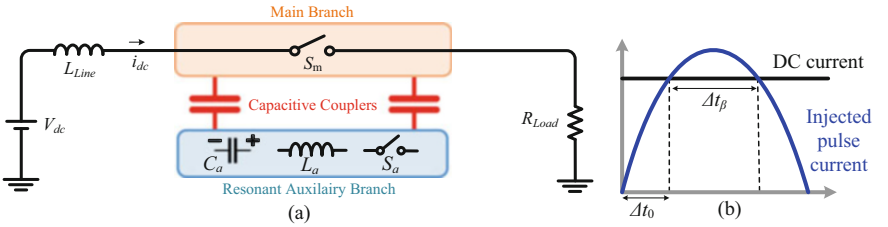


Fig. 6.5 Capacitively coupled current commutation [27]. (**a**) A capacitive couple-based interface between the main branch and the auxiliary branch is shown. Coupling capacitors allow pulse current to flow through between two branches, but they block the flowing of short circuit fault currents. (**b**) The emulated injected pulse current and the DC fault current are shown in (**b**); Δt_β is required to achieve a soft turn-off operation; Δt_0 should be minimized to optimize coupling capacitors

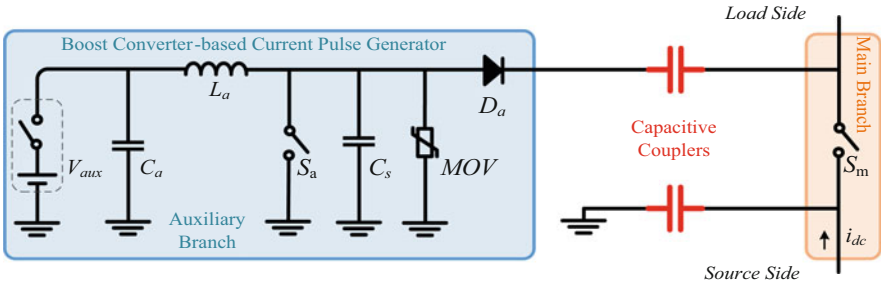
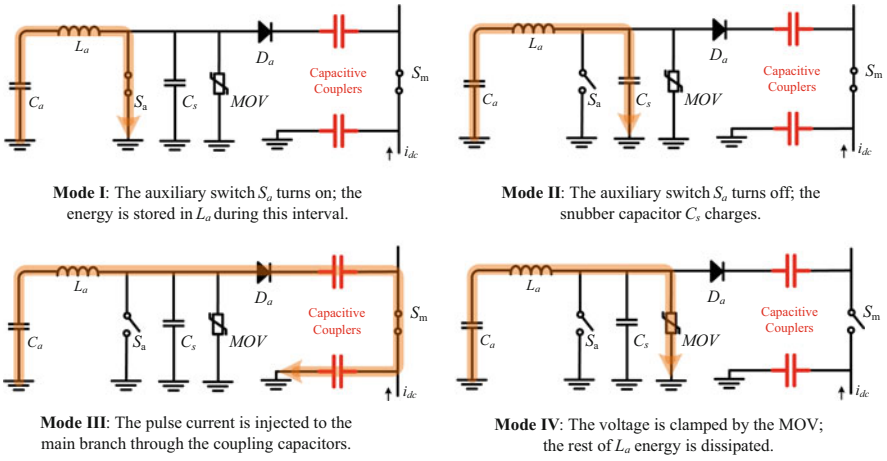


Fig. 6.6 Boost converter-based current pulse generator is represented [30]. The current pulse generator is designed using the working principle of the Boost converters

4. A well-defined digital communication is required between the main and auxiliary branches during DC current interruption.
5. Both modular topologies illustrated in Fig. 6.2 can be applied to the capacitively coupled SSCBs.
6. Energy-absorbing elements can be directly connected in parallel to the main branch, and it does not interfere with the operation of the auxiliary branch and the capacitive couplers.

With respect to Fig. 6.5a, the auxiliary active injection branch should generate a pulse current with a short duration to optimize the coupling capacitors. That is, Δt_β of Fig. 6.5b aims to be decreased as much as possible, which helps to reduce charge currents flowing through the coupling capacitors. To achieve this goal, the Boost converter-based current pulse generator of Fig. 6.6 is highly applicable [30].

The current pulse generator mainly includes an auxiliary low voltage DC source V_{aux}, an injection precharge capacitor C_{a}, an injection inductor L_{a}, an injection controlling switch S_{a}, a snubber capacitor C_{s}, an MOV element for protecting the injection switch, and an output diode D_{a}. The auxiliary branch is connected in



Mode I: The auxiliary switch S_a turns on; the energy is stored in L_a during this interval.

Mode II: The auxiliary switch S_a turns off; the snubber capacitor C_s charges.

Mode III: The pulse current is injected to the main branch through the coupling capacitors.

Mode IV: The voltage is clamped by the MOV; the rest of L_a energy is dissipated.

Fig. 6.7 The operating modes of the Boost converter-based current pulse generator are represented [30]. It is assumed that the injection capacitor C_a is charged by the auxiliary source V_{aux}, and V_{aux} is not involved in the presented analysis

parallel to the main branch through the capacitor couplers. The main branch consists of MOSFET switches whose body diodes help achieve soft turn-off operation.

Figure 6.7 indicates the operating modes of the Boost converter-based current pulse generator in injecting a countercurrent pulse current to the main switch S_m. The operation is explained in the following.

Mode I The auxiliary switch S_a turns on, and the energy stored in the precharge injection capacitor C_a is transferred to the injection inductor L_a. The inductor current begins to increase whose slope depends on the pre-charge voltage on the injection capacitor V_{aux}, the injection capacitance C_a, and the injection inductance L_a. During this mode, no current flows through diode D_a and capacitive couplers. Also, as the injection switch S_a is ON, the voltage across the snubber capacitor C_s, the MOV, and coupling capacitors remains zero.

Mode II The amplitude of the injection inductor current reaches a threshold value specified in the SSCB; then, the control algorithm triggers the injection switch S_a to be OFF. In this case, the snubber capacitor C_s, connected in parallel to S_a, starts charging. The value of C_a is chosen optimally to protect S_a from high dv/dt during the turn-off process. The voltage across C_a continues increasing; the current in the injecting diode D_a is still zero.

Mode III The voltage across the snubber capacitor C_s reaches the auxiliary voltage V_{aux}. The injection diode D_a turns ON, where it begins to conduct the countercurrent pulse and inject it to the main branch through the capacitive couplers. Simultaneously, the current in the main switch S_m reduces to zero, obtaining a current zero-crossing point in the main switch. As the current approaches zero in S_m, the main branch's control board turns S_m off, meaning a soft turn-off operation,

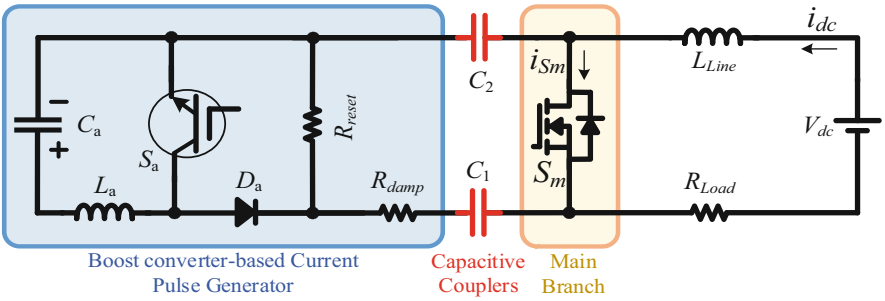


Fig. 6.8 Capacitive couple-based SSCB is shown in a medium voltage DC system with the line inductor L_{Line} and the resistive load R_{Load} [27]. The Boost converter-based current pulse generator is connected to the main branch through coupling capacitors C_1 and C_2

e.g., Fig. 6.1b. It is noted that the body diodes of the main switch S_{m} are effective, highlighted in the next section.

Mode IV As the pulse current flows through the capacitive couplers, the coupler's voltage rises. As the voltage reaches the clamping voltage of the snubber MOV, the MOV switches to the clamping mode. The MOV's resistance reduces significantly and conducts the tail of the injection inductor current L_{a}. In this case, the current in the injection diode D_{a} and the coupling capacitors reduces to zero. The MOV continues in the conduction mode till it absorbs all the energy of the injection inductor L_{a}. Finally, the MOV returns to the leakage current mode and blocks the auxiliary voltage V_{aux}.

The design procedure of the current pulse generator has been well described in [30]. The primary aim is to obtain a countercurrent pulse with sufficient amplitude and profile to implement a reliable soft turn-off during DC current interruption. The next design objective is minimizing the capacitance of the couplers, as it helps to achieve a compact and low-cost design. Therefore, the auxiliary source voltage V_{aux}, the injection capacitor C_{a}, the injection inductor L_{a}, and the clamping voltage of the snubber MOV along with all the parasitic components are included in the design procedure.

Regarding the soft turn-off technique, the capacitive couple-based interface, and the Boost converter-based pulse current generator, an MVDC soft turn-off SSCB with the capacitive couple interface is developed and analyzed. Figure 6.8 indicates the capacitively coupled MVDC SSCB [27]. The dc bus voltage is V_{dc}, L_{Line} emulates the line inductor, and the load is assumed to be resistive R_{Load}. The main branch is constructed from SiC power MOSFET modules. The auxiliary branch follows the same topology as the current pulse generator in Fig. 6.6. Capacitive couplers are labeled as C_1 and C_2 whose values are assumed to be the same, meaning $C_1 = C_2 = C$.

As indicated in Fig. 6.8, the current pulse generator also includes the couplers reset resistor R_{reset} and the damping resistor R_{damp}. The couplers' reset resistor

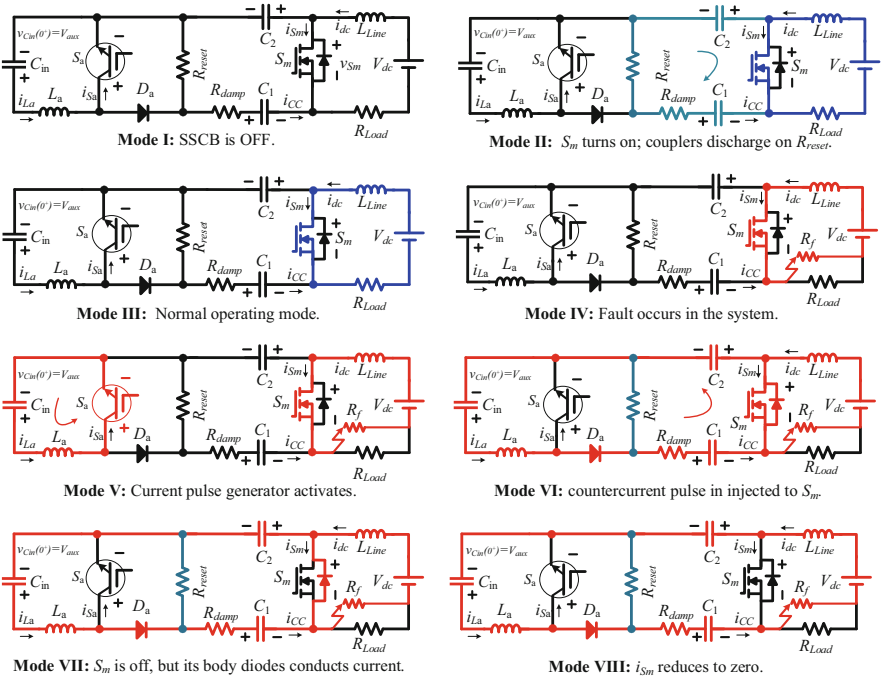


Fig. 6.9 The operating modes of the capacitive couple-based SSCB are shown [27]. The circuit breaker is in a DC system with the line inductor L_{Line} and the load R_{Load}. Modes II and III indicate the closing process and couplers reset mode. Also, a short circuit fault is emulated by R_{f}, where it starts from mode IV. The circuit breaker reacts to fault in mode V

is used to discharge the capacitive couplers when the main switch S_{m} turns on, but small values of R_{reset} result in leakage currents during the breaker OFF-state. Therefore, a tradeoff should be made in selecting R_{reset}. Also, the damping resistor R_{damp} damps the ringing flat-top of the injected countercurrent pulse, but large values of R_{damp} lead to a small Δt_{β} shown in Fig. 6.5b.

The operating modes of the capacitively coupled soft turn-off SSCB are shown in Fig. 6.9, where the closing process, normal operating mode, and fault current interruption are indicated. Also, the corresponding critical electrical waveforms of Fig. 6.9 are displayed in Fig. 6.10. Regarding Figs. 6.9 and 6.10, the operation of the breaker is explained below.

During mode I (before t_0), the circuit breaker is OFF. The DC bus voltage places on the main branch $v_{\text{Sm}} = V_{\text{dc}}$. In the auxiliary branch, the injection capacitor C_{a} charges to V_{aux} using an auxiliary voltage source $V_{\text{Cin}} = V_{\text{aux}}$. As the current in the injection inductor L_{a} is zero, the injection switch S_{a} holds the same V_{aux} voltage, meaning $v_{\text{Sa}} = V_{\text{aux}}$. Each capacitive coupler holds half of $V_{\text{aux}} + V_{\text{dc}}$. It is noted that both coupling capacitors are assumed to be the same; in this case, $v_{C1} = v_{C2}$.

The circuit breaker turns on during modes II and III ($t_0 \leq t < t_1$) and undergoes its closing stage and capacitive couplers' reset process. S_{m} turns on at $t = t_0$ and

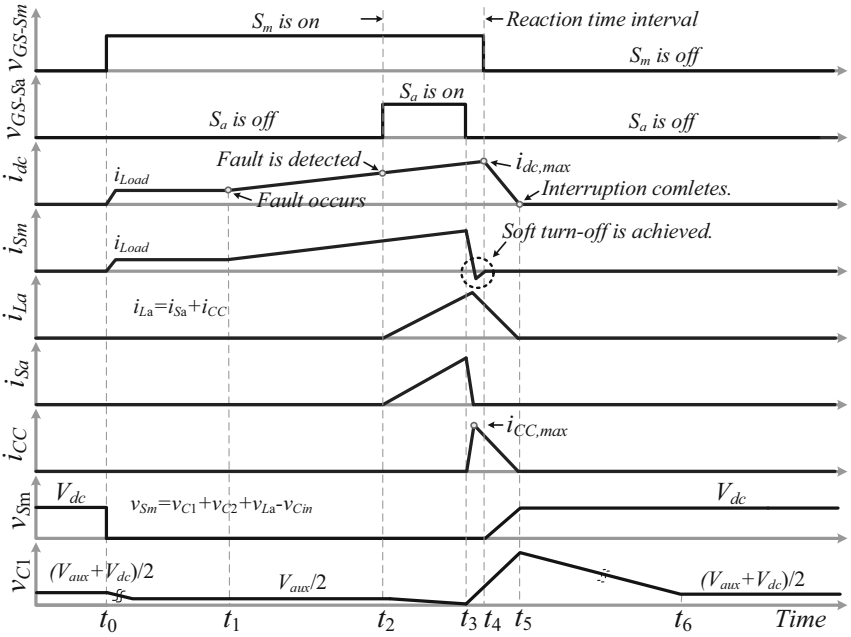


Fig. 6.10 The critical electrical waveforms of the capacitive couple-based SSCB are shown [27]. The intervals consist of the OFF-state (mode I before t_0), closing stage (mode II at $t = t_0$), couplers reset mode (mode II during $t_0 < t < t_1$), normal operating mode (mode III during $t_0 < t < t_1$), fault occurrence (mode IV during $t_1 \leq t < t_2$), and fault current interruption ($t_2 \leq t < t_6$) are shown

conducts the load current. The capacitive couplers begin discharging on the reset resistor R_{reset}, where their voltage finally reaches $v_{C1} = v_{C2} = V_{\text{aux}}/2$. The current in the auxiliary branch remains zero. There is a leakage current in resistor R_{reset}, but it is negligible.

A short circuit fault with the fault resistance R_{f} occurs at $t = t_1$ during mode IV. The circuit breaker reacts to the fault during mode V by turning on the injection switch S_{a} ($t_2 < t < t_3$). Consequently, the pulse current in the injection inductor L_{a} increases. As shown in mode VI, at $t = t_3$, S_{a} turns off, and the current of the injection inductor L_{a} flows through the capacitive couplers as also described in Fig. 6.7.

In mode VII, at $t = t_4$, the main switch S_{m} current reduces to zero, and S_{m} is triggered to be OFF. A soft turn-off operation is achieved, where S_{m} turns off under zero power shock. During mode VIII ($t_4 < t < t_5$), the fault current commutates to the auxiliary branch, and it finally reduces to zero. Also, the remaining inductive energy of the injection inductor L_{a} is dissipated in the snubber MOV (refer to Fig. 6.7). The interruption completes, and the circuit breaker goes back to mode I. The voltage on S_{m} stabilizes on V_{dc}, and the voltage on each coupler is $(V_{\text{aux}} + V_{\text{dc}})/2$.

4 Experimental Study of Capacitively Coupled-Based SSCBs in MVDC Systems

To further analyze the proposed capacitively coupled soft turn-off SSCB, it is experimentally studied [30, 31]. Figure 6.11 shows the experimental setup. The SSCB is shown in Fig. 6.11. In the main branch, 12 CAB-450M12XM3 SiC MOSFET power modules are connected in a 4 × 3 matrix. MOV-RCD snubber circuits include MOV V661HA40, the snubber diode C4D20120, and 100 Ω and 200 nF as the snubber resistor and capacitor, respectively. The main branch gate drivers are supplied by an inductive wireless power transfer system to obtain voltage isolation between four layers. The main branch is controlled by a TMS320F28335 DSP from TI.

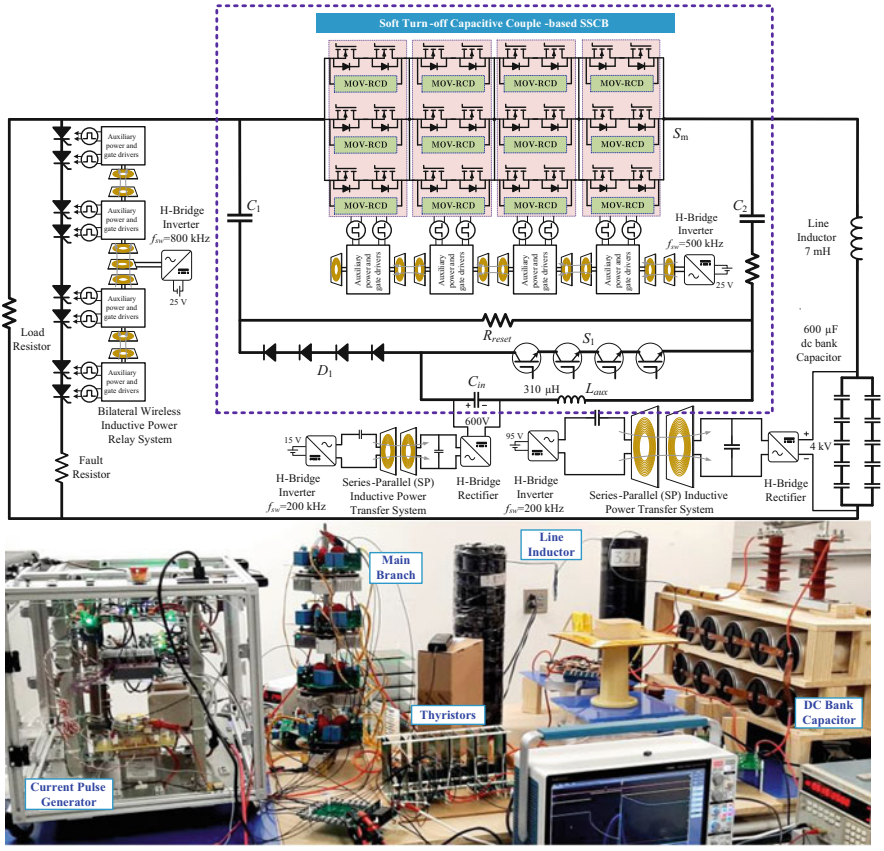


Fig. 6.11 4 kV/100 A DC short fault current interruption setup [31]. The system involves a 600 μF DC link capacitor charged to 4 kV using an inductive wireless capacitor charger. The line inductor is 7 mH; the load resistance is set to 285 Ω. Thyristor switches are used to emulate a short circuit fault current. The schematic of the soft turn-off capacitive couple-based SSCB is highlighted, where main branch switches are constructed from 12 SiC power modules in a 3 × 4 matrix

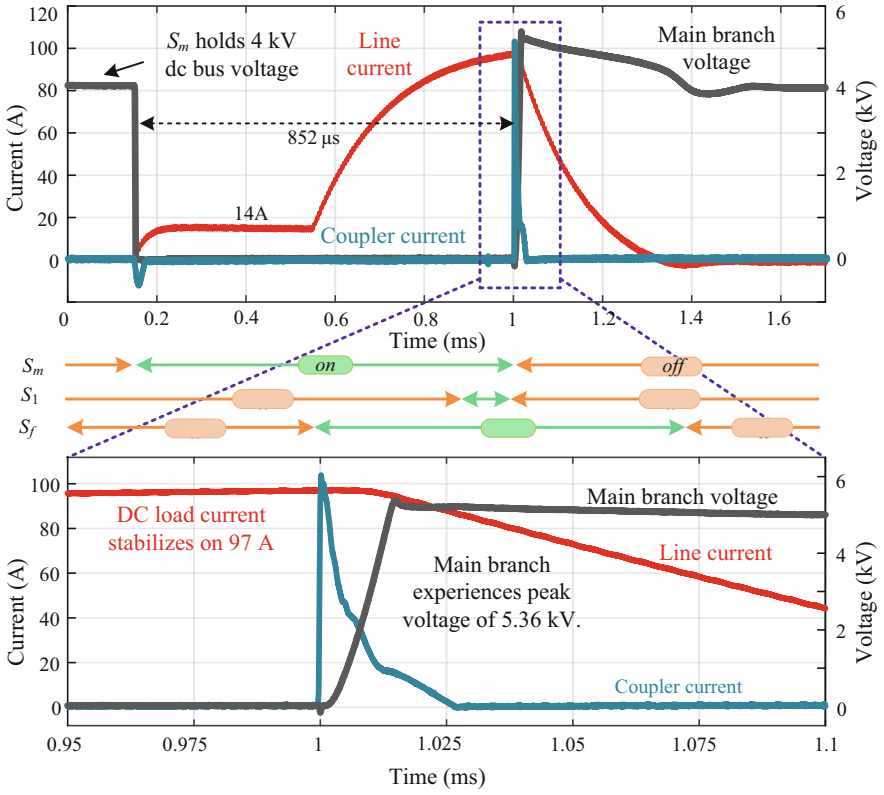


Fig. 6.12 Experimental results of the soft turn-off capacitive couple-based SSCB [31]. The main branch voltage, line current, and capacitive couple current waveforms are represented

Two 280 nF/10 kV film capacitors are used as the coupling interface between the main and auxiliary branches. In the auxiliary branch, two 5SNG-0300Q170300 IGBT power modules are used for the injection switch S_a. The injection inductor is $L_a = 314$ µH; the injection capacitor $C_a = 200$ µF, where its voltage is kept at 600 V using a series-parallel inductive wireless power transfer converter. The injection diodes are C4D20120, and the R_{reset} and R_{damp} resistors are 3 kΩ and 15 Ω, respectively. The breaker is tested in a 4 kV DC system, where the line inductor is 7 mH and the resistive load is 285 Ω. To emulate a short circuit fault, four MCNA650P2200CA thyristors are connected in series, where a bilateral wireless power relay system is used to trigger the thyristors reliably.

Figure 6.12 shows the experimental results. The line current, capacitive coupler currents, and the main branch voltage are indicated. In steady-state, the circuit breaker supplies 14 A load current. A short circuit fault is created at $t = 550$ µs through the thyristor switches. The breaker interrupts the fault current within 77 µs, where the peak of system current reaches 97 A and S_m experiences 5.36 kV overshoot voltage.

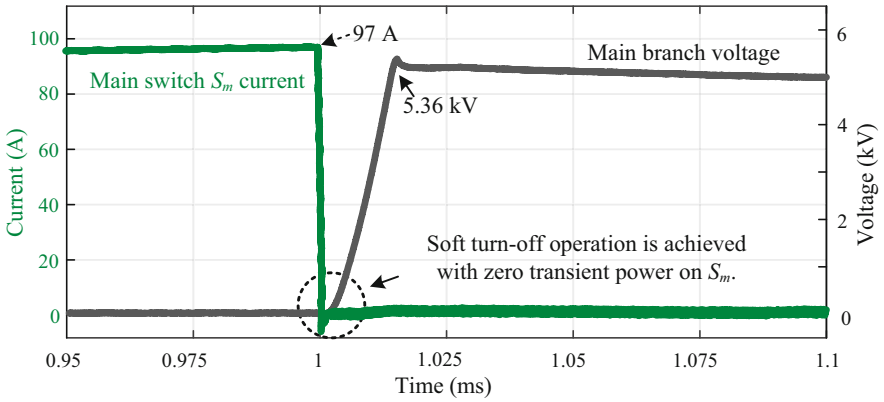


Fig. 6.13 Experimental results of the soft turn-off capacitive couple-based breaker. The main branch voltage and the main switch current waveforms are shown. As indicated, the main switch S_m turns off under zero power shock

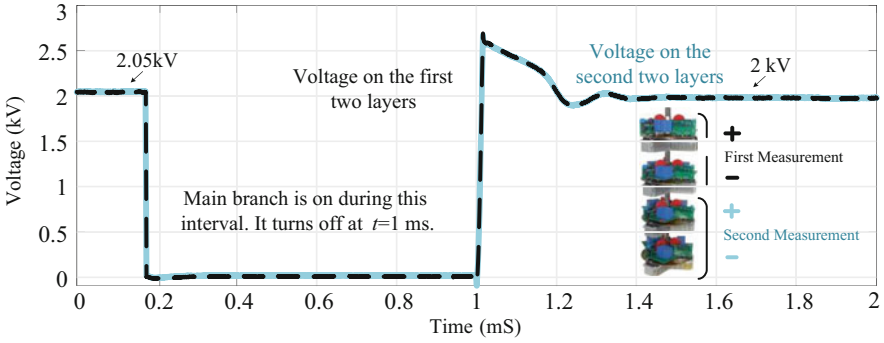


Fig. 6.14 Experimental results of the soft turn-off capacitive couple-based breaker [31]. The voltage balance between different layers of the main branch is shown. The voltage measurements indicate a voltage balance between the top two layers and the bottom two layers

Figure 6.13 reveals one of the promising advantages of the soft turn-off SSCB based on a capacitively coupled interface. The main switch current and the main branch voltage waveforms are displayed in Fig. 6.13. According to the operation of the capacitive couple-based SSCB, the main switch S_m turns off when the current in S_m reduces to zero. That is, the main switch voltage rises when there is no current in S_m, leading to a zero transient power on the main switch. This point has been highlighted in Fig. 6.13. The achieved zero power shock in the main switch S_m obtains a safe operation, improves its current interruption capability, and helps to enhance reliability.

Furthermore, Fig. 6.14 shows the transient voltage balance between the top and bottom layers during DC current interruption, which verifies the effectiveness of the

implemented symmetrical and efficient structure in the main branch. As is clear in Fig. 6.14, the voltage of the top two layers and the bottom two layers are evenly balanced during the transient and steady-state operation.

5 Conclusions

Applying transient current commutation to DC SSCBs achieves a soft turn-off operation during current interruption. For soft turn-off SSCBs, in the main branch, the voltage and current waveforms of the main switch have no overlaps during the turn-off process, leading to zero transient power and energy. Also, reducing the main switch current to zero mitigates the gate's voltage oscillations, resulting in a higher degree of reliability. When the main switch experiences a high change in its drain-source voltage, its gate voltage has already stabilized at zero or negative values, which reduces the possibility of a false turn-off. All these advantages improve the reliability of the SSCBs and extend the lifetime in the long term. Meanwhile, the active injection branch is fast and compact under modularity and scalability.

A capacitive couple-based interface between the main and auxiliary branches enhances the reliability of the DC system under operation. It prevents short circuits in the DC link close to the upstream breakers. In the meantime, a Boost converter-based current pulse generator allows transient current commutation through capacitive couplers. The current pulse generator works with a low-voltage auxiliary source, its generated pulse current is adjustable in terms of amplitude and duration, and it communicates synchronously with the main branch in a reliable manner. As the injected pulse current is short, the coupling capacitors' values are small, resulting in a compact design. The capacitively coupled soft turn-off MVDC SSCBs are a promising solution for implementing a robust protection system in MVDC power networks.

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Chapter 7
Review of Z-Source Solid-State Circuit Breakers

Keith A. Corzine and Robert W. Ashton

1 Introduction

The Z-source dc circuit breaker can be accurately categorized as a special type of solid-state circuit breaker (SSCB). Solid-state dc breakers were developed long ago, and over the years there has been considerable research into a wide variety of circuit designs [1–9]. Several recent publications sum up a few of these circuits [3–9]. The common principal of operation is to use a bi-directional semiconductor switch in the main path between the source and load. Next, a circuit is set up to quickly detect a fault, typically an over-current. The circuit then switches the semiconductor off to isolate the faulty load from the source. Naturally, the energy built up in the source inductance will create a large voltage across the semiconductor, and so an MOV can be placed across it to clamp the voltage until the current goes to zero [3–5]. Reference [3] discusses the testing of a prototype 1 kV 1 kA dual-pole bidirectional IGBT-based SSCB. Each bidirectional pole switch contains two series connected IGBTs with antiparallel diodes. A parallel connected MOV is utilized to passively limit the peak switch voltage. The breaker control employs a time-current curve which determines the variation in trip time versus the magnitude of the fault current. Two different source inductances are exploited to assess breaker performance: a low inductance for high di/dt, and a high inductance for energy absorption capability. This breaker was primarily studied in a power hardware in-the-loop simulation to emulate a future medium-voltage solid-state circuit breaker.

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As discussed in [4], variations on the pole semiconductor switch design can include the parallel connection of reverse blocking IGCTs (RB-IGCTs) instead of series connected MOSFETs or IGBTs; this arrangement dramatically reduces on-state loss. In fact, the equivalent dual pole RB-IGCT-based breaker in [4] demonstrated a fivefold reduction in on-state power loss over equivalent series connected IGBTs. Further, this breaker's mechanical pole packages an MOV sandwiched between two hockey-puck type IGCTs. Orientation free pulsating heat pumps provide an excellent thermal path for both IGCTs and the MOV. The 1 kV 1.5 kA breaker has a voltage suppression index (VSI $= V_{\text{peak}}/V_{\text{bus}}$) of 2.1 during fault clearing permitting the use of 2.5 kV RB-IGCTs. Other devices can be placed in parallel with the switch to contain peak switch voltage during a fault. One such example is a switched MOV. For [5] the electronic MOV is only connected during a fault through the use of an SCR and a passive breakover diode (BOD). Further, the BOD acts as a gate trigger and assists the MOV during standby by increasing its maximum continuous operating voltage. For the 2 kV 500A SSCB in [5], the peak fault switch voltage is only 2.84 kV easily allowing the use of 3.3 kV IGBTs. The series MOV with axillary SCR-BOD can reduce the transient over-voltage of the main switch by more than 30% (i.e., a VSI reduction from 2.2 [4] to 1.42 [5]).

A classical method of implementing a solid-state dc breaker is to add auxiliary resonant circuit [1] in parallel with the main switch that can be activated during a fault [2]. Upon detection of a fault, the resonant circuit is activated and the resonant current, opposing the main path current, forces the main switch current to zero. This concept has been expanded with recent developments including a main path switch with stacked SiC devices to reduce losses and wireless capacitive coupling of the resonant branch [6, 7]. In [7] the authors present three single-pole unidirectional dc breakers which utilize series-parallel switch combinations constructed in symmetrical layouts to optimize current sharing. The traditional MOV and resistor-capacitor-diode snubber circuits are optimized based on thermal dissipation and snubber charge time. The two 500 V class MOSFET breakers achieve a VSI of <2.26. The 2 kV class, 3-series 3-parallel, SiC breaker has a VSI of 2.44. The estimated efficiencies range from 99.94% to 99.96%. When extrapolated to a 2-pole bidirectional equivalent, the efficiency would be greater than 99.75%. The extrapolated efficiency of the baseline single element non-parallel control-breaker is approximately 99.5%.

Some variations on the SSCB involve power converter elements. An example is the T-breaker constructed from three branches of half-bridge modules [8]. The capacitors of the arm branches can be pre-charged using the center branch, and the breaker can readily use the charged capacitor as a clamping device rather than an MOV. The T-breaker is a fault protection device with modular multilevel converter functions that is capable of series and shunt compensation similar to a flexible ac transmission system (FACTS) device on a power system. The test results for the SiC-based 1 kV 500 A prototype T-breaker in [8] demonstrated the capability to successfully interrupt a 4.5 kA (nine times rated) fault current while minimizing submodule voltage to a VSI of 1.5. The full-current on-state efficiency was tested and found to be 99.58%. Another extensive scheme that employs the use of power

converters to limit fault current is realized with the iBreaker [9]. This topology involves back-to-back buck dc/dc converters with a shared inductor. It has the added advantage of controllable breaker behavior. The iBreaker includes a variable frequency PWM current limiting state for soft-start, fault authentication and fault locating functions. Two classes of GaN wide bandgap single-pole common ground iBreakers, made form series and parallel connected devices, were tested: a 380 V 20 A (1-series 5-parallel) and 1 kV 10 A (2-series 8-parallel). Each had an on-state efficiency of 99.5%.

The primary distinction of the Z-source breaker is that it does not rely on fault detection circuitry. Instead, an incipient fault takes a high-frequency path and causes the semiconductor current to trend towards zero as the fault current is increasing. After a very short time (microsecond scale) the semiconductor current goes to zero and can remove the fault. Therefore, one advantage of the Z-source breaker is not having to implement the fault detection circuitry. Another advantage is that breaker coordination is not needed in larger systems involving multiple breakers (either upstream or in parallel). This is because the Z-source breaker nearest to the fault will rapidly switch off. Further, the source current decreases when the fault occurs preventing other breakers from tripping, and also not subjecting the source to the fault current.

The Z-source breaker does have some limitations. Compared to other SSCBs, the Z-source breaker requires passive components which lead to increased volume and mass. The classic Z-source breaker can mistake large step changes in load for a fault. However, coupled-inductor versions can be tuned for fault sensitivity as described below. The Z-source breaker also does not naturally respond to long-term arcing faults. However, intelligent arc fault detection and switch-off capability can be added as shown below.

The review below will first discuss the origin of the Z-source breaker. Inspired by the Z-source inverter [10, 11] and impedance-source circuits [12–14], the Z-source solid-state dc circuit breaker was introduced [15–17]. Popular variations on the Z-source breaker will be discussed [18–29]. More practical and more significant variations involving coupled inductors are then reviewed [30–46]. Lastly, some Z-source breakers incorporated in power converters are considered [47, 48].

2 Z-Source Breaker Concept

The original Z-source inverter concept concatenates a crossed-impedance network with a standard six-transistor inverter [10, 11]. This circuit showed some unique characteristics such as interfacing with a voltage or current source as well as buck and boost operation. Over the years, the Z-source inverter has been researched heavily and has become a well-established circuit. Further, researchers have investigated a seemingly infinite number of impedance circuits [12–14]. As an example, a number of impedance circuits are shown in Fig. 7.1.

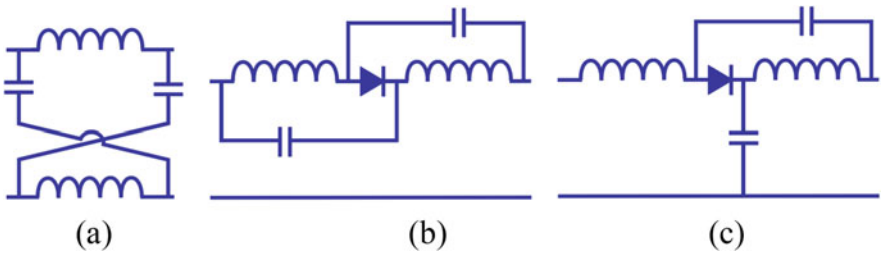

Fig. 7.1 Examples of impedance-source networks: (**a**) crossed connection, (**b**) in-line connection, (**c**) capacitor-shunt connection

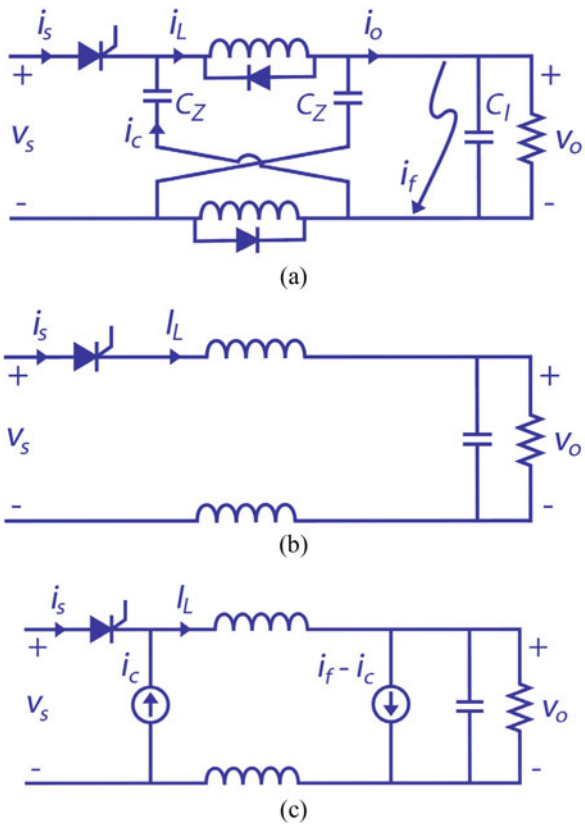

Fig. 7.2 The Z-source dc circuit breaker: (**a**) classic design, (**b**) low-frequency equivalent circuit, (**c**) high-frequency equivalent circuit at fault inception

The Z-source circuit breaker combines the Z-source circuit with an SCR thyristor. The basic circuit is shown in Fig. 7.2 [15, 16]. As can be seen, this is the impedance-source circuit from Fig. 7.1a with an SCR on the front end. The operation of the circuit is as follows. During normal operation, the dc current takes the low-frequency path shown in Fig. 7.2b. When a sudden fault occurs, the transient current takes the high-frequency path through the capacitors. Effectively,

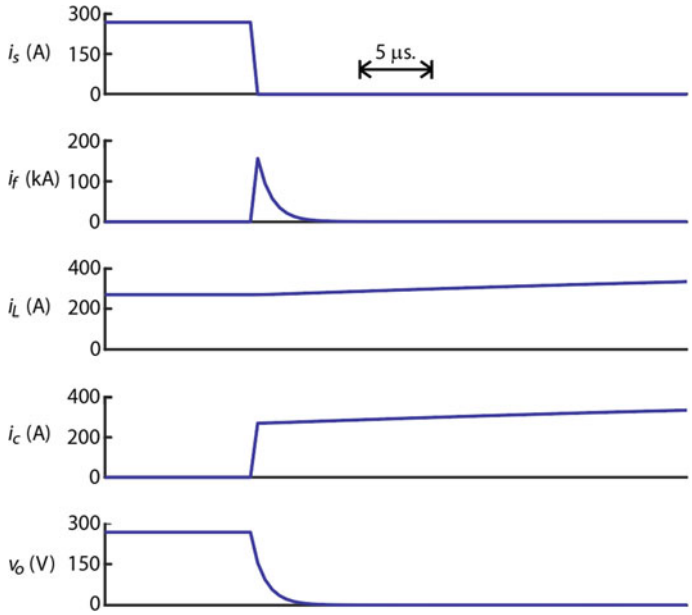

Fig. 7.3 Waveforms of the classic Z-source circuit breaker

the transient current can be represented by the current sources shown in Fig. 7.2c. With the inductor current nearly constant, the transient capacitor current i_c pushes the SCR current to zero and, assuming the SCR is not gated, it switches off.

Figure 7.3 shows the waveforms of the Z-source breaker during a fault. These are labeled correspondingly to Fig. 7.2a. The important feature of a Z-source breaker, as originally conceived, is that as the fault current rises on the output of the breaker, the source current decreases. To be more exact, the source current is driven to zero by the capacitor current which is a function of the transient fault current according to (7.1). In this topology, the source current is the SCR current, and so, in a very rapid manner, the SCR will switch off and disconnect the faulty load from the source.

$$i_c = \left(\frac{C_Z}{C_Z + 2C_1} \right) i_f \tag{7.1}$$

After the breaking operation, there is a resonance formed by the inductors and capacitors in the breaker which is stopped by the diodes placed across the inductors at which point the capacitor current goes to zero. After this, the inductor current is extinguished in milliseconds due to the power loss of the diodes.

In comparison to other solid-state circuit breakers, the Z-source breaker has an additional burden in that added passive components are needed which increases the volume and mass. Furthermore, there is a requirement of an inverter grade SCR (or fast switch) with a small turn-off time [16]. Another disadvantage is that the

Z-source breaker is not set up for long time arcing faults. However, the circuit can be modified with an auxiliary switch and arc detection circuitry as well be shown below. The classic Z-source breaker may also misconstrue a large step in load as a fault. Newer designs, described herein, are tunable so that they can handle large step changes in load.

The Z-source breaker has a number of advantages and unique features when compared to other solid-state breakers. As demonstrated in Fig. 7.3, the response to a fault is automatic, without requiring external detection and control circuitry. This yields a significant advantage in that the fault response is very rapid. Another advantage is that the source (as well as the SCR) does not experience the fault current. In fact, the source current will not go over the system rated current. Probably one of the strongest advantages is autonomous operation in a multi-breaker system. In systems involving multiple Z-source breakers, only the one nearest the fault will switch off [17].

3 Variations on the Z-Source Breaker

Although derived with alternate consideration, it seems nearly all Z-source breakers could stem from impedance source circuits [13, 14]. As an example, consider the impedance source circuit of Fig. 7.1b. By replacing the diode with an SCR, the circuit breaker topology of Fig. 7.4 is obtained [18–20]. This variation with passive components in-line, sometimes called the parallel Z-source breaker [19, 20], has the feature that the source and load have the same common ground. One disadvantage of this circuit, as seen in the waveforms in Fig. 7.5, is that the source does experience a transient surge during the fault. Although the SCR current switches off immediately, the source current briefly goes to twice the steady-state value and then resonates a bit higher until the diodes stop the resonance.

Another variation of the Z-source breaker is the topology shown in Fig. 7.6 [21–23], sometimes referred to as a series Z-source breaker [21]. This topology can also be derived from the impedance-source circuits by comparing Fig. 7.6 to Fig. 7.1c. In this structure, the source and load have a common ground, which is expected in some power systems. A further technical detail is that the voltage transfer characteristic of this circuit is that of a low-pass filter. In contrast, the classic Z-source breaker

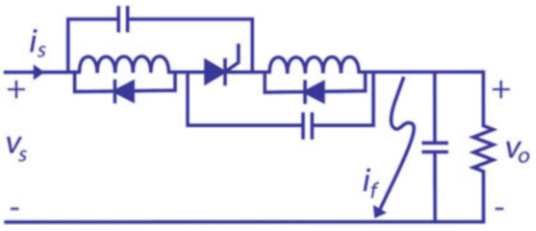

Fig. 7.4 The Z-source breaker with in-line components

Fig. 7.5 Waveforms of the "parallel" Z-source breaker with in-line components

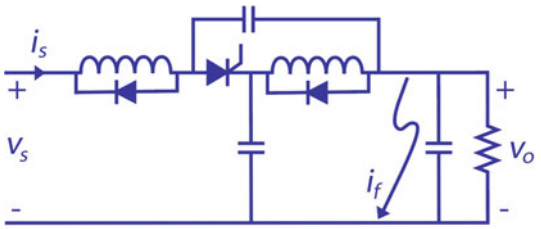

Fig. 7.6 The "series" Z-source breaker topology

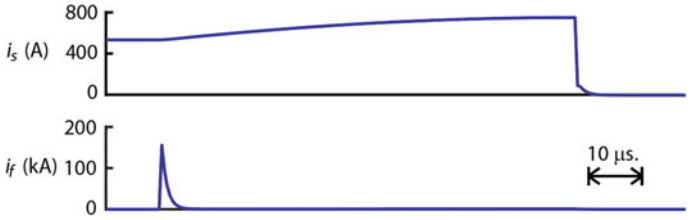

Fig. 7.7 Waveforms of the "series" Z-source breaker topology

will attenuate high frequencies but has a resonant point based on the L-C values. In many dc power systems, the low-pass characteristic is desirable.

Figure 7.7 shows the waveforms of the series Z-source breaker. One drawback of this topology is that there is a series L-C impedance connecting the source and load after the SCR switches off. This causes the source to experience the resonant current after the fault. Although not as large as the fault current, there is an uptick in current drawn from the source when a fault occurs as can be seen in Fig. 7.7.

A number of other variations on the Z-source breaker have been conceived over the years besides those mentioned above. Most notably, a number of researchers have suggested bi-directional topologies where power flow can occur in both directions [25–29]. Dc power systems may require bidirectionality to permit energy flow between various dynamic sources and loads, especially in modern-day microgrids where loads may also generate power, such as battery energy storage systems.

Figure 7.8 shows a version of the Z-source breaker which is a straightforward extension of the classic Z-source breakers with bi-directional switches on each side

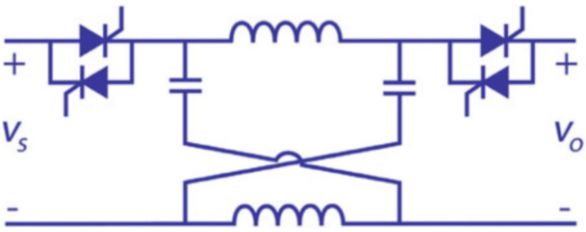

Fig. 7.8 A Z-source circuit breaker adopted for bi-directional operation

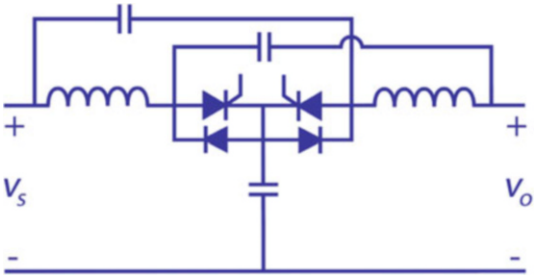

Fig. 7.9 Bi-directional Z-source breaker with in-line and shunt capacitors

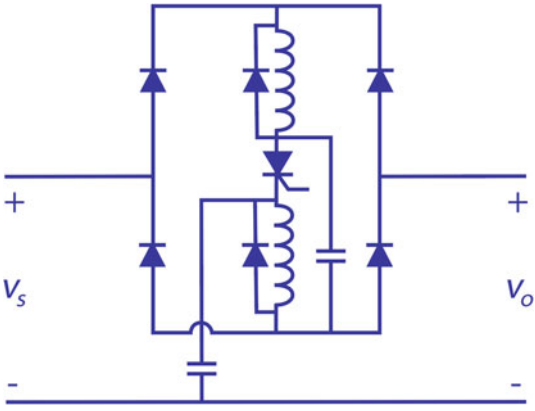

Fig. 7.10 Bi-directional Z-source breaker using a diode bridge

[25–27]. Once current is flowing in either direction, the gate signals can be removed to arm the breaker. The operation can be understood to be similar to that shown in Fig. 7.3.

Figure 7.9 shows another bi-directional variation of the Z-source breaker. The operation of this can be seen as similar to that of the breaker shown in Fig. 7.6 [27, 28]. On consideration of the circuit, it can be seen that this operation occurs with power flow in both directions.

Another bi-directional Z-source dc breaker is shown in Fig. 7.10 [29]. The four additional diodes connected to the source and load side act as a bridge rectifier. Thus, the current in the center branch will be unidirectional regardless of the overall power flow direction. Inside the bridge, the Z-source circuit operates much like that of Fig. 7.6.

4 Coupled-Inductor Z-Source Breakers

In Z-source breaker circuits, coupling of the inductors yields considerable advantages. Namely, the circuit can be reconfigured and one of the capacitors can be eliminated. This was first pointed out in [30]. As with the circuits mentioned above, Z-source breakers with coupled inductors [30–46] can be derived from the general impedance-source circuits [12, 14]. Figure 7.11 shows a general magnetically coupled impedance-source circuit [14]. Some popular variations are shown in Fig. 7.12.

First, consider the T-source dc circuit breaker [30–36] shown in Fig. 7.13. This is a clear implementation of the circuit of Fig. 7.12b with the diode replaced by an SCR. A diode is placed in anti-parallel to the capacitor which will prevent the capacitor voltage from going negative and stops the resonance after the breaker has opened. This also exemplifies another advantage of coupled-inductor Z-source

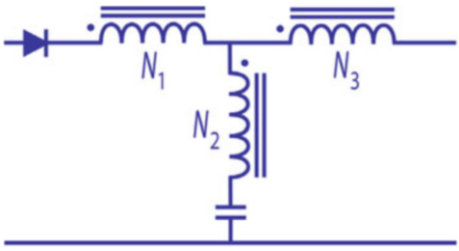

Fig. 7.11 The general magnetically coupled impedance-source circuit

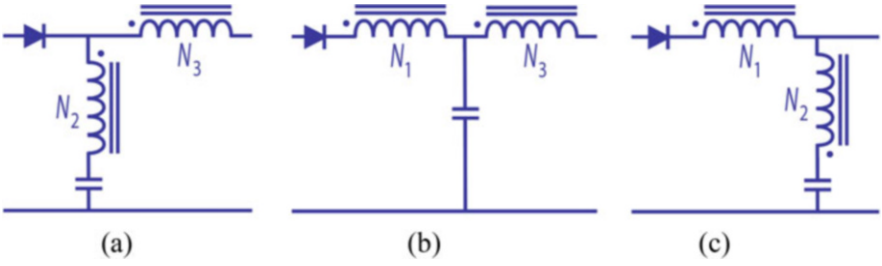

Fig. 7.12 Variations on the magnetically coupled impedance-source circuit: (**a**) the Γ-Z source network, (**b**) the T-source network, (**c**) the flipped Γ source network

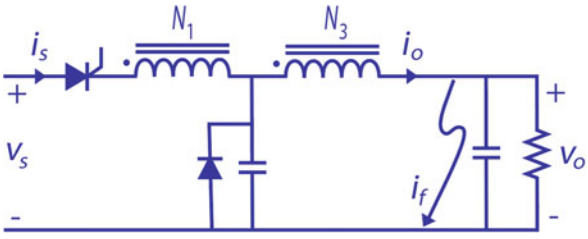

Fig. 7.13 The T-source dc circuit breaker

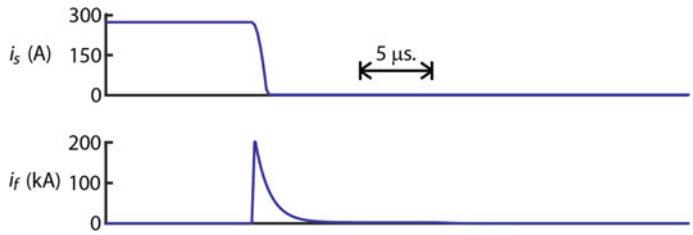

Fig. 7.14 Waveforms of the T-source dc circuit breaker

breakers over uncoupled versions in that only one diode is required. (An alternative version places the diode across one of the coupled inductors [39]).

The T-source breaker works in the following way. During normal operation, the source supplies the load through the series combination of the primary and secondary inductor windings and the SCR; the breaker capacitor is charged to the source voltage. A fault at the output causes a current to circulate in the short path involving the capacitor and secondary winding N_3. Transient current flowing into the dot terminal of the secondary causes current to flow towards the source on the primary, forcing the SCR current to zero. Figure 7.14 shows the source current and fault current for the T-source breaker.

The T-source breaker has considerable advantages over the uncoupled Z-source breaker other than requiring only one capacitor. Further, the source and load share a common ground which may be important in certain applications. The source current is the SCR current and so will trend toward zero as the fault current rises. Additionally, the voltage transfer function will filter out high-frequency noise in the dc system above a resonant frequency.

The T-source breaker has an even bigger advantage over the uncoupled Z-source breaker and that is that the performance is tunable by choosing a turns ratio between the primary and secondary windings. This allows the designer to decide how much of a step in output current would be considered a fault and how much might just be a natural load step. To simplify the analysis, consider that the coupled inductors do not have leakage inductance and that a step change in load current happens instantaneously. Let the steady-state current be I_{dc}. With a step change in load current ΔI_{o}, the breaker output current is

$$i_{\mathrm{o}} = I_{\mathrm{dc}} + \Delta I_{\mathrm{o}} \tag{7.2}$$

Then, the current at the input of the circuit breaker is

$$i_{\mathrm{s}} = I_{\mathrm{dc}} - \frac{N_3}{N_1}\Delta I_{\mathrm{o}} \tag{7.3}$$

Now, assume that the step in load is 100%; that is to say, $\Delta I_{\mathrm{o}} = I_{\mathrm{dc}}$. If the turns ratio is 1:1, the input current will go to zero according to (7.3), and the breaker will

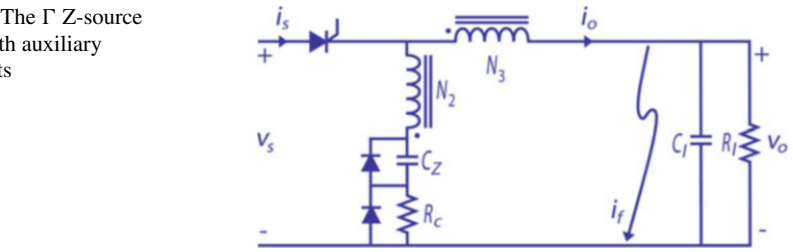

Fig. 7.15 The Γ Z-source breaker with auxiliary components

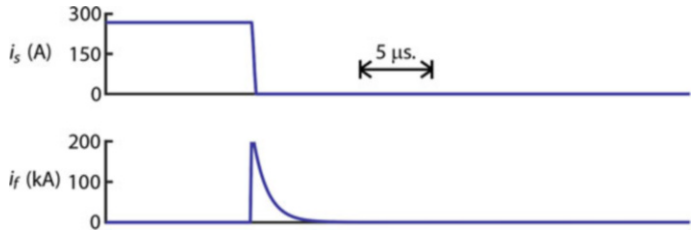

Fig. 7.16 Performance of the Γ Z-source breaker during a fault

switch off. Therefore, load changes that are below 100% will not be treated as a fault, but a load change greater than 100% will appear as a fault. This behavior is not acceptable in some applications where loads are constantly switching on and off, microgrids, for example. In fact, uncoupled Z-source circuit breakers also have this property with the exception of some specific designs [22]. With the T-source breaker, the turns ratio can be set so that the breaker will not trip when there is a large change in load (i.e., 100%, 200%, 500%, etc.). However, a fault is typically well above these settings and will still trip the T-source breaker. Another interesting application for coupled-inductor breakers is where one might want the breaker to switch off when there is a 50% step change in load (just slightly above stead-state current). This would not trip a traditional Z-source breaker, but in the coupled-inductor breaker the turns ratio could be set with $N_3/N_1 > 1$ for that to occur.

Using the circuit of Fig. 7.12a, another variation of the coupled-inductor Z-source breaker is formed: the Γ Z-source breaker [37]. An example is shown in Fig. 7.15. Therein, an added feature is introduced and that is the "soft-start" circuit. When the SCR is initially gated on, the capacitor C_Z will be charged through the charging resistor R_C. However, during a fault, the discharge path uses the diode in parallel with R_C. This feature can also be added to the T-source breaker described above.

Figure 7.16 shows the source current and fault current of the Γ Z-source breaker in response to a fault. As with the T-source breaker, the source current immediately goes to zero at the fault inception and so the performance is very similar. Considering this in more detail, researchers have noted that the output current i_o spike will be less during a fault with the Γ Z-source breaker as compared to the T-source breaker [34].

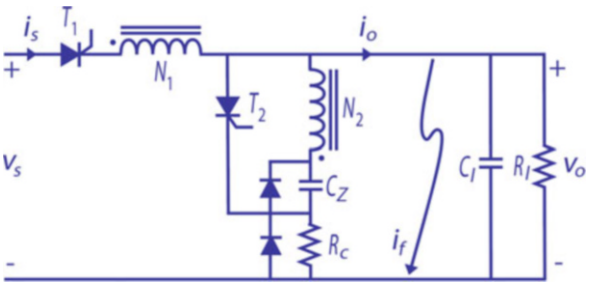

Fig. 7.17 The flipped Γ Z-source breaker with auxiliary components

Table 7.1 Parameters of the flipped Γ Z-source breaker example

$v_s = 270$ V	$L_{m1} = 100$ μH	$N_1/N_2 = 6$	$R_{l1} = 5$ Ω
$R_c = 10$ Ω	$C_Z = 100$ μF	$C_l = 0.1$ mF	$R_{l2} = 1$ Ω

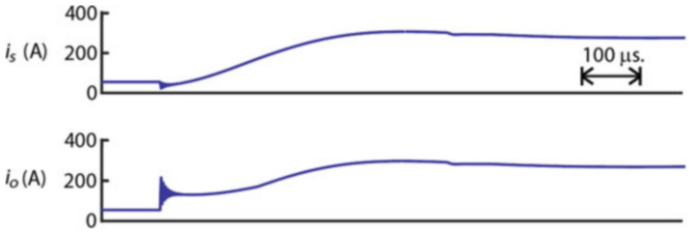

Fig. 7.18 Performance of the flipped Γ Z-source breaker during a step in load

Following the circuit in Fig. 7.12c, an example of a flipped Γ coupled-inductor dc breaker [38–41] is shown in Fig. 7.17. Therein, another feature is introduced and that is the addition of a switch-off SCR T_2. If this SCR is activated in the steady-state, the capacitor C_Z discharges into the winding N_2 causing T_1 to switch off. Therefore, T_1 and T_2 can be used to switch the circuit on and off. This added switch introduces an important feature to the breaker. By monitoring the current i_o, long-term faults with low di/dt (such as arcing faults) can be detected and the breaker can be switched off via T_2. For the flipped Γ breaker, this has been demonstrated where an arcing fault was identified using a short-time Fourier transform and a clustering algorithm [40]. This setup protects dc systems with both low di/dt and rapid-inception faults. As with the Γ Z-source breaker, the flipped Γ Z-source breaker has an advantage over the T-source breaker in that the steady-state current only flows in one winding which reduces steady-state power losses a bit.

To illustrate the operation with a numerical example, the system parameters shown in Table 7.1 are to be used. The two load resistance values represent a light load of 5 Ω switching to a heavy load of 1 Ω.

Figures 7.18 and 7.19 show two operating modes of the flipped Γ Z-source breaker. In Fig. 7.18, the circuit is initially operating in the steady-state with the source supplying power to the light load. The load is suddenly changed to the heavy load. From the parameters of Table 7.1, the load current will step from 54 to 270 A

Fig. 7.19 Performance of the flipped Γ Z-source breaker during a fault

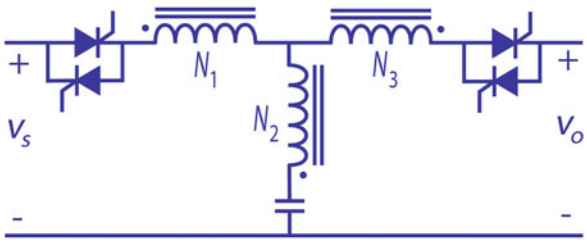

Fig. 7.20 Topology of the Y-source dc breaker

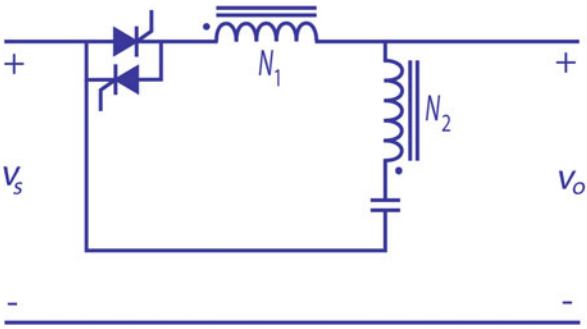

Fig. 7.21 Topology of the O-Z-source dc breaker

during this change. According to (7.3), the step change in load will not switch off the SCR. The source current in Fig. 7.18 initially decreases as the load steps but not enough to switch the breaker off. Then, the source current then increases to match the output current.

Figure 7.19 shows the response of the flipped Γ Z-source breaker to a fault, where the SCR switches off. As with the T-source and classic Z-source breaker, the source current simply and rapidly goes to zero, starving the SCR of current and disconnecting the source from the fault.

There are a myriad of other types of Z-source breakers based on coupled inductors. An interesting type is the Y-source breaker [42, 43] which uses a three-winding transformer as shown in the fundamental circuit of Fig. 7.11 and is shown in Fig. 7.20. This type of breaker also has bi-directional capability. Other novel topologies such as the O-Z-Source breaker [44] of Fig. 7.21 and Q-Z-Source breaker [45] of Fig. 7.22 can be seen as derivatives of the flipped Γ and T-source breaker, respectively, with the capacitor connection attached to the positive terminal of the

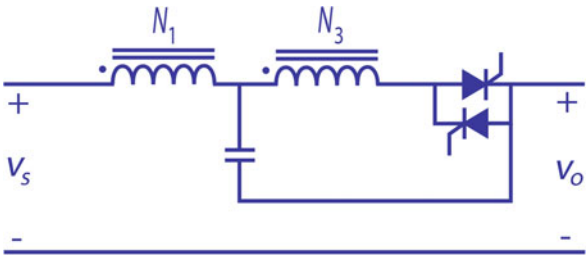

Fig. 7.22 Topology of the Q-Z-source dc breaker

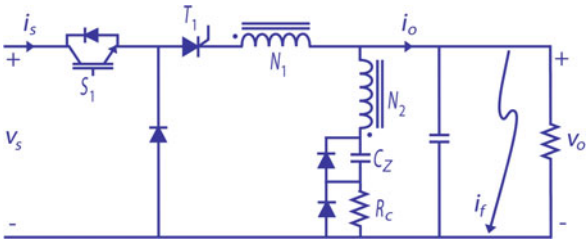

Fig. 7.23 Integration of the Z-source breaker into a buck converter

load instead of the system ground. The capacitor connection of the T-source breaker can also be attached to the positive terminal of the source as another variation [46] which would look like a flipped version of the entire circuit of Fig. 7.22. Due to space limitations, these circuits are not described herein, but the interested reader is directed to the literature on coupled inductor breakers which have been growing in numbers in recent years [42–46].

5 Integrating Z-Source Breakers into Power Converters

The Z-source dc breaker has also been incorporated into dc/dc power converters. Two examples of this will be considered herein. First, Fig. 7.23 shows the flipped Γ Z-source breaker built into a standard buck dc/dc converter [47]. From the left, the typical buck converter switch S_1 and freewheeling diode are seen. This is followed by the SCR T_1 and components of the flipped Γ Z-source breaker. In this converter, the magnetizing inductance of the coupled inductor takes the place of the inductance in the buck converter. The output of the buck converter contains a capacitance as usual.

Table 7.2 shows the parameters used for a detailed simulation of the circuit of Fig. 7.23. In this example, a 270 V load is being supplied from a 600 V source, and so the duty cycle of the transistor switch is set accordingly. Figure 7.24 shows the simulation results. The source is supplying the load in steady-state when a fault occurs. From the inductor current, it appears the buck converter is in normal continuous conduction mode operation before the fault. This is the case except for the small perturbations in the secondary current that happen at the onset of the switch off state due to the leakage reactance of the coupled inductor and C_Z.

Table 7.2 Parameters used in the dc/dc converter examples

$v_o = 270$ V	$L_{m1} = 100$ μH	$N_1/N_2 = 6$	$f_{sw} = 20$ kHz
$R_c = 10$ Ω	$C_Z = 100$ μF	$C_l = 1$ mF	$R_l = 1$ Ω

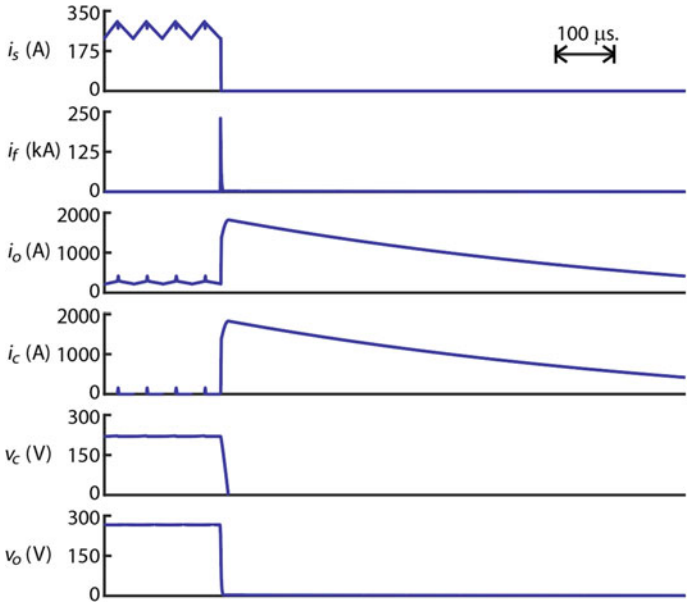

Fig. 7.24 Performance of the buck converter with integrated Z-source breaker

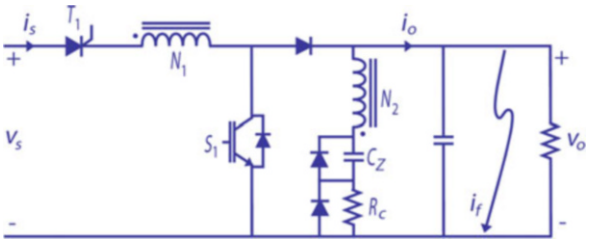

Fig. 7.25 Integration of the Z-source breaker into a boost converter

However, these can barely be seen in the source current waveform. When a fault occurs, the discharge of capacitor C_Z through the secondary winding N_2 produces the expected result and the SCR switches off.

The next example is shown in Fig. 7.25. It is the flipped Γ Z-source breaker integrated into a standard boost dc/dc converter [48]. From the left, at the front end, the SCR is located in series with the primary winding of the transformer. As with the previous example, the magnetizing inductance of this transformer will be used as an energy conversion element in the converter. The transistor switch and freewheeling diode are seen in their expected configuration. The secondary winding is now located on the output of the boost converter.

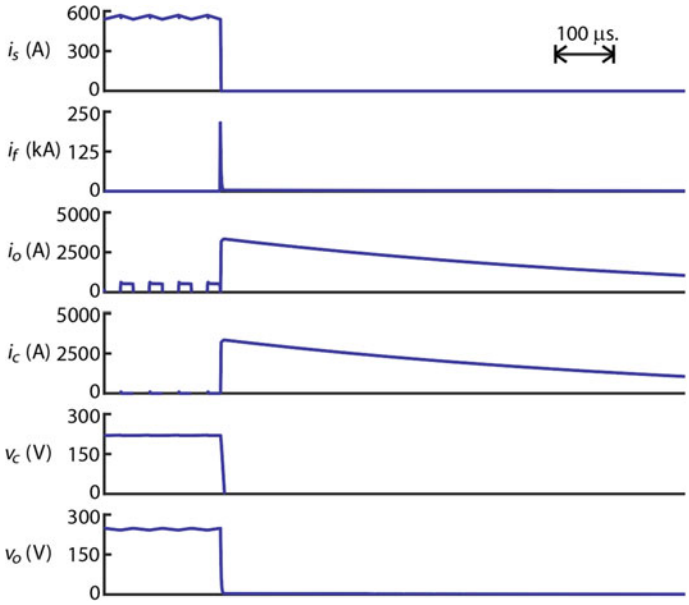

Fig. 7.26 Performance of the boost converter with integrated Z-source breaker

The parameters in this example are shown in Table 7.2. In this case, a 120 V source supplies a 270 V load, and the boost converter duty cycle is set accordingly. Figure 7.26 shows the converter operation. When a fault occurs, the capacitor C_Z discharges through the secondary winding N_2 causing a current which is reflected in the primary to switch the SCR off. The output current continues after the output voltage drops due to the magnetizing current of coupled inductors. However, this is extinguished quickly by the voltage drop across the diodes in parallel with R_C and C_Z.

6 Concluding Remarks

Like a traditional mechanical breaker, an SSCB is expected to respond to a fault and mitigate the affected circuit branch. This chapter first presented an overview of a number of dc SSCB arrangements. The many different SSCB configurations generally optimize one or more important attributes desired for a particular system. These attributes may include (1) cost, (2) time-current curve programmability, (3) functionality (i.e., multistate operation), (4) voltage and/or current suppression requirements, and (5) bidirectionality for energy flow between various dynamic sources and loads. The SSCB may be based on MOV protected semiconductor switches, more complex energy suppression MOVs and snubbers, or converter-

based multifunctional constructs. In general nearly all SSCB circuits rely on fault sensing and detection to actively open the main semiconductor switch path. However, the primary focus of this chapter is the Z-source breaker where fault sensing is not necessary, since passive pass-element commutation occurs "automatically" during a load fault transient. The Z-breaker concept began with the combination of the "zigzag" Z-source circuit in conjunction with a source-side SCR. This implies for most variations that the source current actually decreases as fault current rises. A number of variations of the Z-breaker concept are presented along with perceived advantages and disadvantages. For instance, the series and parallel Z-source breaker configurations have a common ground but unfortunately permit source transient current during a fault. However, a variety of coupled inductor arrangements do provide clear improvements over their uncoupled cousins: (1) common ground, (2) elimination of one capacitor and one diode, (3) tunable performance via the inductor turns ratio, and (4) high frequency filtering of the source. This chapter includes a coupled inductor Z-source breaker design example as well as suggestions on breaker system integration. Numerical examples of Z-source breakers integrated into buck and boost choppers are also presented.

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Chapter 8
Medium Voltage High Power Density Solid-State Circuit Breaker for Aviation Applications

Di Zhang

1 Introduction

Hybrid electric propulsion is a promising solution to improving fuel burn efficiency and reducing carbon emission for aviation applications in the near future [1]. The power rating of the electrical power system to support hybrid electric propulsion is in the range of megawatts (MW) to tens of MW. Thus, to reduce the total weight of the electric power system, especially the cable weight, the medium voltage direct current (MVDC) system is selected due to its numerous advantages compared with the traditional alternating current (AC) system [2].

As in other MVDC applications, hybrid electric propulsion needs protection devices to handle the system short circuit fault. Although the mechanical breaker and hybrid circuit breaker have such benefits as low conduction loss, the solid-state circuit breaker (SSCB) is more desirable mainly due to its superfast response, arc free operation, and simple structure [3].

SSCB is not a fundamentally new technology. The traditional SSCB design mainly consists of the semiconductor switches, voltage clamping circuit (VCC), and the fault current limiting device. The semiconductor switch carries load current in the normal operation condition and generates most of the losses. After the occurrence of system short circuit fault, the fault current limiting devices together with system parasitic inductance limit the fault current ramping speed. Then, the semiconductor switches are turned off to commutate the fault current to the voltage clamping circuit, which typically involves metal oxide varistor (MOV). The voltage clamping circuit can clamp the voltage across SSCB to a level higher than the system

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dc bus voltage, which drives the system current down and eventually clears the fault in as short as tens of microseconds.

Many works have been done in this area to improve SSCB's performance [3]. However, compared with the SSCB in other applications, the aviation applications introduce certain unique design challenges as follows, which require different design principles and technical solutions.

The first design challenge is extremely high specific power. As is well known, the weight is critical for any components on aircrafts. Especially for hybrid electric propulsion, any electrical component in the power system means extra weight compared with the traditional airplane architecture. In fact, the hybrid electric propulsion concept only becomes practical when its fuel burn reduction benefits outweigh its fuel burn penalty due to the additional weight and power loss of power system. For example, a 100 kW/kg specific power is targeted for SSCB to make the hybrid electric propulsion feasible for aviation applications [4]. It should be noted that the MVDC system is flight critical, so such system must be able to operate continuously at full power with single point ground fault. To achieve this goal, one SSCB is needed in each dc pole. In other words, the SSCB's specific power target is 200 kW/kg each.

The second design challenge is high efficiency. For the same reason mentioned above, any power loss in the electrical component means additional fuel burn penalty, which can jeopardize the feasibility of the hybrid electric propulsion concept. In addition, such power loss also means extra weight penalty related to the thermal management system. Especially for power electronics devices-based components, including SSCB, the maximum device junction temperature is much lower compared with the electric motors and combustion engines. So the coolant temperature for power electronic devices must also be reduced accordingly. This will further bring down the efficacy of the heat exchanger, leading to an even heavier thermal management system. Other than that, an inefficient external heat exchanger will also increase the drag of the aircraft, causing more fuel burn penalty at system level. In this design, the total efficiency target is 99.5% minimum, or 99.75% for each SSCB.

The third design challenge is insulation capability at high altitude. Not like the low power aviation applications, such as drones or e-taxi, hybrid electric propulsion is designed to improve fuel burn efficiency and reduce carbon emission for commercial airplanes whose common cruising altitude can be as high as 51 k ft. At such high altitude, the creepage and the clearance distance required to withstand the same voltage is much higher compared with at sea level. And the partial discharge initial voltage (PDIV) or extinct voltage (PDEV) will also drop significantly. Although theoretically, such electric power system can be installed in a pressurized environment to emulate the sea level pressure condition, it will certainly add undesirable system complexity and weight. And more importantly, this means the system cannot continue working if the aircraft lost the pressure in the worst cases. Thus, it is prudent to design the components with the capability of running at high altitude under unpressurized conditions.

The last but not the least design challenge is reliability. Unfortunately, as an emerging application, there are no existing standards or design targets for SSCB's reliability, such as FIT or MTBF number. But, in principle, SSCBs, as the protection devices for the MVDC system, must be much more reliable than the other electrical components in hybrid electric propulsion systems.

To address these challenges, a few design principles are kept in mind including fewer components, simple and non-compact mechanical layout, and leveraging proven technologies as much as possible.

Fewer components mean lower component weight, volume, loss, and failure probability. This is the key to achieve the extremely high specific power, high efficiency, and good reliability. But the traditional SSCB's structure is already very simple. The key question would be how to further reduce the number of components without sacrificing the critical functions and design margins as in the traditional SSCBs.

Simple and non-compact mechanical structure can help mitigate the insulation design challenges. However, this also means higher parasitic inductance in the SSCBs, which are not welcomed in electrical design aspects. How to accommodate such high parasitic inductance is one of the most critical issues in electrical design procedures.

Mature and proven technology is great for system reliability, but it also means limited design options. For example, Si IGBT is mature for aviation applications, but without the new wide band gap devices, it is very challenging to meet the efficiency target.

With all these design principles implemented, a novel SSCB structure is proposed for aviation hybrid electric propulsion, and the benefits are presented with a 2 kV 1.2 kA solid-state circuit breaker prototype sponsored by NASA. This chapter is organized as follows: Section 2 explains the operation principle of the proposed SSCB. Sections 3 and 4 illustrate two key innovations compared with traditional design, the fault current limiting scheme, and voltage clamping circuit. Section 5 emphasizes the importance on insulation design and testing, followed by hardware experimental results in Sect. 6.

2 Operation Principle

The topology of the proposed SSCB is depicted in Fig. 8.1. Compared with the traditional SSCB design, the proposed design eliminates the fault current limiting inductor and adds two antiparallel silicon-controlled rectifier (SCR)s in series with the MOV.

In hybrid electric propulsion, the battery can be the main or auxiliary source, and rectifiers' dc capacitors can be connected to the dc bus directly, so the breaker is connected directly to a low-impedance source and the breaker design cannot depend on the assumption that a high system impedance is always present to limit the fault current. With the current limiting inductor eliminated, the 200 kW/kg specific power

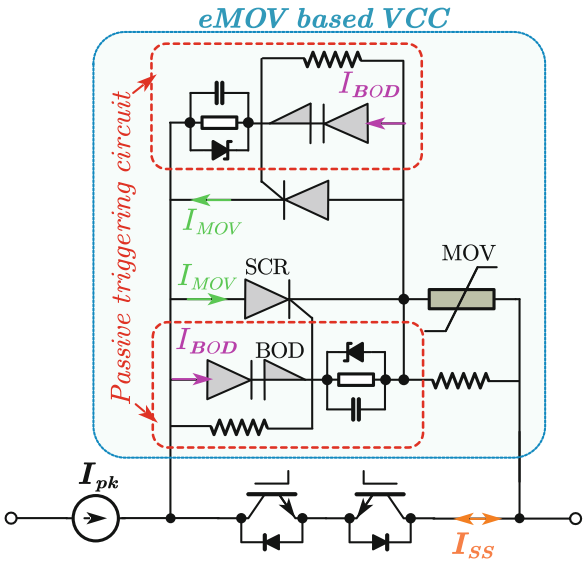


Fig. 8.1 Topology of a proposed SSCB for hybrid electric propulsion application

for each SSCB becomes feasible. The key function of the fault current limiting inductor in the traditional design is achieved by the Si IGBTs' current saturation characteristics with reduced gate voltage.

The inserted SCRs can share steady-state dc voltage with the MOV, so a lower voltage rating MOV can be used. This can reduce the peak clamping voltage of SSCB, enabling the usage of Si IGBTs with lower voltage rating. Thus, the conduction loss of the main semiconductor devices can be minimized to meet the 99.75% efficiency target with mature Si IGBT devices. The SCR itself is a mature technology, which are triggered only with circuits consisting a few highly reliable passive components, such as diodes, resistors, and capacitors.

The recently developed wide band gap devices, such as the Silicon Carbide (SiC) MOSFETs, have higher current density and lower conduction loss compared with Si IGBTs. Once the new devices become mature enough for aviation application and gain the capability with lower saturation current level, the proposed design can certainly use the advanced devices to further improve SSCB's efficiency and power density.

One thing that cannot be seen from Fig. 8.1 is that the main semiconductor switches are turned off in a much slower or "softer" manner compared with the traditional SSCB design. In the traditional SSCB, since the peak fault current is determined by the fault current limiting inductor and the total response time, to minimize the inductance value, a fast turn-off action is preferred. However, in the proposed design, the peak fault current is limited in a different principle which is independent of the system impedance and the SSCB's response time. Thus, the turn-off time can be extended by a few times compared with the traditional design. As a result, the fault current can be commutated from the Si IGBTs to the

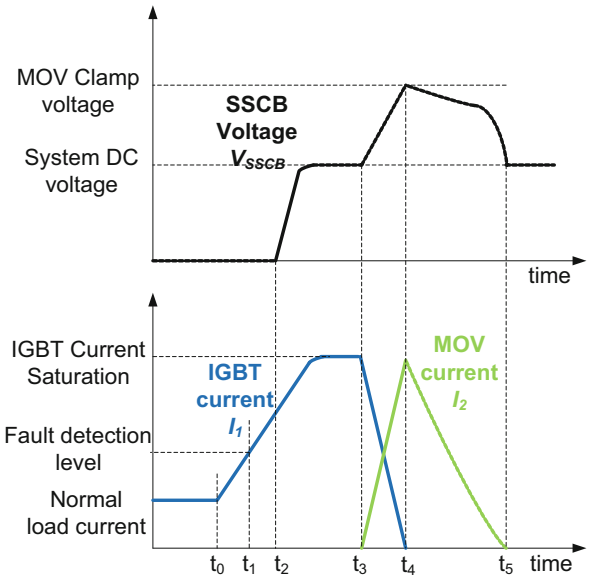


Fig. 8.2 Typical switching waveforms of the proposed SSCB

MOVs relatively slowly, which mitigates the impact of parasitic inductance inside SSCBs. And the internal mechanical layout of SSCB components can be optimized to achieve high power density and larger geometry distance to reduce local electric field intensity for better insulation capability.

The typical switching waveforms of the proposed SSCB are shown in Fig. 8.2. The top figure in Fig. 8.2 shows the waveform of the voltage across the SSCB, and the bottom figure shows the waveforms of the current flowing through the IGBT and MOV. Before t_0, the system is under normal operation, the voltage across the SSCB (V_{SSCB}) is close to zero, and the system current only flows through the IGBT. At t_0, a short circuit fault occurs, and the IGBT current (I_1) starts to increase. Without the current limiting inductor, the system fault current rising speed is very high. Like the case with the traditional design, the fault current is detected at t_1, and after t_{d}, the IGBT is turned off at t_4. After the fault current is commutated to MOV, the MOV's clamping voltage is higher than the dc bus voltage. Thus, after t_4, the MOV's clamping voltage will drive the current down and eventually clear the fault at t_5.

In the traditional SSCB, the IGBT always operates in saturation region. The voltage drop across the IGBT is only a few volts, and the fault current continues increasing until it is commutated to the MOV. Thus, the peak fault current is determined by both the fault current ramping speed and SSCB's response time.

However, in the proposed SSCB, when the system fault current is high enough between t_1 and t_3, the IGBT exits the saturation region and enters the active region around t_2. Consequently, the voltage across the IGBT increases rapidly together with the system fault current until it reaches the system dc voltage level as shown in Fig. 8.2. At this moment, the voltage drop across the system inductance is zero, so the system fault current will stop increasing or be clamped at the IGBT saturation

current level until the IGBT is turned off. In this process, the IGBT replicates the same current limiting function without a current limiting inductor.

3 Fault Current Limiting Scheme

One key benefit of the proposed SSCB is its high specific power, which is undoubtedly critical for aviation applications, due to the elimination of current limiting inductors.

In the traditional SSCB, the rising speed of fault current is determined by the dc bus voltage (V_{dc}) and the total value of system inductance (L_{sys}) and current limiting inductor (L_{CB}) as in Eq. (8.1).

$$\frac{di}{dt} = \frac{V_{dc}}{L_{sys} + L_{CB}} \tag{8.1}$$

As illustrated in Fig. 8.2, once the fault current exceeds the predefined protection threshold (I_{th}) at t_1, the fault protection scheme is activated. After that, the fault current will keep increasing until the IGBT is turned off at t_3 and the fault current is fully commutated from IGBT to MOV around t_4. The time difference between t_1 and t_4 is called the response time t_d, which includes the process time of the control circuit to generate the turn-off command and the time to fully turn off the IGBT.

If fault current can continuously increase in t_d, the peak fault current can be estimated as

$$I_{pk} = I_{th} + \frac{V_{dc}}{L_{sys} + L_{CB}} t_d \tag{8.2}$$

Based on (8.2), if L_{sys} is close to zero in the worst case, a current limiting inductor must be installed to limit *di/dt*, so that the peak current will not exceed the maximum value within t_d. Although a lower I_{th} and t_d can help to limit the fault current, which means the protection system needs to respond earlier and faster, their impact is limited if the system current rising speed is very high. In addition, a lower I_{th} or t_d could make the SSCB sensitive to the system noise, especially in a harsh EMI environment, such as the converter-based high power system.

To meet the 200 kW/kg specific power target, the weight of each 2 kV 1.2kA SSCB is only 12 kg. In this design, the peak fault current is limited to 5000A, and the fault detection level is designed to be 2000A.

If the response time (t_d) is selected to be 1.5 μs and no system inductance exists, to achieve this goal, the value of one current limiting inductor can be calculated as

$$L_{CB} = \frac{V_{dc} t_d}{\Delta i} = \frac{2000\ \text{V} \times 1.5\ \mu\text{s}}{(5000 - 2000)\ \text{A}} = 1\ \mu\text{H} \tag{8.3}$$

Such a 1 μH inductor needs to carry 1200 A current continuously and to handle a transient current of 5 kA without significant core saturation. Without a detailed inductor design, the weight of such a 1 μH inductor can be estimated based on the existing design with similar current ratings. As reported in [5], a 1.5 μH 430 A inductor weighs 3.3 kg so the energy density is 42 kJ/kg. With a similar energy density, such 1 μH 1200 A inductor weighs about 17 kg, without even considering the requirement to handle the peak transient current. With a much larger core size to handle the peak current, it would be no surprise if the actual weight of the inductor is higher than 20 kg.

With an optimized design, the inductor weight could be lighter than the estimated value. But with the traditional current limiting inductor, it is obviously impractical to meet the 12 kg weight or 200 kW/kg specific power target.

As is well known, the IGBT normally operates in the saturation region when the load current is within its rated range, and the voltage drop across the device usually is only a few volts. However, once the current is sufficiently high, IGBT will exit the saturation region and enter the active region. Consequently, the IGBT terminal voltage will increase dramatically with the load current, until the load current reaches the IGBT saturation current level. In other words, the system current is only determined by the IGBT's saturation current level, and the IGBT acts similar to an ideal current source. To maintain the saturation current level, IGBT can adapt its terminal voltage automatically until there is no net voltage to drive the system current up or down, like an active current limiter. For any specific IGBT, its saturation current level is mainly determined by the gate voltage and device temperature.

In the example SSCB design, to carry 1.2 kA continuously, block 2 kV dc, and meet the efficiency target of 99.75%, the 3.3 kV 1500 A FZ1500R33HL3 module is selected. As recommended by most of the device vendors, a 15 V gate voltage is typically used as the gate drive voltage to strike a good balance between the device conduction loss and gate voltage safety margin. With 15 V gate voltage, the IGBT saturation current level is 6.4 kA at 150 °C junction temperature [6]. At lower junction temperature, the saturation current level is even higher, which cannot meet the 5000 A peak current requirement.

With 12 V gate voltage and 25 °C die temperature, the IGBT starts to enter active region when carrying 3 kA and the IGBT terminal voltage (V_{ce}) increases to 20 V correspondingly. This is shown as the moment of t_2 in Fig. 8.2. The IGBT can enter active region when carrying only 2.5 kA if the die temperature is increased to 125 °C [6]. The datasheet doesn't provide the saturation currents with different gate voltages. Thus, tests are conducted to measure the saturation currents at different gate voltages at room temperature. Based on the test results, 12 V is selected in the example design.

With the new fault current limiting scheme, the gate voltage is reduced to 12 V. This unsurprisingly will increase the IGBT conduction loss. However, as indicated in Fig. 8.3, in which the *VI* curve of the IGBT module with different gate voltages are compared, when carrying 1200 A the typical voltage drop is 2.8 V with 15 V gate voltage and 3.1 V with 12 V gate voltage, resulting in a voltage difference of

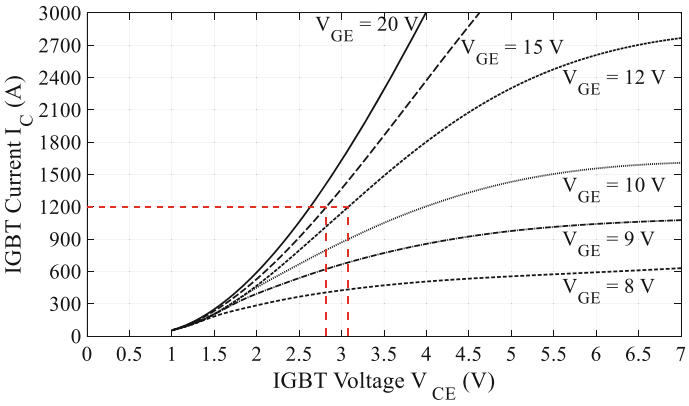


Fig. 8.3 *VI* curve of FZ1500R33HE3 with different gate voltages at 150 °C junction temperature

0.3 V. In other words, the reduction of gate voltage from 15 V to 12 V introduces an additional power loss of 360 W per IGBT. The impact on the overall SSCB efficiency is only 0.03% in the 2.4 MW system.

A 0.03% efficiency loss in the semiconductor devices is negligible especially considering that the power loss in the current limiting inductor is eliminated in the proposed solution. In addition, the data in Fig. 8.3 is for 150 °C junction temperature. Since the device junction temperature is lower under normal operation, the additional loss is even lower.

One potential risk related to this current limiting scheme is the high junction temperature.

With the rated gate voltage, e.g., 15 V, the typical IGBT saturation current level is around 5 times of its rated current, and the IGBT can only carry such current for a very short time, e.g., 10 μs. During this short period of time, the IGBT blocks full dc voltage and carries high current simultaneously. In the example design, each IGBT can carry 5 kA and block 2 kV at the same time, leading to a 10 MW power loss. Such a high-power loss can transiently increase the IGBT's die temperature. Although the IGBT module's reliability is typically related to thermal stress quantified as temperature swings occurring in the semiconductor dies and the power module structure, the temperature surge caused by the proposed solution can also potentially impact the device lifetime and reliability.

In the proposed SSCB, this issue is mitigated with lower gate voltage and shorter duration time. With 12 V gate voltage, the short circuit current is reduced by roughly 30% compared with the typical case with 15 V gate voltage, and the duration is limited to be less than 10 μs, e.g., around 5 μs. In addition, the IGBT only blocks up to 2 kV instead of 2.5 kV, and the junction temperature is much lower than 150 °C as specified in the short circuit test condition in [6]. Therefore, the total accumulated loss is reduced to be less than 50% of the worst case listed on the datasheet with additional junction temperature margin. If both SSCBs operate identically, each

SSCB only needs to block half of the dc link voltage so the power loss can be further reduced by half.

There is no systematic study on the negative impact of simultaneous high voltage and high current, or high power dissipation, on device reliability. More analysis and experimental evaluation are needed to quantify the impact.

For the proposed SSCB, the worst case is when there are two system ground faults with one SSCB bypassed. This is a very rare case in the operation lifetime of SSCB. In most cases, the SSCB only needs to cut normal current with the IGBT not in active mode. Due to the low probability of worst case scenario, its negative impact on the overall reliability of SSCB is very limited. By the time this chapter is prepared, the same IGBT module has been tested in this condition for more than 100 times. No failure or performance degradation has been observed, which can partially support the conclusion. Even though the operation of IGBT in this mode reduces the lifetime of the SSCB, as long as such negative impact can be quantified, the SSCB can always be replaced after a certain number of operations. Considering its benefits, the proposed method still is a practical and advantageous solution.

4 Peak Voltage Clamping Scheme

As demonstrated in Fig. 8.2 after the IGBT is turned off, the system current is commutated from the IGBT to the MOV between t_3 and t_4. As in any converter power stage, there is parasitic inductance in the commutation loop between the IGBT and the MOV as shown in Fig. 8.4.

In Fig. 8.4, the current flows from left to right, and the left IGBT needs to be turned off. The commutation loop parasitic inductance is represented as L_{cir}. Such parasitic inductance cannot be eliminated, and its value is mainly determined by the mechanical layout. When the system fault current is commutated from the IGBT to the MOV, a transient voltage is generated due to high *di/dt*. Such a transient voltage together with the clamping voltage across the MOV determines the maximum voltage across the IGBT, which can be estimated as

$$V_{\text{peak}} = V_{\text{clamp}} + L_{\text{cir}} \frac{di}{dt} \tag{8.4}$$

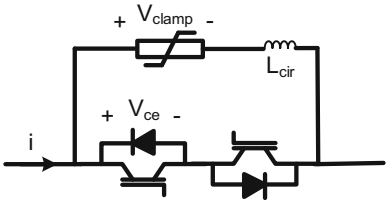


Fig. 8.4 Commutation loop between IGBT and MOV

where L_{cir} is the commutation loop inductance and V_{clamp} is the MOV's clamping voltage when carrying the fault current.

It is critical to limit such voltage below IGBT's maximum voltage rating to avoid IGBT damage. A IGBT with higher voltage rating can be used to meet such requirement. However, a higher voltage rating IGBT generally has higher conduction loss. For example, with the same mechanical package dimension, FZ1500R33HL3, a 3.3 kV IGBT module, generates 3.2 kW loss when carrying 1.2kA current; FZ1200R45KL3, a 4.5 kV IGBT module, generates 3.8 kW loss; and FZ750R65KE3, a 6.5 kV IGBT module, generates 5.5 kW. All of these modules are built by the same vendor with similar semiconductor technologies and mechanical dimensions. For higher SSCB efficiency, it is desirable to use the 3.3 kV IGBT, if the peak voltage is below 3.3 kV with sufficient margin.

From (8.4), to reduce the transient voltage, either the current is commuted with a slower speed, or the mechanical structure needs to be optimized to minimize the parasitic inductance. As mentioned above, to limit the peak fault current below 5 kA with 1 μH inductance, the response time needs to be 1.5 μs or lower, which includes the fault detection time and IGBT turn-off time. Thus, the IGBT needs to be turned off in less than 1 μs and the corresponding *di/dt* is higher than 5 kA/μs. In other words, to limit the transient below 500 V, the parasitic inductance needs to be below 100 nH.

Such low parasitic inductance can be realized with a compact mechanical layout and/or laminated busbars, which works for most applications at sea level. However, these methods can introduce significant challenges for aviation applications. First of all, a compact mechanical layout and laminated busbar will introduce insulation challenges, such as partial discharge (PD), and require special design for high altitude operation [7, 8]. If additional encapsulation material is used to enhance the insulation performance, the weight of SSCB will increase, leading to a lower power density. And the laminated busbar can be much heavier than regular busbar, because the current paths are not fully controlled and not all the conductor material can be fully leveraged to carry current evenly.

With the proposed SSCB solution, the peak current is limited to IGBT's saturation current level independent of the fault response time. Thus, it is safe to apply a fault response time much longer than 1.5 μs, so the IGBT can be turned off in a much slower manner. For example, if the turn-off time is increased to 4 μs, the parasitic inductance can be increased to 400 nH while still limiting the transient voltage below 500 V. This can provide tremendous design freedom for mechanical layout. And the component layout can be optimized for easier assembly and higher clearance to handle insulation challenges at high altitude other than lower parasitic inductance. In addition, non-laminated busbar with special shapes can be used to accommodate the mechanical layout for volume and weight reduction.

With the transient voltage limited, the next key challenge is how to reduce the MOV's clamp voltage.

The MOV is a highly nonlinear device whose typical *I-V* characteristics are as shown in Fig. 8.5 [9]. In the standby region, it presents as a large resistor (10^9–10^6 Ω) with low leakage currents (μA) exhibiting a negative temperature coefficient.

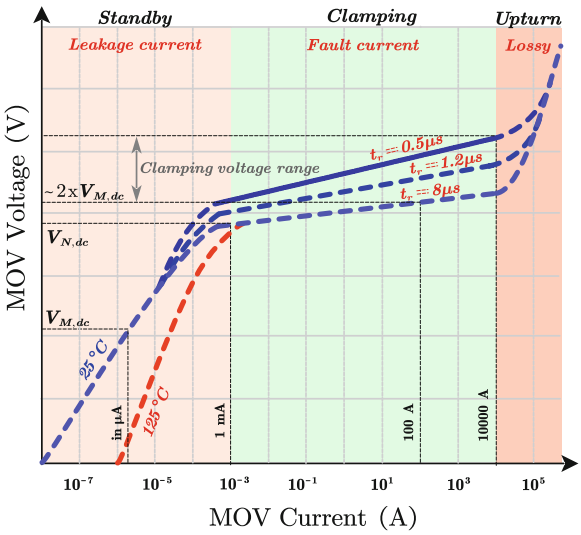


Fig. 8.5 *I-V* characteristics of MOV

In contrast to its high transient energy rating, the continuous power rating is very low (typically <1 W). Therefore, the steady-state working voltage of the MOV must be below its maximum continuous dc operation voltage ($V_{M,dc}$).

In the clamping range, as shown in Fig. 8.5, the MOV's *IV* curve can be approximated as for any two operation conditions (V_1, I_1) and (V_2, I_2)

$$R_\alpha = \frac{\log(V_2) - \log(V_1)}{\log(I_2) - \log(I_1)} \tag{8.5}$$

So the peak clamp voltage can be estimated as

$$\log\left(V_{MOV\_pk}\right) = \log(V_{dc}) + R_\alpha\left(\log\left(I_{pk}\right) - \log\left(I_{\_V_{dc}}\right)\right) \tag{8.6}$$

where I_{pk} is the peak fault current and I_{-Vdc} is the current flowing though MOV when it is blocking V_{dc}. In the traditional design, when MOV is connected in parallel with semiconductor switches, $I_{\_Vdc}$ is much less than 1 mA, and its peak voltage (V_{pk}) is typically between *2*× and *3*× $V_{M,dc}$ depending on the current magnitude.

For the example SSCB design, V172BB60 MOV can block up to 2150 V dc continuously, and the *VI* curve of V172BB60 MOV is listed in Fig. 8.6.

From Fig. 8.6, such MOV's clamping voltage when carrying 5 kA is 5000 V. So the ratio between peak clamping voltage and continuously dc blocking voltage is 2.32.

Based on (8.4), a 6.5 kV IGBT must be used, therefore leading to much higher conduction loss compared with the case with only 3.3 kV IGBTs.

It is to be noted that faster current rise times (denoted as t_r) introduce an "overshoot effect" increasing the maximum V_{pk} (up to 30% higher for $t_r = 0.5$ μs

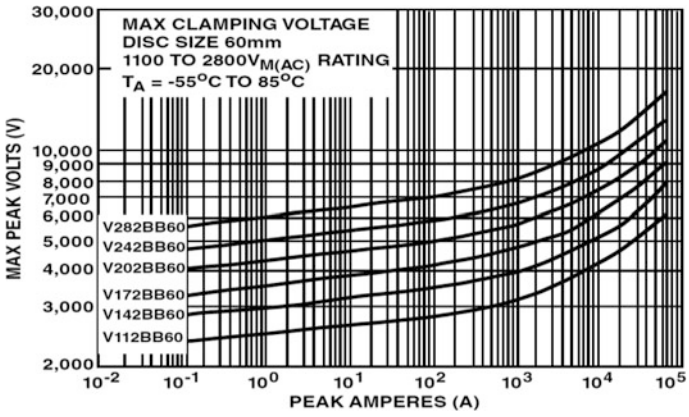


Fig. 8.6 *VI* curve of V172BB60 [10]

versus 8 μs) in the clamping region. In the proposed design, the overshoot effect has been mitigated with IGBT's slow turn-off speed. Additional RC snubbers can also help to reduce the overshoot effect by reducing the current t_r.

From (8.6), with given V_{dc} and R_α, there are mainly two methods to reduce peak clamp voltage: reducing I_{pk} or increasing I_V_{dc}.

One common solution to reduce the peak current in each MOV is to parallel several MOVs so as to limit the peak clamping voltage. However, this method increases the weight, size, and cost of the system. In addition, this solution is not very effective to reduce the peak clamp voltage. With the same V172BB60 MOV as example, even 10 of such MOVs are connected in parallel, the peak current is reduced to 500A, but the clamp voltage is only reduced from 5000A to 4300 V. It is still too marginal to use 4.5 kV class IGBTs, especially considering the transient over voltage due to parasitic commutation loop inductance. And the total weight of MOVs is already 5 kg. Let along the additional weight of busbars for interconnection and structure for mechanical support.

Since MOV can only carry sub milliamp when blocking V_{dc} in the standby mode, to increase I_V_{dc}, the MOV must be disconnected from the circuit fast enough once the fault current is clearly.

One way to realize this is to disconnect the whole SSCB from the dc system with one additional switch. Such switch needs to carry the full system current in the normal operation condition and break the leakage current when MOV is blocking the dc link voltage. Thus, a medium voltage high current mechanical contactor is a good fit. This method can also provide galvanic isolation. However, there is no commercially available medium voltage mechanical contactor, and its weight will certainly limit the overall specific power.

Another way is to insert an auxiliary switch in series with the MOV only, such as in Fig. 8.7.

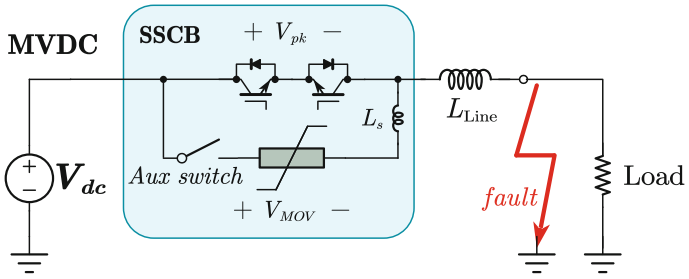


Fig. 8.7 MOV with auxiliary switch to disconnect MOV in standby mode

Such auxiliary switch doesn't carry any current in normal operation condition, so it will not affect the SSCB's efficiency. And such auxiliary switch only carries a pulse current as the MOV, so such switch doesn't need to be actively cooled. However, such auxiliary switch must be turned on right before the fault current is commutated from the IGBT to the MOV and turned off right after the system fault current is cleared. How to realize the required control speed and accuracy without complicate control circuit introduces serious challenges. Otherwise, the reliability of the SSCB may be jeopardized.

[11] uses an IGBT whereas [12] uses a SiC MOSFET in series with the MOV for this purpose. High device cost, peak current capability of a single device, additional gate drivers, and control signal coordination lower the feasibility of these approaches. In [13], a gas discharge tube (GDT) is connected in series with the MOV to share the V_{dc} in the standby condition. However, GDTs have poorer reliability in SSCB applications (repetitive surge events with prolonged arcing times due to t_{clear} of 100 s of μs can degrade contacts faster) and lack operational consistency (±20% fluctuation in sparkover voltage due to contamination). Besides, they are slow to conduct compared to solid-state devices which is suboptimal for the fast clamping required by the VCC [14].

To realize the function of the auxiliary switch, a novel VCC scheme is used termed as the electronic MOV (eMOV) which combines mature and reliable thyristor technologies with the traditional VCC to reduce the peak clamping voltage. It features silicon controlled rectifier (SCR)-breakover diode (BOD) pairs where the BOD with its sharp breakover voltage and stable *I-V* characteristics assists the MOV in the standby period improving the maximum blocking voltage of the eMOV unit, while the SCR with its high pulse current capability provides fast fault current bypass by inserting the MOV into the circuit for fault current extinction. Further, the BOD provides a passive triggering mechanism for the SCR eliminating the need for a dedicated gate driver and control strategy. Lastly, the eMOV components are inexpensive and proven in protection applications such as the popular crowbar circuit [15].

The proposed eMOV-based VCC is shown in Fig. 8.1. The BOD, connected between the anode and gate of the SCR, serves a dual-purpose. It shares the V_{dc}

with the MOV during the standby period, whereas during the fault transient, its voltage rises to its breakover voltage (V_{BO}) providing the gate current necessary to turn on the SCR thereby inserting the MOV into the circuit. The BOD needs not be rated for high pulse current (I_{SM}) as the BOD branch current is limited by the MOV impedance (fault current is quickly bypassed by the SCR) but requires a PN diode in series for reverse blocking capability [16, 17]. For the SCR, several commercial modules are applicable including ones optimized for fast, pulse type applications [18]. The low-pass RC filter (R_g, C_g) at the Gate-Cathode (G-K) terminals improve SCR *dv/dt* immunity. Because both the BOD and MOV exhibit high non-linearity where their standby region leakage currents are largely dependent on their material properties, identical high value ($M\Omega$) static balancing resistors (R_{static}) are used in parallel across each device to force equal voltage sharing in the steady state. Thanks to the static balancing, the standby region voltage of each part satisfies (8.7), where V_{MOV} and V_{BOD} are the voltage across the MOV and BOD during static state.

Another important point to note is that the eMOV's current when blocking the full dc link voltage (I_{lk}) should be below the SCR's $I_{H,SCR}$ rating so the latter can turn off after fault current extinction as in (8.8).

$$\begin{cases} V_{MOV} = V_{BOD} \\ V_{MOV} < V_{M,dc} \\ V_{BOD} < V_{BO} \end{cases} \tag{8.7}$$

$$I_{lk} < I_{H,SCR} \tag{8.8}$$

The dynamic operation during the fault transient is in Fig. 8.8. The three time intervals of significance are explained below:

$0 - t_1$: The circuit is under normal operation until the main device is gated "off" at t_1.

$t_1 - t_2$: The voltage across the main device increases due to the inductive effect. The dynamic voltage sharing between the MOV and the BOD depends on their ac impedance. From their physical structure, the junction capacitance values are such that $C_{BOD} << C_{MOV}$. Thus, the BOD nearly tracks the device voltage reaching its V_{BO} at t_2. The voltage across the main device at t_2 is denoted as V_{th} in Fig. 8.8 where $V_{MOV}(I_{BO})$ is the MOV voltage at I_{BO} which is typically a few mA.

$t_2 - t_3$: The BOD starts to conduct immediately, providing a peak gate current of $I_{g,pk}$ thus triggering on the SCR.

$t_3 - t_4$: The SCR is in the on-state and takes on shunts the fault current through the MOV. During this time, the SSCB voltage V_{SSCB} is clamped by the MOV. Beyond t_4, the fault current reduces to zero after which the SCR turns off due to (8.8) and the system returns to the standby state described earlier.

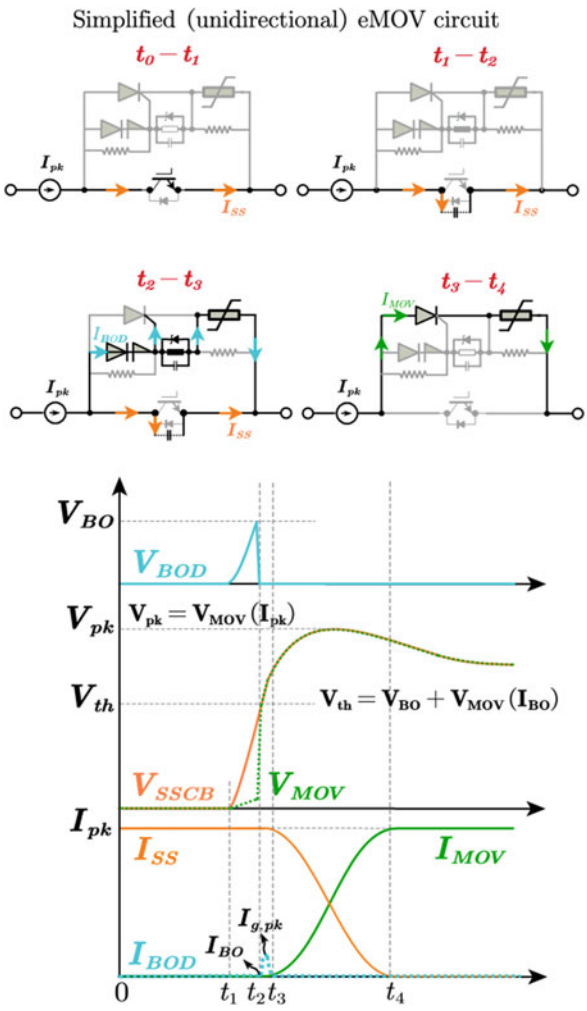


Fig. 8.8 Zoomed in view of the critical (idealized) waveforms during the fault turn-off transient

The design criteria for the eMOV are summarized below:

1. For successful standby region operation, the BOD and MOV parts must be selected as per (8.9) in contrast to enabling reduced V_{pk} values.

$$\begin{cases} V_{\mathrm{M,dc}} > V_{\mathrm{dc}}/2 \\ V_{\mathrm{BO}} > V_{\mathrm{dc}}/2 \end{cases} \tag{8.9}$$

Further, the R_{static} selection must ensure both (8.7) and (8.8).

2. To prevent overvoltage across the solid-state device, the following conditions must also be satisfied.

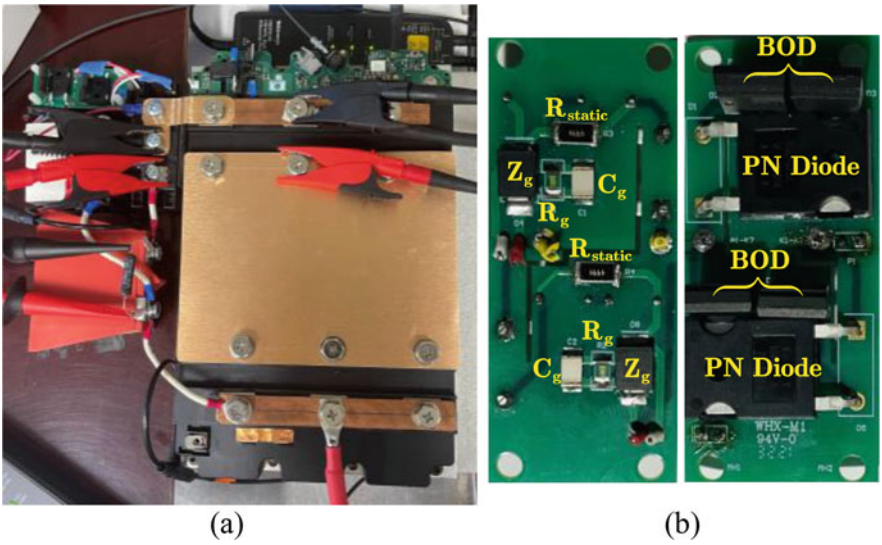


Fig. 8.9 (**a**) eMOV in prototype 1.2kA 2 kV SSCB; (**b**) Passive triggering circuit PCB

$$\begin{cases} V_{\mathrm{MOV}}\left(I_{\mathrm{BO}}\right) + V_{\mathrm{BO}} < V_{\mathrm{rated}} \\ V_{\mathrm{MOV}}\left(I_{\mathrm{pk}}\right) < V_{\mathrm{rated}} \end{cases} \tag{8.10}$$

Accordingly, the main device V_{rated} can be selected with a minimum 10% safety factor.

3. The SCR module *V*-*I* ratings must satisfy (8.11).

$$\begin{cases} V_{\mathrm{RRM/DRM}} > V_{\mathrm{BO}} \\ I_{\mathrm{TSM}} > I_{\mathrm{pk}} \end{cases} \tag{8.11}$$

The MOV energy needs to be considered as well but based on separate analysis, with a maximum 50 μH system inductance, the selected MOV's energy capability can easily meet the system requirement with sufficient margin.

The eMOV prototype is shown in Fig. 8.9a and the passive trigger circuit board is shown in Fig. 8.9b.

The MOV in Fig. 8.9a is V881BA60. Its $V_{M,\,dc}$ is 1150 V, which is higher than half of the dc link voltage and its clamping voltage when carrying 5kA is less than 3 kV. So the ratio between the clamping voltage and the DC bus voltage is reduced to 1.5.

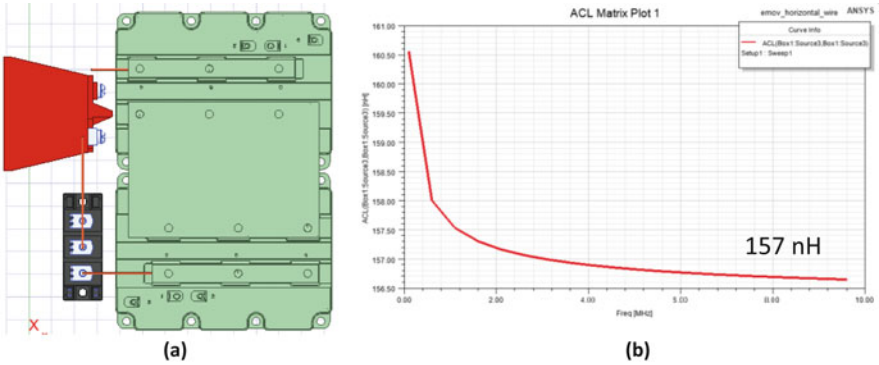


Fig. 8.10 Commutation loop inductance analysis with eMOV. (**a**) Simulation model. (**b**) Analysis result

Due to the additional components in the commutation loop between MOV and IGBTs, the parasitic loop inductance is much higher than in the traditional design. The simulated loop inductance is shown in Fig. 8.10.

Considering the additional parasitic inductance in the IGBTs and thyristor modules, the total loop inductance is more than 200nH. Such loop inductance is manageable with reduced IGBT turn-off speed. Please note that, the loop inductance can be reduced by replacing the high voltage wire (rated at 20 kV) shown in Fig. 8.9 with busbars. However, since compact design is not necessary, it is obviously much easier for insulation design with commercial off the shelf high voltage wire.

5 High Altitude Design

The high altitude insulation design can be handled at two different levels: the component level and the system level.

Ideally, all components are commercially available and qualified for high altitude aviation application, and there are standards as design guidance to follow at system level, such as the clearance and creepage distance requirement at different altitude and voltage level.

Unfortunately, the hybrid electric propulsion application is still in its early stage. There is no aviation qualified high voltage component in the market and no existing standards to follow. Thus, the potential component candidates need to be screened via dedicated tests for insulation capability evaluation. And sufficient margins should be left at system level design. In addition, the final insulation performance must be verified by experimental results under emulated high-altitude condition.

The most critical component for the solid-state circuit breaker is semiconductor devices, which is Si IGBT in this example design. EC 61287-1 [19] is the only available standard for power converters issued for railway applications that has proposed

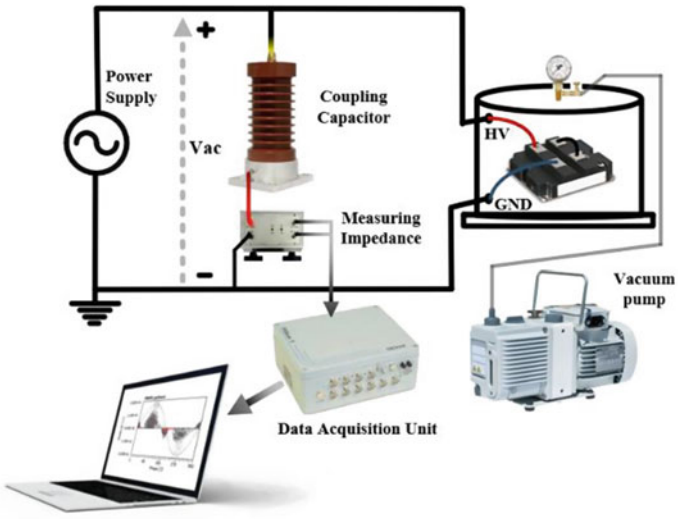


Fig. 8.11 PD test setup used at low pressure tests for (pre-heated) IGBT samples

a general PD testing procedure for insulation qualification of modules. However, the suggested test method is to apply a 50 or 60 Hz AC voltage with defined specific magnitudes in the short time intervals between interconnected terminals and the base plate for PD assessment. It has overlooked the possibility of weak electrical points between the electronic components on the internal substrate and has not addressed the impact of harsh environmental and operational conditions on PD activity for other applications. Therefore, a more efficient testing configuration for the IGBTs which can identify these possible weak locations is adopted.

As shown in Fig. 8.11, the conventional PD measuring system proposed by IEC 60270 equipped with vacuum chamber and pump is used for recording the PD pulses inside a Faraday cage filtering the noises higher than 15 pC. In order to extract the accurate PD pulse waveforms with wide frequency bandwidth (16 kHz-48 MHz), direct measured PD pulses from measuring impedance in mV are presented without additional conversion to pulse charge in pC. The test samples are placed inside a vacuum chamber connected to a pump to adjust the pressure before applying the voltage.

Several potential IGBT candidates were screened with the same method. Two of them are listed in this chapter to show the importance of such PD screen tests. They are from the same vendor with very similar packages and have maximum rated voltage of 3.3 kV and 4.5 kV, respectively.

As mentioned, the general test procedure for PD endurance test suggested by the standard is to assess the insulation performance between the interconnected terminals and baseplate (common mode) where the substrate and multilayer structure used in AMB (active metal brazed Cu on the AlN) layout is employed. Bearing that in mind, weaknesses of the triple junction point where the metal, substrate, and

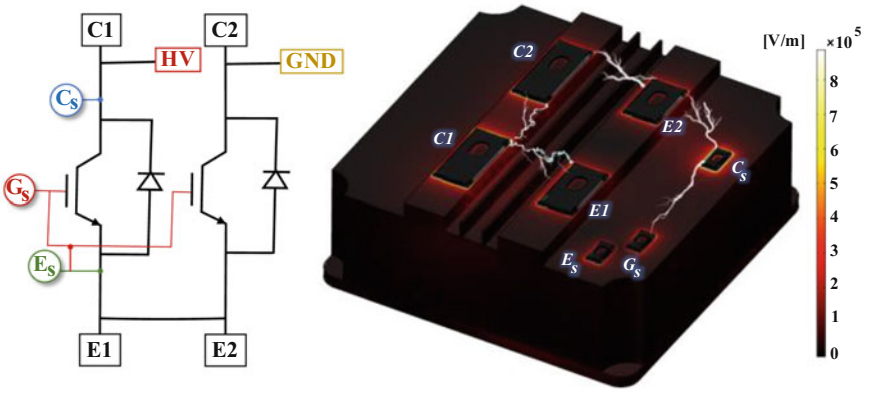


Fig. 8.12 A 4.5 kV IGBT module with electric potential exterior package and simplified substrate structure, and schematic circuit diagram representing the test connections

silicone gel meet have been evaluated and discussed for the experiments mainly conducted at ambient conditions such as in [20–22]. This chapter highlights the importance of the localized highly stressed areas at harsh environmental conditions among the different metallized regions on the substrate surface fed by the collector, emitter, gate, and ground terminals (differential mode) in direct copper bonding (DCB) substrates as common design of high voltage IGBTs and possible operational scenario during blocking mode.

PD tests under AC voltage, conducted in the study, compared to the DC voltage for assessing the IGBT blocking capability not only have more mature testing procedure defined by the standard but also can easily trigger the PD activity from any possible electrically weak insulated areas in differential mode of module operation. To apply AC voltage across the IGBT samples, two IGBTs are required to be connected anti-series. For the IGBT modules under test, they have two identical IGBTs inside which can realize such configurations by itself.

Figure 8.12 demonstrates the test connection on a simulated 4. 5 kV IGBT module package used in the experiments as well as the 3D electric potential profile on the IGBT package simulated in COMSOL. High voltage and ground terminals are connected to the collector terminals and emitter terminals are interconnected. Parallel diodes are short circuit in the negative half-cycle of the voltage, so the maximum electric potential difference between the collector and emitter is the peak of applied voltage at the positive half-cycle. Electrostatic 3D simulation results for a multi-scale design are achieved by COMSOL Multiphysics 5.5.

These modules were firstly tested at ambient temperature. This group of tests was conducted at fixed pressures of 20 kPa, 15 kPa, and 10 kPa inside the vacuum chamber corresponding to the altitudes of 38 kft, 45 kft, and 52 kft, respectively. The voltage was ramped up with a rate of 200 V/sec up to 2.4 kV_{rms} or 3.3 kV peak for 3.3 kV IGBT modules and 3.35 kV_{rms} or 4.5 kV peak for 4.5 kV IGBT modules (hereinafter kV instead of kV_{rms} for the applied test voltage). Inconsistent

PD occurrence was the main characteristic of the PD behavior for these samples. Therefore, the PD data is recorded in repeated tests performed on nine test samples in a 2-minute duration after increasing the voltage from zero to the different voltage levels lower than the rated voltage of modules. The latent PD incident and the possible progression of PD source can be captured in this recording time interval. Distribution of the recorded PD data (number of PDs and PD pulse magnitudes) is statistically represented in Fig. 8.13 with boxplots consisting of minimum, maximum, interquartile range (from first to third quartiles) of the data.

Accumulative PD magnitude is obtained by the summation of all PD pulse magnitudes detected for each test. Wide variation in the recorded data is observed in each scenario. However, the impact of pressure on the intensity of the PDs is evident. PD initiates with low probability at the rated voltage in the pressure of 20 kPa and occurs at lower voltages in lower pressures. Consistent PD occurrence with higher pulse magnitudes and repetition rate was detected beyond 2.2 kV for 3.3 kV IGBTs and 2.6 kV for 4.5 kV IGBTs where all recorded results are represented with the bars having non-zero minimum value for the detected number of PD pulses and their magnitudes. However, inconsistent PD results at 2.4 kV at 15 kPa and 2 kV at 10 kPa for 3.3 kV IGBT, and 3.35 kV at 15 kPa and 2.4 kV at 10 kPa for 4.5 kV IGBT with higher concentration of the values at top half of the bars should be taken seriously as well. Although both types of IGBTs have similar packaging and exterior dimensions, repetitive flashover incident was observed on the package surface of 4.5 kV IGBTs with higher rated voltage at 10 kPa.

It should be noted that although the differential mode was the main connection configuration in our tests, the same tests were performed for common mode at low pressures and no significant PD activity was observed and recorded.

Based on the test results, the PDIV are significantly lower for both modules at high altitude as expected. And the 4.5 kV module has better PD performance than the 3.3 kV module. This observation seems very reasonable because the 4.5 kV module is designed to handle higher voltage.

After the ambient temperature test, the test samples were heated up to emulate the actual operation condition. When the IGBTs are carrying and chopping current, the normal IGBT die temperatures are between 60 °C and 120 °C. In these tests, test sample was heated inside an oven for 1–1.5 hours until the temperature of baseplate reaches to the desired value before the test outside the oven. So, a temperature-drop less than 5 °C was observed during the test inside the vacuum chamber. The main observation about this group of tests was the detectable PDIV with high repetition rate of PDs at higher temperatures compared to the previous tests. More intense PD activity occurred considering impact of both pressure and temperature.

The distribution of the PDIV values including minimum, maximum, and the mean at different pressures and temperatures is summarized in Fig. 8.14. At ambient pressure, unlike the 3.3 kV IGBTs with safe operation, PD initiates for 4.5 kV IGBT at temperatures beyond 80 °C, and PDIV is considerably higher than that of the values recorded at lower pressures. Also, a linear relation between the PDIV values and pressure/temperature was achieved.

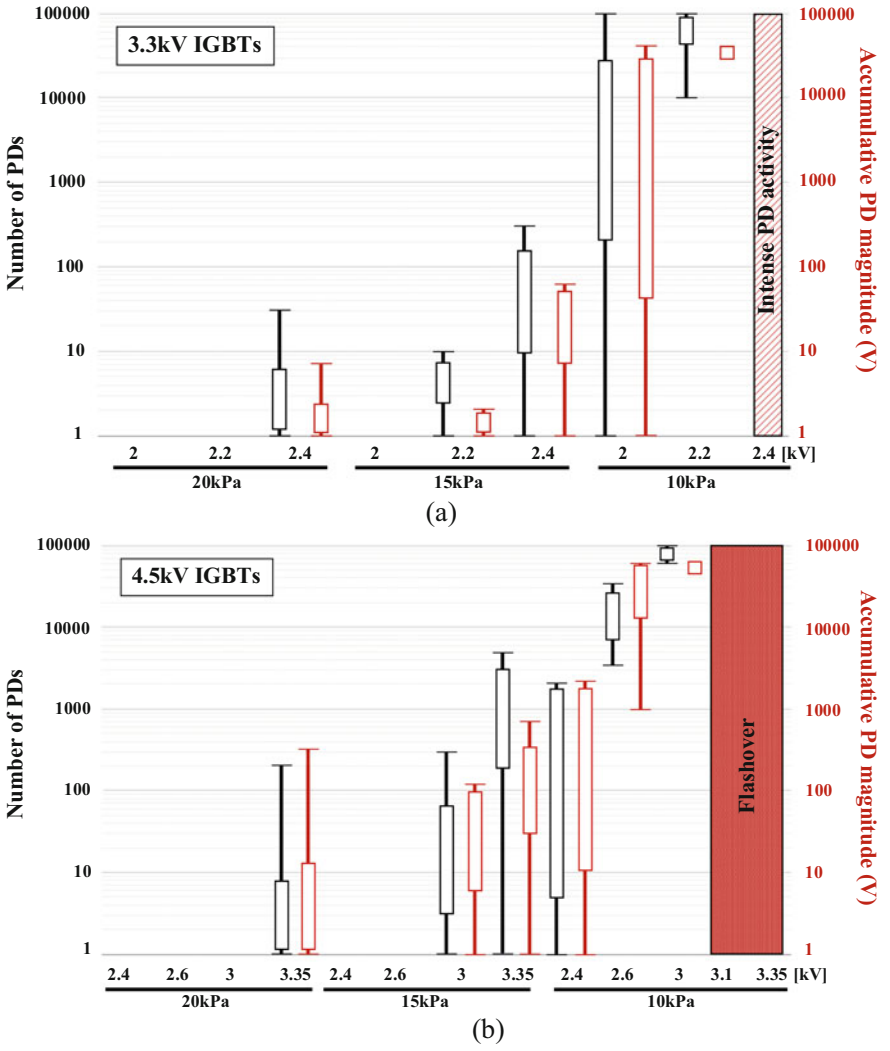


Fig. 8.13 Statistical data on PD activity at different voltage levels in separate tests and different adjusted pressures for both types of IGBT samples (data was recorded for 2 minutes in each separate test with maximum 100,000 PDs)

As a surprising observation, when heated up, the 3.3 kV IGBTs have much better PD performance compared with 4.5 kV IGBT especially when the junction temperature is close to 120 °C. In other words, when carrying current, the 4.5 kV IGBT under test can trigger PD easier than the 3.3 kV IGBT. And different 3.3 kV IGBT modules from different vendors also show a relatively wide PD performance variation.

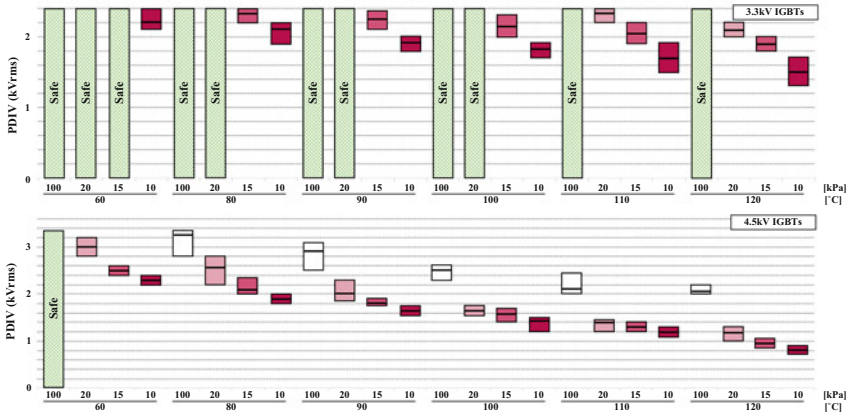


Fig. 8.14 Statistical data of PDIV values at different pressures and temperatures for both 3.3 kV and 4.5 kV IGBTs

Other than the IGBTs, all electric components were screened with similar procedure, including the MOV, thyristors, gate drive power supplies, and other PCBs which may see high voltage potential during operation.

6 Prototype Design and Test Results

The prototype based on the proposed SSCB solution is shown in Fig. 8.15a and its weight breakdown shown in Fig. 8.15b. The volume of the SSCB without the extruded busbar for cable connection is 0.025m^3 and the total weight is 40 lb. The specific power is 133 kW/kg and the power density is 96 MW/m^3. And the measured efficiency at 1200 A is 99.76%.

The switching performance of the SSCB prototype has been evaluated under various operating conditions, including different short circuit impedances, different junction temperatures, and different gate drive parameters.

A 2 kV/1 kA SSCB prototype is built and tested for performance evaluation. Figure 8.16 presents the SSCB test circuit diagram, and a photograph of the test setup is shown in Fig. 8.17.

As detailed in Section III, reduced gate voltage provides significant advantages in SSCB applications without incurring too high a penalty. For this reason, an on-state gate voltage of 12 V is selected. The test results are presented in this subsection. Figures 8.16 and 8.17 show the SSCB voltage and current waveforms during the interruption of a short circuit developed with a system inductance of 25 μH and DC source voltage of 2000 V when the IGBT junction temperature is at room temperature and 100 °C, respectively. The short circuit is detected and then acted upon by the gate drive's desaturation protection circuit. The system inductance is

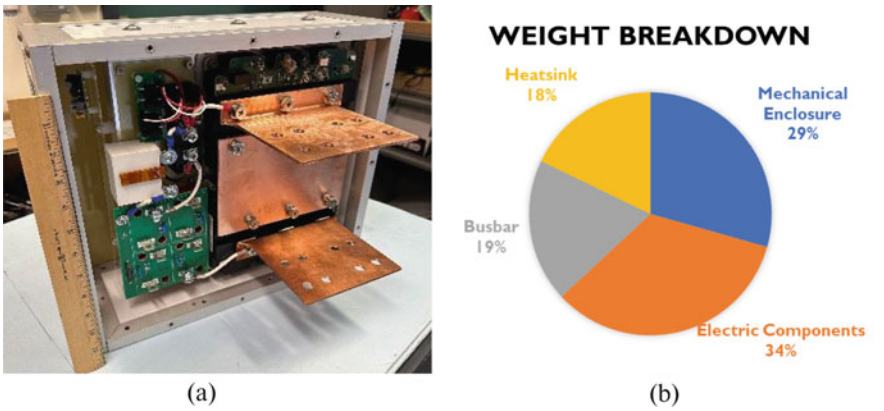


Fig. 8.15 SSCB Prototype mechanical design. (**a**) Prototype with side panel removed. (**b**) Weight break down

Fig. 8.16 Circuit diagram of the test bed

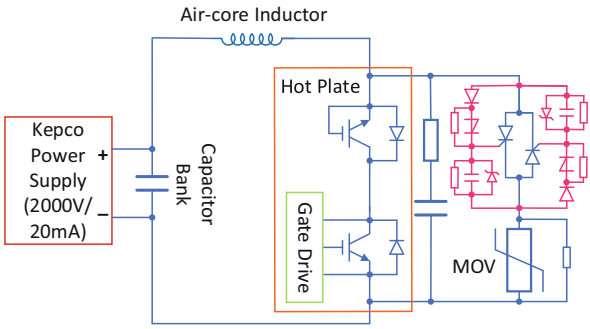
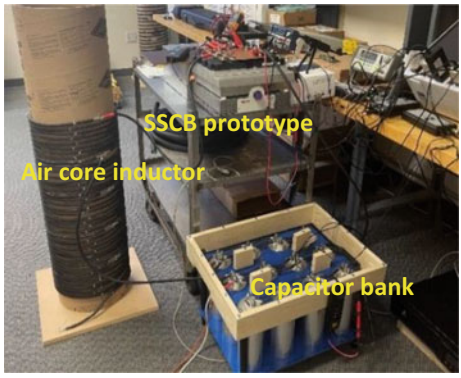


Fig. 8.17 Photograph of the switching test bed



sufficiently high, so the fault current is interrupted before the IGBT enters the active region. The IGBT voltage and current trajectories during the short circuit current interruption stay well within its reverse bias safe operating area, thanks to the eMOV as well as properly sized RC snubber. At a higher junction temperature, the short

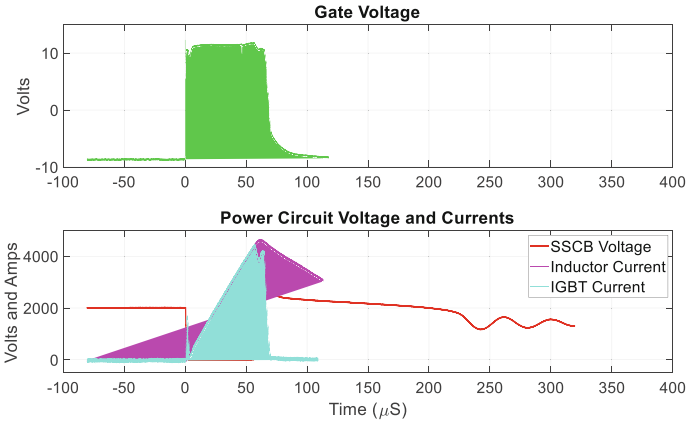


Fig. 8.18 Switching waveforms, $L_{\text{System}} = 25$ μH, $V_{\text{DC}} = 2000$ V, T_{Junction} is room temperature

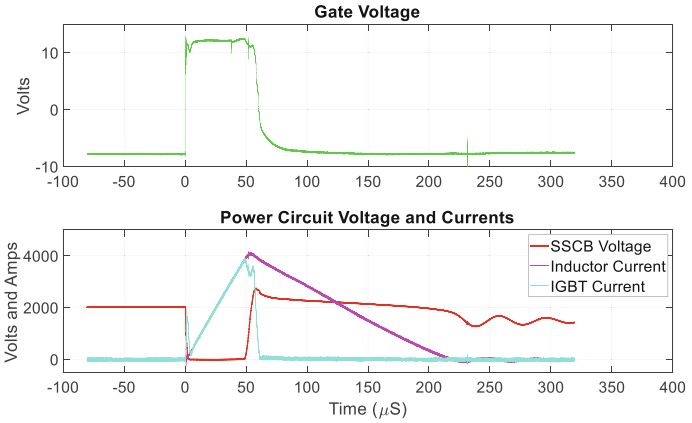


Fig. 8.19 Switching waveforms, $L_{\text{System}} = 25$ μH, $V_{\text{DC}} = 2000$ V, $T_{\text{Junction}} = 100$ °C

circuit condition is detected sooner, lower the fault current peak value is lower (Figs. 8.18 and 8.19).

Figures 8.20 and 8.21 present the SSCB voltage and current waveforms during the interruption of a short circuit developed with minimum system impedance, with the air-core inductor shown in Fig. 8.17 bypassed. The system inductance is only 300nH, mainly due to the power cabling. And the parasitic inductance inside SSCB is about 200nH. Thus, the total inductance limiting the fault current is around 500nH. As seen in these figures, the IGBT enters the current saturation mode shortly after the fault initiation and before the gate drive circuit detects the fault and responds to turn off the gate. The IGBT voltage stays well above zero during the short circuit. The initial ramping rate of the fault current is contained below 3 kA/μs. And the peak fault current flowing through the IGBT is effectively

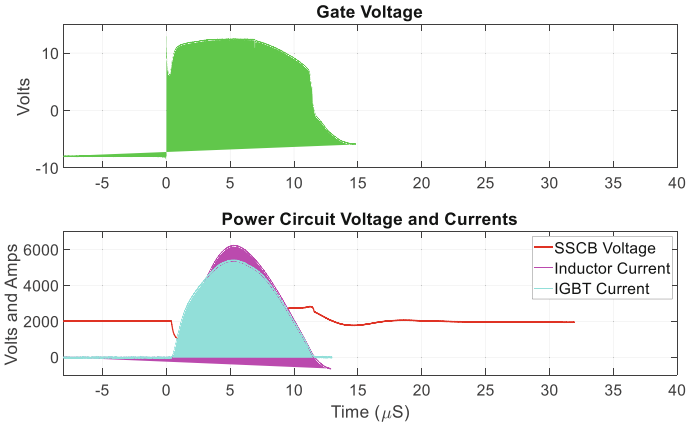


Fig. 8.20 Switching waveforms, $L_{\text{System}} = 0$ μH, $V_{\text{DC}} = 2000$ V, T_{Junction} is room temperature

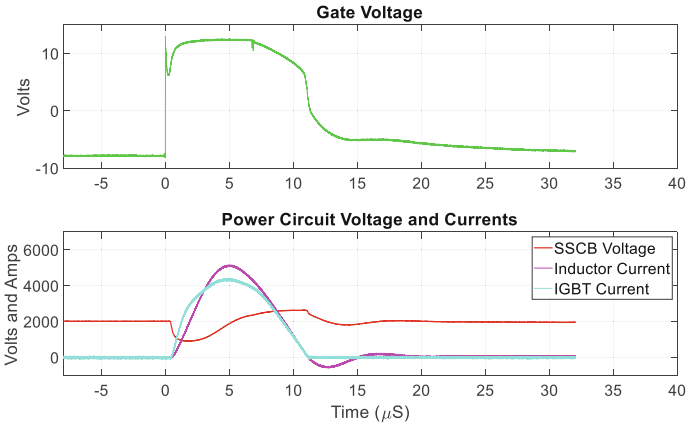


Fig. 8.21 Switching waveforms, $L_{\text{System}} = 0$ μH, $V_{\text{DC}} = 2000$ V, $T_{\text{Junction}} = 100$ °C

limited to 5 kA which consequently is interrupted after the protection circuitry is triggered. Such peak fault current is further reduced to 4 kA with higher junction temperature, which is closer to the real case.

7 Concluding Remarks

The aviation applications introduce unique design challenges for SSCB design, including extremely high specific power, high efficiency, insulation capability at high altitude, and high reliability. A novel SSCB design is developed to address all challenges. Such SSCB eliminates the current limiting inductor in the traditional

design which substantially improves the specific power and implements an eMOV circuit to enable 3.3 kV IGBT for high efficiency. Due to slow switching of IGBT, the mechanical layout is optimized to enhance the insulation capability, and mature technologies are adopted to increase the technical readiness level and reduce risk. The design principles and performance are verified with a 2 kV 1.2 kA prototype. All key specifications including 100 kW/kg, 99.5% efficiency, and 35 kft PD free operation are met.

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Chapter 9
Light-Triggered Solid-State Circuit Breaker for DC Electrical Systems

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1 Introduction

A power system can store a considerable amount of energy in the inductance and capacitance of cables, and in the inductance and capacitance of line and load filters. In particular, when a circuit breaker opens, the intent is to reduce the line current to zero; the inductive flyback must be managed to avoid damaging components. While mechanical circuit breakers are robust to temporary over-voltage and over-current stresses, a solid-state circuit breaker (SSCB) is less capable of absorbing this energy. To circumvent this, our approach is to divert the current to an energy storage component, namely, a capacitor, using a fast semiconductor switch. In this way, the cable energy is absorbed and not dissipated in the semiconductor switches of the SSCB. Herein, we consider a novel, ultra-fast, normally-OFF optically triggered gallium nitride (GaN) photoconductive semiconductor switch (PCSS) to redirect this latent energy while the SSCB is opening.

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2 Medium Voltage DC Applications

Emerging medium voltage, direct-current (MVDC) systems (5 kV to 65 kV) encompass important applications including electric rail and electric ship transportation, DC power distribution networks in industrial complexes, DC grid power distribution, and distributed energy integration/management including renewable energy sources such as photovoltaics (PV) and off-shore wind [1]. The principal driver for increased interest is economic. Since energy resources and loads increasingly utilize direct current, it is appealing to eliminate the DC-AC and AC-DC power conversion, as well as bulky AC transformers, where possible. The principal value proposition of using AC is for more efficient long-distance transmission. However, if, for example, a solar photovoltaic source (DC) is co-located with a battery back-up resource (also DC) and a dense load center that includes LED lighting and computers (predominantly DC), there may be little need for AC power, and the complexity, installation costs, and maintenance costs of an MVDC power distribution and management system may be lower. The ease of integrating energy storage and distributed generation and the increasing prevalence of DC loads are the principal "driving forces" behind DC power distribution [2]. Figure 9.1 illustrates the reduction in complexity of a grid-tied photovoltaic (PV) system when using a DC power distribution network with DC resources. It is noted that the medium voltage AC system requires additional power conversion stages as well as transformers, not to mention more conductors. This added hardware and complexity adds installation cost and diminishes conversion efficiency at the system level.

A large impediment to fulfilling state and utility renewable portfolio standards is the high levelized cost of solar PV energy ($109.8/MWh) compared to other sources (e.g., a conventional coal plant at $60.4/MWh) [3]. This disparity in cost is due primarily to the high installed cost of commercial and utility-scale solar PV systems

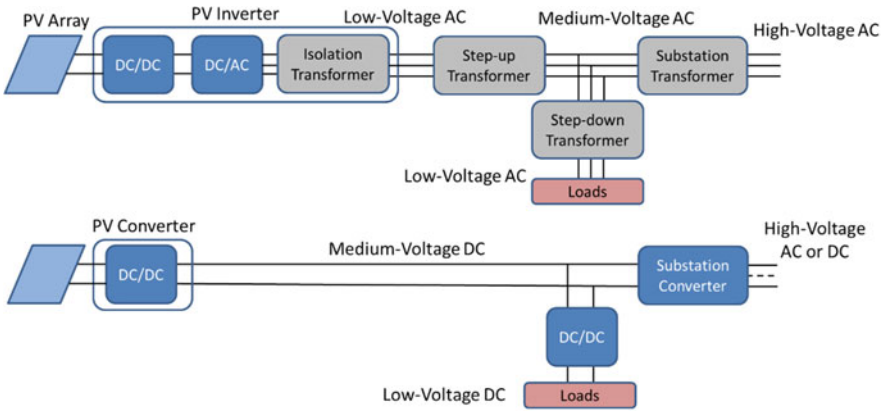

Fig. 9.1 A notional grid-tied PV system based on (top) a conventional AC network with DC resources and AC loads, and (bottom) a DC network with DC loads

(relative to capacity factor), which currently totals between $1.77/W and $2.28/W [4]. Furthermore, inefficiency and construction costs associated with AC distribution and transmission and DC-AC conversion are motivating many, including the US Department of Energy (DOE), to consider advocating direct connection of PV to DC distribution (and even DC transmission) circuits. Currently, the benchmark cost for commercial and utility-scale inverters averages $0.12/W, installation labor averages $0.21/W, and the balance of the system (BoS) averages $0.16/W [3]. The proposed converter is expected to yield a solution with $0.05/W for the converter and $0.15/W for the installation cost. Furthermore, the higher-voltage modular design will yield $0.02/W BoS savings [4]. Finally, a projected 2% improvement in conversion efficiency is expected to yield an equivalent $0.04/W benefit, totaling $0.19/W savings in commercial and utility-scale installation cost. These costs consider only the PV plant itself, and do not include the DC-AC or DC-DC converter station, the reduced conduction losses in DC distribution cables, and the improvements and cost savings it is purported to provide.

With the exception of smaller boutique designs for yachts and recreational boats, ships utilize medium voltage alternating current (MVAC) power distribution [5]. This limits how the ship propulsion can be controlled and requires multiple bulky AC transformers in the limited space available. There is increased interest in the development of MVDC power system architectures for maritime applications as well as for the US Navy [6]. MVDC requires less hardware, eases the interconnection of energy storage, and can be used to drive variable frequency drives for more agile propulsion control.

Safe operation of these MVDC power distribution systems requires a resettable circuit breaker (CB) technology to isolate faulted portions of the network from the normally operating portion. DC systems present a challenge for these safety devices, as there is no zero crossing (as with AC systems) to interrupt the formation of an arc. In addition, power electronic converters are typically less resilient than transformers and cannot support fault currents for as long; thus, the circuit breaker must be able to interrupt these currents more quickly than contemporary mechanical AC circuit breakers.

3 MVDC PCSS-Based Solid-State Circuit Breaker

Solid-state circuit breakers (SSCBs) utilize semiconductor-based device technologies of various designs, resulting in fast response times (typically several orders of magnitude faster than mechanical CB technologies), limiting the fault-induced energy from impacting the rest of the DC system. Additionally, because there are no moving parts, the potential lifetime of the SSCB can be significantly longer than that of their mechanical counterparts. Finally, the small size of the solid-state technology could lead to more compact, higher-power-density SSCBs, which is advantageous in space-limited applications such as rail and ship transportation. Disadvantages of SSCB technology include higher cost of the parts compared to mechanical CBs, as

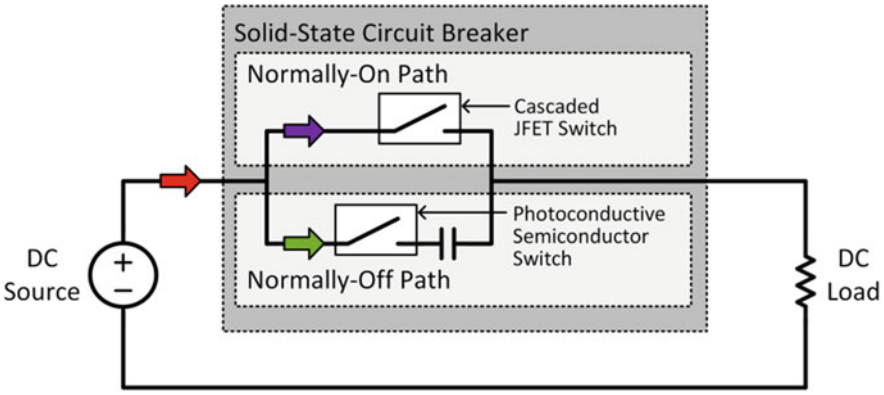

Fig. 9.2 Conceptual breaker diagram with source and load

well as potential current and voltage limits of the devices, thereby requiring series- and parallel-connected circuit architectures that can complicate SSCB control.

A diagram of the proposed SSCB circuit is shown in Fig. 9.2. The breaker consists of two subcircuits which operate in close coordination. The two subcircuits are referred to as the normally-ON and normally-OFF paths, named in accordance with their state during normal (pre-fault) operation. The normally-ON path consists of cascaded JFET devices which act as a high-voltage switch. The normally-OFF path includes a photoconductive semiconductor switch (PCSS) in series with a capacitor. The function of the normally-OFF path is to momentarily divert fault currents from the normally-ON path during a turn-OFF event, allowing the normally-ON path to transition to an OFF state without the massive thermal stresses associated with breaking fault currents.

A conceptual representation of the expected breaker behavior is shown in Fig. 9.3. A fault occurs at time t_0, causing the current through the normally-ON path to rise. At time t_1, the JFET circuit gate driver triggers, forcing the cascaded JFETs to begin transitioning to the OFF state. The voltage across the normally-ON path begins to rise. The PCSS fires at time t_2, immediately diverting current away from the normally-ON path and into the shunt capacitor. Between t_2 and t_3 the capacitor voltage rises and the current through the normally-OFF path tapers, eventually reaching a cut-OFF threshold. Thereafter, the normally-OFF path ceases to conduct current, concluding the breaker turn-OFF transient.

Design and Operation of Normally-ON Path

Figure 9.4 shows the proposed high-voltage switch topology, generalized to n number of SiC JFETs connected in series. As will be explained below, the JFET leg is controllable to provide DC voltage blocking between the terminals labeled *Source* and *Drain*. Also shown in Fig. 9.4 is a leg constituted by series-connected avalanche diodes $D_1 - D_{n-1}$, and a leg constituted by series-connected capacitors $C_1 - C_n$. Each avalanche diode is connected between the gates of two sequential JFETs.

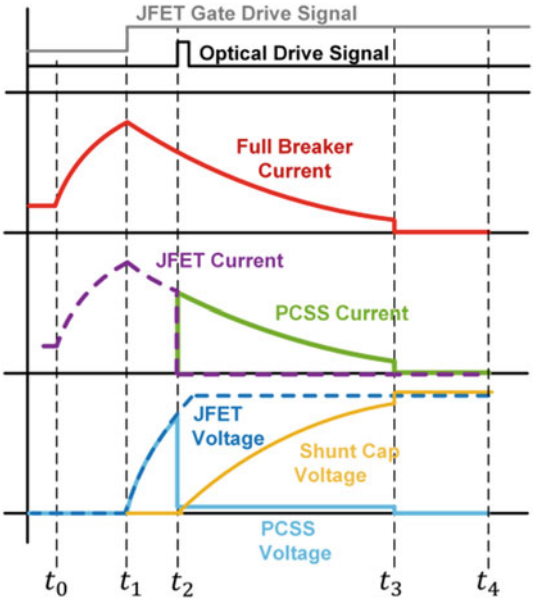

Fig. 9.3 Predicted voltage and current timing diagram for different parts of the circuit breaker

Likewise, each capacitor is connected between the gates of two sequential JFETs, except that C_1 is connected between the *Source* terminal and the gate terminal of J_2, and C_n is connected between the gate terminal of J_n and the *Drain* terminal.

The avalanche diodes are to protect the transistors in the event that an overvoltage greater than V_{DC}/n is applied across any of them. The capacitors are designed to dynamically balance the voltage sharing on each transistor during the ON and OFF transitions, which will be described below. Figure 9.4 also shows a balancing network of resistors $R_1 - R_{n+1}$, which is connected between the *Source* and *Drain* terminals to balance the static voltage across the JFET leg. It is noteworthy that this static balancing network comprises more than one leg of series-connected resistors. The illustrated example has two legs. One leg comprises resistors $R_1 - R_{[n/2]+1}$, and the other leg comprises resistors $R_{[n/2]+2} - R_{n+1}$, where $[n/2]$ represents the truncation of $n/2$. Alternatively, the passive balancing network may have three legs, or even more, up to a maximum of $n - 1$.

In the illustrated example, each resistor, with certain exceptions, is connected between the gates of two JFETs that are separated in sequence by one intervening JFET, with staggering by one JFET position between the two legs. The exceptions are:

- R_1 is connected between the *Source* terminal and the J_2 gate terminal (G_2).
- $R_{[n/2]+1}$ is connected between the J_n gate terminal (G_n) and the *Drain* terminal.
- $R_{[n/2]+2}$ is connected between the *Source* terminal and the J_3 gate terminal (G_3).
- R_{n+1} is connected between the J_{n-1} gate terminal (G_{n-1}) and the *Drain* terminal.

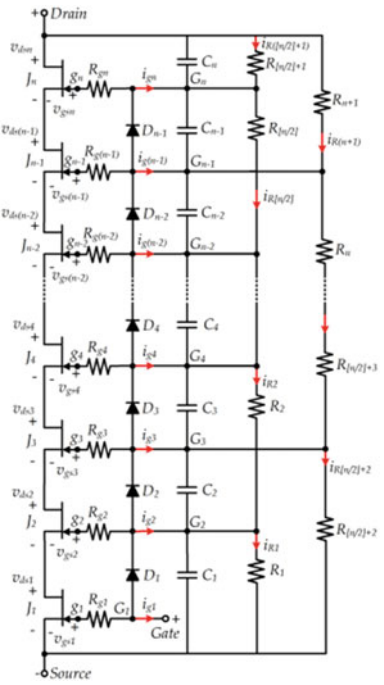

Fig. 9.4 Proposed normally-ON high-voltage switch with cascaded transistor topology

Turn-ON Transition

The initial condition of the cascaded switch is the OFF state, and the total DC voltage V_{DC} is assumed to be divided evenly among the n JFETs. The gate-source voltages of the JFETs are at a level slightly below the threshold voltage V_{th}, except for v_{gs1}, which is at the subthreshold voltage V_{G-}; i.e., $V_{G-} < V_{th}$. The voltage across each balancing capacitor is V_{DC}/n, except that the voltages across C_1 and C_n are $V_{DC}/n + V_{th}$ and $V_{DC}/n–V_{th}$, respectively. Due to their high values, the balancing resistors R_1 to R_{n+1} have no significant effect on the turn-ON and turn-OFF processes. Hence, they are treated as open circuits in the following discussion.

For simplicity of presentation, the following analysis is directed to an illustrative JFET leg in which there are four JFETs, denoted J_1, J_2, J_3, and J_4, respectively. The corresponding circuit diagram is shown in Fig. 9.5. However, the presented equations modeling the operating modes will be given in a generic form for n JFETs connected in series. The model to study the switching process assumes an inductive load, as is common practice for modeling the behavior of power converters, although in practical applications, the load can have any combination of inductive, capacitive, and resistive components. The model includes a free-wheeling diode together with the inductive load, in accordance with the well-known double pulse test (DPT) circuit configuration. Results indicative of switching behavior are shown in Fig. 9.6, to which attention will be drawn in the following discussion.

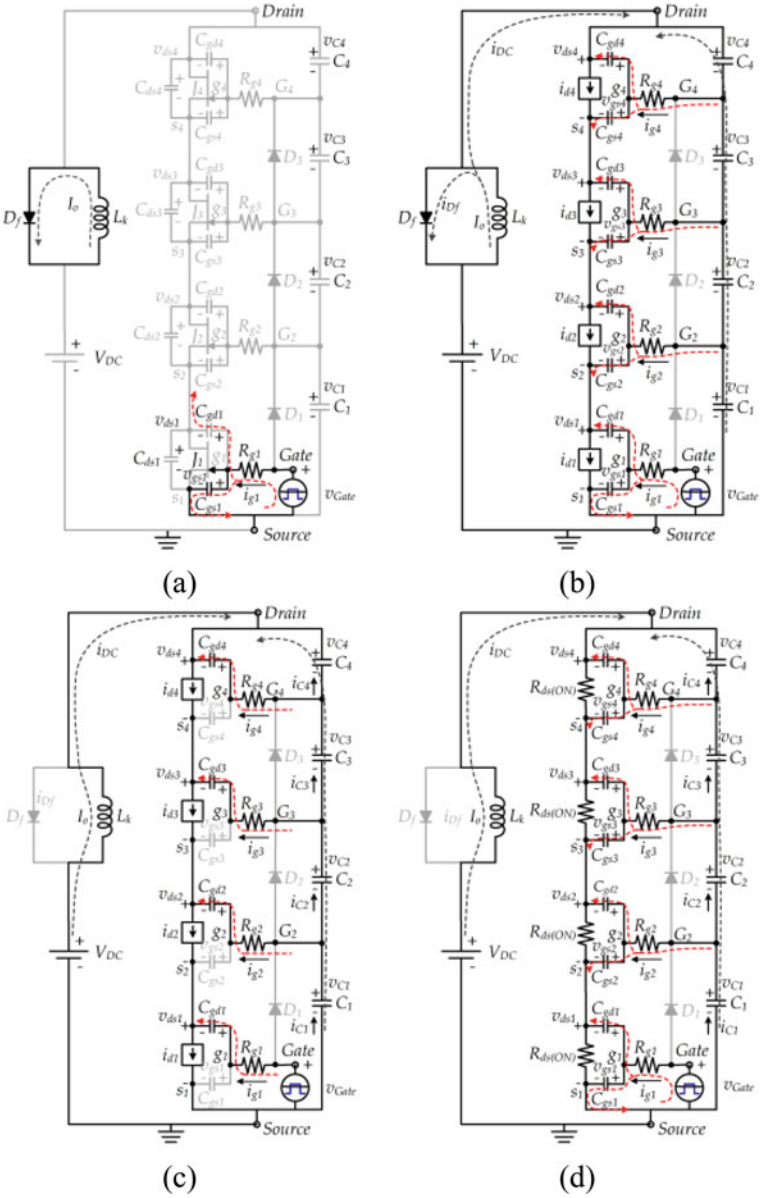

Fig. 9.5 Equivalent circuits during the turn-ON transient for (**a**) $[0 - t_0]$ interval, (**b**) $[t_0 - t_1]$ interval, (**c**) $[t_1 - t_5]$ interval, and (**d**) $[t > t_5]$ interval

1. $[0 - t_0]$ interval: At $t = 0$, $v_{\text{Gate}} = V_{\text{G+}}$ is applied between the *Gate* and *Source* terminals of the cascaded switch. This causes the voltage v_{gs1} to rise from its initial value $V_{\text{G-}}$, while v_{ds1} remains constant at $V_{\text{DC}}/4$. The capacitances C_{ds},

C_{gs}, and C_{gd} are inherent properties of the JFET devices. Note that C_{ds} is not considered in this analysis as it is much smaller than C_{gs} and C_{gd}. The gate current i_{g1} conducts through C_{gs1} to ground, and through C_{gd1}. C_{gd1} is in series with an equivalent capacitance connected to ground. Since C_{gs1} is approximately an order of magnitude greater than C_{gd1}, the effect of C_{gd1} is minimal in this operating mode. An analytical calculation yields the following expression for the evolution of the gate-to-source voltage of J_1:

$$v_{gs1} = V_{G+} + (V_{G-} - V_{G+})\, e^{-t/(R_{g1}C_{gs1})}. \tag{9.1}$$

The interval ends at t_0 when v_{gs1} equals V_{th}.

2. $[t_0 - t_1]$ interval: When $t > t_0$, all JFETs have a gate-to-source voltage greater than V_{th}, so they all begin to conduct, as indicated by the rise of i_{DC} in Fig. 9.6. The reason for this is that when J_1 reaches threshold, its channel begins to conduct current, causing a small decrease in the J_1 drain voltage. According to the series connection of the JFET leg, the J_1 drain terminal is connected to the J_2 source terminal. Hence, the voltage drop at the J_1 drain terminal raises the J_2 gate voltage relative to the voltage at the J_2 source terminal. This change raises the J_2 gate voltage above threshold and causes J_2 to conduct. The same process continues to propagate very rapidly up the JFET leg in a chain reaction until all JFETs are conducting.

   The freewheeling diode D_f still conducts part of the load current I_o as shown in Fig. 9.5b. Therefore, the voltage across the cascaded switch is V_{DC} and

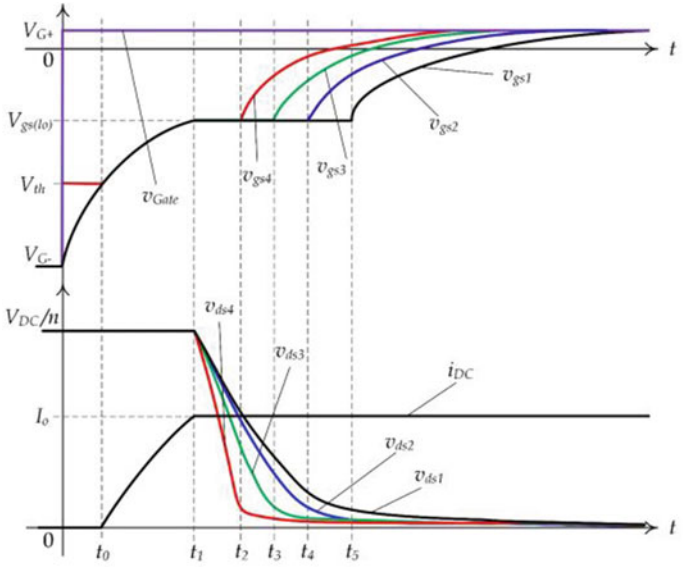

Fig. 9.6 Normally-ON leg theoretical waveforms during the turn-ON transient

across each JFET is $V_{DC}/4$. All JFETs operate in the saturation region since $v_{ds} \geq v_{gs} - V_{th}$. Then, the drain current i_d of each JFET is given by:

$$i_d = g_m \left(v_{gs} - V_{th}\right), \tag{9.2}$$

where g_m is the JFET transconductance. Since all JFETs have the same current $i_d = i_{DC}$, the gate-to-source voltages v_{gs} are equal as seen from (9.2) if all JFETs are considered identical. This interval ends at t_1 when $i_d = I_o$.

3. $[t_1 - t_5]$ interval: v_{Drain} is not clamped to V_{DC} any longer, since D_f is reverse biased and the switch circuit conducts the entire load current I_o, as seen in Fig. 9.5c. The balancing capacitors begin to discharge, increasing the JFET drain currents $i_{d1} - i_{d4}$. The gate-to-source voltages v_{gs} of all JFETs remain almost constant at the plateau level $V_{gs(idx)}$ because the JFETs are in the saturation region ($v_{ds} \geq v_{gs} - V_{th}$). The gate currents $i_{g1} - i_{g4}$ flow entirely through the C_{gd} capacitances because the currents through the C_{gs} capacitances are zero. Therefore, v_{ds1} decreases linearly respect to time as:

$$\frac{dv_{ds1}}{dt} = -\frac{V_{G+} - V_{gs(i_{d1})}}{R_{g1}C_{gd1}}. \tag{9.3}$$

The relationship between the rates of change of the drain-to-source voltages of two consecutive JFETs is found as:

$$\left(C_x + C_{gdx}\right)\frac{dv_{dsx}}{dt} = C_{x-1}\frac{dv_{ds(x-1)}}{dt}, 1 < x \leq n. \tag{9.4}$$

Then, the drain-to-source voltage of a JFET J_x will decrease faster than the drain-to-source voltage of a consecutive lower JFET J_{x-1} if $C_{x-1} > C_x + C_{gdx}$. Under those conditions, J_4 is the first JFET to reach the triode region at t_2 when $v_{ds4} = v_{gs4} - V_{th}$, then J_3 at t_3, J_2 at t_4, and lastly J_1 at t_5. While in the triode region, each JFET is modeled by the ON resistance $R_{ds(ON)}$ connected between the drain and source terminals. Since $R_{ds(ON)}$ is small, the gate current i_g of each JFET can be assumed to flow through the gate resistance R_g in series with the parallel combination of the C_{gs} and C_{gd} capacitances. Therefore, once in the triode region, the v_{gs} voltages of all JFETs will increase with a time constant equal to $R_{gx}(C_{gsx} + C_{gdx})$ where $1 \leq x \leq n$. v_{gs} will increase until reaching V_{G+} for J_1, and zero for $J_2 - J_n$.

4. $[t > t_5]$ interval: This interval starts when J_1 enters the triode region as shown in Fig. 9.5d. At that point, all JFETs are modeled with their ON resistances $R_{ds(ON)}$ between drain and source. The v_{gs} voltage of J_1 starts to rise with the same time constant as $J_2 - J_4$ as shown in Fig. 9.6. The drain to source voltage across each JFET will be the product of I_o and $R_{ds(ON)}$. Then, the cascaded switch is considered to be fully turned ON.

Turn-OFF Transition

1. $[0 - t_0]$ interval: Initially, the cascaded switch is fully ON and is conducting the load current I_o. v_{ds} is zero for all JFETs, and v_{gs} equals V_{G+} for J_1 and zero for $J_2 - J_4$. The turn-OFF transition starts when a negative voltage V_{G-} lower than the threshold voltage V_{th} is applied between the *Gate* and *Source* terminals of the cascaded switch as shown in Fig. 9.7a. Since v_{ds1} equals zero, the gate current of J_1 (i_{g1}) flows through the parallel combination of C_{gs1} and C_{gd1}. The gate-source voltage of J_1 (v_{gs1}) is found as:

$$v_{gs1} = V_{G-} + (V_{G+} - V_{G-})\, e^{-t/R_{g1}(C_{gs1}+C_{gd1})}. \tag{9.5}$$

As time increases, v_{gs1} decays exponentially as seen in Fig. 9.8 until, at time t_0, a constant voltage level equal to $V_{gs(Io)}$ is reached as J_1 enters the saturation region ($v_{gs} \leq v_{ds} + V_{th}$).

2. $[t_0 - t_1]$ interval: At the beginning, J_1 is the only JFET operating in the saturation region while the others remain in the triode region. i_{g1} keeps constant and conducts through C_{gd1} since v_{gs1} keeps constant at $V_{gs(Io)}$ as shown in Fig. 9.7b. Therefore, v_{ds1} increases linearly with respect to time as:

$$\frac{dv_{ds1}}{dt} = \frac{I_o/g_m + V_{th} - V_{G-}}{R_{g1}C_{dg1}}, \quad t_0 \leq t \leq t_n. \tag{9.6}$$

As v_{ds1} rises, the gate-to-source voltages of $J_2 - J_4$ decrease as the gate currents $i_{g2} - i_{g4}$ flow through the parallel combination of C_{gs} and C_{gd} of each JFET and the balancing capacitors $C_1 - C_4$. v_{gs} of the JFET next to J_1 decreases at higher speeds than v_{gs} for the JFETs farther from J_1. This interval ends at t_1, when v_{gs2} equals $V_{gs(Io)}$ and J_2 begins operating in the saturation region.

3. $[t_1 - t_2]$ interval: In this interval, J_1 and J_2 operate in the saturation region, as shown in the equivalent circuit of Fig. 9.7c. The gate current of J_2 (i_{g2}) flows only through C_{gd2}, since v_{gs2} equals $V_{gs(Io)}$. v_{ds2} increases at a rate that can be approximated to be proportional to the rate of v_{ds1}:

$$\frac{dv_{ds2}}{dt} = \frac{C_1\frac{dv_{ds1}}{dt} - C_2\frac{dv_{gs3}}{dt}}{C_{gd2} + C_2} \approx \frac{C_1}{C_2 + C_{gd2}}\frac{dv_{ds1}}{dt}. \tag{9.7}$$

While v_{ds1} and v_{ds2} increase, v_{gs3} and v_{gs4} continue to decrease. This interval ends at t_2, when v_{gs3} equals $V_{gs(Io)}$ and J_3 enters the saturation region.

4. $[t_2 - t_3]$ interval: As shown in Fig. 9.7d, J_3 enters the saturation region at t_2, so v_{ds3} starts to rise at a rate approximately proportional to the rate of v_{ds2}:

$$\frac{dv_{ds3}}{dt} = \frac{C_2\frac{dv_{ds2}}{dt} - C_3\frac{dv_{gs4}}{dt}}{C_{gd3} + C_3} \approx \frac{C_2}{C_3 + C_{gd3}}\frac{dv_{ds2}}{dt}. \tag{9.8}$$

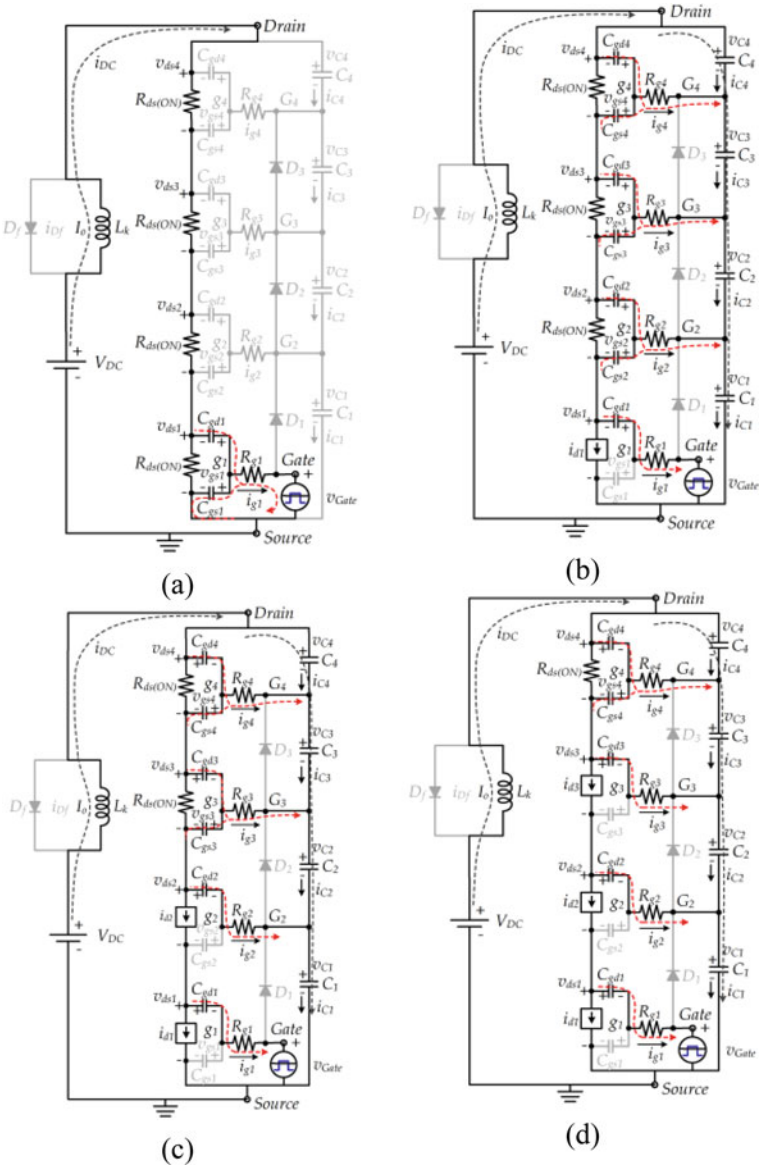

Fig. 9.7 Equivalent circuits during the turn-OFF transient for (**a**) $[0 - t_0]$ interval, (**b**) $[t_0 - t_1]$ interval, (**c**) $[t_1 - t_2]$ interval, and (**d**) $[t_2 - t_3]$ interval

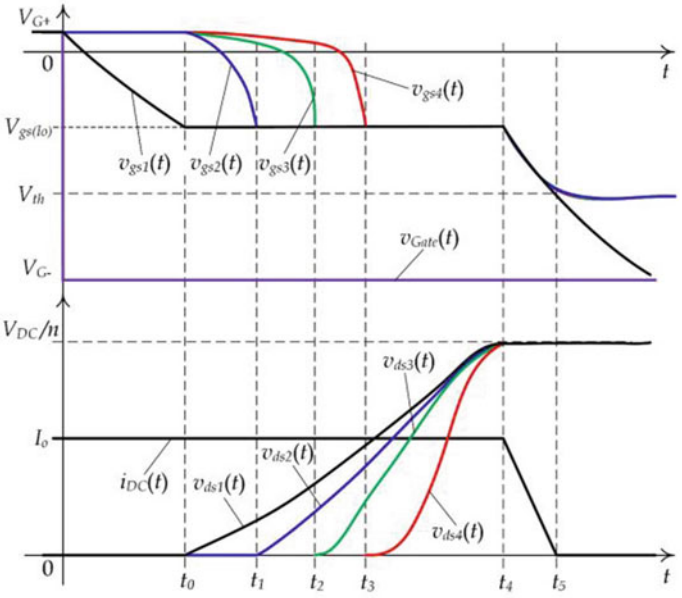

Fig. 9.8 Normally-ON leg theoretical waveforms during the turn-OFF transient

As v_{ds3} increases, v_{gs4} decreases until v_{gs4} equals $V_{gs(Io)}$, when J_4 enters the saturation region.

5. $[t_3 - t_4]$ interval: In this interval, all JFETs operate in the saturation region with their v_{gs} voltages clamped to $V_{gs(Io)}$, as shown in Fig. 9.8. The v_{ds} voltages of all JFETs increase linearly with respect to time as in (9.6) until reaching V_{DC}/n at t_4.
6. $[t > t_4]$ interval: D_f starts conducting, clamping the voltage across the cascaded switch at V_{DC}. The current through the diode i_{Df} increases while the v_{gs} voltages of the JFETs decrease. At t_5, the v_{gs} voltages of the JFETs reach the threshold voltage V_{th} and the cascaded switch current i_{DC} falls to zero. After t_5, $v_{gs2} - v_{gs4}$ remain close to V_{th}, while v_{gs1} continues decreasing until V_{G-} is reached.

Selection of Balancing Resistors

Resistors $R_1 - R_{n+1}$ form the resistive balancing network, the main objective of which is to maintain a stable and evenly distributed voltage across each JFET, particularly during the OFF state. Voltage mismatches can occur in serial connection of devices due to parasitic resistances and parasitic capacitances that cannot be completely controlled during device manufacturing. Additionally, the resistive balancing circuit between the gate terminals of the cascaded JFETs is subject to further voltage imbalances due to gate leakage currents.

R_1 to R_{n+1} are carefully calculated to maintain a stable DC voltage across the JFETs. The steady-state voltages across the resistors when the cascaded switch is

OFF can be calculated from Fig. 9.4. For example, the voltages across the resistors of the left leg, $v_{R1} - v_{R[n/2]+1}$, are expressed as:

$$v_{Rx} = \begin{cases} v_{\mathrm{G}_2}, & x = 1, \\ v_{\mathrm{G}_{2x}} - v_{\mathrm{G}_{2(x-1)}}, & 2 \le x \le [n/2], \\ V_{\mathrm{DC}} - v_{\mathrm{G}_2[n/2]}, & x = [n/2] + 1 \end{cases} \tag{9.9}$$

The voltages across the resistors of the right leg, $v_{R[n/2]+2} - v_{R_{n+1}}$, are:

$$v_{R[\frac{n}{2}]+1+x} = \begin{cases} v_{\mathrm{G}_3}, & x = 1, \\ v_{\mathrm{G}_{2x+1}} - v_{\mathrm{G}_{2x-1}}, & 2 \le x \le [(n-1)/2], \\ V_{\mathrm{DC}} - v_{\mathrm{G}_{2[(n+1)/2]-1}}, & x = [(n-1)/2] + 1. \end{cases} \tag{9.10}$$

The gate voltages v_{G} in (9.9) and (9.10) are calculated by neglecting the gate resistances R_{g} and assuming that V_{DC} is perfectly distributed across the JFETs as:

$$v_{\mathrm{G}x} = \begin{cases} v_{\mathrm{G}-}, & x = 1, \\ \frac{x-1}{n} V_{\mathrm{DC}} + V_{\mathrm{th}}, & 1 < x \le n. \end{cases} \tag{9.11}$$

The power P dissipated in the balancing resistors can be approximated by assuming the gate leakage currents are zero:

$$P = \sum_{i=1}^{n+1} v_{Ri}\, i_{Ri} \approx \sum_{i=1}^{n+1} v_{Ri}\, I_R = 2V_{\mathrm{DC}}\, I_R. \tag{9.12}$$

Based on the desired maximum power dissipation for the balancing network $P_{\max}$, the balancing resistor currents are calculated as:

$$I_R \simeq \frac{P_{\max}}{2V_{\mathrm{DC}}}. \tag{9.13}$$

The ideal balancing resistors are obtained with the following equation, applying (9.9), (9.10), and (9.13) as:

$$R_x = \frac{v_{Rx}}{I_R}, \quad 1 \le x \le n+1. \tag{9.14}$$

After the ideal resistors are obtained, the balancing performance can be evaluated by comparing the ideal voltages, v_R from (9.9) and (9.10), with the real ones, v_R^*, which are obtained from simulations or experimental results. If needed, the balancing performance can be improved by including the effect of the leakage currents, which can be estimated by using the real balancing resistor voltages. The leakage currents can be calculated as:

$$i_{g(2x)} = \frac{v^*_{R_{(x+1)}}}{R_{(x+1)}} - \frac{v^*_{R_x}}{R_x}, \quad 1 \le x \le [n/2], \tag{9.15}$$

$$i_{g(2x+1)} = \frac{v^*_{R_{[\frac{n}{2}]+2+x}}}{R_{[\frac{n}{2}]+2+x}} - \frac{v^*_{R_{[\frac{n}{2}]+1+x}}}{R_{[\frac{n}{2}]+1+x}}, \quad 1 \le x \le [n/2]. \tag{9.16}$$

where (9.15) gives the leakage currents for the even JFETs and (9.16) gives the leakage currents for the odd JFETs. The balancing resistor currents affected by the leakage currents i^*_R can be calculated using (9.17). Then, the adjusted balancing resistors are obtained as:

$$R^*_x = \frac{v^*_{R_x}}{i^*_{R_x}}, \quad 1 \le x \le n+1. \tag{9.17}$$

Selection of Balancing Capacitors

The dynamic transient of the voltage overshoots can be controlled either actively [7–9] or passively [10, 11]. For the proposed configuration, the balancing capacitors, $C_1 - C_n$, prevent transient over-voltages across the drain-to-source terminals of the JFETs, specially at turn OFF where v_{ds} rises from zero to V_{DC}/n. As seen from Figs. 9.6 and 9.8, the durations of the ON and OFF intervals are determined by the times for J_1 to turn ON and to turn OFF, respectively. Also, the top JFETs transition faster than the bottom JFETs, J_1 being the slowest one. The condition for J_x to transition faster than J_{x-1} can be obtained from (9.4) as:

$$C_{x-1} > C_x + C_{gdx}, \quad 1 < x \le n. \tag{9.18}$$

By substituting (9.18) with all the different cases of x, the relationship between the bottom-most capacitor C_1 and the top-most capacitor C_n can be found as:

$$C_1 > C_n + (n-1)\, C_{gd}, \tag{9.19}$$

where C_{gd} is the average of C_{gd} from 0 V to V_{DC}/n. Once C_1 and C_n are selected, the capacitors $C_2 - C_{n-1}$ are calculated as:

$$C_x = C_{x-1} + \frac{C_1 - C_n}{n-1}, \quad 2 \le x \le n-1. \tag{9.20}$$

The exact capacitor values can be further fine-tuned using simulation and experimental results. An overvoltage across J_x can be corrected by increasing the value of C_x, while an undervoltage can be corrected by decreasing it.

Simulation of Normally-ON Path

The particular case with $V_{DC} = 6$ kV, $I_o = 15$ A, and the SiC JFET UJ3N120035K3S from United SiC [12] is presented. Based on the JFET's voltage rating, $V_{DS} = 1.2$ kV, $n = 8$ is selected for an adequate safety margin for the voltage

Table 9.1 SiC JFET cascaded switch parameters

SiC JFETs		Specifications	
		United SiC − UJ3N120035K3S	
$J_1 - J_8$		BV_{ds}, I_d = 1200V, 46A @ 100 °C	
		C_{iss}, C_{oss}, C_{rss} = 2145, 180, 172pF	
Balancing Resistors	Value (MΩ)	Balancing Capacitors	Value (pF)
R_1	0.7385	C_1	2500
R_2	1.4978	C_2	2100
R_3	1.467	C_3	1800
R_4	1.5778	C_4	1500
R_5	0.77464	C_5	1200
R_6	1.4885	C_6	900
R_7	1.5305	C_7	600
R_8	1.5315	C_8	275
R_9	1.5397		
Gate Resistors		Value (Ω)	
$R_{g1} - R_{g8}$		15	
Avalanche Diodes		Specifications	
$D_1 - D_7$		Vishay − BYG23M-E3/TR3	
		1 kV/1.5 A	

across the devices. The balancing passive network is designed for a total power loss P_{max} = 12 W, which defines the balancing resistor current I_R = 1 mA. Then, the balancing resistors are calculated and adjusted using later-acquired experimental results to include the effect of leakage currents. The implemented balancing resistor values are shown in Table 9.1. The balancing capacitors are calculated using an approximated value C_{gd} which is obtained from [12]. Then, $C_1 > 2.4$ nF should be selected after $C_8 = C_{gd}$ was chosen. C_1 is selected as 2.5 nF, and the capacitors $C_2 - C_7$ are obtained, after some small adjustments were implemented.

SPICE simulations were performed for the cascaded switch of Fig. 9.4, with the parameters of Table 9.1, and in an ideal double-pulse test circuit but with a current source instead of an inductor. Figure 9.9 shows the turn-ON and turn-OFF drain-to-source voltages of $J_1 - J_8$ and the cascaded switch current i_{DC} as functions of time. The graphs indicate that the balancing networks operate successfully in both steady state and during the switching transitions. The total bus voltage V_{DC} is evenly distributed among the drain-to-source voltages of the JFETs. As expected from the analysis described previously, the bottom-most JFET, J_1, is the slowest to transition, while the top JFETs are faster.

Design and Operation of Normally-OFF Path

Use of Photoconductive Switches in Normally-OFF Path

Photoconductive semiconductor switch, or PCSS, research has been ongoing for decades in the USA for various electrical and optical short-pulse applications including high-voltage pulsed-power systems, high-speed imaging, and optical

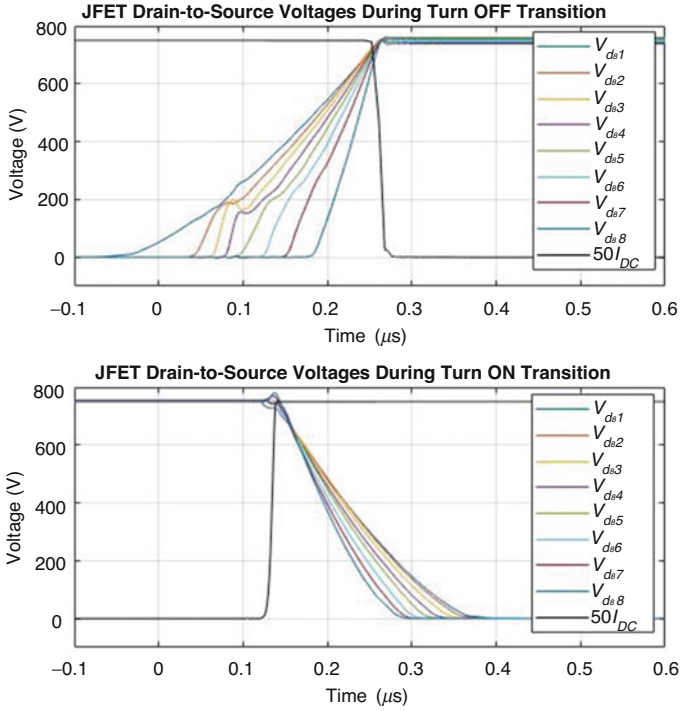

Fig. 9.9 Spice simulation results over an expanded timescale for the drain-to-source voltages and cascaded switch currents during the OFF transition (top) and the ON transition (bottom)

or electrical range sensing. PCSS research has encompassed a wide range of semiconductor materials including silicon (Si), gallium arsenide (GaAs), silicon carbide (SiC), and gallium nitride (GaN) [13–15].

PCSS in GaAs has the capability to operate in two different modes – a linear mode where each photon excites an electron and a linear current is induced in the device, and a non-linear mode where there are much additional electrons excited per photon due to an avalanche-type process in the device. Linear-mode operation occurs in all PCSS semiconductor materials and behaves in a way where uniform current conduction occurs when there is sufficient photon energy injected into the device. The non-linear characteristics have only been seen in specific semiconductors (GaAs), and the device operates such that current conduction persists until the electric field across the device drops to a level where current can no longer be sustained. However, operation of the device in non-linear mode causes current filamentation in the semiconductor, which limits the peak current that these devices can conduct and can force more complex designs for the PCSS to create multiple filaments. The device operates in linear or non-linear mode based on the electric field across the device and the laser fluence used to trigger the device.

Table 9.2 Candidate PCSS materials' bandgap energy and wavelength

Material	Bandgap energy	Bandgap wavelength
Si	1.12 eV	1107 nm
GaAs	1.42 eV	873 nm
SiC	3.26 eV	380 nm
GaN	3.4 eV	364 nm

Table 9.3 Material parameters for candidate PCSS materials [16, 17]

	Critical electric field	Electron saturation velocity	Bandgap
Si	3×10^5 V/cm	1×10^7 cm/sec	1.12 eV
GaAs	5×10^5 V/cm	2×10^7 cm/sec	1.42 eV
SiC	3×10 V/cm	2×10^7 cm/sec	3.26 eV
GaN	3×10^6 V/cm	3×10^7 cm/sec	3.4 eV

Critical electric field values are at 1×10^{16} cm^{-3} doping

With low enough field and fluence, the device operates in linear mode. As they are increased above a certain threshold, the device will begin to operate in the non-linear operating mode. Besides the ability to use short laser pulse widths to trigger longer electrical pulses in non-linear mode, another benefit of non-linear mode is that the device could be switched with sub-bandgap laser energy. Table 9.2 shows PCSS candidate materials' bandgap energies and the corresponding wavelengths. This allows for more laser wavelengths to be utilized on the device. The efficiency of the switch is determined by the operating field vs. remnant field and the laser energy required to turn ON the switch. Non-linear operation of the switches could be more efficient due to the ability to use short pulses (ns) of high-power lasers to conduct current for long periods of time.

After the non-linear operating mode was found in GaAs PCSS devices and PCSS were being evaluated for higher-voltage applications, the use of wide-bandgap materials was an obvious choice for increasing the capability. Wide-bandgap semiconductor devices are more suitable for high voltage applications due to their large bandgap, high breakdown electric field strength, and high electron saturation velocity compared to traditional semiconductors, as shown in Table 9.3. With the advancement in SiC and GaN in recent years for other high-voltage devices, they are options for investigation in PCSS for both linear and non-linear operating regimes. GaN was chosen to be investigated for the DC circuit breaker application as it is a direct-bandgap semiconductor which was thought to be more likely to have non-linear traits as GaAs has been shown to have.

The normally-OFF circuit utilizes a GaN PCSS for its electrical isolation from the control circuitry and fast turn-ON time to divert fault current away from the normally-ON circuit. The operating parameters of concern for the PCSS include hold-OFF voltage, leakage current, laser triggering threshold fluence, turn-ON time, ON-resistance, and current carrying capability. For a 10 kV circuit breaker, a vertical PCSS topology utilizes the GaN material more efficiently by voltage hold-OFF through the bulk of the material. Initial experiments have utilized lateral PCSS

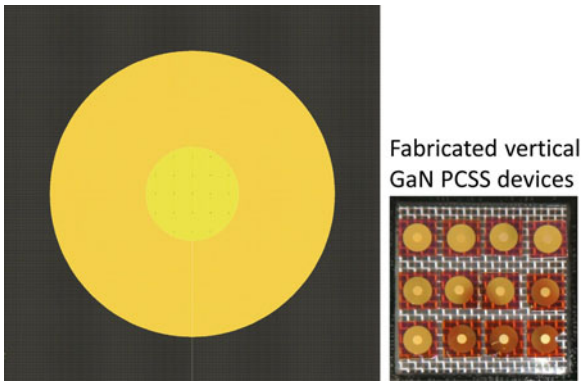

Fig. 9.10 Top view of the GaN PCSS

topologies for their ease of manufacturing, but there would need to be multiple such devices connected in series to meet a 10 kV goal, and with serial connections come difficulties with the laser triggering mechanism for the devices. Additionally, the current filamentation in non-linear PCSS operation with a single filament per PCSS would require parallel devices to meet a 100 A fault current goal, and with the use of vertical devices, there are ways to trigger the device with many parallel filaments to circumvent the need to parallel devices.

Figure 9.10 shows the device fabricated to achieve many parallel filaments. The design requires higher energy lasers in order to create many filaments, and to do this efficiently in the future there would have to be a way to pass laser light into each opening with a vertical-cavity surface-emitting laser (VCSEL) array or similar semiconductor laser generation.

Figure 9.11 shows waveforms from operation of a lateral GaN PCSS device during its initial testing. As shown, this was lower voltage than the circuit breaker's intended operation level because it was utilizing a lateral switch that was only designed to operate at 2 kV. Testing at 1.5 kV helped to understand the operation of the device and determine its linear and non-linear characteristics and where the threshold exists between the two [15]. As noted, the primary types of semiconductor switches being considered for the PCSS-based SSCB are composed of either GaAs or GaN. Both types of switches exhibit a phenomenon termed lock-ON (LO) that enables fast switching. This phenomenon is triggered optically, which leads to rapid growth of photoconductive current that persists in the absence of optical triggering. The interpretation of the phenomenon is that the optical trigger has induced switching from an OFF state to an ON state, and in both cases experiments have guided the development of these switches. The very large currents cause heating at the contacts that leads to destruction of the switch, unless the current source limits the current. Accordingly, much effort has focused on controlling the effects of heating during the ON state.

Theory of PCSS Lock-ON

In these devices, the flow of current can either be along the surface (lateral switch) or perpendicular to the surface (vertical switch). Both lateral and vertical switching has been observed for GaAs. Lateral switching has been observed for GaN, but

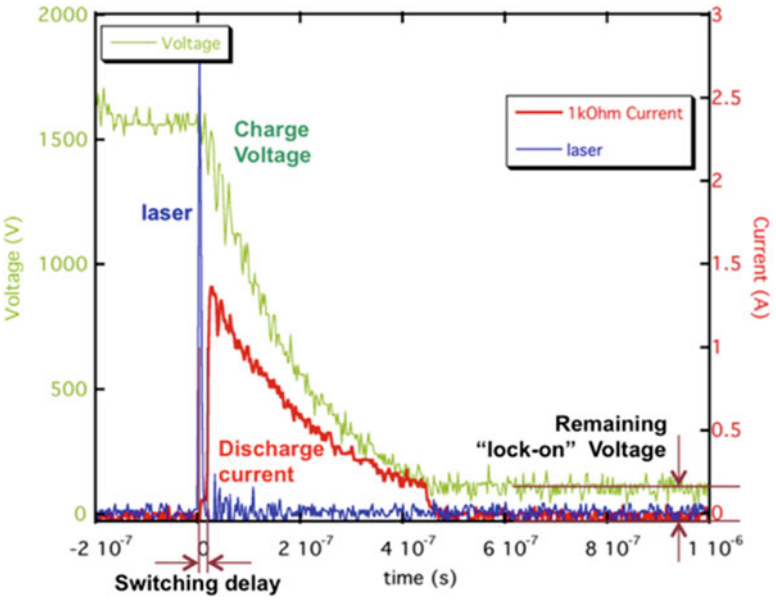

Fig. 9.11 Data from pulsed measurement of lateral PCSS showing laser pulse (blue), voltage from the positive terminal of the PCSS to ground (green), and current through the current viewing resistor (red)

vertical switching has been challenging to verify. For both types of switches, the LO characteristics are similar, and for both cases, the current during LO flows in filaments. Also, the sustaining field during the LO stage is similar, approximately 4 kV/cm for both types of switches. The low field rules out conventional avalanche breakdown as a mechanism. For both materials, the avalanche breakdown field exceeds 1 MV/cm. Thus, alternative mechanisms have been sought.

For GaAs, the presence of a low-energy secondary valley in the conduction band allows a mechanism, collective impact ionization, that can operate at high carrier density. However, this collective effect is not available for GaN because the secondary minimum for GaN lies at an energy that is too high. Thus, the electric field for the collective effect would be much higher than the LO field. The inapplicability of an intrinsic mechanism to GaN has led to consideration of other mechanisms. One alternative mechanism could involve the surface, and another could involve defects. Both types of mechanism are being considered.

The present defect-related model for GaN switches that exhibit LO assumes a large density of acceptor defects within the active region. Electrical transport calculations have shown that a distribution of acceptors can explain both the OFF and ON states of GaN switches. These transport calculations focused on the effects of Mn acceptors. The electronic properties of the Mn defects are obtained via density functional calculations (DFT) using SeqQuest [18]. This software uses

methods that are tailored for the properties of defects in GaAs, GaN, and other III-V semiconductors. The OFF state can be explained by trapping of the injected electrons, and this explanation applies to a switch with n-type contacts. The trapped electron charge will produce a field that will oppose further injection of electrons, and thus the initial capacitive current, which is large, decays and finally becomes negligible. Electrical transport calculations have validated this reasoning. In addition, such calculations have explored the effects expected for a large voltage bias and photo-injection of electrons and holes. These calculations have revealed that if the voltage bias and the photo-injection rate exceed threshold values, a very large current will flow. For this case, the injected electrons become trapped near the anode. Two effects control the current flow. One, the injected electrons create a very large field at the anode. Two, the injected holes recombine with the trapped electrons near the cathode. This eliminates the barrier to injection of electrons, and the large field at the anode, if it exceeds a threshold value, will cause avalanche injection of holes. The combined effects of electron and hole injection at opposite contacts will lead to very large current. This would be the current found in an ON state.

Experiments to characterize the OFF state would measure the photocurrent prior to the transition to the OFF state. The present model suggests that photocurrent will tend to be quenched as the traps near the anode are populated.

Simulation of Normally-OFF Path

A behavioral model of the PCSS devices was created using the SPICE [19] simulation platform. The goal of the model is to replicate, as closely as possible, PCSS behavior through passive lumped circuit components. As such, it is necessary that the model can replicate three key PCSS behaviors:

- Linear mode conduction
- High-gain mode conduction, where the high-gain model is only initiated if a laser is pulsed while a high field is present across the device and conduction ceases once the field is below the lock-ON voltage
- Delay in high-gain mode

The developed PCSS model can replicate these key features of the device. Figure 9.12 shows the PCSS model. The PCSS model is composed of two conduction legs. The first leg replicates linear mode conduction and is composed only of a resistor (R_{linear}) and a switch ($\text{SW}_{\text{linear}}$). The switch is directly controlled by the laser pulse that is typically represented by a voltage pulse of the same duration as that of the physical laser pulse. This linear mode will only conduct if the laser voltage is above some voltage threshold. The second leg replicates the high-gain mode conduction. This leg is composed of a variable resistor (R_{highgain}) in parallel with a simple resistance representing a parallel conduction pathway (R_{shunt}). These two resistors are in series with two switches ($\text{SW}_{\text{highgain1}}$ and $\text{SW}_{\text{highgain2}}$).

In the high-gain conduction mode leg, the combination of switches is used to replicate the latching and hysteresis behavior demonstrated by an actual PCSS. The first switch ($\text{SW}_{\text{highgain1}}$) replicates latching behavior with delay of the PCSS device. It is closed after some time, t_{delay}, after the laser pulse. This switch remains

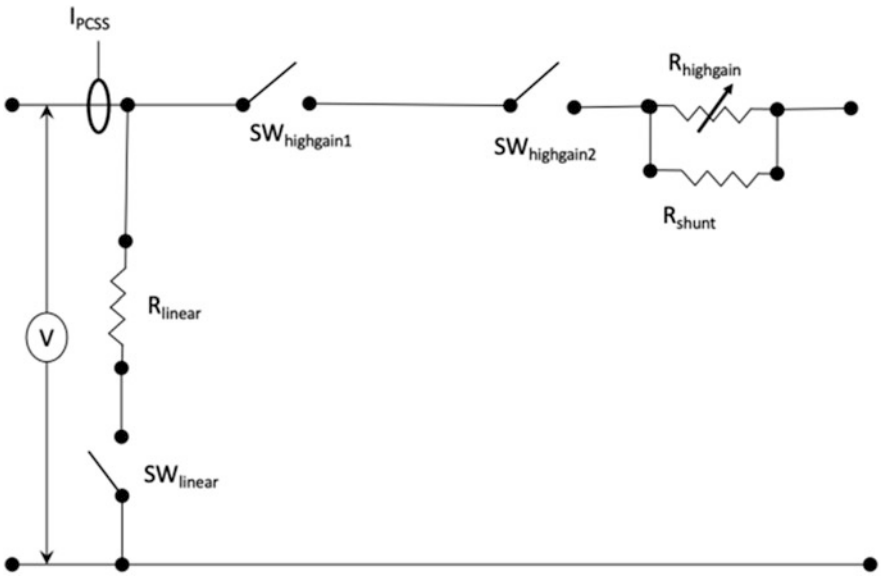

Fig. 9.12 Diagram of PCSS equivalent model

activated after the laser turns OFF. In SPICE formulation, this latching behavior is typically modeled using a large capacitor as a voltage reservoir. This switch has a built-in buffer that replicates the time delay in high-gain mode conduction that is a function of laser pulse energy as well as applied voltage across the device. The second switch ($SW_{highgain2}$) is incorporated to replicate the hysteresis behavior of high gain made. The switch turns ON when the voltage at the positive terminal of the PCSS (denoted by V in Fig. 9.12) is greater than a threshold voltage (V_{th}) and turns OFF when the voltage is below some lock-ON voltage (V_{lo}) required to maintain high-gain conduction. Other than the two switches, the high-gain leg is composed of a variable resistor ($R_{highgain}$) with a parallel conduction pathway (R_{shunt}). The variable resistor attempts to maintain voltage across the PCSS at V_{lo}. The parallel conduction pathway ensures that the variable resistor cannot become arbitrarily small. Without this parallel conduction pathway, $R_{highgain}$ can keep the voltage across the PCSS at V_{lo} indefinitely (and thus, never stop conducting).

The actual SPICE implementation of the PCSS device is shown in Fig. 9.13. The three switches in the SPICE model are controlled by voltage sources. The linear leg switch (*SW_linear*) is controlled by the laser pulse. The first switch in the high-gain leg (*SW_highgain1*) incorporates latching behavior as well as time delay. The time delay is enabled by the digital buffer, denoted as Delay. The latching behavior is enabled through a diode (*D1*) and capacitor (*C1*) as a voltage reservoir. The laser voltage pulse will charge the capacitor, which will remain charged, holding *SW_highgain1* closed. The diode is present to prevent discharge of the capacitor reservoir, *C1*, through the linear side leg. The second switch in

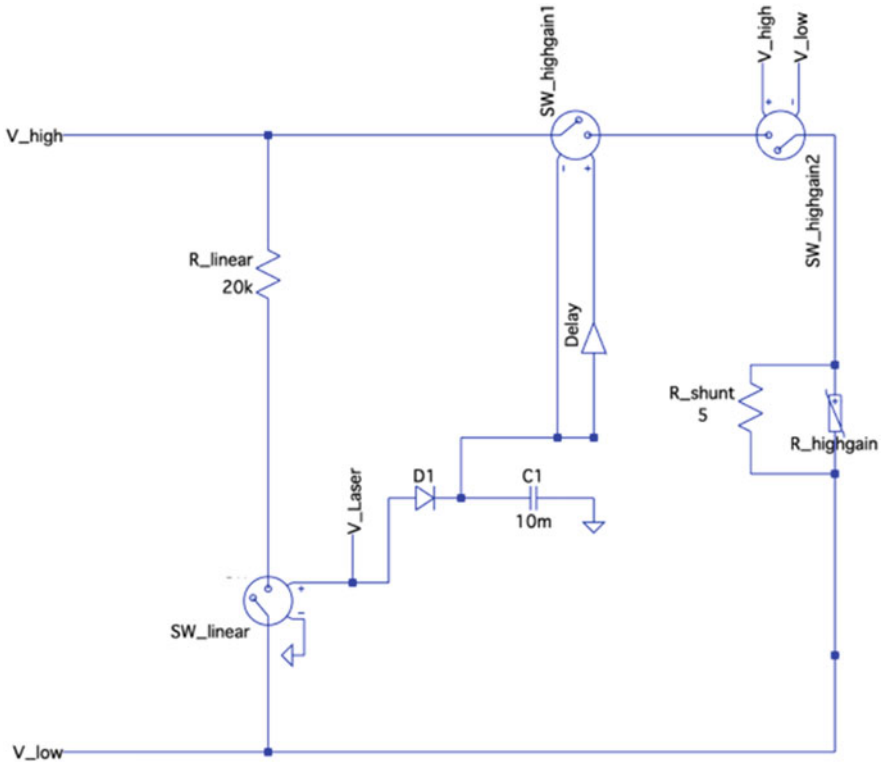

Fig. 9.13 Close-up of PCSS circuit model showing two parallel conduction pathways of the PCSS

the high gain leg, *SW_highgain2*, incorporates the hysteretic behavior through the switch model, *SW3*. This switch model is controlled to turn ON and OFF by high and low voltages, V_{th} and V_{lo}, respectively. The variable resistor, *R_highgain*, is a varistor model controlled by a voltage source, *V1*. In this case, the varistor will change its impedance to maintain a set voltage drop, determined by *V1*. In parallel with the varistor is a shunt resistor, *R_shunt*, that has a value of 5 ohms.

The PCSS model described above was utilized to fit the experimental data described in [20] for an underdamped pulse line measurement of a lateral PCSS device. The experimental current and voltage traces were shown previously in Fig. 9.11.

Figure 9.14 shows the simulated voltage (left) and current (right) traces compared to the experimental data. The simulated vs. experimental behavior matches well and shows the high-gain conduction mode. The simulated PCSS circuit accurately captures the variable resistance portion of the high-gain conduction and the shut-OFF behavior once the applied voltage decreases below V_{lo}. Further detail of the transition between linear conduction and high-gain mode delay is shown in the close-up in Fig. 9.15.

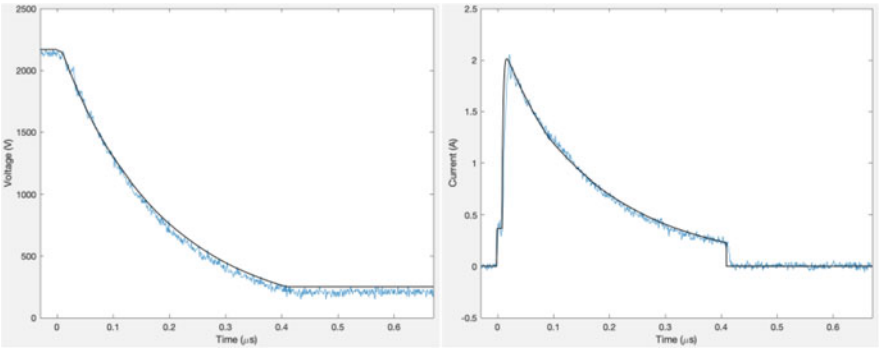

Fig. 9.14 (left) Simulated (black) and measured (blue) voltage from the PCSS positive terminal to ground showing the effect of high-gain model delay, the high-gain mode variable resistance, and the lock-ON state reached. (right) Simulated (black) and measured (blue) current through the PCSS device showing the high-gain mode variable resistance and the shut-OFF once the voltage reaches the lock-ON voltage

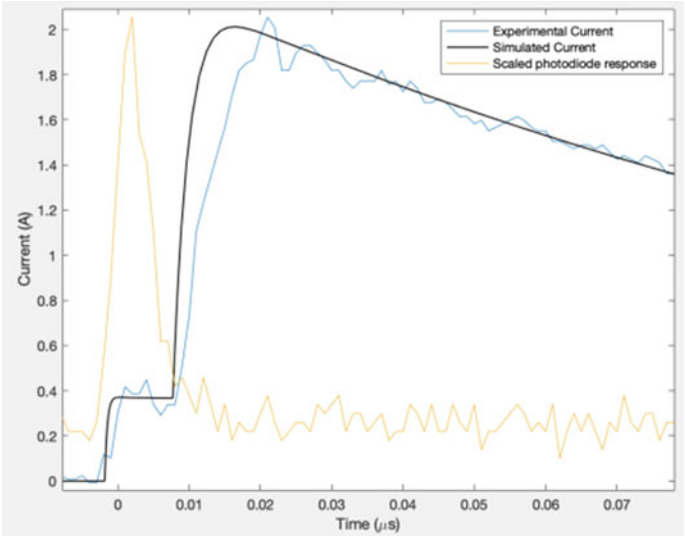

Fig. 9.15 Close-up view of the simulated (black) and measured (blue) current through the load resistor with the photodiode response (yellow). The model accurately describes the linear mode behavior as well as the delay in high-gain conduction

Since the applied voltage is greater than the threshold voltage to cause high-gain mode conduction, switch *SW_highgain2* is ON. At time zero, the laser pulse is activated. This causes the linear mode switch (*SW_linear*) to turn ON and the linear mode to start conducting. As this linear mode pathway is highly resistive, the current only rises to ~0.1 A. After a delay of 9 ns, the latching high gain mode switch (*SW_highgain1*) activates and the current rises due to high-gain mode conduction.

During high-gain mode conduction, the varistor value varies over time. When the voltage across the device reaches the low voltage threshold, *SW_highgain2* shuts OFF and conduction stops.

The PCSS model fits the experimental data well and can replicate the behavior of the PCSS switch. This includes both linear and high-gain conduction modes, latching and delay behavior of high-gain conduction, variable resistance in high-gain mode, and hysteresis in turn-ON/turn-OFF.

4 System Simulation and Optimization

To evaluate the DC breaker response in a system and evaluate breaker behavior as a function of both system configuration (length of lines, load type, etc.) and breaker configuration (capacitance, control scheme, etc.), a full model of the normally-on path (cascaded JFET switch) as well as the normally-OFF path (PCSS) was created. These individual models were validated against experimental data. The operation of the combined normally-ON and normally-OFF paths was then evaluated in parameterized studies of different DC systems and compared to experimental laboratory testing.

An integrated system model was assembled in SPICE using circuit models for the normally-ON path cascaded JFET design and PCSS shunt circuit described previously (Fig. 9.16). The DC circuit breaker device was inserted into the system with a DC voltage source, MVDC cable length, and load. The MVDC cable is modeled using a classical lumped parameter π- equivalent model based on 10 kV HVDC cabling [21]. The load is modeled using resistive (R), inductive (L), and capacitive (C) elements with a flyback diode. A low impedance fault (R_fault) is controlled by a switch (SW_fault). The current model is configured to evaluate a nominally 1700 V system.

For preliminary system simulations, the nominal DC bus voltage is 1.8 kV, the input line length is 1 m, the shunt capacitor value is 0.1 μF, and the load inductance and capacitance are 100 μH and 100 μF, respectively. The fault impedance is varied from 1 mΩ to 100 Ω and is initiated at a simulation time of 7 μs. The JFET stack is triggered at 7.2 μs, and the PCSS is turned ON at 7.4 μs. Results for these simulations are shown in Fig. 9.17. The initiation of the fault significantly increases JFET current (green). The turn-ON of the PCSS leg decreases the current through the JFET leg. However, the fault impedance has a direct relationship to the PCSS turn-ON state, since it changes the voltage profile in time across the PCSS, and hence the time that high-gain conduction mode begins.

The model in Fig. 9.16 for a 1.2 kV_{DC} breaker was used to predict the sensitivity of the system performance to variations in transmission line length, load power, shunt capacitance value, and other system parameters for a fault event. In particular, the system was simulated for several values of each parameter of interest in the system, and the peak voltage transient and energy dissipation in the switches were computed in each permutation.

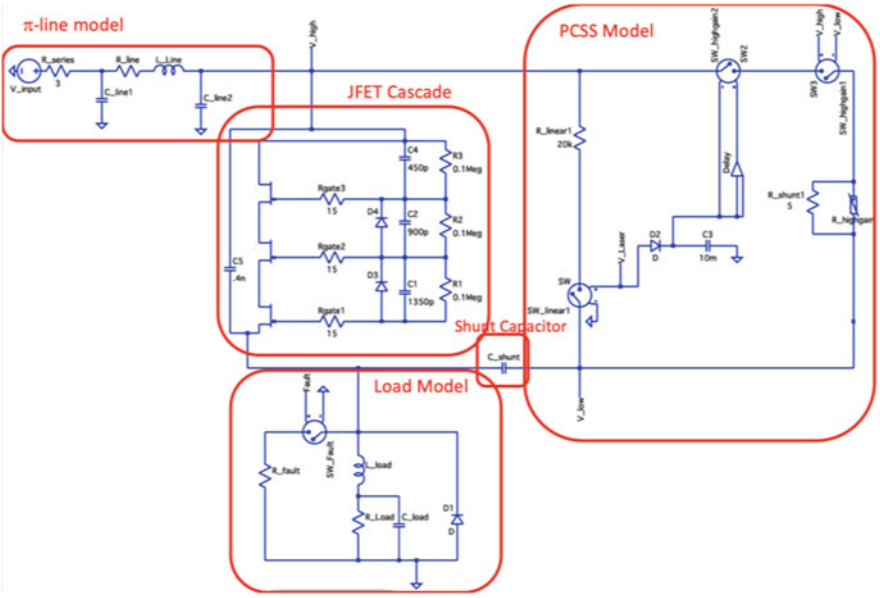

Fig. 9.16 Integrated Circuit Model of breaker with principal components labeled

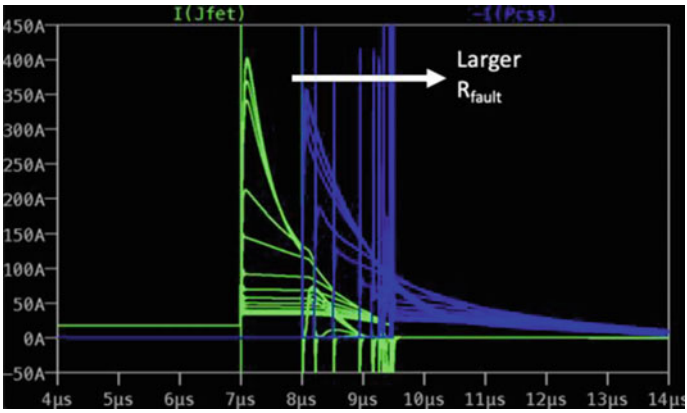

Fig. 9.17 JFET current (green) and PCSS current (blue) during fault event for fault impedances from 0.001 to 100 Ω

Figure 9.18 shows a two-dimensional sensitivity analysis for load impedances from 100 to 1800 Ω (y-axis) and line lengths from 0.01 to 1000 km (x-axis). The numbers in the matrix indicate the total energy loss in the Breaker (JFET and PCSS legs) in Joules. The red numbers indicate higher values, while blue numbers indicate lower values. The treatment shows quite clearly that load impedance does not affect the energy dissipation through the Breaker. This is because, during the fault event, the system is dominated by the fault impedance rather than the load impedance.

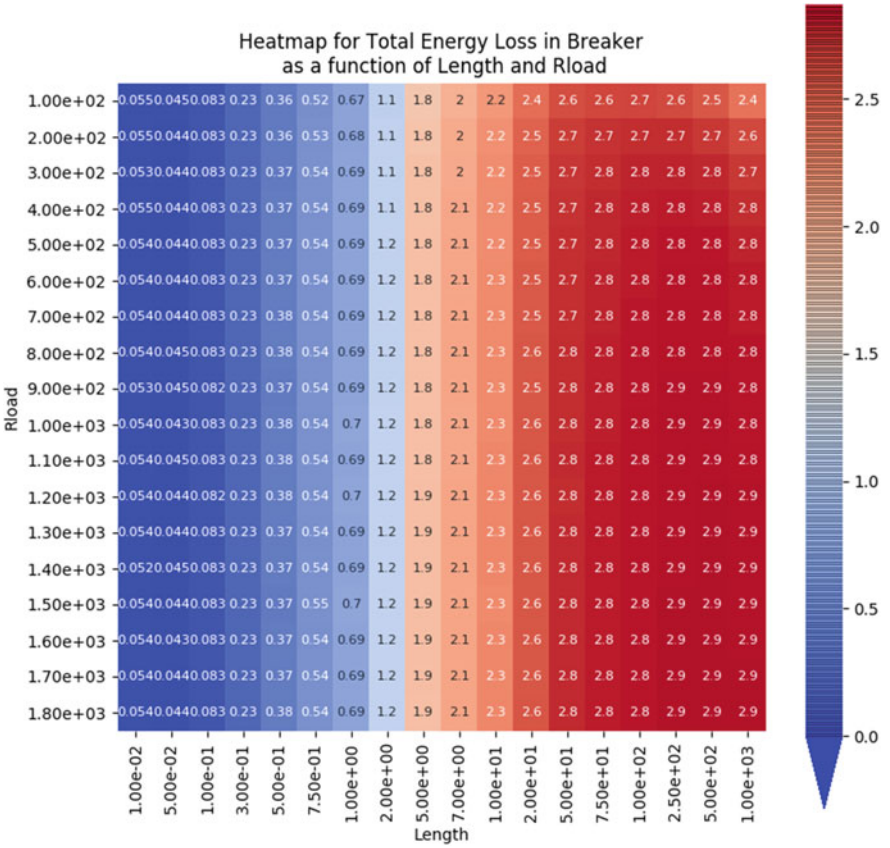

Fig. 9.18 Two-dimensional heat map for Breaker operation of fault event for different load impedances (*y*-axis) and line lengths (*x*-axis). The numbers indicate energy in joules dissipated by the Breaker during the fault event

Additionally, there is no dependence on the load capacitance or inductance. Energy dissipation through the Breaker increases with line length. This is due to the line storing charge, which dissipates through the Breaker. Long lines store greater charge, which results in a larger energy dissipation.

Figure 9.19 shows a two-dimensional sensitivity analysis for input voltages from 500 V to 2.2 kV (*y*-axis) and fault impedances from 1 mΩ to 100 Ω (*x*-axis). The energy dissipated in the Breaker depends on both the input voltage and the fault impedance. The energy dissipated scales inversely with fault impedance since lower impedance faults will increase the fault current flowing through the breaker device that it must arrest. As input voltage increases, the energy dissipated in the Breaker also increases. This is to be expected for an infinite-bus approximation where the bus voltage does not collapse in the presence of a fault but is able to source enough current to feed the fault and keep the voltage at some nominal value. For a

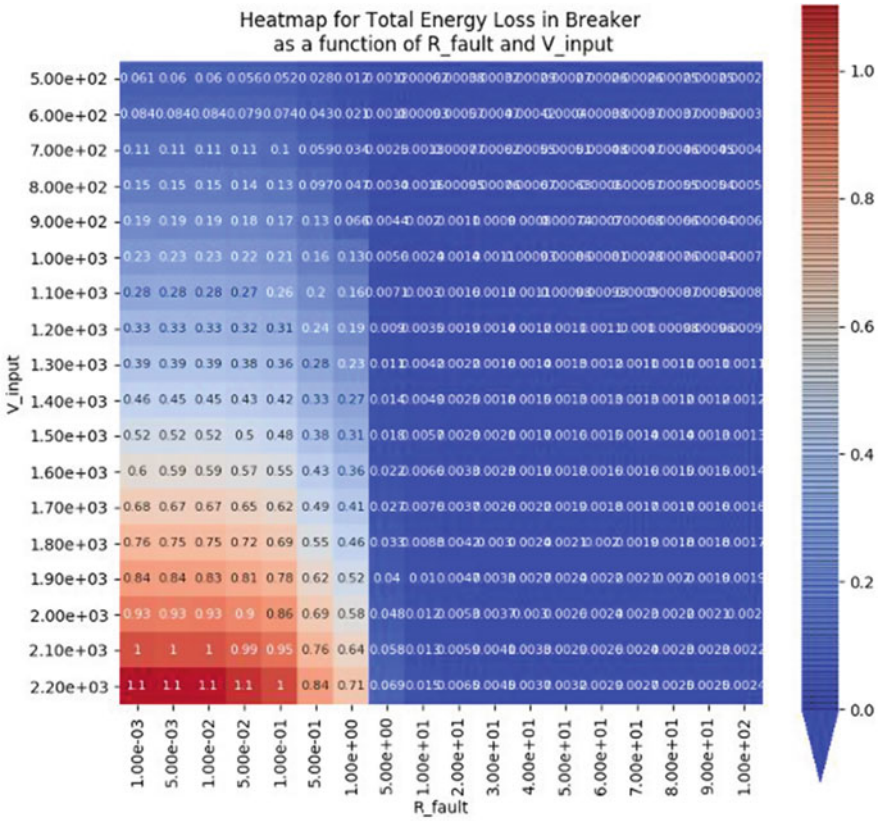

Fig. 9.19 Two-dimensional heat map for Breaker operation of fault event for different system voltages (*y*-axis) and fault impedances (*x*-axis). The numbers indicate energy in joules dissipated by the Breaker during the fault event

non-infinite bus, low fault impedances will tend to drive the bus voltage to zero, which will decrease energy dissipation in the breaker to give a more complicated relationship between input voltage, fault impedance, and energy dissipation.

In general, as the shunt capacitor value increases, the turn-OFF time of the PCSS leg will increase (Fig. 9.20), which increases energy dissipation. The key to shunt capacitor sizing is to choose a capacitance that is large enough such that the PCSS remains on until the JFET leg is completely OFF, but not so long that it is ON for excessive lengths of time after the JFET leg is OFF (and thus conducting fault current during that time). Nonlinearity is introduced in the energy dissipation due to voltage oscillations during the turn-OFF phase. The time period of oscillations varies according to the capacitance value, which can affect the calculation of energy dissipation.

Temperature rise in the junction of the normally-ON path's JFETs will most likely be the limiting mechanism determining the operational envelope of the SSCB

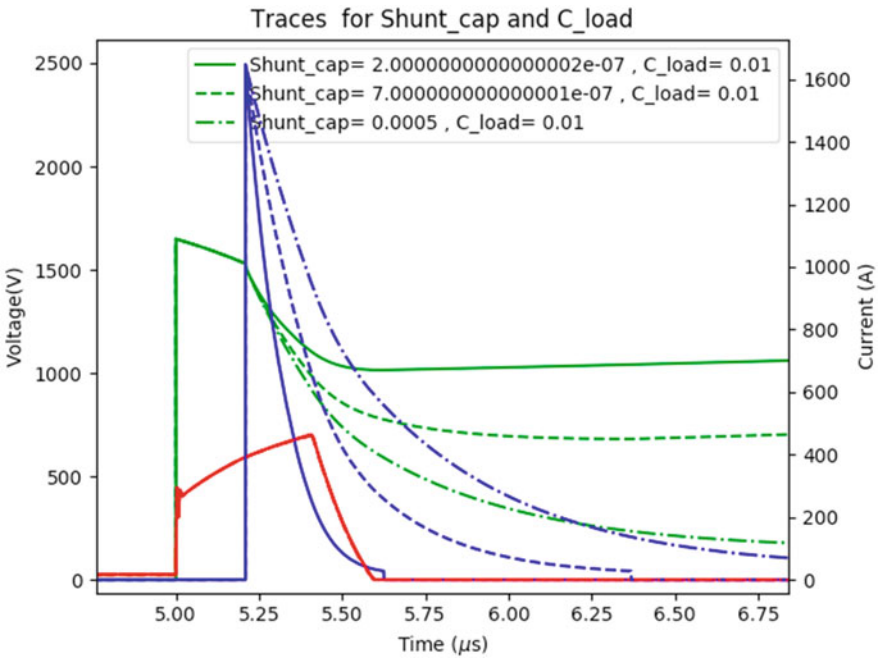

Fig. 9.20 Voltage (green) across the Breaker and current through the JFET leg (red) and PCSS leg (blue) for different shunt capacitor values of 0.2 μF, 0.7 μF, and 0.5 mF

device. To more accurately determine this envelope, simulations where carried out where the worst-case internal temperature of the JFET was estimated. This required simulations where the voltage/current profiles for each JFET were tracked and their internal temperatures estimated for both steady-state operation as well as during the fault event. This process is used to determine the time that a fault must be detected and the JFET leg triggered in order to keep the JFETs within temperature specifications.

For the purposes of analytical calculation, a square wave current profile during the fault is assumed, as shown in Fig. 9.21. It is further assumed that the resistance of the SSCB device is negligible compared to R_{load} during steady state ($V_{\text{BREAKER}} \sim 0$) and during the fault state, the fault resistance (R_{fault}) is negligible compared to the breaker resistance so that $V_{\text{BREAKER}} \sim V_{\text{bus}}$. Using this sequence with the stated assumptions, we can calculate an estimate of the time required to turn OFF the JFET (t_{fault}) to keep the junction temperature below a target. In this case, the temperature rise for a JFET is a combination of the ambient temperature rise, the temperature rise from the steady-state condition, and the transient temperature rise from the fault condition. Using the steady-state and transient thermal resistances, the junction temperature rise can be calculated using (9.21).

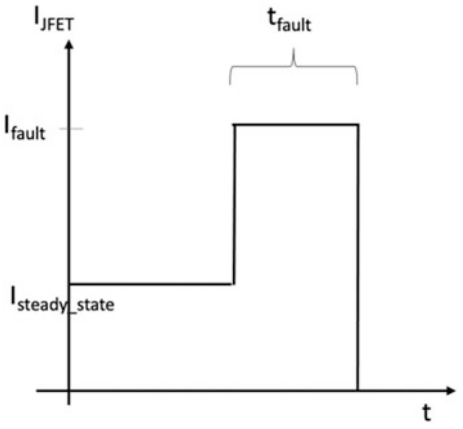

Fig. 9.21 Current profile for a fault event. The time required to turn OFF the JFET cascade (t_{fault}) can be determined so that the junction temperature of the JFET is below T_{jrated}

$$T_{\text{JFET}} = T_{\text{ambient}} + P_{\text{steady\_state}} \bullet R_{\text{th}}^{\text{steady}_{\text{state}}} + P_{\text{fault}} \bullet R_{\text{th}}^{\text{fault}} \tag{9.21}$$

$$P_{\text{steady\_state}} = \frac{{V_{\text{bus}}}^2}{R_{\text{load}}}$$

$$R_{\text{th}}^{\text{fault}} = 0.001 \bullet \sqrt{\frac{t_{\text{fault}}}{1e^{-6}}} \text{ from [22]}$$

$$R_{\text{th}}^{\text{steady}_{\text{state}}} = 0.35°\text{C/W} \text{ from [12]}$$

$$P_{\text{fault}} = {I_{\text{fault}}}^2 \bullet R_{\text{JFET}} = \left(\frac{V_{\text{bus}}}{R_{\text{fault}}}\right)^2 \bullet \frac{0.35 \bullet S}{N}$$

where S is the number of JFETs in series and N are the number of stacks in parallel [22].

The envelope of response time for the JFET cascade can be solved by substitution and rearrangement of (9.21) to give (9.22):

$$t_{\text{fault}} = 1\text{e}^{-6} \bullet \left(\frac{N \bullet R_{\text{fault}}^2 \bullet \left(175 - 35 - \frac{0.35 \bullet {V_{\text{bus}}}^2}{R_{\text{load}}}\right)}{35\text{e}^{-3} \bullet S \bullet V_{\text{bus}}^2 \bullet 0.001}\right)^2 \tag{9.22}$$

To evaluate this analytic envelope compared to detailed simulation, a series of simulations for the 10 kV breaker operation was carried out. The breaker system is composed of a 10 kV source followed by a distributed π-line model to emulate a 10

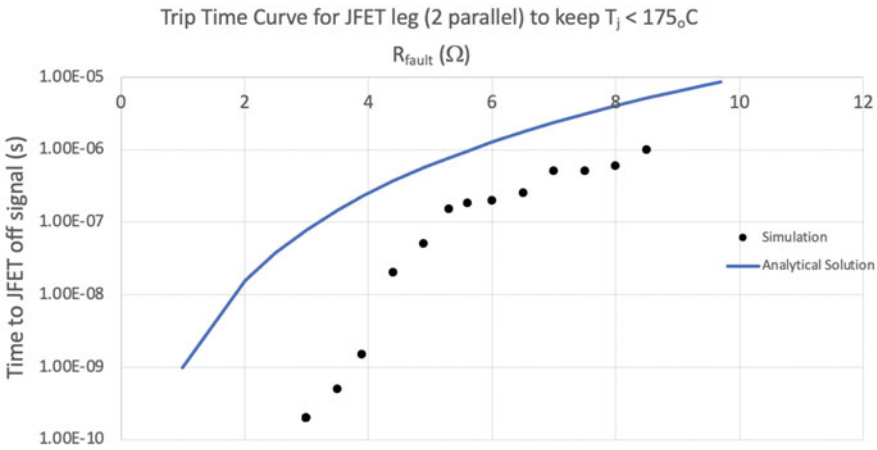

Fig. 9.22 Required time response vs. fault resistance calculated by (9.21) (blue curve), and derived via simulation for full stack paralleling ($N = 2$, black dots) of the JFET cascade. Full stack paralleling with an extra parallel switch for the bottom JFET is represented by gray dots

kV transmission line [23]. The JFET stack of 8 devices in series (S) and two stacks in parallel (N) composes the normally-ON leg while the PCSS model is the normally-OFF leg. Finally, the load is an RLC load. A pure resistance fault is initiated at the load. The fault is initiated at 5 μs (t). The time to trigger the JFET leg ($t + t_{fault}$) is varied and the fault is detected and the PCSS is triggered at $t + 0.5*t_{fault}$.

The results of the analytical calculation of the required fault time and the simulation results are shown in Fig. 9.22. As would be expected, the larger the fault resistance, the greater the time allowed to arrest the fault (due to the correspondingly lower fault current). Very low impedance faults require very short durations (~ns) to keep the junction temperature of the JFETs within specifications. The maximum junction temperature of the JFET stack calculated through circuit simulation is shown by the black dots. In all cases, the simulation shows a smaller required fault time than would be expected from (9.21). This deviation between the analytical solution and the simulation is primarily due to two reasons. The first is that there is a non-uniform temperature distribution between the JFETs in the cascade. The JFET stack turns OFF in a cascaded manner so that the JFET at the top of the stack fully turns OFF before the lower JFETs. This means that the bottom JFET in each stack sees higher stress and higher junction temperatures than the JFETs at the top of the stack. In some cases, this deviation in junction temperatures may be as much as 20%. This is not replicated in the analytical solution, which assumes equal temperature distributions along the JFET stack. The second reason for the deviation is that some of the assumptions used in the analytical expression do not hold during the transient fault period, namely, that the JFET junction resistance is constant. During the transient periods, the junction resistance of the JFETs increases above the nominal datasheet value (35 mΩ [12]).

5 Hardware Realization and Characterization

Normally-ON Path

To validate the dynamic and steady-state balancing of the cascaded JFET switch in a DC circuit breaker operation, a 6 kV prototype was developed by cascading 1.2 kV, 35 mΩ SiC JFETs from UnitedSiC, UJ3N120035K3S [12]. The same circuit configuration shown in Fig. 9.4 with eight JFETs was used for the hardware prototype development. Extensive circuit breaker experiments have been performed to analyze and validate the proposed cascaded JFET topology's operational schemes. The cascaded switch prototype shown in Fig. 9.23 is connected in series with the high-voltage/high-current terminals of a testing enclosure and with a resistive load to simulate a fault condition.

The steady-state balancing of the cascaded JFETs across a wide range of blocking voltages has been evaluated by measuring the voltage balancing on each JFET device. Figure 9.24 shows the voltage stress across the drain-to-source V_{ds} on each device over different applied voltages. The total blocking voltage ranging from 500 V to 6 kV with an increment of 500 V can be seen to be evenly distributed across the eight FETs, plotted with a cluster of data points. Comparing the experimental data against the ideal case plotted with a dashed line in Fig. 9.24, it is clear that an even distribution of the bus voltage is observed across the JFETs with only a minor divergence.

Furthermore, the dynamic balancing behavior of the cascaded JFET switch has been experimentally evaluated. Figure 9.25a shows the breaker voltage and current waveforms during a turn-OFF transition. It shows the circuit breaker's operation at 6 kV with different current levels. Figure 9.25b depicts the circuit breaker voltage and current waveforms during a turn-ON transition. The load current was varied to

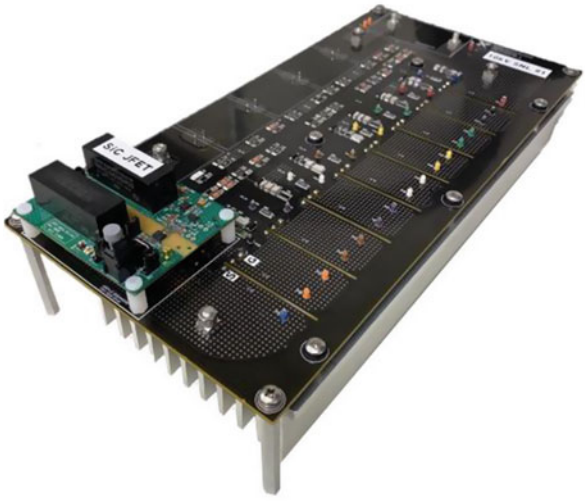

Fig. 9.23 Photo of the developed 6kV SiC JFET cascaded switch

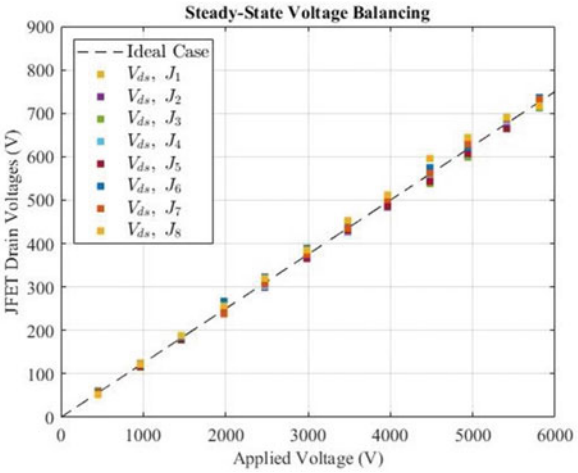

Fig. 9.24 Drain-to-source voltage distribution with V_{DC} up 6kV

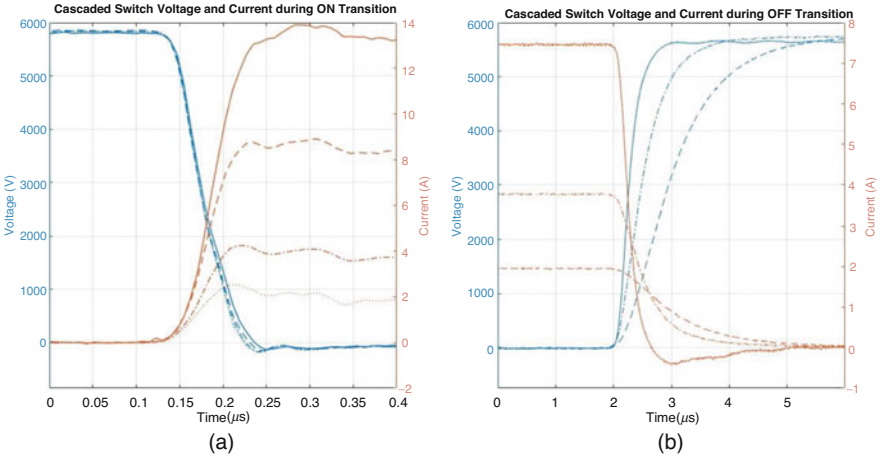

Fig. 9.25 Breaker voltage and current experimental waveforms at different levels of load current during (**a**) the turn-OFF transition, and (**b**) the turn-ON transition

examine the breaker's behavior at different operating conditions. One observation made from the resistive load switch tests was the impact of the switch's turn-ON and turn-OFF times at different load conditions. It can be seen that the higher the load current, the faster the turn-OFF time due to the rapid charging of the output capacitances of the devices and the lower plateau voltage. However, the turn-ON time shows a minimal impact with the load current as the balancing and output capacitances mainly drive the transition rate with a resistive load switching condition.

Figure 9.26a, b show the dynamic balancing of the proposed cascaded switch during turn-OFF and turn-ON transitions at 6 kV with a resistive load of 400 Ω. The

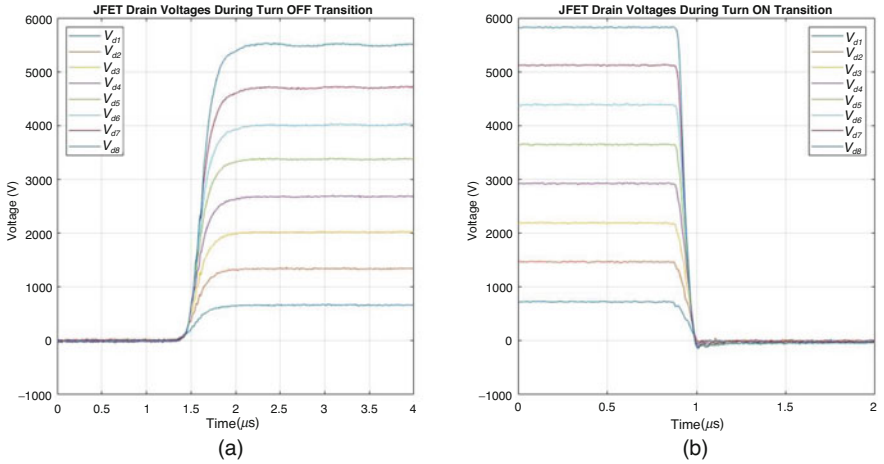

Fig. 9.26 Drain voltage across the JFETs during (**a**) the turn-OFF transition and (**b**) the turn-ON transition

waveforms represent equal voltage distributions during the switching transitions, as well as a seamless transition from the conduction state to the blocking state, and vice versa.

Normally-OFF Path

Fabrication of the different PCSS designs uses commercially available semi-insulating (SI) GaN substrates obtained from various vendors. Different intentional dopants acting as mid-bandgap traps are used by the commercial vendors to render the material semi-insulating, and this choice of dopant has implications on the choice of optical trigger wavelength and pulse energy to operate the GaN switch in the lock-ON mode. For example, both Fe and Mn are used as the mid-gap trap with the switches described in this chapter using the Mn-doped material. Conventional semiconductor fabrication techniques are used to create both the lateral and vertical PCSS switches. The lateral switch fabrication process uses standard contact lithography and liftoff techniques to deposit the patterned Ti/Al/Ni/Au top contacts, and a thicker Ti/Au bondpad contact is patterned on top of the original contact to allow for wire-bonding to the final package design. The performance of the switch is determined by the distance between these contact pads, with designs ranging from 0.6 mm to 3 mm having been demonstrated. No additional processing is performed other than dicing of the devices to singulate for packaging. The vertical switch fabrication process is more complex, starting with a similar top contact deposition and patterning process, with a perforated design to allow access for the optical trigger. Then a front side dielectric layer, SiN, is deposited over the entire pattern, and a lithography and etch process is used to remove the dielectric over most of the top contact. Like the lateral switch, a thick Ti/Au layer is patterned over the first contact layer, also with perforations, to allow wire-bonding to the package and to

handle the large device currents. Then the wafer is flipped over and a SiN backside dielectric is deposited, and a window is opened through the dielectric using patterns aligned to the front-side metal layers. Lastly, a thick back-side metal contact using a Ti/Al/Ni/Au-based metal stack is deposited over the opening in the back-side dielectric layer for the other electrical contact. Lastly, the completed devices are diced out of the wafer for packaging into the circuit breaker. Future designs for the PCSS will include the growth of doped p- and n-contact layers to improve electrical contact performance during the high-current device operation to improve device lifetime.

Testing of Integrated SSCB

To verify the functionality of the circuit breaker design, experiments were performed with a 6 kV prototype. The experimental setup matches the diagram shown in Fig. 9.2; the circuit breaker prototype is positioned between a DC power supply and a passive resistive load. The power supply is capable of sourcing up to 50 kW at 6 kV and remains on throughout the tests. The experiment begins with the breaker in the ON state, i.e., conducting current to the load through the normally-ON path. Current and voltage waveforms are recorded during a turn-OFF transient, in which the breaker transitions to a high impedance state and breaks the DC current flowing to the load. The main point of interest in these experiments is the coordinated behavior of the normally-ON and normally-OFF subcircuits within the breaker. This is controlled by the timing of the control signals sent to the PCSS's optical driver (benchtop Nd:YAG laser) and the JFET circuit's gate driver.

The primary goal of the breaker hardware testing is to verify the behavior depicted in Fig. 9.3. Successful breaker operation involves precisely timed activation of the PCSS to achieve lock-ON behavior and effectively re-route current from the JFET circuit. The critical control parameter governing circuit timing is the delay between the JFET trigger (t_1 in Fig. 9.3) and the PCSS firing (t_2 in Fig. 9.3). Lock-ON behavior in the PCSS requires some minimum voltage across the device at the time of activation. Since the PCSS is not conducting before it fires, the PCSS voltage is equal to the voltage across the JFET circuit, which begins to rise after the gate driver turn-OFF signal is issued. If the PCSS fires too early, the voltage across the device will not have risen sufficiently to achieve lock-ON. If the PCSS fires too late, the JFET circuit turn-OFF will have completed while bearing the full fault current, causing significant thermal stress to the normally-ON path.

The experiments differ slightly from the conditions represented in Fig. 9.3 in that the turn-OFF transient is initiated from a known, constant current magnitude rather than a rising fault current. This change allows the current magnitude at the transition to be controlled by varying the load impedance.

Test results for a successful turn-OFF transient at 6 kV are shown in Figs. 9.27 and 9.28. Line current prior to the turn-OFF transient was 5 A. The optical driver was configured to deliver 1.35 mJ of laser energy during this test. Voltages across the full breaker, shunt capacitor, and load were measured directly. Line/load current and current through the normally-ON and normally-OFF circuit legs were measured using Hall-effect current probes. Dynamics for all waveforms over the full turn-

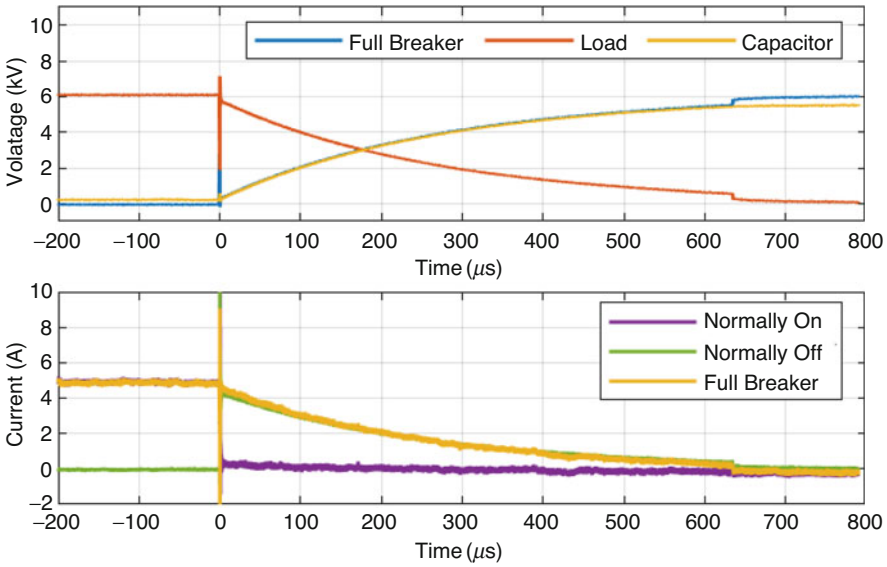

Fig. 9.27 Longer duration turn-OFF transient voltage and current behavior for 6 kV hardware demonstration

OFF transient are shown in Fig. 9.27. At this timescale, the turn-OFF duration is dominated by the charging time of the shunt capacitor, which is conservatively oversized for the load current being interrupted.

An inset of the same turn-OFF transient is shown in Fig. 9.28. At this scale, the coordinated behavior of the normally-ON and normally-OFF circuit legs is evident. As the turn-OFF transient begins, the voltage across the cascaded JFETs begins to rise. Since the shunt capacitor in the normally-OFF leg is uncharged, the voltage across the PCSS is equal to the voltage across the JFETs. Once this voltage reaches a critical threshold, the optical driver fires, actuating the PCSS. This causes the voltage across the JFETs to drop, and all current is diverted away from the normally-ON path into the PCSS and shunt capacitor.

These results successfully demonstrate the key features of the breaker's functionality. In particular, lock-ON is achieved in the PCSS, and current is diverted into the shunt capacitor, reducing thermal stress on the JFET devices during the turn-OFF transition. In contrast, Fig. 9.29 shows a 5 kV test in which the PCSS fires too early and fails to achieve lock-ON. As a result, no current is diverted from the normally-ON path, and all turn-OFF energy is dissipated in the JFETs. These results have two implications for practical breaker implementation. First, a precise optical driver with consistent propagation delay is critical for ensuring timely activation of the PCSS. Second, the ideal time of PCSS activation depends on the voltage threshold for achieving lock-ON. When this threshold is large relative to the system's rated line voltage, the window for achieving lock-ON is small, and the potential for reducing

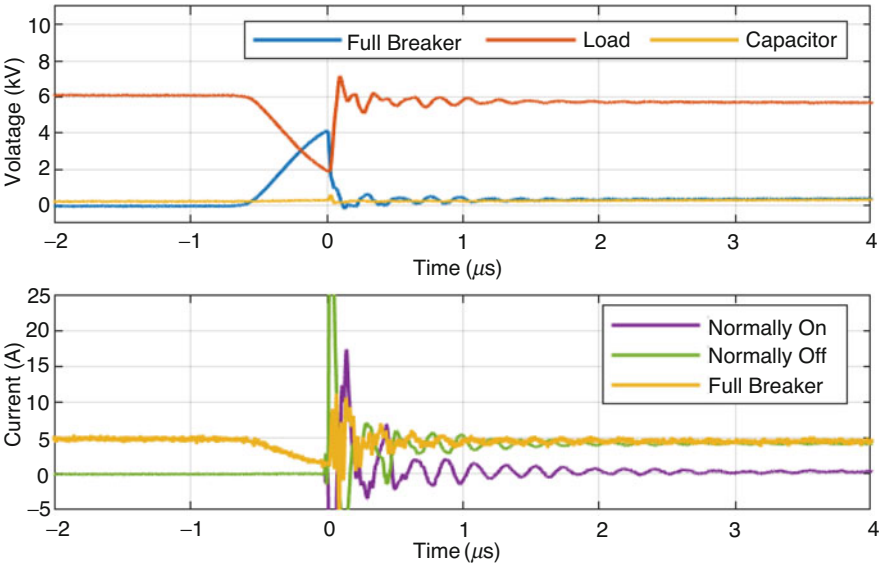

Fig. 9.28 Shorter duration turn-OFF transient voltage and current behavior for the 6 kV hardware demonstration

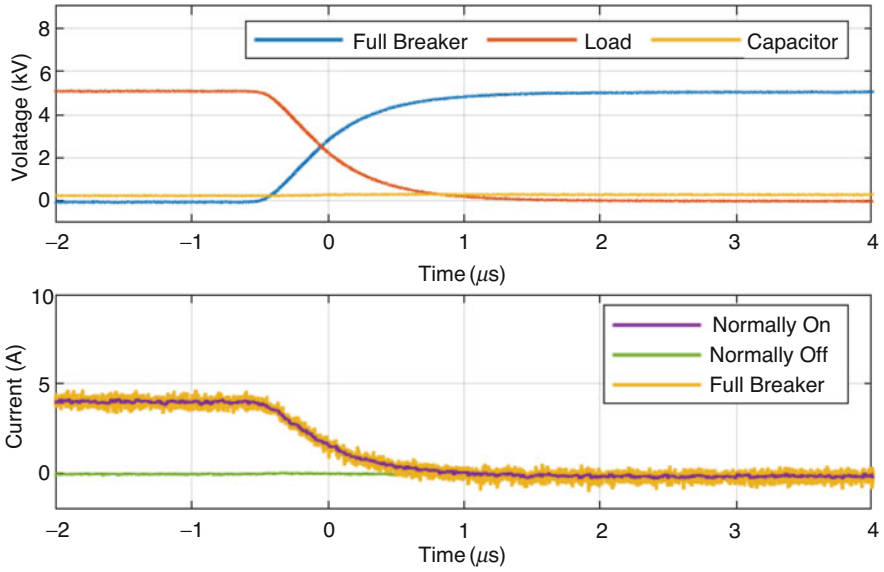

Fig. 9.29 Shorter duration turn-OFF transient voltage and current behavior when the PCSS optical trigger event happens too early and the switch fails to achieve lock-ON behavior

stress on the JFETs is low. However, as the system line voltage increases, the outlook for achieving lock-ON and significant JFET stress reduction improves.

6 Future Directions and Conclusions

The work presented herein has demonstrated the viability a SSCB design utilizing a GaN photoconductive switch as the basis for the breaker's normally-OFF leg, coupled with a normally-ON leg composed of cascaded SiC JFETs. Future work should focus on the scaling of the voltage and current ratings of the PCSS, particularly for the vertical device, as well as better understanding the physics of the lock-ON mechanism and the sub-threshold triggering, which will aid in miniaturizing the laser trigger source and thus the overall circuit.

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Part III
Hybrid Circuit Breakers

Chapter 10
ABB's Recent Advances on Hybrid DC Circuit Breakers

Jesper Magnusson and David Schaeffer

1 Introduction

The hybrid circuit breakers considered in this chapter consist of a combination of mechanical and solid-state devices. The idea is to utilize each component where it has the maximal performance and to compensate for the other components' shortcomings at the cost of increased complexity. For the hybrid topology to be competitive compared to both the solid-state circuit breaker and the mechanical circuit breaker, the combination must provide the possibility to reduce the requirements on both components compared to the alternative solutions.

2 PowerFul CB: A Hybrid Fault Current Limiting Circuit Breaker for AC Distribution Networks

Between 2017 and 2022, a project developing and testing a hybrid fault current limiting circuit breaker (FLCB) was running under the name PowerFul CB. The project is a collaboration between ABB and UK Power Networks, an electrical distribution network operator covering London, the South East, and East of England. The application as an FLCB is to limit and interrupt the current before the first peak in the event of a fault in an AC network to avoid reaching the system design limit. This technology can enable more generation to be added to the network and allows

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an increase in the prospective fault current, without requiring costly upgrades to the substations and their switchgear.

Even though this project has its application in an AC distribution network, the task of limiting and interrupting the rising current before its first peak is very similar to interrupting a rising fault current in a DC system. During the project, a device has been developed and implemented in a pilot installation. The device was tested according to applicable parts of the standards and additional project-specific features to be qualified and allowed for installation in the electric distribution network of London in the UK. After testing, installation, and commissioning, the pilot device has successfully proven its capabilities in the network during a 2-year long trial period.

Limitation of fault currents in AC distribution systems is out of the scope of this book, so the application will not be described in detail here. More information about the application can be found in the detailed project description [1]. Considering the shortage of MVDC systems where circuit breakers can be tested under real conditions, this project provides an important contribution to the proof of concept of hybrid DC circuit breakers' capabilities and to build confidence in the technology. The hybrid topology is very suitable to limit and interrupt fast rising currents also in an MVDC network, and the pilot device described here can be used in such an application without adaptation.

Requirements of the FLCB

One major challenge when developing new technologies is to define relevant design parameters. As this project was initiated from a clearly defined application within the MV distribution network, the requirements were rather well-defined. However, from a product point of view, with market analysis and cost-benefit analysis, there is a desire to reach a larger market. Further, other parameters such as space requirements and availability are added to the technical specifications. Therefore, the design values for the device were agreed according to Table 10.1. The voltage level in the trial site is 11 kV, and the current differs depending on the running arrangement of the FLCB.

Topology and Design Considerations

In its simplest form, the mechanical-solid-state hybrid circuit breaker consists of three parallel components: a mechanical switch, a power semiconductor, and a metal oxide varistor as shown in Fig. 10.1.

Table 10.1 FLCB design parameters agreed between ABB and UK Power Networks

Power frequency: 50 Hz
Nominal voltage: 12 kV (RMS, line to line)
Maximum continuous current: 2000 A (RMS)
Prospective fault current: 25 kA (RMS)
Limited peak current: 13 kA
Current limited in less than 1 ms after fault detection

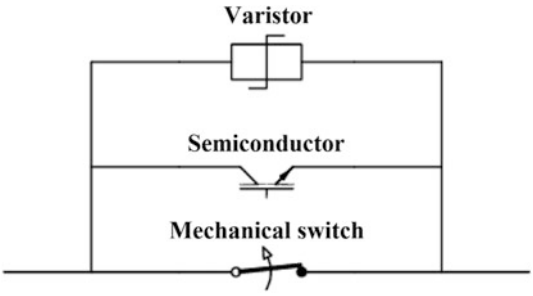

Fig. 10.1 Basic topology of a hybrid FLCB or DC circuit breaker

The actual current limitation and energy absorption is, as in most DC circuit breaker topologies, performed by a metal oxide varistor. Its non-linear resistive behavior is utilized both to limit the voltage across the other components and to absorb the magnetic energy stored in the system, forcing the current down to zero.

The purpose of the other two components can be viewed in two different ways. Most commonly, the hybrid circuit breaker is considered as a solid-state circuit breaker, where the power semiconductor is used as the main interruption means, but due to the high conduction losses, it is bypassed by a mechanical switch during normal operation to fulfill specifications on cooling or energy efficiency. However, it can also be viewed from another perspective: a power semiconductor is introduced to aid in the current interruption and relax the demands on the mechanical device. Interrupting and limiting direct currents at higher voltages is challenging for a traditional mechanical circuit breaker as the demands on arc voltage and speed of operation are high. When the interruption is performed by a power semiconductor, the requirement on the mechanical switch is changed from current interruption capability to a capability of commutating the current into the semiconductor. The arc voltage only has to be high enough to push the current through the parasitic inductance between the mechanical switch and the power semiconductor. Thus, the mechanical switch can be made lighter and hence naturally faster.

The implementation of the PowerFul CB can be seen in Fig. 10.2. To increase the reliability, the FLCB is built up of four series connected modules, each consisting of the three parallel branches. The components are chosen such that three modules are enough to handle the system voltage to limit and interrupt the current. By including a fourth module in series, a redundancy is introduced so that the trial device can accept one failure in any of the component and still manage the interruption. This redundancy significantly increases the reliability of the device to meet the high requirements of power availability in the distribution network.

To decrease cost and development time, and increase the confidence in the pilot device, many of the components used in the FLCB are existing products. The semiconductors are high power BiGTs, the surge arresters are off the shelf products, while the mechanical commutation switches are specifically developed for the project.

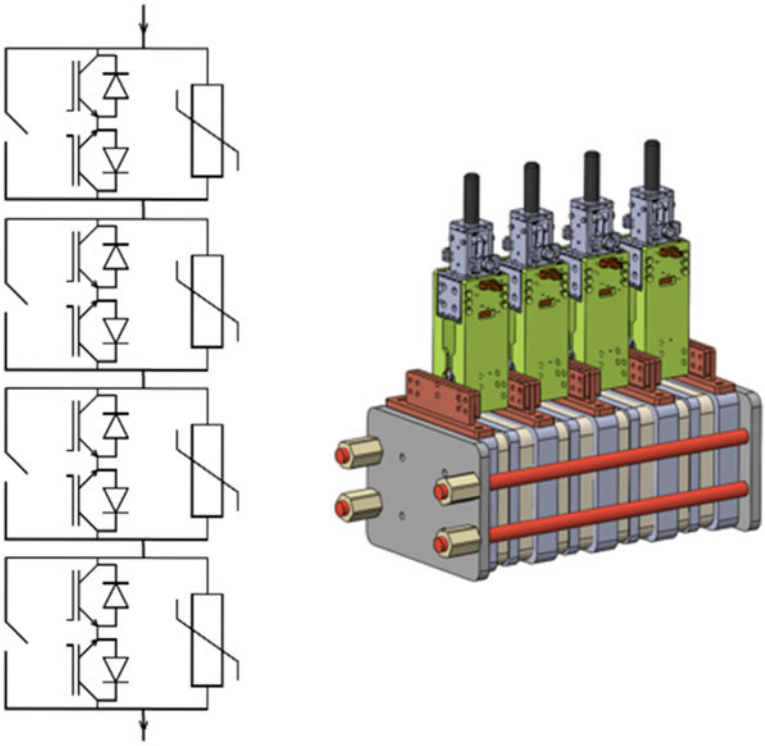

Fig. 10.2 FLCB topology, circuit diagram to the left, and physical layout to the right

Operation Principle

Figure 10.3 shows the current and voltage during interruption of a rising current by the hybrid circuit breaker in a test of a single module. When a low impedance fault is applied to the system around $t = -0.4$ milliseconds, the current starts to rise rapidly in the mechanical switch (fast commutation switch, FCS) as shown in yellow. At $t = 0$ the circuit breaker is tripped, and a command is sent to open the mechanical switch. Due to the mechanics, there is a delay before the contacts of the mechanical switch separate, here around $t = 0.4$ milliseconds, and an electrical arc is formed between the contacts. As the arc voltage is higher than the voltage drop across the semiconductors, the arc voltage commutates the current into the parallel branch containing the power semiconductors (here BiGT). It is desired that the loop between the parallel branches is small to facilitate a fast commutation to minimize the arcing time. Once the current has commutated fully, the arc ceases. The current, shown in purple, is now allowed to flow through the semiconductors as the mechanical switch continues to open and regain insulation strength between the contacts. Once the mechanical switch has opened enough, the semiconductors are turned off at $t = 0.7$ milliseconds, forcing the current into the third branch containing the metal oxide varistor. The voltage across the device rises up to the

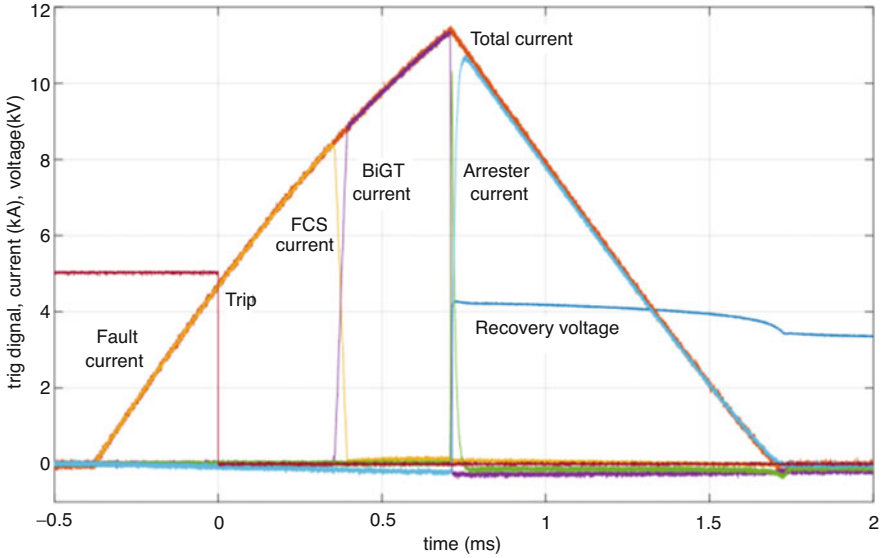

Fig. 10.3 Current and voltage during interruption by the hybrid FLCB or DC circuit breaker

conduction level of the surge arrester, and as this is higher than the system voltage, the current starts to decrease. Once the current reaches zero, the voltage across the hybrid circuit breaker is equal to the system voltage, and only a small residual current flows through the surge arrester.

Testing

Development tests have been performed on all components during the design phase, and qualifying tests on the FLCB for installation in the network have been carried out. As far as possible, the FLCB was tested according to the AC circuit breaker standard IEC 62271-100 in line with the qualification of all other equipment in the system. However, some features of the FLCB, like the current limitation capability, are not applicable to standard circuit breakers and had to be verified specifically for the FLCB. Table 10.2 summarizes some of the tests performed according to the standard and some of the additional tests performed on the FLCB in agreement with UK Power Networks.

Figure 10.4 shows the current and voltage waveforms in one phase when interrupting a short-circuit current during the qualification type-test. At the time $t = 0$, the circuit is closed by an external switch, and a current with a prospective amplitude of 25 kA rms starts to rise. The prospective fault current is shown in a dashed red line, and it is slightly asymmetric reaching above 50 kA on the positive peak. At a level of 4 kA instantaneous current, the fault is detected by the FLCB control system, and the FLCB operation is triggered. The blue curve shows the actual current that flows through the FLCB. It is limited within a millisecond and

Table 10.2 Qualification tests performed on the FLCB pilot device

Testing according to standard (IEC 62271-100)	Additional tests for pilot
Interruption, 25 kA prospective	Current limited 0.7 ms after trip
Close-Open, 25 kA prospective	Current peak limited to <13 kA
28 kV AC, 1 min	Mechanical endurance
75 kV BIL	Electrical endurance
2000 A temperature rise	EMC
STC, 25 kA, 1 s	STC, 16 kA, 3 s
Internal arc testing	

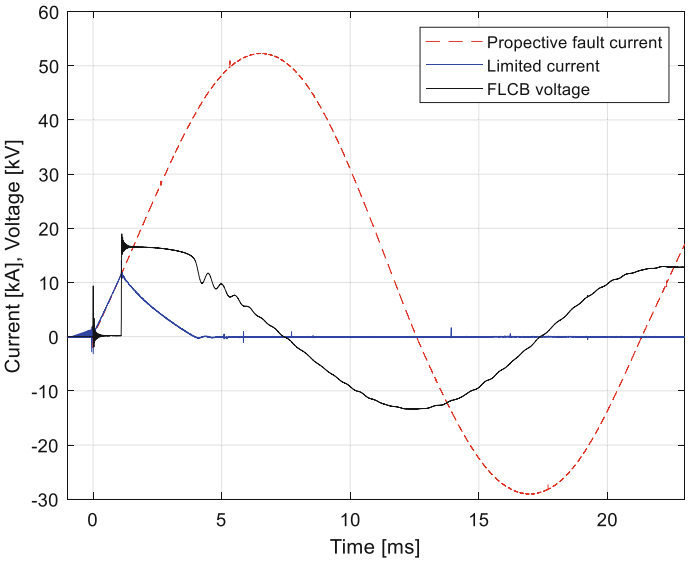

Fig. 10.4 Limitation and interruption of a fault current during type-testing of the FLCB

reaches a peak below 13 kA before it decays down to zero. The voltage across the FLCB is shown by the black curve. Due to the low resistance of the mechanical switches, the voltage across the FLCB is low, typically less than 1 Volt, during the rise of the fault current. Once the FLCB has operated, the decaying current is conducted by the metal oxide varistors that limit the voltage, and due to their non-linear characteristics, the voltage across the FLCB is kept almost constant around 15 kV during the decay. When the current reaches zero, the FLCB blocks further current from flowing, and the voltage across it follows the sinusoidal system voltage.

A Close-Open test was performed during the type-test and is shown in Fig. 10.5. The system voltage, shown in black, is applied across the FLCB, and the FLCB is closed by turning on the BiGTs at the time $t = 0$. The blue curve shows that the current starts to rise rapidly due to the low impedance of the circuit. As in the previous test, the fault is detected, and the FLCB is tripped when the current passes 4 kA. At this point, the current through the FLCB is carried solely by the

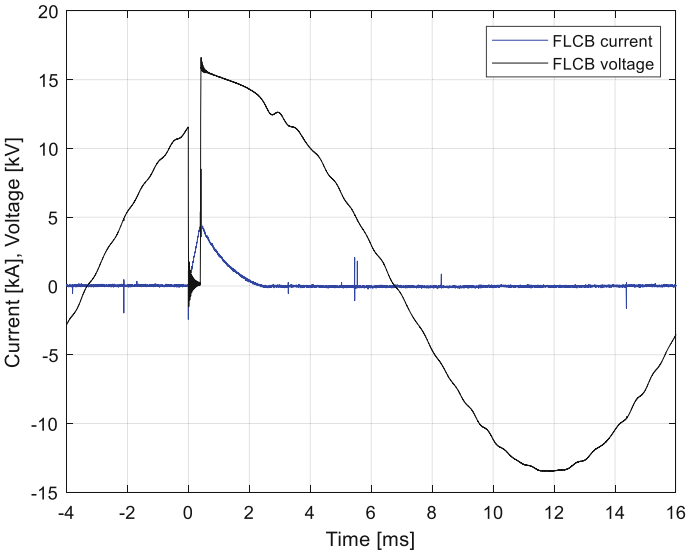

Fig. 10.5 Voltage and current waveforms during a close-open operation into a solid short-circuit during type-testing

semiconductors, and the mechanical switches are still open. Hence, the FLCB acts as a solid-state circuit breaker, and the current is interrupted within microseconds. A transient over-voltage from the metal oxide varistors is seen in the voltage during the decay of the current before the current reaches zero, and the voltage across the FLCB returns to follow the system voltage.

Field Experience

The FLCB pilot device was installed in the electricity distribution network of London during a 2-year long trial period to confirm its long-term performance. Most of the time, it was connected as a bus-coupler, tying two busbars in the substation together to increase the redundancy and reliability of the network. It was also tested in another network configuration where it carried the full load current from one of the feeding transformers. Both configurations render similar fault current shapes and are very similar to applications as a circuit breaker or bus-tie in a DC-system.

Figure 10.6 shows an example of a fault current that was detected, limited, and interrupted during the trial. Before the fault occurs, symmetrical load currents in all three phases flow through the mechanical switches of the FLCB. Close to the negative peak of the load current, a single phase to ground fault occurs in phase L1, shown in blue. Since the power factor is rather close to 1, the phase to ground voltage is also close to its maximum resulting in an almost linear rise of the fault current. The rate of rise of the fault current is determined by the system voltage and network impedance, but also by the impedance of the fault, i.e., both the location

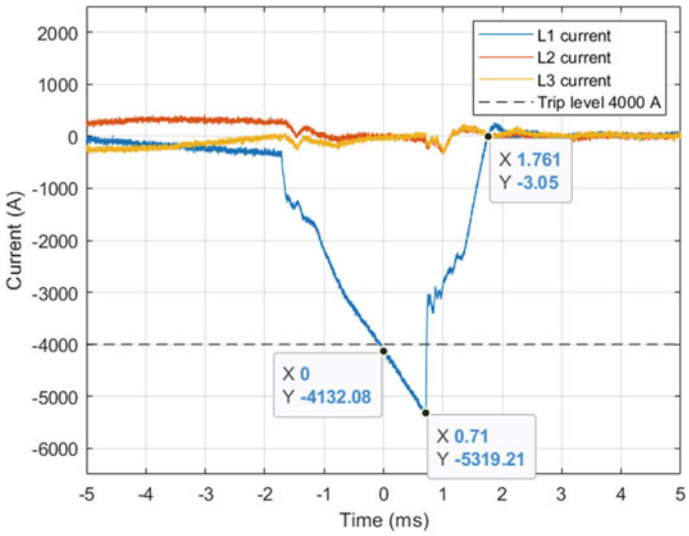

Fig. 10.6 Typical fault current interrupted by the FLCB during the trial period

and impedance of the fault itself. In this case the rate of rise can be estimated to 1.8 kA/ms, which is rather low compared to the initial rate of rise of 11 kA/ms for a 25 kA symmetric fault that the FLCB is designed for. Once the current crosses 4 kA, the FLCB control system detects it as a fault current and trips the FLCB. During the FLCB operation, the current keeps rising almost unaffectedly, and 0.7 ms after the trip, the semiconductors are turned off and the current is limited. The decay of the current to zero depends on the phase angle of the voltage, and the system configuration and loading. Within a few milliseconds, the current through the FLCB reaches zero.

When a fault occurs close to peak voltage, considering a mainly inductive circuit, the fault current is symmetric around zero. This means the prospective peak current is lower than for an asymmetric fault, where the fault occurs close to the voltage zero-crossing. However, the symmetric fault current provides the highest rate of rise of the fault current, and since the FLCB acts and limits the current on the rising edge, the resulting limited peak current is higher for the symmetrical fault than for the asymmetrical fault. For a simple DC-system that consists of a 6-pulse rectified AC voltage source, and neglecting the contributions from any smoothing capacitors, the rise of the fault current is very similar to the symmetrical fault current in the AC-network [2].

During the trial, the FLCB has proven its capabilities of current interruption on the rising edge and to limit the fault current within 0.7 milliseconds after fault detection. The peak current could be further decreased by decreasing the tripping level of the FLCB, but this level is always a trade-off between low peak current and avoiding unnecessary tripping. During the trial, several faults with lower amplitude

have also occurred where the FLCB did not trip as the fault current did not reach the trip level. This ability is easily forgotten but is an important part of the selectivity and discrimination schemes of the protection in the electrical power system.

Scaling
For low voltage DC applications, the parallel hybrid topology is often considered too expensive. Partly because the market is very cost-driven so that full scale power semiconductors become unreasonably expensive, but also because that mechanical circuit breaker technology is more feasible due to the lower system voltage.

For high voltage DC applications, the hybrid topology becomes rather expensive since many semiconductors are required in series to handle the system voltage. Further, the voltage drop across these components becomes high, increasing the requirements on the arc voltage of the mechanical commutation switch. One possible solution to this is to split the mechanical switch into two components: a load commutation switch and an ultrafast disconnector [3].

The parallel hybrid topology is well suited for medium voltage DC applications. There are power semiconductors available in suitable voltage ranges, the required commutation voltage is manageable, and the voltage level gives reasonable dimensions for the mechanical switches.

Summary
In the PowerFul CB project, a hybrid fault current limiting circuit breaker has been developed, tested, and demonstrated in field. During a 2-year long trial in an 11 kV electric power distribution network, the device has proven its capability to limit and interrupt fast rising fault currents in a real environment. Since the topology of the FLCB is identical to a hybrid DC circuit breaker, the project and the successful trial also contributes to the proof of concept and long-term development of future hybrid DC circuit breakers.

3 A Novel Low Voltage Hybrid DC Switch Using Resonant Current Injection

In this part, a novel concept of a low voltage DC switch is reported based on a resonant current injection technique. Instead of pre-charging a resonant capacitor prior to each operation, the main feature of this design is that the arc voltage across the contacts is utilized to charge the capacitor. Thyristor groups are used to control the charging and the discharging of the resonant capacitor in appropriate polarities. This concept presents a low-cost design with shorter breaking time than a conventional DC switch. A prototype of a DC switch based on the proposed concept was built and tested in the ABB Corporate Research Center in Västerås, Sweden, during the years 2014–2017. The concept, the design, and the tests presented here have been carried out by Zichi Zhang, Stefan Valdemarsson, and Erik Johansson.

Introduction

Conventional low voltage DC switches often connect all three or four poles of an AC switch in series, to create an arc voltage high enough to overcome the system voltage and force the current to zero. However, it is challenging for conventional DC switches to interrupt direct current at higher voltage ratings than 1 kV. Combined in one device, many splitter plates are required to be piled up to generate a high enough arc voltage. Hence, the dimensions of the switches become very bulky and costly. Another way to break a direct current is to generate an injection current from a pre-charged capacitor, creating a local current zero crossing in the switch [4]. Unfortunately, the market for low voltage switches is cost sensitive, and the cost of such a solution for a low voltage DC switch is generally too high. Pure solid-state devices are even more expensive, and losses need to be handled with active cooling, especially when the maximum continuous current is higher than 1 kA.

Hybrid switches have been a recent trend as they combine the advantages of conventional mechanical devices (passive cooling, overload abilities, etc.) and solid-state devices (fast interruption, controllability). At low voltage, ABB launched the world's first low voltage molded-case hybrid switch in 2014 [5]. Further, Eaton has released a hybrid DC contactor up to 1000 VDC [6]. Among these low voltage hybrid switches, the solid-state parts are used to break the nominal current lower than 1 kA. For higher currents, these hybrid switches still rely on conventional arc chamber technology to break the current, due to the high cost of solid-state parts for higher currents.

This novel concept of a low voltage DC switch is classified as a hybrid switch containing both mechanical devices and semiconductors, but it is not the solid-state device that interrupts the current. Instead, it is based on current injection to create a local zero-crossing of the arc current. However, unlike a traditional resonant circuit breaker topology like the one described in [4], the proposed design doesn't need to pre-charge the resonant capacitor. Instead, the semiconductors use the arc voltage to build up a high enough voltage across the capacitor to create the desired zero-crossing of the arc current. The most distinctive features of the novel design are the fast current interruption, and the relatively low cost of the power electronic components.

Basic Principle

The diagram of the proposed DC switch is shown in Fig. 10.7. This hybrid switch conducts current and provides current interruption capabilities in both directions. It consists of two groups of thyristors, a resonant circuit with a capacitor and an inductor, a surge arrester (MOV) and a mechanical switch, here represented by two moving electrical contacts in series. The surge arrester provides counter overvoltage to interrupt current in the circuit, transforming the magnetic energy stored in the external system inductance into heat. The mechanical switch can be of single contact or dual contact design. In the case of dual contact design, the current injection parts and the surge arrester are parallel to only one electrical contact while the other contact can be seen as a disconnector.

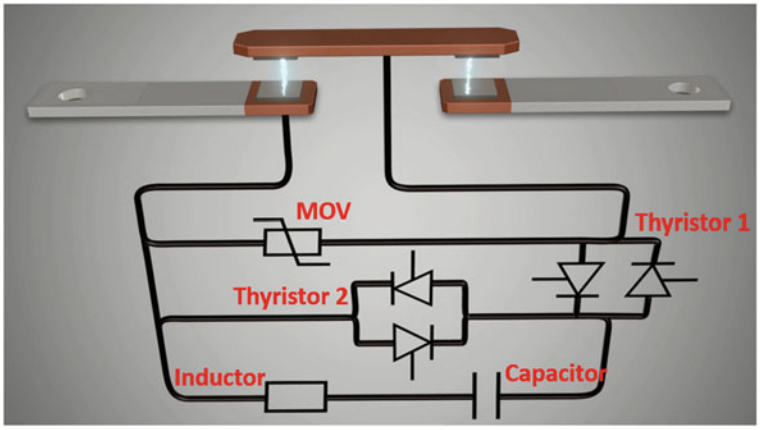

Fig. 10.7 Circuit diagram of the hybrid switch using resonant current injection

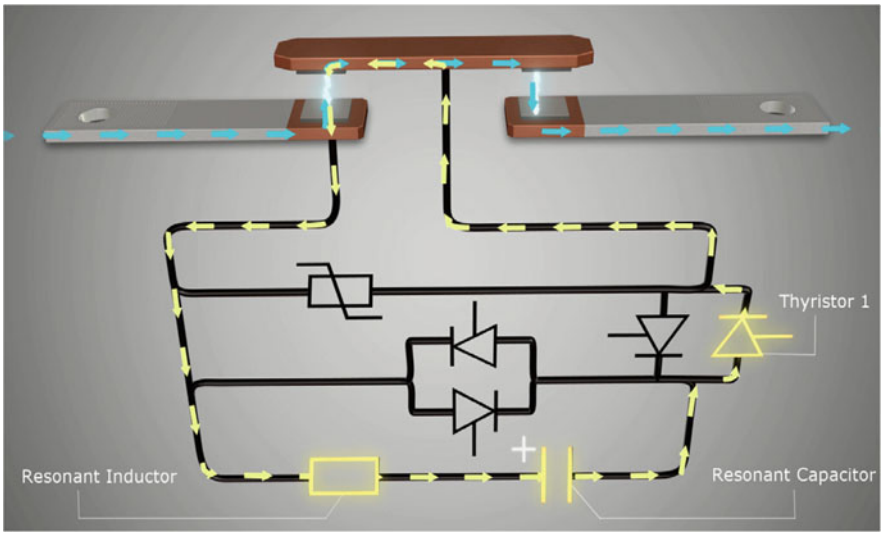

Fig. 10.8 Step 1: arc voltage charging resonant capacitor

Once the arc voltage across the contacts of the switch is detected, thyristor T1 is fired. The capacitor is charged by the arc voltage across the contact on the left; see Fig. 10.8. T1 switches off automatically once the injection current reaches zero, and the capacitor is fully charged.

Once the blocking state of T1 is checked, the thyristor T2 is fired to let the resonant capacitor discharge and change polarity at the end of this discharge half-period, according to Fig. 10.9. By repeating the described process of firing T1 and T2, a series of progressively larger resonant injection currents are generated. When the injection current reaches the amplitude of the load current, a local current

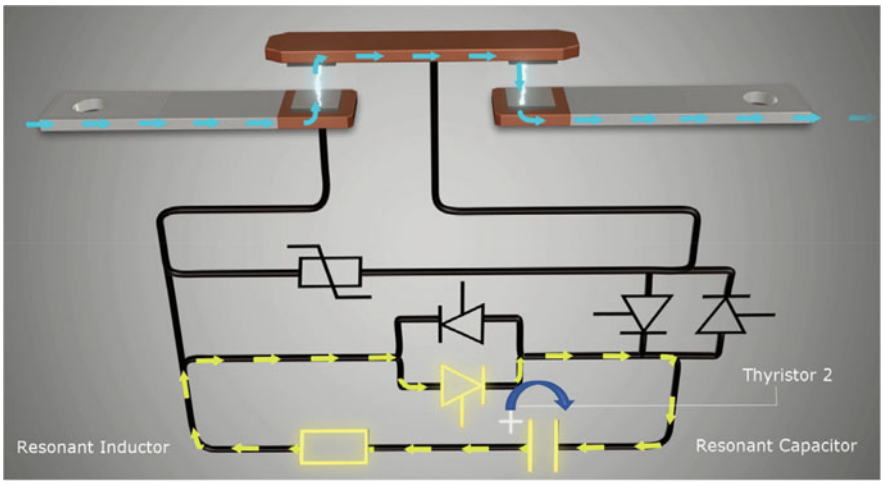

Fig. 10.9 Step 2, resonant capacitor discharging and changing polarity

zero crossing is created at the contact gap on the left, and the electrical arc can be successfully extinguished.

The thyristors are placed in pairs, coupled in antiparallel to be able to react similarly for both current directions. It is enough to fire both thyristors in the same group together as the arc voltage (positive or negative) will determine which one will conduct.

Once the arc is interrupted, the main current charges the resonant capacitor until the operation voltage level of the surge arrester is reached, as shown in Fig. 10.10. At that time, the current commutates to the surge arrester and eventually reaches zero after a time depending on the overvoltage formed by the surge arrester and the external inductance in the circuit; see Fig. 10.11.

The arc might restrike if the transient recovery voltage between the contact gap is larger than the voltage withstand strength (between contacts on the left in the figures). In this case, T2 should be fired again to change the polarity of the resonant capacitor. The same procedure of firing T1 and T2 goes on till the current is properly interrupted. The dual contact design can provide the disconnection function for this hybrid switch so that no external mechanical disconnector is required between the load and the source.

The current interruption process is summarized in Fig. 10.12 in terms of injection current i1, discharge current i2, DC main current Idc, and voltage across this DC switch. After contact separation, an arc is detected by an arc voltage across the device, and T1 and T2 are fired following a defined time sequence. After the second pulse of i1 in the illustration, the injection current reaches an amplitude to interrupt the current in the contact gap. The main current Idc charges the capacitor, and the contact voltage increases until an arc is reignited in the contact gap. The current injection process starts again to eventually interrupt the arc current a second time.

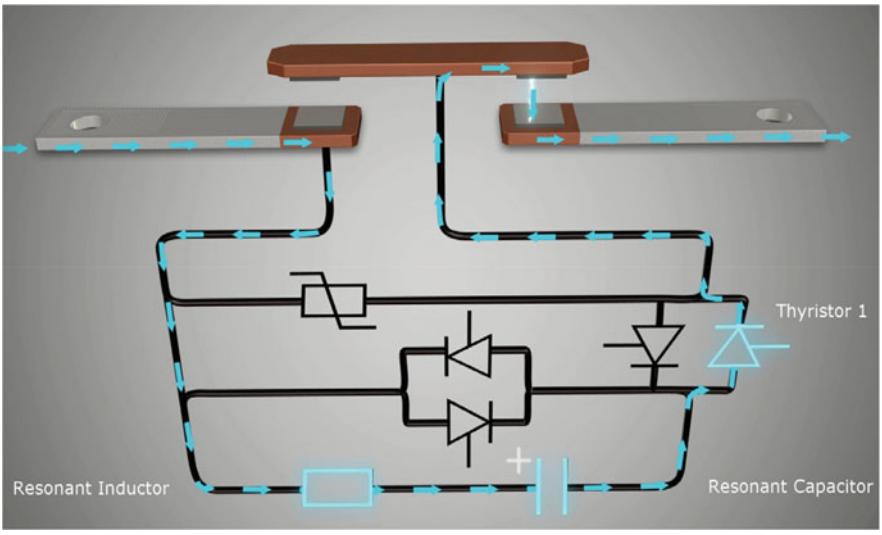

Fig. 10.10 Step 3, main current charging resonant capacitor, after arc extinction across contacts

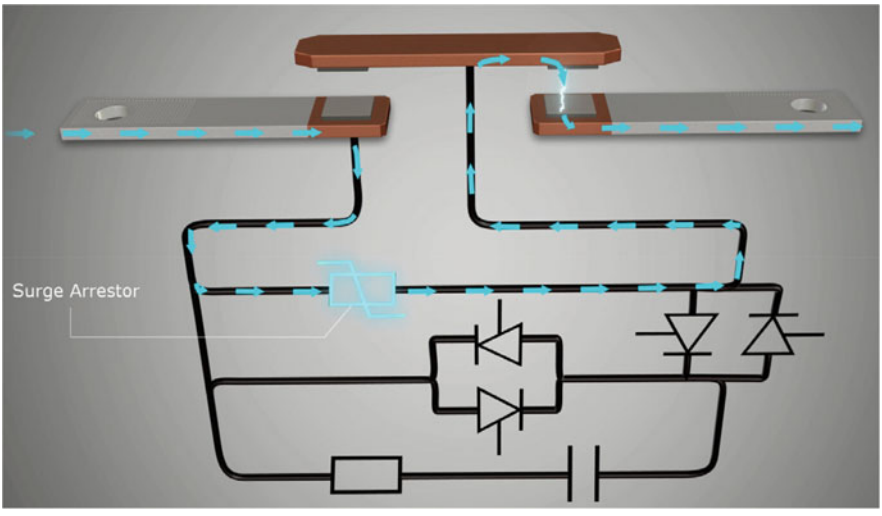

Fig. 10.11 Step 4, current through surge arrester, once operation voltage of surge arrester is reached across contacts

The current Idc charges the capacitor until the gap voltage across the switch reaches the operating voltage of the surge arrester. The surge arrester clamping voltage is chosen higher than the system voltage to create an overvoltage which limits and eventually interrupts the current Idc in the circuit.

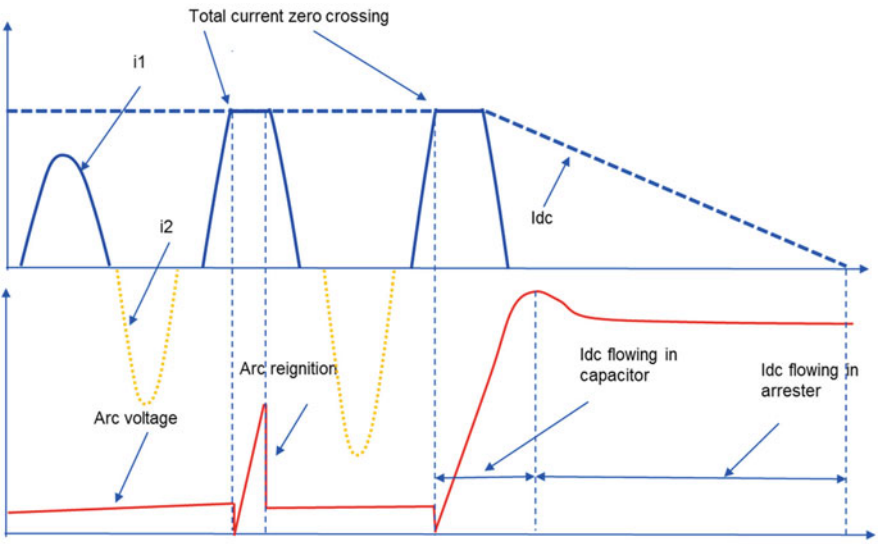

Fig. 10.12 Injection current (i1), discharge current (i2), main current (Idc), and voltage across the contact gap in red

Simulation Results

A PSCAD simulation model was built to study the feasibility of the concept and evaluate the important parameters for a successful interruption. A simulation result is shown in Fig. 10.13. The simulation uses the current to interrupt 1 kA, with a system voltage of 1 kV, the resonant capacitor 60 μF, the resonant inductor 5 μH, and the arc voltage 55 V. The switch opens at 0.049 s and the arc immediately exhibits a constant 55 V. The current injection is initiated 1 ms after the contact separation. The amplitude of the positive current injection pulses increases each time, and the current zero crossing is reached at the fourth positive pulse. The current I_total charges the capacitor and the contact voltage U_total increases up to the clamping voltage of the surge arrester, around 1.3 kV. The surge arrester operates and the current in the circuit i_total drops to zero at 0.053 s.

Design Considerations

The electronic and the control unit needs power. To avoid extra equipment to be connected to the device and relying on an external power supply, a self-powered supply is configured to accept the arc voltage over the electrical contacts as its source and deliver a stable 5 V TTL level. This voltage powers a microcontroller which generates the sequence of control pulses to fire the thyristors T1 and T2. As soon as an arc voltage is detected, the power supply needs to be turned ON and stabilized, which means that a waiting time is required before being able to start the T1 and T2 firing sequence. The minimum dead time is estimated to be 1 ms between the contact separation and the first T1 firing, but to guarantee a sufficient margin, the deadtime is set to 2 ms.

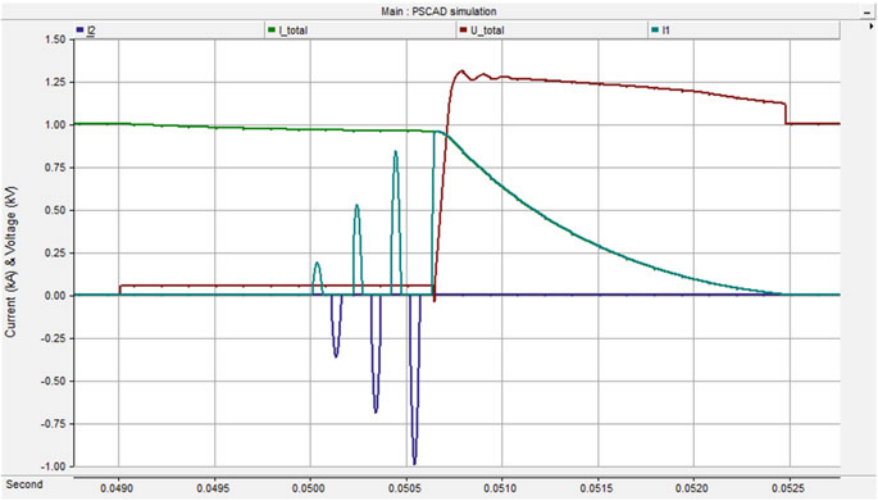

Fig. 10.13 PSCAD simulation result demonstrating the feasibility of the concept

Furthermore, the control system checks if the thyristor T1 is indeed in blocking mode, before firing T2. The sequence then continues until a stop condition is fulfilled. Those conditions are timeout, no voltage supply available, or information output that the gap voltage is above a high voltage threshold indicating that the interruption has been successful. If a restrike occurs, the control unit receives the information of HV failure. The microcontroller can react by restarting the pumping sequence by firing T2 first this time; see Fig. 10.12. More information is available in [7].

A special arc chute has been designed to face the challenges of interruption of such currents with electrical contacts in air. It is placed in the vicinity of the electrical contact on the left in the Figs. 10.7–10.11. A novel design of splitter plates has been proposed to improve the re-ignition voltage withstand, the arc resistance and the current interruption, compared to the arc chute used in standard AC switching devices (steel plates as standard). It is especially necessary for high current interruption that the arc enters in the arc chute to provide enough arc voltage to inject high enough current per pumping cycle and interrupt faster, thus reducing the arcing time. If the current interruption is faster, it is less likely to have an arc restrike because long arcing time degrades the strength of the recovery voltage withstand of the open gap contact. Furthermore, the electrical endurance is improved by reducing the arcing (erosion) time. The novel design combines steel splitter plates with laminated brass layers on top and bottom surfaces. Steel provides magnetic forces to attract the electrical arc from the contacts into the arc chute whereas brass brings high re-ignition voltage withstand and arc resistance. More information is available in [8].

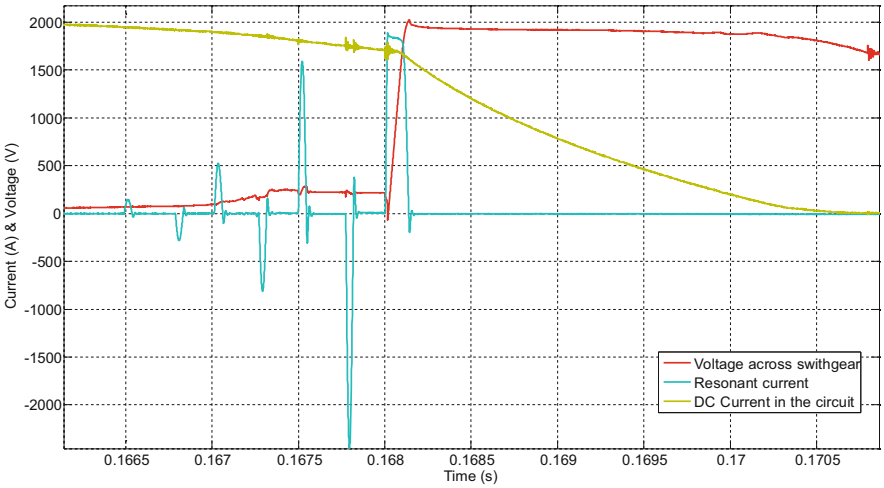

Fig. 10.14 A current of 2000 A is interrupted in a 1650 V system by the prototype within 7 ms after contact separation

Experimental Results

A prototype of the described switch was built to verify the concept at ABB Corporate Research in Västerås, Sweden. A series of tests have been performed at different current and voltage levels. One of the test results is shown in Fig. 10.14 to illustrate the efficiency of the concept. The device is made with a single arc chute of 7 laminated splitter plates to interrupt the arc current and limit the probability of reignition.

The current in the circuit at this specific test is 2000 A and the system voltage around 1650 V. Once the arc starts, the current in the circuit drops a bit due to the arc voltage, limiting the current. The current injection process starts 2 ms after contact separation. The current injection pulses increase stepwise until reaching the main current amplitude at 0.168 s, creating the conditions for a successful arc current interruption. The contact gap voltage reaches the operating voltage level of the surge arrester, and the main current in the circuit is commutated into the surge arrester. The current in the circuit is eventually interrupted after time 0.1705 s. The time to interrupt the current by the surge arrester depends on the time constant of the circuit, the surge arrester clamping voltage, and the system voltage.

Summary

The hybrid DC switch uses the arc voltage to start an oscillation of an injection current. The injection current pulses increase stepwise until a local current zero crossing is created. The costs of this device are greatly reduced because low-cost thyristors can be used, compared to equivalent conventional hybrid devices. The complexity of having a pre-charged capacitor to inject a counter current and create a local current zero crossing is avoided. Furthermore, the current interruption of

this design has been shown to be faster than a traditional DC switch with only splitter plates as means for interruption, and this prototype is even potentially more compact than a traditional equivalent device. The simulations and the experiments demonstrate the feasibility of this low voltage hybrid DC switch design to break DC load current up to 2000 A.

4 Conclusions

This chapter has presented two recent projects with hybrid DC circuit breakers performed at ABB. The concepts are very different in their topologies, but both utilize a combination of semiconductors and mechanical contacts to maximize the performance. The hybrid technology has its most obvious advantages in the medium voltage range where the semiconductors decrease the demand on the mechanical contact's arcing voltage without requiring excessive number of components in series to handle the voltage level. However, it has also been shown that different hybrid topologies can be used to facilitate efficient switching both for lower and higher voltage systems.

In addition to the two projects presented here, ABB has also been active in research on other DC switching technologies, including solid-state, resonant, and pure mechanical. The different technologies have both benefits and drawbacks meaning there is no optimal DC circuit breaker topology for all applications. The choice of technology and topology should therefore always be based on the requirements of the application, and optimized considering both performance, cost, and complexity.

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Chapter 11
Hybrid Circuit Breakers with Transient Commutation Current Injection

Z. John Shen, Steven Schmalz, Steven Chen, and Dong Dong

1 Introduction

Hybrid circuit breakers (HCBs) combine the advantages of mechanical and solid-state circuit breakers and offer low conduction losses, high interruption capability, and reasonable response times of several milliseconds. As discussed in other chapters of this book and survey papers such as [1, 2], there are a multitude of HCB topologies, each having distinct advantages and disadvantages but all featuring two parallel current paths: a mechanical path for conducting the load current efficiently under normal conditions and an electronic path to commutate a fault current from the mechanical path under a fault condition and then turn off after the mechanical switch fully opens. In addition, one or more varistors (MOVs) are placed in parallel to clamp the overvoltage surge during the turnoff of the electronic path and to absorb the residual electromagnetic energy. For example, the electronic path can be a passive or active LC resonant circuit in parallel to the mechanical path. When the mechanical switch (MS) opens in response to a circuit fault, the LC circuit would

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generate a resonant current which cancels the mechanical current at certain time instances, subsequently creating zero current crossings in the mechanical path to aid the opening of the mechanical contacts. A true arcless HCB concept through the use of a load commutation switch (LCS) in series with the mechanical switch was developed by ABB [3–7]. The LCS, made of semiconductor switches with a much lower-voltage rating than the HCB, forces the fault current to commutate from the mechanical to the electronic path when being turned off. The mechanical contacts can therefore open under a true zero current condition without any arcing. One major drawback of the LCS approach, however, is the additional conduction power losses on the LCS, which still has on-state resistance many times that of the mechanical contacts even with a large number of lower-voltage power devices being used in parallel. LCS power losses will become an even bigger challenge with a significant penalty in size and weight as the HCB current rating increases and thus needs to be addressed with innovative solutions.

A new HCB architecture was recently proposed which uses a switching-mode transient commutation current injector (TCCI) instead of the series LCS approach to commutate the fault current from the mechanical to the electronic branch and realize arcless breaker operation [8, 9]. The TCCI circuit remains in a standby mode with near-zero power loss under normal conditions but can rapidly generate a pulse current dynamically matching the fault current and therefore facilitate current commutation from the mechanical to the electronic path. It completely eliminates the conduction power loss associated with the LCS and delivers an ultra-high transmission efficiency. A relatively low-power TCCI-based HCB prototype demonstrated a total active response time of 310 μs and a peak interrupted fault current of 89 A at a DC voltage of 400 V [9].

In this chapter, we will report the development of a 6-kV/200-A TCCI-based HCB designed for medium-voltage DC (MVDC) applications, funded by the US Department of Energy ARPA-E BREAKERS Program [10]. MVDC holds the promise of addressing limitations faced by legacy AC systems including (1) better utilization of existing infrastructure, (2) improved network stability and simplified management of power flow, (3) lower transmission/distribution losses, and (4) easier integration with renewable energy sources. A key to realizing MVDC systems is meeting the requirement for overcurrent fault protection. The development of TCCI-HCB for MVDC power ratings presents unique technical challenges and design considerations in terms of subsystem design, system integration and packaging, control and communication, and dielectric isolation. We will discuss these design issues after a brief review of the basic TCCI-HCB concept.

2 Basic Concept

Figure 11.1 conceptually depicts the circuit topology and switching waveforms of the total load current i_L, mechanical branch current i_M, and electronic branch current i_E during the interruption operation of the HCB in response to a fault condition.

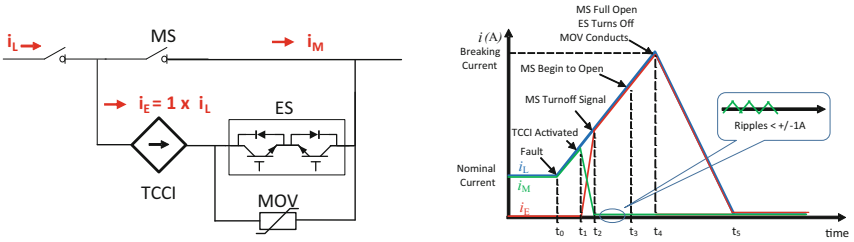

Fig. 11.1 Notional circuit topology and switching waveforms of an HCB with transient commutation current injector (TCCI) [9]

A switched-mode TCCI circuit, shown as a current-controlled current source in Fig. 11.1, is placed in the electronic path. It remains inactive with near-zero power loss during normal operation until t_0 when a short-circuit fault occurs. At t_1, the overcurrent condition is detected. At this point, the TCCI will immediately inject a pulse current i_E from its pre-charged capacitors and dynamically track the fault current with high precision and force the fault current to commutate from the mechanical to the electronic path at t_2. The current through the mechanical branch will remain as a small high-frequency AC ripple current until the mechanical switch (also referred to as high-speed vacuum switch or vacuum disconnect switch later in this chapter) opens at t_3. The small AC ripple current results from the control errors of the TCCI and has the same switching frequency in the range of 100–200 kHz as the TCCI. The mechanical vacuum switch receives a turnoff signal at t_2 and generates a gap between the contactors at t_3 after a short delay without arcing under the near-zero current condition, leaving the electronic branch to carry the entire fault current during t_2 to t_4. At t_4, the mechanical vacuum switch provides a sufficiently wide gap to support the rated voltage, and the electronic switch (ES or referred to as power electronic interrupter (PEI) later in this chapter) turns off, leaving the metal oxide varistor (MOV) to absorb the residual electromagnetic energy during t_4 to t_5.

3 HCB Subsystems

The TCCI-HCB is comprised of several key subsystems, including transient commutation current injector (TCCI), high-speed vacuum switch (HSVS), power electronic interrupter (PEI), and auxiliary power supplies with high-voltage isolation capability. This section discusses the operation principles and design considerations of those subsystems in detail.

3.1 *Transient Commutation Current Injector (TCCI)*

TCCI is the most critical subsystem in the new HCB architecture. The crucial performance target of the TCCI design is its capability of dynamically tracking the fault current within a short delay (<30 μs) and with a high precision (<5%). The TCCI is a switched-mode power electronic circuit, similar to the design of high-current high-precision pulse power sources used for controlling the magnetic fields in linear accelerators [11, 12]. These current sources can quickly generate a pulse current of several kA with extremely small tracking errors (current ripples) of 10–100 ppm (0.001–0.01%) from a pre-charged capacitor bank. It is worth noting that our TCCI needs to track a time-varying fault current instead of a constant "flattop" reference current in these pulse current sources. This challenge can be addressed by operating the TCCI converter at a high PWM frequency for superior dynamic response. On the other hand, our TCCI only needs to operate for hundreds of microsecond instead of hundreds of millisecond as in these prior-art pulse current sources and thus needs a much smaller energy storage capacitor (typically hundreds of microfarad) and power and cooling components with significantly reduced power ratings for this unique "single-shot" pulse mode operation. The TCCI design should be fairly compact and inexpensive.

A simplified bidirectional TCCI topology is proposed in this work as shown in Fig. 11.2, along with other key subsystems of the HCB, such as the vacuum interrupter (VI) and power electronic interrupter (PEI). A 3D rendering of the TCCI is also shown in Fig. 11.2 with the key components clearly labeled. The TCCI is comprised of three parts: a simple buck converter made of IGBT Q_1, freewheeling diode D_1, and filter inductor L_1; a bidirectional current-steering bridge made of four

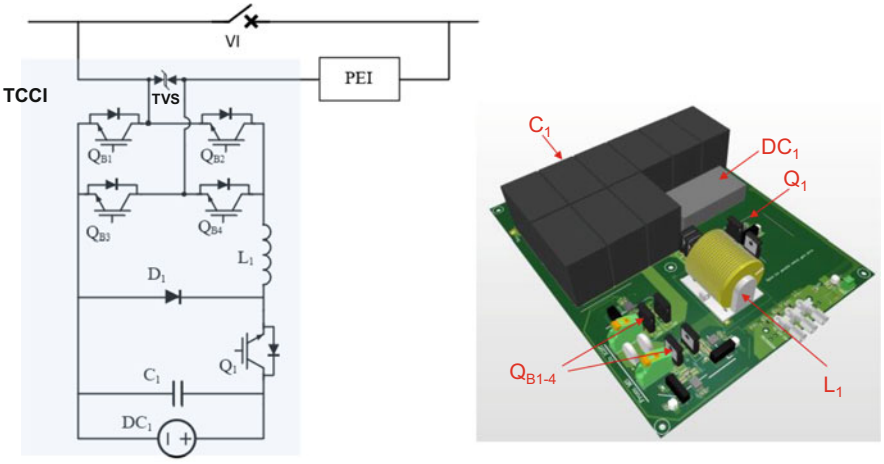

Fig. 11.2 Simplified bidirectional TCCI circuit diagram along with the vacuum interrupter (VI) and power electronic interrupter (PEI) subsystems of the HCB. A TCCI physical design is also shown

IGBTs, Q_{B1}, Q_{B2}, Q_{B3}, and Q_{B4}, and a transient voltage suppresser (TVS); and a capacitor bank C_1 along with its charging power supply DC_1. Depending on the direction of the current in the electronic path, either Q_{B1}/Q_{B4} or Q_{B2}/Q_{B3} is in the on-state to inject a countercurrent to VI through PEI. The TVS is used to prevent undesirable transient overvoltage across the output terminals of the bridge circuit. The basic function of the buck converter is to generate a transient countercurrent to precisely cancel the mechanical branch current by discharging the pre-charged capacitors C_1 in a well-regulated manner. Once an overcurrent condition (e.g., 2× of the nominal current) is detected, Q_1 turns on for a certain period of time to provide an initial pulse current injection within a few tens of microsecond to quickly commutate the mechanical branch current to the electronic branch. During the next 200–500 μs, Q_1 turns on and off in a PWM mode to regulate the TCCI output current, so it closely matches the continuously increasing fault current. The pre-charged C_1 serves as the input energy source for the buck converter. During this phase of operation, the main objective of the TCCI is to track the fault current with a high precision and ensure only a small AC ripple current through the mechanical VI so it can open under a near-zero current condition. After the VI is fully opened, Q_1 turns off, leaving the total fault current flow through D_1, L_1, and Q_{B1}/Q_{B4} or Q_{B2}/Q_{B3} without active control (freewheeling current). PEI is the main static switch in the electronic path, which turns off after VI completely opens as will be discussed later in this chapter. A dual-band hysteretic control method for the TCCI is adopted, which offers fast dynamic response and excellent stability. By carefully selecting the two bandwidths of the dual-band hysteretic PWM controller, the high- and low-voltage phases will work in concert as the coarse (quick) and fine tuners for the high-precision current source. Note that the TCCI is on standby with near-zero power loss during normal operation.

The TCCI design needs to be optimized based on the voltage and current ratings as well as the timing requirement (i.e., how fast the mechanical VI can fully open), including the selection and sizing of the key components (energy storage capacitors, inductor, power transistors, and current sensors). The TCCI essentially discharges the pre-charged capacitors C_1 in a well-controlled manner to generate the required transient commutation current pulse. It is important to select the right size and voltage level of C_1 to ensure sufficient charge storage while avoiding cost and size penalty. Since the TCCI only needs to be activated for a very short time period (typically hundreds of microsecond) when the HCB needs to turn off, it is C_1 that supplies the high pulsed current, while a small isolated DC power supply DC_1 (only rated at a few watts) only serves to pre-charge C_1 when the circuit is under normal operation. In the 6-kV/200-A HCB design case, C_1 is in the range of several hundreds of microfarad with an initial charging voltage of 500–550 V. Film capacitors can be used for this purpose as shown in Fig. 11.2. The value of L_1 is determined by the trade-off between the requirement of the initial fast rise of the TCCI injection current and the requirement of a small AC ripple of the TCCI current after the initial rise. The *di*/*dt* of the TCCI current needs to be 5 ~ 20 times greater than that of the fault current (typically 1–2 A/μs) so the TCCI can effectively commutate the fault current from the mechanical to the electronic path. On the other

hand, the AC ripples on the TCCI current after the initial fast rise needs to be within 5% of the total current so the mechanical contacts can separate without arcing. In the 6-kV/200-A HCB design case, L_1 is in the range of 10–30 μH. Furthermore, 1200-V IGBTs and FRDs are selected for Q_1 and D_1, respectively. 600-V IGBTs are selected for bridge transistors Q_{B1}, Q_{B2}, Q_{B3}, and Q_{B4}. During the TCCI operation, Q_1 switches at a PWM frequency of 100–200 kHz but only for a small number of cycles, similar to pulse power applications; thus, the relatively high switching loss of the IGBTs can be tolerated. The concern here is more associated with reducing the voltage drop across the IGBTs at a very high fault current up to 1000 A.

3.2 High-Speed Vacuum Switch (HSVS)

A second key element in the HCB architecture is the high-speed vacuum switch (HSVS), which serves as the primary conduction path under normal operation of delivering power to the load. Design of the HSVS incorporates a fast actuator, damping and latching mechanisms, and an optimized vacuum interrupter. It is essential to effectively combine all these elements to realize a mechanical switch capable of achieving an interruption time of less than 0.5 ms.

3.2.1 Fast Actuator

High speed and fast response are the primary requirement for this type of mechanical switch in the MVDC hybrid circuit breaker application. In conventional mechanical circuit breakers for AC circuit protection, a typical response time is about 50 ms from the moment of initiating a trip command to actual breaking of the circuit. In this specific design, the required response time (<0.5 ms) is about 1/100th that of a typical mechanical circuit breaker. Contact gaps of MV vacuum interrupters are generally between 2 and 12 mm, depending on voltage ratings and actual applications [13]. For this 6-kV/200-A HCB design, a high-speed vacuum switch (HSVS) is developed with a DC voltage and current rating of 6 kV and 200 A, a contact gap of 6 mm, and a contact moving mass of about 0.5 kg. There is a significant difference in the estimated kinetic energy needed to drive a conventional vacuum switch versus an HSVS because of the different response time requirements. A conventional switch or breaker with a similar moving mass would need a kinetic energy of 0.5–1.0 J to reach an average opening speed of 1–1.5 m/s across a 6-mm gap to interrupt the AC current with mechanical efficiencies fully considered. The new HSVS design, on the other hand, needs a kinetic energy of approximately 9 J to achieve an average speed as high as 6 m/s to meet the specified response time. Since the response times are significantly different between the two (50 and 0.5 ms), the times to disburse the energy are very different too, which dictates the power of actuation. The instantaneous power needed to drive the contact in a conventional design is approximately 150 W. For the HSVS, the power needed may

exceed 18,000 W in order to achieve the required response time for successful fault current interrupting operation.

The large power requirement of the new HSVS determines the type of actuation technology that needs to be used. Actuator mechanisms widely used for conventional switches or circuit breakers, such as springs or solenoids, are no longer practical for the HSVS. Other actuation means need to be explored considering size, weight, cost, and capability of instant power factors. As alternative methods, piezoelectric actuators (material force) and Thomson coils (field force) demonstrate their potential to provide quick acceleration for a movable contact. Piezoelectric actuators have advantages in terms of precision, speed, high force, and durability but can only deliver very small displacement. It is difficult for a piezoelectric actuator to realize more than 1 mm of contact travel even with sizable and sophisticated displacement amplifiers [14]. For the HSVS design in this work, we choose not to adopt piezoelectric actuators after detailed analysis, especially with the consideration of design scalability to higher voltage and current ratings. Thomson coil actuators, an application of Faraday's law of induction, can also produce enough force to move the contacts quickly with larger travel distances. They are particularly effective for vacuum interrupter contacts that normally need to a gap of several millimeters for high dielectric withstanding ability. In a typical form factor volume for a modern MV vacuum switch or circuit breaker, a Thomson coil actuator can produce forces of tens or hundreds of thousands of Newtons, which is impossible for conventional mechanisms to match. Figure 11.3 conceptually shows the anatomy of the new HSVS in this work. The vacuum interrupter (VI) is placed on the top which is mechanically linked to a primary Thomson coil actuator by an insulated drive link rod. The HSVS subsystem also includes an over-toggle damping mechanism and a shock absorber.

There are many factors that must be carefully considered to properly design a Thomson coil actuator. The drive current characteristics (including stored energy requirements), coil impedance, geometry and metallurgy of the moving plate, and overall mechanical configuration must be determined. An assortment of interdependent parameters influences these characteristics and dictates what is and what is not achievable. It can be overwhelming at first look, but the key is to clearly define the required performance of the actuator, which may include efficiency, size, physical constraints for integration, and manufacturing considerations. As in most endeavors, knowing what matters most will lead to an optimized design for the intended purpose [15]. Actually, having so many customizable variables in Thomson coil design is an advantage and provides opportunity for scalability.

Damping Mechanism

A defined open-contact position is always required, even in the case of an HSVS designed for current commutating operation of the HCB. While its initial contact gap of 1–2 mm is critical for successful current commutation and transient voltage withstanding, a wider and settled open-contact gap, 6 mm in this case, is also

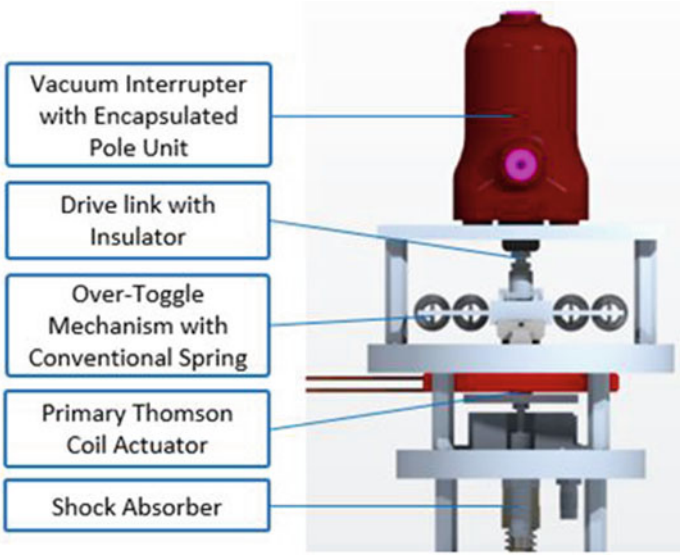

Fig. 11.3 High-speed vacuum switch (HSVS) anatomy

needed. The larger gap is needed to safely withstand, in some conditions, prolonged voltage stresses or occasional voltage surges from the power system in which it is installed, especially when the circuit breaker is in a "hot" standby condition where the disconnector for the line remains closed. While opening speed is the key for achieving the desired performance of current interruption, a controlled deceleration of the moving contact cannot be neglected. The residual kinetic energy stored in the moving mass of the moving contact can be significant, reaching more than ten times that of a conventional vacuum switch. If there is no means provided to properly absorb the residual kinetic energy, the contacts can bounce back, resulting in reduced contact gap during the transient phase of current interruption or commutation that may lead to voltage breakdown. Otherwise, contact overtravel could also occur, which will overstress the bellows of the vacuum interrupter resulting in reduced mechanical life.

Damping can be an efficient method to deal with the residual kinetic energy and can be realized by using commercially available shock absorbers [16]. Although the wide variety of available options may satisfy the specific performance requirement, cost, size, and reliability have to be considered in final selection. For this new design, commercial-type of shock absorbers are used as a quick and feasible solution. Proper damping can sufficiently absorb the energy, but in addition, a purposefully customized damping profile can control contact gap establishment to positively influence events including current commutation, arc interruption, and dielectric strength recovery which happen at different stages in the contact parting process. Contact material, contact configuration, and the targeted application must also be factored into the sequence.

Latching Mechanism

The movable contact of the new HSVS needs to be securely latched in two stable positions, closed and open, similar to all conventional vacuum switches or circuit breakers. The latching in conventional switches or circuit breakers is commonly made by mechanical mechanisms with multiple parts or magnetic mechanisms. If there is anything special for the HSVS, it is with respect to its requirement for fast response. The impact of the latching mechanism due to faster response time must be minimized and could be affected by added mass, rotating joints, or demagnetizing time. To latch the contact open, faster opening speed leaves less time for a latching mechanism to operate. In a conventional switch or circuit breaker, the time for the latch to operate is on the order of tens of milliseconds. For the new designed HSVS, the latching operation must be completed within 0.5 ms. The challenges mandate a simplified latching mechanism that contains less parts and joints, although more complex alternative solutions may still exist. The final implementation employed an over-toggle latching mechanism design for the HSVS, which is able to latch the moving contact in both closed and open positions.

Vacuum Interrupter

A mechanical switch for an MVDC hybrid circuit breaker application must be capable of (a) switching off the circuit quickly to assist the completion of fault current commutation and (b) withstanding the high rate of rise of interruption recovery voltages generated by the power electronic interrupter during its turnoff operation, especially when very fast response time is required. The recovery voltage rate of rise can be more than 5 kV/μs, even greater than that of the standard lightning impulse voltage, which is about 3.5 kV/μs [17]. These required capabilities make vacuum interrupters stand out from all other mature switch technologies in medium-voltage applications. The advantage is rooted in the vacuum interrupter's superior dielectric strength and its quick recovery from the transient state during current switching or interruption [13] (see Table 11.1). The advantage makes vacuum interrupters particularly suitable for MV HCB applications where fast response time is demanded because the high dielectric strength allows for a smaller contact gap and the shorter distance reduces travel time. In addition, the quick recovery of dielectric strength makes current interruption faster which reduces the time of current commutation. Finally, short-contact travel distances require less energy to drive the actuator which reduces the size of actuation mechanism.

Table 11.1 Dielectric strength of common insulation materials used in medium-voltage rated equipment

Dielectric strength (kV/mm) (in general good condition)	
Vacuum	~20
Mineral oil	~15
SF6	~10
Dry air	~3

Fig. 11.4 Vacuum interrupter (VI) employed in the HSVS

Figure 11.4 shows the vacuum interrupter used in the HSVS. It measures about 50 mm in diameter and 75 mm in length. During the current interruption operation of the HCB, the current commutation is completed before the vacuum contacts separate. At the same time, it is subject to peak transient interruption recovery voltage generated by the power electronic interrupter of 12 kV with a rate of rise greater than 5 kV/μs. The stable open gap is set to 6 mm to reliably withstand 20 kV for 1 min, in case extended voltage withstanding is needed.

Figure 11.5 illustrates the anatomy of a typical vacuum interrupter. Medium-voltage vacuum interrupter technology has been well developed over more than 60 years and is used in many applications, from load switching to generator protection. There are many variables which can be managed in a design, such as contact material, contact structure, shield profiles, contact position, or electrode lengths, among others, to address the needs of a particular application. These needs may include dielectric performance, interruption capacity, energy efficiency, etc.

Though it is mature in technology for conventional designs and applications, the HSVS for HCB application poses a new challenge to the vacuum interrupter – the mechanical life of its bellows under repeated high-speed impacts. In a vacuum interrupter, the bellows, which are usually formed from thin stainless steel sheets, are subjected to impulse force and motion as the contact is made to open and close with different acceleration rates, speeds, and often sudden stops. With continuous improvement over the decades, the mechanical life of the bellows in a conventional circuit breaker's vacuum interrupter is in the range of 10,000–30,000 operations. For contactors' vacuum interrupters, the bellows' mechanical life may exceed 1×10^6 operations, where the contact gap can be smaller and contact moving speed can be slower. In all these, the contacts' speeds are normally within 2 m/s.

The HSVS performance specifications stated above are not from calculations or simulations. Rather, they are instead from real tests with real circuit breakers and switches. They are accumulated general results. There may be no practical tool to allow plugging in parameters to predict reputable mechanical life of VI bellows. Nevertheless, a large variety of bellows are commercially available designed to

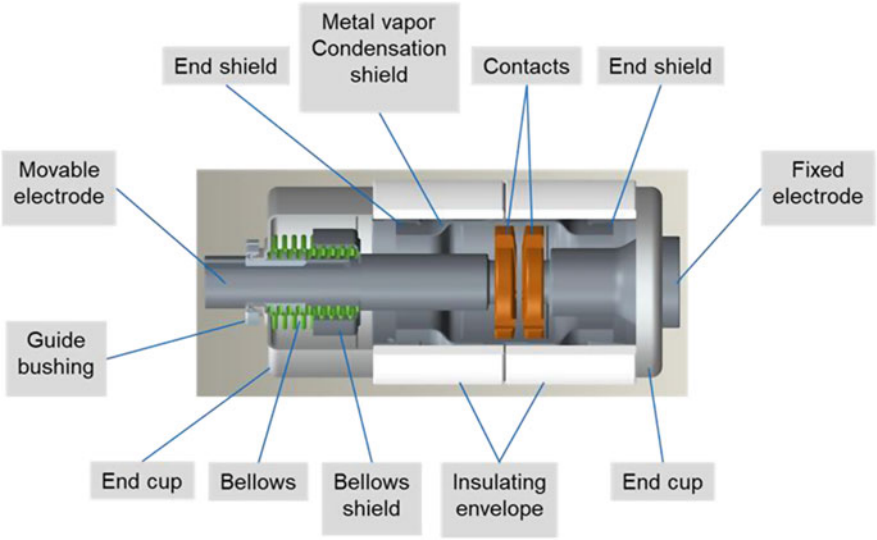

Fig. 11.5 Vacuum interrupter (VI) anatomy

many different service conditions in vacuum interrupter applications with accumulated knowledge and experiences, especially from reputable manufacturers. Although the conditions of the vacuum interrupter used in the newly designed HSVS are considered unusual at this time, to select its bellows from the commercially available options is a practical first step. Initial experiments indicated that its mechanical life has a good chance to be in range of that for conventional vacuum circuit breakers. Careful future optimization of the actuation and damping will only improve its longevity.

3.3 Power Electronic Interrupter (PEI)

The power electronic interrupter (PEI) is the third key subsystem in the HCB and functions essentially as a high-power solid-state switch. It is responsible for interrupting the fault-current and ultimately driving it to zero in a very short period after the VI completely opens. This is enabled by creating a transient voltage across PEI higher than the DC source voltage. Therefore, the PEI in the HCB acts very similar to a solid-state circuit breaker (SSCB), which needs power semiconductor devices and energy absorption components like MOV. The key difference between PEI in HCB and SSCB is that the PEI only needs to carry the fault current for a short time period like a pulse current. This requires the devices in PEI with a high pulse current capability and a large thermal capacitance. PEI can be designed with power semiconductor devices, such as IGBT, IGCT, or SiC MOSFETs. Among

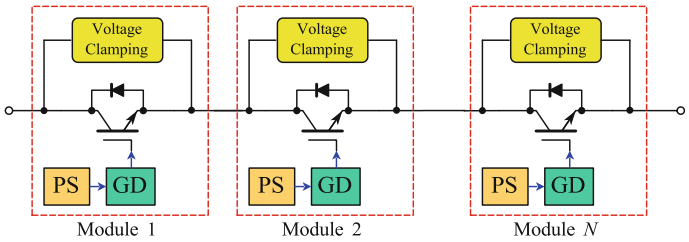

Fig. 11.6 Modular PEI with distributed voltage clamping circuit

them, IGBT presents more design flexibility and benefits in PEI as it can handle high *di/dt* than IGCT and also has a high pulse current ratio due to its large chip size than existing SiC MOSFETs.

As PEI needs to sustain a higher voltage than the DC bus voltage during the current breaking transient, MV IGBTs of 3.3 kV or higher ratings can be considered. To reach even higher blocking voltage than that of a single MV device, series connection of IGBTs can be considered, and the main challenge is the voltage sharing [18, 19]. Therefore, the modular structure as shown in Fig. 11.6 has been adopted in most PEI topologies [20]. For instances, the Zhangbei 500-kV HVDC HCB uses 320 series modules to realize the required blocking voltage requirement [21]. The distributed voltage clamping circuit paralleled with low-voltage device could be regarded as one module, whose maximum voltage is thereby limited and balanced by the voltage clamping circuit. Besides the low cost and high flexibility, another advantage of this modular approach is that the cascading damage can be avoided even when one of the series modules is damaged.

Since the modular structure can handle high clamping voltages, the challenge is to achieve conduction and safe interruption of the fault current. High peak current capability and high transient thermal capacitance are the two key parameters used to select the power devices. The peak current capability is mostly associated with the device material and structure, while the transient thermal capacitance is mostly related to the physical size of the device and the package.

Voltage clamping circuit can help suppress the overvoltage across the device and absorb the energy stored in line inductor. Various voltage clamping components have been discussed in [22, 23], including the metal oxide varistor (MOV), transient voltage suppression (TVS) diode, resistor-capacitor (RC) snubber, etc. The design of voltage clamping circuit is typically driven by the peak clamping voltage, the leakage current at nominal voltage, and the total absorption energy. MOV is a nonlinear resistor with its resistance value as a function of the applied voltage [24]. When a low voltage is applied, it has a very high resistance, whereas it has the lowest resistance with the clamping voltage applied. Besides, there is a steep front effect to affect the peak voltage, which is proportional to *di/dt* [25].

To reduce the *dv/dt* and *di/dt* impact to the device and the gate-driver circuit, a snubber circuit is usually needed in PEI. Figure 11.7 shows a typical RC-based

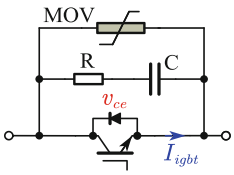

Fig. 11.7 MOV paralleled with RC snubber

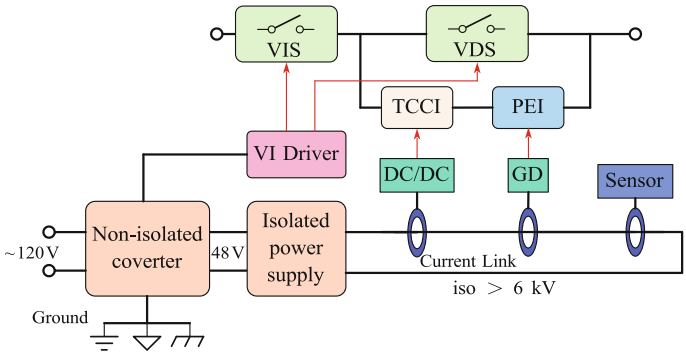

Fig. 11.8 Auxiliary power supply architecture for the HCB system

snubber circuit that is paralleled with the MOV. The RC snubber could also help lower the turnoff power loss and limit MOV voltage overshoot [20].

In the whole system, the auxiliary power supply needs to deliver the power for all electronic and sensing components in HCB. The drive circuit for the Thomson coil of the vacuum disconnect switch (VDS) (a.k.a. the high-speed vacuum switch) and VIS does not need isolation, because the insulation layer is inserted between the coil and the VI [15, 26]. However, an isolated power supply with enough insulation capability is necessary to drive the TCCI, PEI, and some sensors as shown in Fig. 11.8. The insulation capability should be at least higher than the maximum voltage seen by the system, i.e., the clamping voltage. This high-insulation capability makes the auxiliary power supply special than other applications. There are many auxiliary power supply solutions that offer high-insulation capability. But considering the different locations and power rating of multiple loads, a current-link single-turn transformer-based power supply is considered in this work [27].

As shown in Fig. 11.9, the primary circuit can provide a constant sinusoidal current i_p, while the secondary side uses a diode bridge and a boost converter to regulate the output voltage. By changing the turn number of secondary winding, the output power rating is changed accordingly. Electrical insulation is provided by the single-turn transformer. Within the PEI unit, due to the modular structure, the gate-driver power supply for IGBT in each module should be isolated with each other. Although the gate-driver voltage potential difference between the first module and last module will be the total clamping voltage, the voltage potential difference between two nearby modules will not exceed the clamping voltage of selected MOV. Therefore, a cascade power supply architecture can be adopted inside PEI to reduce

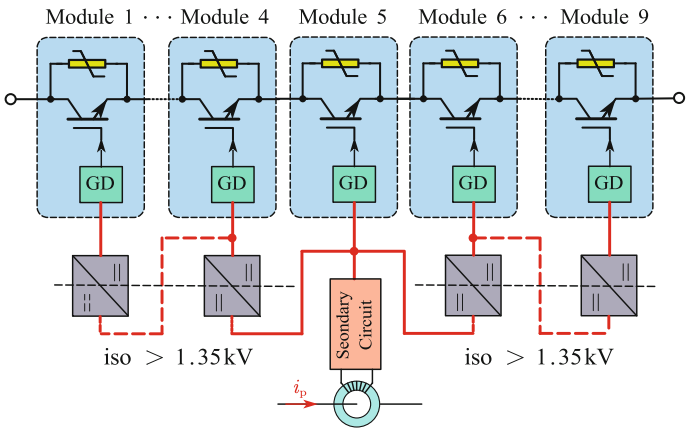

Fig. 11.9 Cascaded gate-driver power supplies used in PEI

the isolation voltage requirement for the small gate-driver power supply. As shown in Fig. 11.8, the output of secondary circuit is connected to the middle module, and then the power is delivered to series modules one by one. In this way, the commercial compact DC/DC power supply used for MV IGBT gate driver is sufficient to meet this isolation voltage requirement.

The interruption time of the HCB is predominantly limited by the opening speed of the mechanical contacts, which is greatly slower than that of SSCB. Gap distance and contactor opening speed of the VDS are in the range of tens to hundreds of microsecond per millimeter gap. Only after enough dielectric strength has been established across contacts of the VDS will the PEI be allowed to be turned off as shown in Fig. 11.1 (t_4). Otherwise, the arcing of VDS will occur to commutate the current back to the VDS branch and cause the failure of HCB. A long waiting time for PEI leads to a very large peak current and a long total HCB interrupting time.

In order to reduce the waiting time for the PEI, a staged turnoff strategy is introduced in [28] to make full use of the gap distance curve. Since the PEI consists of series identical modules, they could be turned off sequentially to create a staged clamping voltage waveform as shown in Fig. 11.10. The coordination of the PEI turnoff sequence and opening of the VDS contacts is very important to make sure that arcing will not occur. It can be seen that the peak fault current, total absorption energy, and clearing time will be reduced after applying this staged turnoff strategy.

4 System Control and Integration

Key to the implementation of the hybrid circuit breaker is the coordination and control of all the subsystems described above. As described earlier in the principle

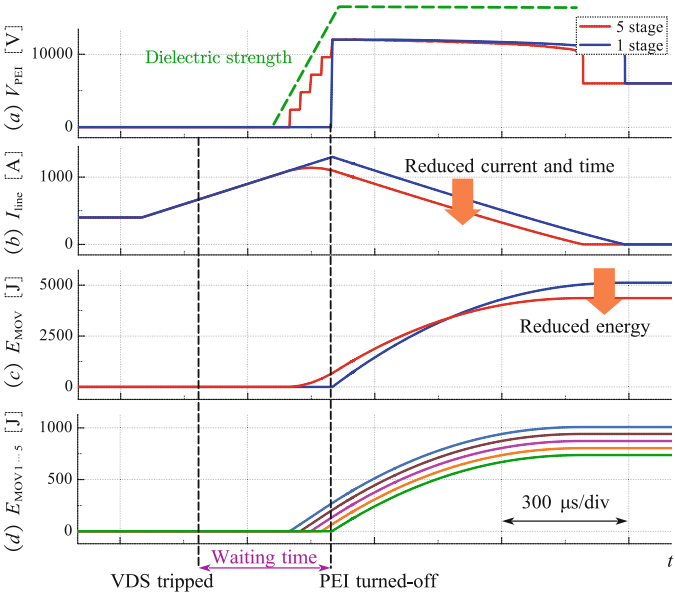

Fig. 11.10 Comparison between single-stage and five-stage turnoff schemes

of operation for the circuit breaker's interruption sequence, each component must operate precisely in the prescribed order to successfully interrupt the current flow. As a designer, one must weigh the options when it comes to implementation of a compact, cost-effective, and robust control scheme. Both centralized and distributed control architectures were considered for this hybrid design. Given the fact that the circuit breaker is primarily a self-enclosed system with the subsystems in close proximity, a distributed architecture provides no particular advantage and would likely add complexity from both hardware and software perspectives. Therefore, a centralized control architecture was employed as it offered the most efficient approach to achieve the precise timing required and avoid potential latency challenges with distributed control methods while minimizing electronic hardware in each requisite subsystem. Figure 11.11 conceptually depicts the hardware control architecture of the HCB system in this work.

By nature, circuit breakers designed for medium voltage have unique requirements when it comes to providing dielectric isolation between the live switching components and the grounded chassis. The necessary circuitry to sense and detect overcurrent faults and control the breaker operation (i.e., trip, reclosure, and nominal switching) is referred to as the "trip unit" and is typically implemented in hardware on a printed circuit board employing a microprocessor in modern circuit breakers. The need to interface with the various components of the HCB (TCCI, PEI, and actuators for the vacuum interrupters), which may be electrically connected and referenced to the medium-voltage potential, presents significant

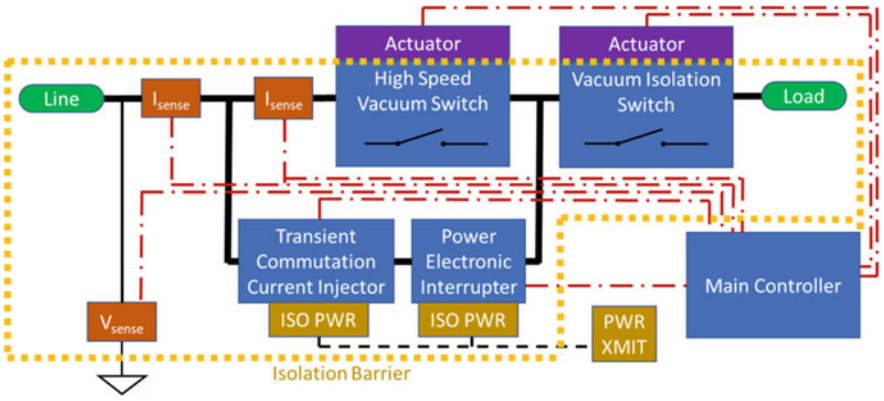

Fig. 11.11 Hybrid circuit breaker hardware control architecture

challenges in trip unit design. The trip unit controller must derive its power, convey command signals, and monitor sensor inputs while maintaining dielectric isolation from the live components. This is fundamental, due not only to the low-voltage nature of integrated circuitry but also to assure safety of the switchgear overall. Industry standards require clearly defined boundaries between ground-referenced components and live elements such that breakdown (i.e., flashover) does not occur and all control elements remain isolated under all circumstances. This includes meeting extreme transient requirements including short-term voltage withstand and basic impulse-level capability (i.e., lightning strike) which can exceed 100 kV depending on breaker rating. Not surprisingly, isolation dictates much of how a circuit breaker's control is implemented.

The means to provide isolated power for the TCCI and PEI power electronic subsystems, as well as sensors, were described in the previous section. In this HCB design, power for the main controller is derived from a dedicated 120-VAC auxiliary control power circuit, which is independent of the medium-voltage mains. While in some low-voltage systems derivation of control power from the mains is possible, it is generally not practical for MV switchgear. Other means of providing control power could also be considered, including lower-voltage DC (24 or 48 V) supplies, but typically they all employ a dedicated source separate from the mains.

Beyond powering the main controller and subsystems is the ability to communicate control signals between these components while retaining MV isolation. Fiber optics are typically employed in MV equipment to meet this requirement. Plastic fiber cables are relatively low cost and provide high dielectric isolation across even short linear lengths if dirt and contamination on the cable surfaces can be environmentally mitigated. Fiber-optic cabling is also not affected by electromagnetic interference (EMI), which is also essential in MV applications where the field intensities can be extreme. Discrete and serial digital data and command signals can thereby be optically exchanged between the controller and MV-referenced components in the breaker. Magnetically coupled approaches could

also be considered for transmission of both power and data across an electrically isolated barrier. However, depending on the level of isolation needed, implementation of magnetic-based isolation techniques may present significant trade-offs for more extreme applications.

Sensing of current and voltage is particularly challenging for MVDC circuit breakers. AC breakers generally utilize current and potential transformers (CT/PT) to monitor real-time electrical parameters during operation. Unfortunately, neither is capable of measuring DC. Other DC-compatible sensors that were capable of providing isolation needed to be employed in the HCB. Current sensing bandwidth requirements of the TCCI posed the most challenging aspect of the control and drove the decision to utilize noncontact Hall effect current sensing. The analog sensor output signals are provided directly to the central controller rather than a digitized serial data stream to minimize latency in signal processing. This approach does present challenges with EMI and retaining adequate levels dielectric isolation, but at the targeted voltage and current ratings for our prototype, these were manageable.

However, as breaker voltage and current ratings scale upward, a designer must be cognizant of the limitations in state-of-the-art sensing technologies. Commercial off-the-shelf sensors are generally not designed for the rigors of the medium-voltage environment where partial discharge phenomena can compromise component life. Furthermore, in circuit breaker applications, sensors must be able to be subjected to extreme transients without lasting degradation to their performance. Specific design considerations must be made when applying Hall effect, flux-gate, and magneto-resistive current sensing methods to address these extremes. Furthermore, as breaker ratings scale up, so too do the sensing dynamic range requirements, which often leads to compromises in precision and bandwidth. All these aspects must be considered in the control design, and more advancements in current sensing will likely be needed to meet the needs of future high-power MVDC systems.

5 Experimental Results

Experimental validation of the TCCI-based hybrid circuit breaker took an incremental approach, with each subsystem tested individually as a standalone device. This allowed each project development team to work independently at first and to progressively evolve the essential functionality of the subsystem designs prior to completion of the overall control architecture and without impact on other teams. This typically involved functional emulation of other subsystems to validate the basic system-level operation in tests at reduced voltage and current levels. For example, early versions of the TCCI used a commercial off-the-shelf vacuum relay and single-stage IGBT switch to mimic the behavior of the high-speed vacuum switch and power electronic interrupter, respectively, while it was still in development. After first exploring design alternatives in simulation and basic breadboards, multiple iterations of hardware for each subsystem were progressively built and tested, as described in previous sections. Eventually, prototype assemblies

rated for the full 6-kV voltage target were prepared and ready for mating in system integration testing and debugging.

Integration started in the Illinois Institute of Technology (IIT) with the TCCI hardware platform as the base element. This platform was capable of conducting circuit interruption tests at source voltages up to 1 kV and peak currents up to 200 A by discharging a low-voltage capacitor bank to simulate a bolted fault condition. The first step in integration was to replace IIT's original controller, which was only configured to operate the scaled down emulated components, with a full-functional controller with interfaces for the full-scale assemblies. Once the control hardware and software portability were validated, the next step was replacing each emulated component in turn with the fully rated subsystem. These tests validated additional control circuitry and software on the main controller to operate the actual multistage PEI and HSVS actuators with proper timing of the interruption sequence. It was during these tests that some anomalous behavior of the TCCI was observed, stemming from the fact that the single-stage emulated PEI that was used in its development exhibited a much lower on-state voltage drop than the fully scaled PEI design. The higher-voltage drop made it more difficult for the TCCI to commutate higher peak fault current levels. Improvements to remedy the problem have been identified and will be employed in future prototypes. Regardless, the TCCI functioned more than adequately enough to validate the HCB's operating principle at the peak interruption current-level goals for the initial testing milestone of 200-A peak.

The successful rounds of testing at IIT paved the way for the final test series at the Virginia Tech CPES lab at the target full 6-kV rated voltage for the HCB and at higher peak interruption current levels. The final hardware test configuration included the main controller board (with further upgraded software), the nine-stage PEI, the TCCI 1.0 power block, and a new HSVS assembly with integrated high- and low-speed actuators. The mechanical switch assembly also incorporated the vacuum isolation switch (VIS) encapsulated pole unit with actuator, although it was not operated and remained closed throughout the interruption testing, as its operation was not fundamental to the interruption process. In order to also validate the complete HCB packaging concept as much as possible, the electronic PCBs were mounted to a vertical panel adjacent to the HSVS/VIS assembly in nearly identical position as that envisioned for the final HCB prototype. The lab test setup is illustrated in Fig. 11.12.

As before, overcurrent faults were facilitated via discharge of a capacitor bank charged to a predetermined bus voltage, since no continuous MVDC sources readily exist for this type of testing. We utilized CPES's medium-voltage test bay which is equipped with a 2.3-mF capacitor bank rated to 10-kV DC with a charging power supply. Two series configured 6.5-kV IGBT modules served as a test control and emergency interrupt switch, to both initiate the test by applying the 6-kV bus to the closed breaker assembly and also disconnect power if the breaker failed to open within the prescribed timing. Various combinations of series inductance and resistance were used to limit fault current peak and rise time in the form of fixed

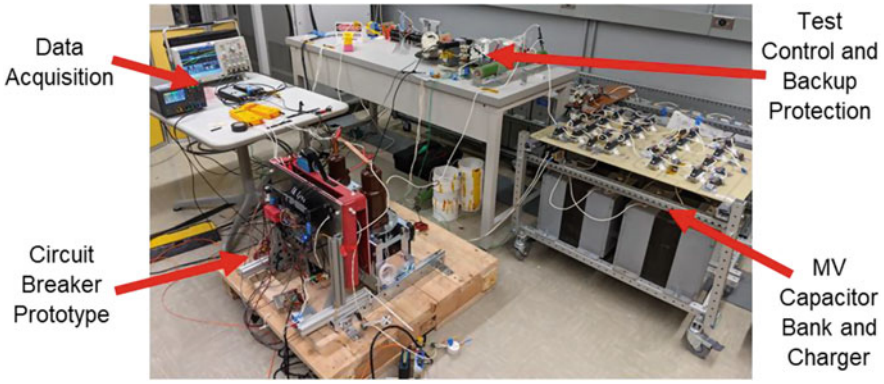

Fig. 11.12 6-kV capacitive discharge interruption testing in lab

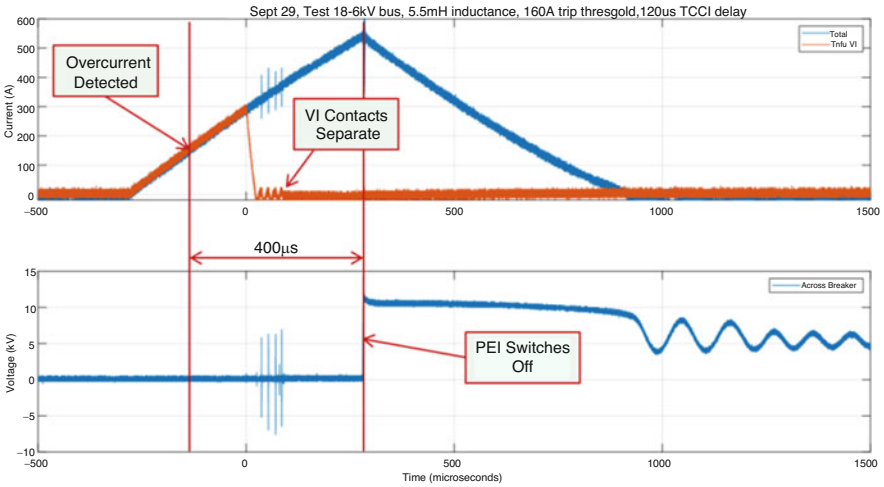

Fig. 11.13 Experimental testing waveforms of HCB fault interruption

spools of wound wire. The test setup and breaker were remotely operated from a separate control room via fiber-optic communications/control link.

Results of the medium voltage met or exceeded the targeted goals, which were to prove the TCCI-based hybrid circuit breaker concept would work at the full 6-kV rated voltage at peak fault current levels equivalent to those achieved in the previous low-current testing rounds. Figure 11.13 illustrates an example trial showing the breaker's ability to interrupt a 6-kV fault within 400 µs after detection with a peak fault current nearly 540 A. As can be seen in the figure, with overcurrent detection threshold set to 160 A, the TCCI activation is delayed 120 µs before it begins commutation of current from the HSVS to the PEI. Once active, the TCCI regulates the HSVS current to a triangular waveform between approximately + and − 12 A.

Once the HSVS vacuum interrupter (VI) contacts begin to separate approximately 220 μs after fault detection, current through the HSVS is halted and remains zero thereafter. At 400 μs after detection, with the HSVS contact gap now at a distance capable of holding off a 12-kV MOV clamping voltage transient, all nine stages of the PEI are simultaneously turned off, thus completing interruption of the circuit. After the energy stored in the inductor is depleted and the fault current falls to zero, the voltage across the breaker settles to the 6-kV source voltage after a short period of oscillations due to the resonance between the line inductance and the PEI snubber capacitance. This test sequence proved the viability of the HCB's operating principle and exceeded the initial test goals.

6 Concluding Remarks

A prototype circuit breaker capable of protecting medium-voltage DC power systems rated up to 6 kV and 200 A was developed. The breaker's design incorporated a unique hybrid architecture employing a novel means of commutating current between mechanical and power electronic conduction paths in breaker. A transient commutation current injector (TCCI) actively drives the current through the mechanical vacuum switch to nearly zero, allowing the vacuum switch to stop current flow without the current zero crossings inherent in AC systems. Since architecturally the TCCI resides outside the steady-state conduction path for the breaker, efficiency of the breaker exceeds what was previously possible in other medium-voltage DC-capable designs.

The performance design goals of this project were based on a notional concept, loosely aligned with requirements for an MVDC shipboard application for the US Navy. Currently, however, there are no true commercial or military applications that precisely match the current ratings of this prototype design, so no plans are in place yet to industrialize it. Nevertheless, the project succeeded in demonstrating that a hybrid circuit breaker based on this novel architecture is indeed a practical approach and could serve as an enabler for the deployment of MVDC systems in a variety of markets (e.g., utility distribution, shipboard power, electric rail, data centers, offshore wind and oil platforms, MV photovoltaic power, fast electric vehicle charging, aerospace, etc.). At the time of this writing, analysis is underway to assess the scalability of this approach for higher voltage and current ratings. Indications at this time are that most MVDC systems will require circuit breaker protection current ratings of 2000–4000 A based on very early-stage system concepts and by drawing analogies from legacy AC systems. It is the team's aspiration that this hybrid approach could be scaled to be compatible with system voltages up to 50 kV or more through multistage series configurations. Understandably, to realize such designs, more research will be required to assess the design trade-offs, including evaluation of available and new power semiconductor devices, sensing technology, capacitive storage elements, high-power density inductive current limiting, and optimization of vacuum interrupters for this higher-voltage range. As an example,

one potential enabler for this could be leveraging wide-bandgap semiconductors capable of voltage ratings beyond what silicon can achieve. This could reduce the number of devices needed in series to implement the power electronic interrupter subsystem.

In order to make MVDC systems a reality, work still remains to study the value propositions MVDC can provide in all the potential markets. Benefits in terms of ROI, efficiency gains, system reliability, and utilization of existing infrastructure need to be quantified through modeling and eventual deployment of pilot project hardware installations. One of the primary objectives of this project was for the development of the prototype to serve as a linchpin for the further evolution of MVDC, filling a long-standing gap, namely, the unavailability of capable protection devices. It is our hope that market entities interested in launching new MVDC systems will recognize this new technology and ultimately utilize it to take the next steps toward fruition.

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Chapter 12
Efficient DC Interrupter with Surge Protection (EDISON)

Lukas Graber, Michael Mischa Steurer, Maryam Saeedifard, Zhiyang Jin, Qichen Yang, and Maryam Tousi

1 Introduction

Several different hybrid solid-state/mechanical breaker topologies have been proposed and tested over the years [1–3]. They all aim at bypassing the solid-state portion of the breaker by a mechanical switch in order to reduce on-state losses. One of the major challenges with such an approach is the commutation process of the current from the mechanical switch to the semiconductor path. The mechanism of current commutation is based upon the initiation of a superimposed loop current, which flows in the opposite direction of the main current in the mechanical switch and rises much faster than the main current. Eventually, the sum of the main current and this counter current reaches zero. At that time, the mechanical switch can start gaining voltage withstand capability. To create this counter current flow, the authors in [2] allowed the mechanical switch to produce a voltage drop as an arc developed between the fast opening contacts. Once the arc extinguished at the zero crossing, the still opening mechanical contacts had to keep on traveling a certain distance for the switch to gain its required voltage withstand capability. While this approach certainly minimized the overall losses of the hybrid breaker by completely bypassing the semiconductor path with a mechanical switch, the additional time for arcing and subsequent voltage recovery after the arc rendered this approach suboptimal. In order to avoid any arcing between the mechanical contacts, the authors in

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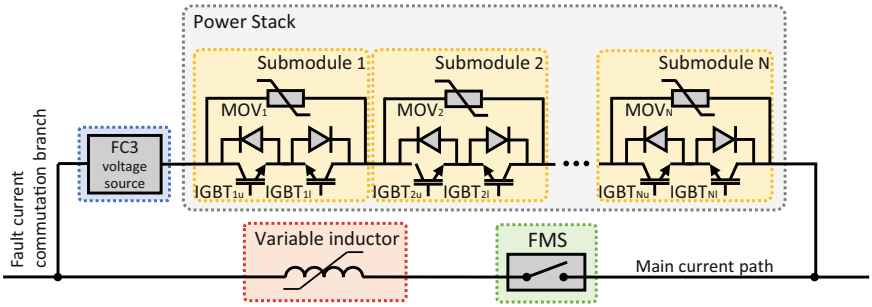

Fig. 12.1 Topology of EDISON with main current path and fault current commutation branch

Table 12.1 Target specifications for EDISON

Rated voltage	12 kV (DC)
Continuous current	2 kA
Trip criteria	3 kA and 40 A/μs
Time for fault current limitation	200 μs
Total opening time	450 μs
Minimum source inductance	300 μH
Peak fault current	8 kA
Maximum energy to absorb during one event	30 kJ

[3] inserted another semiconductor switch into the main current path. That auxiliary switch was designed for withstanding only a fraction of the rated system voltage and thus only caused a modest increase in overall losses when closed.

The new topology of the EDISON breaker described herein (as shown in Fig. 12.1) combines the advantages of both designs: the extremely low-power losses in the closed state of the mechanical switch and the increase in gaining voltage withstand capability by avoiding any arcing in the mechanical switch. This is accomplished by inserting a controllable voltage source into the fault current commutation branch. This fault current commutation circuit (FC3) voltage source causes voltage within the commutation loop in the same direction as the auxiliary switch in [3]. However, since it is not in the main current path, it does not contribute to losses when the hybrid breaker is closed. The efficiency, the power density, and the response time of this topology are further improved by the synergistic combination of the major components of EDISON such as the new mechanical switch, the fault current commutation circuit, and a new control strategy. These components are explained in detail in the next sections. Table 12.1 lists the complete set of ratings of EDISON.

2 Design and Topology

A digital controller within the EDISON breaker senses the fault current and initiates the sequence of events once the trip conditions (i.e., a combination of current level and rate of rise) are met. First, all IGBTs are turned on to allow the FC3 voltage source to commutate the current from the main path to the fault current commutation path. As the current in the main path reaches zero, the overarching controller commands the FMS to open. As it gains the necessary voltage withstand capability during opening, the controller turns off one IGBT after the other which sequentially inserts the MOVs (as shown in Fig. 12.2) and thus builds up voltage drop across the EDISON breaker. This stepwise increasing voltage drop reduces the rate of rise of the fault current, which subsequently reaches approximately the same but negative initial value, which drives that current to zero as shown in Fig. 12.3. In order to finally provide galvanic isolation between the two main terminals, the EDISON breaker requires an external disconnect switch (not shown in Fig. 12.1).

Before closing the EDISON breaker, the controller recharges the FC3 voltage source so it becomes ready for an immediate opening action after the FMS eventually closes and a fault occurs in the system. To close the breaker, the controller turns on the IGBTs sequentially, thereby stepwise reducing the voltage drop across the breaker. During that sequence, the controller compares the current against the expected current in a non-faulted system. If a fault is sensed during this initial sequence, the IGBTs are all turned off again and the breaker locks out. Otherwise, all IGBTs are eventually turned on, and the load current flows in the fault current commutation path. Since that path is not designed for continuous current flow, the

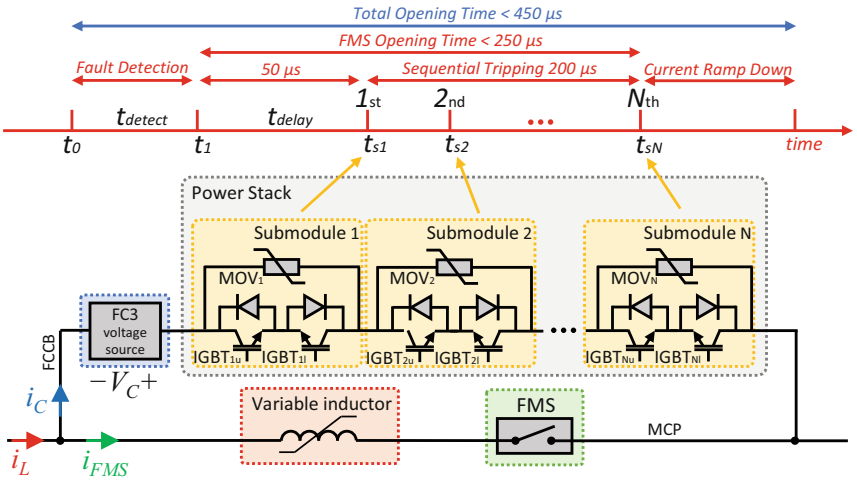

Fig. 12.2 Circuit diagram of the breaker with N breaker submodules

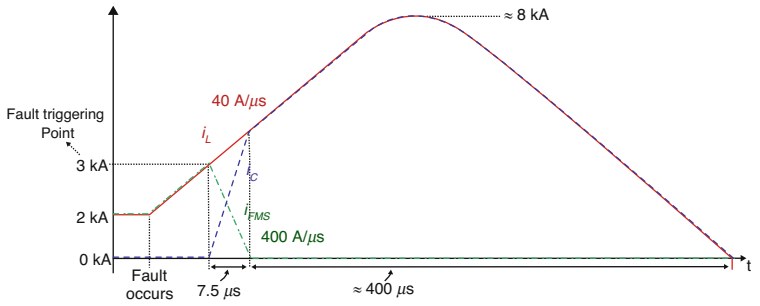

Fig. 12.3 Simulated current waveforms when a fault occurs

FMS must close quickly to allow the load current to naturally commutate to the low impedance main current path formed by the then closed FMS. At that time, the EDISON breaker is ready to trip for another fault-limiting and interruption sequence if the controller senses the necessary condition.

The FC3 voltage source is a controlled voltage source, which – if turned on – causes the fast-rising current in the loop formed by the two current paths shown in Fig. 12.1. This causes the current in the main current path to drop while the current in the fault current commutation path rises (along with the rise of the actual fault current in the power system). The FC3 voltage source is designed to ensure a rate of rise of that loop current approximately one order of magnitude greater than the rate of rise of the fault current as shown in Fig. 12.3. Once the current in the main current path reaches zero, the challenge with this approach is to maintain approximately zero current to allow the FMS to open. The solution is to introduce a variable inductor in the main current path. This inductor is designed to saturate above several amperes, thus providing a very small inductance during the commutation process itself. Only when the current falls below the saturation level will this inductance increase by at least two orders of magnitude. Several ferrite rings placed over a cylindrical copper bus bar, at the main current path, provide sufficiently large inductance. The unsaturated inductance significantly slows down the remaining falloff current in that path. This provides the necessary condition for the FMS to open while absorbing only extremely low energy during contact separation. Subsequently, the gap between the FMS contacts gain voltage withstand capability, which as the gap increases in turn allows for the introduction of ever increasing voltage drop by sequentially opening IGBTs and thus inserting one MOV after the other into the circuit.

3 Fault Current Commutation Circuit

The function of fault current commutation circuit (FC3) is to commutate the fault current from the FMS branch to the fault current commutation branch (FCCB)

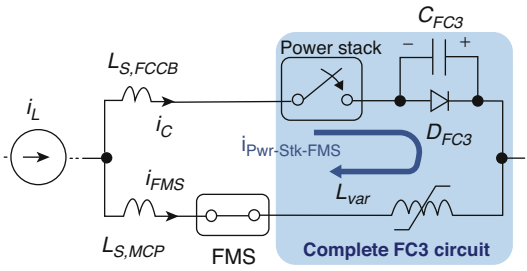

Fig. 12.4 Equivalent circuit diagram of EDISON, including FC3 circuit. The power stack is shown symbolically as an ideal switch

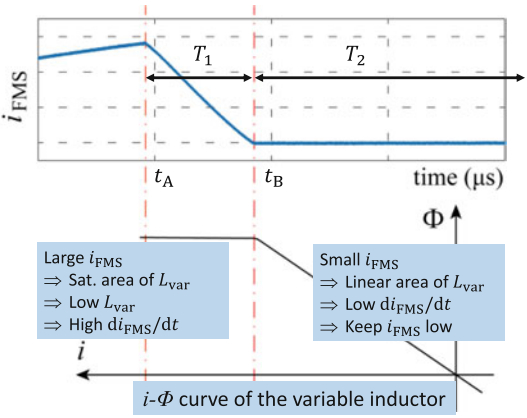

Fig. 12.5 Fault current commutation period and zero-crossing period – function of the variable inductor

and hold the current though the FMS at low level for a certain time to facilitate the opening of FMS. The complete FC3 circuit, including a pre-charged capacitor (C_{FC3}), a bypass diode (D_{FC3}), and a variable inductor (L_{var}), is illustrated in the blue block in Fig. 12.4, where the power stack is depicted as a closing switch as it triggers the fault current commutation process. It is noteworthy that, except for the charging circuit (not shown for simplicity), the major parts of FC3 circuit are passive components.

Figure 12.5 illustrates the current regulated by the FC3, where the variable inductor plays an important role. The whole process contains two phases, i.e., commutation phase, T_1, and zero FMS current phase, T_2.

At t_A, the power stack receives the triggering signal from the controller to turn on the switch. Subsequently, C_{FC3} starts to discharge, and $i_{PwrStk\text{-}FMS}$ starts rising (see Fig. 12.4), which leads to the rapid decrease of i_{FMS} until t_B. In the time frame T_1 (from t_A to t_B), as illustrated in Fig. 12.5, the large i_{FMS} keeps the magnetic core of L_{var} saturated and, thus, keeps L_{var} low. Therefore, the variable inductor does not inhibit the rapid fault current commutation process.

At t_B, i_{FMS} decreases to a very low level so that the magnetic core of L_{var} starts to work in the non-saturated region, thus significantly increasing the inductance in FMS path. Therefore, during the time period T_2, di/dt is kept at a very low (still negative) level which in turn keeps the current at a low level for the time required

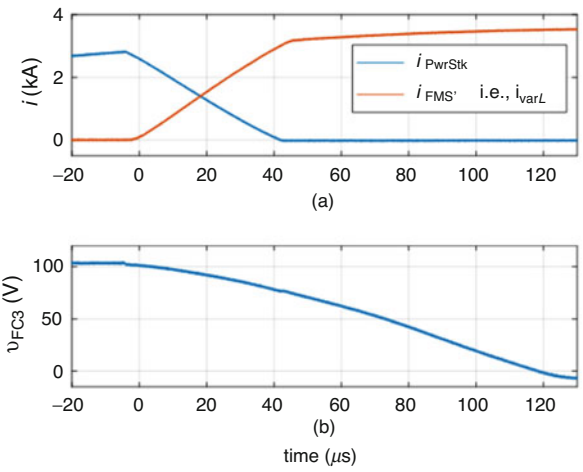

Fig. 12.6 Experimental waveforms of the fault current commutation period and zero-holding period: (**a**) current through FMS (i.e., variable inductor) and current through power stack, (**b**) voltage across the capacitor of the FC3

to open the FMS. Once the FMS has interrupted the small residual current and started to build up voltage withstand capability, the sequential tripping scheme can commence.

Figure 12.6 illustrates the experimental waveforms during the fault current commutation period and the zero-holding period. After the IGBTs are turned on, the capacitor in FC3 starts to discharge, as shown in Fig. 12.6b. Because of the reverse current injected by FC3 and the small loop inductance (with fully saturated variable inductor) in Fig. 12.4, current through the FMS, i.e., current through variable inductor, decreases to zero with a rate of change of 62 A/μs, and thus the fault current commutates to the power stack, as illustrated in Fig. 12.6a. When the current through the variable inductor becomes small enough to bring that inductor out of saturation, its inductance increases by approximately two orders of magnitudes. This in turn reduces the rate of change of the current through the FMS and hence holds it around zero to allow zero-current (arc-less) opening of the FMS.

Figure 12.7 shows the zoomed-in voltage and current of the variable inductor during the zero-holding period, during which the current through the variable inductor is less than 5 A, as illustrated in Fig. 12.7a. Figure 12.7b shows that, during the process, with the decrease of the FC3 voltage, the voltage across the variable inductor increases gradually.

4 Sequential Insertion Control Scheme

To expedite the operation of the breaker, an improved insertion control strategy called "sequential insertion" has been proposed to precisely trip the breaker submodules [4]. Compared to the conventional insertion strategy, in which all semiconductor switches of the N breaker submodules are switched off simultaneously,

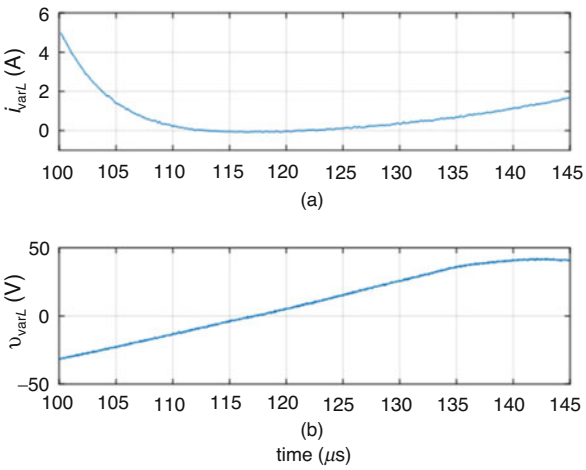

Fig. 12.7 Experimental zoomed-in waveforms during the zero-holding period: (**a**) current through the variable inductor, (**b**) voltage across the inductor

sequential insertion strategy trips submodules sequentially, following the optimal order to speed up fault clearance.

The opening of the breaker is divided into N stages, as shown in Fig. 12.2. Consisting of IGBTs and their paralleled metal oxide varistors (MOVs), each submodule is treated as an individual breaker. The trip signals for these submodules are generated sequentially at $t_{s1}, t_{s2}, \ldots, t_{sN}$. The MOVs within these submodules are rated at lower voltages, enabling them to introduce a lower-voltage stress when inserted into the circuit individually. By inserting these submodules sequentially, the voltage across the FMS is built up step by step. Since the voltage withstand capability of the FMS is established incrementally [3–7], the breaker submodules can be tripped earlier, even before the FMS is fully opened. For example, the switches of Submodule 1 are commanded to open at t_{s1}, which is earlier than the original tripping instant in the conventional method. The fault current tends to increase slowly with the MOVs in Submodule 1 being inserted. Sequentially, Submodule 2 is tripped at t_{s2}; thereby, the rate of rise of fault current is further limited. This process is repeated until all of the N submodules are switched off, which allows the voltage across the hybrid circuit breaker to increase incrementally. Consequently, the fault clearance time can be reduced, and the overvoltage and the overcurrent stresses on the system are relieved as well.

The results of the comparison between the strategy in which all breaker submodules are tripped simultaneously and the proposed sequential insertion strategies are provided in Fig. 12.8a, b show the voltage and current waveforms of the breaker under the sequential insertion strategy. A fault occurs at $t = 1$ ms and is detected 30 μs later. The fault current is then routed from the main current path to the fault current commutation branch through the operation of FC3. After a 50-μs delay for the opening of the FMS, in the sequential insertion case, the breaker submodules (ten submodules) are tripped one by one. On the contrary, as observed from Fig. 12.8c, d, all breaker submodules are opened simultaneously at $t = 1.3$ ms. As shown in Fig.

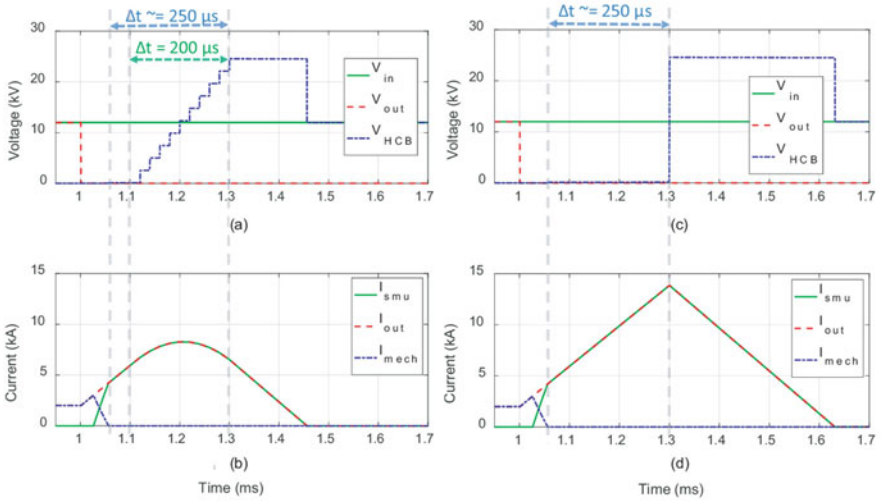

Fig. 12.8 Simulated results comparing simultaneous and sequential insertion for a breaker with ten submodules: (**a**) voltage across branches of breaker submodules in sequential insertion case, (**b**) current flowing through the breaker branches in sequential insertion case, (**c**) voltage across branches of breaker submodules in simultaneous insertion case, and (**d**) current flowing through the breaker branches in a simultaneous insertion case

12.8a, b, with the sequential insertion strategy applied, the switches of Submodule 1 open around 200 μs earlier than the simultaneous case. As a result, the fault current reaches a lower peak (8 kA vs. 14 kA) and can be cleared earlier.

However, apart from the advantages offered by the sequential tripping, the energy absorbed by each module tends to be distributed unevenly. Those modules that are tripped earlier tend to dissipate more energy, making them vulnerable to thermal overloading. Assuming that the clamped voltage of a MOV inside Submodule i is $v_{\mathrm{EAP},\,i}$ and the corresponding current is $i_{\mathrm{EAP},\,i}$, the energy absorption of the MOV i can be expressed by

$$W_{\mathrm{EAP},i} = \int_{t_{ai}}^{t_{bi}} v_{\mathrm{EAP},i} i_{\mathrm{EAP},i} dt, \tag{12.1}$$

where $W_{\mathrm{EAP},\,i}$ is the absorbed energy and t_{ai} and t_{bi} are the starting and ending time instants of insertion of the MOV in Submodule i, respectively. Therefore, the absorbed energy of each MOV is largely proportional to the duration in which each of them is inserted into the circuit. The energy difference is enlarged when a higher delay is applied between each module.

To address this issue, a modified sequential tripping strategy is proposed to equally distribute the energy among all MOVs, which adjusts the MOV insertion timings in such a way that the voltage withstand capability established by the FMS

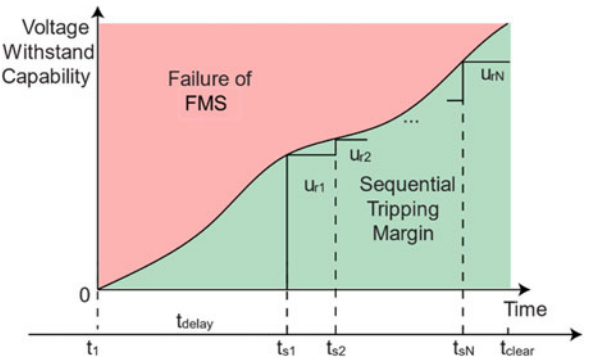

Fig. 12.9 Generic voltage withstand capability versus opening time of the FMS

can be optimally utilized at every instant while ensuring successful opening of each submodule.

The voltage withstand capability of the FMS is a function of time, largely determined by its contact travel curve and insulation medium [5–8]. This capability is built up with the increment of distance between the contacts [8, 9]. A non-decreasing characteristic of the FMS is generally assumed and depicted in Fig. 12.9. At the time Submodule i opens, the inserted voltage established by the MOVs is applied to the FMS. At this moment, the corresponding voltage withstand capability of the FMS should be higher than this voltage. As shown in Fig. 12.9, the tripping schedule is determined by both the rated voltages u_r and tripping stages N. These two parameters will ultimately influence the system performance metrics, i.e., fault clearance time, overcurrent, overvoltage, and energy absorption.

Typically, a module with a smaller u_r can be tripped earlier provided that a smaller additional withstand capability is required. However, this will result in an increment of the tripping stages. A large number of stages will add to the complexity of the controller and will potentially lead to a higher overvoltage. Additionally, the clearance time cannot be further improved with too many stages involved. To this end, the parameters of the sequential tripping should be selected wisely considering the trade-offs between different system metrics. An optimization should be performed to achieve such a balance. In a real application, it is likely that the MOVs within the breaker modules are rated at the same level, for the sake of the simplicity of manufacturing maintenance. On the other hand, these MOVs could be rated at different levels from an economical perspective. Thus, two optimization approaches are provided with respect to these considerations.

Approach 1

In the first approach, the rated voltage of the MOVs of all submodules is set to be the same. The task is then to minimize the system performance metrics with respect to this rated voltage u_r and the number of tripping stages N.

In case u_r and N are selected, the earliest tripping instants of each submodule, t_{si}, can be determined from the characteristic of the FMS. To prevent the FMS from failure, Submodule i should not be opened until the FMS is able to withstand

the voltage inserted by the MOVs. As shown in Fig. 12.9, at each instant t_{si}, an additional voltage u_{ri} is added on top of the previously accumulated voltage through the insertion of Submodule i. Intuitively, the earliest trip instant of Submodule i is the moment when this accumulated voltage curve intersects with the FMS characteristic curve. With this approach, t_{si} can be written as

$$t_{si} = f_1\left(u_r, N\right). \tag{12.2}$$

The expressions of the current flowing through DC circuit breaker, i_{dc}, and the voltage across DC circuit breaker, v_{dc}, are given as

$$i_{dc} = f_2\left(u_r, N\right) \tag{12.3a}$$

$$v_{dc} = f_3\left(u_r, N\right) \tag{12.3b}$$

where these transient functions can be obtained through the time-domain calculation method proposed in [4]. In this way, the system metrics, i.e., peak overcurrent i_{max}, peak overvoltage v_{max}, fault clearance time t_{clear}, and energy absorption W_{sum}, are given as functions of u_r and N as

$$i_{max} = g_1\left(u_r, N\right), \tag{12.4a}$$

$$v_{max} = g_2\left(u_r, N\right), \tag{12.4b}$$

$$t_{clear} = g_3\left(u_r, N\right), \tag{12.4c}$$

$$W_{sum} = \sum_{k=1}^{N} W_{EAP,i} = g_4\left(u_r, N\right). \tag{12.4d}$$

Each of the four metrics can be used as the objective function for the optimization problem formulated in (12.5)

$$\underset{u_r, N}{\text{minimize}} \quad g\left(u_r, N\right) \tag{12.5a}$$

$$\text{subject to} \quad N_{min} \le N \le N_{max}, \tag{12.5b}$$

$$u_{r,min} \le u_r \le u_{r,max}, \tag{12.5c}$$

$$u_r \times N \le u_{r,sys}, \tag{12.5d}$$

where $g(u_r, N)$ represents one of the system metrics in (12.4). Inequalities (12.5b) and (12.5c) ensure N and u_r stay within their reasonable limits. The total rated voltage of the DC circuit breaker is limited by the insulation capability of the system, $u_{r,sys}$. This constraint is given by (12.5d).

A set of u_r and N is obtained by solving the optimization problem (12.5). However, the energy among N submodules is not strictly balanced using the modified sequential tripping strategy. Considering that the tripping intervals are not necessary to be the same, the $N - 1$ tripping instants t_{s2}, t_{s3}, ..., t_{sN} are open to be manipulated around the previous values to balance the energy. Given u_r and N, each

$W_{\mathrm{EAP},\,i}$ can be written as a function of $t_{\mathrm{s}2}$, $t_{\mathrm{s}3}$, ..., $t_{\mathrm{s}N}$. Solving a set of $N-1$ energy balancing equations $W_{\mathrm{EAP},\,i} = W_{\mathrm{EAP},\,i+1}$, $i \in \{1, ..., N-1\}$ with respect to the $N-1$ tripping instants, the energy of each submodule is kept equal.

Approach 2

In some cases, the MOV within each submodule can be sized in such a way that the cost is minimized. The ratings of these MOVs can thus be determined individually as $u_{\mathrm{r}1}$, $u_{\mathrm{r}2}$, ..., $u_{\mathrm{r}N}$. It is assumed that the summation of all rated voltages is $u_{\mathrm{r,\,sys}}$ and the number of tripping stage N is fixed.

Based on the time-domain calculation method provided in [4], the four system metrics can be written as functions of the rated voltage of each MOV. The optimization problem is formulated as

$$\underset{u_{\mathrm{r}1},\ldots,u_{\mathrm{r}N}}{\text{minimize}} \qquad h\left(u_{\mathrm{r}1}, \ldots, u_{\mathrm{r}N}\right) \tag{12.6a}$$

$$\text{subject to} \qquad \sum_{k=1}^{N} u_{\mathrm{r}k} = u_{\mathrm{r,sys}}, \tag{12.6b}$$

$$u_{\mathrm{r,min}} \leq u_{\mathrm{r}k} \leq u_{\mathrm{r,max}}, k \in \{1, \ldots, N\}, \tag{12.6c}$$

where $h(u_{\mathrm{r}1}, \ldots, u_{\mathrm{r}N})$ represents one of the system metrics with respect to $u_{\mathrm{r}i}$.

5 Power Stack

The purpose of the power stack is to produce the required voltage drop and absorb the residual energy after the fault current is commutated to the main breaker path. It is composed of N series-connected submodules, as shown in Fig. 12.1, where each submodule consists of parallel-connected metal oxide surge arresters and semiconductor switches. Series connection of these modules is required to (i) limit the voltage per submodule to a value manageable by the semiconductor switch, (ii) allow for the application of the sequential tripping method, and (iii) provide scalability of the power stack, which makes it applicable to different voltage levels. The optimization process of how many series-connected submodules are required as well as the electrical ratings of the semiconductor switches and surge arrestors is based on the required lifetime of the devices, or switching operations of the EDISON breaker, and was determined using a set-based design approach [10].

The power stack, as currently implemented in EDISON, needs to manage fault current flowing only in one direction. To make the power stack bidirectional, several ways to arrange semiconductor switches in each submodule have been proposed in the technical literature. Reference [11] reviews a few possible semiconductor switch arrangements; however, most of them suffer from the following issues:

(i) High number of required semiconductor devices. For example, the configuration in [2] is composed of a full diode rectifier in conjunction with a controllable solid-state device; it requires five semiconductor devices for each submodule.
(ii) Poor scalability, as demonstrated by the topology in [12]. The authors in [12] connect two solid-state switches in parallel to conduct and interrupt fault current from either direction. However, if the system voltage rating changes, the parallel IGBTs may need to be resized and replaced.

In comparison, the topology proposed in [3] addresses the above two issues by connecting controllable semiconductor devices, e.g., IGBTs, in series. This arrangement is scalable because if the working voltage rating is changed, more IGBTs can be added by simply connecting them in series. Furthermore, the topology only requires two semiconductor devices to interrupt fault current coming from either end by connecting them in the opposite directions.

EDISON adopts the topology in [3]. To enhance the reliability of the power stack, $N + 1$ redundancy is considered. This is realized by selecting "fail-short" IGBTs, where press-pack IGBTs are appropriate for this application.

6 Fast Mechanical Switch

The fast mechanical switch (FMS) for EDISON is based on a piezoelectric actuator as the contact actuation mechanism and high-pressure supercritical fluids as the dielectric medium (Fig. 12.10). The FMS is built to achieve a switching time of less than 250 μs, a continuous current rating of 2 kA, and a withstand voltage of 30 kV when the contacts are fully open. The open contact gap distance is 100 μm.

6.1 Piezoelectric Actuator for Fast Switching

Most actuator mechanisms that are used for conventional switchgear, such as spring-loaded mechanisms, hydraulics, pneumatics, and geared motors, are not suitable for fast actuation. Many concepts for fast mechanical switches therefore rely on electrodynamic actuation such as the so-called Thomson coil. These devices often suffer from limited controllability and a nonoptimal contact travel curve. They furthermore require a significant amount of stored energy to create the required high current pulse in the coil. Building up the magnetic field in the coil reduces the responsiveness and requires high-voltage levels to overcome the coil's inductance. Therefore, a different mechanism, based on a piezoelectric actuator, was chosen for the FMS in EDISON.

Piezoelectric actuators are based on a stack of crystalline material with a significant piezoelectric effect such as lead zirconate titanate $Pb[Zr_xTi_{1-x}]O_3$ (PZT). Electrodes connected to the piezoelectric ceramic control the electrostatic

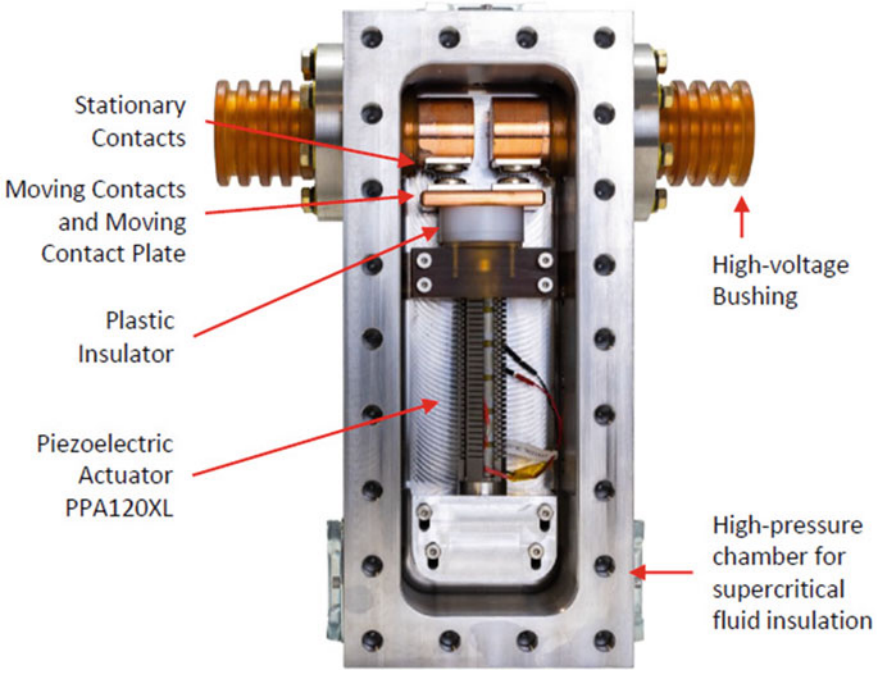

Fig. 12.10 One of FMS designs and its assembly (without showing the lid for the high-pressure chamber). The high-pressure chamber is made of precipitation hardened stainless steel (17-4 PH)

field, which triggers the expansion of the material along the electric field lines. The displacement of the actuator can be controlled precisely at nanometer scale by the voltage across it. This high accuracy of piezoelectric actuators can be used to shape the travel curve, to minimize the travel time, to reduce contact bouncing, and to limit contact wear during switching processes.

However, like Thomson coil-actuated disconnect switches, the dominant challenge for the travel curve of piezoelectrically actuated high-speed disconnect switches is mechanical oscillations. The oscillations will get worse with increasing moving mass as well as with increasing acceleration, which is often required to minimize the switching time. To reduce unwanted oscillations in travel curves, a closed-loop control scheme can be implemented as shown in Fig. 12.11 [13, 14]. Further improvements are currently being implemented by a combination of (i) reduction of moving mass, (ii) individual control scheme of PZT ceramics, and (iii) adopting new actuator materials [15, 16].

6.2 Supercritical Fluids as Dielectric Medium

Piezoelectric actuators have submillimeter contact travel and require a medium with high dielectric strength to withstand voltage when the disconnect switch is open. The

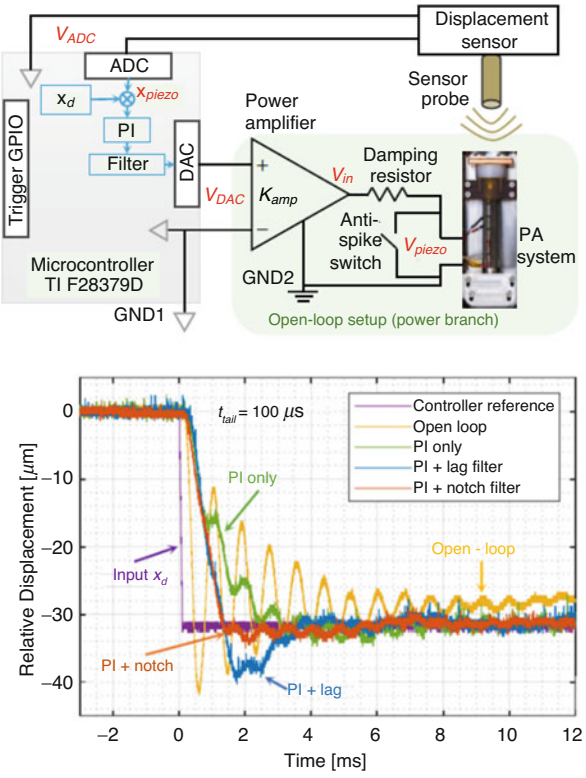

Fig. 12.11 Schematic of the closed-loop control system with a piezoelectrically actuated disconnect switch in the power branch and a microcontroller unit executing the tuned switching motion control schemes (upper). Measured closed-loop travel curves with different control strategies, compared with the travel curve under the open-loop control (lower)

lower actuation forces also necessitate smaller contacts and a low viscosity medium. Literature suggests that certain supercritical fluids (SCF) have the potential to satisfy all these requirements since they combine low viscosity, partial compressibility, and excellent dielectric and thermal characteristics [17]. Figure 12.12 shows the phase transition properties of supercritical CO_2 and a phase diagram of CO_2 at different temperatures [18]. In the preliminary breakdown experiment with SCF CO_2, uniform field electrodes were used, and the gap was set to 0.1 mm. The voltage between the electrodes was ramped up until breakdown occurred and repeated. The average breakdown voltage was 25 kV (DC), which under uniform electric field assumption results in a dielectric strength of 250 kV/mm [19]. This is approximately an order of magnitude higher than SF_6 gas at pressure levels typically used in switchgear applications. Such high dielectric strength of supercritical CO_2 enables the use of actuator technologies with limited displacement like the proposed piezoelectric actuator. In addition, CO_2 is very accessible and environmentally friendly and has nearly unlimited life expectancy under nonarcing conditions.

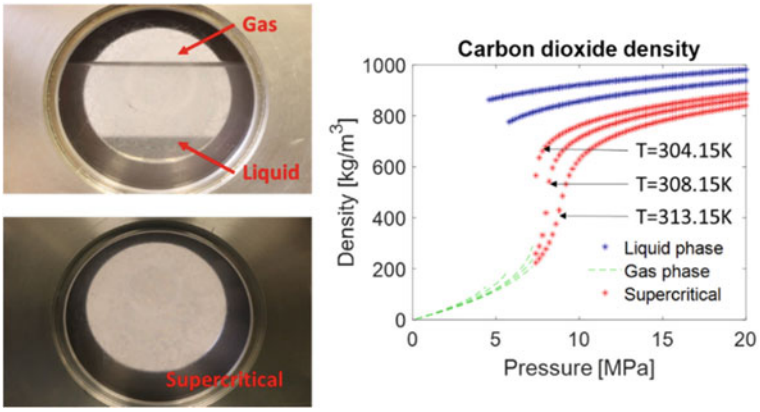

Fig. 12.12 Optical method confirming the phase of CO2 at different conditions, showing CO2 in subcritical (top left) and supercritical state (bottom left). Phase diagram of CO2 at different temperatures (right)

7 Concluding Remarks

Four new technologies have been proposed to improve current concepts of hybrid circuit breakers for DC applications: a new topology, a new control scheme, a new type of actuator in the mechanical switch, and a new switching medium. While each of them is interesting and applicable on their own, the greatest benefit is expected to be gained by the combination of all four due to synergistic effects. Such a hybrid circuit breaker could play an enabling role for the materialization of the widespread use of more reliable and resilient DC power applications in microgrids, shipboard power systems, wind collector systems, wildfire prevention, and arc flash mitigation, among others.

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Chapter 13
535 kV/25 kA Hybrid Circuit Breaker Development

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1 Introduction

This section will focus on the development of the 535 kV hybrid DC circuit breaker for the Zhangbei flexible DC transmission project [1, 2], the world's first HVDC grid, based on the 535 kV hybrid circuit breaker topology proposed by Tsinghua University [3]. This chapter will give the development process of the ultrafast mechanical switch (MS) [4], the modular-designed high-current bidirectional solid-state switch (SS) [5, 6], the current commutation driver circuit (CCDC) [7], and the isolation energy supply system [8]. Finally, 25 kA breaking experiment and reclosing experiment of the 535 kV circuit breaker are designed and carried out.

There are three main technical approaches to realize the fault isolation and protection of DC side based on protection equipment: (1) AC circuit breaker, (2) adopt converter with self-clearing capability of DC side fault, and (3) DC circuit breaker. Among them, the DC circuit breaker plays an important role in closing, carrying, and breaking the current under normal circuit conditions, converting the operating mode of the system, and breaking the fault current to protect the system. It is the preferred solution to realize the fault handling of the DC power grid.

According to the topology and breaking principle, DC circuit breakers can be divided into mechanical DC circuit breakers, solid-state DC circuit breakers, and hybrid DC circuit breakers. Among them, the mechanical DC circuit breaker has low conduction loss, but its breaking speed is relatively slow, and the breaking dispersion is high. The solid-state DC circuit breaker has an extremely fast breaking speed, but its on-state loss is large, and the cost is high. The hybrid DC circuit breaker combines the advantages of mechanical DC circuit breakers and solid-

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state DC circuit breakers and has the advantages of strong controllability and fast reclosing, which can meet the needs of flexible DC power grid fault protection, so it has become one of the main development directions of DC circuit breakers.

Reliable and fast current transfer is a prerequisite for the successful current interruption of hybrid DC circuit breakers. According to the principle of current transfer, the commutation modes of hybrid DC circuit breakers can be divided into natural commutation type, voltage zero-crossing type, and resistance zero-crossing type. The hybrid DC circuit breaker based on the natural commutation has the advantages of small on-state loss, fast breaking speed, etc. However, this commutation method is limited by the mechanical switching arc voltage. With the increase of the voltage level of the DC circuit breaker, the number of devices required in series in the power electronic switch branch increases, and the on-state voltage drop of the transfer branch increases. To ensure that the current is fully diverted to the power electronics branch, higher voltages will be required, placing higher demands on the switches and the power electronics branch. In the hybrid DC circuit breaker based on resistance zero-crossing, since the main power electronic switch conducts current for a short time and the conduction loss is very low, it is not necessary to install a cooling system. However, the auxiliary power electronic switch passes through the rated current for a long time, and the on-state loss is tens of kilowatts, which requires a water-cooled heat dissipation system, increasing the complexity and maintenance cost of the system. Tsinghua University proposed a voltage zero-crossing hybrid DC circuit breaker based on the coupled negative voltage circuit. The coupled negative voltage circuit can ensure the fast and reliable transfer of bidirectional current without increasing the on-state loss of the DC circuit breaker. The main circuit has only mechanical switches, no additional cooling device required. Compared with other methods, this topology has the advantages of simple structure, reliable commutation, and suitable for any voltage level (Fig. 13.1).

2 535 kV Coupling Negative Voltage Commutation Hybrid DC Circuit Breaker Overall Design

The hybrid DC circuit breaker is the same as most hybrid DC circuit breakers, with three branches: an ultrafast mechanical switch, a bidirectional solid-state switch module, and an energy-consuming MOV [9, 10]. The circuit breaker topology and breaking process are shown in Fig. 13.2. In addition, a current commutation driver circuit that can actively generate a pulse voltage is connected in series with modular solid-state switches to replace the load commutation switch on the mechanical switch branch. This allows the load current to flow only through the mechanical switch without other loss when the circuit breaker is normally operated [11]. When a short-circuit fault occurs, the mechanical switch starts to open, generating an arc. At the same time, the modular solid-state switches will be turned on, and CCDC

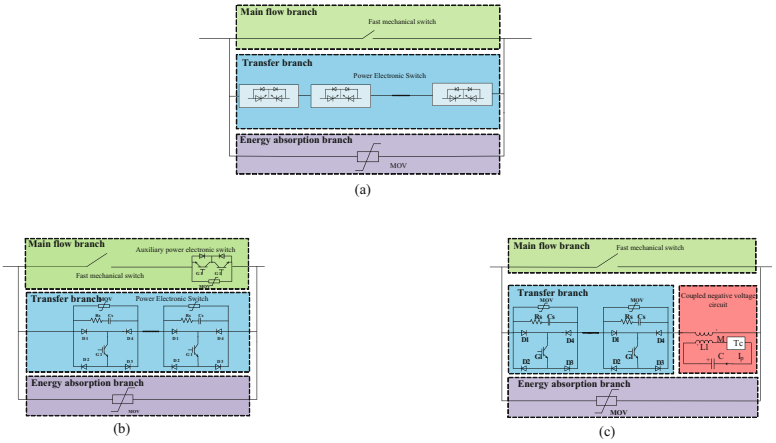

Fig. 13.1 Hybrid DC circuit breaker topology comparison. (**a**) Natural commutation hybrid DC circuit breaker topology. (**b**) Resistor zero-crossing hybrid DC circuit breaker topology. (**c**) Voltage zero-crossing hybrid DC circuit breaker based on coupled negative voltage

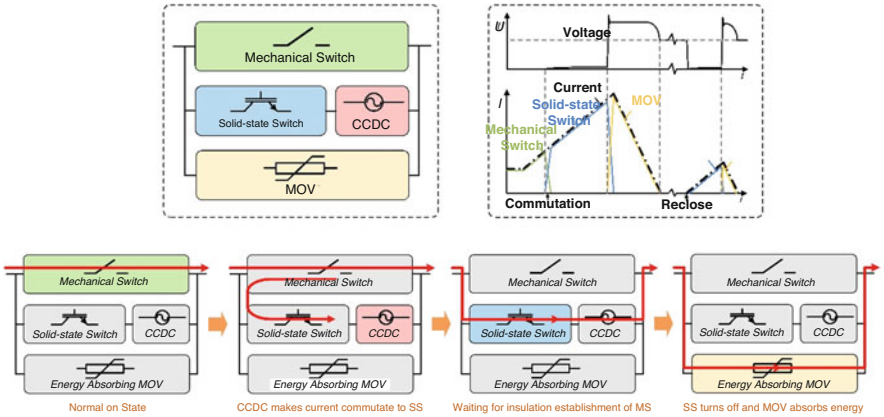

Fig. 13.2 The interruption process of the proposed HCB

generates a pulsed voltage and drives the fault current to commutate from the mechanical switch to the solid-state branch. The voltage generated by the CCDC is alternating. So, bidirectional commutation of the circuit breaker can be achieved. The arc in mechanical switch is extinguished when the current crosses zero, while solid-state switches continue to carry current until the mechanical switch contacts are pulled apart far enough to withstand the overvoltage. Finally, the solid-state switches are turned off, and the energy-consuming MOV will absorb the remaining energy [12, 13]. In addition, the reclosing function can be easily realized by using the solid-state switches. The CCDC can be regarded as a small inductance of 100 μH

Table 13.1 Main parameter requirements of 535 kV circuit breaker

Index	Parameters
Rated voltage	535 kV
Rated current	3300 A
Breaking capability	25 kA
MOV residual voltage	800 kV
Breaking speed	<3 ms

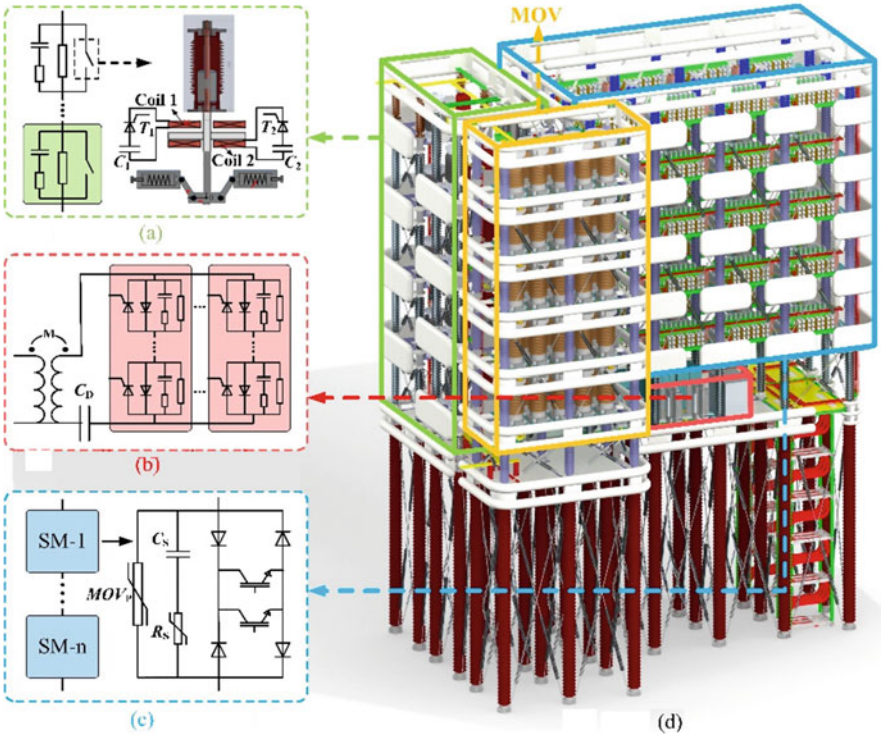

Fig. 13.3 Design of key components of coupling negative voltage hybrid DC circuit breaker. (**a**) Mechanical switch. (**b**) Coupling negative voltage device. (**c**) Solid-state switch. (**d**) Structure

when it does not work, which will have no significant impact on the solid-state switches.

According to the system requirements, the main parameters proposed for the DC circuit breaker are shown in Table 13.1. The following will introduce the design of the 535 kV hybrid DC circuit breaker in detail, as shown in Fig. 13.3, including design of mechanical switch for rapid breaking and restoration, modular-designed high-current bidirectional solid-state switch, and design of reliable CCDC.

3 Ultrafast Mechanical Switching of DC Circuit Breakers

The breaking time of the hybrid circuit breaker mainly depends on the speed of the mechanical switch. The solid-state switches can be turned off when the contact distance of the mechanical switch can withstand the overvoltage. Therefore, the moving contact must be separated to a certain distance as quickly as possible [14]. The bidirectional Thomson-coil actuator, which can accelerate and decelerate the moving parts, is developed to achieve this goal. As shown in Fig. 13.4, to achieve a better arc recovery effect, the ultrafast mechanical switch adopts a vacuum interrupter that the moving contact is connected to a metal disk placed between the two coils. In the closed state, the metal disc is close to the coil 1. When the precharged capacitor C_1 discharges through thyristor T_1 to coil 1, the metal disk, which is connected to the moving contact, will be forced to move away from coil 1. Then, after several milliseconds, the precharged capacitor C_2 discharges through thyristor T_2 to coil 2 to decelerate the metal disk and avoid the heavy bounce when the moving parts reach the other side. In addition, the switch also uses a bistable spring mechanism as a holding unit, so that the moving and static contacts can be closely contacted to ensure a sufficiently small contact resistance during normal flow.

Typical moving curves for ultrafast mechanical switch opening are given in Fig. 13.5. It can be seen that the electromagnetic repulsion mechanism can pull the switch contacts apart by a distance of 15 mm within 3 ms, which can withstand 160 kV operating overvoltage. Under the buffer action of coil 2, the speed of the moving parts is reduced to fewer than 1 m/s to protect the mechanical structure.

The overall mechanical switch branch consists of eight ultrafast mechanical switches connected in series. Figure 13.6 shows the comparison of the moving curves of eight ultrafast mechanical switches. Within the initial movement of about 15 mm, the switches are relatively consistent. But when the coil 2 starts to buffer, the movement of switches is different obviously because of the mechanical properties of the switches. During the breaking process of the circuit breaker, only the action characteristics of the mechanical switch in the first 3 ms are concerned. The total

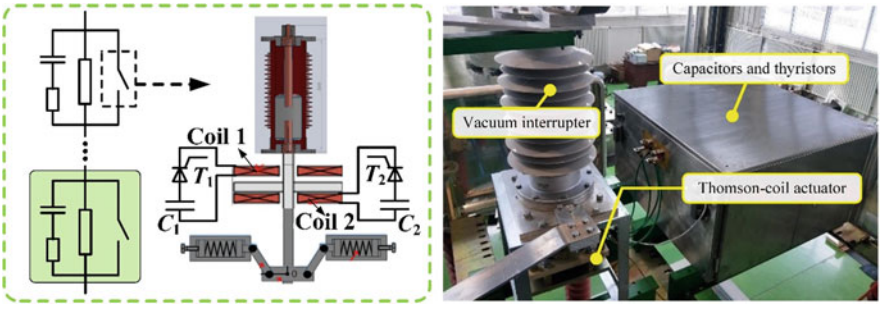

Fig. 13.4 Principle and physical map of fast mechanical switch

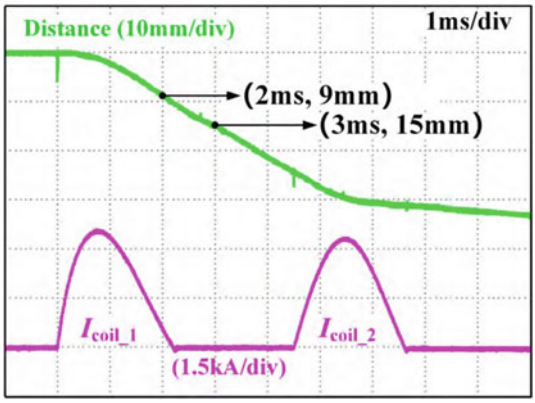

Fig. 13.5 Typical switch travel curve

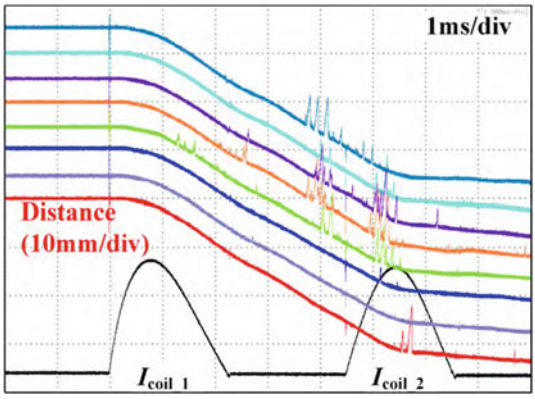

Fig. 13.6 Comparison of eight switch moving curves

opening distance of eight mechanical switches can reach more than 96 mm in 2 ms, which is enough to withstand the 800 kV overvoltage. In addition, in order to avoid uneven voltage between switches, each switch is also connected in parallel with a static voltage equalization resistor (300 MΩ) and a dynamic voltage equalization *RC* circuit (300 Ω, 5 nF).

4 Design and Development of 535 kV/25 kA Solid-State Switches

The modular-designed high-current bidirectional solid-state switch is the core component of the hybrid DC circuit breaker. It not only needs to have a surge capacity to withstand millisecond-level fault currents but also a cutoff capability of up to 25 kA. In addition, as part of the 500 kV HCB, it must withstand the rated voltage and transient overvoltage. To ensure the reliability of the solid-state branch, this project requires at least two parallel full-control devices in a solid-state switch

module. In this way, the two parallel devices are bypass switches for each other to avoid the failure of current commutation caused by the refusal of a single device (such as driving optical fiber, poor lead contact, etc.).

4.1 Selection of Power Electronic Devices

In the application of hybrid high-voltage DC circuit breakers, IGBT-type devices with strong current shutoff capability usually are used as full-control devices for solid-state switches [15]. Considering the device characteristics, prices, and application reliability, Toshiba's 4.5 kV/3 kA IEGT (ST3000GXH24A) was finally selected [16]. IEGT is a kind of IGBT that uses an enhanced injection structure with a low on-state voltage, making it ideal for use in DC circuit breakers that require high-current capability. The effect of the enhanced injection structure makes the internal current distribution closer to the IGCT when the device is turned on. So the desaturation current of IEGT will be greatly improved after the gate voltage is increased. Figure 13.7 shows the result of the turnoff capability test of IEGT. In Fig. 13.7a, it can be seen that the device has obvious desaturation at about 10.4 kA with

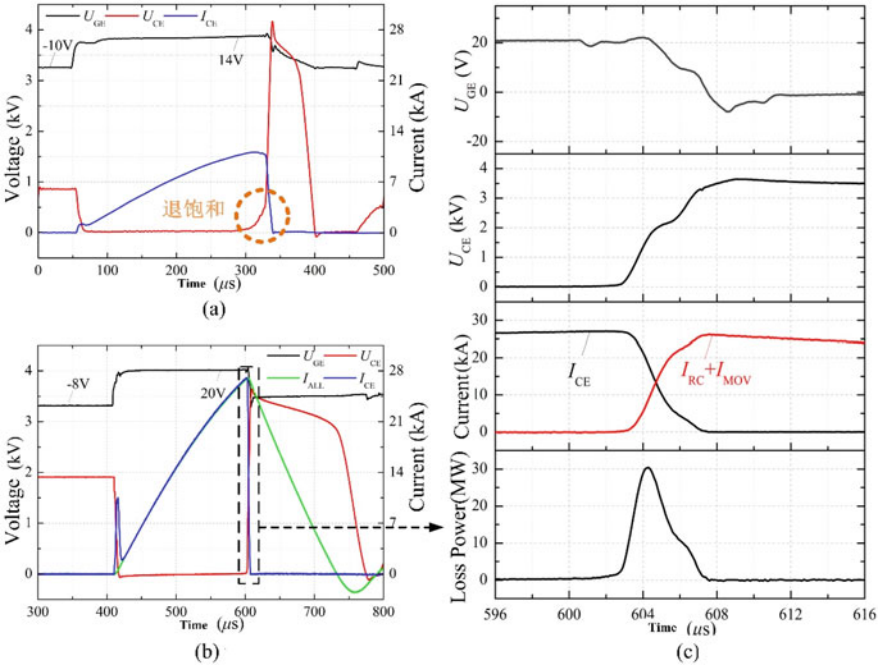

Fig. 13.7 IEGT turnoff performance test. (**a**) Desaturation of IEGT at 10.4 kA. (**b**) The waveform of breaking 27 kA current. (**c**) The detail of breaking 27 kA current

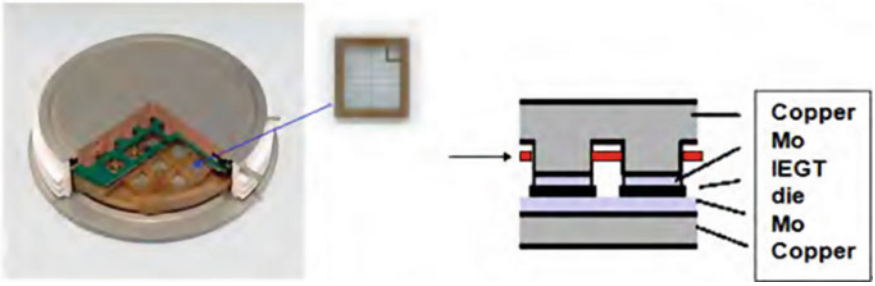

Fig. 13.8 IEGT in press-fit package

14 V gate voltage. Because it is turned off after a short time, IEGT is not damaged when breaking 10.4 kA current. When the gate voltage is increased to 20 V (Fig. 13.7b), the current reaches 27 kA without desaturation, and it is successfully turned off. As is shown in Fig. 13.7c, the transient power loss that the IEGT can withstand when turned off can reach 30 MW, which is enough to meet the requirement of Zhangbei Project for the turnoff capability of IEGT.

Because IEGT is a double-sided crimp construction (Fig. 13.8), there is no bonding line inside. In this configuration, the silicon chip is sandwiched between the molybdenum material and the copper for the outer packaging. When a short-circuit fault occurs, the metal alloy material formed after melting can ensure long-term reliable flow, which is called long-term failure short-circuit mode. In this way, when IEGT in the module fails, it can maintain a short-circuit state by itself and have no influence on other modules, improving the reliability of equipment.

Because of the optimization of the diode bridge structure, a standard recovery diode with low cost and strong surge capability can be used to form a bidirectional structure. The diode was selected as Infineon D1800N48T (4800 V 1800 A). Because the conduction voltage drop of standard recovery diode is very low, the surge capability in 3 ms of this diode can exceed than 35 kA.

4.2 Structural Design and Optimization

The module structure needs to be as compact as possible to reduce the impact of stray inductance on the commutation process, as shown in Fig. 13.9. First, to achieve consistency of parallel IEGT in a module, two IEGTs are symmetrically pressed, and the cathodes of them share the same heat sink. Then four diodes are individually press-fitted in another valve section to avoid the mutual influence with IEGT valve. Besides, snubber circuit and MOV are symmetrically placed on the outside of the diode bridge to realize the bidirectional current flow. All connecting copper bars need to be placed as close as possible to reduce the effect of stray inductance on the breaking process.

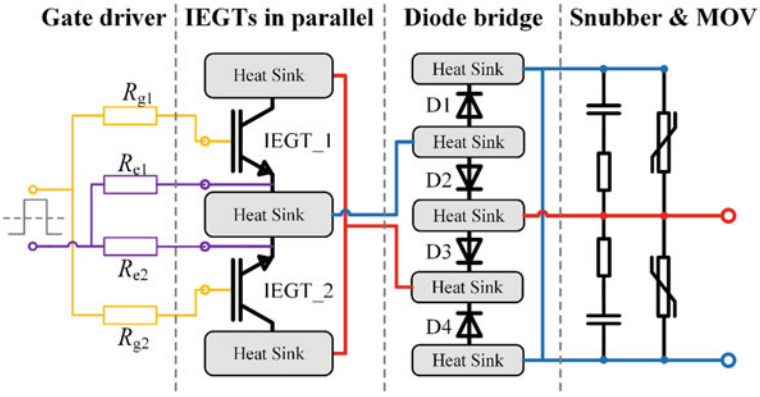

Fig. 13.9 Schematic diagram of the parallel structure of power electronic multilevel direct-series switches

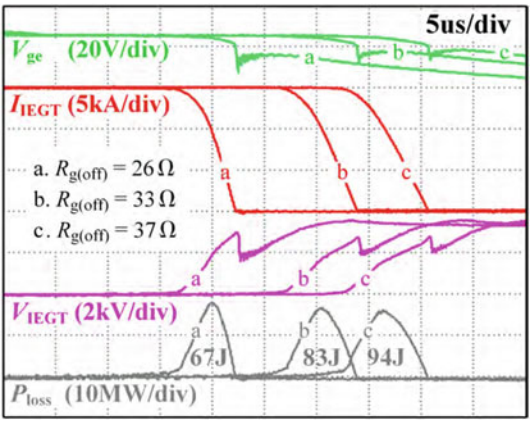

Fig. 13.10 Gate resistor adjustment

The gates of the parallel IEGTs are connected to the output port of the driver through two independent gate resistors ($R_{g1} = R_{g2} = 33\ \Omega$) which are the same in resistance. Two cathode resistors are also added to suppress the circulating current caused by the asymmetry of the driver connection line ($R_{e1} = R_{e2} = 1\ \Omega$). The gate resistance affects the turnoff speed of IEGT. Generally speaking, if the turnoff speed is too high, the overvoltage will cause the breakdown of the device. However, if the turnoff speed is too slow, it will increase loss and cause the device to overheat. Overvoltage in the switch will be limited by the MOV. So turnoff losses and turnoff peak power are major problem. As shown in Fig. 13.10, the turnoff process of different gate resistors is tested under the same current. It can be seen that as the gate resistance increases, the turnoff power decreases, but the loss increases. A relatively moderate value (33 Ω) was finally chosen based on the maximum instantaneous power provided by the equipment manufacturer and the temperature threshold in actual operation.

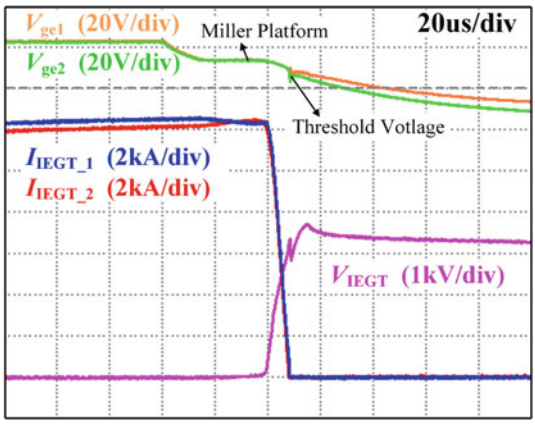

Fig. 13.11 25 kA Test of parallel IEGTs

The results of 25 kA test are shown in Fig. 13.11. Although the structure has been as symmetrical as possible, the current is still unbalanced slightly between the two IEGTs at on-state. However, since independent resistors are used to connect to gate and cathode to suppress the circulating current, the turnoff process of two IEGTs is very synchronous, which improves the turnoff reliability.

4.3 Design of the Overall Modular-Designed Solid-State Switches

After completing the design of a single solid-state switch, it is necessary to further connect the modules in series to form overall power electronic multilevel series switches. According to the engineering technical specification, the series modular-designed solid-state switches need to withstand the DC voltage which are 1.1 times higher than the rated DC voltage (535 kV) and the impulse voltage which are 1.38 times higher than the overvoltage (800 kV), considering 8% of the series modules is breakdown. Because the parallel MOV is designed to be discrete, there is no need to calculate the unbalance factor between solid-state switches. The total voltage level is calculated by the series module. The rated voltage and maximum overvoltage of a modular solid-state switch are determined by the reference voltage $U_{\text{ref}} = 2.4$ kV and residual voltage $U_{\text{res}} = 4$ kV of the MOV connected in parallel. The final number of series modules is 320. The margins for DC and impulse voltages are 23% and 14%, respectively, which can meet the design requirement.

Because the energy of the 535 kV flexible DC system is very large, the circuit breaker requires the MOV to absorb energy more than 100 MJ. If only the discrete MOV design is adopted, each MOV needs to absorb energy more than 300 kJ, which will increase not only the volume of every module but also the cost of package of MOV. Additionally, the series redundancy of modular solid-state switches can create the overvoltage which exceeds 800 kV when all switches are working normally, potentially stressing other equipment.

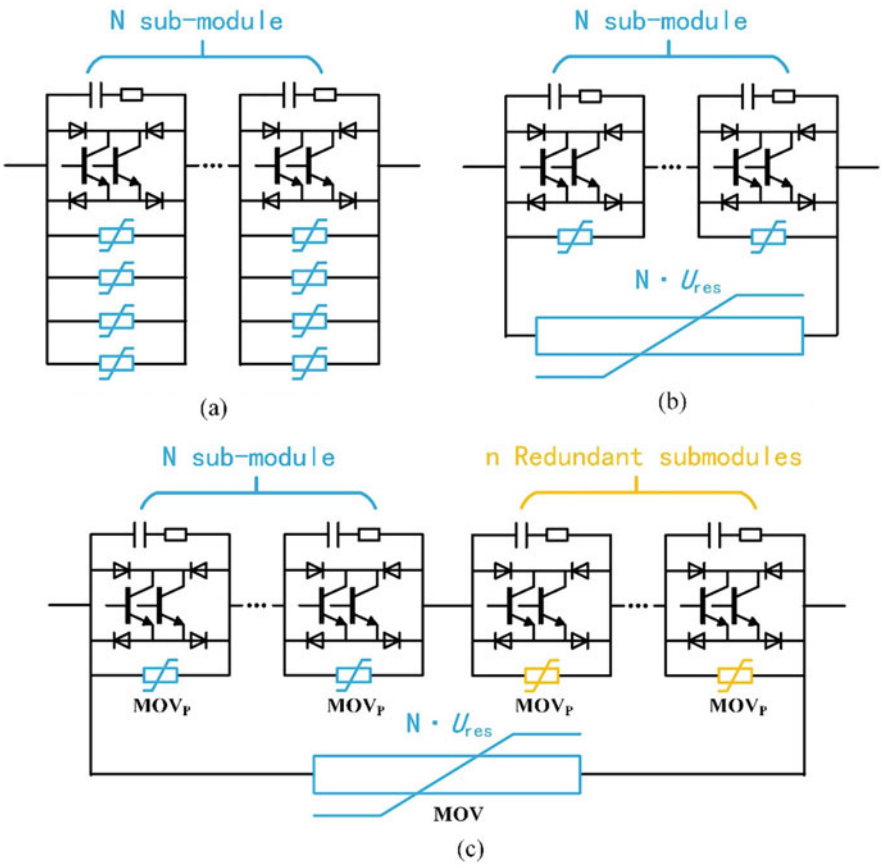

Fig. 13.12 MOV hierarchical design. (**a**) Original discrete MOV design. (**b**) Partial MOV integration. (**c**) Redundant modules added to maintain out-of-voltage characteristics

So, MOV is designed in layers, as shown in Fig. 13.12b, c. Original N sub-modules meet the overvoltage requirements. Then a lumped MOV is parallel to the series modular-designed solid-state switch valve to replace most of the MOV_s in the sub-modules, which not only meets the series voltage equalization requirements but also reduces the number of parallel MOVs in each module. To meet the voltage level and increase reliability, add the redundant modules as shown in Fig. 13.12c. The redundant modules are connected in series with the original N modules. Through hierarchical design, the functions of voltage-limiting protection and energy absorption of the original MOV are separated. In order to distinguish these two kinds of MOVs, the MOVs connected in parallel in the module are called protection MOV_p, and the MOVs connected in parallel with the overall solid-state switch valve are called energy absorption MOVs.

4.4 Experimental Verification

Eight modular-designed solid-state switch modules are integrated into a valve section, as shown in Fig. 13.13. Each module is only equipped with an MOV_p to limit overvoltage. Then the valve section is arranged as a valve tower. Each valve section will undergo a 25 kA shutoff test for component integrity after press-fitting, with typical waveforms shown in Fig. 13.14. It can be seen that the valve section is successfully turned off by 25 kA. Although there are some inconsistencies in the establishment of voltage of each module, they are all limited by their respective MOV_p after reaching the highest voltage.

To verify the effectiveness of the hierarchical design of MOV, a group of energy-absorbing MOV_s with a residual voltage of 160 kV were connected in parallel to 64 modules. A 25 kA turnoff test was performed on them. The result is shown in Fig. 13.15. After the IEGT is turned off, the current first strikes the MOV_p. Then the current is quickly transferred to the energy-absorbing MOV. The speed of the current transfer depends on the stray inductance of the circuit. During the entire breaking process, the overvoltage has been below 160 kV. Although the overall energy is not high due to the experimental conditions, it can be seen that the energy-absorbing MOV will absorb most of the energy, while MOV_p will only absorb the energy in the stray inductance on the branch of the solid-state switch.

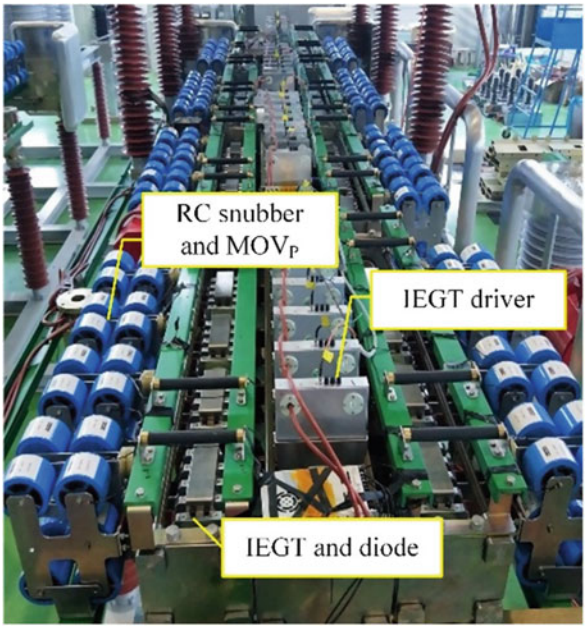

Fig. 13.13 Actual diagram of solid-state switch valve section

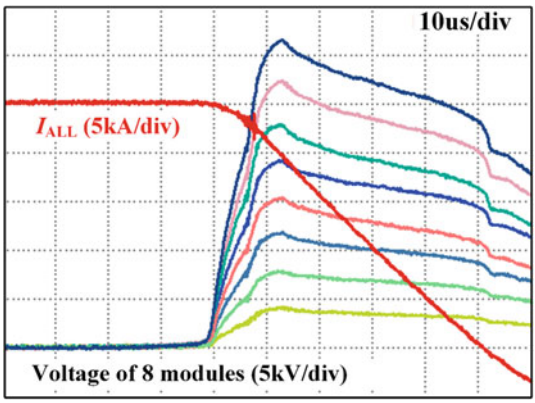

Fig. 13.14 Eight-series modules shut down 25 kA test

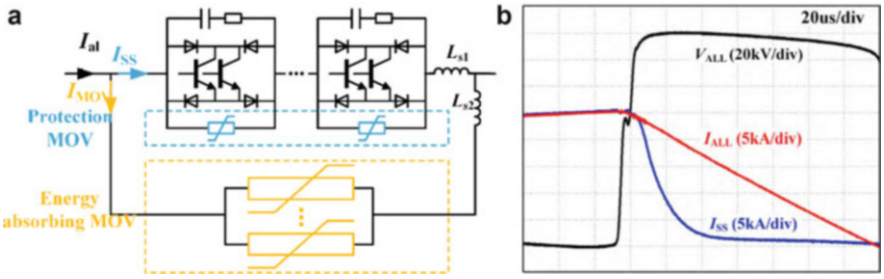

Fig. 13.15 (**a**) Test circuit and (**b**) waveform result

5 Design and Development of Current Commutation Device Circuit

The CCDC is used to commutate the current from the mechanical switch branch to the solid-state switch branch, which is the core equipment for the HCB to transition from the steady state to the transient state. It is the core equipment for transitioning the hybrid circuit breaker from steady state to dynamic. As depicted in Fig. 13.16, the CCDC consists of a transformer, a precharged capacitor C_D, and a pulse-closing switch based on thyristors. When the thyristors are turned on, the C_D will discharge through the transformer's winding, thereby inducing a corresponding voltage on the winding of the other side. At this time, the MS is in the arcing state after the contact is separated, and the SS is in the on-state. Therefore, the CCDC can generate an oscillating circulating current between the MS and the SS to realize the transfer of current. It should be noted that both the CCDC and other components of the HCB, including the mechanical switch branch and the solid-state switch modules, need a high-voltage isolated power supply to work.

The C_d is continuously charged by a controllable power supply to keep its voltage at the required level, and the precharge is only used for a one-shot operation. When a fault occurs, the CCDC only operates once in the first breaking action of the HCB to

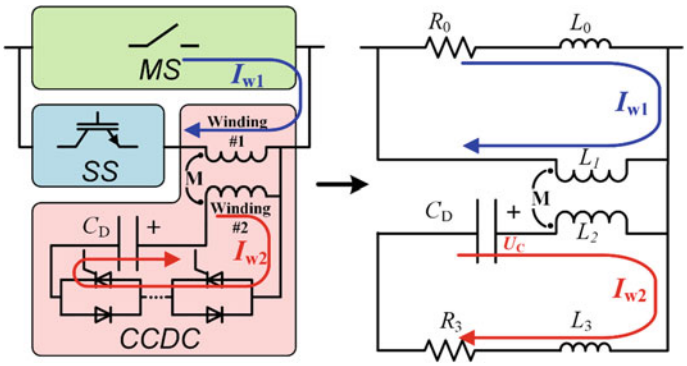

Fig. 13.16 Commutation principle of coupling negative voltage device

commutate the current from the mechanical switch branch to the solid-state switch branch. In the subsequent reclosure operation of the HCB, whether or not there is a fault, the commutation function of the CCDC is no longer needed. After the HCB completed the breaking and reclosing action, it will lock for a period of time, during which the energy storage capacitor of the CCDC will be recharged and the cooling time of the MOV will also be given.

The research team from Tsinghua University has carried out a detailed study on the parameter optimization method of the CCDC. The parameters of coupling negative voltage of the 535 kV DC circuit breaker needs to match the commutation current of 25 kA and the circuit parameters of the DC circuit breaker. As shown in Fig. 13.16, the air core transformer can be equivalent to L_1, L_2, and mutual inductance M. The arc voltage of MS is relatively low and can be ignored. Therefore, the commutation circuit composed of MS and SS can be simplified as RL circuit (R_0 and L_0). Likewise, the RL circuit on the CCDC's side can also be equivalent to R_3 and L_3. Therefore, the circuit equation during commutation is:

$$\begin{cases} (L_0 + L_1)\frac{di_{\omega 1}}{dt} - M\frac{di_{\omega 2}}{dt} + R_0 i_{\omega 1} = 0 \\ (L_2 + L_3)\frac{di_{\omega 2}}{dt} - M\frac{di_{\omega 1}}{dt} + R_3 i_{\omega 2} = u_C \\ i_{\omega 2} = -C_D\frac{du_C}{dt} \end{cases} \tag{13.1}$$

Therefore, the expression of the commutation current component i_{w1} in the MS and the SS can be written as:

$$i_{w1}(t) = A \cdot e^{-\sigma_1 t} + B \cdot e^{-\sigma_2 t} \sin(\omega t + \varphi) \tag{13.2}$$

Next, it is necessary to obtain R_0, L_0, R_3, and L_3 as accurate as possible through experiments or simulations. Among them, the stray inductance L_0 of the MS of the circuit breaker and the SS has the greatest impact on the results. At the same time, because the inductance is related to the structure, it can only be obtained through

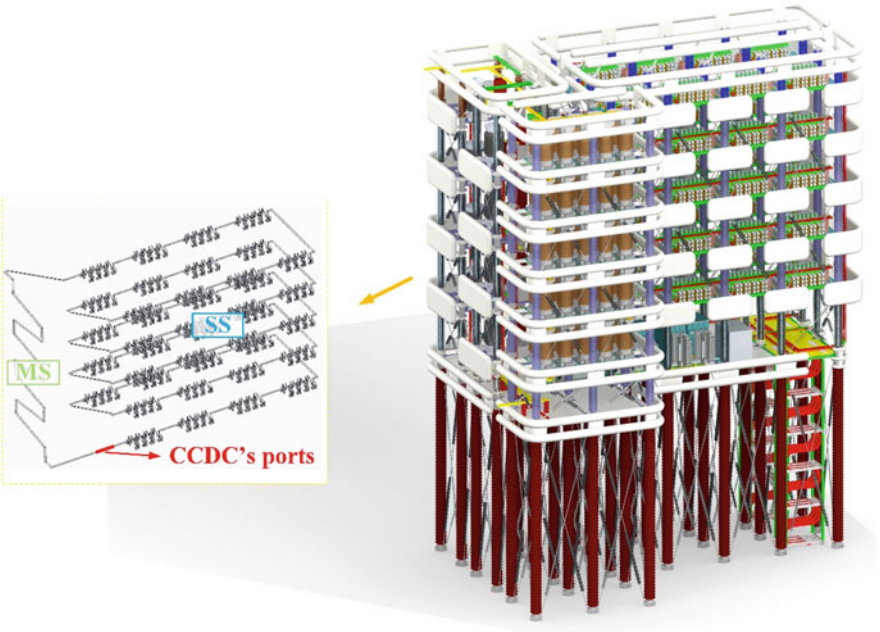

Fig. 13.17 Simulation of stray inductance of circuit breaker structure

structural simulation before the assembling of the circuit breaker. As shown in Fig. 13.17, the current path of the MS and the SS is modeled, and the simulation result of the structural stray inductance is $L_0 = 247\ \mu\text{H}$.

The positive and negative peaks of i_{w1} need to reach 25 kA, then a series of solutions can be obtained by solving Eqs. (13.1) and (13.2). At this time, given a set of values of C_D and L_1, the current capability i_{w2} and precharging voltage U_C required by the corresponding CCDC can be obtained. This gives the cost of CCDC. Among them, the cost of the capacitor is linearly related to its energy, the cost of the thyristor is related to the number of series and parallel connection, and the cost of the charging device is linearly related to the voltage:

$$\begin{cases} \text{Cost of Capacity} = K_1 \cdot C_D U_C^2 \\ \text{Cost} = K_2 \cdot \text{ceil}\left(\frac{U_C}{U_T}\right) \cdot \text{ceil}\left(\frac{I_{W2}}{I_T}\right) \\ \text{Cost of Precharge Device} = K_3 \cdot U_C \end{cases}$$

Finally, the total cost is optimized: the energy storage capacitor $C_D = 650\ \mu\text{F}$, and transformer parameters $L_1 = 257.5\ \mu\text{H}$, $L_2 = 44.3\ \mu\text{H}$, and $M = 104.9\ \mu\text{H}$ are finally determined.

Figure 13.18 shows the real CCDC and the equivalent load test waveform. The coupling transformer adopts an ironless air core to avoid saturation at high

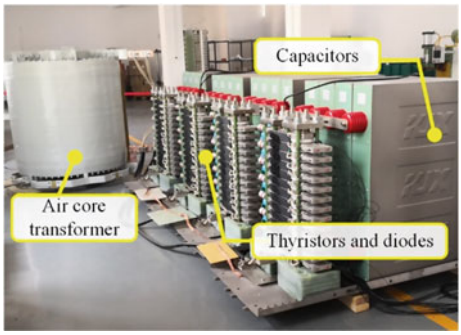

Fig. 13.18 Real product of CCDC

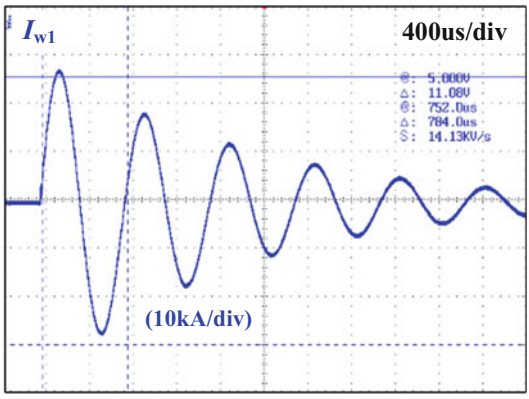

Fig. 13.19 Equivalent load test waveform

current. Capacitor and thyristor switches are divided into four parallel modules for high-current capability. Because the current generated by the CCDC needs to cooperate with the actual MS and the SS, the equivalent impedance is used for the commutation test at that time. Test results show that the CCDC can generate the required positive and negative current peaks (>25 kA) within 0.6 ms (Fig. 13.19).

6 Integration of DC Circuit Breaker and Multipotential High-Voltage Isolation Power Supply System

Figure 13.20 shows the connection diagram of the 535 kV DC circuit breaker. First, 8 MSs are connected in series (the voltage-equalizing circuit is omitted in the figure) to form the current-conducting branch of the DC circuit breaker. The SS is divided into five layers, each layer of the SS includes 64 sub-modules, and the energy-absorbing MOV is also divided into five layers in parallel with the corresponding layer of the SS. The layered design is mainly considered from the structural insulation. Because the number of redundant modules is large, if the damaged locations of the modules are concentrated in the same area, the original

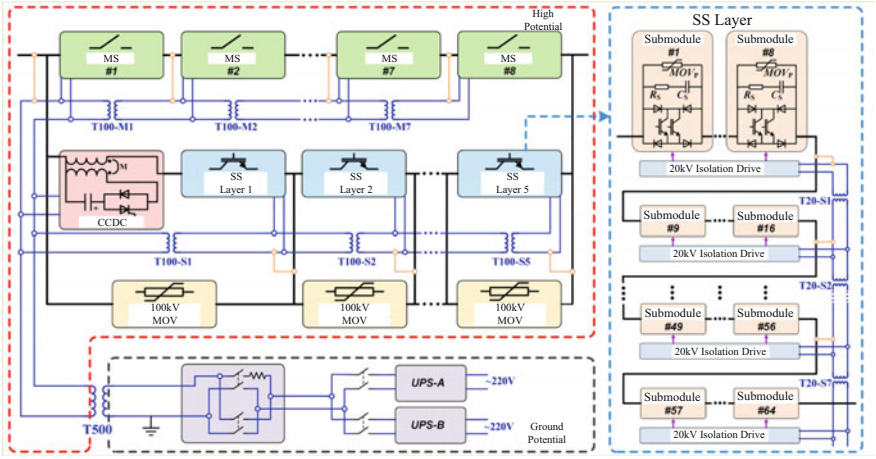

Fig. 13.20 535 kV DC circuit breaker connection diagram

potential distribution of the circuit breaker will be greatly changed, increasing the difficulty of the corresponding insulation design. After the layered design is adopted, the maximum insulation level between the layers is given. The SS part is firstly designed by standard of the 100 kV rating and then stacked to become a 535 kV SS. It should be pointed out that after layering, the redundant modules of each layer are no longer shared. So when the loss of any layer of modules exceeds the design value, the entire breaker needs to be shut down. The CCDC is special. It is connected in series with the first layer of SS and then in parallel with the first layer of energy-absorbing MOVs. Because the CCDC can be placed at any position of the MS and the SS circuit, it will not affect the commutation. In addition, when the SS is turned off, the CCDC is only equivalent to an inductance of the order of 100 μH, which will not bring additional effects.

In general, the integrated design idea for 535 kV DC circuit breaker is to connect low-voltage-level devices in series. After using the modular series technology, the increase of the voltage level of the circuit breaker will not cause other technical problems. But there is another problem that will gradually become prominent as the voltage increases, that is, the problem of high-voltage isolated power supply.

In fact, the operating conditions of DC circuit breaker are very special for high-voltage power electronic equipment, which bring great difficulties to the power supply system. As shown in Fig. 13.21, the power electronic modules in the converter will withstand a certain voltage during operation, so the device can directly obtain energy from the potential difference by the DC-DC power supply. Or in some other applications where it is difficult to find a stable potential difference, the energy can be acquired from the line by electromagnetic induction through the alternating current in the device. In contrast, DC circuit breakers can be regards as a small resistance in the normal state. The voltage of power electronic devices is almost 0V. At the same time, energy cannot be obtained from the current in the

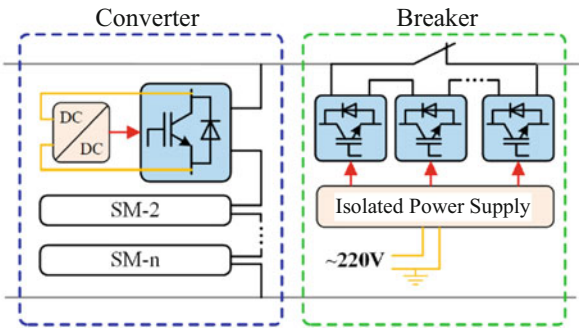

Fig. 13.21 Comparison of power supply mode between converter and DC circuit breaker

DC line. So, the DC circuit breaker can only obtain the energy from the external distribution network and then supplies for the electrical equipment through the isolated power supply system.

The 535 kV circuit breaker contains a large number of electrical equipment; each SS module, each MS, and the CCDC need to be powered; and these devices are not on the same potential, which brings huge difficulties to the isolated power supply. Hence, a multipotential high-voltage isolation power supply system needs to be specially designed for the 535 kV DC circuit breaker. The main structure of the isolated power supply system has been given in Fig. 13.20.

Firstly, the components of the DC circuit breaker are actually at the same high potential when it is in the closing state. However, the DCCB needs to withstand the transient overvoltage and the bus voltage during the transient breaking process; thus, the potentials of the series modules are inconsistent. So a 535 kV isolation transformer (T500) is used to take 220 V alternating voltage from the ground to the high potential and provides a power supply port for the DC circuit breaker at the same potential as the high-voltage line.

Secondly, the 100 kV isolation transformer (T100) is used in cascade form to provide power supply ports with different potentials for five layers of SS and 8 MS. It should be noted that the isolation transformers (T100-M1 to T100-M7) for the 7 MS and the isolation transformers (T100-S1 to T100-S5) for the 5 SS both withstand 535 kV terminal voltage of DC circuit breaker. Because the SS adopts a layered design, the isolation transformers can be directly connected to each layer of 100 kV MOV in an equipotential connection after they are cascaded, and there is no need to consider the problem of voltage equalization. However, there is no MOV in parallel with the MS but the static balancing resistor and the dynamic balancing RC circuit in parallel with the MS, so the isolation level needs to be relatively high. In order to unify the specifications in the project, the same 100 kV isolation transformer is adopted here. In addition, the same idea is used inside the SS, and the 20 kV isolation transformers are used for the cascaded power supply (T20-S1 $\sim$ T2-S5) for the valve section (includes eight modules). Figure 13.22 shows the physical map of 535 kV, 100 kV, and 20 kV isolation transformers, and the specific parameters are given in Table 13.2.

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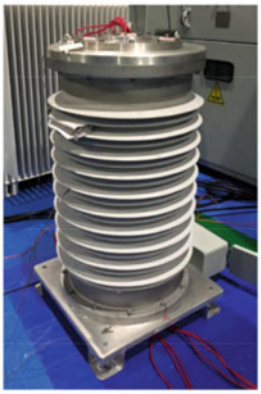

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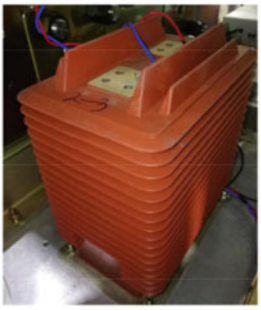

(c)

Fig. 13.22 Physical drawing of isolation transformer. (**a**) 500 kV isolated transformer. (**b**) 100 kV isolated transformer. (**c**) 20 kV isolated transformer

Table 13.2 Parameters of isolation transformers

Parameter	500 kV isolated Transformer T500	100 kV isolated Transformer T100	20 kV isolated Transformer T20
Operating range	190 to 250 V AC, 45 to 65 Hz		
DC withstand voltage	588 kV	110 kV	20 kV
Short-time DC withstand voltage (1 min)	856 kV	179 kV	35 kV
Peak of switching impulse withstand voltage	1292 kV	193 kV	45 kV
Peak of lightning impulse withstand voltage	1425 kV	233 kV	50 kV

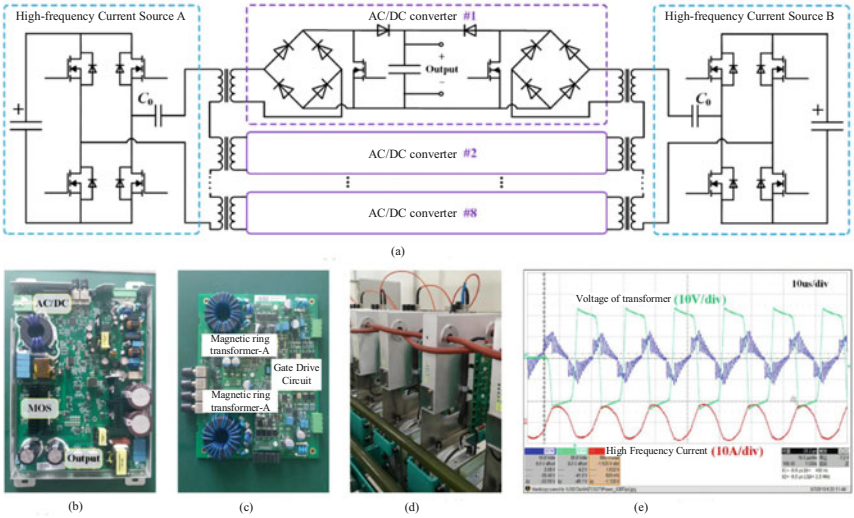

Fig. 13.23 Double-redundancy high-frequency isolation energy supply method based on magnetic ring. (**a**) Principle of dual redundancy high-frequency isolation power supply unit. (**b**) High-frequency current source. (**c**) Energy acquisition module. (**d**) Insulated cables. (**e**) Typical waveform

So far, 220 V AC power can be supplied to each valve section, and a high-frequency isolation power supply unit based on magnetic ring is used inside the valve section, which can directly provide isolated power for eight modules. First, a high-frequency current source is used to generate a resonant current of about 60 kHz, and then an insulated cable is used to make the current pass through the magnetic ring transformer of the drive board in each module, and the corresponding AC voltage is induced on the secondary side of the transformer. After rectification and stabilization, it can be used for IEGT gate driver. As shown in Fig. 13.23, both the high-frequency current source and the magnetic ring energy acquisition module adopt double redundancy, which can ensure continuous working when any part fails.

7 Experimental Research of the Whole DC Circuit Breaker

Figure 13.24 shows the experimental circuit and control sequence of the interruption platform for the 535 kV DC circuit breaker. In order to test the reclosing function of the DC circuit breaker, the experimental platform is equipped with two independent discharge capacitors. Among them, C_{DC1} is used to generate a fault current of 25 kA, and C_{DC2} with a smaller capacitance is used to simulate the situation that the system fault is not cleared during reclosing.

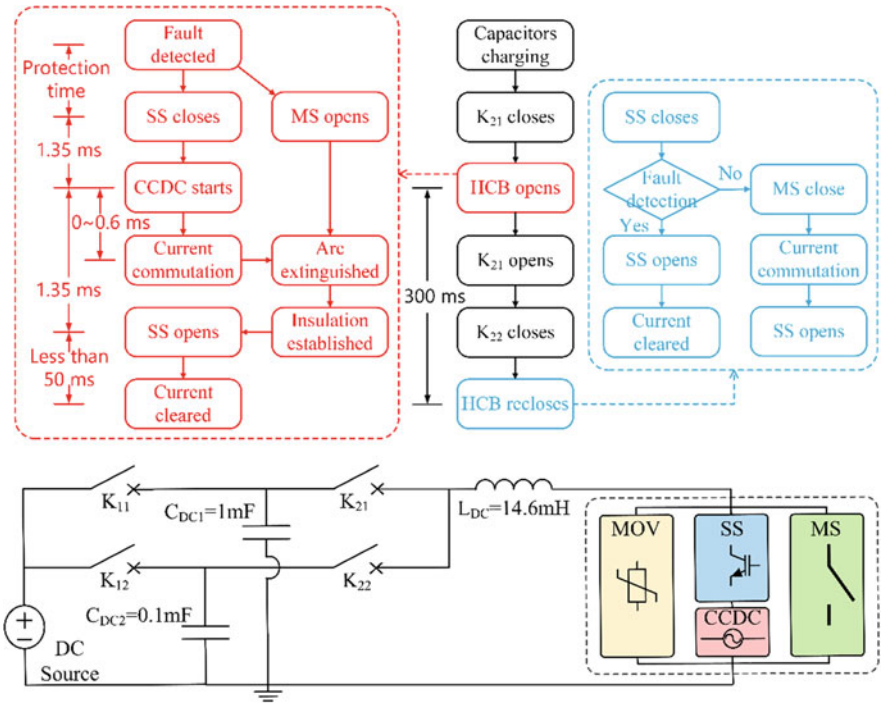

Fig. 13.24 Schematic diagram of experimental circuit and control flow of DC circuit breaker

The overall experimental process is as follows: the DC circuit breaker is initially in the closed state, and the two groups of capacitors are charged separately under the control of K_{11} and K_{12}. At the beginning of the experiment, K_{21} is closed, and C_{DC1} discharges the inductor L_{DC}. When the protection device detects the fault current, it sends a breaking command to the DC circuit breaker. The DC circuit breaker will trigger the MS, the SS, and the CCDC successively through the preset action sequence and finally clear the fault. After the current is completely removed, the circuit breaker is in the blocking state. At this time, K_{21} is opened, and K_{22} is then closed. After that, the controller will send a reclosing command to the DC circuit breaker. The circuit breaker will first turn off the SS and observe the current rise to determine whether there is a fault. If the current is not too large, the MS will be closed. Because the voltage drop of the MS is lower than that of the SS, the current will be automatically commutated to the MS, and the SS will resume blocking state after a period of time. Otherwise, if the current is too large, the SS will directly turn off and clear the fault. Figures 13.25 and 13.26 shows the practical photograph of the experimental platform and DC circuit breaker.

Before the final breaking experiment, a 25 kA current turnoff experiment test was performed on the integrated SS to verify the reliability of the centralized operation of 320-series modules. The test results are shown in Fig. 13.27. The results show

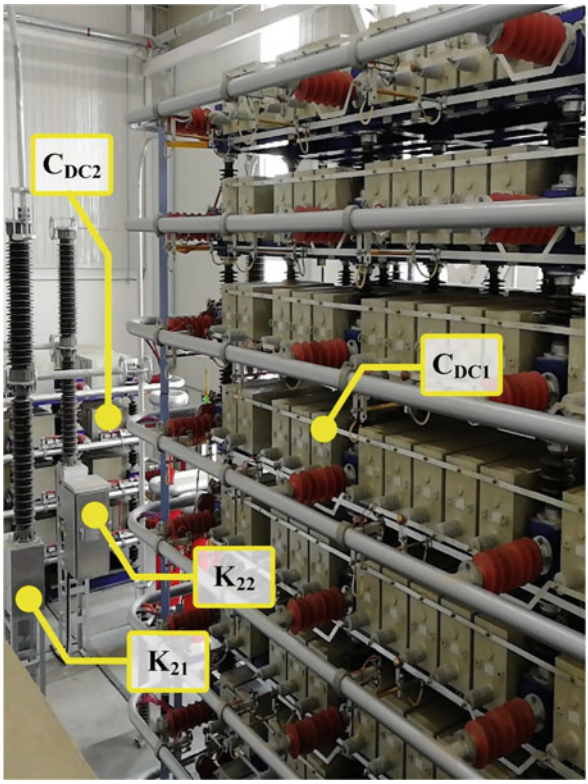

Fig. 13.25 High-current experimental platform

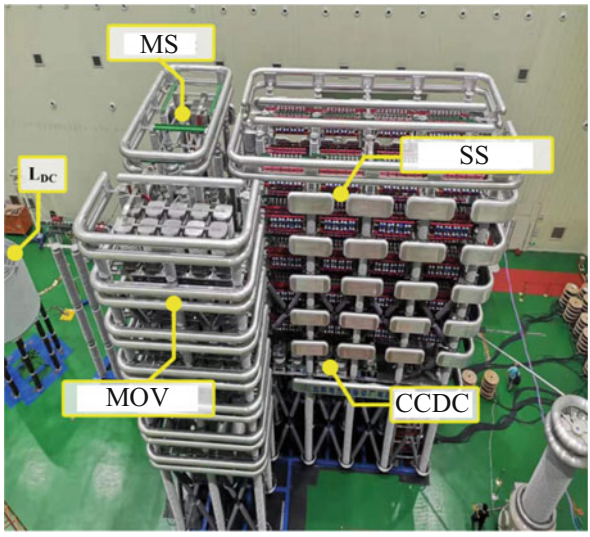

Fig. 13.26 Practical photograph of circuit breaker

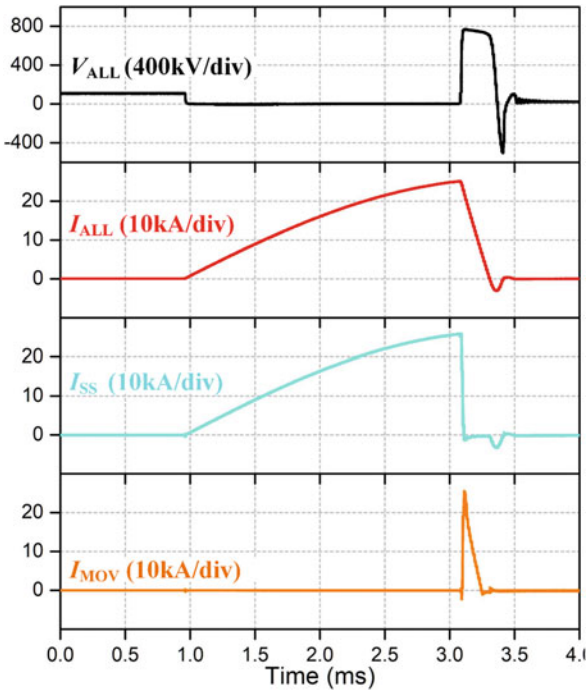

Fig. 13.27 25 kA turnoff test of the integrated SS

that the integrated SS can successfully turn off the current of 25 kA, and the energy absorption MOV limits the overvoltage to less than 800 kV at 25 kA. Because the terminal has withstood an operating impulse voltage of 800 kV, the experiment also examines the insulation between the terminals of the mechanical structure and the stability of the isolated power supply system.

Since only the estimated equivalent load is used to verify the commutation capability of the CCDC in Sect. 3, it is necessary to retest the CCDC in actual MS and SS. The thyristor in the CCDC is triggered when both the MS and the SS are in a conducting state. The actual measured current in the SS and the thyristor is shown in Fig. 13.28. The CCDC successfully generated an oscillating current of 25 kA between the MS and the SS. The first oscillation period is 0.8 ms, indicating that the calculation of stray inductance is roughly accurate. However, because of the existence of the voltage drop of the device in the SS, the equivalent resistance of the SS is larger when the current is smaller, so the amplitudes of current in the subsequent oscillation periods are different from those used equivalent load previously. At 3.8 ms, because the voltage generated by the CCDC is no longer enough to cover the turn-on voltage drop of all devices, the current in the SS completely stops oscillating. But in fact, only the first two peaks of current affect the commutation capability of the CCDC, so it is only required to pay attention to whether the peaks at 0.2 ms and 0.6 ms can reach 25 kA.

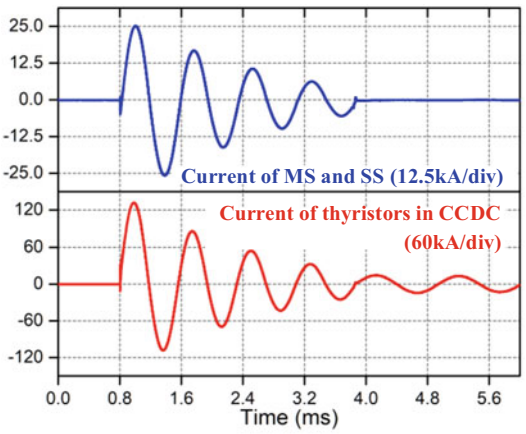

Fig. 13.28 Test of practical load commutation capacity of CCDC

After verifying that all components have reached the expected performance, the current breaking and reclosing test of the circuit breaker was carried out as shown in Fig. 13.29. Because of the asymmetry of current of CCDC, both forward and reverse current tests are required. The results are shown in Fig. 13.29, respectively. The experimental platform needs to charge C_{DC1} to 115 kV to generate 25 kA and then discharge the circuit through K_{21}. It can be seen that after the DC circuit breaker receives the breaking command, the MS starts to open first, but the current of the MS continues to rise because the vacuum arc voltage is very low. After 1.35 ms, the CCDC is triggered and causes an oscillating current in the MS and the SS. During the forward current breaking process (Fig. 13.29 left), the initial direction of the oscillating current is the direction which commutation requires, so the MS current directly drops to zero. In the reverse current breaking process (Fig. 13.29 right), the initial direction of the oscillating current is opposite to the direction of commutation, so the MS current first increases and then decreases, and before the second oscillation peak, it drops to zero. Because the SS is in the conducting state at this time, once the current of the MS crosses zero, the arc will be extinguished directly. After that, the SS continues to carry the fault current. Finally, at 2.7 ms after the command is received, the MS contacts are sufficiently spaced, and the SS is turned off, resulting in an overvoltage of 800 kV to rapidly decay the current, and the breaking is completed.

Figure 13.30 shows the test results of the reclose. After the DC circuit breaker completes the first 25 kA current interruption, K_{21} is opened, and K_{22} is closed to connect C_{DC2} to the experimental circuit to simulate the pre-fault in the system. After 300 ms, the DC circuit breaker tries to reclose through its SS and turns off again quickly when the current rises to 6.8 kA.

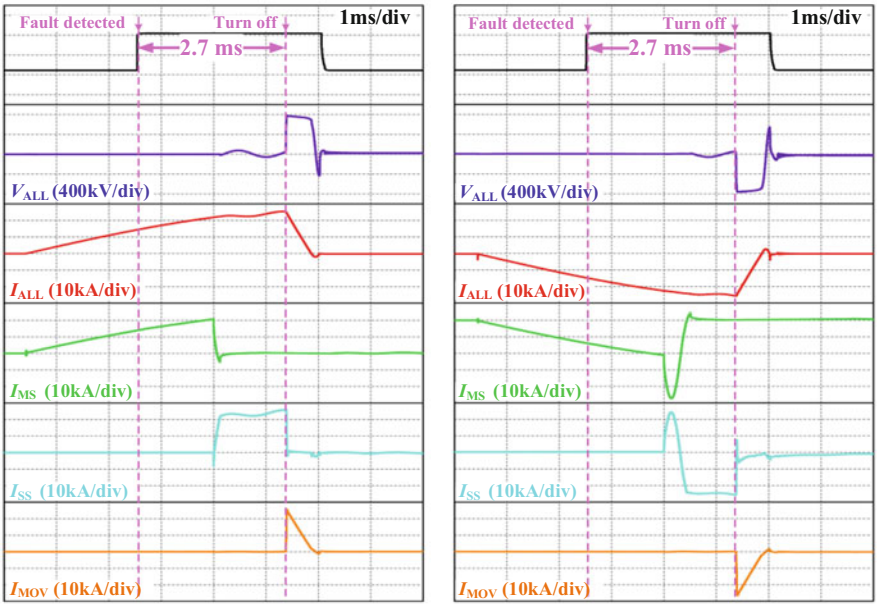

Fig. 13.29 DC circuit breaker current shutdown test waveform

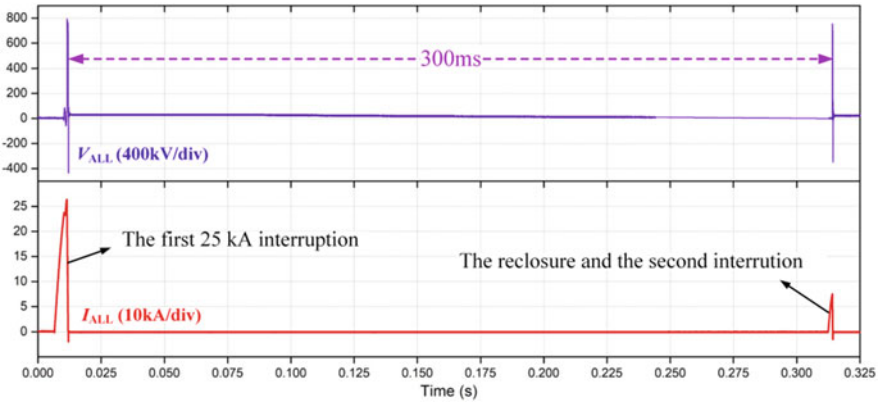

Fig. 13.30 Opening and reclosing test waveform

8 Concluding Remarks

In this chapter, the engineering application research of 535 kV hybrid DC circuit breaker is carried out:

1. A 535 kV/25 kA power electronic multilevel switch is developed based on the discrete MOV modular connection and the diode bridge bidirectional optimized

Fig. 13.31 535 kV DC circuit breaker in the Kangbanuoer converter station

structure. IEGT and ordinary recovery diodes are successfully applied to the field of DC circuit breakers for the first time. On the basis of the research, the fast MS and the current commutation driver circuit suitable for 535 kV DC circuit breaker are developed, respectively.

2. A dedicated multipotential high-voltage isolation power supply system is also designed for large-scale electrical equipment in DC circuit breakers. Two experimental platforms for power electronic series devices and hybrid DC circuit breakers are built to realize interruption testing of DC circuit breaker. It has been proven by experiments that the 535 kV hybrid DC circuit breaker can interrupt a current of 25 kA within 2.7 ms and withstand 800 kV overvoltage during the breaking process, reaching the world's leading level.
3. At present, two 535 kV hybrid DC circuit breakers based on the scheme in this chapter have completed all installation and commissioning in the Kangbanuoer converter station of Zhangbei Flexible DC Project (Fig. 13.31) and have been put into official operation.

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Chapter 14
Ultra-fast Resonant Hybrid DC Circuit Breaker

Nathan D. Weise

1 Hybrid DC Circuit Breaker

DC breaker technology prevalent in practice has many issues including: (1) Arcing in vacuum interrupters that damages the contact faces, (2) hybrid breakers have semiconductors in the path of the load current during normal operation resulting in low efficiency, (3) actuators lack sufficient force to open vacuum interrupters in under 1 ms, (4) low power density, and (5) lack of scalability.

1.1 DC Breaker Technologies

DC breaker solutions fall into one of the three categories. The first one is a mechanical DC breaker, shown in Fig. 14.1. This mechanical DC breaker usually consists of a solid contact made of copper for the conduction of the load current. These devices are simple to operate. An electro-mechanical actuator moves the contacts between being open and closed. The closing operation is simple and typically does not create arcs between contacts when closing due to system inductance. However, the opening operation is more complex and generates arcs. These arcs contain high energy and high temperature leading to potentially deforming or destroying contact interfaces over time. Arcs can lead to decreased lifetime of the mechanical circuit breaker. Furthermore, some application specifications cannot tolerate having arcs present. Mechanical breakers often implement a component called an arc chute. This device is designed to move the arc away from the current conducting interface into a chute

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https://doi.org/10.1007/978-3-031-26572-3_14

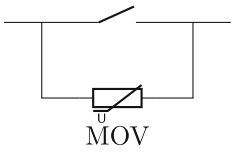


Fig. 14.1 Mechanical DC circuit breaker

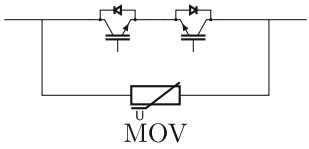


Fig. 14.2 Solid-state DC circuit breaker

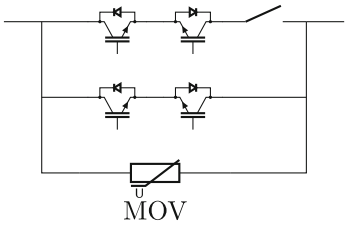


Fig. 14.3 Hybrid DC circuit breaker

to spread the arc over a larger distance and extinguish it. The arc chute increases the lifetime of the mechanical breaker.

The second DC breaker category is the solid-state DC circuit breaker, depicted in Fig. 14.2. They typically consist of two semiconductor devices in anti-parallel, illustrated as IGBTs, but could be MOSFETs or any other type of semiconductor depending on voltage and current requirements. In parallel with the semiconductors is an energy absorber that can be realized with metal oxide varistors (MOVs) or transient voltage suppression diodes (TVSs). Solid-state circuit breakers are extremely fast at opening and closing operations and are only limited by the semiconductors switching speed and stray inductances. Since the current through the semiconductors can be shut off much faster than the current that can be brought to zero via the system line inductance, the residual energy stored must have a path to flow; otherwise, the semiconductors will be destroyed. Once the current has commutated out of the semiconductors, the MOVs or TVSs will forward bias and conduct current until the line current reaches zero. Although these breakers can be very fast in practice, due to the semiconductors in the path of the current, they suffer from low efficiency and require thermal solutions for the semiconductors.

The third DC breaker category is the hybrid DC circuit breaker, illustrated in Fig. 14.3. In theory, the hybrid dc breaker is designed to combine the benefits of both the mechanical breaker and the solid-state breaker into one breaker. That is to say that the hybrid breaker uses a mechanical contactor for low resistance and high efficiency. Additionally, it contains power electronics to commute the current to zero through the contactor before the contactor opens. The power electronic circuit to commute the current comes in various implementations depending on the type of hybrid. Lastly, in parallel is an energy absorption component that will conduct

Table 14.1 Quantitative technology comparison

Technology	Cost	Power Density	Efficiency	Lifetime	Scalability	Response Time
Mechanical Breaker	Low	High	High	Low	Low	Slow
Solid State Circuit Breaker	High	Low	Low	High	High	Fast
Hybrid Circuit Breaker	High	Low	Medium	High	High	Medium
Ultra Fast Resonant DC Breaker	Low	High	High	High	High	Fast

current when the power electronics and contactor are open to remove any residual energy left in the system.

A qualitative comparison of critical metrics for the three technologies is shown in Table 14.1. Mechanical breakers suffer from low lifetime, low scalability, and slow response time. Solid-state circuit breakers solve those issues, but at high cost, low power density, and low efficiency. Hybrid circuit breakers increase efficiency but still suffer from high cost and low power density.

The ultra-fast resonant DC breaker (UFRDCB) solves the issues regarding the previously discussed technologies. The UFRDCB utilizes a mechanical contactor for low losses and high efficiency, an ultra-fast actuator to enable sub-500μS opening times, resonant power electronic current source to drive the current to zero through the contactor during opening, and a TVS-based energy absorption circuit to dissipate residual energy stored in the line during turnoff. The UFRDCB presents a comprehensive solution for the DC breaker market. In the next section, each component of the UFRDCB will be discussed, the normal operation will be presented, the fault operation will be discussed, and finally hardware results of the breaker will be presented.

2 Ultra-fast Resonant DC Breaker

The UFRDCB is shown in Fig. 14.4. The UFRDCB is composed of six distinct components crucial to the operation of the breaker. The first component is the vacuum interrupter shown as VI in the circuit diagram in Fig. 14.4. An Eaton vacuum interrupter is illustrated, cut open, to show the internal contacts, springs, and bellows within the bottle. The VI is the component that flows the complete load current during normal operation. It is critical that this device has a very low resistance so that the breaker will have a very high efficiency. Other devices can be used in this position, such as a relay or a contactor. The second component is the actuator. This is an electro-mechanical device that produces linear force in order to open and close the vacuum interrupter. An Eaton actuator for their AC recloser series is shown in Fig. 14.4 on the left. The actuator will have accompanying power electronics to actuate the actuator open and closed. The third component is the resonant current source and is shown as a dependent current source in Fig. 14.4. This is a power electronic h-bridge with a DC bus in series with a resonant inductor capacitor tank (Fig. 14.5).

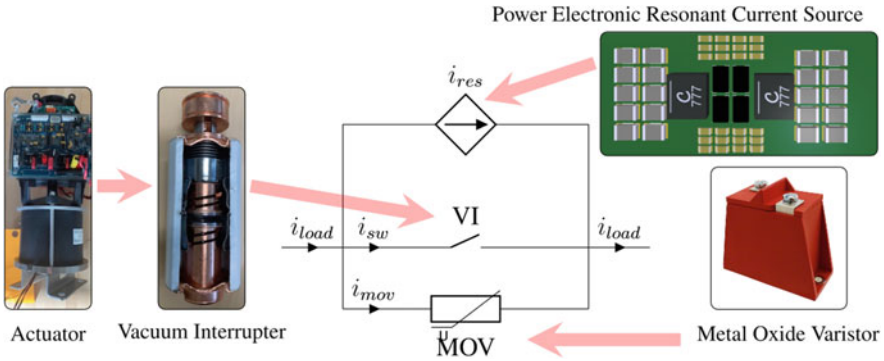


Fig. 14.4 Hybrid resonant DC circuit breaker

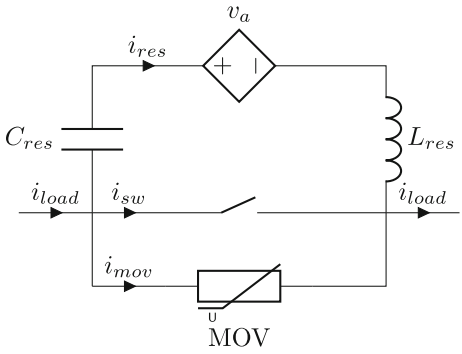


Fig. 14.5 Equivalent resonant circuit for Hybrid resonant DC circuit breaker

3 Normal Operation

The circuit implementation of the hybrid resonant DC circuit breaker is shown in Fig. 14.6 implemented in a full system with a source, line impedances, and load. The energy source is modeled as an ideal voltage source V_{source}, the line impedance between the source and the DC breaker is Z_{l1}, the line impedance between the DC breaker and the load is Z_{l2}, and the load impedance is labeled as Z_{load}. It is important to note that the ideal voltage source, V_{source}, and two line impedances, Z_{l1} and Z_{l2}, are linear and thus serve as good enough models for discussion and simulation purposes. The load impedance, Z_{load}, here is modeled as a linear RL load, but in practice this impedance can be highly nonlinear due to things such as front-end diode rectifiers and the like.

The hybrid resonant DC breaker is shown in green in Fig. 14.6. The inductance L_s is not required but is added if needed to slow the rate of increasing current during a short. For example, if the system that is being protected by a DC breaker has very low impedance, Z_{l1} and Z_{l2}, such that the DC breaker cannot open or respond in time during a short circuit event, L_s is added to guarantee a minimum amount of impedance and set the floor for the smallest rate of rise of current during an

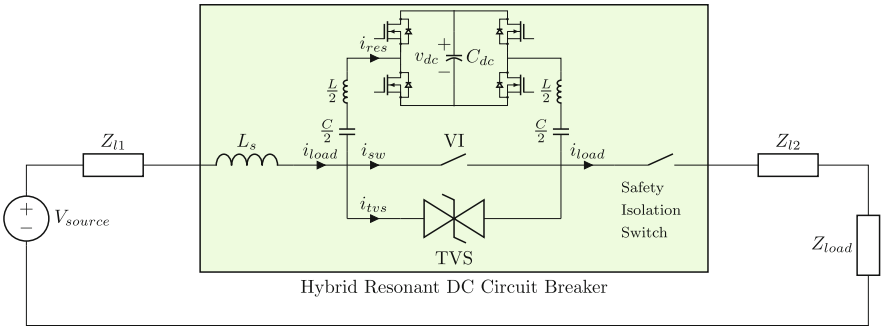
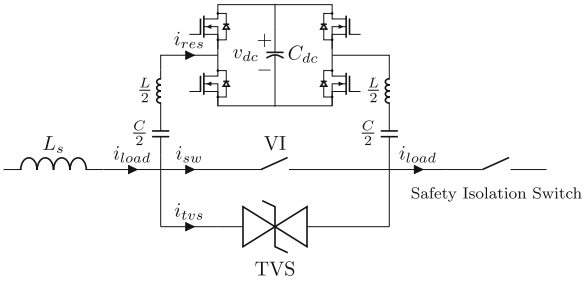


Fig. 14.6 Hybrid resonant DC circuit breaker

Fig. 14.7 Hybrid resonant DC circuit breaker



unexpected short circuit. In order to determine if this inductance is needed in the DC breaker, an independent analysis of the system to be protected has to be conducted for each individual application. The interrupter is depicted as VI in Fig. 14.6. The VI is the main switch and carries the full load current during normal operation. The transient voltage suppressor diode is labeled as TVS. This device will carry current after the VI opens removing any residual energy in the system. The resonant current source is implemented with a full bridge consisting of 4 MOSFETs and a DC bus v_{dc}. Additionally, there is a capacitor and an inductor, C and L, that make up the resonant tank. For balance, the inductor and capacitor value is split in half between each side of the VI and the h-bridge.

3.1 Off Operation

The hybrid resonant DC breaker in the off operation is shown in Fig. 14.7. Both the VI and the safety isolation switch are open. No current can flow between the source and the load in this configuration. Furthermore, because the hybrid resonant DC breaker also contains a safety isolation switch, there is no leakage current between the source and the load through the resonant current source and the TVS.

3.2 On Operation

The hybrid resonant DC breaker in the off operation is shown in Fig. 14.8. The load current is shown in red and flows from the source through the inductor L_s, the VI, and the safety isolation switch to the load.

The steady-state losses of the DC breaker depend on the resistance of the inductor L_s, the VI, and the safety isolation switch and are illustrated in Fig. 14.9. The total resistance in the path from the source to the load inside the hybrid resonant DC breaker is shown in (14.1).

$$R_{dc} = R_s + R_{VI} + R_{SIS}. \tag{14.1}$$

Furthermore, the on-state losses of the hybrid resonant DC breaker are defined in (14.2).

$$P_{loss} = i_{load}^2 R_{dc}. \tag{14.2}$$

The efficiency of the hybrid resonant DC breaker is defined in (14.3) assuming the input impedance, Z_{l1}, is zero.

$$\eta = \frac{V_{source} i_{load} - P_{loss}}{V_{source} i_{load}}. \tag{14.3}$$

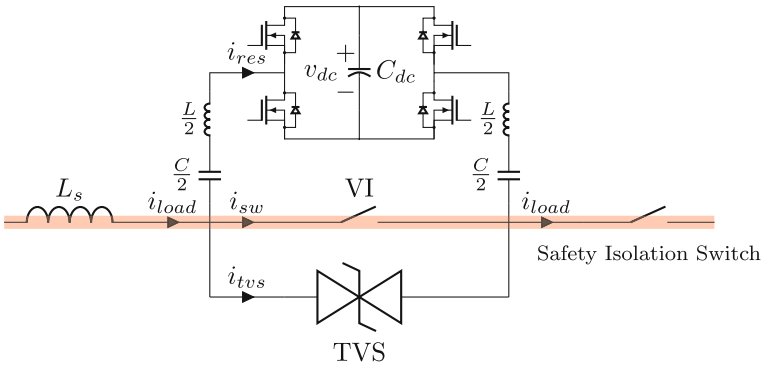


Fig. 14.8 Hybrid resonant DC circuit breaker, normal operation, DC breaker feeding load

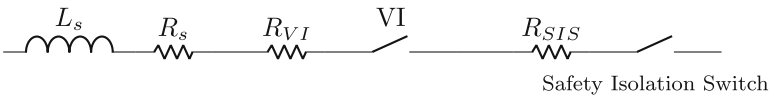


Fig. 14.9 On-state resistance path for DC breaker on

3.3 *Transition from On to Off State*

This subsection will describe in detail the ideal transition from on state to off state of the hybrid resonant DC circuit breaker. The load current, i_{load}, the VI current, i_{VI}, and the resonant current-source current, i_{res}, for a complete turnoff sequence are illustrated in the first plot in Fig. 14.10. Additionally, the half-bridge voltage, v_{HB}, and the breaker voltage, v_{TVS}, are illustrated in the second plot. There are four main states of the breaker when turning off.

The first state is the on state, and VI carries the full load current. This is illustrated from time t_0 to time t_1 in Fig. 14.11. The blue current is the load current, and it matches the VI current shown in red. The resonant current-source current is zero. This state is illustrated schematically in Fig. 14.8.

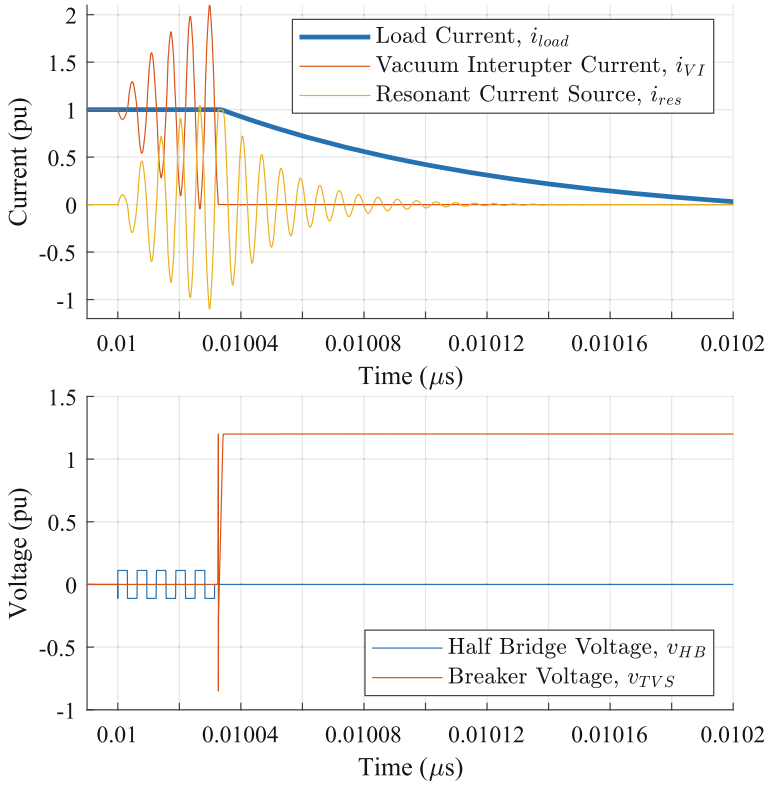


Fig. 14.10 Timing for opening of Hybrid resonant DC breaker

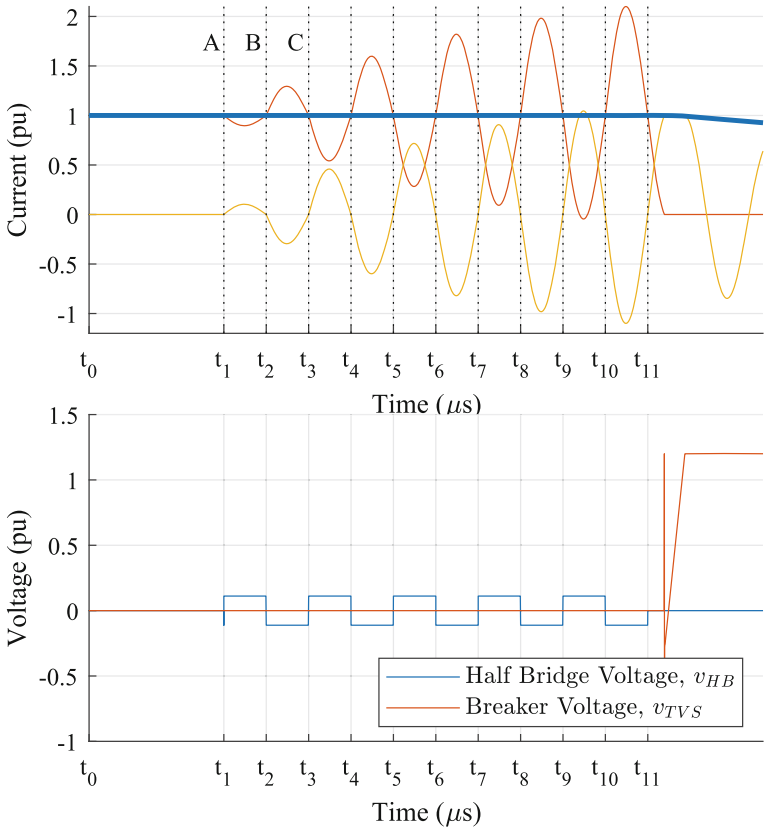


Fig. 14.11 Timing for opening of Hybrid resonant DC breaker

The next state is the ramping of the resonant current source. The goal of the ramping is to match the resonant current-source current to the load current such that the VI current is zero. During time t_1 to time t_2, two switches turn on in the resonant current source as depicted in Fig. 14.14. The equation for calculating the current for this state is shown in Eq. 14.9. The major advantage of this type of current source is that you can leverage lower voltage devices in the h-bridge relative to the DC voltage being protected by the DC breaker.

The experimental results of an opening operation of the dc breaker are shown in Fig. 14.15. At time zero, the opening operation starts and the resonant current starts to ramp up. Consequently, the current through VI ramps toward zero. Approximately fifty microseconds into opening, the current goes to zero in the VI, the VI opens, and the residual current commutes over to the MOV. The breakdown voltage of the MOV sets the rate of decay of the residual current. The current decays through the MOV to zero and completes the opening operation.

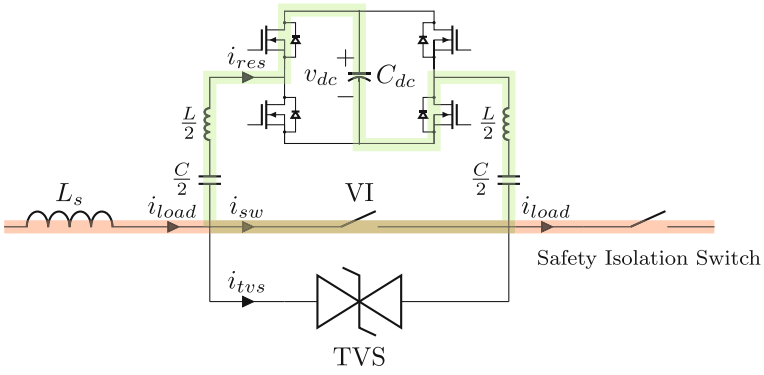


Fig. 14.12 Hybrid Resonant DC circuit breaker, normal operation, DC breaker feeding load, applying positive VDC to resonant circuit

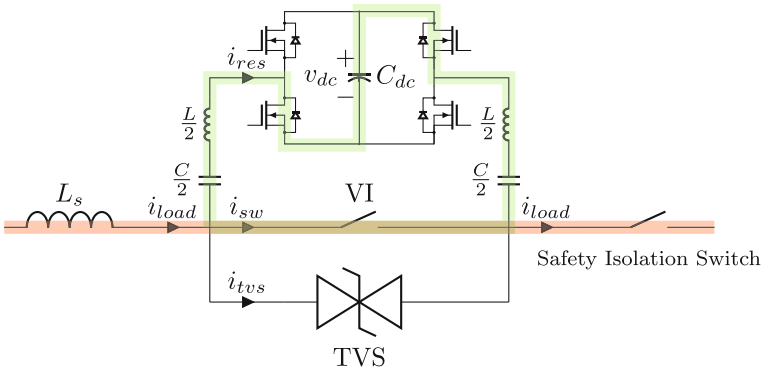


Fig. 14.13 Hybrid Resonant DC circuit breaker, normal operation, DC breaker feeding load, applying negative VDC to resonant circuit

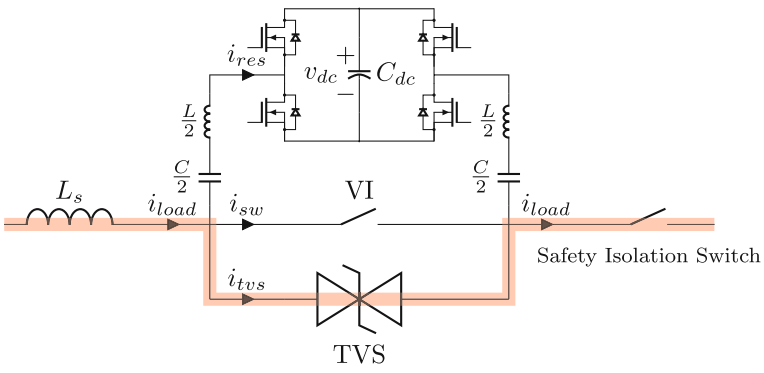


Fig. 14.14 Hybrid Resonant DC circuit breaker, TVS absorbing residual system energy

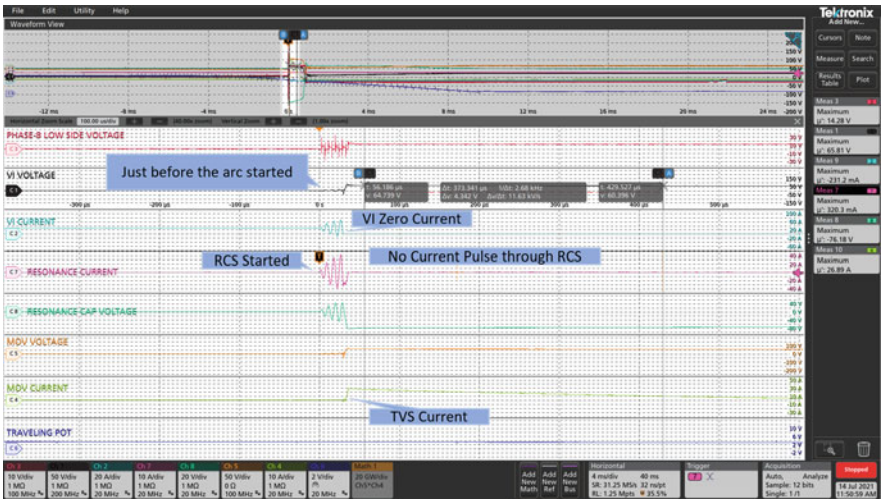


Fig. 14.15 Hybrid resonant DC circuit breaker opening experimental result

4 Resonant Current Source

In Fig. 14.16, let the damped radian frequency be

$$\omega_d = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}, \tag{14.4}$$

where R is modeling the finite resistance of the switches used to create a controllable voltage source and the resistance of the vacuum interrupter. The controllable voltage source is realized with a h-bridge and can realize output values of $+V_d$, 0, and $-V_d$, where V_d is the voltage of the DC bus. The inductor L and capacitor C are external components. Let the damping be defined as

$$\alpha = \frac{R}{2L}. \tag{14.5}$$

The voltage applied to the resonant circuit, in Fig. 14.5, alternates between V_d and $-V_d$ at the damped radian frequency, see Figs. 14.12 and 14.13. The first time instant at which the current peaks, refer to Fig. 14.17, in the resonant current source is defined as

$$t_{peak1} = \frac{1}{\omega_d} \arctan\left(\frac{\omega_d}{\alpha}\right). \tag{14.6}$$

The subsequent time instants in which the current will peak are defined in

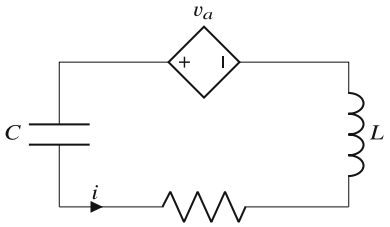


Fig. 14.16 Resonant current-source circuit topology for theoretical analysis

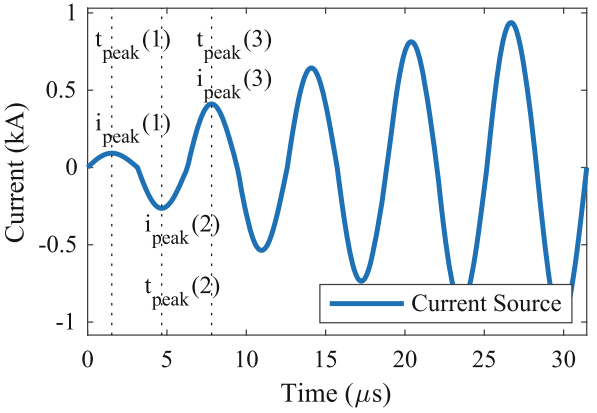


Fig. 14.17 Resonant current source timing

$$t_{peak}(n) = (n-1)\frac{\pi}{\omega_d} + t_{peak1}, \tag{14.7}$$

where n is a positive integer, representing how many cycles of alternating voltage have been applied to the resonant series circuit. The coefficient of the underdamped ringing current for each cycle is defined by

$$B_2(n) = \frac{V_d(-1^{n-1}) - V_c(n-1)}{L\omega_d}, \tag{14.8}$$

where V_d is the DC bus voltage of the H-bridge and V_c is the initial capacitor voltage. The peak current for each cycle can be found as

$$i_{peak}(n) = B_2(1)e^{-\alpha t_{peak1}} \sin(\omega_d t_{peak1}). \tag{14.9}$$

Finally, the voltage stored in the capacitor at the end of a cycle can be found using

$$V_c(n) = B_2(n)\frac{1}{C}\frac{\omega_d}{\alpha^2+\omega_d^2}(e^{-\alpha\frac{\pi}{\omega_d}} + 1) + V_c(n-1). \tag{14.10}$$

The analysis allows for calculation of the current peaks, the timing when those peaks occur, and damped radian frequency. The peak values of current and when in time they occur for the resonant current source are depicted in Fig. 14.17.

Fig. 14.18 Resonant current-source ramp to 600 A at 82 kHz

Furthermore, the analysis allows to find the maximum current that the resonant circuit will be able to provide. This value is crucial for the design of the breaker because it needs to be able to source the worst-case fault current. This analysis is used for the design of the inductor and capacitor for the resonant current source. A significant advantage of this topology is that the resonant current-source h-bridge can be any voltage, it does not depend on the breaker voltage, and thus it can be substantially lower than the breaker blocking voltage. This permits the use of low-voltage high-current devices leading to smaller weight, smaller volume, and lower cost.

The experimental resonant current-source results for a 600 A peak at 82 kHz pulse ramp are shown in Fig. 14.18. The top two waveforms are the PWM gating signals for the switches in the h-bridge. The h-bridge applies an alternating voltage to the resonant circuit. The next waveform is the capacitor voltage. The voltage oscillates at the damp radian frequency. The last waveform is the resonant current. This current oscillates at the damped radian frequency, and the magnitude increases cycle to cycle. The h-bridge pulsed five times and resulted in a 600 A peak current.

Another experimental result is shown in Fig. 14.19 based on a different damped radian frequency. The frequency is 212 kHz, and the current ramps to 1 kA in only 3 cycles.

5 Actuator

The efficacy of the ultra-fast resonant hybrid DC breaker is highly dependent on the implementation of the actuator. The high rate of rise of current $\frac{di}{dt}$ during

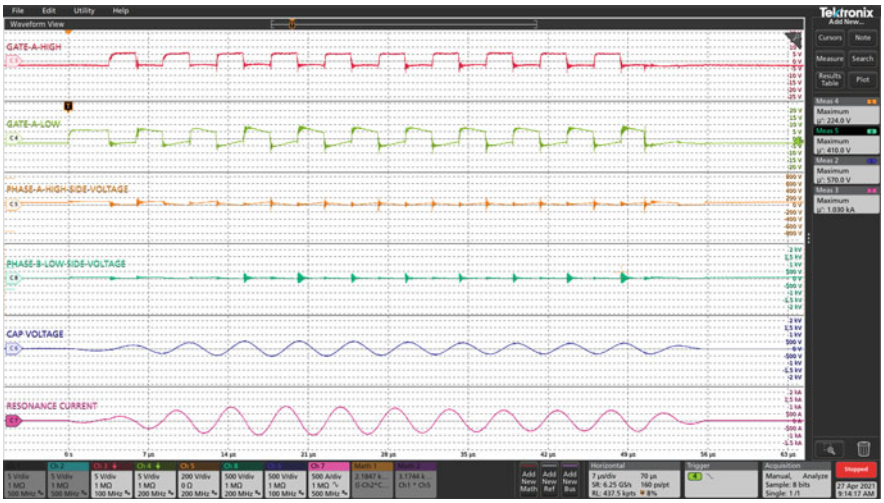


Fig. 14.19 Resonant current-source ramp to 1 kA at 212 kHz

faults requires fast mechanical actuation in order to mitigate potential damage. Fast actuating mechanisms are predominately electromagnetic as opposed to pneumatic, hydraulic, or spring loaded mechanisms. The latter devices are not suitable for DC breakers as they require several milliseconds to open, while the former can achieve sub-millisecond opening times making them sufficient for protecting DC. Additionally, actuation devices based on piezoelectric, magnetostrictive, and other smart materials exist, but the small stoke length of these mechanisms remains a considerable drawback.

5.1 Design Considerations

The design of a actuator system is divided into four critical components: latching mechanism, drive mechanism, drive and control, and buffer system. Additionally, the following list are requirements to be considered during the design:

- Stroke length
- Speed
- Energy required for opening/closing operations
- Type of bi-stable mechanism
- Damping requirement
- Structural composition
- Device materials
- Drive and control circuit composition

The stroke length is the distance the actuator needs to move and maintain for voltage breakdown in the open position. This is a critical design parameter and will predominantly depend on the working system voltage with larger voltages requiring a large distance and lower voltages requiring less distance. Just as important as stoke length is the speed in which the stroke length is obtained. Again, the higher voltages with lower system inductances will require fast actuator, and lower voltages with higher system inductances can operate slower. The energy requirement for opening and closing operations will depend highly on the actuator topology. The energy will be required to be stored in capacitors due to the high amount of energy required in short duration during an opening event. The faster the actuator opens the more required energy. The bi-stable mechanism is a device that latches the actuator in the open and closed positions without requiring electrical energy to hold it in a particular position. There are traditionally four different types of these mechanisms, and they will be discussed in Sect. 5.3. The actuators produce large forces and acceleration in order to opening in sufficient time for DC applications. This high speed and acceleration exposes the structure to high stresses. This will require a damping device in order to slow the actuator down during the changing of positions, thereby reducing structural stress and reducing bouncing. Typical damping solutions include mechanical dampers and/or electrical control of actuator. The drive and control circuit of the actuator will require processing large current and/or voltage during the open/close operations. These circuits could be single pulse drive, multiple pulse, or pulse forming. Traditionally, these circuits process kiloamps of current, and thus, it is not economical to introduce a PWM-based converter for drive control.

An electromagnetic-based actuator provides the best performance for fast actuation among the possible candidate technologies. The following section will discuss the electromagnetic actuators reported in the literature and the design of a single- and double-sided Thomson-coil-based actuator.

5.2 Single-sided Thomson Coil Actuator

Two topologies of electromagnetic actuators are predominately reported in the literature. These devices are the Thomson-coil-, Table 14.5, and permanent-magnet-based actuators. A review of permanent-magnet-based actuators reported in the literature is shown in Table 14.2. Note that all of these devices are in the tens of millisecond range for opening. These devices are too slow for protecting DC-based systems as the fault current would rise to disastrous levels before the actuator would open. Permanent-magnetic-based actuators are more efficient and more power dense relative to Thomson-coil-based actuators. Furthermore, they are more force dense relative to Thomson-coil-based actuators. Despite these advantages, they are more expensive, at risk of demagnetization, and are more expensive than Thomson coils.

A single-sided Thomson coil is depicted in Fig. 14.20. The figure shows half of a cylindrical axis symmetric Thomson coil with the fixed coil on the bottom and the movable disc on top.

Table 14.2 Comparison of permanent-magnet-based actuators

Structure	Key features
Level shaft and two magnets operated by two coils [6, 10]	Rated voltage/current: 12/17.5/24 kV, 3150/3150/2500 A
	Opening time: 30∼50 ms
Used in ABB VM1 Vacuum	Closing time: 40∼60 ms
Circuit breaker [1]	Distance between terminals: 31 mm
Auxiliary PM on two ends for latching	Rated voltage/current: 45 kV
	Opening time: 35 ms
Moving coil and iron core [5]	Distance between terminals: 80 mm
Based on NdFeB Magnets	Rated voltage/current: 400 V/3200 A
A co-simulation (Simulink–Adams) method is used to predict transient performance [7]	Opening time: 40 ms
	Distance between terminals: 22 mm
Improved control methods	Rated voltage/current: 400 V/3200 A
Two coils are supplied with direct impulse currents [8]	Opening time: 13 ms
	Closing time: 22 ms
	Distance between terminals: 22 mm
Two coils	Maximum speed: 4.3 m/s
PM remanence 1.25 T [14]	Detent force: 5900 N
	Distance between terminals: 20 mm

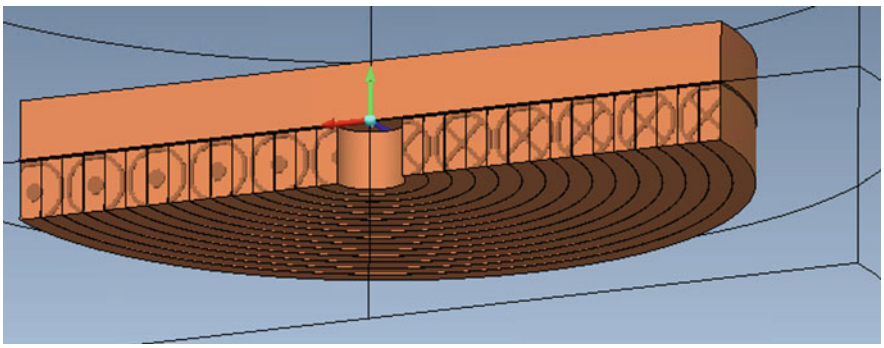


Fig. 14.20 Single-sided Thomson coil

In the figure, the current coming out of the page is denoted on the left of the coil, and the current going into the page is denoted on the right side of the coil. When the coil is excited with current, the solid disc is accelerated in the upward direction away from the coil. Critical design parameters that affect the operation of the Thomson coil are as follows: coil material, coil turns, coil thickness, coil height, disk mass, disk radius, disk material, capacitor bank storage, and dc voltage of capacitors. Table 14.3 contains a list of parameters considered for the design of a single-sided Thomson coil shown in Fig. 14.20.

Table 14.3 Single-sided Thomson coil parameters

Item	Value			
Capacitor bank (mF)	2.3	1.5	1.5	1.5
DC voltage supply (V)	600	1200	1800	2400
Turns number (fixed coil)	15			
Outer diameter (movable coil) (mm)	78	96	140	152
Material (fixed coil)	Conventional copper (Cu)			
Material (movable coil)	Copper beryllium (CuBe)			
Simulation traveling distance (mm)	8			
Disk mass (kg)	0.3	0.71	1.51	2

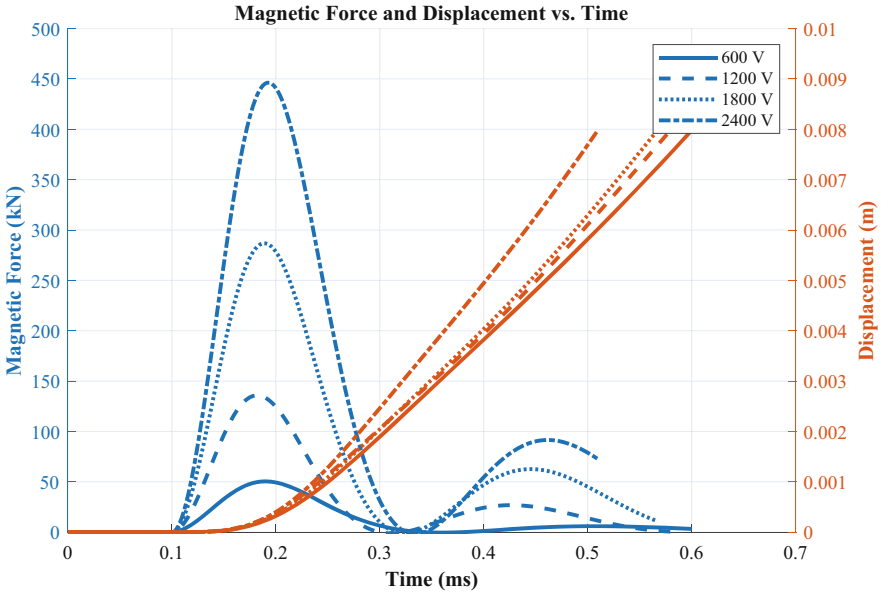


Fig. 14.21 Force and displacement versus time of Thomson coil designs

The Thomson coil actuator shown in Fig. 14.20 is simulated in a FEM magnetics package with the parameters shown in Table 14.3. The voltage of the capacitor bank, the mass of the disc, and capacity of the capacitor bank, and disc diameter are investigated for various values. The objective is to determine if there are trends in certain design parameters that are advantageous or disadvantageous. The force and displacement of the single-sided Thomson coil are shown in Fig. 14.21 for various parameter combinations noted in Table 14.3.

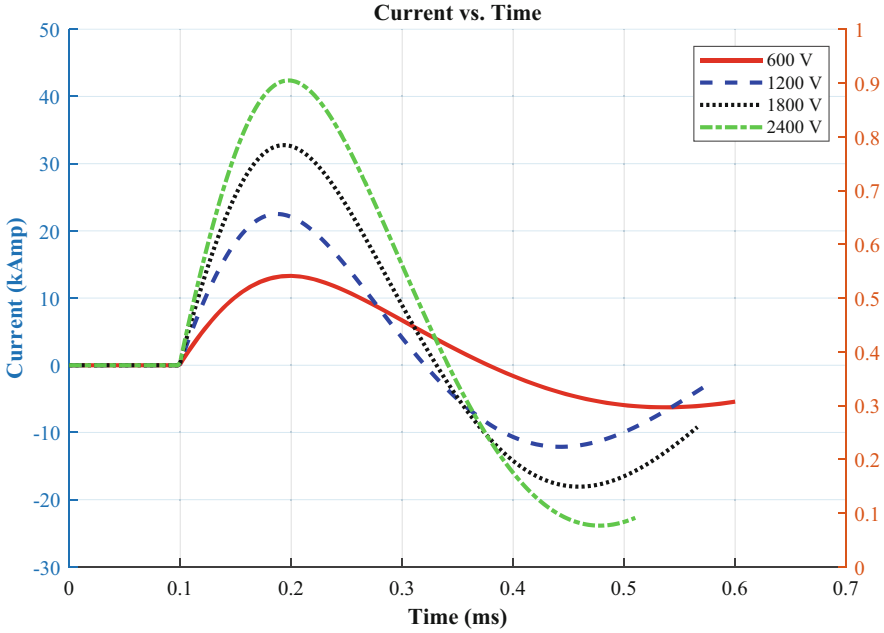


Fig. 14.22 Current versus time of single-sided Thomson coil

Four distinct capacitor voltages are simulated. These are the voltages the coil is connected to when simulating an opening event. Note, that higher voltages translate to higher forces and lower voltages to lower forces. Figure 14.22 illustrates the current vs. time during the opening event.

The larger the voltage source, the larger the current and thus the larger the force. The current rings vs. time because this actuator is connected to a capacitor. Note the current is in the range of kiloamps. At these large currents, it is very typical to simply connect an energy source across the coil, and let the dynamics dictate the operation as opposed to controlling the current and force with a converter. Controlling currents in these ranges is entirely too expensive and is generally not economical for these types of applications. The displacement of these simulations is relatively similar because the mass and radius of the disc were adjusted to keep them similar. This illustrates the importance of knowing the complete mass of the moving parts of your system. The more mass of moving parts, the increased currents and voltage needed in the design to meet a given displacement, velocity, and acceleration profile. When designing a Thomson coil, a key parameter will be the mass of the moving parts, and this mass will drive many design decisions.

Figure 14.23 shows the ohmic losses in the coil during the opening event. Note these losses are in the range of kilowatts. The losses are significant; however, they are for a short duration and therefore there is no concern. The energy of the single-sided Thomson coil is shown in Fig. 14.24 across four voltages. The peak energy

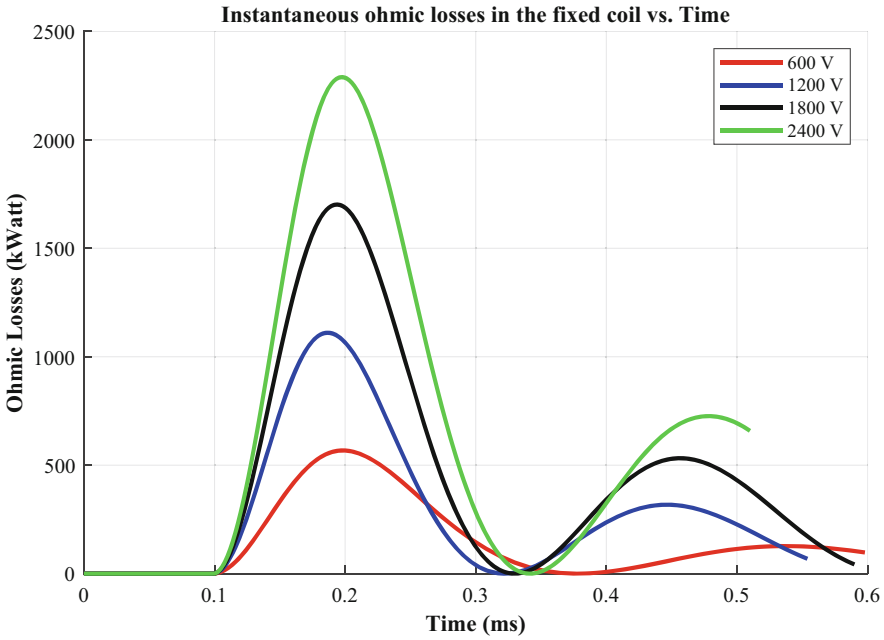


Fig. 14.23 Ohmic losses versus time of single-sided Thomson coil

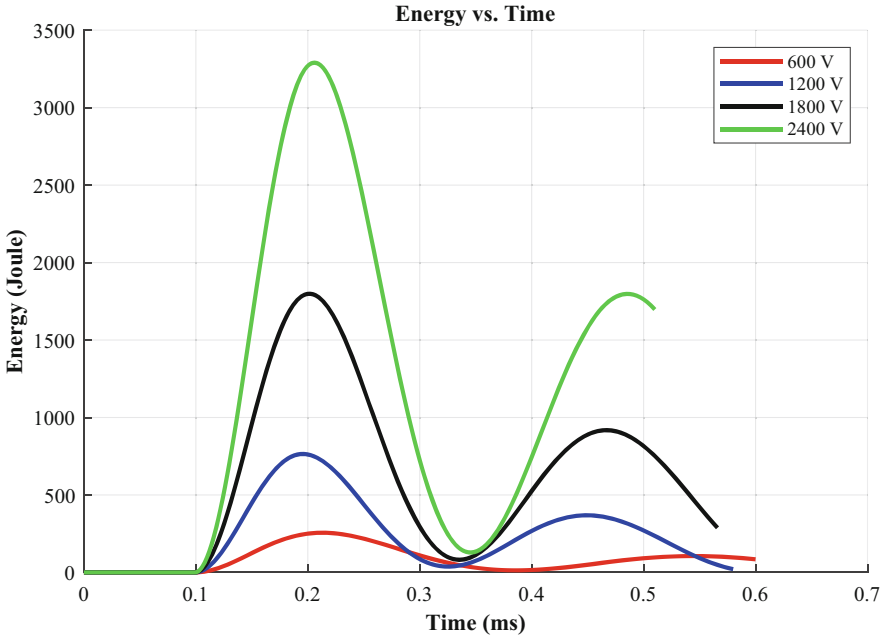


Fig. 14.24 Energy vs time of single-sided Thomson coil

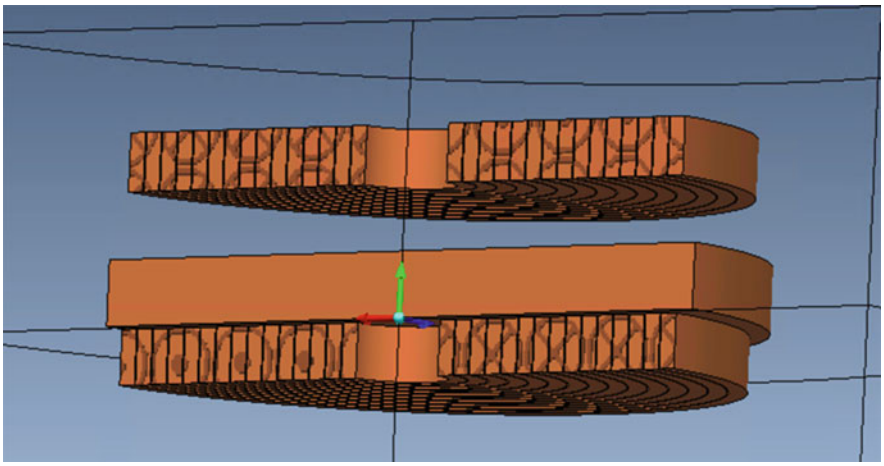


Fig. 14.25 Double-sided Thomson coil

Table 14.4 Double-sided Thomson coil parameters

Item	Value
Capacitor bank (mF)	1.5
DC voltage supply (V)	1200
DC voltage supply (V)	600
Turns number (fixed coil)	15
Material (fixed coil)	Conventional copper (Cu)
Outer diameter (movable coil) (mm)	100
Turn dimension (mm)	2.5×7.5
Thickness (movable coil) (mm)	9
Material (movable coil)	Copper beryllium (CuBe)
Simulation traveling Distance (mm)	8
Disk mass (kg)	0.63

again is significant. Thomson coils are known for low efficiency but the trade-off is high force in a short duration of time.

The Thomson coil actuator shown in Figure 14.25 is simulated in a FEM magnetics package with the parameters shown in Table 14.4. The voltage of the capacitor bank, the mass of the disc, capacity of the capacitor bank, and disc diameter are investigated for various values. The objective is determined if there are trends in certain design parameters that are advantageous or disadvantageous. The force and displacement of the double-sided Thomson coil are shown in Figure 14.26 for various parameter combinations noted in Table 14.4. Note that this arrangement can produce significantly more force relative to the single-sided Thomson coil. Moreover, this arrangement can open and close the actuator. The energy and velocity versus time of the double-sided Thomson coil is shown in Fig. 14.27. Note that energies peak around 65 Joules and velocity around 12 m/s. The upper and lower

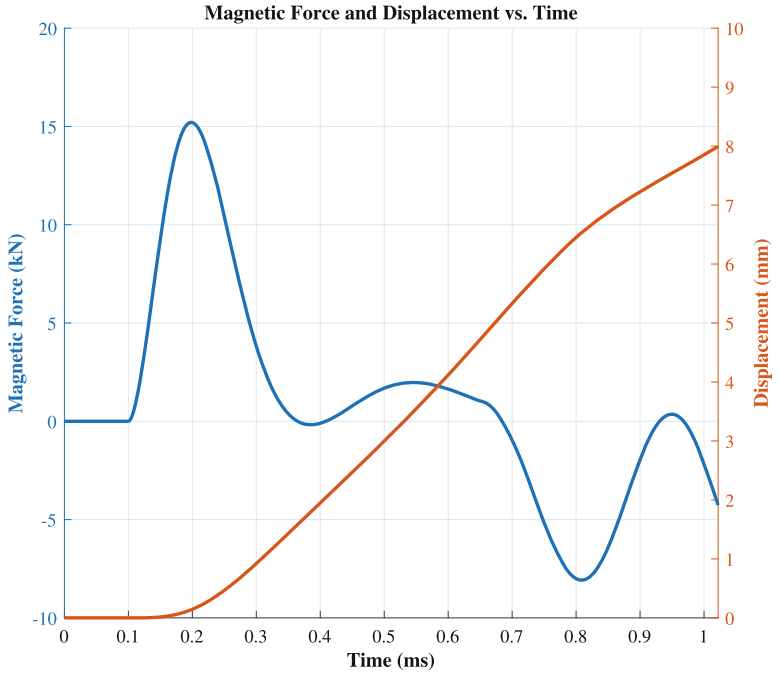


Fig. 14.26 Force and displacement versus time of double-sided Thomson coil

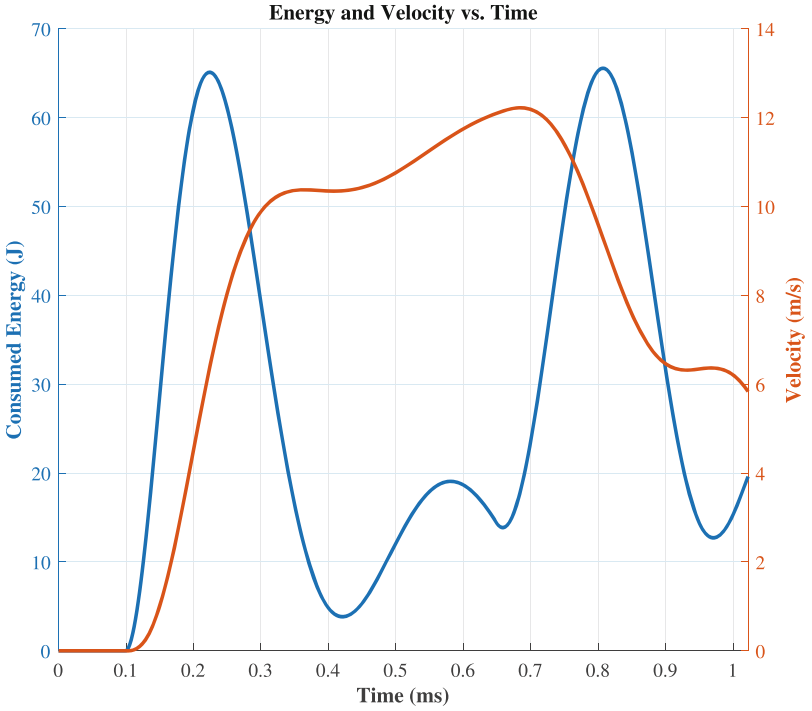


Fig. 14.27 Energy and velocity vs time of double-sided Thomson coil

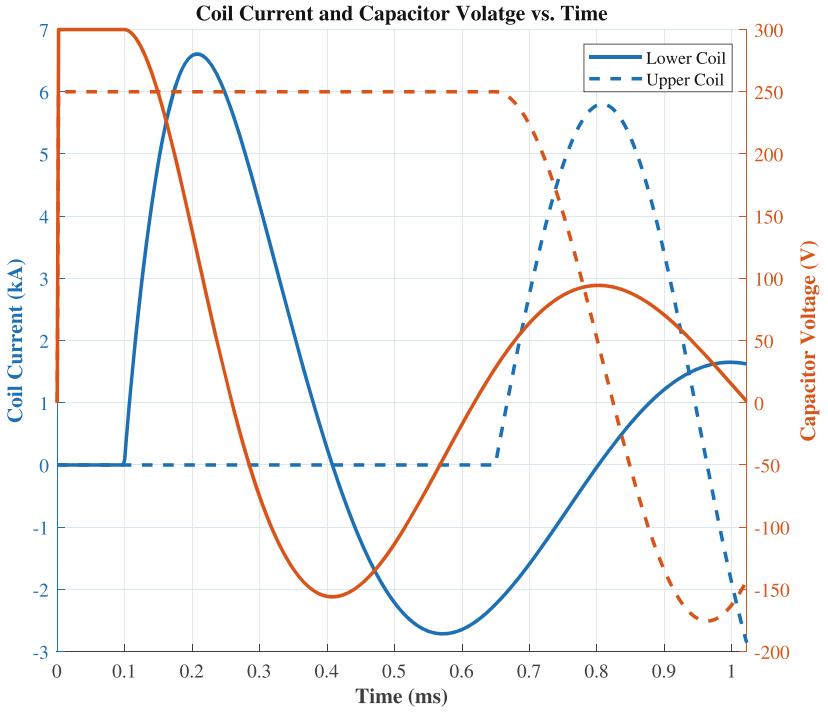


Fig. 14.28 Current and voltage versus time of double-sided Thomson coil

coil current and voltage of the double-sided Thomson coil is shown in Fig. 14.28. Observe that the currents and voltages of the double-sided Thomson coil are two to four times lower than in the single-sided Thomson coil. Furthermore, in spite of the reduced current and voltage, the acceleration and displacement of the double-sided Thomson coil is comparable to the single-sided Thomson coil. The currents and voltages experienced in the single-sided Thomson coil potentially could prove difficult to implement economically in a realized product.

5.3 Holding Mechanisms

Typically, the actuator is directly connected mechanically to the vacuum interrupter. The actuator needs a latching mechanism in order to create two stability points for the open and closed positions of the actuator. There are a variety of mechanisms that can achieve two stable positions for a linear actuator such as a helical spring, bi-stable spring, disc spring, and magnet holding. Table 14.6 contains a list of holding mechanisms in the literature for linear actuators [3].

Table 14.5 Comparison of Thomson-coil-based actuators

Structure	Key features
Copper disk, opening and closing coils, damping and holding mechanism, vacuum interrupter [9]	Rated voltage/current: 30 kV, 630 A
	1.3 mm in the first 1 ms
	3.1 mm in the first 2 ms
	Capacitor bank: 360 V, 2 mF
Pawl for latching Only one coil [12]	Current: 8 kA Max driving force: 200 kN
	Max speed of mover: 18 m/s
	Acceleration: 38000 m/s^2 in 450 us
	Opening time: 2 ms; Travel distance: 25 mm
	Capacitor bank: 2 kV, 1250 uF
Bidirectional Thomson coil actuator [2]	Rated voltage/current: 40.5 kV
	Opening time: 2.3 ms
	Distance between terminals: 28 mm
	Capacitor bank: 1400 V, 2.5 mF
Thomson coils with Arm mechanism Aluminum disk [4]	Opening time: 2 ms
	Traveling distance: 6 mm
	DC supply: 250 V

Table 14.6 Different holding mechanisms' performance [3]

Mechanism	Ref	Load/contact force	Stroke	Time	Device stiffness/weight
Helical spring	[11, 13]	2 kg/3.8 kN	25 + 3 mm	2 ms	34.6 kN/m
Bi-stable spring		5 kg/1000 N	26 mm	2.3 ms	63 N/mm 0.2 kg
Disc spring		4 kN	5–22 mm	2.7–4.5 ms	–
Disc spring		0.5 kg/330 N	11.68 mm	2 ms	1650 MPa 30 g
Magnet holding		375–632 N *	6 mm	2.75 ms	–
Magnet holding		1200 N	5 mm	4.9 ms	–

5.3.1 Bi-stable Spring

The bi-stable spring mechanism is widely used in linear actuators for vacuum interrupter applications. The mechanism has two stable states that keep the vacuum interrupter in the closed position or the open position. The bi-stable positions of this mechanism are achieved by supplying upward force in one position and supplying downward force in the other position. This device will add additional mass to the system, additional components susceptible to wear and tear, and a repulsive force that will need to be overcome by the actuator during opening and closing operations.

5.3.2 Helical Spring

Helical spring mechanisms use a compressed spring to maintain the closed state of actuator. When the actuator is to open, the force from the actuator compresses

the spring until a mechanical lock latches the spring in a compressed state thereby maintaining the open position. The lock unlatches when the actuator is to close from the open state, releasing the spring and forcing the actuator to close.

5.3.3 Disc Spring

A disc spring is a washer that forms a cone as you move from the outer radius to the inner radius. The disc spring works by deforming from one position to another between states. The mechanism is simple in nature that is useful for large loads, short stroke length and uses minimal space. This mechanism is generally not preferred in breaker type applications due to the stress and deformation of the material during state changes resulting in reduced lifetime and short stroke length.

5.3.4 Magnet Holding

A magnet holding mechanism is composed of a permanent magnet and magnetic material such as iron. These devices utilize the permanent magnet and magnetic material to create the holding force in the open and closed positions. The permanent magnet wants to naturally latch to the iron in either the open or closed position. These devices are relatively simple to design and operate. The disadvantage of this device is that it requires expensive magnets, the magnets are prone to demagnetization, and the device is bulky adding mass to the system.

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Part IV
Other Fault Protection Topics

Chapter 15
Gas Discharge Tubes for Power Grid Applications

David Smith and Timothy Sommerer

1 Introduction

Gaseous electronic devices or *gas discharge tubes* are hermetically sealed assemblies of electrodes and insulated enclosures that contain a specified gas composition and can be controlled to conduct current and block voltage. The goal of this chapter is to highlight the features and capabilities of gas tubes as an enabling technology for future direct current (DC) electric power systems, including meshed power grid, warships, subsea oil-and-gas distribution systems, and wind and solar farms.

Figure 15.1 shows an example of a laboratory-scale gas tube designed for 100-kV and 500-A rated voltage and current. This figure provides a schematic view of the device with the critical elements highlighted as well as a practical view of the device under test.

Gas tubes may be designed to achieve high standoff voltage and typically operate at moderate conduction current. Figure 15.2 shows the typical range of voltage and current limits for gas discharge tubes in comparison with various switch technologies. This highlights a clear benefit in standoff voltage capability that is attractive for various grid-scale applications. To provide the greatest benefit in power systems, the gas tube rating should be sufficient to handle the full-system voltage including transients, V_{sys}, across a single tube. Series connection should be avoided, where possible, to eliminate the complexity of voltage-sharing and be able to handle failures of devices in parallel only. Rather, tubes should be placed in parallel to handle the total system current, for the so-called $N + 1$ redundancy. Current-sharing circuitry is required. Tubes must be engineered to reliably fail open, to reduce the need for complex protective equipment.

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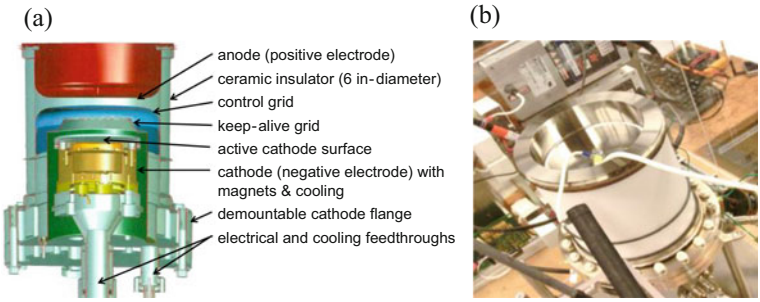

Fig. 15.1 Example laboratory gas tube designed for 100 kV and 500 A: (**a**) cutaway, (**b**) in test

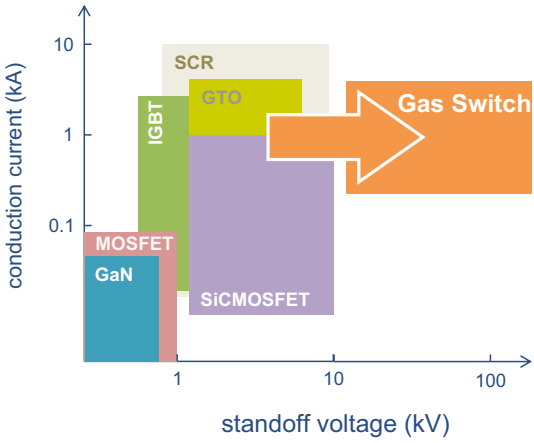

Fig. 15.2 Comparison of voltage and current limits for different switch technologies

Below, a brief overview is provided of system-level features and capabilities of gas tubes followed by an in-depth discussion of the device design and operation. Having established these details, example benefits of gas tubes in electric power systems are discussed, focusing on applications in DC-AC converters and circuit breakers. Finally, the operational considerations for gas tubes in electrical systems are outlined, along with recommendations for the technology development to become viable for the targeted applications.

2 Brief Overview of Gas Tube Features and Capabilities

Gas tubes are "fully controllable" in that they can be closed on command but can also open against current flow. The opening and closing transitions times are short (<5 μs). Switching losses are therefore low, and high-frequency operation ≫60 Hz is possible for uses like pulse-width modulation of line-frequency power.

Gas tubes close like an insulated-gate bipolar transistor (IGBT), latch on like a thyristor, and open like an integrated gate-commutated thyristor (IGCT). Closing is initiated by a voltage signal to the control grid (CG). Closing is fast because of rapid ionization growth in an overvolted gas volume. Current continues to flow after the CG is electrically disconnected (i.e., the device latches on). Opening is initiated by momentarily diverting the conduction current through the CG into associated power electronic controls. The opening time is also short, and energy dissipation on opening is correspondingly low because conductors are swept out of the HV region by an ion-acoustic wave, rather than by slower diffusion and recombination processes [1].

Gas tubes can block voltage bidirectionally, but in their basic form, they are unidirectional in terms of current flow and control. If full bidirectional operation is required, then a pair of antiparallel tubes can be used, or a more sophisticated tube can be constructed with two cathodes (negative electrodes) in a single hermetic housing [2].

Gas tube forward volt drop, V_{fwd}, is typically *low* during conduction, but at up to 500 V, the losses can be startlingly high depending on the system voltage. The value of V_{fwd} must be viewed in context that a single tube will handle the entire system voltage, 320–500 kV when used in HVDC applications. Even if $V_{\text{fwd}} = 500$ V can appear to be small relative to a 500-kV system voltage (i.e., 0.1%), such a voltage drop may be comparable with power semiconductors and eliminate the competitive advantage. However, the actual value of forward volt drop is dependent on the specifics of the device. Mode of cathode operation (cold or thermionic cathode) is the primary driver for determining the forward voltage, but cathode material type and gas type are also contributing factors. For cold cathodes, we may reasonably expect that the range of V_{fwd} is 200–500 V, whereas for thermionic cathodes 10–30 V is a representative range.

Gas tubes are extremely compact because they are insulated by dielectric liquids rather than air. The length of gas tubes 100–300 kV is only 20–40 cm. They are robust to certain transients and processes that would irreversibly damage solid-state devices. Specific cases must be analyzed, but some general tendencies can be stated. If a tube is subjected to an HV transient that is beyond its rating, it will close and conduct current, but the HV performance will not be permanently degraded. This is in contrast with solid-state devices, which are likely to be permanently damaged once exposed to excessive voltage. Likewise, a tube can withstand some degree of overcurrent and overheating without permanent degradation of overall performance; rather, the calendar operating life might be degraded. Ionizing radiation will not damage a tube, and a tube is relatively immune to spurious closure by ionizing radiation. In that sense, gas tubes are self-healing devices, like most nonsolid isolated devices, in contrast to power semiconductors which are typically permanently damaged once failed short or open.

Demonstrated gas tube current values remain modest relative to the requirements of large electric power systems. A few hundred amperes have been demonstrated in various experiments, with limited prospects of reaching thousands of amperes. Scaling to higher current is simple in principle: design the tube for a given current

density and then increase the cross-sectional area to achieve the desired total current up to the maximum current that the tube can open. However, there are important challenges to address in maintaining a radially uniform current distribution as well as overall heat dissipation for larger current devices. The practical limit to scaling is not known at this time.

The overall packaging of a gas power tube has not been designed, but it can be extrapolated from engineering practice for medical X-ray vacuum tubes, especially the X-ray tube systems in modern computed tomography scanners [3]. X-ray tubes operate at HV ~150 kV, dissipate ~15 kW/l during operation, are insulated by a dielectric fluid-filled jacket, are connected through HV quick connects to power and thermal management equipment of power density 5 kW/l, and are extremely reliable for the intended use. The entire X-ray tube system power and thermal system is ruggedized and packaged to operate on a rotating gantry with centripetal acceleration ~50 g (50 times Earth's gravity).

3 Gas Tube Design and Internal Operation

In this section, we will summarize the development, internal configuration, and operation of a gas tube. While there are several different physical configurations, we have focused on one that is derived from a pulsed-power gas tube [1]. That device, in turn, owes much to the design of metal-ceramic thyratrons. Several documents summarize this development and its commercial status:

- Historical evolution of the hydrogen thyratron [4]
- Factors leading to the development of ceramic hydrogen thyratrons [5]
- Description of modern thyratrons [6]

Aside from a brief recap of the important issues in these three references, we will focus here on aspects that have not been previously described, as well as the work that has been done to transform pulsed-power (low duty-cycle) thyratrons and gas tubes into a new continuous power (high duty-cycle) device for electric power system applications.

The mechanism for gas tube opening and closing is the same as in thyratrons and has been described in some detail for earlier pulsed-power tubes [1]. When electrically open, the voltage is held across the short, gas-filled gap between the anode and the CG. When electrically closed, an intense but diffuse (non-arc) plasma conducts electricity between the anode and cathode. Electrical turn-on is achieved via a voltage signal on the CG, while electrical turn-off is effected by transiently intercepting the conduction current through the CG to external power electronic controls. Figure 15.3 shows a schematic of the internal gas tube properties in open and closed states for the cold-cathode configuration. This includes a keep-alive grid to assist in plasma initiation in addition to the cathode, CG, and anode. Figure 15.4 shows a view of the plasma in a diode arrangement laboratory apparatus for both cold-cathode and thermionic cathode operation.

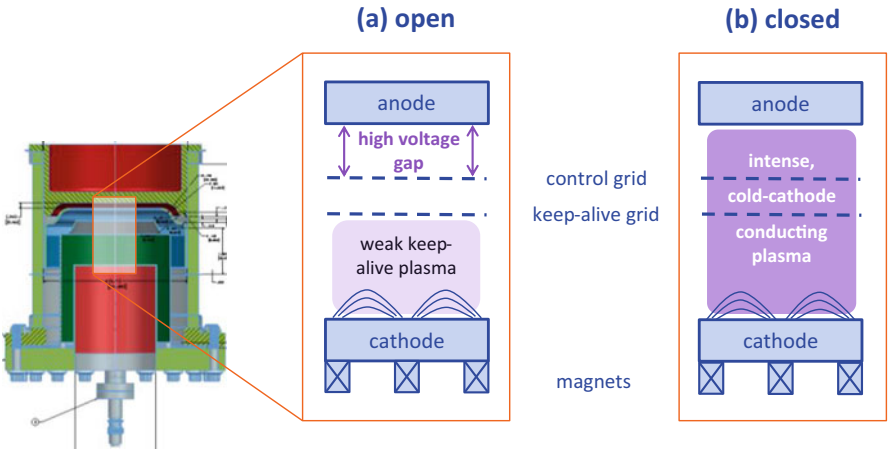

Fig. 15.3 Internal gas tube properties in (**a**) open and (**b**) closed states, shown for a cold-cathode configuration. The keep-alive grid assists in plasma initiation, while the control grid acts as the gate to open and close the device

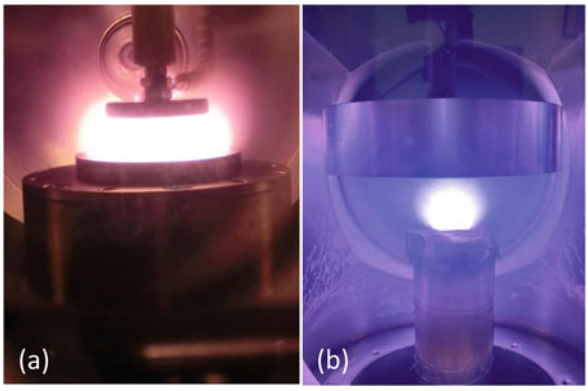

Fig. 15.4 Photograph of the laboratory apparatus during plasma conduction for (**a**) cold-cathode and (**b**) thermionic cathode operation

3.1 High-Voltage Design

Gas tube HV design is driven by the need to avoid three physical processes that lead to HV failure: (i) ionization and electrical breakdown of the insulating gas based on the applied voltage and gas volume (Paschen or gas breakdown), (ii) electron emission by solid conducting surfaces when exposed to strong electric fields perpendicular to the surface (vacuum breakdown), and (iii) electron multiplication along dielectric surfaces when exposed to strong electric fields parallel to the surface (flashover).

These HV considerations lead to a similar physical design for both the gas tube and its ceramic thyratron ancestor, a cylindrical insulator capped by reentrant

electrodes, where the electrode faces are separated by a relatively small distance and fit tightly within the cylindrical insulator [4].

The basic sequence of gas tube HV design [7] must cover the following elements. The HV electrode separation (anode-CG) must be large enough to avoid vacuum breakdown, where the intervening field is strong enough to pull electrons out of the (cathodic) CG by field emission. The gas pressure (number density) in the anode-CG space must be low enough to prevent Paschen (gas) breakdown. The gas pressure (number density) in the gas tube must also be sufficiently high to form a highly conductive gas plasma when the gas tube is electrically closed. The latter two requirements conflict with each other and ultimately limit the voltage rating of the device [7, 8] for a given conduction current.

Once these internal constraints are satisfied, the length of the insulating cylinder must be large enough to prevent flashover on the exterior of the insulator between the external connections to the anode and CG. The required cylinder length will therefore depend on the external medium. We generally assume that tubes will be held in an electrically insulating liquid that also provides cooling, similar to the practice for medical X-ray tubes [3]. Gas tube test devices can be conveniently developed and tested in air up to the voltage limit of air flashover, after which the complication of external fluid insulation must be introduced.[1]

Two additional considerations should be noted. First, these devices operate "on the left side of Paschen's curve" (see Fig. 15.5), and the so-called long-path gas breakdown along the interior surface of the insulator must be inhibited [9]. This leads to designs where the anode and CG cylinders fit tightly within the cylindrical insulator.

Second, the functions of the various electrodes change during operation. Gas tube HV design considerations apply to the anode, CG, and intervening space, without much regard for the space between the CG and the "true" cathode that emits electron current conduction. The CG functions as the cathode both during HV standoff and during the electrical opening transient.

3.2 Thermionic Cathode Material, Geometry, and Operating Conditions

As is the case for most gaseous electronic devices, there is a trade-off between cathode operating current and calendar life (lifetime at rated current). High-current cathodes generally emit electrons only in response to some physical mechanism

[1] A bushing-like enclosure (as for surge arrester) could be also engineered to avoid liquid dielectric. The final option may depend on the applications (breaker or converter switches). For breakers, it will also depend on the option of dead tank (which allows metallic support close to ground) versus live tank (which requires insulating support that needs to be sized based on the system voltage). For example, a liquid dielectric enclosure might be suitable for HVDC stations and dead tank breakers, while air-insulated enclosure might be suitable to live-tank breaker applications.

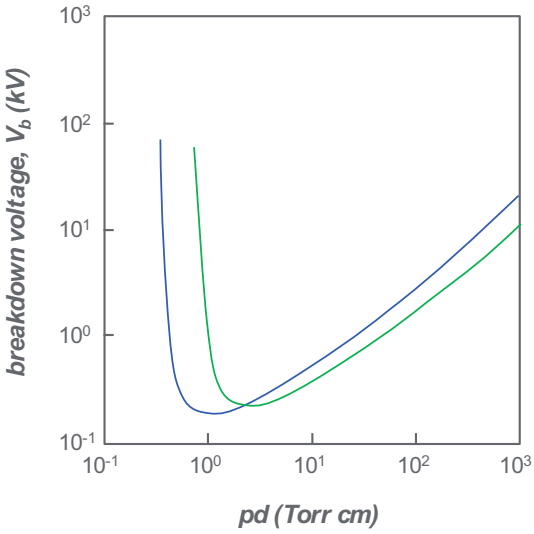

Fig. 15.5 Schematic example of the Paschen breakdown curve showing the voltage required to initiate a plasma between two electrodes as a function of the product of the gas pressure, p, and electrode separation, d. Illustrative examples are shown for two different gas/electrode combinations (green and blue lines), showing that there is a minimum voltage that typically occurs ~1 Torr cm. Below this value (left side of Paschen's curve), initiation is limited by the number of atoms or molecules available for electron impact ionization

(e.g., thermal energy or high-energy incident ions) that also damages the cathode. As an example, for hot cathodes, the elevated surface temperature that provides thermionic electrons for electrical conduction also leads to evaporation and loss of the cathode material.

Both the cathode material and its physical design are important for overall performance. The selection here of LaB_6 as the cathode material [10] and a hollow cathode geometry [11] is based on decades of careful development and life testing of the material for interplanetary spacecraft propulsion [12].

Notably, the conditions in, and constraints on, gas tubes for electric power systems are quite different both from spacecraft applications and from earlier work on pulsed-power gas tubes [13]. Space propulsion systems flow gas into the hollow cathode with a throttled exit to maintain a relatively high working pressure 1–10 Torr (~10^2–10^3 Pa) in the hollow cathode. Gas tubes are stagnant gas systems that must operate at much lower pressure 20–200 mTorr (3–30 Pa) everywhere in the hermetic volume so that the HV region can operate properly on the left side of Paschen's curve.

Oxygen, water, and other similar contaminants are effectively absent in propulsion systems, where they are only introduced by the incoming gas and from very small containing volumes (delivery tubes and the hollow cathode itself). A gas tube has significant internal volume bounded by relatively large surfaces that can be long-term sources of such contaminants.

The flowing gas of a propulsion system carries away gas contaminants, whereas they accumulate in the stagnant gas of a gas tube. Since active pumping is not practical in a gas tube, impurity getters [14] are used to remove contaminants throughout life.

The gas tube presently operates on hydrogen, deuterium, or argon, whereas thrusters operate on xenon, as did earlier pulsed-power gas tubes [13]. Helium has also been used in cold-cathode gas tubes. There is certainly more opportunity for deleterious chemistry with hydrogen or deuterium as the working gas, but even the noble gases are not identically "inert" in a plasma environment.

Since the thruster design and conditions are not identical to gas tube practice, how to make use of the vast knowledge accumulated for thrusters? Our general approach to cathode development for gas tubes is to measure the cathode mass loss rate while operating in a gas tube environment. If the mass loss rate is similar to that found in the thruster literature as a function of electron emission current density, then we assume that we can make use of the thruster life testing experience. If our mass loss rate is higher than found in the thruster literature, then use our judgment to identify the root cause and make changes (e.g., improved part handling or additional impurity getters). To date, this strategy has been successful.

3.3 Control Grid Design for High-Current Conduction and Interruption

The CG is central to the tube operation, in that it is part of the HV design, it influences the tube turn-on and conduction loss, and it sets the maximum current that can be interrupted by the tube. If the current density at the grid exceeds the design limit, the tube will latch on until the current density drops below this level for some other reason. The basic current interruption process at the CG is described in [1].

For best performance, the CG is patterned with a hexagonal array of closely spaced circular apertures (see Fig. 15.6). The open area is maximized to reduce conduction losses, consistent with mechanical integrity. A thicker CG may be needed to account for material loss during switching in order to achieve cycle life (number of interruption events until end of life). Smaller aperture diameter leads to higher interruption current density, but excessively small hole diameter increases losses and can inhibit electrical turn-on. Total current interruption capability can be enhanced by increasing the CG area, within practical physical limits.

The ability of the CG to interrupt a given current density depends on the plasma density at the grid, which in turn is influenced by the cathode electron emission mechanism and the gas properties (mass, ionization potential). It is therefore necessary to relate the plasma density to the current density. This relationship can be estimated analytically for some conditions but more generally requires experimental measurements or a sophisticated plasma model [15].

The CG surface that faces the anode must be mechanically and chemically polished to remove microscopic asperities where the electric field can concentrate, leading to spurious electron field emission and HV instability or failure. The body of HV experience [16] has shown that molybdenum is the best cathodic material for

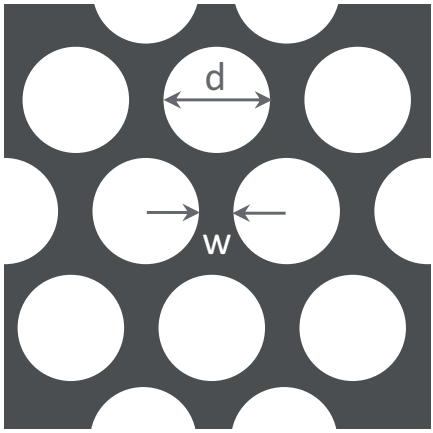

Fig. 15.6 Hexagonal grid design with aperture diameter, d, and edge-to-edge spacing, w, separating adjacent holes. For this design, the optical transparency is given by $T_g = \frac{\pi}{2\sqrt{3}}\left(\frac{d}{d+w}\right)^2$

HV performance, in that it can withstand the highest electric field on the surface without electron field emission. However, molybdenum is an exceptionally difficult material to fabricate, so stainless steel is used instead for practical considerations and wherever HV performance is not the utmost criterion.

3.4 Gas Pressure Management Throughout Life

Gas tubes should be sealed, self-contained devices (without active pumping or external gas supply) for practical implementation in the electrical power grid. The relatively low pressure of internal gas needs to be maintained against small internal sources and sinks that can accumulate over life. Hydrogen and deuterium can be conveniently supplied and removed by using a resistance heater to control the temperature of a metal hydride reservoir [6]. We have demonstrated that rare gases can be similarly controlled by a temperature-controlled "sorb" of activated carbon at temperatures that can be achieved with a conventional thermoelectric cooler [17, 18].

In either case, a carbon sorb of volume $\ll$1 l, with a simple thermoelectric cooler and/or resistance heater, is expected to be able to manage the gas pressure within a gas tube over its operating life. The internal pressure can be determined directly from a sensing unit or inferred from the electrical characteristics of the tube.

4 Example Benefits of Gas Tubes in Electric Power Systems

The common thread of all the applications that are mentioned in this chapter is that the gas tube is just another switching device, albeit a fast one with a voltage rating far above the typical 3-10 kV value of power semiconductors. The gas tube has a particular combination of properties and idiosyncrasies, just like thyristors, IGBTs, and IGCTs. Any application that is limited by the voltage rating of the power semiconductors or that requires series connection of power semiconductors to achieve the needed voltage is a potential candidate for the gas tube. Furthermore, the possibility of a fast (<5 μs), compact, high-temperature switch with high-voltage capability ≫20 kV could pave the way to new power system designs including a DC circuit breaker where extremely fast response time can benefit the design of the entire DC line. Indeed, unlike in AC applications where the breaker is designed to operate after the peak current, in DC system, the response time of the breaker will directly affect the maximum short-circuit current. Faster DC breakers will allow smaller fault currents and therefore reduce the short-circuit withstand requirements and the maximum current rating of the entire system.

A limited number of systems have been analyzed in depth to estimate the performance and possible advantage of gas tubes as switching devices. AC-DC converters have received the most attention, particularly very high-voltage and high-power converters used on HVDC electric transmission systems. Fast, compact DC circuit breakers have also been analyzed in some depth. These two applications will be discussed in detail. Other applications like DC-DC converters, components of flexible AC transmission systems (FACTS), have also been considered. Further information can be found in the literature [19, 20].

4.1 Converter Stations

HVDC converters, where electric power is converted between AC and DC, were the initial impetus to evaluate gas tube technology for grid applications. Power system engineers can view a plot like Fig. 15.2 and quickly recognize the potential for cost savings through the use of HV devices. The underlying technology is irrelevant at this point, so long as the promised device performance, life, and cost can be achieved.

Conceptual system designs based on HV gas tubes have been developed and compared with a reference concept system based on power semiconductors (Table 15.1). Initial work was done for the well-established LCC (line-commutated converter) design that is used to transport bulk power unidirectionally over long distances. Gas tube-based LCC converters were estimated to be about half the cost of power semiconductor-based converters, thereby reducing the crossover distance (line length beyond which a DC system with two converters is cheaper than an AC line). Based on the estimated cost of a gas tube switch and its scaling with both

Table 15.1 Estimate of HVDC converter cost savings enabled by gas tube technology for strong grid and black start applications, assuming six tubes in parallel (5 + 1 for redundancy)

Parameter	Strong grid thyristor	Gas switch	Black start thyristor	Gas switch
Assumed switch operating voltage (kV)	7.2	300	7.2	300
Assumed switch conduction current (A)	3000	600	3000	600
Valve details	90 in series	5 + 1 parallel	90 in series	5 + 1 parallel
Switches per station	>2000	144	>2000	288
Estimated gas switch cost ($/kVA)	–	0.22	–	0.19
Energy losses (%)	0.7	0.7	0.7	0.7
Capitalized loss cost ($M)	110	110	110	110
Valve cost ($M)	50	25	50	35
Station equipment ($M)	235	150	360	160
Turnkey cost ($M)	335	210	460	230
Total cost ($M)	445	320	570	340

The forward voltage drop for the gas switch was assumed to be 200 V, a low value for a cold-cathode device, but significantly higher than a switch with a thermionic cathode. The total system savings was estimated to be 28% for strong grid and 40% for black start applications

voltage and current, the cost of an HVDC station is lower when using a smaller number of more costly gas tubes (288 per station) than a larger number of cheaper series-connected thyristors (>2000 per station).

An even more important part of the cost savings is that there is no need for expensive ancillary equipment around each thyristor to ensure voltage-sharing along a series-connected stack of thyristors. Such voltage-sharing must be effective both during the relatively slow line-frequency waveform and during high-voltage switching transients that are imposed on one device as other devices in the system open and close.

LCC systems do not take full advantage of gas tube functionality, because they require only semi-controllable devices like thyristors. Semi-controllable devices can close on command but cannot open against current and only open when the AC current next crosses zero. In some sense, one is therefore paying for the functionality of a fully controllable device but not using it. (Note that a cheaper semi-controllable gas tube system could be made by eliminating the high-current opening circuitry.) Subsequent work was therefore done to evaluate VSC (voltage-source control) designs capable of greater functionality, including “black start” capability, where

a converter can initiate the production of 50/60 Hz AC power when there is no AC signal on the AC side of the converter.

4.2 In-Line Circuit Breakers

Two implementations of circuit breakers (CBs) for DC power grid have been considered in some detail: (i) a *hybrid* CB where a gas tube conducts current only briefly during CB opening and (ii) an *in-line* CB where the gas tube conducts current continuously during normal operation. In both cases, the system voltages of interest are relatively high, certainly >20 kV, compared with levels where traditional power semiconductors are typically satisfactory (<5 kV).

For CB in grid applications, power efficiency is particularly important considering that the breaker can remain closed continuously through its service life except during maintenance or faults. Efficiency is the power loss at full load in the CB relative to the rated power. In DC, it is also the voltage drop across the CB relative to the system voltage, which is the language we will use here. Losses should certainly be <1%, more likely <0.1% and preferably <0.03% [21], because the losses occur during normal system operation and can aggregate to a large amount of energy during CB service life. There are very few active switching devices that have sufficiently low forward volt drop to be placed in the normal current path.

4.3 Hybrid Circuit Breakers

Various hybrid CB designs are used to minimize system losses [22–24]. We note that CIGRE TB683 [22] is focused on HV, but the same hybrid principles apply to medium voltage. As described in earlier chapters, in hybrid systems, the normal current flows through a relatively low-voltage commutation switch and a mechanical switch. The mechanical switch is slow but has negligible V_{fwd}, and the commutation switch has relatively low V_{fwd}. Indeed, because the commutation switch must only withstand a fraction of the full-system voltage V_{sys} during the current interruption process, it does not require to be built with a large number of power devices; therefore, it has a low V_{fwd}. When the CB should open, the commutation switch provides enough back voltage to force the current into a parallel commutation path. The commutation path has a fast-opening switch that can withstand not only V_{sys} but also the transient overvoltage that will arise when the current is reduced in a circuit with system inductance. This switch can have high V_{fwd} because it carries current for only a fraction of a second during CB operation and does not cause losses during normal operation. The line current is carried through this conduction path for several milliseconds, while the mechanical switch in the normal current path is opened, at which point the fast-opening switch turns off to stop current flow.

With both paths open, the current is then diverted to a third parallel path that consists of surge arrestors to dissipate the stored energy $1/2LI^2$ in the system inductance.

Power semiconductors are used in prototype and fielded mechanical and power-electronic (MPE) HVDC CBs that have been shown to date, both for the commutation switch in the normal current path and the opening switch in the commutation path [22]. These CBs are physically large because of the need to air-cool the solid-state devices and to provide air electrical insulation of the commutation path opening switch, which must withstand the maximum transient voltage. The CB must be housed in a climate-controlled room with filtered air, either in the HVDC converter valve hall or in its own facility. Such climate-controlled space is expensive, and adding it to an existing installation may be problematic if space is constrained.

Cold-cathode gas tubes have been proposed to replace the opening switch, recognizing that they have unacceptably large V_{fwd} for use in the normal current path, but they can close and then open quickly during CB operation, and that they can withstand large transient voltage. Cold-cathode gas tubes do not require heating power to maintain the temperature of a hot cathode. They are also able to operate at high temperature and can be fluid-insulated, leading to a very compact design. It has been proposed to house a gas tube-based DC CB inside an ordinary shipping container in a substation, thereby avoiding the need for a large, climate-controlled enclosure [25].

5 Operational Considerations for Gas Tubes in Electrical Power Systems

We will make two assumptions in this section to discuss possible applications and benefits of gas tubes in large electric power systems. The first assumption is that gas tubes can become as mature and proven as power semiconductors, which are marvels of consistent, reliable performance. The second assumption is that so long as electrical insulation is sufficient, higher operating voltage is always desirable to reduce conductor mass, volume, and power loss. If the operating voltage exceeds the rating of individual power semiconductors, then there is some rationale to investigate the potential benefits of gas tubes.

5.1 Voltage Considerations

Some large electrical systems like HVDC converters already operate at sufficiently high voltage for various reasons, where gas tubes might have significant economic benefit. For this application, it is necessary to mature gas tube technology and

transition from the experience base with power semiconductors to the new world of gas tubes.

Other large electrical systems like airborne and shipboard power systems operate at relatively low voltages and high currents that are well within the capabilities of power semiconductors. However, conductor size and weight are important for ships and defining for electric aircraft, so why not operate at higher voltage and lower current? The answer seems to be that such systems operate at the highest practical voltage allowed by the *insulation* (by which we mean the insulating materials and structures of all components in the power system) and thermal management.

Insulation in this broad sense is an enabling technology for electric flight and future warships, and it permeates the internal design of every component from generator through load. It is difficult to determine to what extent system voltages are selected for best overall performance, versus being accepted because insulation limits have been reached [26]. A fresh system design is needed that is free of inherent assumptions about insulation performance.

5.2 Interruption Time Considerations

Gas tubes open and close very quickly, transitioning in a few microseconds. Fast transitions reduce switching energy and enable high-frequency modulator operation; 200 kHz has been demonstrated [1]. Fast switch-on and switch-off times are a feature of gas tubes, as described above. It is therefore possible to use pulse-width modulation in AC-DC converters for 50/60 Hz power systems.

For comparison, fast mechanical switches for high-power systems have operating times of several milliseconds, and even some power semiconductors have relatively slow ~millisecond deionization times when designed to meet other performance criteria.

For circuit-breaking applications, it would seem that faster opening is better, to limit the fault current that the system components must be able to briefly withstand. In fact, there is a trade-off because fast opening leads to high transient voltages because of the system inductance. For physically large HVDC systems with correspondingly large inductance, the current is expected to double in a millisecond, and a circuit breaker opening time of several milliseconds is thought to be a good compromise [27]. Somewhat longer operating times are used in field applications [23, 24]. As is the case for insulation, it is difficult to know whether these operating times are truly the best choice or whether they are simply accepted as the fastest that that can be done. Shipboard power systems are physically compact, the system inductance is lower, and the rate of current rise is very fast. AC CBs cannot operate faster than the time to the next current-zero crossing, but faster CB operation may be desirable for DC systems.

It is generally difficult to make general statements about DC power systems, because they are much more tightly coupled than AC systems. A comprehensive

DC system analysis is required to determine the best fault control strategy and then specify the requirements for individual components, including the CBs [23, 24].

5.3 Compact Installations

Compact equipment size is important for many applications, examples being switchgear on ships and HVDC converters on platforms for offshore wind. Even land-based power system applications have space constraints, particularly if the space must be climate-controlled, or the equipment is located in a congested urban area.

Fluid insulation leads to much smaller installed size than air insulation. Both gas tubes and power semiconductors can in principle use either insulating medium [28], so it becomes a design choice. Nonetheless, air insulation dominates for power semiconductors, in part because of the large number of devices for a given voltage and the need to occasionally replace failed devices. Gas tubes will likely be packaged in a manner similar to large medical X-ray tubes, in a fluid-filled jacket for both electrical insulation and thermal management [3]. Figure 15.7 shows examples of a water-cooled, air-insulated, thyristor GEC Alsthom converter and an English Electric prototype oil-insulated, oil-cooled thyristor valve.

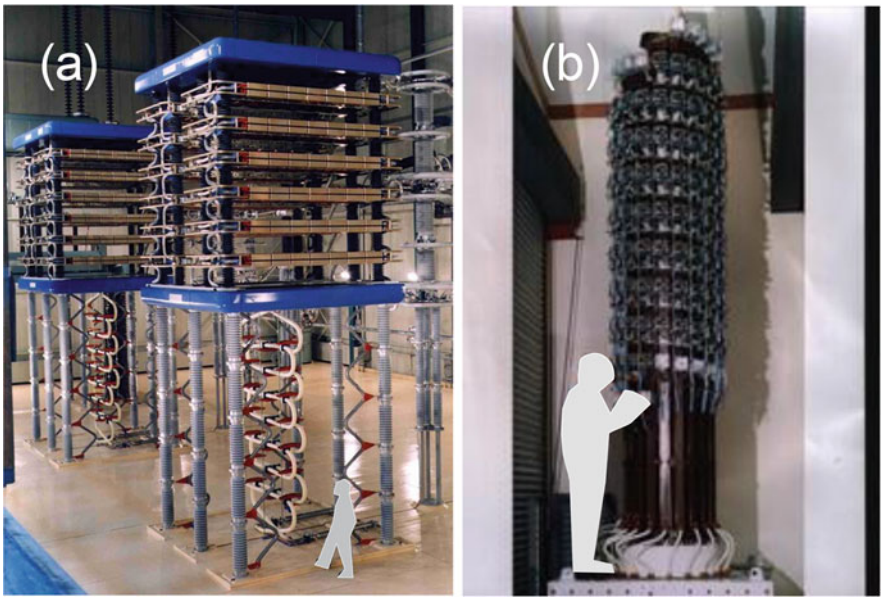

Fig. 15.7 Comparison of (**a**) a water-cooled, air-insulated, thyristor converter for valve group 13 of the Nelson River Bipole 1 HVDC transmission project in Canada (c. 1994) and (**b**) a prototype oil-insulated, oil-cooled thyristor valve (c. 1970)

Gas tubes can operate at high temperature, at least several hundred degrees Celsius, and are therefore amenable to compact, high-power-density packaging. The temperature limit is set by the braze materials that are used to hermetically join ceramic and metal components. Operating temperatures of 300–400 °C are widely practiced for X-ray tubes [3], and very high-temperature operation (800 °C) is possible with proper selection of materials and processes [29].

6 Recommendations for Development of Gas Tubes and Their Applications

This section summarizes key work that must be performed in development of gas tube technology. It also notes where opportunities must be identified for improved system performance with gas tubes and to better define gas tube development goals.

6.1 High-Current Cathode

Low-loss, long-life hollow cathodes have been demonstrated to hundreds of amperes to meet the expected needs of planned spacecraft [15, 30]. There is no fundamental reason why they cannot be scaled to thousands of amperes, although certainly much good engineering and development will be required [31]. The biggest impediment to the development of hollow cathodes 1–10 kA is the requirement for thousands of hours of life testing of a high-power device, perhaps tens of thousands of hours. To date, gas tube development has benefitted from the extensive work to develop hollow cathodes for spacecraft propulsion. There is at present no application, other than gas tubes, to justify the work required to develop high-current hollow cathodes. A coordinated program to develop high-current cathode beyond the 500 A that has already been demonstrated [31] would benefit gas tubes and other electric discharge devices.

6.2 High-Voltage, High-Power Test Facilities

The high-voltage performance advantages of gas tubes can also make development more difficult and costly, because of the need to perform tests at full voltage. A staged approach is therefore needed, analogous to what is done for power semiconductor-based systems, where most development and testing are performed on individual, lower-voltage modules, and series-connect modules are tested only at key development milestones. Similarly, gas tube conduction and switching performance can be validly tested at lower voltage, and full-voltage switching is

performed only at key milestones. If a gas tube can close with ~2 kV across the terminals, then it can close at HV, and if it can open against current to reach ~2 kV across the terminals, then it can open against current to HV. However, sustained full-voltage, full-power testing is required to validate key development milestones.

6.3 Basic Data on High-Voltage Breakdown of Low-Pressure Gases

Data for electrical breakdown of gases at low gas pressure is sparse above 100 kV [32]. Such data is needed for HV gas tube design up to the maximum transient voltage. Gas electrical breakdown is a function of total voltage, not electric field, so it is not possible to perform "scaled" experiments where the desired electric field is tested over a shorter electrode separation. Experimental testing must be conducted with test equipment that prevents "long-path" breakdown; one example approach is the gas tube itself, where reentrant electrodes are tightly fit into a concentric insulating housing. Computational models have been used successfully [33]; they can be quantitatively accurate at higher voltages because the high-energy collision and impact phenomena are often simpler and better known than the low- and intermediate-energy processes.

6.4 A Quantitative Relationship Between Conduction Current Density and CG Plasma Density

The plasma density at the CG, along with the CG design and area, determines the maximum current that a gas tube can interrupt. It is therefore critical to relate the plasma density at the CG to the conduction current, for proper tube design. This relationship can be estimated for steady-state conditions with reasonable certainty from both experimental Langmuir probe measurements and reported plasma models [15, 30]. However, it is most critical to know this relationship during transient fault conditions, when the hollow cathode temperature will not rise quickly enough so that its operation can be described as a sequence of steady-state snapshots. More sophisticated models are needed to describe such transients. One potential beneficial outcome of such work is that means might be found to reduce the CG plasma density for a given current density (e.g., by modifying the hollow cathode exit geometry), thereby improving the overall capability of gas tube technology to interrupt current.

6.5 Gas Tube Implementation in Systems

Several general system requirements can be noted. Parallel-connected tubes will require current-sharing circuitry; such methods were also needed for mercury-arc valves, so those approaches can be updated [34]. Power electronic controls for the gate drive are substantial and may be located at high electric potential; power must then be tapped locally or delivered through some non-galvanic connection like an isolation transformer, compressed air, laser, etc.

To simplify and minimize the cost of protection circuitry for parallel-connected devices, gas tubes should consistently fail open circuit. Gas tubes do block voltage bidirectionally and will be rated for the maximum transient overvoltage, so fail open is natural for some failure modes such as cathode degradation. One important concern is loss of hermiticity and/or rise of internal gas density to the point where the tube is no longer "on the left side of Paschens curve".

Internal gas tube gas pressure 20–200 mTorr (3–30 Pa) must be regulated and maintained throughout life. Gas supplies and pumps are impractical, so "reservoirs" are used: devices that can emit and absorb the gas tube working gas from a gas sponge or sorb based on an electrical signal. Hydrogen and deuterium reservoirs are available, and a helium reservoir based on an activated carbon sorb has been demonstrated [17, 18]. Other noble gases have been proposed and tested for various reasons in gas tubes, notably, the use of argon and xenon to reduce V_{fwd}. Activated carbon is also expected to work for heavier rare gases like xenon, but the operating temperature is expected to be well above ambient temperature, requiring only a simple resistance heater. The use of any noble gas will require more or less development of reservoir technology, depending on the exact gas choice.

7 Fault Control for Future Large DC Power Systems

Two important ways in which large DC power systems differ from large AC power systems are their relative *technical maturity* and the *degree of coupling* between various components. By technical maturity, we mean that there are AC standards and experience that allow a catalogue of CBs to be offered and then selected to meet the requirements of a specific application. By degree of coupling, we mean that the stress on an AC breaker during a fault is relatively predictable without the need to know the details of the breaker itself, and vice-versa.

Part of the reason for the low degree of coupling for AC systems is that the breaker operating time is relatively slow, since current can only be interrupted at current zero. AC CB operating time is therefore one to two cycles after a fault detection time of 0.5–1.0 cycle (where each cycle corresponds to 20.0 and 16.7 ms for 50 and 60 Hz systems, respectively). Contrast this relatively long time with hybrid HVDC breaker prototypes that open in ~3 ms [25, 27]. Ongoing development work on for MVDC systems has targeted even faster operating times <0.5 ms [21]

to address the very fast rate of current rise in physically small systems with low characteristic inductance.

Despite these differences, there has been little effort to understand the benefits and challenges of very fast CB operation in DC systems. A gas tube opens instantly (<5 μs) in practical terms relative to even the interval between current readings (say, 25 μs) and the need to confirm a fault over several readings (say, 150 μs). Given such design freedom, what is the proper balance between faster opening (large transient voltage) and slower opening (higher current, longer duration)? Could a fast-operating breaker with high voltage and thermal withstand capabilities allow fast repetitive reclosing to verify clearing of the line fault and therefore provide stability benefits to the power system? How much cost savings could be realized by a fast DC CB reducing the maximum fault current to which the system is exposed? Such questions can only be answered by assessing example DC systems with high fidelity modeling and simulations and these possibilities in mind.

8 Concluding Remarks

We have provided an overview on the potential benefits of gas discharge tubes as an enabling technology for medium- and high-voltage direct current power systems. High-voltage, high-power gas tubes are a recent development in a long line of proven gaseous electronic devices for large power systems that includes thyratrons and mercury-arc rectifiers and valves.

The gas tube is naturally a higher-voltage, lower-current device with very attractive electrical opening and closing times (<5 μs), overvoltage capabilities, compactness, and applicability to high-temperature installations. Present representative voltage and current values are 50–300 kV and <500 A, with increases to be expected if they are developed toward specific goals.

It is therefore natural to seek applications that require high voltage, where long strings of series-connected power semiconductors would ordinarily be needed, and lower current, within the capability of established hot (thermionic) cathode technology. One example of such an application is an HVDC *tap*, where a small fraction (say, 10%) of the power on a point-to-point HVDC line is diverted onto the AC grid at some intermediate location. Taps can help overcome the public resistance to new HVDC lines by those living along the line, who currently see no local power benefit. In a tap, the full HVDC voltage must be handled (say, 320 kV), but the current might be ~300 A rather than ~3000 A. The cost of a tap converter based on power semiconductors does not scale down very well with current, such that it is not substantially lower than the cost of a full-power converter station. Conversely, 300 A is within the range of what has already been demonstrated in aspects of gas tube development.

Gas tubes also appear to meet many of the requirements for use as in-line MVDC breakers, including efficiency, operating speed, power density, calendar life, and cycle life. More development is needed to show capability for steady-state operation

at thousands of amperes and to open against fault currents of 10–100 kA. System analyses are needed to quantify the benefits of a fast, compact in-line MVDC breaker in future MVDC power systems, to motivate further development of gas tubes for this application.

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Chapter 16
Converter-Based Breakerless DC Fault Protection

Hui Helen Li, Ren Xie, and Robert M. Cuzner

1 Introduction

Breaker-based protection provides an effective solution to improve system reliability. The prospects of market drivers for HVdc and MVdc breaker-based protection are different. There are commercially available solutions for HVdc applications [1, 2], driven by existing HVdc transmission worldwide, and the emerging need for multiterminal HVdc networks. Solutions for MVdc breaker-based protection are presently neither commercially viable nor commercially available due to limited applications. Still, there is an increasing need for MVdc distribution systems, and fault protection will be a paramount concern. The MVdc SSCB is still under development and faces many technical challenges [3]. The primary challenge for MVdc breaker-based protection is the need to deliver continuous-rated power in the multi-MW range. For MVdc systems, this results in a simultaneous need for power semiconductors with *both* voltage and current ratings beyond what is available in commercially available devices. Similar to the HVdc application, a number of power semiconductors in series are required to safely block voltage; however, it is also common for the multi-MW, MVdc system to require continuous current rating of >1 kA at points of feed and connection. During short-circuit

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faults, breaker-based protection will require current well in excess of the continuous current rating during fault clearance operations, which either limits the power semiconductors that can be utilized or necessitates *both* series and parallel device connections. This requirement, when combined with size/weight/cost constraints in many applications, presents challenges and risks for breaker-based protection.

Breakerless protection provides an alternative protection solution to breaker-based protection in dc systems [4–16]. This method utilizes voltage foldback capabilities in upstream generation, coordination with ac-side breakers or the inherent current-limiting capability of at least one dc bus forming power electronic converter (PEC), and its controls, to actively engage in the fault clearance and post-fault recovery. Breakerless protection is well suited for systems having redundant feeds to bus-tie connections, multiterminal networks, and systems with dual-fed critical loads or critical load buses. Considering the added cost and size/weight concerns of both the HCB and SSCB and loss concerns of the SSCB, as well as technical challenges that HCBs and SSCBs present, a breakerless approach does not rely upon MVdc breakers and will result in lower system cost, higher power density, and lower implementation risks.

The MVdc shipboard Integrated Power and Energy System (IPES) presents a very good application use case for demonstration of breakerless protection due to the abovementioned advantages [4–9, 11, 13–16]. The MVdc shipboard power system is driven by the need for the IPES particularly in naval ships. The IPES is an MVdc power and energy delivery network that effectively addresses the high ratio of connected load power to installed generation and enables optimization of stored energy installation location, usage, and control to ensure operability over a wide range of mission scenarios. The IPES has emerged from the combination of integrated medium-voltage power for electric and hybrid electric propulsion with low-voltage mission and ship service loads in the ship and the increasing insertion of high-energy electronic weaponry into naval ship platforms. Survivability and, ultimately, resilience of these ships are critical, and the dependability of the protective system approach is a key consideration for any IPES application or candidate IPES architecture. Lessons learned from breakerless protection in shipboard systems will be extensible to a wide range of emerging MVdc applications as they become more prevalent over time.

Figure 16.1 shows a breakerless electric ship MVdc architecture where the zones of protection concept is adopted to isolate the faulted zone and reconfigure the electric architecture during survivability events. Each zone may include the following:

- Power generation module (PGM), containing engine generator and ac-dc PECs that convert MVac input to inter-zonal MVdc bus voltage or bulk energy storage plus dc-dc power conversion module (PCM) for battery energy storage (BES) to MVdc conversion
- Power distribution module (PDM), which contains no load switches (NLSws) for dc connection/disconnection and fault isolation

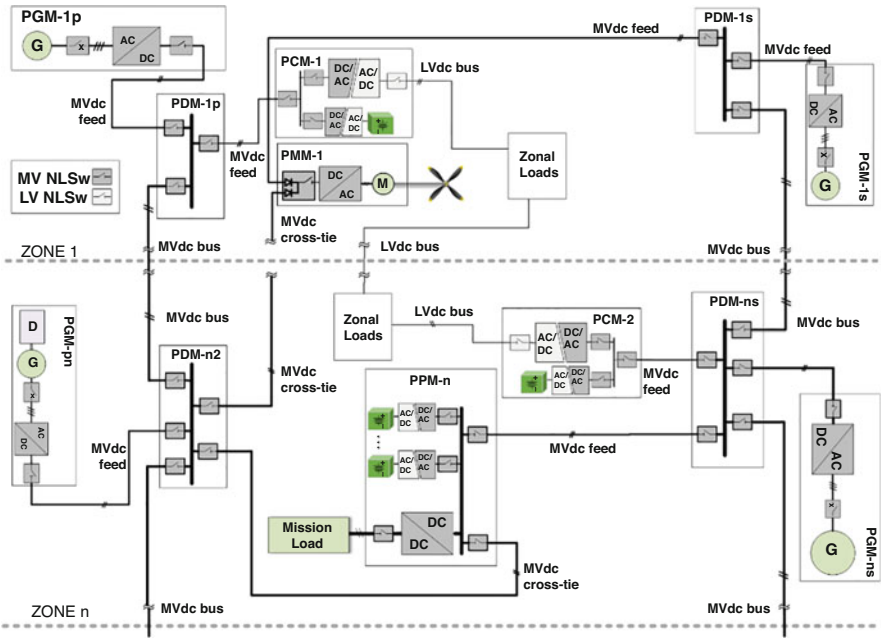

Fig. 16.1 Electric ship MVdc architecture with breakerless protection

- MVdc to LVdc PCM, comprising solid-state transformers (SSTs) for LVdc bus inter-zonal connections and BES for fault recoverability and NLSws
- Direct MVdc-connected loads such as the propulsion motor module (PMM) for interface to propulsion or the pulse power module (PPM), which services medium-voltage mission loads associated with electronic warfare

Other PCMs that convert inter-zonal LVdc bus power to ship service LVdc or LVac distribution system loads are contained with the zonal loads.

In the breakerless shipboard power system of Fig. 16.1, there are two types of PECs connected to MVdc bus, e.g., ac-dc rectifiers in PGM and SST dc-dc converters in PCM shown in Fig. 16.2. Breakerless protection takes advantage of the inherent dc-side current-limiting capability within these PECs, in coordination with NLSws in the PDMs distributed zonally and in the LVdc zones, executing fault detection isolation and recovery, in order to detect and isolate low-impedance faults on shared MVdc and LVdc buses.

The MVdc-interfacing converters must be capable of controlling or blocking current flow into the MVdc bus during low-impedance fault incidence. For an MVdc-interfacing ac-dc rectifier, the desired voltage and current waveforms during a line-to-line (LL) fault is shown in Fig. 16.3. When a short-circuit fault happens on the MVdc bus, the bus voltage drops, and fault current surges, the converter enters current-limiting operation mode to suppress the current peak and can maintain the fault current at a desired value to facilitate the fault point localization. It should

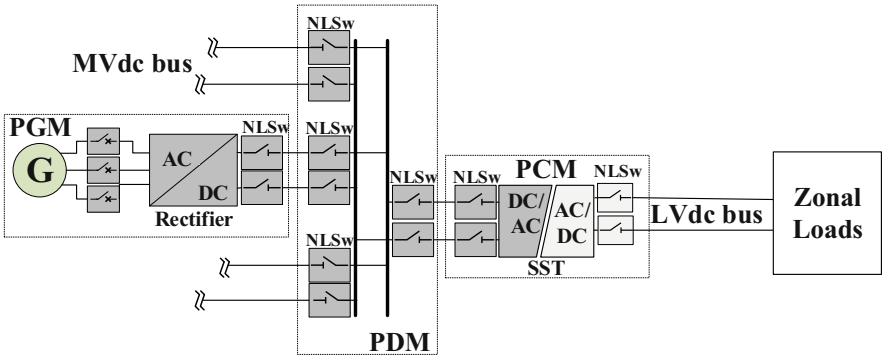

Fig. 16.2 MVdc-interfacing converters in a breakerless shipboard power system

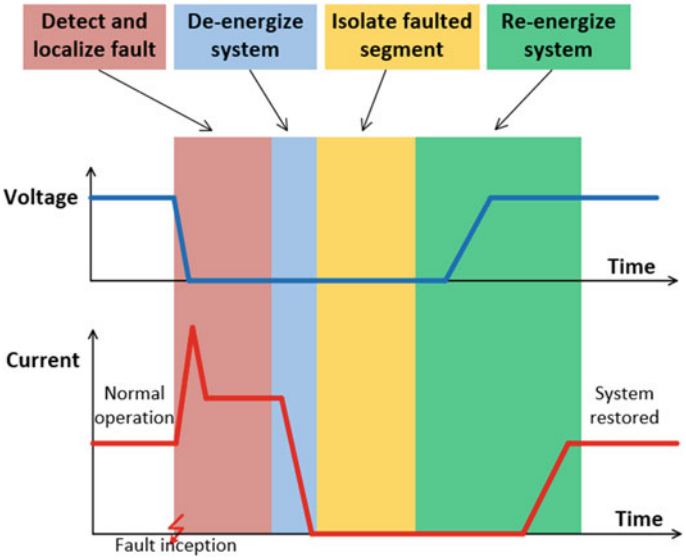

Fig. 16.3 The desired waveforms of a PGM ac-dc converter during an LL fault [13]

be noted that the initial current surge fed from the bus capacitors is beyond the control of the converter and thus minimized MVdc bus capacitors are preferred. After the faulted sections are identified, the PGM ac-dc rectifier must drive the current down to zero and actively de-energize the whole MVdc bus that it is feeding. The corresponding NLSws can then be activated to physically isolate the faulted section of the MVdc from the remaining healthy system.

It should be noted that critical loads downstream of the faulted bus must be sustained during the time it takes to locate the faulted section, de-energize the faulted bus, open the required NLSws to isolate the faulted sections of the bus, and then re-energize healthy sections of the bus. Downstream load sustainment is accomplished

either through local BES or cross-feeding of downstream loads through a diode-auctioneering circuit. The LVdc bus shown in Fig. 16.1 is fed by PCMs connected to alternating port (p) and starboard (s) MVdc buses. These p and s buses span longitudinally from bow to stern and are not directly connected to each other. Through diode auctioneering, if either p or s MVdc bus is faulted, critical loads will seamlessly shift to the healthy bus. What this means is that the healthy bus may be subject to a temporary overload during faulted bus downtime. Resilient system design will ensure that overload conditions are removed when power sourcing rebalances following bus re-energization. If the remaining healthy system cannot support the resultant loading following restoration, then loads are shed, according to predetermined criticality levels, in order to ensure post-fault recoverability. The system of Fig. 16.1 shows a single LVdc bus, although alternative architectures may also contain p and s LVdc longitudinal inter-zonal buses. The downstream LVdc and LV bus critical loads will depend upon distributed energy storage for bus holdup during fault events. Controllable distributed BES systems (BESSs) can be installed at points of LV system feed (i.e., the PCM-1s shown in Fig. 16.1) or close to critical loads within the LV distribution system.

Unlike breaker-based approaches which allow for the entire range of converter circuit topologies, only some specific circuit topologies can apply to the PGM converter in an MVdc breakerless system. Figure 16.4 shows the issues if a conventional voltage-source converter is adopted as the PGM rectifier. This converter type is not suitable for breakerless protection.

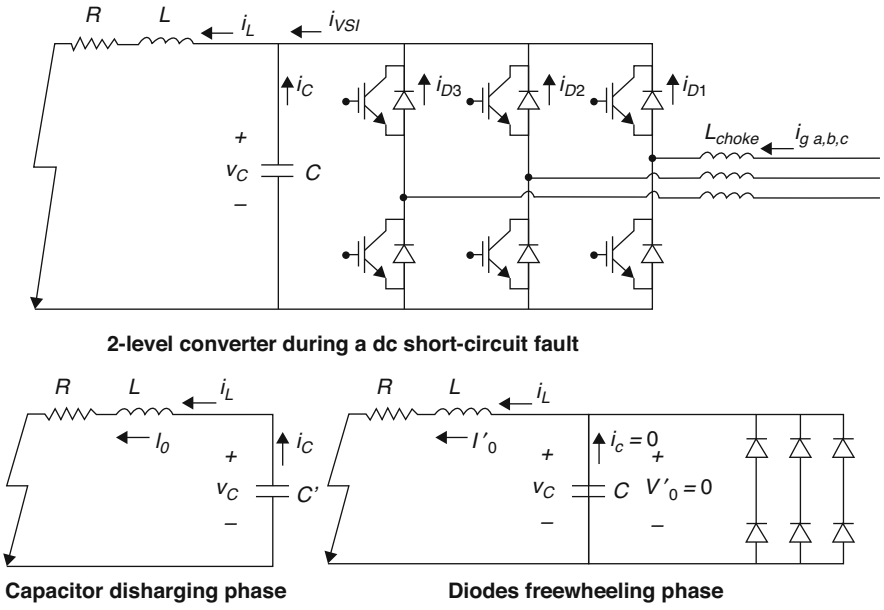

Fig. 16.4 Issues of a conventional rectifier in a breakerless MVdc power system [17]

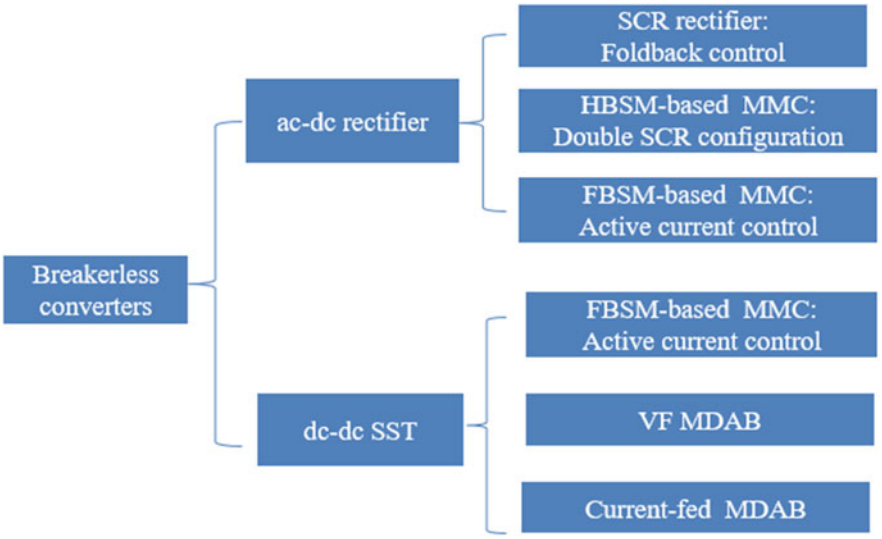

Fig. 16.5 Classification of reported converters that can be applied in a breakerless MVdc power system

When the LL fault happens, the converter shuts down immediately, and the dc-link capacitor discharges to feed the fault. Once the capacitor voltage decreases to zero, all diodes of the converter are forward biased to conduct freewheeling current through the fault path inductor *L*. The current initially is close to the peak resonance current and then decays naturally to zero. After the energy stored in *L* is dissipated completely, the diodes may continue to conduct if ac-side source feeds the dc-side short-circuit fault. Thus, this topology cannot block the fault, and the diodes will suffer high thermal stresses [17]. Some breakerless approaches are based on de-excitation of upstream generator (if there is a single feed to the ac-dc rectifier) to limit current from MVac side [14] or rely upon MVac-side circuit breakers to interrupt fault current. If these approaches are taken, then the ac-dc rectifier power semiconductors must be sized to handle the fault current under the worst-case LL MVdc-side fault condition. Such approaches inevitably lead to significant overdesign of the ac-dc rectifier and therefore will not be considered in this chapter.

Various approaches to utilizing the current-limiting capability of PEC have been reported [8–13, 16, 18, 19]. Figure 16.5 shows how the classification of current-limiting PEC types break down for the ac-dc rectifier and SST. Considering first the ac-dc rectifier, according to the literature, the most common current-limiting PEC types are thyristor rectifier and full-bridge submodule (FBSM)-based modular multilevel converter (MMC) with active dc-side current-limiting controls. A thyristor rectifier using foldback control has been proposed as a PGM rectifier in an MVdc breakerless shipboard system because of high-power throughput capacity [8], but significant capacitor discharge into low-impedance faults and the

time it takes to re-energize the MVdc bus after fault isolation present significant challenges to recoverability [15]. Alternatively, the MMC does not have dc terminal capacitor, so direct dc-side capacitor discharge into dc-side faults is avoided. If half-bridge submodules (HBSMs) are used in the MMC, the ac-side source will feed the dc-side fault through the lower diodes of HBSMs. The resulting high thermal stresses still may damage converter diodes. Therefore, the MMC with HBSMs cannot prevent the fault propagation between the ac and dc sides in a breakerless system. The FBSM MMC, on the other hand, has the capability of fully arresting dc fault current, blocking dc terminal capacitance discharge into faults and maintaining full control over dc-side fault current while maintaining full charge of its submodule dc capacitors. These capabilities of the FBSM-based MMC yield significant advantages when it comes to fault recoverability in breakerless approaches to protection [20–22]. Furthermore, the FBSM-based MMC provides bidirectional current control during both ac and dc short-circuit faults. An MMC consisting of HBSMs but equipped with bidirectional thyristors reported in [18] and a hybrid MMC consisting of both HBSMs and FBSMs reported in [19] are additional topologies that are suitable for the PGM rectifier in the breakerless protection approach. The MMC with a three-level submodule is also proposed in [23] to achieve fault-blocking capability, but the complexity of a three-level submodule compared to FBSM may limit its adoption and will therefore not be discussed in this chapter.

At the points of dc-dc interface, the assumption of transformer isolation between the MVdc system and a downstream LVdc distribution system has been made. A range of non-isolated dc-dc interfaces to MVdc loads could have also been considered, but these apply to specific load-interfacing converters described as the PMM and PPM in the zonal MVdc ship platform of Fig. 16.1. Breakerless protection of point of load converters should be accepted as a matter of fact, and voltage-source converters applied at point of load are buck converters and, therefore, have inherent fault current-limiting capability. The dc output of the SST, which provides isolated dc-dc conversion capability, may be followed by additional cascaded downstream power conversion to provide dynamic and decoupled voltage control to LVdc/LVac loads or distribution systems. Both voltage-source and current-source SSTs, including MMC-based as well dual-active bridge (DAB) approaches, have been considered in the breakerless system application as a means of achieving bidirectional MVdc-side protection at points of load and universally achieving downstream LVdc protection at points of feed [9–12].

The topology and fault control of converters summarized in Fig. 16.5 are presented in Sect. 2 with discussions of merits as well as disadvantages.

2 Converter Topologies and Fault Control for Breakerless Power Systems

This section reviews the most common of the promising converter topologies summarized in Fig. 16.5, which are utilized in dc networks with breakerless

protection. The discussion is limited to MVdc distribution systems and generally based upon the shipboard MVdc system of Fig. 16.1. However, the main points can easily be extended to other types of MVdc and HVdc networks, including terrestrial MT HVdc and MVdc networks. The performance of the converters is explored for the extreme corner case fault of suddenly applied, zero ohm, short-circuit LL fault across the dc bus at the terminals of the converter. Any feasible approach must have the capability of safely handling this fault condition without damage to the converter. Recovery of the dc bus after fault isolation is also compared for the various converter types. Other fault scenarios present less stressful conditions to the converter and are not the focus of this discussion. As long as the extreme corner case capability is in place, breakerless protection capability is easily extended to the handling different rates of fault inception, higher LL fault impedances, and LL fault locations at various locations in a dc network.

2.1 ac-dc Rectifiers

Points of ac-dc conversion and feed to the dc network present the starting point for the discussion of breakerless protection. Any dc network must interface with an ac network, whether it be at points of interface to distributed generation or points of interface to a larger ac grid. The former case is well-illustrated by the PGM rectifiers within a zonal network (Fig. 16.1). The latter case is generally referred to as the voltage-source converter in MT MVdc and HVdc networks.

2.1.1 Thyristor Rectifier Topology with Foldback Control

The thyristor-based rectifier is a good candidate for MVdc high-power application due to the availability of high-current high-voltage rating thyristor devices with high surge current capability. Moreover, the thyristor rectifier can be implemented with a current limit function, namely, the "active foldback." The generator rectifier output can be temporarily turned off by active foldback control to limit the fault current before disconnecting the faulty branch. Therefore, the thyristor rectifier is one way of achieving the fault isolation in a "breakerless" architecture.

A six-pulse thyristor rectifier topology is discussed in [7] and shown in Fig. 16.6. It is composed of six devices and a dc inductor. $\boldsymbol{V_d}$ is the output voltage and the output dc current $\boldsymbol{I_D}$ can be regulated by changing $\boldsymbol{V_d}$. The dc component of $\boldsymbol{V_d}$, $\boldsymbol{V_D}$ is expressed in (16.1).

$$V_{\mathrm{D}} = \frac{3\sqrt{2}}{\pi} E_{\mathrm{LL}} \cos\alpha - \frac{3}{\pi} X_{\mathrm{z}} I_{\mathrm{D}}. \tag{16.1}$$

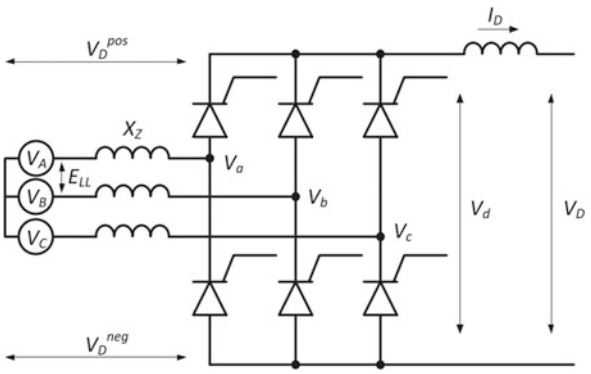

Fig. 16.6 Thyristor rectifier topology [8]

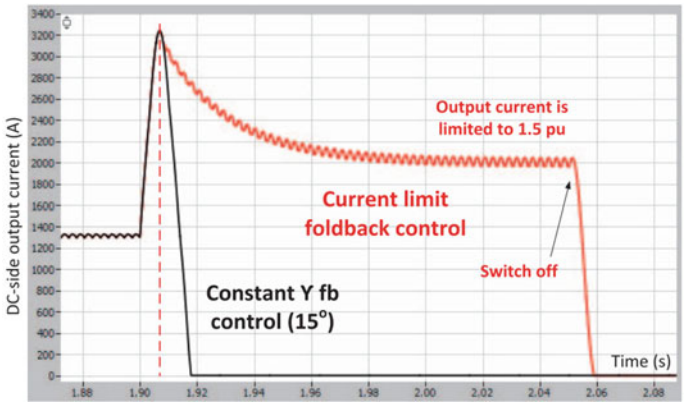

Fig. 16.7 DC fault current with two active foldback control methods [8]

If the firing angle α is between 0° and 90°, the output voltage polarity is positive. The firing angle will be negative when α is between 90° and 180°, capable of effectively lowering the current $\boldsymbol{I_D}$ during short-circuit fault.

As is shown in Fig. 16.7, the dc fault current can be effectively limited by active foldback control. Once the fault occurs at 1.9 s, the dc current rises quickly from 1.3 to 3.2 kA during 8 ms before the thyristor foldback controls activated. Two foldback control methods are demonstrated in Fig. 16.7. The first method directly forces the dc-side short-circuit fault current to zero within 10 ms by regulating the firing angle $\boldsymbol{\alpha}$ between 90° and 180° to provide negative rectifier output voltage, represented by the black line in Fig. 16.7. However, if the fault cannot be localized during the above fault clearing time of up to 18 ms, it will be necessary to hold the fault current at a controlled level in order to provide more time to identify the fault location. This second method is denoted by the red line in Fig. 16.7. Here, the fault current is limited to a manageable but detectable level, e.g., 1.5 per unit, by utilizing *current limit foldback control*. The foldback control structure is displayed in Fig. 16.8, the current limit function is achieved by the inner current

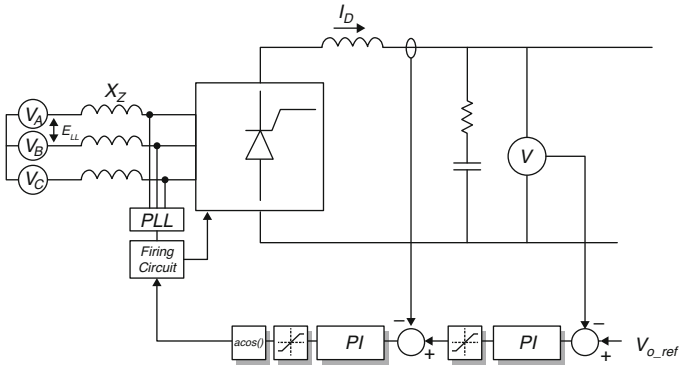

Fig. 16.8 Control structure of current limit foldback strategy [8]

control loop, and the corresponding firing angle $\boldsymbol{\alpha}$ is adjusted around 90° to output a small dc voltage in order to maintain the fault current I_D at a preset value. As fault localization completed after 150 ms, the foldback control drives the current to zero, de-energizing the system to enable isolation of faulted bus segment by NLSws.

In summary, the thyristor rectifier based on foldback control is a cost-efficient solution to breakerless fault protection. However, the utilization of semi-controllable power devices lowers the control bandwidth, and the fault clearing time is as long as tens of milliseconds. Furthermore, the fault current level is quite high and mainly determined by the system inductance instead of by converter controls. As alluded to previously, the total time to restore the bus must also include the time it takes to re-energize the dc bus (following fault isolation) through phase-controlled techniques, taking care to ensure that inrush current into the dc-side RC filter network is kept reasonably low (to avoid reinitiation of the fault protection sequence). For this reason, the total time from fault inception to bus restoration (see Fig. 16.3) is minimally between 0.2 and 1 s. This is due to the large size of capacitance in the RC filter required to stabilize the dc network during normal operation with downstream constant power loads. This time period does not take into account the time it takes for NLSws to isolate the fault.

2.1.2 Double-Thyristor Configured HBSM-Based MMC

The MMC is a promising solution for ac-dc rectifiers in both HVdc and MVdc systems. The application of MMC to HVdc is becoming the standard solution. The tremendous benefit of the HBSM-based MMC is that lower-voltage rated HBSMs can be produced in quantity for a wide range of applications, yielding the economy of scale required for commercial solutions. Each HBSM consists of force commutated devices, most commonly the insulated gate bipolar transistor (IGBT), with the inductance-sensitive connections of these devices constrained

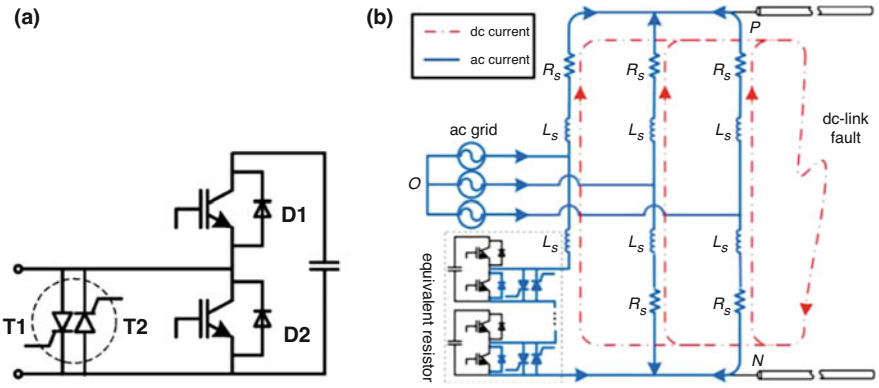

Fig. 16.9 DTC HBSM-based MMC: (**a**) a modified HBSM with double-thyristor configuration to enable FRT and (**b**) DTC HBSM-based MMC containment of dc-side LL short-circuit fault [18]

within the submodule converter layout. As MVdc applications (i.e., with bus dc voltage less than 50 kV) become more common, the HBSM-based MMC will be increasingly applied that are either IGBT-based or integrated gate-commutated thyristor (IGCT)-based. Robust and scalable solutions can be realized through series and series/parallel combinations of HBSMs without the need to carefully manage the interconnection inductance between them.

Unfortunately, as has been pointed out, the HBSM-based MMC cannot clear the dc short-circuit fault due to the freewheeling of lower diode D2 of HBSM, as shown in Fig. 16.9a. However, by adding two antiparalleled thyristors in parallel with D2, the MMC can implement fault ride through (FRT) to achieve breakerless operation at points of PGM interface, through the double-thyristor configured (DTC) HBSM-based MMC shown in Fig. 16.9 [18]. FRT as a means of breakerless fault protection is best described in Fig. 16.3, where, upon dc-side LL fault inception, the dc-side fault current is immediately driven to zero and held there while the appropriate NLSws within the network are opened to isolate the fault, and then healthy parts of the dc bus are restored to full voltage through re-energization at points of feed from the PGM. The speed of FRT is the distinguishing feature between different ac-dc rectifier types in a dc network with breakerless protection.

The DTC HBSM-based MMC ac-dc rectifier is adequate for FRT in MT, zonal, and point-to-point networks where a longer time can be tolerated during response to dc-side LL fault events. However, the bus recovery time is not nearly as long as what will be required in the thyristor rectifier with active foldback controls. The DTC HBSM-based FRT operation principle is illustrated in Fig. 16.9b. Once the fault condition is detected, the three phase legs are actively shortened on the dc side by turning on all thyristors T1 and T2. Therefore, the fault point on the dc side is decoupled from the ac-side fault energy source, the ac-side generator, or grid. As a result, dc-side fault current can decay naturally to zero after three to five time constant of the short-circuit path loop. The fault localization and dc bus de-

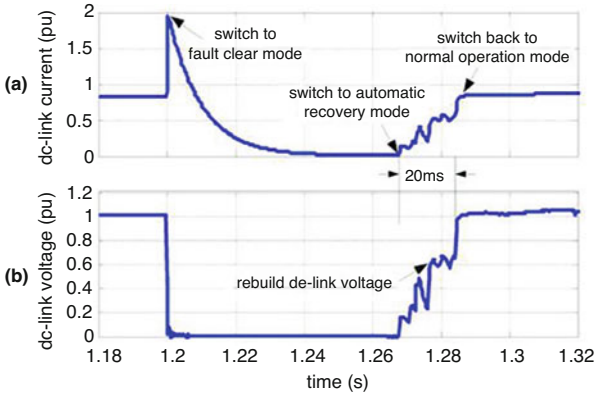

Fig. 16.10 Breakerless fault protection using DTC HBSM-based MMC: (**a**) dc bus current and (**b**) dc bus voltage [18]

energization are expected to be achieved during this period. The ac-side fault will then be cleared within up to one line cycle by blocking gate pulses to thyristors. By intentionally generating a short-circuit path between ac and dc sides, the ac and dc-side fault can be tackled independently.

Figure 16.10 demonstrates the breakerless fault protection including the fault clearance and post-fault recovery. The protection threshold is set to be 2.0 p.u. When dc-link current exceeds 2.0 p.u. at 1.2 s, the protection is activated. Since the diode freewheeling effect is eliminated by switching on all thyristor switches, the overcurrent on the dc link is effectively suppressed, and the dc-link current starts to decay. At 1.266 s, dc-link voltage is restored after fault clearance. At 1.286 s (20 ms after the dc-link fault current is cleared), all IGBTs are unblocked, and MMC is automatically switched back to normal operation.

This FRT strategy is attractive due to its easy and cost-efficient implementation. However, since the fault clearance time extends for multiple line cycles, it may not be suitable for applications sensitive to power continuity or to systems where downstream BESSs cannot be relied upon to support critical loads.

2.1.3 FBSM-Based and Mixed Cell MMC

The FBSM-based MMC will effectively decouple a dc-side LL short-circuit fault from the ac-side grid or generator by inhibiting the gating of the FBSM IGBTs or IGCTs with minimal and controllable FRT times. The bus restoration time is practically negligible when compared to the approaches discussed so far. As a result, the FBSM-based (and mixed cell) MMCs can eliminate the need for diode auctioneering of downstream bus converters and critical loads and may even allow for MVdc ring bus architectures, having similar survivability characteristics to breaker-based architectures. Unfortunately, FBSM-based MMC suffers from high

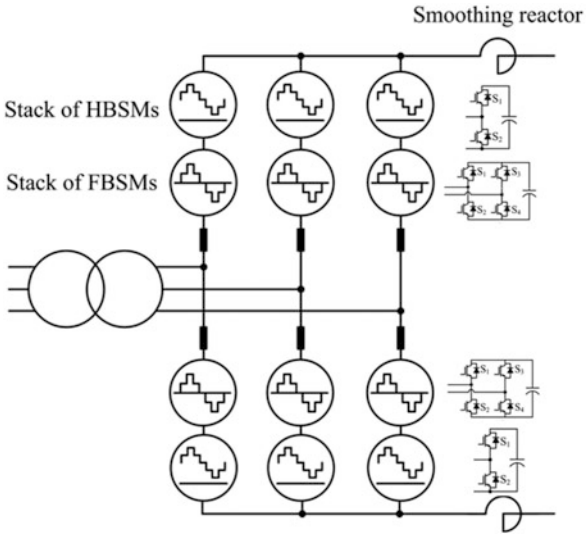

Fig. 16.11 Hybrid MMC composed of HBSMs and FBSMs [19]

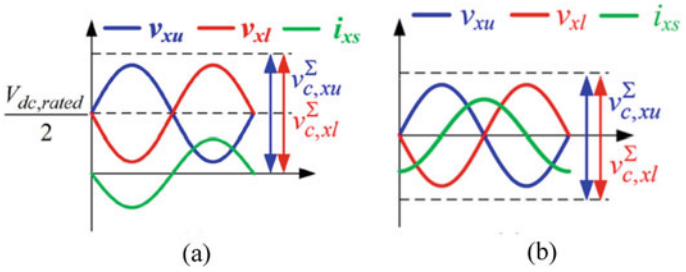

Fig. 16.12 MMC operation principles of (**a**) normal mode and (**b**) DC LL short-circuit FRT [19]

conduction losses and large number of power semiconductor devices, which have discouraged its application.

Mixed cell MMC topologies provide the same performance benefits of the FBSM-based MMC while minimizing cost and efficiency penalties. A wide range of mixed cell MMC topologies have been proposed in the literature. The most straightforward approach, which utilizes both HBSMs and FBSMs, is shown in Fig. 16.11 [19]. This topology reduces the required number of power devices and the conduction losses by 25%. It should be noted that during FRT, HBSMs are bypassed and only the FBSMs will be active. The following sections address operation of the FBSMs during these events and, therefore, apply to both the FBSM-based and the specific mixed cell MMC of Fig. 16.11.

The MMC operation principles of normal and dc FRT mode are illustrated in Fig. 16.12. For the normal mode shown in Fig. 16.12a, in the phase $\boldsymbol{x}$, the combined HBSM and FBSM outputs of one arm $\boldsymbol{v_{xu}}$, $\boldsymbol{v_{xl}}$ are positive with half dc bus voltage as dc offset. During the dc-side FRT response to a dc-side short-circuit LL fault, shown

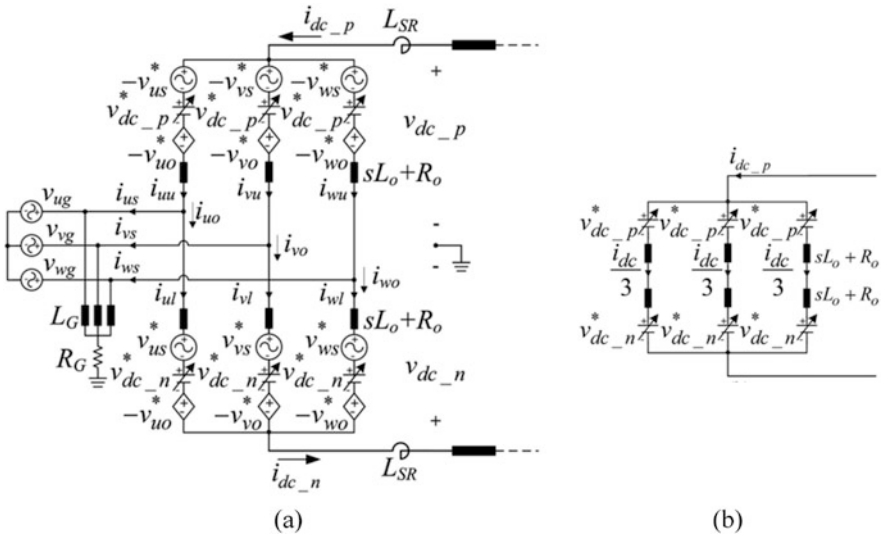

Fig. 16.13 MMC modeling (**a**) equivalent circuit of system and (**b**) equivalent circuit of dc current [19]

in Fig. 16.12b, the dc offset of $\boldsymbol{v_{xu}}$, $\boldsymbol{v_{xl}}$ is removed, through active gating, to avoid feeding the dc fault. The FBSMs can implement zero dc offset through active gating, without possibility of short-circuit paths through IGBT or IGCT reverse diodes, because of their bipolar output capability.

The FRT control strategy can be explained using MMC circuit model of Fig. 16.13 [19]. Figure 16.13a demonstrates that any arm voltage can be split into three parts: ac component, dc component, and circulating component. The dc fault current is dominated by the dc current which can be controlled by adjusting the arm output dc component $\boldsymbol{v^*_{dc\_p}}$ $\boldsymbol{v^*_{dc\_n}}$. Specifically, zero, positive, or negative dc components can hold, increase, or reduce the fault current. Thus, in a breakerless dc system, PGM MMC can also effectively control the fault current profile to achieve the fault localization, isolation, and post-fault recovery. The energy balancing mechanism during FRT is also critical, which is described in [19].

The FRT simulation results of a hybrid MMC are shown in Fig. 16.14. The fault occurred at $t = 2$ s and was detected soon and the hybrid MMC transferred to FRT control mode by bypassing HBSMs and activating FBSMs. A negative dc offset is generated on the FBSMs' output voltages to actively eliminate the fault current in 40 ms. In a typical breakerless system, this duration can be expanded by holding the fault current to the preset value, e.g., 1.5 p.u., to facilitate the fault localization. After fault is cleared at $t = 2.2$ s, the MMC is transferred back to normal operation mode to recover the system. During the FRT process, capacitor energy balance among the submodules is maintained.

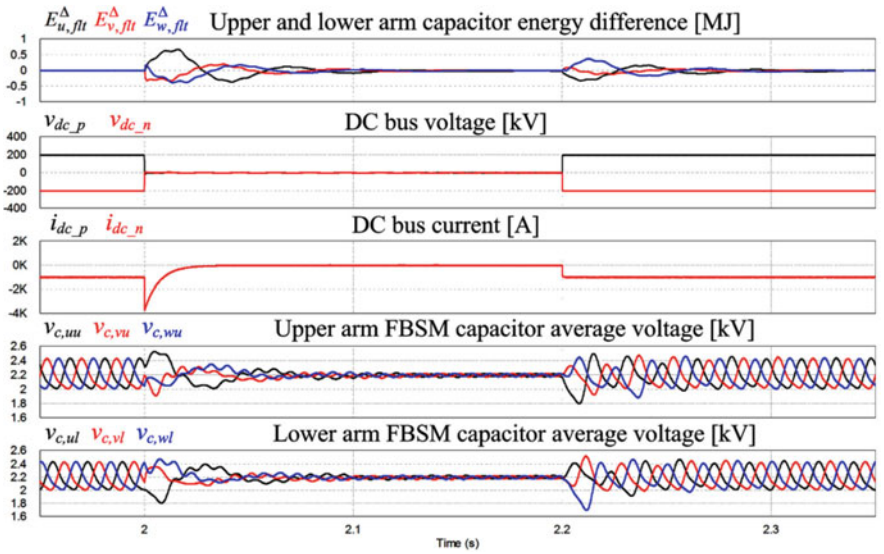

Fig. 16.14 Simulation results of MMC FRT under the pole-to-pole short circuit [19]

2.2 dc-dc Solid-State Transformers (SST)

Unlike ac-dc rectifiers, the dc-dc SST is a two-port bidirectional converter interfacing with both MVdc bus and LVdc bus. When a short circuit occurs on MVdc side, the desired operation of an SST is to ride through the MVdc fault by inhibiting switching of SST power semiconductors. If the MVdc fault is recovered in sufficient time, the internal energy storage can buffer the impact to the LVdc side and minimize the impact. Otherwise, a BESS is required to sustaining LVdc loading during MVdc-side fault isolation and recovery. If the LVdc side has a short-circuit fault, the SST LVdc port will operate in a similar manner to that of MVdc-interfacing ac-dc rectifiers, and MVdc side will be unaffected. It is important to note that the principle of an SST in a breakerless MVdc system can also be applied to the dc-dc converter interfacing battery energy storage system. The most common SST topologies are MMC-based and modular DAB-based.

2.2.1 MMC-Based SST

In an MVdc system, a dc-dc SST is the interface between the MVdc bus and LVdc bus. An MMC-based SST (iM2DC) has been proposed for a breakerless MVdc shipboard power system [10]. The topology shown in Fig. 16.15 is comprised of two FBSM-based three-phase MMCs linked with a medium-frequency (MF) transformer. As discussed above, the FBSM-based MMC has dc FRT capability,

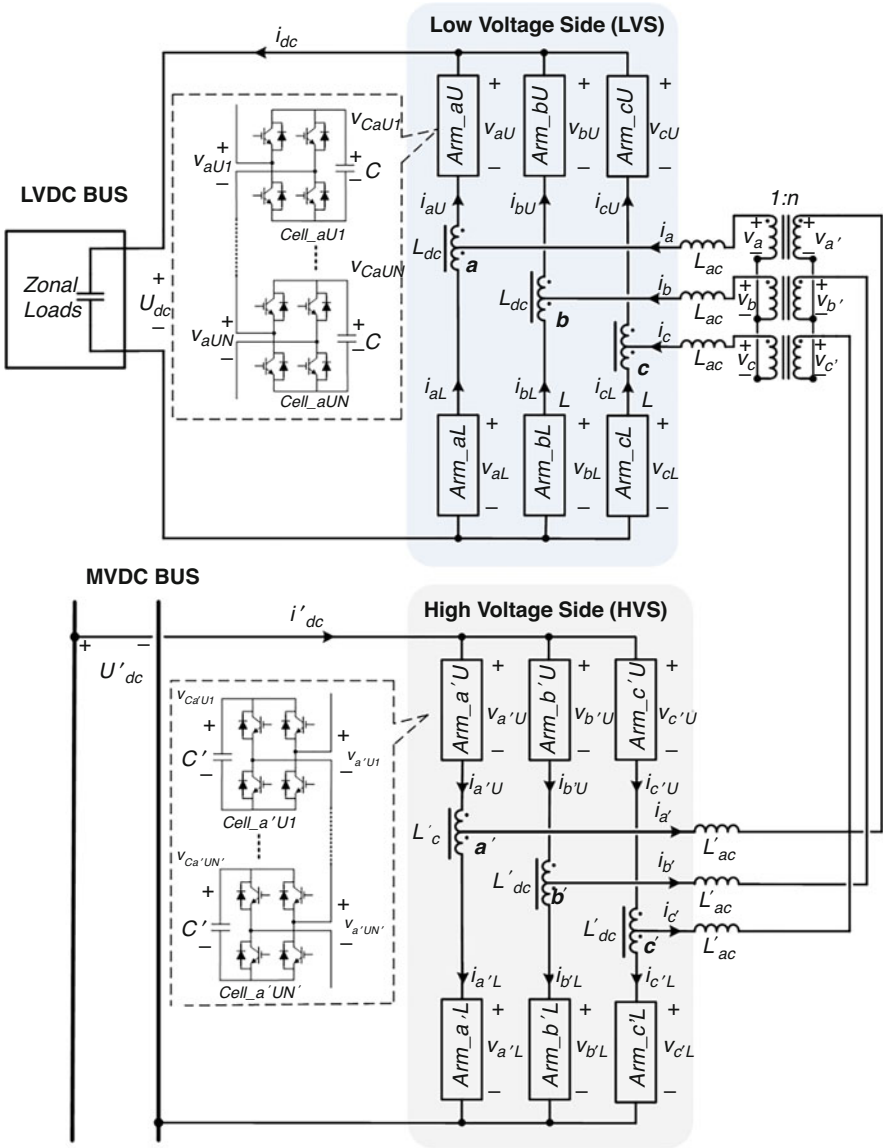

Fig. 16.15 iM2dc topology-based SST [9]

and thus iM2DC can implement FRT and breakerless fault management on either the MVdc and the LVdc side.

The ac link power flow control within iM2dc is implemented by combining both high-voltage side (HVS) control and low-voltage side (LVS) control illustrated in Figs. 16.16 and 16.17, respectively. The ac components of FBSM outputs $\boldsymbol{v^*_a{}'}$,

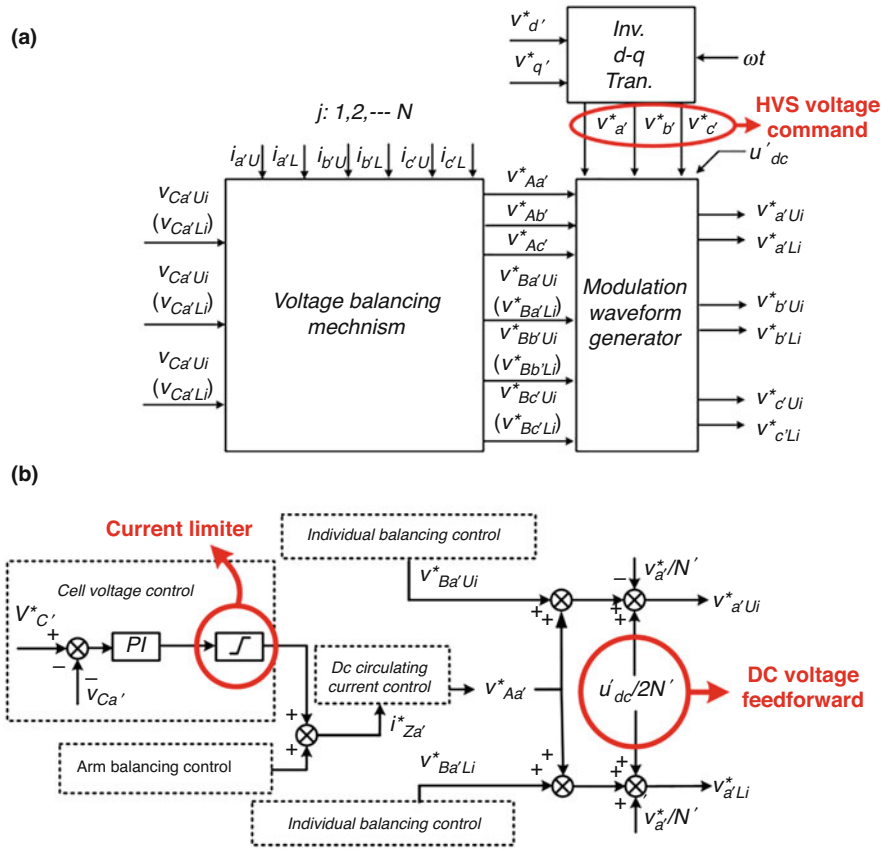

Fig. 16.16 HVS MMC control. (**a**) Control diagram. (**b**) Phase a dc power control loop with FRT capability in the voltage balancing mechanism and modulation waveform generator [9]

$v^*_b{}'$, $v^*_c{}'$, v^*_a, v^*_b, v^*_c will determine the ac link operation. As is shown in Fig. 16.16a, open-loop control of the HVS ac link voltage $v_a{}'$, $v_b{}'$, $v_c{}'$ is achieved on HVS MMC, while Fig. 16.17a shows that LVS control constitutes of averaged cell voltage outer loop control and ac link current i_a, i_b, i_c inner loop control. Since the twin MMCs share one common ac link, the transferred ac power flow can be regulated by adjusting the ac voltage through HVS control and by adjusting ac current through LVS control, respectively. Only active power will be transferred from MVdc to LVdc side by the ac link, and the energy is stored in the cell capacitors. The cell energy is subsequently deployed to the LVdc bus u_{dc} through LVS dc power control as shown in Fig. 16.17b. On the MVdc side, MVdc bus can charge HVS cell capacitors and averaged cell voltage v'_{Ca} needs to be controlled, as shown in Fig. 16.16b.

In the case of a dc short-circuit event, the iM2dc can ride through the fault by only isolating the faulted side dc power flow from the rest of system to minimize the fault impact. The MVdc fault scenarios are depicted in Fig. 16.18a, where the

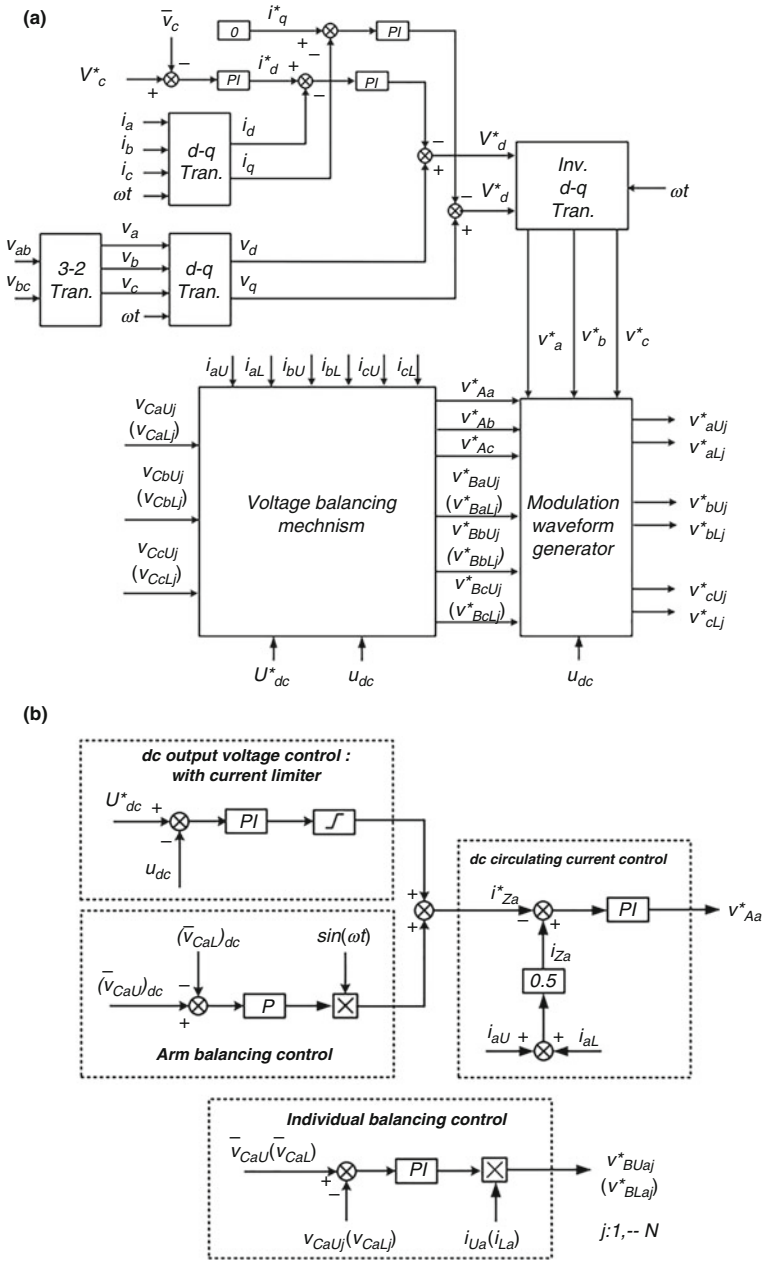

Fig. 16.17 LVS MMC control. (**a**) Control diagram. (**b**) Dc power control loop with FRT capability in the voltage balancing mechanism [9]

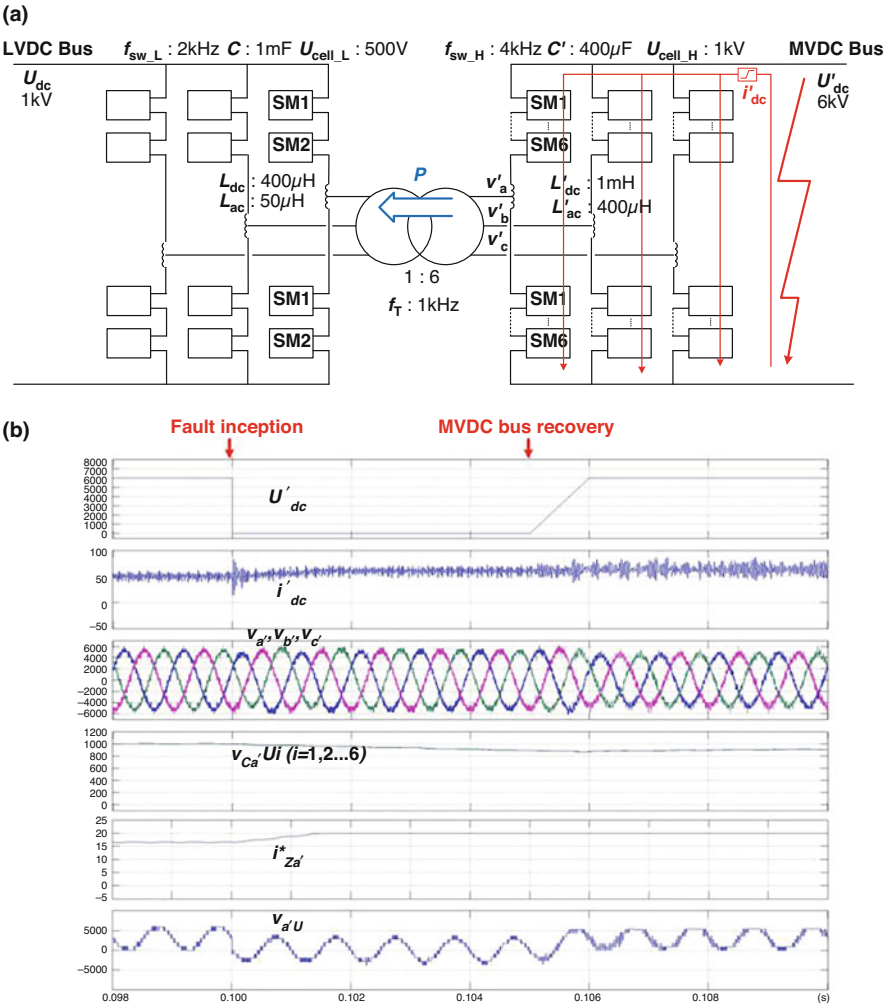

Fig. 16.18 Simulation results of MMC-based SST at MVdc short-circuit fault. (**a**) Converter topology and simulation parameters. (**b**) Simulation results: MVdc bus voltage U'_{dc}, MVdc current i'_{dc}, three-phase HVS ac link voltage $v_{a'}, v_{b'}, v_{c'}$, cell capacitor voltages of HVS phase a' upper arm $v_{Ca'Ui(i=1,2,\ldots,6)}$, HVS phase a' dc circulating current reference $i^*_{Za'}$, output voltage of HVS phase a' upper arm $v_{a'U}$ [9]

dc circulating current control in Fig. 16.16b will operate in saturation mode by triggering the current limiter. Additionally, the dc voltage feedforward signal in the modulation waveform generator can further accelerate fault current limiting by removing the dc bias from FBSM output during an MVdc fault. The dc fault current i'_{dc} from SST can be changed by setting the current limiter as needed to assist the MVdc bus breakerless fault protection. Meanwhile, the ac power flow from MVdc

to LVdc bus is unchanged, and no fault is propagated to LVdc side. Thus, the FRT capability enables an uninterruptible power supply (UPS) function during the MVdc fault by utilizing the stored energy in the HVS MMC cell capacitors.

Figure 16.18b shows simulation results of iM2dc during MVdc fault, where the i'_{dc} is limited to 60 A, once the fault occurrs at 0.1 s, and no reversal fault current is generated to feed the fault point. It should be noted that no fast fault detection and operation mode transition is needed to control the fault current. The dc voltage feedforward control removes the dc bias arm output voltage $v_{a'U}$ to accelerate dc fault current limiting. Meanwhile, the ac link voltage v_a', v_b', v_c' is almost unchanged during the fault to implement FRT process. It should be pointed out that the cell capacitors operate as energy buffers to provide power flow and the cell voltage $v_{Ca'Ui(i=1,2,\ldots,6)}$ and keep on decreasing until the MVdc bus recovered. The recharging of these cell capacitors requires slightly larger power than normal state until cell capacitors fully recharged at 0.13 s. This behavior can increase bus recovery time and increase the need for downstream ride-through energy storage or diode auctioneering from dual buses. Fortunately, this short-term overload condition can be controlled by adjusting the upper limit of dc current reference. Higher upper limit reference leads to faster recovery, and vice versa. This trade space will enable optimization of the fault handling capability against other objectives, such as limiting device stresses and increasing of power density.

Similar to MVdc fault case, the LVdc fault current i_{dc} can be limited by triggering the current limiter and removing dc bias in LVS control in Fig. 16.17b. As is shown in Fig. 16.19a, the FRT capability can facilitate the breakerless fault management on the LVdc bus. At the same time, no ac power exchange between MVdc and LVdc bus is needed since no load exists during LVdc fault. The HVS MMS simply operates in normal mode under zero loads, and no fault is propagated to MVdc bus. The simulation results in Fig. 16.19b show the complete breakerless fault management on LVdc bus. The fault occurs on the LVdc bus at 0.1 s, and the system recovers to normal operation after 6 ms. The LVdc fault current i_{dc} is limited to a preset value, 400 A, for 2 ms to enable fault detection and localization. The LVS ac link current i_a, i_b, i_c is reduced by LVS MMC control to avoid overcharging of cell capacitors. Thus, the HVS converter simply treats this LVdc fault as a load change, and no fast fault detection nor mode transfer is required on the HVS MMC. Subsequently, the dc current limiter decreases the fault current to zero in order to de-energize LVdc system. The faulted branch can then be isolated by an NLSw at 0.103 s. After releasing the restriction on dc current reference, the bus voltage recovers softly by increasing its reference from 0.104 to 0.105 s. This faster rise time or practically instantaneous step change capability of bus voltage to bus restoration is possible due to the absence of a dc bus capacitor. On the other hand, voltage ripple will be larger due to the lack of loads and dc capacitors, and inevitable bus voltage dip occurred once load step change was applied at 0.106 s. Here again, design space variables are introduced that will enable the optimization of normal-mode power quality against speed of fault recovery.

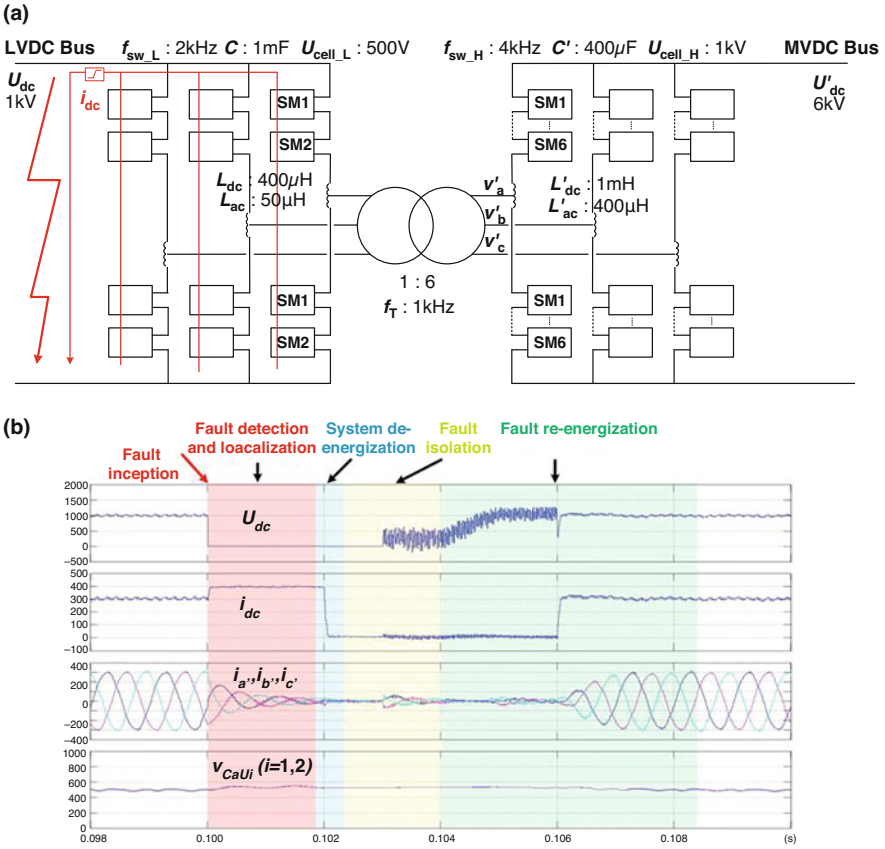

Fig. 16.19 Simulation results of MMC-based SST at LVdc short-circuit fault. (**a**) Converter topology and simulation parameters. (**b**) Simulation results: LVdc bus voltage $\boldsymbol{U_{dc}}$, LVdc current $\boldsymbol{i_{dc}}$, three-phase LVS ac link current $\boldsymbol{i_a}$,$\boldsymbol{i_b}$,$\boldsymbol{i_c}$, and cell capacitor voltages of LVS phase $\boldsymbol{a}$ upper arm $\boldsymbol{v_{CaUi(i=1,2)}}$ [9]

2.2.2 VF-DAB-Based SST

The DAB is an isolated dc/dc converter featuring high efficiency, low cost, and high power density because of characteristics of high-frequency ac link and soft switching. Specifically, a modular input-series-output-parallel (ISOP) configured DAB can operate as an SST to facilitate breakerless fault protection in the shipboard MVdc system interfaces to zonal LV distribution systems. As is shown in Fig. 16.20, one ISOP DAB consists of $\boldsymbol{M}$ DAB submodules, and each module contains two full-bridge cells linked by a high-frequency transformer.

The control of the modular ISOP DAB is distributed for each submodule, as illustrated in Fig. 16.21 [10]. During the normal operation, the power flow from MVdc (primary side) to LVdc (secondary) side and the LVS bus voltage $\boldsymbol{U_{dc}}$ are

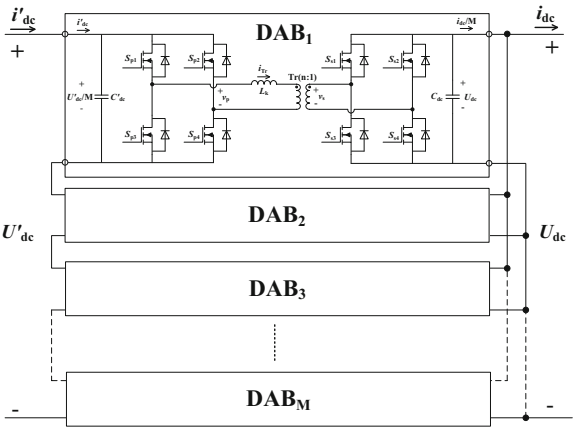

Fig. 16.20 ISOP DAB-based SST

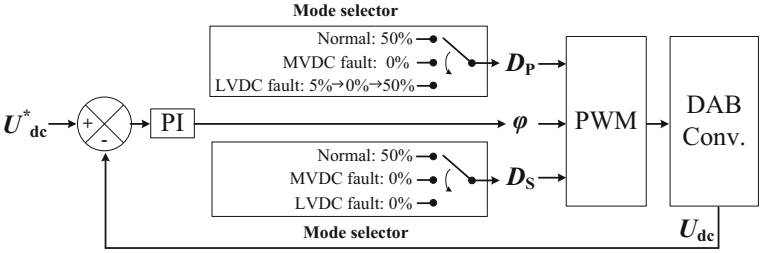

Fig. 16.21 Control block diagram of each DAB submodule in normal or fault operation mode

controlled by adjusting the phase shift angle φ between primary and secondary side full-bridge cells, while the duty cycles of both sides $\boldsymbol{D}_{\mathbf{p}}$ and $\boldsymbol{D}_{\mathbf{s}}$ are fixed to 50%. When the short-circuit fault happens on the MVdc bus, the DAB needs to shut down to avoid fault propagation to LVdc side. During the LVdc fault scenario, gate signals are blocked on the secondary side full-bridge cell, while the primary HVS will keep on switching to control the LVdc fault current and implement breakerless fault management on the LVdc side. The corresponding primary-side duty cycle $\boldsymbol{D}_{\mathbf{p}}$ is lowered (e.g., 5%) to suppress the current stress on the devices and transformer. It is important to point out that controlled mode transitions between normal and fault modes of operation are required. To minimize the possibility of transitional operational modes, a very fast fault detection mechanism is required for ISOP DAB converter.

A 6-kV/1-kV 300-kW ISOP DAB converter with six submodules is designed to illustrate the breakerless fault management procedure. The fault operation principle and simulation results during MVdc-side fault are demonstrated in Fig. 16.22. The fault occurrs at 0.1 s, and the MVdc-side filter capacitor $\boldsymbol{C}'_{\mathbf{dc}}$ discharges to feed the fault, and a reversal current spike can be observed on MVdc current $\boldsymbol{i}'_{\mathbf{dc}}$. As the MVdc bus voltage $\boldsymbol{U}'_{\mathbf{dc}}$ is forced to zero by the short-circuit LL fault, the four antiparallel diodes of primary devices $\boldsymbol{S}_{\mathbf{p1}}$–$\boldsymbol{S}_{\mathbf{p4}}$ are forward-biased due to the

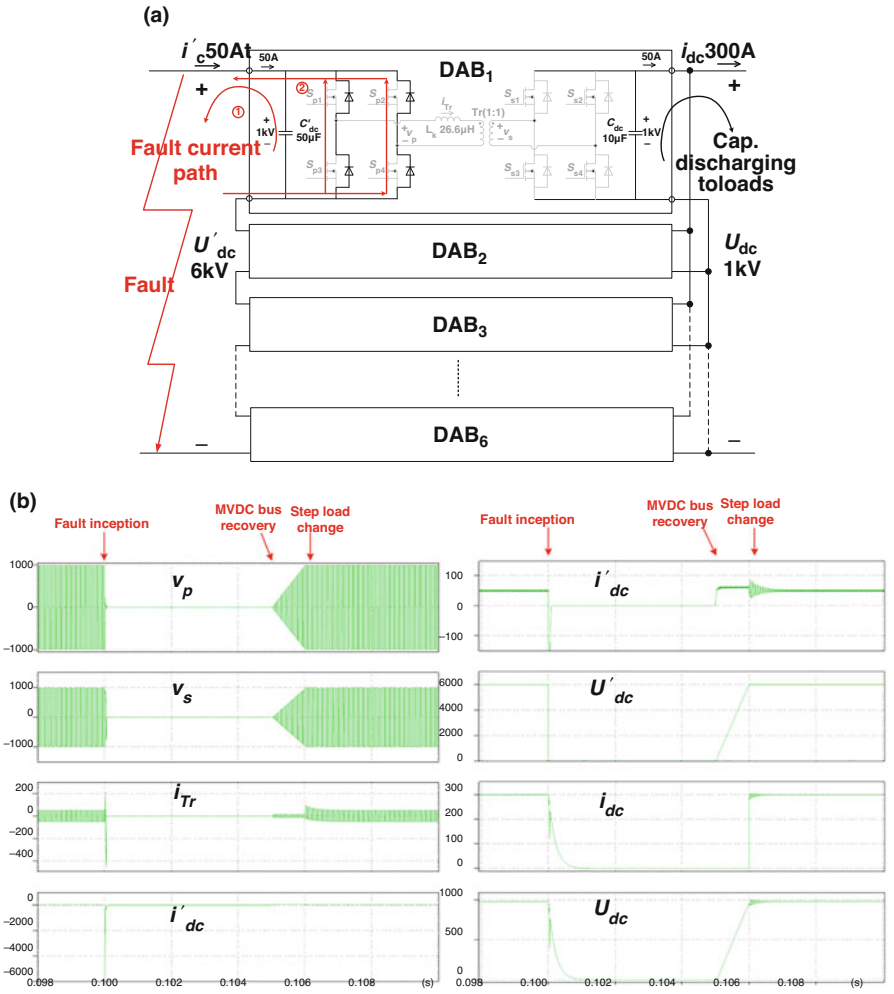

Fig. 16.22 Simulation results of DAB-based SST during MVdc fault. (**a**) ISOP DAB topology and simulation parameters and (**b**) simulation results, where v_p the submodule primary-side (HVS) transformer voltage and v_s the submodule secondary side (LVS) transformer voltage, i_{Tr} the submodule transformer current, i'_{dc} the MVdc bus current, U'_{dc} the MVdc bus voltage, i_{dc} the LVdc bus current, and U_{dc} the LVdc bus voltage [9]

fault loop inductance. It should be noted that this reversed fault current caused by capacitor discharging is unavoidable and beyond the control of DAB converter. This fault current profile strongly depends on the passive components within the fault path. In this MVdc fault simulation case, fault path inductance and resistor are assumed to be 2 μH and 50 mΩ, and thus a 10-kA current spike was generated and naturally decayed to zero after 150 μs. The induced current and thermal stresses may damage the free-wheeling diodes. The LVdc-side filter capacitor C_{dc} will also

discharge into the MVdc-side fault through the DAB converter. As can be seen from the transformer current $\boldsymbol{i_{Tr}}$, 500-A fault current flows across devices and the transformer 40 μs after fault inception. The converter detects the fault and transfers to MVdc fault operation mode with all devices chopping paused to limit this fault current. The transformer leakage inductor $\boldsymbol{L_k}$ influences the fault current slew rate. A fast fault detection method is required to limit the fault current. Device-level overcurrent protection, such as Desat protection, may be triggered to effectively protect the devices from permanent failure. However, the subsequent automatic system recovery and breakerless FRT will be disrupted. Consequently, a fast fault detection method is preferred for breakerless system application.

Referring again to Fig. 16.22, the remaining energy in the LVdc capacitor $\boldsymbol{C_{dc}}$ is dissipated into fault, and the LVdc bus is completely de-energized at 0.101 s. After MVdc fault management, the system recovery starts at 0.105 s, and a soft bus voltage recovery lasting 1 ms will limit the charging current to MVdc capacitor $\boldsymbol{C'_{dc}}$, as can be seen in MVdc voltage $\boldsymbol{U'_{dc}}$. In this case, a hard restart, direct transition to normal operation mode with devices switching in 50% duty cycle, was possible to effectively limit the converter current, as shown by $\boldsymbol{i_{Tr}}$ from 0.105 to 0.106 s. This is due to a no load pre-charging stage to filter capacitors $\boldsymbol{C'_{dc}}$ and $\boldsymbol{C_{dc}}$. A step load change is applied, and the system finally recovers to normal state. However, if the MVdc system recovery is not "soft" enough, a converter soft restart method should be adopted, which is addressed below.

Owing to the symmetrical structure of DAB converter, if the fault occurrs on the LVdc bus, a similar fault current profile results in the LVdc current $\boldsymbol{i_{dc}}$. One noteworthy difference is that the fault current fed from the MVdc side, the current path highlighted by #3 in Fig. 16.23a, can be controlled to implement breakerless LVdc fault management.

After the LVdc fault is identified, the DAB converter switches to LVdc fault operation mode with secondary LVdc-side full-bridge cell gating off and operating as diode bridge rectifier. Simultaneously, the primary MVdc-side full-bridge cell continues to be gated with a small duty cycle in order to limit the transformer current $\boldsymbol{i_{Tr}}$. After rectification by the diode bridge and filtering by LVdc capacitor $\boldsymbol{C_{dc}}$, ac current is converted to a constant dc current. This preset dc fault current can be adjusted by changing the primary-side duty cycle $\boldsymbol{D_p}$. Similar to the MVdc-side fault, fast fault current detection is essential to minimize the fault propagation to MVdc side and limit the fault current flowing across DAB converter. The MVdc-side full-bridge cell is shut down in order to de-energize the LVdc bus at 0.102 s after fault localization. Once fault current driven to zero, an ultra-fast NLSw is opened to isolate fault segment physically at about 0.103 s. Then a soft restart strategy is applied to charge LVdc capacitor $\boldsymbol{C_{dc}}$ under this no load, zero current condition. The duty cycle of primary MVdc-side $\boldsymbol{D_p}$ is increased from 0% to 50% in a controlled fashion in order to control the charging current. Finally, the secondary LVdc-side full-bridge cell restarts and loads are applied to recover the system completely. Based upon the described FRT strategy, closed loop control of the fault current has been proposed as a means of controlling charging current and bus recovery [10].

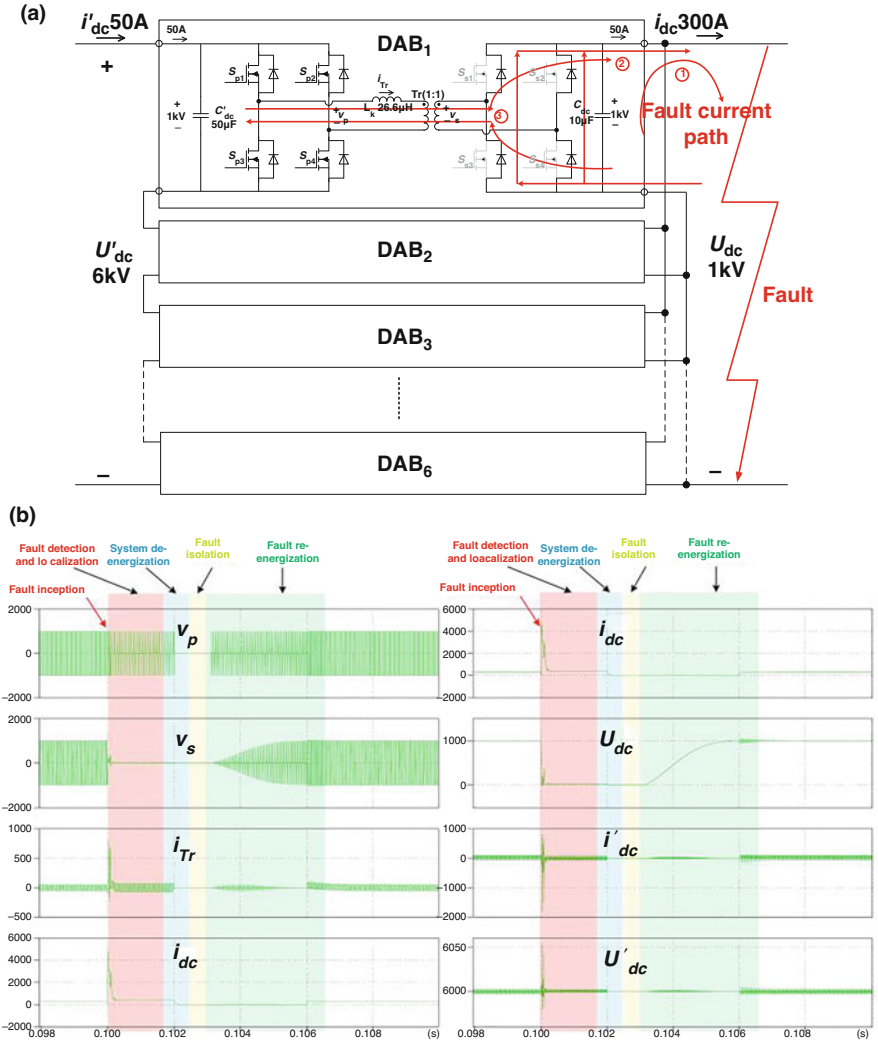

Fig. 16.23 Simulation results of DAB-based SST during LVdc fault. (**a**) ISOP DAB topology and simulation parameters and (**b**) simulation results, where v_p the submodule primary-side (HVS) transformer voltage and v_s the submodule secondary side (LVS) transformer voltage, i_{Tr} the submodule transformer current, i'_{dc} the MVdc bus current, U'_{dc} the MVdc bus voltage, i_{dc} the LVdc bus current, and U_{dc} the LVdc bus voltage [9]

2.2.3 CF-MDAB-Based SST

Compared to the voltage-fed DAB converter, the current-fed DAB (CF-DAB) converter has direct dc current control to realize dc FRT operation while inheriting the soft-switching capabilities. Additionally, terminal capacitor discharging is avoided

to minimize the fault current, and thus a fast recovery is realized. To be applied to the MVdc system, a current-fed modular DAB (CF-MDAB) converter with an inductor tank using HBSMs or FBSMs is proposed, as shown in Fig. 16.24a [11]. HBSMs are preferred for high-efficiency operation and high power density. Though the topology seems similar to the abovementioned iM2dc, its operation principle originates from the CF-DAB converter. Thus, the cell capacitors operate at a high frequency to significantly reduce passive component size. To realize the dc FRT operation, a hybrid arm structure composed of HBSMs and a certain number of FBSMs are utilized, where only FBSMs are active during dc FRT process, as is shown in Fig. 16.24a. All the HBSMs are bypassed, and the FBSMs output bipolar voltage with the magnitude reduced to $2\boldsymbol{qV_c}$, where $\boldsymbol{q}$ is the FBSM number in one arm and $\boldsymbol{V_c}$ the cell capacitor voltage. Meanwhile, the LVS ac voltage is matched by lowering the inserted SM number $\boldsymbol{p'}$. As can be seen in Fig. 16.24b, with the upper and lower arm 180° phase shifted, the averaged dc output voltage and the dc current $\boldsymbol{i_{dc}}$ are determined by duty cycle $\boldsymbol{D}$.

Specifically, the averaged circuit model of CF-MDAB under dc fault operation mode is depicted in Fig. 16.25, where the arm capacitor $\boldsymbol{C'_{arm}}$ now includes only the inserted FBSM cell capacitors. Two power conversion stages form the CF-MDAB. In the left hand-side first stage, the arm capacitor $\boldsymbol{C'_{arm}}$ is charged by the LVS-side sources. Then, the averaged dc output voltage is regulated by $\boldsymbol{D}$ implements direct dc current control. Correspondingly, the control system in FRT mode is given in Fig. 16.26. DC current is controlled by duty cycle $\boldsymbol{D}$, and the averaged arm capacitor voltage $\boldsymbol{v'_{arm}}$ is regulated by the phase shift angel φ.

A breakerless fault protection scheme is demonstrated on a downscaled setup based on the above-described FRT strategy, and the experimental results are shown in Fig. 16.27. When fault happens, the dc current $\boldsymbol{i_{dc}}$ rises quickly to the threshold of 18 A. It is assumed that no additional fast fault detection method is achieved and the fault can only be detected by the current sampling performed each switching cycle, resulting in a maximum if one switching cycle delay after fault detection. The fault current is limited by the dc arm inductance $\boldsymbol{L_{dc}}$. Approximately 30 μs after the fault inception, the dc fault is detected, the converter is shut down immediately, and i_{dc} decreases to zero within microseconds. The gating to the converter is inhibited until the dc voltage v_{dc} drops below a certain threshold. At $t = 175$ μs, the dc voltage is detected below the threshold of 25 V, and the converter transfers to current-limiting mode. With the designed duty cycle control, the dc current is regulated to the preset value at 12 A. After providing dc fault current for 10 ms, the converter is disabled again, and i_{dc} decreases quickly to zero. At $t = 20$ ms, the dc fault is cleared, and the bus voltage starts to restore. At $t = 58$ ms, the dc bus voltage reaches the arm voltage, and the converter returns back to normal operation.

Another CF-MDAB applied to the SST application for a breakerless MVdc system is proposed in [12]. The topology is shown in Fig. 16.28. Instead of using a direct current-fed DAB, similar to the approach in [11], an FBSM with an inductor is added to a voltage-fed SRC DAB converter to form a current-source port to interface MVdc side. The current control strategy is shown in Fig. 16.29, which is similar to that of MMC-based SST.

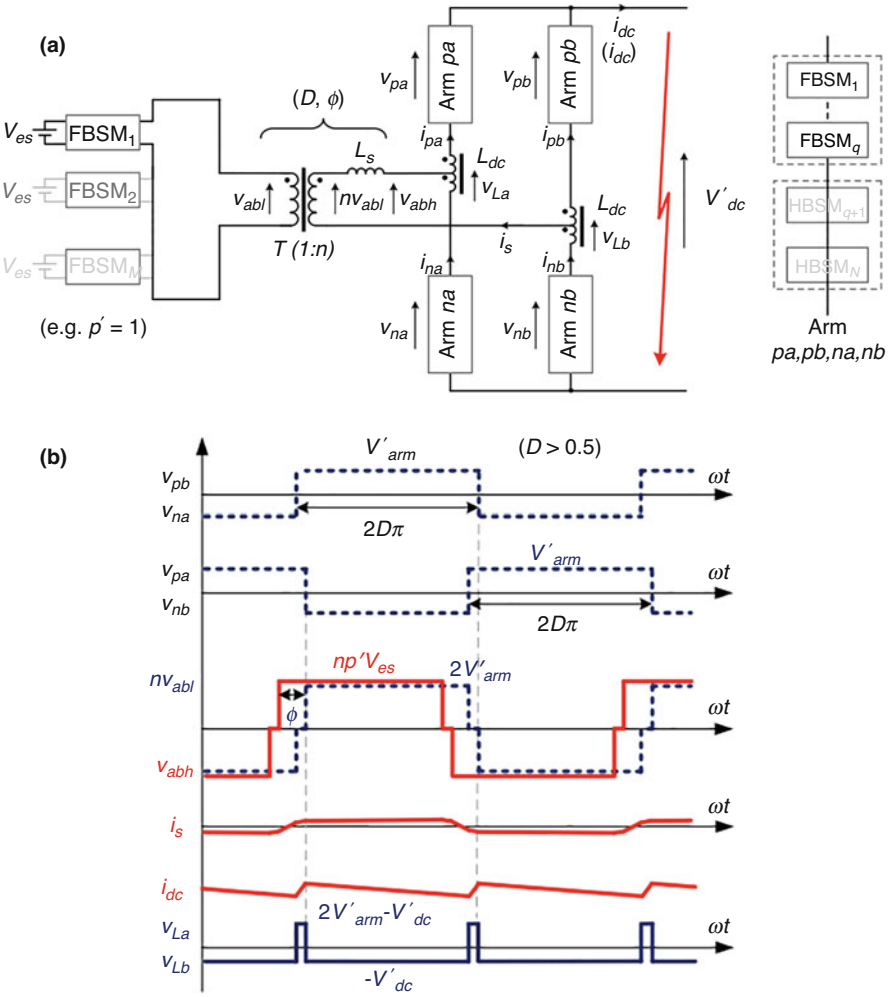

Fig. 16.24 CF-MDAB converter. (**a**) Dc fault operation mode and (**b**) typical operating waveforms [11]

3 Concluding Remarks

A breakerless MVdc power system is achieved by coordinating the control of MVdc-interfacing converters and the high-speed, near-zero current breaking mechanical disconnectors, i.e., NLSws, to detect and isolate low-impedance and, effectively, short-circuit faults on MVdc and LVdc buses (as well as other types of faults such high-impedance faults causing overcurrent conditions). This chapter has

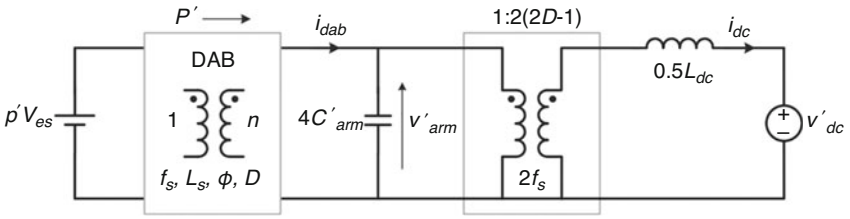

Fig. 16.25 Averaged circuit model of the CF-MDAB under dc fault operation mode [12]

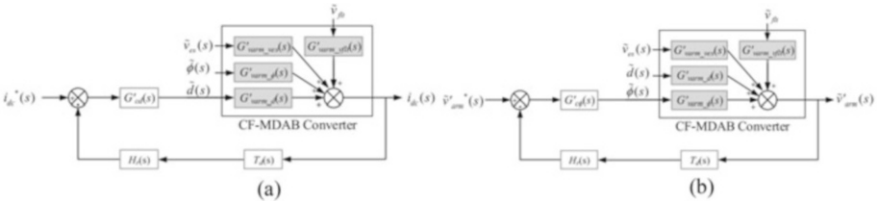

Fig. 16.26 Control block diagrams of the CF-MDAB under dc fault operation mode: (**a**) DC current control and (**b**) averaged arm voltage control [11]

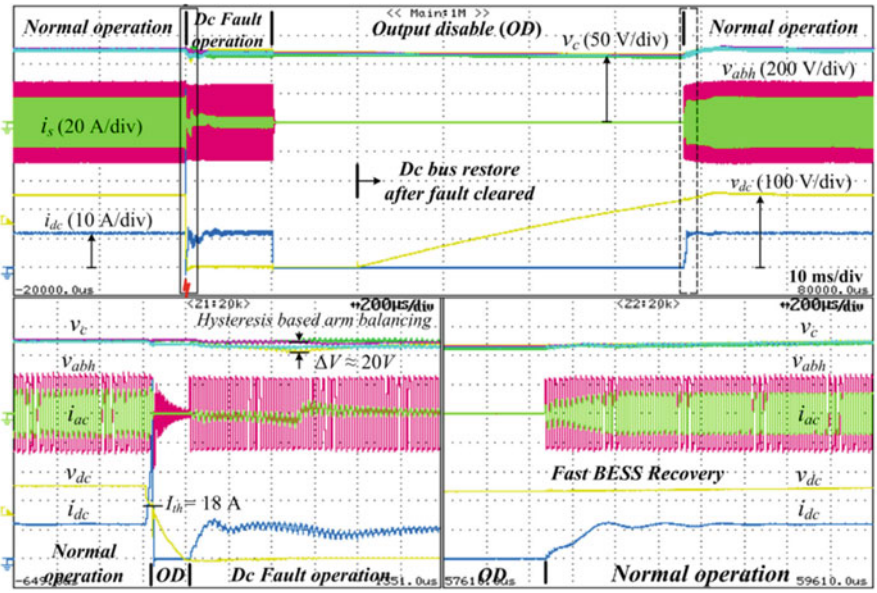

Fig. 16.27 Experimental results of an CF-MDAB converter-based breakerless fault protection process at $\boldsymbol{V_{dc} = V_{arm}} = 250$ V, $\boldsymbol{V_{es}} = 125$ V, $\boldsymbol{I_{dc}} = 12$ A [11]

focused mainly on the MVdc systems, although the concepts apply with complete generality to HVdc systems.

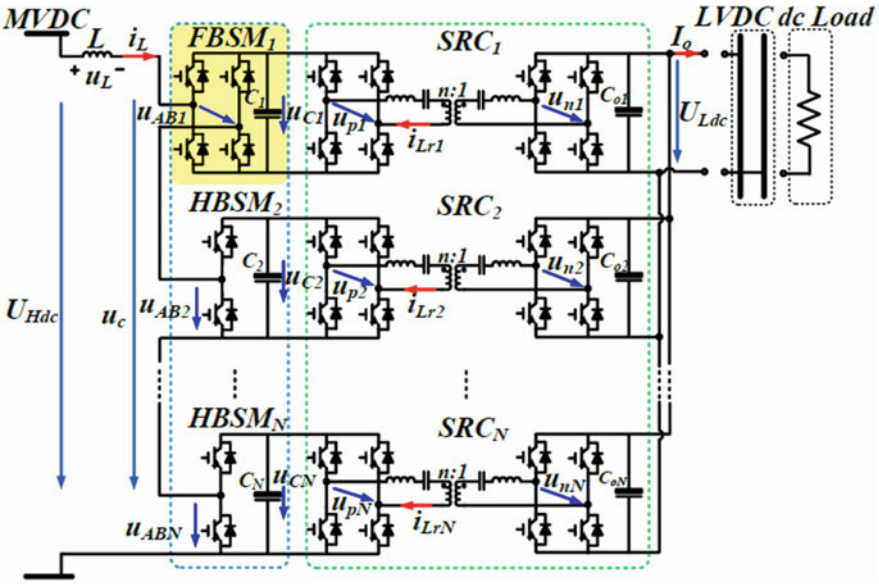

Fig. 16.28 A current-source DC SST based on SRC DAB topology for breakerless MVdc application [12]

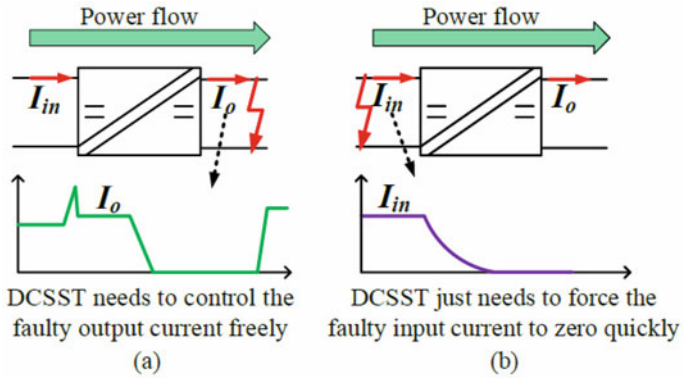

Fig. 16.29 The fault current control strategy proposed for this current-source DC SST [12]

Any power electronic converter topology capable of generating negative voltage across its dc output terminals can quickly diminish dc-side fault current to controllable levels. Power converters with this capability, such as thyristor rectifier and MMC with FBSMs, can be utilized in breakerless power system. In addition, DTC HBSM-based MMC and voltage-fed DAB-based SSTs can also implement FRT with breakerless protection capability by natural damping of fault path at the cost of longer fault clearing time. These two types of converters capable of breakerless operation bring with them trade-offs that must be considered in the implementation

of the dc network—from the standpoints of converter size, weight, cost, efficiency, and fault clearing time—that must be considered. These trade-offs may not be demerits to the entire system implementations if the added space claim, costs, and efficiency impacts associated with breaker-based protection are taken into account. In general, the right approach all comes down to the right approach for the system application.

Candidate power electronic converters for ac-dc and dc-dc points of interface with the dc network have been considered in this chapter. When considering the converter topology itself, the technical readiness, or maturation, of the approach—both from a hardware standpoint and complexity of operational modes versus fault scenarios—must be taken into account in order to reduce risks of implementation. Setting aside the wide range of possibilities for breakerless LVdc approaches—which are generally very low risk and easily extended according to the capabilities of, say, voltage- and current-source-based converters—the challenges and opportunities of breakerless protection have been addressed thoroughly in chapter for the MVdc application.

The current-source topologies such as MMC with FBSMs and current-fed DAB will exhibit better current control capability, which can be utilized for fault discrimination (locating the fault within the dc network). In addition, they are free direct capacitor connection across dc bus feed terminals, which eliminates the complication of dc-link capacitor or dc output filter discharge into the dc-side fault. These fault current arresting topologies also significantly reduce the time required to restore voltage to healthy parts of the dc network, thus increasing significantly the recoverability capability of the dc network and expanding the types of dc network architectures that can be considered.

This chapter has also pointed out that the breaker-based method and breakerless approaches have their own advantages and demerits. The breaker-based method applies the SSCB or HCB as fault interruption elements, which, as a minimum, adds the cost and size due to these breakers. While this approach allows for consideration of the entire range of power converter topologies and associated reduction of risk on the power conversion side and potentially the highest level of achievable of resiliency, a host of considerations are introduced on the dc distribution side. Perhaps the most significant of these considerations are the risks associated with the choice of SSCB versus HCB and the low technical readiness (i.e., commercial viability) of these devices, especially for MVdc systems. It is acknowledged that with time and experience, these risks will be diminished, but, at the same time, it must also be acknowledged that they will never be eliminated altogether. Unlike the ubiquitous electromechanical circuit breaker solutions that are applied to LVac and MVac distribution, which perform their function without changing the non-faulted behavior of the electrical network, the SSCB or HCB has an ever-present impact on the dc network. These impacts show up at one extreme as reductions in efficiency and increased need for thermal management of protective devices (minimal considerations for ac systems). At the other extreme, the proliferation of cascaded SSCBs or HCBs have a negative impact on system nominal transient performance that, as of yet, has not been quantified. This is particularly the case

for HCBs, which require current-limiting reactors to slow the speed of response to faults so that there is time for the solid-state parts to take over control and so that the solid-state parts are not overstressed during the fault event.

Since the breakerless method can remove dc breakers and utilize power converter inherent current control/limiting capability, the breakerless protection-based system seems to many researchers, grid developers, and other stakeholders to be the right approach to any power electronics-based electrical distribution system. Certainly, MVdc systems fall neatly into this category, where the application has limitations in available space and total weight limitations; and, from a power density perspective, it would seem that breakerless protection is the right approach. However, as has been pointed out, the limitations of the selected power converter topologies during the fault event and associated recovery steps must be well understood. Also, total size, weight, cost, and efficiency of the entire system with breakerless protection are not straightforward. The choice of power converter could significantly drive up size, weight, and cost of the individual converters within the system. As a result, the actual trade space between breakerless and breaker-based approach is much larger and more complex than it may seem when comparing one approach versus another. Since dc breakers suitable for MVdc are presently developmental, this trade space cannot be explored fully. Hopefully, in the future, a full exploration of the trade space given a range of viable converter and dc breaker solutions will be possible.

At the present time, there is an interesting conception that has arisen which applies the inherent current control/limiting capability of existing power converters in the breaker-based system to reduce the current stress of SSCB/HCB to improve its reliability. The converters in a breaker-based system usually passively shut, or their gating is temporarily inhibited in reaction to the fault event. The power semiconductor devices in HCB or SSCB and voltage clamping devices such as MOV need to withstand high current. One approach is to utilize the existing power converters paralleled with dc breakers to actively share fault current so that the power converters involved remain in actively controllable states [24]. Another approach is to actively coordinate both power converters with strategic placement of dc breakers to realize more resilient system implementations. While these methods will introduce extra device stresses within power electronic converters or introduce the additional size/weight/cost of dc breakers, they present hybrid alternatives to a purely breakerless protection approach and introduce options for system design that may be more optimal. However, in order to truly assess them, performance objectives and metrics, with respect to, say, operability and resiliency, must be well understood and well defined and must be modelled as part of the full-system design process.

To further emphasize the above point, with respect to the present state of the art, present-day experience indicates that breakerless systems may feature more power dense, lower cost, and lower risk from a nominal functionality standpoint. At the same time, the impacts and new measurements of effectiveness (potentially cross-cutting measures of effectiveness and performance) must be considered when it comes to the survivability and, ultimately, the resiliency of such systems. These measures of effectiveness must include system-wide modeling capabilities capable

of flushing out the nuances regarding communications and grounding mentioned above. Significant research in these areas has yet to occur as of the present date, and there is a tremendous need for such research to move forward if dc distribution, particularly MVdc distribution, is to one day become the way forward toward greener electrification.

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Chapter 17
DC Fault Current Limiters and Their Applications

Bin Li

1 Requirements on Fault Current Limiting

After a dc fault occurs in the flexible dc system, the sub-module (SM) capacitors discharge to the fault point, causing the arm current and dc cable current rising rapidly [1–7]. In existing flexible dc projects, the converter stations are often quickly blocked after the fault to reduce the fault hazard. Then the fault current can be cleared by the AC circuit breaker (for half-bridge MMC) or the converter (for MMC with self-clearing capability, such as full-bridge MMC) [8–12]. However, the above fault isolation scheme triggers the whole system outage, which is unfavorable to the power supply reliability and the stability of the interconnected AC power grid. Therefore, it is a feasible scheme for a flexible dc power grid to carry out fault current limiting to achieve fault ride through. It means that when a dc line fails, the dc protection should quickly locate the faulty line and send a tripping signal to the DCCBs at both ends of the line. Before the fault is isolated, all converter stations are supposed to continue operation to ensure the continuous power supply of the whole network.

In order to ensure power supply reliability, dc circuit breakers (DCCB) are widely adopted in the dc power grid [13, 14], because cooperating with the protection they can realize direct and selective cutoff of the fault. This makes it possible to continue the operation of the converter station after dc faults, that is, to improve the fault ride through of the healthy network [15]. The four-terminal meshed MMC grid, shown in Fig. 17.1, is taken, for example. For example, when the dc fault f_1 occurs on Line_1, Line_1 should be quickly isolated by DCCB B_{12} and B_{21}. Before the DCCB trips, the converter stations S_1~S_4 shall continue to operate to ensure that the healthy

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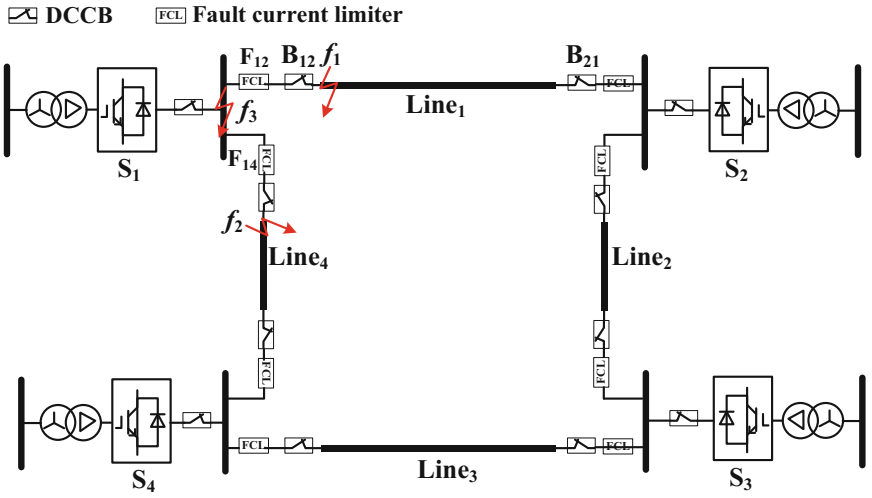

Fig. 17.1 Four-terminal ring MMC DC power grid topology showing DCCBs and FCLs

network can ride through the fault reliably. The converter station is allowed to be blocked only when the dc outlet or the corresponding bus bar fails. For example, S_1 is allowed to be blocked only when the fault occurs at f_3.

The continuous operation of the converter station after dc faults requires that the selective protection and the action speed of DCCB can match the development speed of dc faults [15]. However, in the MMC dc power grid, dc faults develop very fast [1, 6, 7]. After the dc fault occurs, the bridge arm current quickly rises above the threshold value of IGBT self-protection. If no other measures are taken, the converter stations are likely to be blocked during protection and DCCB action. Therefore, effective dc fault current-limiting measures are essential to improve the power supply reliability and operation safety of dc power grids.

The most typical technique of dc fault current limiting is to directly install dc reactors on dc lines [15, 16]. However, the direct installation of a large number of dc reactors in the dc power grid is detrimental to the system's dynamic response and isolation speed of DCCBs. Superconducting fault current limiter (SFCL) also has a certain application prospect in dc power grids [17, 18], but the related technologies still need to be further studied, including rapid quench after DC fault, rapid recovery after fault isolation, etc. Moreover, the FCL based in power electronic devices is widely researched for easy application, which is also analyzed in detail in the following subsections.

2 Analysis and Calculation of Fault Current Limiter

Installing an inductive fault current limiter at both ends of the dc line can effectively limit the fault current [15]. In this section, the method for calculating the value of the current-limiting reactor is given for the continuous operation of the converter.

Shown in Fig. 17.2, the fault voltage and fault current of a 10-kV (25 MW) dc system are given. Suppose a bipolar fault happens at $t = 3$ s at 1 km from the converter outlet and the converter stations are blocked 3 ms after the fault for the fault current has exceeded the tolerance of the electronic devices of the SMs.

To prevent the converter stations from being blocked after the dc fault, the bridge arm current i_{arm} (instantaneous value) should be limited within a certain upper limit value before the DCCB trips. In general, the upper limit of current depends on the threshold value of IGBT self-protection and can be set as $k_1 I_{\text{IGBTN}}$ (I_{IGBTN} is the rated current of IGBT in MMC, k_1 is defined as overload factor, and generally $k_1 > 1$ is reliability). Therefore, to ensure that the converter station can continue to operate after fault, it is necessary to ensure that $i_{\text{arm}} \leq k_1 I_{\text{IGBTN}}$.

In engineering practice, the rated current I_{armN} of the bridge arm is defined as the effective value of bridge arm current, which can be calculated as.

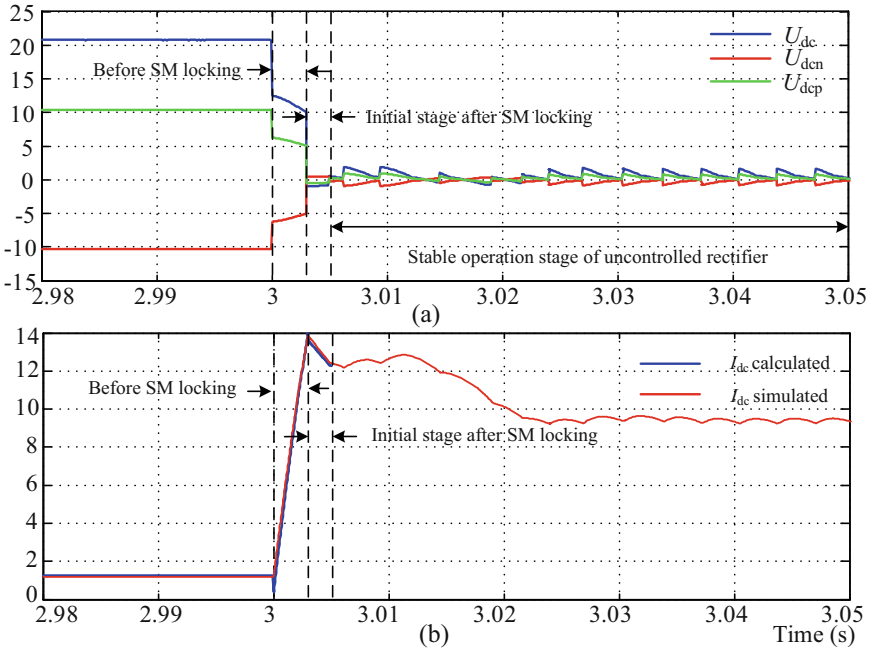

Fig. 17.2 Simulation results of the bipolar fault of MMC dc system. (**a**) DC voltage (kV). (**b**) DC current (kA)

$$I_{\mathrm{armN}} = \sqrt{\left(\frac{1}{3}I_{\mathrm{dcN}}\right)^2 + \left(\frac{1}{2}I_{\mathrm{sN}}\right)^2} \tag{17.1}$$

where I_{dcN} is the rated current of the converter station S_1 and I_{sN} is the ac phase current rating. $I_{\mathrm{sN}} = P/3U_{\mathrm{p}}\cos\varphi$, $P = U_{\mathrm{dcN}} \times I_{\mathrm{dcN}}$, and $U_{\mathrm{p}} = U_{\mathrm{dcN}} \times M/2\sqrt{2}$, so I_{sN} can be deduced as

$$I_{\mathrm{sN}} = \frac{2\sqrt{2}}{3}\frac{I_{\mathrm{dcN}}}{M\cos\varphi} \tag{17.2}$$

where P is the rated active power of the converter station S_1, U_{p} is the ac rated phase voltage, $\cos\varphi$ is the power factor, U_{dcN} is the rated dc voltage, and M is the modulation ratio. Substituting Eq. (17.2) into Eq. (17.1) can obtain

$$I_{\mathrm{armN}} = \sqrt{\frac{1}{9} + \frac{2}{9}\frac{1}{M^2\cos^2\varphi}} \cdot I_{\mathrm{dcN}} \tag{17.3}$$

In order to ensure a certain safety margin, the rated current I_{IGBTN} of the selected IGBT is slightly greater than the rated current I_{armN} of the arm, that is, $I_{\mathrm{IGBTN}} = k_2 I_{\mathrm{armN}}$, where $k_2 > 1$. Therefore, in order to ensure that the converter station is not blocked, the instantaneous value of the bridge arm current after fault must meet the requirement of Eq. (17.4):

$$i_{\mathrm{arm}} \le k_1 k_2 \sqrt{\frac{1}{9} + \frac{2}{9}\frac{1}{M^2\cos^2\varphi}} \cdot I_{\mathrm{dcN}} \tag{17.4}$$

Considering that the rise of bridge arm current at the initial stage of dc fault mainly depends on the rise of dc current [15], Eq. (17.4) can be equivalent to

$$i_{\mathrm{dc}} \le 3\left(k_1 k_2 \sqrt{\frac{1}{9} + \frac{2}{9}\frac{1}{M^2\cos^2\varphi}} - \frac{2}{3}\frac{1}{M\cos\varphi}\right) I_{\mathrm{dcN}} \tag{17.5}$$

Assuming that the time required from the fault time to the tripping time of the circuit breaker is t_{trip}, the current-limiting inductance L_{F} required by the FCL F_{12} can be obtained by solving Eq. (17.6):

$$\begin{aligned} &-\tfrac{I_0\omega_0}{\omega}e^{-\sigma t_{\mathrm{trip}}}\sin\left(\omega t_{\mathrm{trip}} - \beta\right) + \tfrac{U_0}{\omega(L_{\mathrm{s}}+2L_{\mathrm{F}})}e^{-\sigma t_{\mathrm{trip}}}\sin\omega t_{\mathrm{trip}} \\ &= 3\left(k_1 k_2\sqrt{\tfrac{1}{9} + \tfrac{2}{9}\tfrac{1}{M^2\cos^2\varphi}} - \tfrac{2}{3}\tfrac{1}{M\cos\varphi}\right) I_{\mathrm{dcN}} \end{aligned} \tag{17.6}$$

where L_{F} is the only unknown factor. The aforementioned method is also applicable to the selection and calculation of the current-limiting inductance of FCL installed at other locations.

Table 17.1 Parameters of four-terminal MMC-based DC power grid

Parameter	Value
Rated dc voltage (kV)	±200
Rated ac voltage (kV)	200
Rated capacity of S_1~S_4 (MW)	800, 400, 400, 400
Number of sub-modules	100
Capacitor of S_1~S_4 (μF)	13,000, 9750, 9750, 9750
Arm inductor of S_1~S_4 (mH)	32, 64, 64, 64
Equivalent resistance of dc line (ohm/km)	0.032
Equivalent inductance of dc line(mH/km)	1.29
Length of dc line(km)	100

Resource: He et al. [24]. Reproduced with permission of IET

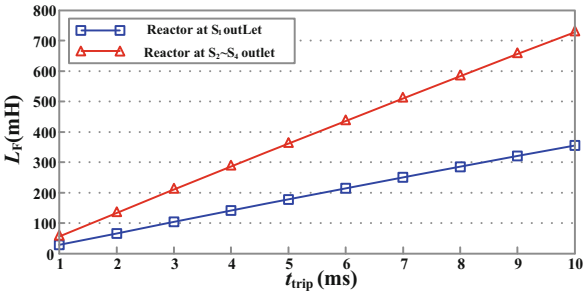

Fig. 17.3 Calculation results of the required current-limiting inductance of the different DCCB tripping time $t_{trip.}$ (Resource: He et al. [24]. Reproduced with permission of IET)

The detailed parameters of the dc system shown in Fig. 17.1 are given in Table 17.1. When different t_{trip} values can be calculated according to Eq. (17.6), the required current-limiting inductance value is shown in Fig.17.3, where k_1 is set as 2, k_2 is set as 1.5, and cosφ is set as 1.

Since the capacity of the converter station S_1 is different from that of other three stations, the corresponding required current-limiting inductance value is also different. Moreover, with the extension of t_{trip}, the required current-limiting inductance increases significantly. Existing studies suggest that the current-limiting reactor should be installed directly on the dc lines [15], but large inductance deteriorates the transient response and stability of the dc power grids. Moreover, the large inductance will also cause the fault current clearing speed of DCCB to be greatly extended. Therefore, the following problems should be solved for the FCL of a flexible dc power grid:

1. Side effect on the normal operation of the dc power grid: The adverse impact of the fault current limiter on the normal operation of the system shall be as small as possible, including transient response speed, operation stability, etc. Therefore, the ideal design is that the current-limiting reactor will not be connected to the dc line during the normal operation of the system.
2. Ensure that the converter station continues to operate after dc faults: During the dc fault, the converter station is expected to continue to operate, that is, fault ride

through. In other words, before the DCCB trips, the bridge arm current of the converter station is required to be limited below the set upper limit threshold. Therefore, the current-limiting inductor must be quickly connected to the fault circuit after the fault.

3. Coordination with DCCB: In dc power grids, the action process of DCCB and FCL is highly coupled, so they will affect each other. Therefore, the current limiter and circuit breaker must be able to achieve efficient cooperation, especially to ensure the rapid removal of the dc fault current.

3 Superconducting Fault Current Limiter (SFCL)

To solve the aforementioned problems, scholars have carried out a large number of research on fault current-limiting-related technologies of flexible dc systems. In terms of the implementation mode of a dc fault current limiter, it includes the use of a conventional current-limiting reactor, superconducting fault current limiter, and various fault current limiters based on power electronic devices.

The superconducting fault current limiter (SFCL) mainly realizes the fault current-limiting function through the superconducting characteristics of superconducting materials. In the flexible dc system, according to the different current-limiting methods of superconducting fault current limiter, it can be divided into resistance SFCL and inductance SFCL, as shown in Fig. 17.4.

The structure of resistance FCL is shown in Fig. 17.4a, which is usually composed of shunt resistance and a superconducting coil. During normal operation, the superconducting coil does not reflect the external inductive reactance. When a dc fault happens, due to the rapid increase of current, the superconducting coil quickly quenches and externally reflects the characteristics of high resistance, in this way limiting the fault current [17–19].

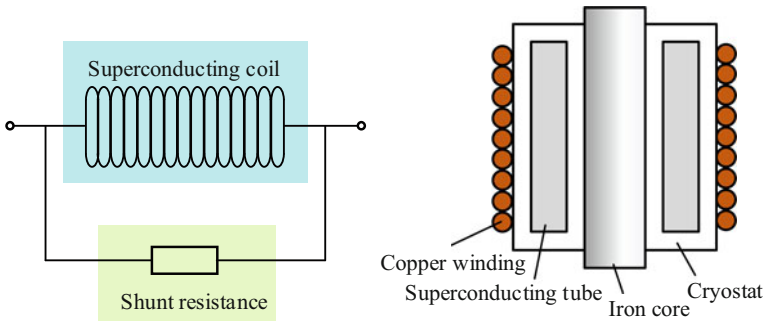

Fig. 17.4 Typical structure of SFCL. (**a**) Resistance SFCL. (**b**) Inductance SFCL. (Resource: Wang et al. [23]. Reproduced with permission of Automation of Electric Power System)

Table 17.2 Research of SFCL

SFCL type	Research institution	Capability	Date
Resistance	Siemens	900 V/1 kA	2005
	Tokyo Denki University	400 V/149 A	2009
	Shanghai Jiao Tong University	4 kV/2.5 kA	2013
	Institute of Electrical Engineering, Chinese Academy of Sciences	400 kV/1.5 kA	2013
		10 kV/400 A	2016
		40 kV/2 kA	2019
	Fast Grid	1 kA/50 kV	2017
	China Southern Power Grid	320 kV/1 kA	2018
Inductance	Seikei University	10 V/6 A	1991
	Wuhan University	500 kV/2 kA	2015
	Huazhong University of Science and Technology	200 V/30 A	2006
		220 V/10 A	2017
	Tianjin University	20 V/25 A	2018
		60 V/50 A	2020

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The topology of inductive SFCL is shown in Fig. 17.4b, which consists of an iron core, the cylinder made of superconducting material, and copper wire from the inside to the outside. During normal operation, the cylinder is in the superconducting state, which can cancel out all the magnetic flux generated by the copper coil, so as to present a zero inductance value, which has no adverse impact on the stable operation of the system. After the fault of the flexible dc system, the superconducting material quickly quenches, and the superconducting cylinder after quenching no longer completely offsets the magnetic flux generated by the copper coil so that the FCL presents inductance to the outside and limits the rise of the fault current [20–22]. Based on the inductive superconducting fault current limiter, Ref. [20] proposed using the inductive superconducting fault current limiter to limit the rising rate of fault current, established the system equivalent model, and verified the current-limiting effect of the inductive superconducting fault current limiter through transient calculation.

At present, the research status of SFCL at home and abroad are shown in Table 17.2 [23], which has superior performance and is an ideal dc FCL. However, this type of FCL still faces breakthroughs in technical problems such as high current carrying high-temperature superconducting tape and rapid recovery of superconducting materials, which is difficult to be popularized and applied in engineering.

4 Power Electronic Fault Current Limiter

FCLs based on power electronic devices refer to the FCLs composed of power electronic switching devices and basic power components such as inductance, resistance, or capacitance. When a short-circuit fault occurs in the flexible dc system, the input and exit of the current-limiting element (inductance/resistance) in different working stages can be realized by controlling the on-off of the power electronic switch in the dc FCL, so as to meet the technical requirements of the flexible dc power grid for fault ride through. Compared with SFCL, power electronic FCL is easy to be realized in engineering and has a very prominent technical prospect in the flexible dc power grid.

At present, scholars have proposed a variety of topologies and control strategies for dc FCL based on power electronic devices. According to the existing research, the FCL based on power electronic devices can be divided into bridge-type FCL, inductive coupling dc FCL, capacitor commutation dc FCL, and resistance/inductance hybrid dc FCL according to their different topologies, components, and working principles:

4.1 FCL with Bridge Topology

The bridge dc FCL is composed of an H-bridge circuit composed of power electronic devices, current-limiting inductance, and other power components. The typical bridge dc FCL topologies are shown in Fig. 17.5. The bridge-type dc FCL uses diode groups to form the H-bridge circuit and installs the current-limiting inductor and dc-biased power supply in the H-bridge, which is shown in Fig. 17.5a [24]. During the normal operation of the system, the current limiter uses the bias current provided by the bias power supply to realize the reliable bypass of the current-limiting inductance and eliminate the adverse impact on the operation stability. After the fault, the current-limiting inductance is connected to the fault circuit automatically. After the DCCB trips, the current-limiting inductor is automatically bypassed, which greatly improves the clearing speed of the fault current.

Based on the H-bridge structure composed of power electronic devices, a fault current limiter is proposed, which composes of the current-limiting inductor and power electronic H-bridge in parallel [25]. Its topology is shown in Fig. 17.5b. During the normal operation of the system, the IGBT in the H-bridge is off-state, and the system current is conducted through the inductance branch. When the system fails, the current-limiting inductor can directly play the role of current limiting. After the DCCB acts, the IGBTs in the H-bridge are controlled to be turned on, and the current-limiting inductor is bypassed by the power electronic devices in the H-bridge to realize the rapid removal of fault current. When the power fluctuation occurs in the system, the control strategy is the same as that when DCCB cuts off

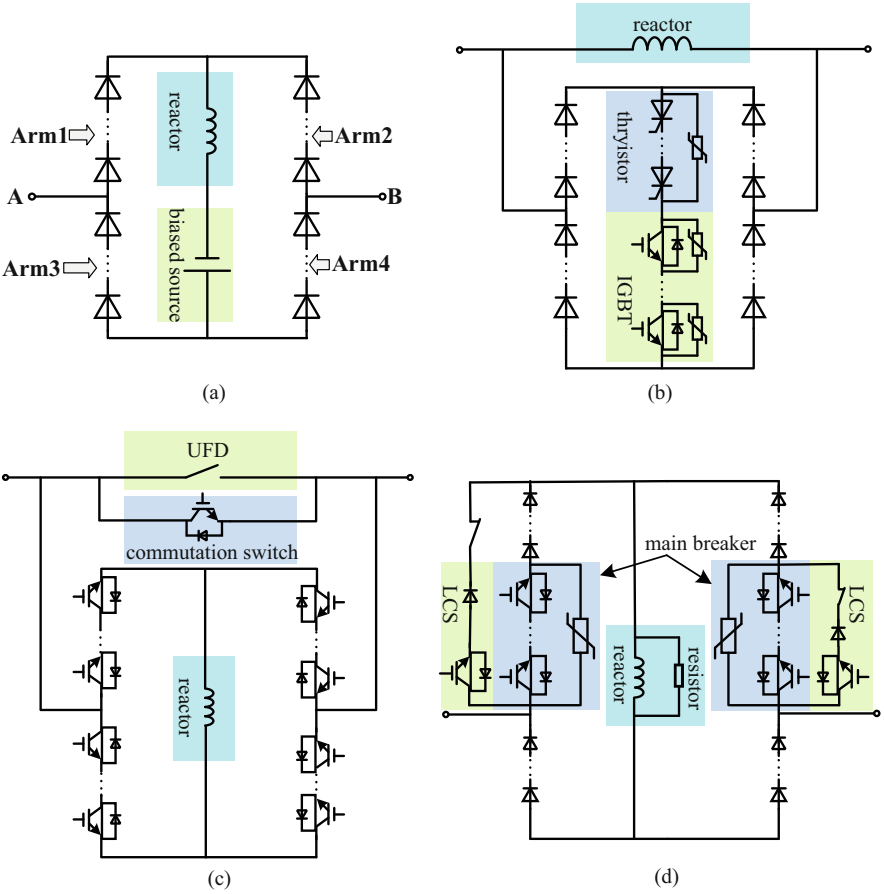

Fig. 17.5 Typical bridge FCL topologies. (**a**) The H-bridge FCL topology. (**b**) FCL based on current commutation. (**c**) Bridge-type dc FCL composed of IGBT. (**d**) The improved self-adaptive FCL with current breaking capability. ((**a**) Source: He et al. [24]. Reproduced with permission of IET. (**b**) Source: Li et al. [25]. Reproduced with permission of IEEE. (**c**) Source: Li et al. [26]. Reproduced with permission of Power System Technology. (**d**) Source: Lyu et al. [27]. Reproduced with permission of IEEE)

the fault, so as to effectively avoid the adverse impact of current-limiting inductance on the transient response speed of the system. Moreover, another bridge-type dc FCL composed of IGBT is proposed in Ref. [26], shown in Fig. 17.5c. When the system operates normally, all the power electronic switches in the topology are off-state. The fast mechanical switch is closed, and the dc current is conducted by this branch. After the short-circuit fault occurs on the dc side, the fast mechanical switch is disconnected, and the commutation branch is used to realize the fault current transfer. Then the IGBTs in the H-bridge are turned on alternately, that is, by controlling the fully controlled IGBT switch, the dc fault current is transformed into

the alternating current flowing through the current-limiting inductor. Fault current limiting is realized by using the characteristics of inductance passing through low frequency and preventing high frequency.

Reference [27] proposed a current-limiting topology with current breaking capability based on the bridge structure, which has an adaptive current-limiting function. Its topology and working principle are taken as an example to be illustrated in detail, shown in Fig. 17.5d:

1. Normal operation state The load branches of Arm_1 and Arm_2 are applied by conducting signals, while the IGBTs in the two main breakers are blocked. When i_{dc} flows from terminal A to B, it covers the load branch of Arm_1, dc reactor L, and Arm_4. The resistor R is bypassed by the dc reactor L. Arm_2 and Arm_3 are blocked due to the unidirectional conductivity of the diodes. Similarly, when the current flows from B to A, i_{dc} flows through the load branch of Arm_2, dc reactor, and Arm_3. Because there are only several semiconducting switches in the load branch, the conducting loss of the proposed topology is much smaller than traditional H-bridge topologies. Although the biased power source is removed, the application of R//L can also significantly minimize the negative impacts of the dc reactor on the stability during normal operation.

2. Fault current-limiting state Under the condition of dc fault, the amplitude of dc current increases significantly. The dc reactor provides a reverse voltage Ldi/dt, and the resistor limits the amplitude of the fault current, which function together to prevent the fault current from ruining the system.

The main factor limiting the isolation speed of the proposed topology is the switching speed of the fast mechanical switch. "Pre-action strategy" is adopted to faster the fault current clearing stage. Generally, when a fault is detected, the IGBT in load commutation switch (LCS) is used to switch off the circuit and realize current commutation. The IGBTs of the main breaker are gated on, the LCS is blocked immediately, and the open signal is applied on the fast mechanical switch. And the fault current is commutated from the load branch to the main breaker, as shown in Fig. 17.6b. If the protection has identified the fault properties as permanent and the FCL needs to be tripped, the tripping signal is applied to the IGBTs in the main breaker. While the fault is just transient, the FCL doesn't need to trip, and then the current can be commutated back to the LCS by sending controlling signals, which faster the fault clearing speed of the proposed topology.

3. Fault current clearing state After the fault is detected and identified by the protection, the corresponding main breaker is tripped to cut off the fault. As shown in Fig. 17.6c, if the fault is on side B, the main breaker in Arm_1 is tripped, yet the main breaker in Arm_2 conducts (i.e., proposed topology installed on positive output). In contrast, if the fault point is located in terminal A, the main breaker in Arm_2 is gated off, while the main breaker in Arm_1 still conducts.

To be specific, during a forward fault (namely, side A), the induction voltage of the reactor is directly exerted on Arm_2, which the diode unit of Arm_2 should withstand. In engineering practice, one diode and one IGBT are configured in the

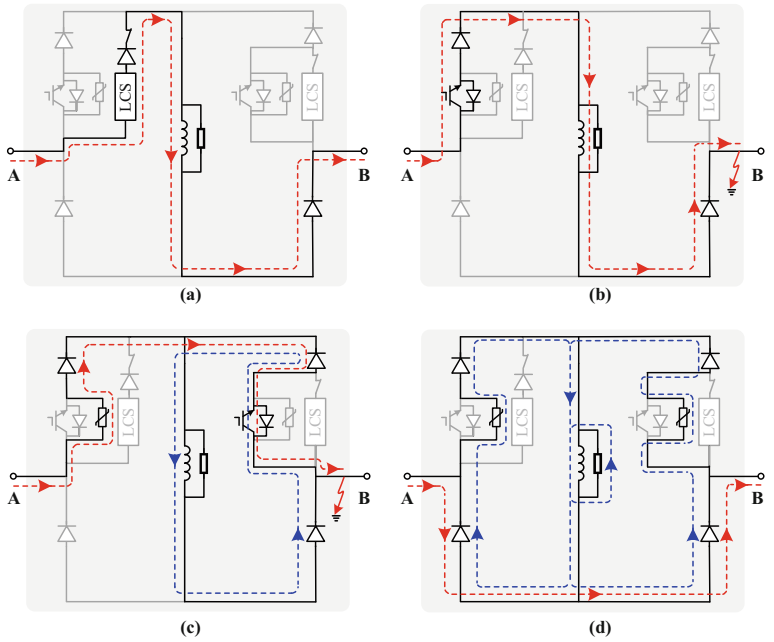

Fig. 17.6 Working principle of the improved self-adaptive FCL with current breaking capability: (**a**) normal operation state, (**b**) fault current-limiting state, (**c**) fault current clearing state, (**d**) recovery state. (Source: Lyu et al. [27]. Reproduced with permission of IEEE)

load branch of Arm_1, because their voltage rating is the conducting voltage drop of the main breaker, which appears when the LCS of Arm_1 is turned off, the mechanical switch has not been opened, and the IGBTs of the main branch have been turned on. After the current is commutated from the load branch to the main breaker, the mechanical switch is opened. And the series-connected IGBTs are turned off only when the mechanical switch is opened completely. This means the alone IGBT in LCS only needs to withstand the conducting voltage of the IGBTs and diodes in the main breaker. The opened mechanical switch bears the turned-off voltage of the IGBTs. During backward fault (namely, side B, i.e., the outlet fault of the converter), the diode of the load branch in Arm_1 bears the voltage drop of the current-limiting reactor. Due to the small capacity of MOV, the fault current-limiting capability is limited. Nevertheless, the corresponding converter must be blocked right away when there is an outlet fault, thus providing zero fault current to the system, and there is no need for current limiting for this converter. The fault current is mainly supplied by other converters in the system, which can be effectively suppressed by the proposed topologies at the outlets of those converters.

As Fig. 17.6c shows, the current through dc reactor i_{L} circulates in $L//R$, Arm_2, and Arm4. Meanwhile, i_{dc} flows through Arm1 and Arm_2. This means that the dc reactor is bypassed by the fault circuit and the fault energy of the dc line is

disconnected from the fault energy stored in the reactor. The connected-in MOV only needs to dissipate the former to clear i_{dc}. Therefore, the MOV capacity can be effectively reduced. T_{clear} of the dc reactor directly installed system is

$$T_{clear} = I_{trip} \cdot (L_l + L) / (U_A - U_{dc}/2) \tag{17.7}$$

where I_{trip} is the fault current at the tripping time, L_l is the equivalent inductance of the fault line, L is the inductance of the dc reactor, U_A is the clamping voltage of the MOV, and U_{dc} is the dc voltage of the system. Generally, L_l is much smaller than L. With the proposed topology installed, the fault current clearing time T_{clear} is computed as

$$T_{clear} = I_{trip} \cdot L_l / (U_A - U_{dc}/2) \tag{17.8}$$

T_{clear} of the dc reactor directly installed system is much larger than T_{clear} with the proposed topology being installed. Therefore, the fault current clearing speed of the proposed topology is much faster than that of the DCCB combined with the dc reactor only, which is very important for ensuring the normal operation of a healthy grid and rapid insulation recovery performance of fault cable.

4. Recovery state Since the dc fault is removed, the fault cable needs to be reconnected to the healthy grid. At the same time, the freewheeling current in the dc reactor needs to recover to I_{dcN}. It should be noted that I_{dcN} and i_L are dissimilar concepts. I_{dcN} is rated dc line current under normal operation, while i_L is the current flowing through L. Under normal operation and current-limiting state, $I_{dcN} = i_L$. In the fault clearing period, the MOV is connected to the fault circuit, so i_{dc} drops rapidly while i_L decreases slowly because there is no MOV in the circuit of Arm_2, L, and Arm_4. Therefore, before fault recovery, i_L is larger than i_{dc}.

During the recovery state, the other main breaker needs to be gated off first. The fault energy stored in the dc reactor is absorbed by R and MOVs, and i_L decreases rapidly. When i_L approaches i_{dc}, Arm_1 and Arm_2 are turned on at the same time, that is, the proposed topology recovers completely, preparing for the next fault. It should be noted that in practical engineering, IGBTs are usually equipped with snubber circuits. When Arm_1 and Arm_2 need to be turned on, if the IGBT in the load branch is directly turned on and the fast mechanical switch is reclosed, the snubber circuit capacitors of the IGBTs in the main breaker can only discharge through the MOV which leads to large time constant and difficult recovery of the proposed topology. Therefore, when Arm_1 and Arm_2 need to be turned on, the IGBTs of the main breaker should be turned on first, then the load branch is connected in, and, finally, the main breaker is turned off again to complete the recovery process of the proposed topology.

According to the above analysis, the recovery process can be divided into two states:

$i_{dc} < i_L/2$: Before recovery state, $i_{dc} = 0$, because the fault line has been cut off by the proposed FCL. When it starts to recover, i_L is equally distributed in Arm_1

and Arm_2, as well as in Arm_3 and Arm_4. When $i_{dc} < i_L/2$, i_{dc} flows through Arm_3 and Arm_4 directly, as Fig. 17.6d shows, so i_{dc} begins to increase rapidly. During this period, the polarities of the MOV's clamping voltages in Arm_1 and Arm_2, respectively, are opposite; thus, the voltage across the proposed FCL $u \approx u_A - u_A = 0$. Therefore, it can be considered that the MOV has no impact on the dc system. That is to say, as soon as the proposed topology enters the recovery state, the fault line is reconnected with the healthy grid. So the faulty grid can be recovered soon, and the recovery process of the proposed FCL does not affect dc grid recovery.

$i_{dc} \geq i_L/2$: In the recovery state, i_L decreases rapidly and i_{dc} rises. When i_{dc} exceeds $i_L/2$, Arm_3 is no longer on, and i_L can only flow through Arm_2 and Arm_4. The voltage over the proposed topology still meets $u \approx u_A - u_A = 0$. Therefore, its recovery process is still regarded having no effect on the dc system.

4.2 Inductive Coupled FCL

Inductive coupled FCL is composed of inductors and other power components with a coupling structure, which changes the external equivalent impedance of the current limiter by changing the current flowing through the coupling inductor, so as to realize the current-limiting function. The typical inductive coupling dc FCL topologies are shown in Fig. 17.7.

Illustrated in Fig. 17.7a, the inductive coupled FCL is composed of a current-limiting branch, an energy-absorbing branch, and a group of diodes [28]. The current-limiting branch is composed of a pair of coupling inductors and a group of turnoff thyristors, and the energy-absorbing branch is composed of an arrester. The FCL uses the mutual inductance between the coupling inductors to enhance the restriction effect on the short-circuit current after the fault and reduce the external equivalent inductance of the current limiter by turning on the thyristors after the DCCB acts, to accelerate the clearing speed of the fault current. The inductive coupling dc FCL proposed in Ref. [29] is composed of a fast mechanical switch, converter switch, and current-limiting branch, shown in Fig. 17.7b. When a short-circuit fault occurs in the line, the fast mechanical switch and converter switch are used to transfer the fault current to the current-limiting branch, and then IGBT is turned on alternately to make the fault current flow alternately between the coupling inductors. Under the mutual inductance of the coupling inductors, the energy in the fault current is transmitted between the two inductors to effectively limit the rise of the fault current. Using the coupling effect of inductance, Ref. [30] proposed an FCL with current breaking capability as shown in Fig. 17.7c. The current limiter is composed of a drainage current limiter part and a fault isolation current limiter part. The drainage current limiter includes a pair of coupling inductors, an IGBT, and a drainage branch connected in parallel with one of the inductors. The fault isolation current limiter is composed of a pair of coupling inductors in series with IGBT and IGBT in parallel. When the system operates normally, the line current is connected in series with IGBT through the inductance in the drainage current

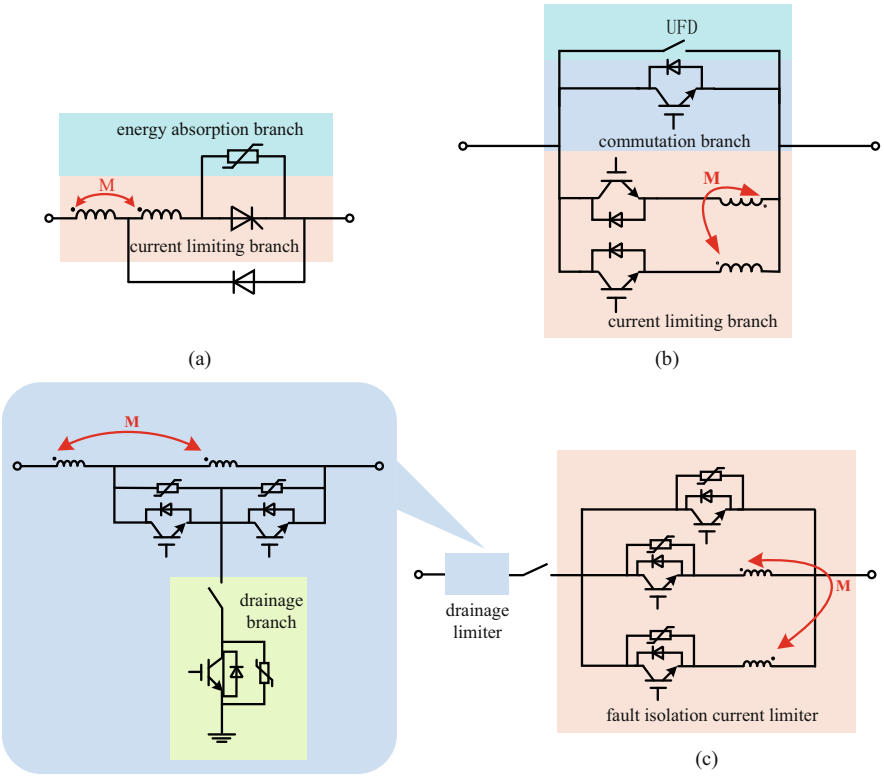

Fig. 17.7 Typical inductive coupled FCL topology. (**a**) Inductive coupled FCL. (**b**) Inductive coupling dc FCL with fast switch. (**c**) FCL with current breaking capability. ((**a**) Source: Zhengzhen et al. [28]. Reproduced with permission of IEEE. (**b**) Source: Guan et al. [29]. Reproduced with permission of Proceedings of CSEE. (**c**) Source: Wang et al. [30]. Reproduced with permission of Proceedings of CSEE)

limiter. After the fault, the IGBTs in the drainage limiter are turned off, and the bypassed inductance in the drainage limiter is forced to connect to the fault circuit to play the role of current limiting. When the protection detects the fault and sends out the action signals, the drainage branch and the IGBT in series with the coupling inductor in the fault isolation current limiter are turned on alternately. Under the action of the coupling inductor, it will reflect a large external impedance and force the fault current to flow through the drainage branch, so as to gradually reduce the current flowing into the fault point to zero and realize fault isolation.

Inductive coupled FCL uses the coupling inductor to convert the fault current into electromagnetic field energy in the coupling inductor, which limits the fault current under the interaction of magnetic field energy. This type of FCL has a good current-limiting effect, but the influence of the actual coupling coefficient of the coupling inductance and electromagnetic interference on the current-limiting effect should be considered in the actual manufacturing process.

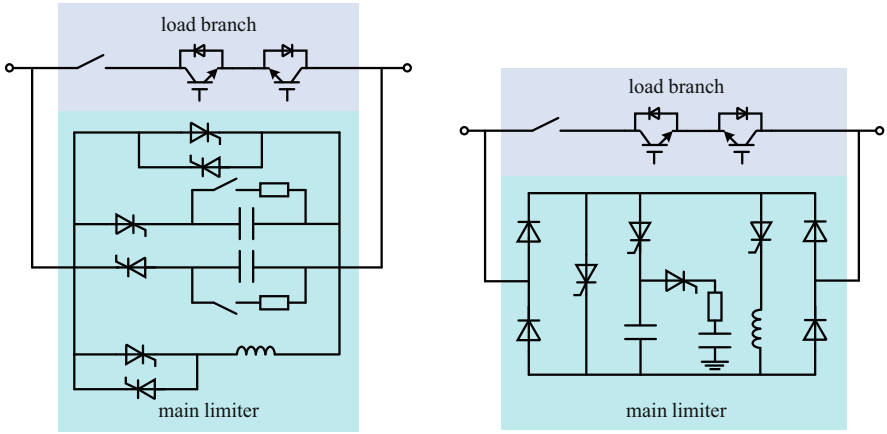

Fig. 17.8 Typical capacitor commutated FCL topology. (**a**) The capacitor commutation dc FCL. (**b**) The improved capacitor commutation dc FCL. ((**a**) Source: Han et al. [31]. Reproduced with permission of Proceedings of CSEE. (**b**) Source: Jianzhong et al. [32]. Reproduced with permission of Proceedings of CSEE)

4.3 Capacitor Commutated FCL

Capacitor commutated FCL is composed of a current-limiting inductor, commutation capacitor, and power electronic switching devices. The typical topologies are shown in Fig. 17.8.

The capacitor commutation dc FCL is composed of load branch and main current limiter [31], as shown in Fig. 17.8a. During the normal operation of the system, the load current flows through the load branch with low on-state loss. When a short-circuit fault occurs in the dc system, the IGBTs in the current branch are turned off, and the thyristor branch in the main current limiter is turned on to commutate the fault current to the main current limiter. After the current transfer process is completed, the thyristor connected in series with the capacitor is controlled to transfer the fault current to the capacitor branch under the action of the capacitor voltage, and the fault current limiting of the current-limiting inductor is realized after the voltage at both ends of the capacitor increases continuously. When the DCCB acts, the thyristor in the main current limiter is used to bypass the current-limiting inductance, to speed up the clearance of the fault current. The on-state loss of this topology is low, but it cannot realize self-recovery due to the capacitor voltage variation after the current-limiting process. Therefore, before being put into current-limiting again, it is necessary to use an additional auxiliary power supply to charge the capacitor and increase the construction investment of the converter. To solve this problem, Ref. [32] proposed an improved topology, as shown in Fig. 17.8b. When the short-circuit fault occurs in the line, the fault current is transferred

from the load branch to the current-limiting branch by controlling the thyristor and charging the capacitor with the fault current, so as to realize the fault current-limiting function. Compared with Ref. [31], this topology reduces the use of thyristors, and the capacitor in the improved topology does not need to be pre-charged before the current limiter is put into the current limiting, thus reducing the construction cost of the FCL.

The capacitive converter dc FCL realizes the input and bypass of the current-limiting inductor through the charge and discharge of the capacitors. However, this type of FCL topology contains many power electronic switching devices, and the control strategy and topology are relatively complex, which needs to be further improved in terms of cost and operation reliability.

4.4 Resistance/Inductance Hybrid FCL

Resistance/inductance hybrid dc FCL includes resistance, inductance, and power electronic switching devices. The typical topologies are shown in Fig. 17.9.

The resistance inductance hybrid FCL consists of a current-limiting inductor and an energy dissipation circuit in parallel [33]. The energy dissipation circuit is composed of an energy-absorbing resistance and a group of antiparallel thyristors. Its topology is shown in Fig. 17.9a. The thyristor groups in the energy dissipation circuit are turned on rapidly after the DCCB trips. At this time, the fault energy stored in the current-limiting inductor is absorbed by the energy absorption resistance and effectively separated from the fault energy storage of the fault line, so as to greatly reduce the energy consumption demand of the arrester in the DCCB

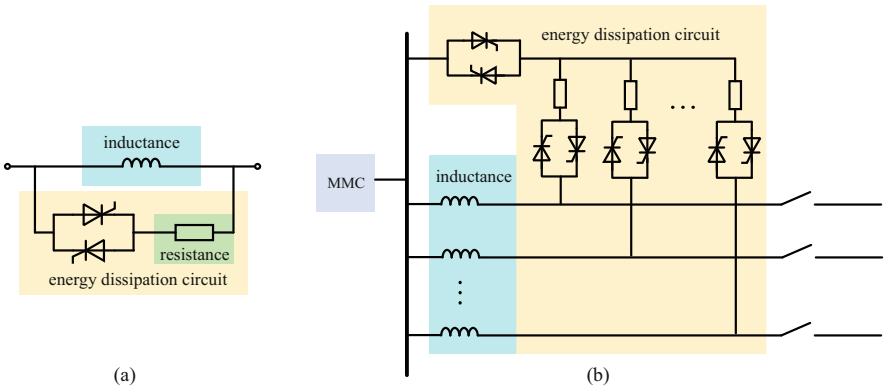

Fig. 17.9 Resistance/inductance hybrid dc FCL topology. (**a**) The resistance inductance hybrid FCL. (**b**) The improved hybrid current-limiting circuit (HCLC). ((**a**) Source: Liu et al. [33]. Reproduced with permission of IEEE. (**b**) Source: Li et al. [34]. Reproduced with permission of IEEE)

and shorten the fault clearing time. The FCL has the advantages of a simple topology and control strategy, low cost, and low manufacturing difficulty. However, the topology does not consider the adverse effect of current-limiting inductance on the operation stability of flexible dc systems. To solve this problem, Ref. [34] improved the topology and control strategy of the current-limiting circuit. In case of a fault in the system, the thyristors are triggered in case of system failure and power fluctuation, and then the adverse impact of the original current-limiting circuit on system stability is eliminated. In addition, the application of multi-ports significantly reduces the construction cost of the current limiter. The topology of the improved hybrid FCL is shown in Fig. 17.9b.

The resistance inductance hybrid FCL uses the current-limiting inductance in the topology to realize the current-limiting effect and uses the resistance to absorb the fault energy stored in the inductance in the fault clearing stage, to shorten the fault clearing time and reduce the energy consumption demand of the arresters.

5 Concluding Remarks

To sum up, the effective FCL is very significant for the fault ride through of the dc system. This chapter mainly studies the application of FCLs, including the directly installing dc reactor, superconducting FCL, and power electronic FCL, focusing on the theoretical analysis method of current-limiting requirements, the topology design and working principle of new fault current limiter, and the analysis of application advantages.

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Chapter 18
Eliminating SF_6 from Switchgear

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1 Introduction

Today, the electric grid in the United States is responsible for distributing over 4 trillion kWh per year of electricity from generators to consumers. It forms an integrated network that has become an indispensable asset to the nation's economy, infrastructure, and security. The physical infrastructure of this network depends on a combination of specialized equipment including transformers, power converters, power factor correctors, and switchgear. A critical component for the safety and reliability of the electric grid is a man-made gas, sulfur hexafluoride (SF_6). In 1937, General Electric (GE) introduced SF_6 as an insulation gas to the electric industry; since then, SF_6 has become ubiquitous in medium-voltage (MV) and high-voltage (HV) equipment. Among its many key attributes are its intrinsic nontoxic, noncorrosive, and nonflammable nature, in addition to its superior stability over a wide operating window, good thermal conductivity, high dielectric strength, and excellent arc-quenching capabilities. These properties make it particularly amenable as an insulating and arc-quenching gas in electrical equipment [1]. As a result, over 90% of gas-insulated switchgear globally uses SF_6 as the insulating gas [2]. However, SF_6 emissions from the electric transmission and distribution sector pose a significant climate risk as a potent and long-lived greenhouse gas (GHG) source. One ton of SF_6 emitted to the atmosphere has an equivalent 100-year global warming potential (GWP) of 22,800–26,700 tons of carbon dioxide and has an

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estimated atmospheric lifetime of 3200 years [3]. As a result of its strong radiative forcing and long atmospheric lifetime, SF_6 was designated as one of the six main greenhouse gases in the 1997 Kyoto Protocol.

As countries set increasingly ambitious emission targets in accordance with the Paris Agreement, emissions of all GHGs, particularly from the electric grid, will be scrutinized. Furthermore, regulations being considered in places like California and the European Union (EU) aim to completely phase out SF_6 from electrical equipment, necessarily setting a timeline to develop alternative solutions to SF_6-insulated equipment. Alternative solutions developed today could define the market for decades to come, both in the United States and globally.

Equipment leaks are a major source of SF_6 emissions from the electrical transmission and distribution sector. This fact is particularly true for aging equipment which, due to natural deterioration, is more prone to gas leaks [4]. A study presented at the 2000 International Conference on SF_6 and the Environment suggests that 10% of circuit breakers in the United States leak; of that 10%, 15% were identified as minor leaks and 85% were identified as major leaks or leaks that required operations to schedule repairs [5, 6]. The National Electrical Manufacturers Association (NEMA) estimates leak rates of 0.1% per year, while the International Electrotechnical Commission (IEC) standard 62271-1 (2004) sets the standard for equipment leakage at 0.5% [7]. Across the entire life cycle of the equipment, however, SF_6 emissions may be as high as 15% and potentially underreported by at least a factor of two [8, 9]. In addition to the emissions associated with equipment service life, losses due to poor gas handling practices are to blame. The operation and maintenance of SF_6 gas carts are considered a major source of handling-related losses [4], and some in industry say the eventuality that all created SF_6 will ultimately end up being released into the atmosphere should be considered [10].

Today, significant effort is dedicated toward supplanting fossil fuel-derived electricity generation with wind and solar power, with the concomitant effect of the grid becoming increasingly decentralized. The electrification of transport, heating, and cooling will also require grid expansions [11]. Barring any disruptive technological advances or policy-driven trends, more gas-insulated equipment (GIE) employing SF_6 will be added to the grid, increasing the emission risks and, ironically, potential climate impacts. Between 1994 and 2022, the measured SF_6 in the atmosphere has increased 3.5-fold [12], and as more clean energy is integrated onto the grid, SF_6 emissions from the transmission and distribution (T&D) sector (0.25% of combined emissions from SF_6 and power generation, 0.07% of total GHG emissions from the United States in 2019) will likely continue to rise and constitute a larger proportion of emissions from the electric grid [13] (Fig. 18.1).

In addition, a large portion of the US grid was built in the 1960s and 1970s, implying that the equipment currently in use is approaching or exceeding its useful life span [11]. The aging infrastructure has two important implications. First, older equipment tends to leak more SF_6 or require more volumes of SF_6 which pose a significant climate risk [4]. Second, within the next few decades, much of this equipment will be replaced and will require large investments. Precluding any market-ready alternatives, this equipment will be replaced with new equipment that

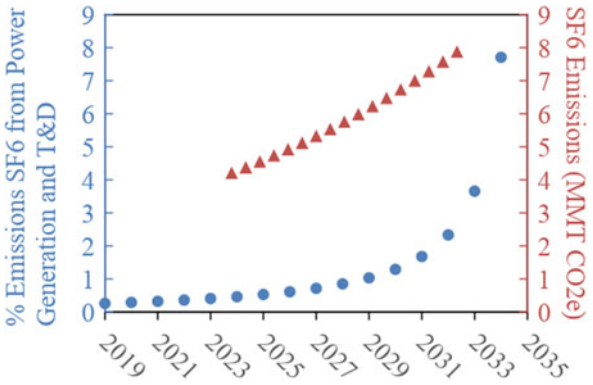

Fig. 18.1 Projected SF_6 emissions as a percentage of the emissions from power generation and T&D and in real terms, expressed as MMT CO_{2e}. Calculations based on emissions from power generation decreasing linearly to zero by 2035 and SF_6 nameplate capacity increasing by 4% per year (consistent with the average historical increase between 1999 and 2013) and SF_6 emission rates of 1.5% consistent with EPA reported values (recent SF_6 emission rates have plateaued since 2015) [14, 15]. Note: SF_6 emission rates may be underreported by a factor of two, as one study suggested, based on atmospheric concentrations [9]

still uses SF_6, potentially locking in this potent greenhouse gas in the grid for the next 20–50 years and increasing the risk of future SF_6 emissions. Because of the environmental challenges associated with using SF_6 in the electric grid, a few states, including California and Massachusetts, are updating their legislation to address SF_6 emission reporting and to set new, more stringent, emission limits. Given the age of the equipment, the investment needed to update and expand the grid, and the stricter policy measures, new technologies and/or alternative gases that minimize or eliminate SF_6 and SF_6 emissions from gas-insulated equipment (GIE) will be required.

2 The Search for SF_6 Substitutes

SF_6 is used extensively as the insulating and arc-quenching medium in MV and HV (12–720 kV) electrical power systems due to its high dielectric strength, nontoxicity, nonflammability, chemical inertness, excellent thermal interruption and heat transfer properties, high vapor pressure at low temperatures, and "self-healing" or fast recovery properties when exposed to an electrical arc. It is an excellent and reliable gas for gas-insulated equipment, were it not for its outsized impact on global warming.

The search for SF_6 alternative gases with a lower environmental impact has been an area of focus for decades [16]. The most critical property for alternative insulating gases is a high dielectric strength, implying that the gas molecules are

Table 18.1 Relative DC uniform field breakdown strengths, V_s^R, of some dielectric gases[a]

Gas	V_s^R [b]	Comments
SF_6	1	Most common dielectric gas to date besides air
C_3F_8	0.90	Strongly and very strongly electron-attaching gases, especially at low electron energies
n-C_4F_{10}	1.31	
c-C_4F_8	~1.35	
1,3-C_4F_6	~1.50	
c-C_4F_6	~1.70	
2-C_4F_8	~1.75	
2-C_4F_6	~2.3	
c-C_6F_{12}	~2.4	
CHF_3	0.27	Weakly electron-attaching; some (CO, N_2O) are effective in slowing down electrons
CO_2	0.30	
CF_4	0.39	
CO	0.40	
N_2O	0.44	
Air	~0.30	
H_2	0.18	Virtually non-electron-attaching
N_2	0.36	Non-electron-attaching but efficient in slowing down electrons
Ne	0.006	Non-electron-attaching and not efficient in slowing down electrons
Ar	0.07	

[a]See also Table 2 in Christophorou and Datskos [111]
[b]Some values are for quasi-uniform fields and may be somewhat lower than their uniform field values

strongly electronegative. Practically speaking, the dielectric strength of the gas is an indication of its ability to reduce the number of free electrons in an electrically stressed dielectric gas. An appropriate substitute, therefore, must be able to scavenge free electrons with a wide range of energies and over a range of temperatures, have favorable electron slowing down properties which reduce additional electron generation from electron impact ionization, and be characterized by a low ionization cross-section/high ionization onset [17].

If the only concern for an SF_6 alternative was the dielectric strength, several alternatives would have been identified decades ago. As can be seen from Table 18.1, which has been reproduced from a 1997 NIST report, there are several gasses with higher dielectric strengths than SF_6.

However, the many gases with high dielectric strengths were ruled out because they did not meet other performance requirements [17]. In addition to dielectric strength, gas insulators must have a high vapor pressure to ensure they stay in the gas phase, even at low temperatures. They must have high thermal conductivity, high specific heat, and long-term thermal stability (i.e., no significant degradation when exposed to elevated temperatures over long periods of time) which is essential for managing the significant thermal loading during an arcing event. They must

also feature high breakdown voltages under uniform and nonuniform electric fields, be robust to factors like surface roughness or moisture content, and be compatible with the materials of construction used for gas-insulated equipment. For safety reasons, gas insulators must be nonflammable and nonexplosive and must have low toxicity to minimize adverse impacts during gas handling or in the event of a gas leak. The chemical compatibility and toxicity levels of the breakdown products after a gas insulator is exposed to an arc must be considered, as these will impact performance and safety over the lifetime of the gas-insulated equipment. These stringent performance and property requirements, on top of environmental considerations like a low GWP and zero ozone depletion potential (ODP), have challenged the search for a suitable gas insulator alternative to SF_6 for decades.

Early candidates considered as possible SF_6 substitutes included carbon dioxide, nitrogen, and mixtures of carbon dioxide and/or nitrogen with SF_6 [17]. A key driver in selecting mixtures based on SF_6 was to find a "universal" drop-in replacement that could be used across all types of gas-insulated equipment with only minor equipment modifications. For some applications, like gas-insulated transmission lines, comparable performance with modest increases in gas pressures relative to pure SF_6 were observed for 50/50 and 40/60 SF_6-N_2 mixtures with the added benefit of slightly lower GWP and lower cost [18–21]. Under some conditions like nonuniform fields or in some interrupter applications, mixtures of SF_6-N_2 were even found to confer superior performance over pure SF_6 due to factors like nitrogen's better insulating properties at high pressures or because nitrogen has complimentary thermal properties at temperatures below 3000 K relative to SF_6 which is better at temperatures higher than 3000 K [22, 23]. However, SF_6 mixtures or pure N_2/CO_2/dry air were found to not be compatible as drop-in replacements for gas-insulated substation circuit breakers and switchgear without a significant thermal derating or redesign [24]. Additional concerns were raised regarding safety issues associated with the rate of pressure rise during an internal failure arc and additional costs associated with gas mixture recycling. It is perhaps because of these and other drawbacks that rollout of these early SF_6 alternatives was limited to MV (12 kV/24 kV) in the case of N_2 and dry air and HV gas circuit breakers up to 72.5 kV for CO_2 [25].

Later research sought to identify alternatives beyond gases like nitrogen and carbon dioxide. One study by Rabie and Franck compared the dielectric strength of SF_6 to 2611 carbonyl compounds as a preselection process to identify potential SF_6 alternatives [26, 27]. They focused their search on groups of hydrofluoro-ketones and hydrofluoro-aldehydes, acyl fluorides, and perfluoro-ketones and perfluoro-aldehydes. Figure 18.2 shows the 2611 molecules grouped into three classes of C_3-, C_4-, and C_5-carbonyl compounds and their predicted dielectric strength (E_r) relative to SF_6 and T_B, the molecules' boiling point. The most promising candidate molecules, due to their relatively high values of E_r and low values of T_B, are captured in the black box. Fluorinated compounds have been of particular interest, in terms of their favorable dielectric strengths, but most had key drawbacks like high GWPs (5000–12,000 for perfluorocarbons) and/or high toxicity (CF_3I) which excluded them from further consideration. Two of the most

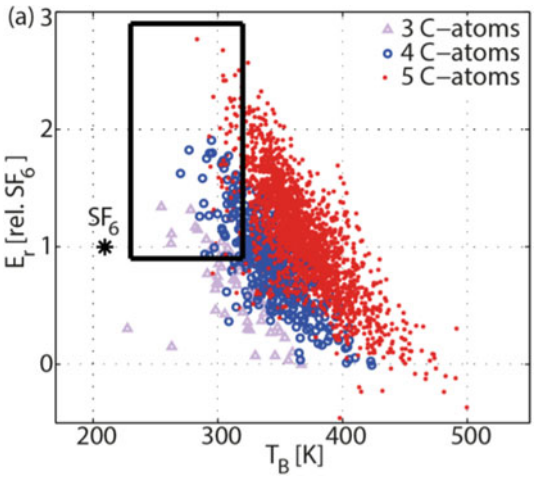

Fig. 18.2 Predicted dielectric strength E_r vs predicted boiling point T_B for 2611 carboxyl compounds. The complete list of molecules is split into carbonyl compounds containing three (triangles), four (circles), and five carbon atoms (dots) [27]

promising fluorinated compounds are a fluoronitrile (C_4F_7N or $(CF_3)_2$-CF-CN) and a fluoroketone ($C_5F_{10}O$ or $CF_3C(O)CF(CF_3)_2$) which have acceptable GWPs and low toxicities [25, 28]. Both are currently marketed under 3 M's Novec™ dielectric gases, Novec™ 4710 and Novec™ 5110, as SF_6 gas alternatives for power utility applications.

Original equipment manufacturers (OEMs) are currently testing mixtures based on the Novec™ dielectric fluids in high-voltage electrical equipment. For example, GE developed green gas for grid (g^3) using CO_2 and O_2 mixed with Novec™ 4710 for gas-insulated substation (GIS) and gas-insulated line (GIL) applications [29]. Testing to assess the performance of g^3 gas in 60 bays of 145 kV gas-insulated substations, over 2000 meters of 420 kV gas-insulated lines, and in 6 AIS 245 kV current transformers has produced promising results. ABB has also developed AirPlus™, which combines dry air with Novec™ 5110, for GIL and GIS applications.

Zhang et al. recently reviewed studies that have modeled and experimentally characterized the arc plasma and decomposition products of the Novec™ gas mixtures [25, 30]. The basic properties of the arc plasma produced from mixtures of C_4F_7N and $C_5F_{10}O$ are critical for understanding arc plasma behavior and evaluating arc-quenching capability. The main takeaway from a comparison of the composition of the arc plasmas calculated assuming local thermodynamic equilibrium conditions (LTE), non-LTE but local chemical equilibrium condition (LCE), and using chemical kinetics models with no equilibrium assumptions reveals a discrepancy at low temperatures. Chemical kinetics are more critical for low-temperature conditions where the impact of energy barriers for each decomposition pathway is expected to dominate; LTE assumptions ignore the influence of energy barriers. Regarding the decomposition products, the recognition that, unlike SF_6, the decomposition by-products of the proposed gas mixture alternatives do not recombine to form the original structure has necessitated studies that characterize

the decomposition products under thermal degradation, spark discharges, corona discharges, and arcing. To this end, researchers have conducted experimental studies to characterize the decomposition products directly and developed computational models to understand the chemical kinetics and decomposition mechanisms [29, 31–46]. Erroneous or incongruous results are still prevalent, however, due to the limitations of the chosen methods. The detection methods most often used in experimental studies that characterize the gas composition are Fourier transform infrared spectroscopy (FTIR) and gas chromatography-mass spectroscopy (GC/MS). FTIR enables in-line gas composition analysis but is limited by a relatively high detection threshold. Conversely, GC/MS is excellent for detecting trace gasses but introduces a significant time delay, so the decomposition products are detected when they are no longer under their formation conditions. In the case of computational methods, the accuracy will necessarily depend on the input assumptions which should be documented carefully and provided with adequate rationale.

A few studies from the last decade focus on the materials compatibility of C_4F_7N and $C_5F_{10}O$ and their decomposition products with metals, metal oxides, common elastomers, and lubricating greases. Early computational results indicate, for example, that C_4F_7N may be more compatible with aluminum than copper, while experimental results from Pohlink et al. found no serious compatibility issues among the most common metals used in HV equipment over a period of several months at 120 °C [32]. The most prevalent compatibility issues for both C_4F_7N and $C_5F_{10}O$ were associated with polymers, particularly ethylene propylene diene monomer (EPDM) which is used as a gasket/sealing material. C_4F_7N can also have an effect on the degradation of other common materials found in circuit breakers such as nitrile O-rings and synthetic zeolite molecular sieves used to remove decomposition by-products [47]. In addition to material incompatibilities, the different decomposition pathways of these gases are important in order to design molecular sieves to capture by-products and to preserve the integrity of the dielectric and cooling properties of the gas in the chamber. In summary, research regarding arc plasma behavior, decomposition products, and materials compatibility are still at the early stages for both C_4F_7N and $C_5F_{10}O$ but are critical to understand before moving entirely away from SF_6.

Although potential gas alternatives like those previously mentioned are promising, several challenges exist in accomplishing full replacement of SF_6. Though some of the proposed alternatives can reduce the GWP by over 98% relative to SF_6, a 98% reduction still leaves many alternatives with a GWP >300 [48]. What's more, alternative gas and gas mixtures are not necessarily drop-in solutions for SF_6 under all conditions; some gas mixtures pose a potential performance risk in colder climate zones due to their higher boiling points, while some gas mixtures require modest increases in pressure to achieve equivalent performance to SF_6 [49]. Alternative gases and gas mixtures may require new or modified equipment specially designed to use these gases, new leak detection and monitoring equipment, and new practices to address end-of-life disposal or recycling. Like the work described earlier related to arc plasma characterization and decomposition products, toxicological studies are also at the beginning stages and reflect conflicting results, though some initial

results are promising [28]. Finally, there is still a degree of uncertainty around the potential of future regulations which may impact adoption. Even if these points are addressed, market adoption will require overcoming challenges associated with workforce training and spacing constraints, in addition to the need to assess the connection compatibility with existing equipment/infrastructure.

A final comment regarding vacuum dry air or vacuum solid dielectric circuit breakers as another route to SF_6-free electrical equipment will be made, which is the route that OEMs like Siemens and Mitsubishi are currently pursuing [50]. A vacuum is used as the arc-quenching medium and insulator between the contacts as part of a vacuum interrupter (VI) and either dry air or a solid dielectric as the insulator around the VI and in the bushings, eliminating the need for SF_6 or related gases entirely. Several manufacturers already have vacuum technologies for 38 and 72.5 kV, while technologies at 145 kV are expected to become available within the next year. Although these vacuum or near-vacuum technologies have a higher dielectric strength compared to SF_6 circuit breakers, OEMs consider scaling to higher voltages (i.e., 245 kV) a difficult technical challenge.

3 SF_6 Life Cycle Considerations

There are other considerations in the life cycle of the equipment beyond developing alternatives for SF_6-insulated GIE. One of the most effective strategies for mitigating SF_6 emissions in existing equipment is to detect leaks early and to fix these quickly. The International Electrotechnical Commission sets the maximum allowable leakage rate of SF_6 at 0.5% per year [51]. Most new equipment achieves leakage rates far below this limit, but as the equipment (which has a useful lifetime of several decades) ages, the leakage rates may exceed 0.5% per year. To achieve this stringent requirement, it is necessary to continuously monitor for leaks; IEEE Guide for the Selection of Monitoring for Circuit Breakers also recommends monitoring SF_6 density which can fluctuate in response to thermal fluctuations. Several technologies are currently available on the market including portable point source nondispersive infrared (NDIR) detectors, NDIR room sensors which detect ppb and ppm SF_6 concentration levels in enclosed GIE substations, and pressure gauges interfaced with alarm systems that monitor changes in pressure in GIE [52–57]. While these technologies are mature and widely available, further improvements in continuous, sensitive, early-warning detection systems are merited. Developing sensors that combine lower cost, higher sensitivity, and continuous monitoring for all equipment settings could lead to advances in early detection technologies that reduce SF_6 emissions in the short and medium term as the electric grid transitions to non-SF_6 alternatives as well as lead to more accurate accounting of emission rates. Of particular interest are cost-effective detection technologies with remote notification systems or systems sensitive enough to detect slow leaks in small-capacity gas-insulated equipment which pose unique challenges that demand low detection limits and high accuracy under a variety of environmental conditions.

Today's continuous sensors primarily rely on pressure gauges that are not sensitive enough to detect slow leaks or leaks in small-capacity equipment. As a result, even with the technology that is on the market today, several small-capacity GIE owners responded to the proposed policy changes in the California legislation by noting that achieving 1% emission rates on a consistent basis is challenging [58]. One percent emission rate still corresponds to the equivalent of at least 1 megaton of CO_2 released per year in the United States; these emissions could potentially increase fivefold by the year 2035 if SF_6 nameplate capacity continues to increase at an average of 4% per year and the emission rate stay the same.[1] NDIR-based sensors offer higher sensitivity than pressure gauges, but they currently have several drawbacks. NDIR point source sensors are more sensitive and can detect ppm or ppb SF_6 concentrations but are not continuous, are cost-prohibitive, and require a technician to manually check all equipment for leaks. NDIR room sensors can continuously monitor dilute SF_6 concentrations but are still costly and are only applicable for equipment housed in an enclosure. Density and pressure sensors carefully located at optimal locations on the equipment and potentially supplemented with CFD models may enable NDIR-level accuracy at a similar cost and robustness of pressure gauges, thereby leading to more accurate leak rate monitoring [51]. Looking longer-term, cost-effective sensors for proposed gas and gas mixture alternatives will be required because the alternative gases on the market today have a GWP potential that is lower than SF_6 but still significant when compared with other greenhouse gases [59, 60]. Of note, alternatives based on gas mixtures may demand higher accuracy or bespoke sensors to monitor the conditions of the gas-insulated equipment where risks of changes in mixture composition will have major implications on the equipment operation. The gas composition must be always known to ensure the dielectric gas is within a safe operational window.

In addition to leak detection, there are other items to consider when using SF_6 alternatives. The characteristics of SF_6 replacements dictate changes to the mechanical structure of the breaker to accommodate variations in pressure and dielectric withstand. Because of this, several studies have been published regarding the life cycle impact of the manufacture, use, and disposal of the new GIE hardware. For example, hardware changes required for Novec 4710™ mixtures for a 145-kV, 40-kA breaker were found to have minimal impact relative to the equivalent SF_6-based switchgear when accounting for the emissions and waste generation from production of material, manufacturing, distribution, construction, operation and maintenance, and end-of-life destruction [61]. In contrast, while vacuum-based breakers will not have any deleterious emissions during use, compared to a Novec 4710™ -based circuit breaker, researchers in [62] conclude that the need for larger

[1] The emissions are estimated by using a 1% emission rate on the reported and projected SF_6 nameplate capacities (see Fig. 18.1). Of note, the EPA does not require SF_6 emission reporting for utility operators with a combined total of 17,820 lbs. SF_6 nameplate capacity, and therefore, the numbers available for nameplate capacity may not be complete.

equipment (a direct result from the vacuum's lower dielectric strength), the GWP, among other negative factors, is higher for vacuum-based breakers at 72.5 kV.

Finally, novel end-of-life processes for SF_6 must be considered as SF_6-insulated equipment is retired and replaced with non-SF_6 alternatives. While SF_6 is available, it poses a significant environmental risk. This represents an opportunity to develop novel SF_6 destruction pathways which are less energy-intensive and do not produce toxic and/or corrosive products [63–65]. Alternative pathways for efficient and complete destruction of SF_6 use strong reducing agents [66–68], low-valent transition metal complexes [69–76], strong nucleophiles [77], monovalent aluminum reagents [78], and catalytically enhanced dielectric barrier discharge processes [79]. A more recent approach has been to use SF_6 as a safe fluorinating agent in organic synthesis, opening new valorization routes for stranded SF_6 supplies when it is no longer needed in electrical equipment [70, 80–86]. For alternative gas and gas mixtures, end-of-life considerations are in their nascent stage.

4 SF_6-Free Circuit Breaker Hardware

Alternative dielectric mediums in HVAC switchgear and near drop-in replacements for SF_6 require changes to the system hardware that can involve significant research, development, design, and testing. While allowing for more significant hardware redesigns offers more options for dielectric mediums, trade-offs in size and life cycle impacts must still be taken into account. Ensuring safety aspects are considered and that the dielectric withstand capability of the circuit breakers can still pass power frequency, lightning impulse, and chopped wave dielectric tests according to IEEE C37-04 or other standards is also critically important when any changes to dielectric medium or hardware are made. Dynamic tests such as those in IEEE C37-04 serve to verify fundamental performance parameters critical for any new design such as how to extinguish the arc quickly and safely and ensure a speedy and full dielectric recovery. For reference, an example of a high-voltage SF_6-based dead tank AC breaker and a corresponding bushing and tank cutaway is shown in Fig. 18.3.

One of the initially more attractive options for SF_6-free switchgear is vacuum-based circuit breakers due to their ease of maintenance and zero GWP [88]. While vacuum interrupters (VI) perform well at lower voltages, at voltages above 72.5 kV, as a result of practical design limitations, there can be diminishing returns for increased gap lengths [89, 90]. As a result, multibreak VI designs are often proposed as a solution though this is still an active area of research and considerations for voltage balancing between the sets of electrodes, such as grading capacitors, must be considered [91]. Other active areas of research for increasing a single VI's interruption capabilities particularly beyond 72.5 kV are similar to those for other mediums such as new contact materials and geometries, improved speed and control of operating mechanisms, new solid insulator material, and improved designs for electric field control [92–95]. For dead tank breakers, an insulating medium must also be used in the tank that contains the VI as well as the bushings. While technical

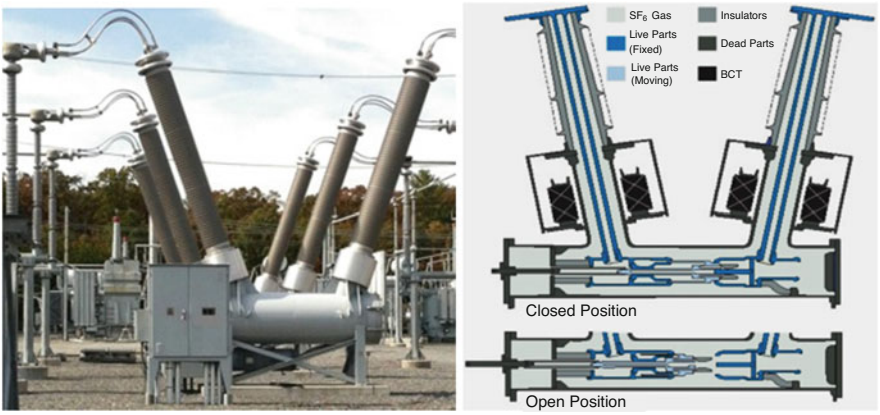

Fig. 18.3 Example of three-phase HVAC dead tank breaker (left) and cutaway drawing of example chamber, bushings, and contacts for a single phase (right) [87]

air is a common choice, VIs with technical air insulators could have weights and footprints 132% higher and 160% larger, respectively, than an SF_6 breaker of similar performance [62, 96]. Recent work has also looked at dielectric mediums primarily for the tank and bushings such as CF_3I-CO_2 to improve the footprint of VI-based breakers with technical air while maintaining lower GWP [97].

In [24], researchers demonstrated how non-vacuum dielectric mediums combined with circuit breaker redesigns can achieve design goals while maintaining a low GWP. Using a 72.5-kV breaker redesigned to use a 0.8-MPa CO_2, the researchers reduced the GWP of the circuit breaker significantly while still meeting the key fault and capacitive switching requirements of IEC 62271-100. The redesign included accounting for the lower heat capacity of 0.8 MPa CO_2 which causes a more rapid pressure rise and fall than SF_6 at similar starting temperatures and pressures. As a result, the CO_2 puffer pressure may not be adequately maintained for long-duration arcs, necessitating a larger puffer cylinder volume. The authors conclude that higher pressures of CO_2 as well as blends with O_2, which has better arc-quenching capability than CO_2, could possibly overcome some of these issues as well as further improve the GWP. Another option for higher-pressure CO_2, as demonstrated in [98], is to use it in its supercritical state. Supercritical carbon dioxide ($scCO_2$) at around 8 MPa has a dielectric strength of around three times that of SF_6 in addition to high heat transfer capability and low viscosity. $scCO_2$-based breakers have already been proposed for a compact, low-arcing, medium-voltage breaker [99]; however, $scCO_2$ breakers have their own challenges as they require the chamber, bushings, and all external seals to manage the 8-MPa pressure and a well-controlled temperature to maintain the CO_2 at supercritical levels. Additionally, during an AC fault, the great amounts of heat energy released from the arc over the course of several milliseconds or partial cycles could cause more overpressure in the switchgear enclosure and bushings, resulting in rupture. While this phenomenon

has been studied at lower starting pressures for SF_6, CO_2, and N_2 [100], further analysis on the higher operating pressure effects over time and in operation during arcing faults in $scCO_2$ are needed.

In addition to looking to CO_2 at higher pressures, in [101], researchers demonstrated that N_2, with a combination of higher pressures and/or increased sparking distance, can achieve a dielectric insulation equivalent to SF_6 at 0.7 MPa. In [102], researchers further evaluated gaseous nitrogen at pressures up 2.6 MPa and with various mixtures of SF_6 and showed that, for example, with a working pressure of 1 MPa and only 5% SF_6 and 95% N_2, a similar insulation performance could be achieved to SF_6 at its typical working pressure of 0.7 MPa. As has been discussed, for application to circuit breakers, a suitable dielectric medium is dependent on many other variables besides dielectric strength, such as gas flow characteristics and various thermal properties, that should be considered to definitively evaluate the equivalency of the insulating medium as a replacement for SF_6 in switchgear.

Other work has also looked at nongaseous forms of nitrogen. If future substations have available liquid nitrogen (LN_2), then concepts proposed in [103] such as a 126-kV LN_2-cooled superconducting fault current limiter (SCFCL), which reduces the fault current energy, could enable a smaller, cryogenically cooled vacuum interrupter in series which would have the added benefit of an "on" resistance of less than a third of a traditional AC breaker. Alternatively, since LN_2 can have a higher breakdown voltage than SF_6 at its standard operating pressure, LN_2 has been proposed as the dielectric medium in the interrupter itself where it can both serve to greatly reduce steady-state losses due to reduced resistivity of the cryo-cooled contacts and extinguish the arc. In [104], the arc-extinguishing capability of LN_2 was tested up to nearly 3-kA peak with 50-mm-diameter contacts, opening at 1 m/s to reach a 25-mm gap. The LN_2 was shown to help successfully extinguish the arc at the zero crossing without reignition for root mean square currents of less than 2085 A. The two concepts of SCFCL and dielectric medium are combined in [105] where researchers have also proposed and tested at lower voltages with LN_2 as the dielectric medium in the interrupting mechanism combined with a SCFCL. The results indicate the system is fast-acting and results in lower current and therefore lower-energy faults, though many other items, including the hardware redesign, the logistics of cooling the LN_2, and how to deal with any GN_2 that is generated, must be considered. For those that envision liquid nitrogen and cryo-cooled elements as part of the solution for the future grid, demonstrating the value of fault current limiters and liquid nitrogen in switchgear could play a part but may require rethinking of traditional fault coordination systems.

Another area of research as it relates to SF_6 alternatives is in the materials, speed, and movement of the mechanisms that separate the contacts, determine the movement of the arc, and control gas flow. In [106], researchers demonstrate in a low-voltage circuit breaker the use of permanent magnets to help guide the arc toward a splitter stack that elongates and cools it. However, physical prototypes to prove the efficacy of these approaches on high-voltage equipment are costly, and theoretically evaluating the range of possible solutions also proves challenging. The simulation of such systems are complex due the multi-physics phenomena related to flow, pressure, contaminants, electrical operating points, mechanical structures, the

shape and movement of contacts, and dielectric medium management mechanisms. Much research has been done to make the simulation problem more accurate and manageable such as defining the ignition of discharges and their lifetime transitions from corona to streamer or to Townsend avalanches by evaluating the discharge's stability mathematically as an eigenvalue problem [107] or defining an iterative calculation of streamer propagation with a dependence on pressure into an algorithm that helps simplify finite element simulation. A similar effort to simplify simulations in [108] uses computational fluid dynamics and detailed enthalpy flow simulations to determine the discharge coefficients of various geometries of gas valves during the circuit breaker operation that can then be plugged into enthalpy flow models of the full circuit breaker system. The need for high accuracy simulations and the multidisciplinary nature of the problem is apparent even in research related to existing high-voltage switchgear. For example, some 550-kV HVAC SF_6-based breakers must now manage higher short-circuit ratings than ever, such as 80 kA versus a previous maximum of 63 kA, as a result of new grid conditions. This increase in peak fault current is compelling researchers to explore electromagnetic- and mechanical-based solutions that can reduce contact travel time and guide the arc so that it extinguishes more effectively so as to not cause significant changes to equipment size and operation as a result of the increased fault current rating [109, 110].

5 Concluding Remarks

The risks of using SF_6 as the insulating medium on the grid due to its outsized GWP have long been recognized by researchers and regulators. The search for suitable alternatives to SF_6-insulated GIE has spanned decades and only recently has it achieved gains in the form of unique fluorinated gas mixtures, vacuum dielectrics pushing higher voltages, and cryo-insulators. Though early results are promising, there remain many open questions related to the life cycle impacts of new GIE or vacuum-based equipment, the performance of the dielectric medium when exposed to an arc, the safety and monitoring aspects that will be required, and the end-of-life handling practices. With much of the current grid infrastructure approaching end of useful life, the introduction of new renewable energy generation to the grid, and upcoming policy mandates, the need for alternatives to SF_6-insulated GIE has never been greater. Addressing these questions, analyzing the findings from ongoing pilot studies, and anticipating future needs for SF_6 alternative technologies are sure to be a top priority for stakeholders in this space and will be critical for achieving a zero-emission grid.

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Part V
Future Outlook

Chapter 19
Fundamental Challenges and Future Outlook

Z. John Shen

1 Fundamental Challenges

Electricity, in its predominant form of alternating current (AC), is at the heart of modern civilization. However, direct current (DC) electricity is re-emerging, long after losing the *War of Currents* over a century ago. DC inherently offers higher transmission efficiency, better system stability, better match with modern electrical loads, and easier integration of renewable and storage resources than AC [1]. DC power is gaining tractions in HVDC or MVDC grids, DC data centers, photovoltaic farms, EV charging infrastructures, and shipboard and aircraft power systems. However, fault protection must be provided that can simultaneously meet the power loss, response time, and cost requirements of the future DC grids.

Interruption of DC currents is extremely difficult due to the lack of current zero crossings which are naturally available in AC power systems. Presently, solid-state circuit breakers (SSCBs) can quickly interrupt a DC fault current within tens of microseconds but suffer from high conduction loss and weight and cost penalty associated with the cooling and semiconductor components. The subject of SSCB is discussed in detail in many survey papers such as [2–5] as well as other chapters of this book. The most distinct advantage of semiconductor devices is their capability of current switching or state changing, while the most distinct disadvantage is their nonnegligible on-resistance and conduction loss when conducting current. Unfortunately, they are used in the SSCBs in the worst way possible—continuously dissipating power except during infrequent fault interruption throughout their service life. This is in stark contrast to digital CMOS transistors that incur a power loss only when actively engaging in logical operations. It would be highly desirable

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to reverse the role of the power devices in future circuit protection solutions, that is, turning on only during the brief and infrequent fault interruption process and otherwise staying off under normal operation.

Alternatively, numerous hybrid circuit breaker (HCB) schemes were reported to offer an on-state resistance orders of magnitude lower than that of SSCBs, such as those discussed in survey papers [6, 7] as well as other chapters of this book. All the HCBs are of parallel-type (although the term "parallel-type" is never explicitly used), in which an electronic path is in parallel with a main mechanical switch or breaker. The fault current in the mechanical path is initially commutated to the electronic path to create artificial current zero crossings in various forms to aid the opening of the mechanical contacts with reduced or no arcing. The electronic path will then be interrupted arclessly. However, these parallel-type HCBs offer only a moderate fault response time of several milliseconds, which may be too slow to limit the fast-rising fault current in many low-impedance DC power networks. For example, the fault current *di*/*dt* of a 10-kV MVDC system with a loop inductance of 1 mH is approximately 10 A/μs. This would allow the fault current to rise dangerously by 10 kA with a delay time of 1 ms, causing excessive stress to the power system. The most distinct disadvantage of all parallel-type HCBs is their relatively long opening time of the mechanical contacts, which is fundamentally limited by the finite amount of force applied to the contacts of a certain mass. During the contact opening process, the fault current continues to rise through the electronic path in parallel, not only stressing the power system but also accumulating significant amount of electromagnetic energy that needs to be dissipated when the electronic branch finally turns off. It would be highly desirable to curtail the total fault current (ideally to zero or near zero) throughout the entire opening process of the mechanical contacts in future HCB solutions.

2 Series-Type HCB (S-HCB) Concept

While combining low on-resistance of mechanical contacts and arcless or arc light interruption of DC fault current electronically in parallel-type HCBs is truly advantageous, we may need to look into alternative ways to reduce their response time and peak fault current. In this section, we will introduce a new concept of series-type HCB or S-HCB, which places the main mechanical switch in series with an electronic circuit that injects a counter voltage against the DC source voltage.

An early example of S-HCB, although not named in such term, placed a coupled inductor in series with a mechanical switch (MS) [8]. The series inductor injects a counter voltage from a pre-charged capacitor by turning on a control thyristor under a fault condition and induces a zero current crossing so the series MS is supposed to open arclessly. Unfortunately, the opening of MS must precisely coincide with the current zero crossing to realize true zero current switching. Otherwise, the MS will open under a large positive current if opening too soon or a large negative current if opening too late, resulting in arcing in either case. In practice, this is a

nearly impossible to realize since the timing control of a mechanical switch (e.g., a solenoid or Thomson coil) is typically on the order of hundreds or thousands of microseconds, much slower than the power electronic circuit. This limitation is mainly due to the single-shot and unregulated nature of the thyristor-based counter current injection circuit in [8]. Nevertheless, the S-HCB topology can help extinct the arc of the mechanical switch with the artificially generated zero crossing if the mechanical switch is allowed to open before the counter voltage injection. A similar topology, termed current commutation drive circuit (CCDC), was proposed earlier [9] and later on adopted into a 500-kV/25-kA parallel-type HCB [10] as was discussed in Chap. 13 of this book.

A true arcless series-type hybrid circuit breaker (S-HCB) architecture was recently invented and demonstrated to provide DC fault interruption with ultrafast response (<10 μs) and ultralow conduction loss [11, 12]. The true S-HCB concept is distinct from any SSCB since its load current does not flow through any power semiconductor switch. The power semiconductor switches are only activated during a fault event, and thus do not incur any power loss under normal operation. It is distinct from any parallel-type HCB since its total fault current (same as the MS current) is forced to zero within a few μs after fault detection and remains at or near zero throughout the entire interruption process, offering μs-scale fault protection. It also differs from the series-type HCB reported in [8] since it actively regulates the fault current into a small high-frequency AC ripple current for a few hundreds of μs and does not need to precisely synchronize the MS opening with a single zero current crossing occurrence. The S-HCB offers the low on-resistance of conventional mechanical contacts for normal operation and μs-scale fault response that is even notably faster than fast-acting SSCBs since it does not need to dissipate the residual electromagnetic energy as in most of the SSCB cases. The basic operation principle, simulation, and experimental proof-of-concept work of the S-HCB are discussed next.

Figure 19.1 shows the notional schematic of SSCB, conventional HCB (parallel-type), and S-HCB (series-type) with all three having a series mechanical disconnect switch SW to provide galvanic isolation and system reconfigurability after the initial fault interruption. The S-HCB comprises a pulse transformer with its primary winding connected to a power electronic voltage injection (VI) circuit and its secondary winding in series with the main DC power bus. Under normal operation, the S-HCB conducts a DC load current through the properly sized secondary winding with a low power loss. The primary side VI circuit is not activated and thus does not incur any power loss other than the standby power consumption of the sensing and control circuitry. Under a fault condition (i.e., overcurrent in the main power bus), the S-HCB injects a transient voltage via the pulse transformer into the main DC power loop by activating the VI circuit and discharging its pre-charged capacitors. This transient secondary voltage exceeds the system DC voltage and drives the fault current to zero within a very short time period (<10 μs), which defines the fault interruption time of the S-HCB. The power electronic VI circuit then operates in a PWM mode to regulate the secondary current (i.e., the fault current) into a small AC ripple current for the next 100–500 μs, allowing the

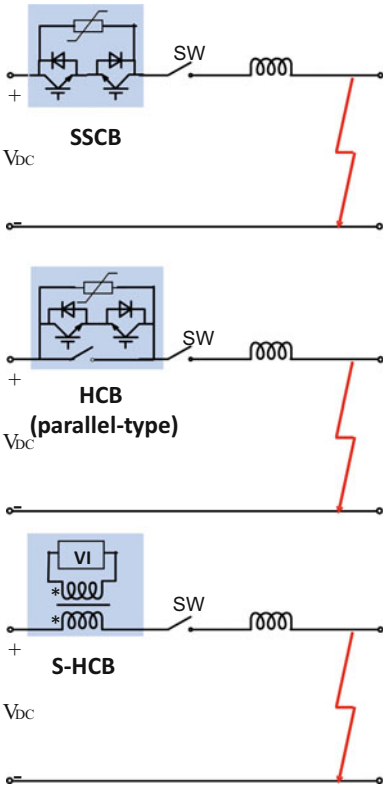

Fig. 19.1 Simplified schematic of SSCB, HCB (conventional parallel-type), and S-HCB (series-type) in a DC power system with a short-circuit fault [10]

series mechanical switch to open safely and isolate the fault. The S-HCB is distinct from SSCBs because there is no semiconductor-related power loss under its normal operation. The S-HCB is also distinct from HCBs since its total fault current is held near zero throughout the entire fault interruption process.

Figure 19.2 shows a detailed circuit schematic of the S-HCB concept under three distinct operation modes. The S-HCB comprises two capacitors, C1 and C2; two power transistors, Q1 and Q2; two diodes, D1 and D2; and a pulse transformer, T1. Note that the magnetizing inductance is shown in the transformer model, but the leakage inductances are not for the sake of simplicity. Upon detection of an overcurrent, the VI circuit is activated from a sleep mode by turning on Q1 and Q2 to discharge pre-charged capacitors C1 and C2 and quickly injects a transient step voltage via the transformer T1. This transient step voltage is designed to exceed the DC voltage in the main circuit loop and forces the fault current to zero within a very short time (<10 μs). Subsequently, Q1 turns on and off in a PWM mode to alternately apply a higher voltage (C1 and C2 in series as in Mode A) or a lower voltage (C2 only as in Mode B) across the primary winding of T1. The pulse-width modulation (PWM) switching of Q1 causes the transformer secondary voltage to fluctuate around the DC bus voltage and therefore holds the fault current to a near-

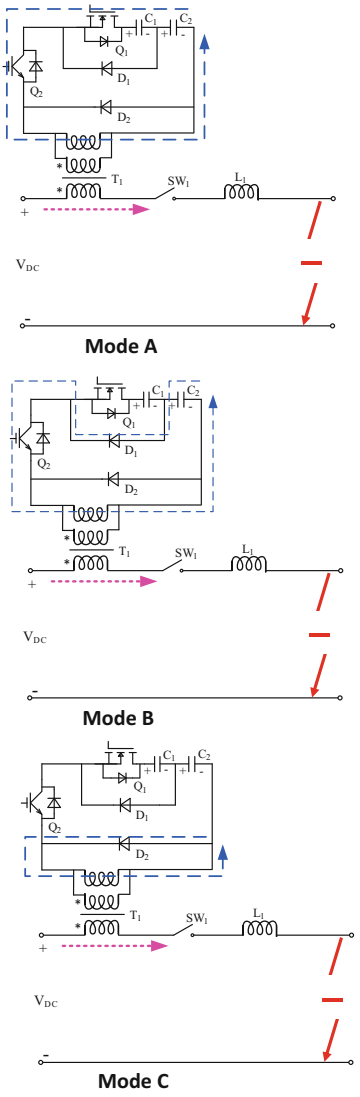

Fig. 19.2 Different operation modes with the marked internal current flow of the S-HCB during fault interruption. The pre-charged capacitors C1 and C2 are discharged in a controlled manner so the secondary current (fault current) can be driven to and held near zero while the mechanical switch SW1 opens [10]

zero small AC ripple current during the next 100–500 μs. The series mechanical switch SW1 then opens under a near-zero current and near-zero voltage condition and galvanically isolates the faulty branch without arcing. Q1 and Q2 then turn off and allow the electromagnetic energy stored in the magnetizing inductor of T1 to slowly dissipate via the freewheeling diode D2 (Mode C). The major difference between this work and the HCB reported in [8] is that the fault current is actively regulated in a PWM mode as a small high-frequency AC ripple current for a long

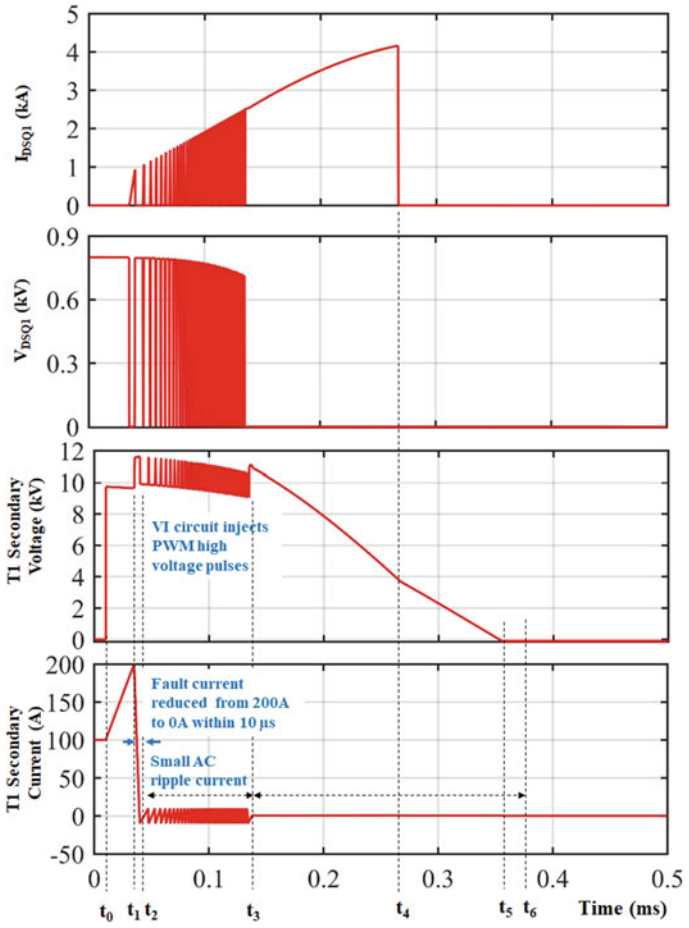

Fig. 19.3 MATLAB/Simulink simulated operation of the proposed S-HCB based on a 10-kV/100 A case study [10]

time period so the MS can open arclessly. There is no need to precisely time the MS with a single zero current crossing.

The S-HCB concept is validated by MATLAB/Simulink simulation for a case study of a DC voltage of 10 kV, nominal current of 100 A, fault current threshold of 200 A (2× nominal), system loop inductance of 100 µH, initial C1 voltage of 800 V, initial C2 voltage of 2500 V, transformer primary inductance of 150 µH, secondary inductance of 2.4 mH, and a turn ratio of 4 (assuming an ideal coupling coefficient k of 1), as shown in Fig. 19.3. Prior to t_0, a nominal current of 100 A flows from the DC power supply (left) to the load (right) in the main circuit loop, and the S-HCB is inactive with C1 and C2 already pre-charged to 800 and 2500 V, respectively. Note that the load current is also the secondary winding current of the transformer

T1. At t_0, a short-circuit fault occurs and the fault current increases rapidly. Note that the secondary self-inductance of T1 spontaneously produces a high counter transient voltage slightly below the DC voltage and effectively limits the rate of rise of the fault current even before the power electronic VI circuit is activated. At t_1, a fault current of 200 A is detected, and the S-HCB is then activated by turning on Q1 and Q2 to discharge C1 and C2. The S-HCB, now operating in Mode A of Fig. 19.2, suddenly applies a step voltage of 3300 V (the total voltage of C1 and C2 in series) across the primary winding of T1, subsequently inducing a transient secondary voltage of approximately 11,600 V. This transient secondary voltage, now exceeding the DC voltage of 10,000 V, forces the fault current to decrease rapidly.

At t_2, the fault current is reduced to zero. The time interval between t_1 and t_2 represents the fault interruption time of the S-HCB and is shown to be less than 10 μs in this example. The S-HCB drives the fault current to zero even faster than an SSCB because it does not need any metal oxide varistor (MOV) energy absorption time. Instead, the system electromagnetic energy is transferred to T1 during the fault interruption process. Between t_2 and t_3, Q1 switches off and on in a PWM mode to maintain a small AC ripple current in the T1 secondary winding. When Q1 is on, the S-HCB operates in Mode A in which both C1 and C2 are discharged through Q1 and Q2. When Q1 is off, the S-HCB operates in Mode B in which only C2 is discharged through D1 and Q2. Note that Q1 needs to switch only between zero and the C1 voltage (maximum of 800 V in this design example) and therefore has a much lower voltage rating (1.2 kV) than Q2 which needs to hold off the total voltage of C1 and C2 (3.3 kV).

At t_3, the mechanical switch SW1 opens under a near-zero current condition. Mechanical switches such as commercial vacuum interrupters can safely interrupt AC ripple currents. At this point, the S-HCB operates in Mode A again to discharge C1 and C2 entirely through the magnetizing inductor of T1 since the secondary winding current is completely cut off by the opening of SW1. Interestingly, the voltage across the contact gap of SW1 increases gradually as the T1 secondary voltage decreases gradually with C1 and C2 being discharged. This is an advantage in preventing arcing and establishing the voltage blocking capability of SW1 without requiring an unreasonably fast opening time of SW1. At t_4, Q1 turns off and D1 turns on to discharge C2. The S-HCB now operates in Mode B. At t_5, Q2 turns off, and D2 turns on to slowly dissipate the electromagnetic energy stored in T1. The S-HCB now operates in Mode C. At t_6, SW1 fully opens to block the full DC voltage. The fault interruption process is now completed. Table 19.1 summarizes performance comparison between SSCB, HCB, and the new S-HCB technologies based on a case study of 10-kV/100 A power ratings.

A 600-V/30-A proof-of-concept prototype is designed and built based on the proposed S-HCB concept as shown in Fig. 19.4. A key component of the S-HCB is the pulse transformer, which operates very differently from conventional power transformers, and has unique design requirements. The transformer primary current remains zero under normal operation but becomes a very high transient pulse current of several hundred amperes over a short time period of several ms during fault interruption. It can therefore use copper wires or tapes with a significantly lower

Table 19.1 Performance comparison between S-HCB, HCB, and SSCB of 10 kV/100 A

Performance	S-HCB	HCB	SSCB
Interruption time	~10 μs	>1000 μs	~100 μs (limited by MOV time)
Conduction loss	<10 W	<10 W	~5000 W
Summary	Low loss, ultrafast interruption, needs no additional isolation switch	Low loss, slow interruption, needs one additional isolation switch	High loss, fast interruption, needs one additional isolation switch

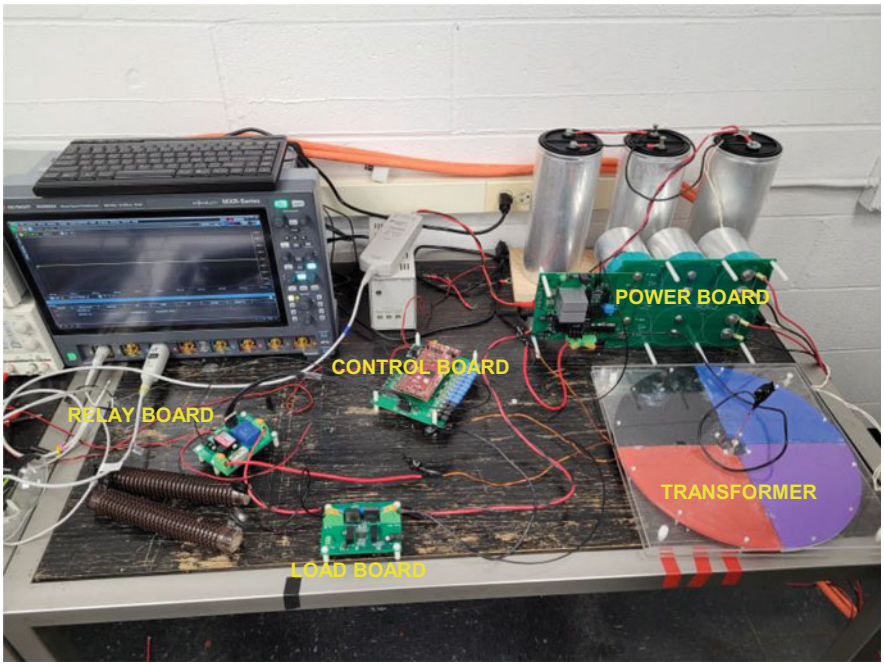

Fig. 19.4 A 600-V/30-A proof-of-concept S-HCB prototype using a package-type pulse transformer

DC current rating. For example, the temperature rise of a 20 A-rated 14-AWG copper wire under a pulse current of 600 A for 60 ms is estimated only 25 °C using a transient temperature calculation model. The secondary winding of the transformer, however, continuously carries the main DC current and must have a low DC resistance. In our ongoing research of 10-kV/150-A S-HCB for turboelectric aircraft MVDC power systems, high-temperature superconducting (HTS) materials and cryogenic cooling are considered for the secondary winding. However, for the 600-V/30-A proof-of-concept prototype reported in this chapter, 17 turns of 14 AWG and 92 turns of 16 AWG copper wires are used for the primary and secondary windings, respectively. An air-core pancake-type transformer structure is adopted to

Table 19.2 Parameter and component list of 600-V/30-A S-HCB

Parameters	Symbol (Fig. 19.2)	Value	Comments
DC voltage	V_{DC}	600 V	DC bus voltage
Transistor 1	Q1	650 V/120 A, 4×	SiC JFET (F3S-C065007K4S)
Transistor 2	Q2	1200 V/150 A, 4×	IGBT (IKY75N-120CS6XKSA1)
Capacitor 1	C1	250 V, 800 μF × 3	Film capacitor
Capacitor 2	C1	150 V, 800 μF × 3	Film capacitor
Transformer	T	L1 of 85 μH, L2 of 1.25 mH, M of 302 μH, S/P ratio of 6.6	Custom made

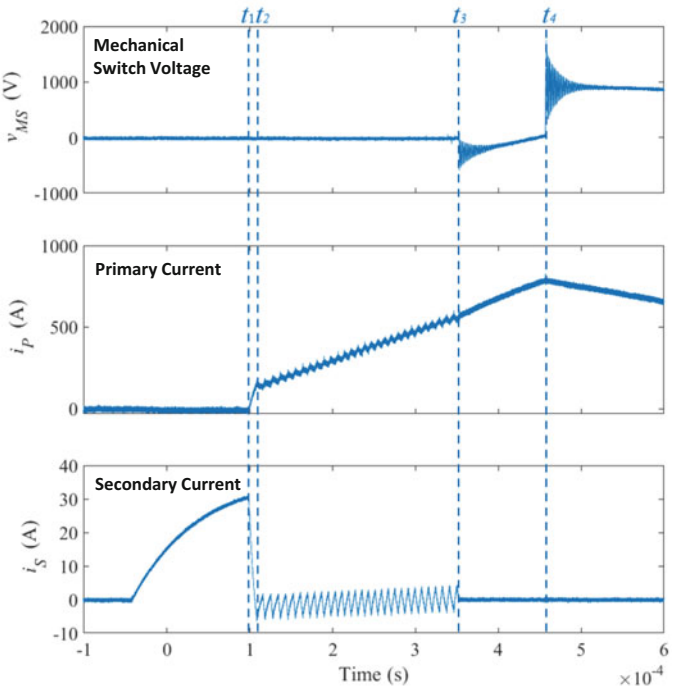

Fig. 19.5 Measured transformer secondary and primary current and mechanical switch voltage waveforms of the S-HCB prototype during a short-circuit interruption under a DC voltage of 600 V

avoid core saturation caused by the high primary current. The custom-made pulse transformer exhibits a primary self-inductance of 85 μH, secondary self-inductance of 1.25 mH, and mutual inductance of 302 μH. Other major circuit components in Fig. 19.2 are listed in Table 19.2. Note that none of the power devices conduct current under normal operation.

The S-HCB is tested for its short-circuit response in a capacitor discharge circuit with a DC voltage of 600 V. Figure 19.5 shows the measured waveforms of the transformer secondary and primary current and the voltage across the mechanical switch (a commercial 2-kV RF vacuum relay) during the short-circuit interruption process. It is clearly shown that the fault current is forced to decrease from 30 A to 0 between t_1 and t_2 in less than 10 μs which defines the fault interruption time of the S-HCB. The fault current then remains as a small AC ripple current until the mechanical switch starts opening at t_3 (~250 μs after fault detection) with the voltage across its contact gap considerably suppressed. At t_4, both Q1 and Q2 turn off, and the magnetizing current circulates through D2 (Mode C in Fig. 19.2). A voltage spike is observed due to the sudden change of the primary current, but SW1 has already established a sufficiently wide air gap to support the voltage at this time. The measurement results qualitatively agree with the simulation results, and together they have validated the S-HCB concept.

During the interruption process of the S-HCB, energy is initially transferred from the pre-charged capacitors, the main DC power source, and the main DC power loop to the primary side of the pulse transformer and eventually dissipated by the freewheeling diode D2 and parasitic resistance of the transformer and the VI circuit over a very long time period (tens of ms) after the mechanical switch completely isolates the fault. Note that no MOV is needed to absorb the residual energy during this relatively low-stress post-fault recovery phase.

There can be many embodiments of the basic S-HCB concept. Figure 19.6 shows a bidirectional embodiment of the S-HCB concept [9]. An H-bridge made of transistors Q2, Q3, Q4, and Q5 along with their antiparallel diodes replaces the transistor Q2 and freewheeling diode D2 in Fig. 19.2 to realize the same function of Fig. 19.2 but allows the main DC current flow in either direction. When the DC

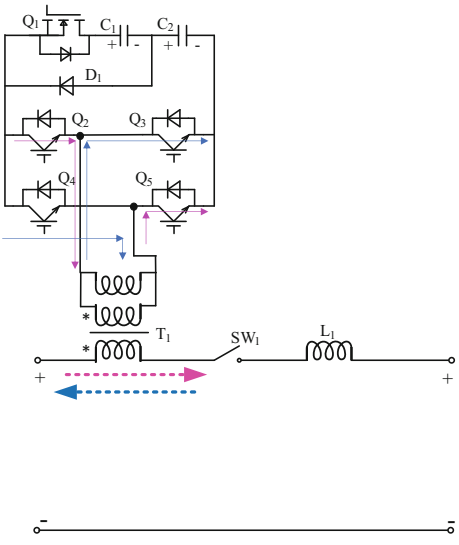

Fig. 19.6 A bidirectional S-HCB embodiment using an H-bridge circuit [9]

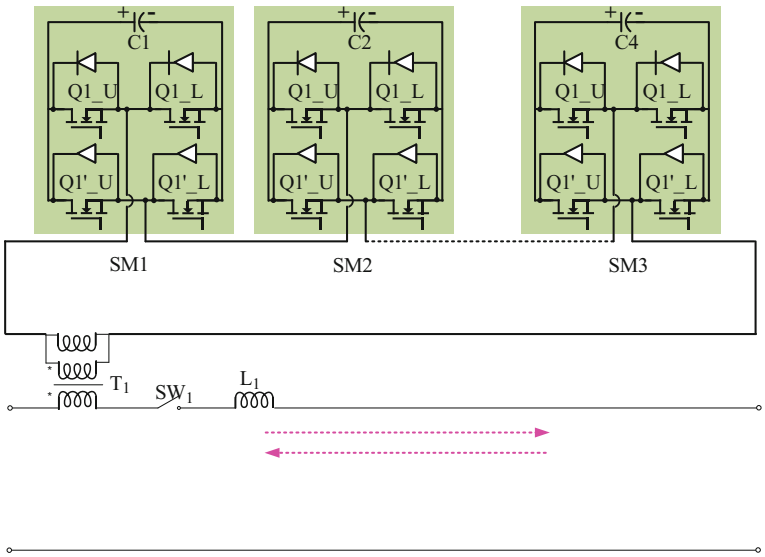

Fig. 19.7 A bidirectional S-HCB embodiment using MMC modules [9]

current in the main power loop flows from left to right, Q2 and Q5 turn on and off once during the interruption process, while Q3 and Q4 remain off. When Q2 and Q5 turn off after the mechanical switch opens, the antiparallel diodes of Q2 and Q5 take on the role of freewheeling diode D2 in Fig. 19.2. Similarly, when the DC current in the main power loop flows from right to left, Q3 and Q4 turn on and off once during the interruption process while Q2 and Q5 remain off. It is also possible to use multiple full-bridge MMC (modular multilevel converter) modules to realize the S-HCB concept as shown in Fig. 19.7 where the pre-charged capacitors are distributed among the MMC modules [9]. It is anticipated that additional scalability and flexibility can be realized with the MMC approach with a penalty in cost and control complexity.

3 Future Outlook

This chapter summarizes the fundamental challenges of the SSCB and HCB prior arts and introduces a new S-HCB DC circuit breaker concept that may overcome these limitations. The S-HCB concept offers low on-resistance of conventional HCBs but a fault interruption time even faster than fast-acting SSCBs. While the basic S-HCB concept is validated through the reported simulation and experimental work, it raises an array of unique technical challenges of multi-scale and multi-physics nature, ranging from kA/kV pulse transformer modeling and optimization under unique step-transient operating conditions to design of current-mode voltage

injection circuits with tightly regulated voltage pulses greater than 10 kV to unique thermal design challenge of megawatt pulsed power in a short time period. More research is needed to address these issues in the future to realize the full potential of this promising concept. New variants of the S-HCB concept need to be further explored. Furthermore, it is possible to develop other revolutionary fault protection concepts beyond incrementally improving the conventional SSCB or HCB schemes and address their fundamental shortcomings.

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Chapter 20
Techno-Economic Aspect and Commercialization of MVDC Power Systems

Daniel W. Cunningham, Isik C. Kizilyalli, and David Zhang

1 Introduction

Alternating current (AC) electric power has dominated the transmission and distribution system in the United States for over a century. However, direct current (DC) electric power offers several benefits over AC, reducing system power losses due to improved electrical conductivity and utilizing fewer power cables with higher power-carrying capacity. DC protection devices provide greater levels of safety compared to their AC counterparts in part due to solid state-based circuit that enable faster fault detection and breaking speeds. Cost benefits are also realized for integrated DC systems through design simplifications that remove layers of power conversion hardware.

A growing number of generation and load assets, including wind turbines, solar PV, energy storage, electric transportation, and consumer devices, all utilize DC power. Because of this evolving power landscape, estimates show that DC loads currently make up over 50% of total electricity consumption in the United States [1].

Recent advances in semiconductor-based power electronics (e.g., wide-bandgap (WBG) semiconductors, voltage source converters (VSCs), and DC-to-DC converters) have created an opportunity for greater utilization of DC in distribution and transmission. The transition from AC to DC will support growth in renewable energy, transportation electrification, and distributed energy resources (DERs).

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DC power provides numerous benefits at low (<1 kV)-, medium (1 kV–100 kV)-, and high (>100 kV)-voltage levels.[1] Both low-voltage DC (LVDC) and high-voltage DC (HVDC) markets are maturing. LVDC markets include consumer electronics, LED lighting, transportation sectors (e.g., electrification of rail, automobiles, and aviation), and commercial and industrial buildings. HVDC is used primarily for long distance over ground and subsea cable transmission and is more cost-effective than HVAC at distances of >500 km and >30 km, respectively [2]. HVDC is also used in conjunction with AC grid distribution and frequency regulation, including the interconnection of Japan's 50-Hz and 60-Hz AC grids [3].

2 MVDC Market Adoption

MVDC is primarily used for rail applications today, with voltages up to 3 kV [4]; however, MVDC benefits extend to a variety of potential markets, including distribution networks (e.g., conversion of existing AC lines to DC), distributed energy resources (DERs), and integrated renewable energy.

DC microgrids offer significant advantages such as control simplicity and fewer conversion stages for energy storage, renewables, electric vehicle (EV) charging, and electronics load integration [5]. These advantages have ignited interest in DC microgrids for data centers, industrial facilities, office blocks, and hybrid ships; they may also be extended beyond the microgrid scale to higher-level MVDC distribution (e.g., primary distribution) [3].

Sources of DC power supply currently include photovoltaic (PV) panels and fuel cells, but a study on off-shore wind collection showed that MVDC distribution would be more cost-effective when compared to HVAC, HVDC, or combined MVDC/HVDC distribution [6]. A general setup for an MVDC substation with representative energy supply, distributed resources, and loads is displayed in Fig. 20.1.

As the MVDC market matures and technology enablement grows, meshed DC distribution and large-scale grid integration of renewables is expected to expand, driven by higher efficiency and flexible system operation [8]. In countries with existing AC networks, an integrated multipoint DC grid could provide a backbone to the existing grid, resulting in greater grid resiliency [9].

Barriers to entry for MVDC markets include high adoption costs, technology availability, and safety concerns. As DC system-enabling technologies (e.g., DC-DC converters and DC circuit breakers) scale, MVDC system deployment costs will fall through mass production. MVDC market demand will drive market competition, which will result in further cost reduction and a greater variety of technology solutions for MVDC developers.

[1] There is currently no industry standard for MVDC except IEEE 1709–2010, which is specific to ships. ANSI C84.1-1989 defines MV as 600 V–69 kV, but this is for AC distribution systems. For this reason, the ranges specified above are defined by ARPA-E for the purpose of this publication.

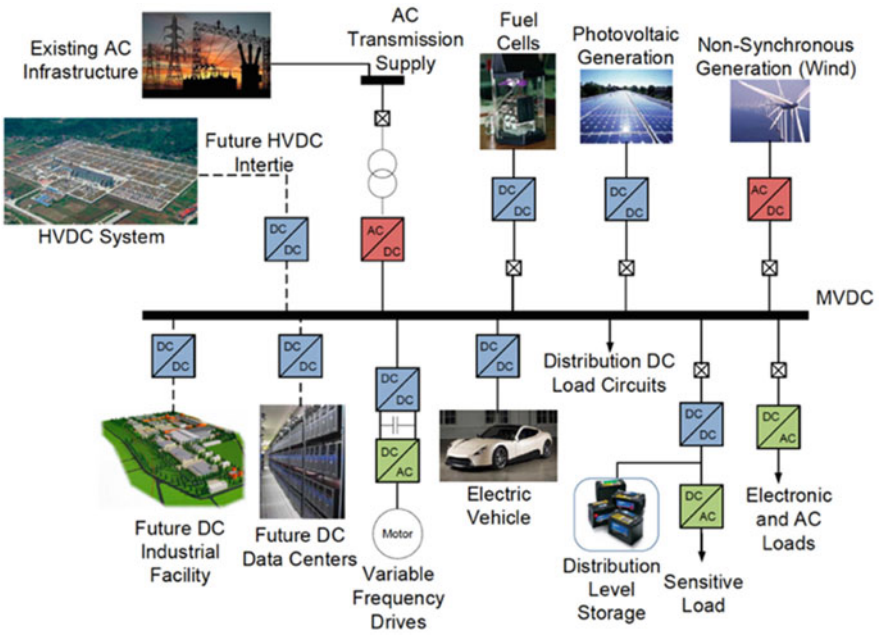

Fig. 20.1 Medium-voltage DC distribution and applications [7]

Safety concerns on managing MVDC faults will be alleviated as DC circuit breaker technologies continue to be tested, validated, and brought into the market. Technology innovation will be coupled with the introduction of new standards for MVDC safety protection to help facilitate smooth market adoption.

MVDC markets are expected to accelerate across the next decade with the changing landscape of generation and load types. The growth of solar PV (2.5× from 2012 to 2017) and battery storage is expected to continue to accelerate, driven by forecasted reductions in material and manufacturing prices [1]. Existing LVDC markets, including electric vehicles, data centers, electric aircraft, and electric distribution will look to capitalize on DC-based generation as they transition to medium voltage due to increased electrification.

3 MVDC Applications

3.1 Distribution Grid

MVDC provides several promising characteristics for electric grid distribution, in the same way that HVDC does for high-voltage grid transmission. DC has improved efficiency due to a lack of reactive power losses, skin effects, and corona losses. DC

Table 20.1 Reference values for DC and AC distribution

	DC	AC
Line losses	3.5% loss/1000 km	6.7% loss/1000 km
Power capacity	3500 MW	2500 MW

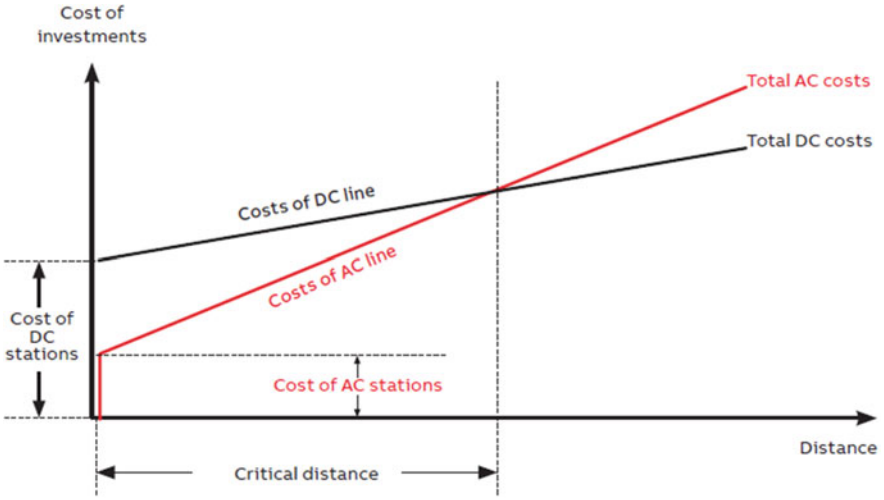

Fig. 20.2 Investment costs of a MVDC distribution line versus an equivalent voltage MVAC line including converters, conductors, and balance of plant [11]

also exhibits greater power delivery capacities compared to AC. The effective value of AC current and voltage has a root mean square (RMS) relationship, which is approximately 70% of peak. Since AC distribution cables still need to be sized for peak voltage, this creates an inherent benefit via greater power delivery with the same sized DC cable or line. Table 20.1 displays reference values for expected line losses and power-carrying capacity for an equivalently sized DC and AC line [10].

The break-even distance displayed in Fig. 20.2 is typically used to gauge whether AC or DC is more cost-effective for grid transmission and distribution. The slope of the "costs of DC line" is flatter due to efficiency and power benefits and the reduced number of conductors required to transmit power. The main cost driver for DC is DC power conversion and safety protection devices. Cost reductions in DC distribution-enabling technologies have decreased the breakeven from 1000 km to 500 km for overhead lines and from 50 km to 30 km for underground cables over the past decade [11] (cables have lower break-even costs due to significant capacitance and dielectric losses in AC cables [2]).

There are a number of pilot projects for MVDC distribution, including the Angle-DC project in the United Kingdom. The Angle-DC project is the first MVDC link in Europe, achieved through the retrofit an existing AC line. The existing 33-kV AC distribution system was converted into a ±27-kV DC distribution. Benefits include the integration of renewable generation, the ability to accommodate a growth in

electricity demand with a 23% power capacity increase, and enhanced thermal capabilities of the circuit [12].

The Angle-DC project exhibits a point-to-point MVDC application. DC networks can also be represented by a collection of point-to-point interconnections or a multipoint network mesh [9]. A multipoint DC network increases grid resiliency and allows for greater diversification of generation, frequency response, and energy arbitrage. DC mesh networks can be scaled up to cover an entire independent system operator (ISO) territory or scaled down to DC microgrid applications.

3.2 Microgrids

The effectiveness of islanded as well as integrated and connected microgrids to improve power delivery solutions is gaining greater interest [13]. These microgrids are often complex systems with PV, wind and traditional generation sources, electrical storage elements, and hybrid AC/DC load requirements. Smart grids can take the form of industrial units that need resiliency to maintain their operational efficiency with high-capacity factors, to modern hybrid and full electric ships and to large building structures such as schools, hospitals, and office complexes that require a reliable power supply to maintain their operations. When interconnected with a wider distribution grid, they can help stabilize weak or compromised grids and optimize control flexibility for the growing number of DC distributed energy resources, as shown in Fig. 20.3.

While this is an emerging space, the focus has been on predominantly AC-based distribution networks due to the predominance of AC loads and the availability of

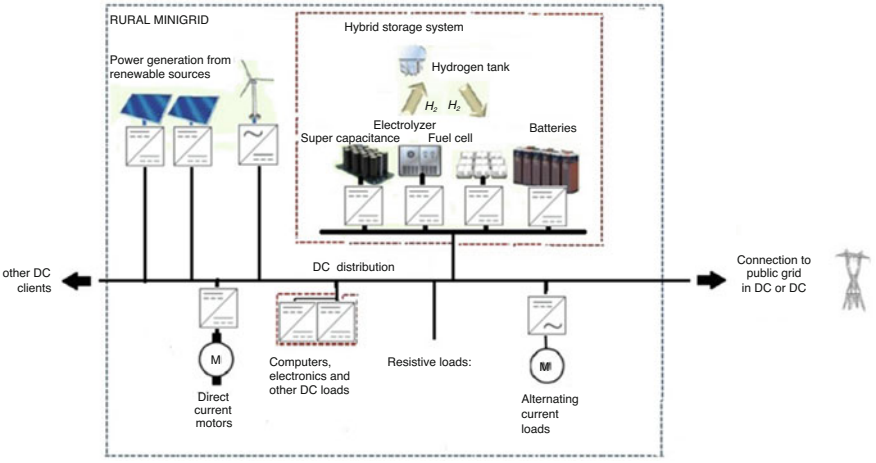

Fig. 20.3 Example of a DC microgrid with multiple DC generation and load assets [11]

cost-effective AC components. As microgrids grow to the MW range over expanded distances, an increase in power losses from AC distribution is impacting system economics and resulting in a growing interest in the transition to DC microgrids [12, 16].

MVDC microgrid networks can reduce power losses associated with skin effect and reactive components that AC systems suffer from. For an equivalent voltage MVDC system, the main loss is resistive and is not impacted by significant reactive power losses. There will, however, be a component of loss associated with the converter (AC to DC and DC to DC). As a result, the techno-economic analysis for the microgrid must consider both the total conductor length and the number of converters deployed.

Converter costs and the associated fault detection and interrupter systems will continue to impact the entry point for MVDC microgrids, but the benefits of lower total conductor costs, with a driving metric of $/km/MW, will provide a pathway for the choice over equivalent DC systems. A multicomponent MVDC microgrid network with interconnected MVDC conductor elements requires discrete breaker devices to close out specific legs of the system without closing the whole network. MVDC breakers offer a lower unit cost option to complex converter systems for rapid shutdown and are key enabling components for any DC microgrid topology.

3.3 Solar PV

As utility-scale PV installations become a growing percentage of the grid makeup, the size of the individual system is growing proportionally as well. These multi-100-MW systems over large land areas have led to a drive by engineering and design stakeholders to increase the system voltage of PV arrays to 1500Vdc, which reduces conductor losses and maximizes overall DC-to-AC conversion efficiency.

The advantage of operating PV systems at higher voltages includes lower currents, which enables smaller diameter cables and leads to a reduction in the number of combiner boxes needed to parallel connect PV strings. However, moving to 1500Vdc has been a challenge for the industry as switchgear, fuses, surge protectors, circuit breakers, etc. require certification at these elevated voltages [14]. In addition, downstream from the PV inverter and power distribution to the grid interconnection point is still commonly performed using AC power and susceptible to losses described earlier in this chapter.

Opportunities to improve efficiency are possible in the power distribution field of a utility-scale PV plant by converting the traditional AC system to an MVDC architecture enabled by innovative power converters and rapid shutdown breaker systems. The advantages of such a system have been modeled to illustrate how MVDC offers a pathway to greater conversion efficiencies both upstream and downstream of the inverter, enabling reduced in-plant distribution lines, relaxed transformer requirements, and simplified balance of plant (BOP) [15]. The scenario compared a current utility-scale PV plant with a plant that utilizes future high-

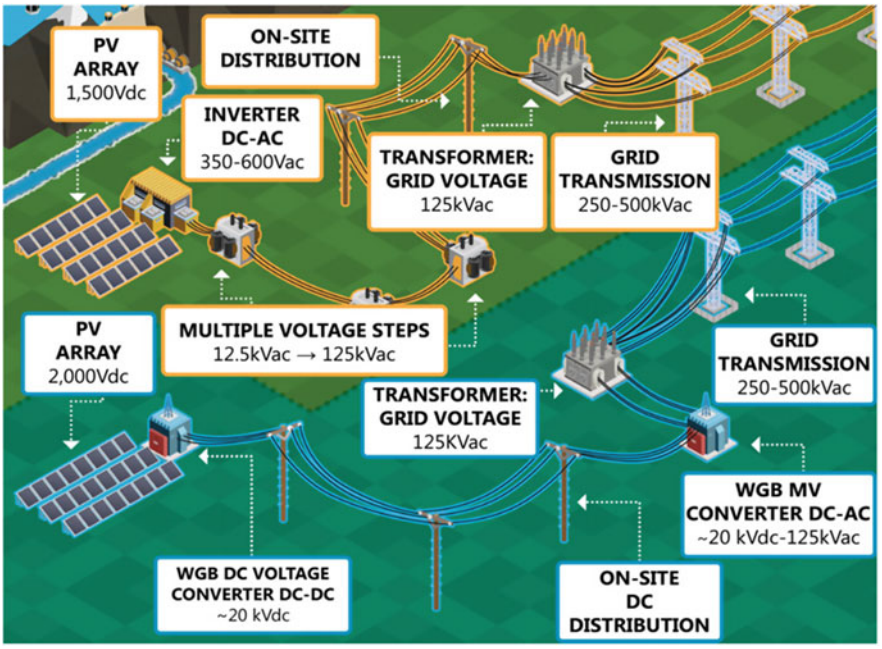

Fig. 20.4 Upper section: typical 1500Vdc utility-scale PV system architecture. Lower section: an aspirational 2000Vdc utility-scale PV system architecture utilizing medium-voltage DC-DC and DC-AC converters with reduced transformer count [15]

voltage WBG-based DC-DC converters, DC-AC solid-state transformers, and DC circuit breakers.

Figure 20.4 illustrates the possible reduction of BOP when MVDC converters and solid-state transformers are used in place of traditional utility-scale architectures. MV PV string voltages would allow reduced structural costs, electrical component count, labor and equipment costs, as well as engineering overhead. In addition, an MVDC architecture allows for the reduction of distribution line requirements within a plant, reducing combiner boxes and BOP (trenching, cement pads, wiring, etc.). This reduction in BOP lowers capital costs and the levelized cost of electricity (LCOE). This system would require MVDC breaker systems both at the 2000-Vdc level and the >20-kVdc distribution level for safety compliance, utilizing technologies described in this book.

However, developing PV modules rated at >1500Vdc will be a challenge as failure mechanisms such as cell-level potential-induced degradation would need to be addressed. Module designers will need to consider larger voltage standoff distances (creepage and clearance), encapsulants with lower water vapor transport rates, and cable/junction box polymers with higher-voltage ratings, in order to prepare (and certify) their products for MV systems [16]. These could increase

pressure on module bill of material costs, which would need to be more than offset by system cost reductions for adoption to be attractive.

In summary, the benefits of an MVDC distribution architecture for a utility-scale PV system include fewer voltage conversions/transformers (approximately 1% efficiency improvement for the elimination of each AC transformer), replacing traditional combiner boxes with isolated DC-DC converters offering improved reliability, data acquisition, and functionality, and easier integration and control of energy storage solutions to increase true plant capacity factor.

3.4 Offshore Wind Farm

MVDC has promising applications to reduce losses from the collection and transport of electricity generated by offshore wind farms. Offshore wind farms offer strong but less turbulent wind, availability of large potential areas for siting, and reduced visual and noise impact. This leads to high-energy production and a reduction of fatigue on the blades and structural components [17].

Most offshore wind farms utilize 33-kV or 66-kV AC cables for their collection systems. Wind farms located close to the shore use 220-kV to 275-kV AC cables. Over the last decade, wind farms have been moving further from the shore to capitalize on higher wind speeds, and the use of MVDC has become more cost-effective through a reduction in cable costs and efficiency losses. Connecting wind turbines directly to onshore inverter stations through direct MVDC results in potential capital cost savings of 10–20% compared with standard AC systems [18].

In an MVDC collection system, voltage conversion is performed using DC/DC converters with a medium-frequency transformer (MFT), which is significantly smaller and lighter than traditional transformer equipment used in HVAC or HVDC export, as illustrated in Fig. 20.5c. Some proposed MVDC designs are able to utilize MVDC up to the grid tie point entirely, removing the need for an offshore platform altogether and saving up to 20% of the offshore wind farm capital cost as displayed in Fig. 20.5d.

A large variety of MVDC wind collector systems have been proposed including standard parallel, centralized parallel, dispersed parallel, and series-parallel collector systems [19]. The standard design consists of parallel connections in which each wind turbine contains a dedicated DC/DC converter and a transformer to step up voltage. The system voltage is then further stepped up at an offshore platform with DC/DC converters for export. Centralized parallel and dispersed parallel MVDC collector systems offer benefits including reduced componentry and maintenance, while a series-parallel collector system removes the need for an offshore platform.

With weight, capital cost, transportation, and maintenance being the key disadvantages of offshore wind farm systems, MVDC systems provide an encouraging value proposition. Various collector topologies have been proposed, and there is significant interest in utilizing MVDC, but real-life applications remain sparse. A reduction in the cost of power electronics and advances in DC control and protection is expected to enable the growth of MVDC-based wind farm projects.

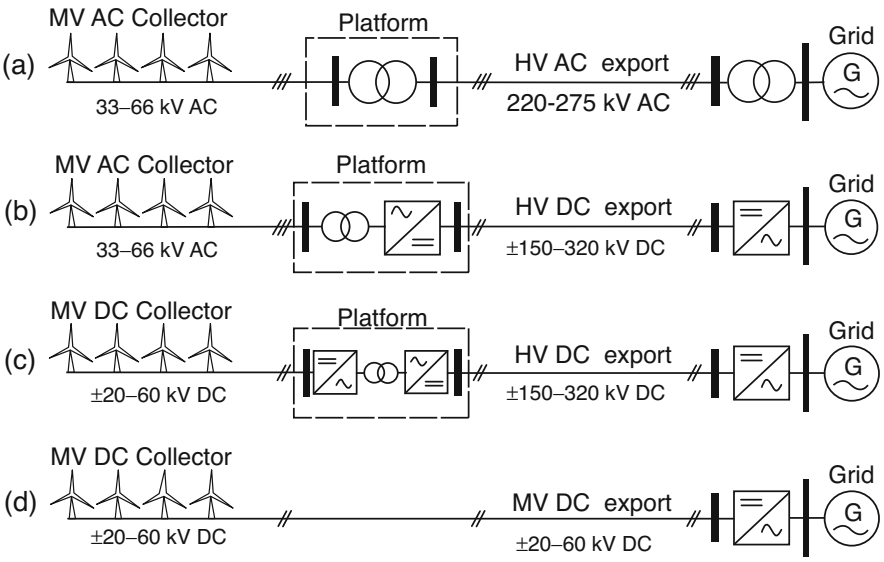

Fig. 20.5 Offshore wind farm collection configurations with AC and DC collection and export to grid: (**a**) MVAC collector with HVAC export, (**b**) MVAC collector with HVDC export, (**c**) MVDC collector with HVDC export, and (**d**) MVDC collector and export. Indicative voltage levels are based on existing AC wind farms and proposed DC wind farm designs [19]

3.5 Aviation

Air travel accounts for a considerable and growing portion of US energy imports and GHG emissions. In 2017, the United States consumed nearly 3.5 quads of jet fuel, about 3.5% of primary energy consumption, or equivalent to about 2% of petroleum imports, and these numbers are only expected to grow [20, 21]. Revenue passenger miles for flights in the United States flown by US certificated carriers nearly doubled between 2002 and 2018, and global growth rates are expected to increase [22, 23]. Reducing GHG footprint is challenging and risky, but there has been growing activity in partially or fully electrified powertrains as a potential pathway toward decarbonized air travel.

Electrified energy conversion systems have the potential to achieve higher fuel-to-propulsive power energy conversion efficiencies compared to conventional gas turbine engines. Hybridized architectures, which may combine gas turbines, batteries, and/or fuel cells in various configurations, can capitalize on the performance strengths of individual technologies relative to the demands at each flight stage, leading to an overall increased efficiency. Distributed propulsion, enabled by electrification, can improve lift-to-drag ratios and expand the design space, further reducing the energy required to carry a given payload.

One of the main barriers to electric aviation is power delivery to motors, which can require up to tens of MW of power [24]. The state-of-the-art maximum onboard electric power generation capacity in operating commercial airliners is

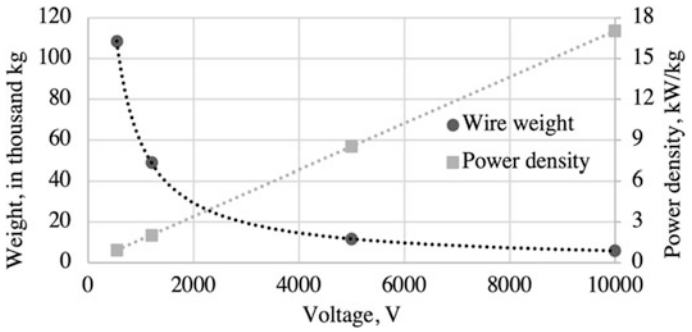

Fig. 20.6 Voltage vs. copper wiring weight and power density (Weight estimation assumptions: 8 × 45 m cable copper wires with no insulation (insulation would contribute additional weight), 50 MW cable, 100 MW notional aircraft, 2× redundancy, 2 generators)

approximately 1 MW on the Boeing 787. Onboard power architecture is supplied via low-voltage AC distribution (115–235 VAC, ±270 VDC) to ancillary electrical power systems such as HVAC, avionics, actuators, and anti-icing/deicing systems. In contrast, Airbus' concept test bed design for a narrow-body, hybrid-electric distribution system, the E-Fan X, includes a distribution system at 3 kVdc and a 2-MW electric propulsor which replaces one of four jet engines [25].

The need to adopt medium-voltage power systems is clear. Distribution of such a large amount of power may require the use of a prohibitive load of cables and connectors. Transformative solutions such as the use of an MVDC distribution system would more likely meet weight and size requirements. To illustrate this, Fig. 20.6 gives an example of how increasing voltage can reduce the wiring weight of the conducting core and increase the gravimetric power density of a cable.

At 540 V and 10 kV, the power losses are estimated to be 48 kW and 2.6 kW, respectively. Performance at medium voltage will be critical to achieving substantial improvements in the gravimetric power density of an electrical system using traditional metals.

It is clear that there is a benefit for the aviation industry to distribute power at MVDC levels to meet the power demands of commercial aircraft propulsion systems. However, there are many challenges in operating MVDC power systems at typical airline cruising altitudes, including increased risk of corona discharge at operating altitude, availability of aviation certified conductors and connectors, and MVDC breaker designs that operate safely in this demanding environment [26].

3.6 Data Centers

Data centers continue to exhibit rapid growth in number and size. Hyper-scale data centers have become the most cost-efficient option for cloud operators due to economies of scale. The total energy consumption is expected to reach as much as 13% of the world's total electricity by 2030 [27]. The continuous expanding size of

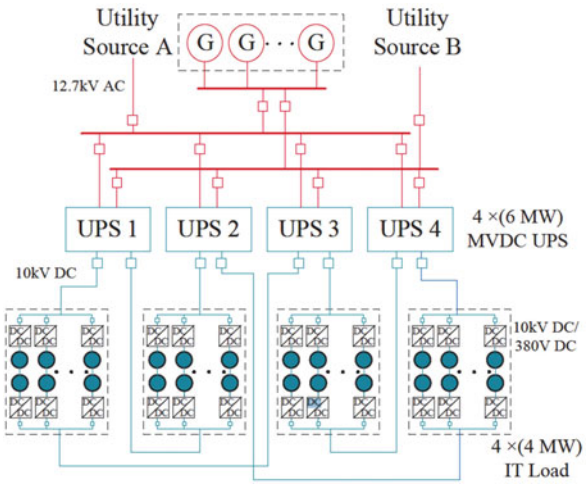

Fig. 20.7 MVDC data center exemplar case

the data center brings new challenges to power distribution. In fact, data centers are among the most critical and energy-intensive loads for power grids. Hence, higher efficiency in power distribution can lead to substantial energy and operational cost savings. On the other hand, data centers include critical IT loads where power outages are costly. The power distribution architectures for data centers require new methods for improvement in terms of efficiency, reliability, and cost reduction.

In order to deliver a high level of power to server rooms, the conventional low-voltage AC (LVAC) architecture requires a large number of devices and large quantities of wiring, resulting in higher economic costs as well as outage risks. DC architectures have been proposed as promising solutions considering the fact that the IT loads use DC voltage to operate [28, 29]. Compared to their AC counterparts, DC systems have fewer power conversion stages, resulting in higher efficiency and lower probabilities of failure. Moreover, DC cables can carry more current than AC cables of equal size which results in lower capital cost [30]. MV distribution architectures are also proposed to address these emerging issues, which bring potential advantages such as less space, reduced losses, and higher reliability [31]. The MVDC architecture is enabled through emerging MVDC breakers. A system is illustrated in Fig. 20.7.

Four economic metrics are usually of interest in order to assess the potential benefits of new architectures such as MVDC data centers: capital cost, operational cost, cost of loss of load, and equipment damage cost. A 10-year horizon is considered, and N-2 post-contingency optimal power flow (OPF) is utilized to evaluate system availability, which is later reflected in the cost calculation. A study for MVDC that considers these value streams and utilizes this methodology is presented in [32]. The results show that using a DC system at the medium-voltage level can substantially reduce the costs of data centers compared to the conventional AC architectures.

4 Regulatory Framework and Standards

Circuit protection protocols in AC systems are very advanced, with IEEE standards already implemented for many grid, ship, and rail systems. However, there has been limited research conducted on DC protection and minimal commercially available products [19]. Medium-voltage DC distributions systems at a grid level are still at a nascent level [18]. Early adoption applications where MVDC breakers have emerging standards include electric ships and marine applications. These are intended to assist in the procurement, design, safety, and practices that dictate effective operation of MVDC electrical power systems [33]. Organizations such as CIGRE are actively assessing the applications and needs of the emerging MVDC standards space.

Key to the definition of a series of standards will be the type and architecture of switching equipment. Considerations will need to be made for closing functionality, commutation technology, speed, current and voltage ratings, and lifetime as a total number of cycles. The MVDC network topology may need to be considered as part of the standard definition, whether the connection is point-to-point or part of a multi-node/multiterminal system.

Standards will also be influenced by application. For instance, ship and rail operate at 6kVdc and 3kVdc, respectively, requiring different sets of standards. Specific standards may be required for hybrid DC-AC networked systems. Fusion energy applications, which would require rapid, high current breakers, would need not just electrical performance and safety standards but also nuclear industry oversight. In this application, high-voltage DC power would be used to control magnetic fields needed to heat plasmas, which are key for fusion energy realization [34].

Lastly, it is likely that certification organizations will leverage existing MVDC standards (used in transportation sectors) and HVDC protocols to meet the growing need for equivalent MVDC applications [35].

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