A Novel Blind Zone Free, Low Power Phase Frequency Detector for Fast Locking of Charge Pump Phase Locked Loops

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Abstract. Phase Frequency Detector (PFD) being one of the important block of the high frequency clock generator encounters two major problems in its design. One being the dead zone and other is blind zone. The presence of the dead zone leads to phase noise. Blind zone increases the lock time of the clock generator. This paper presents a novel edge detector based PFD. In the proposed PFD, zero blind zone is achieved by eliminating the reset pulse beyond the dead zone region. The proposed PFD is designed in UMC 0.18 μm CMOS process. It consumes power of 648 μW at an operating frequency of 1 GHz. It is observed that the proposed PFD locks 43% faster than the conventional PFD.

Keywords: Phase frequency detector · Dead zone · Blind zone · Reset pulse · Clock generator

1 Introduction

High frequency clock generators commonly known as Phase Locked Loop (PLL) is being used in numerous applications across the globe that includes Wi-fi routers, televisions, Zigbee, etc. The widely used PLL is the charge pump based PLL. It consists of five blocks. PFD being the first block of the PLL detects the phase and frequency differences between the reference clock (REFCLK) generated by the crystal oscillator and the feedback clock (FBCLK) generated by the Frequency Divider (FD). It generates UP and DOWN (DN) signals. These signals are converted as a control signal (VCTRL) to the Voltage Controlled Oscillator(VCO) by the Charge pump (CP) and Loop filter (LF) which helps in the locking of the PLL loop. Thus, the ability of the PFD to detect all the phase differences in the range of $[-2\pi, 2\pi]$ is very essential as it helps in fast acquisition of the PLL and also helps in the generation of low phase noise, high frequency clock.

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1.1 Issues Related to Conventional PFD

Conventional PFD is shown in Fig. 1. The operation of the PFD can be easily visualised with the help of the state diagram as shown in Fig. 2.

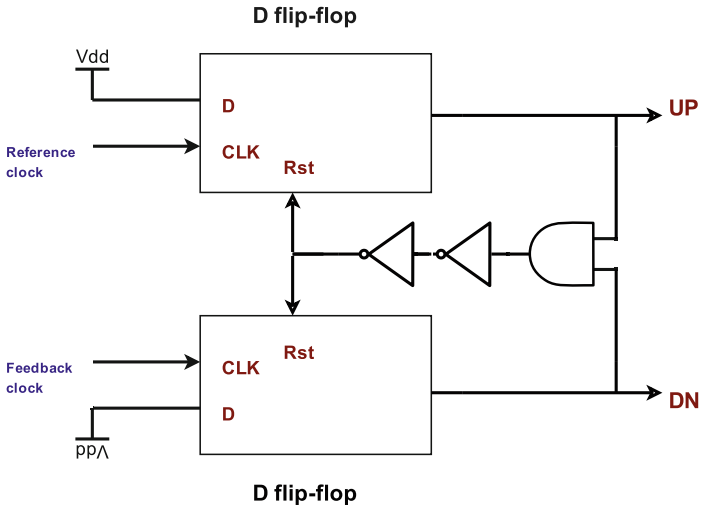

Fig. 1. Block diagram of Conventional PFD

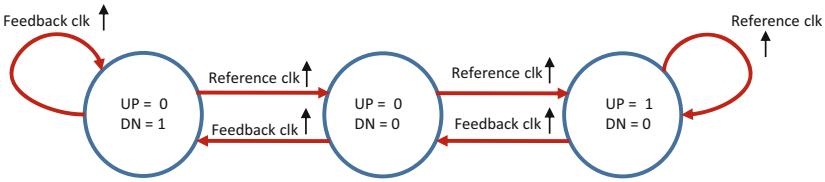

Fig. 2. State diagram

Conventional PFD encounters two issues in its architecture namely dead zone and blind zone that affects the linearity as presented in Fig. 3, thereby reducing the PFD operating range.

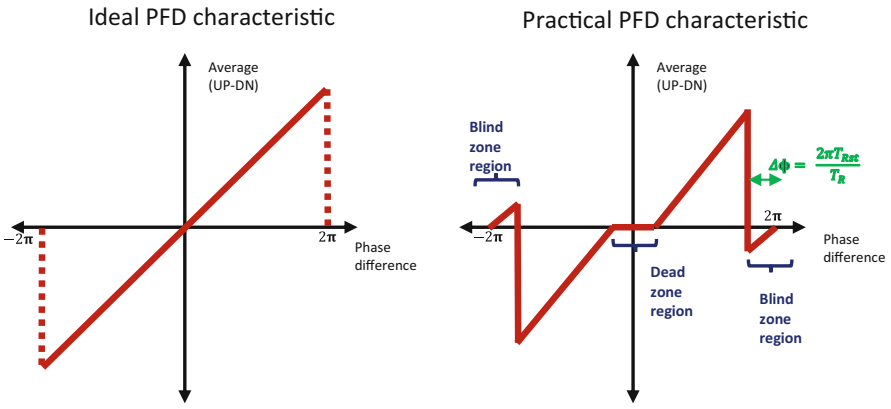

Fig. 3. PFD phase characteristic

In the PFD phase characteristics, dead zone occurs in the neighbourhood of zero phase difference. Due to the presence of finite parasitic capacitances, the PFD output doesn't have enough time to reach a particular logical level 0 or 1 (that is, 0 or Vdd) when small phase difference exists between the input clocks. Thus, PFD fails to trigger the CP leading to accumulation of static phase error until the PFD comes out of the dead zone region. This static phase error translates to phase noise in the PLL. Using finer and finer technology, the dead zone can be reduced but we cannot completely eliminate it. To eliminate completely we can add delay elements in the reset path of the PFD equal to the minimum ON time of the CP switches to turn ON. Hence, even for small phase difference, the charge pump will now be able to turn ON for correcting the phase error and making the PFD as a dead zone free circuit. Thus, increasing the delay in the reset path reduces the dead zone in the conventional PFD. As the delay in the reset path is increased, the highest frequency of operation of the PFD gets limited and also it leads to high blind zone.

The highest frequency of operation(f_{max}) of the PFD is inversely proportional to the reset path delay (T_{Rst}) and is given by [8],

$$f_{max} = \frac{1}{T_{Rst}} \tag{1}$$

Thus, high reset path delay limits the highest operating frequency of the PFD.

In the PFD phase characteristics, blind zone occurs in the neighbourhood of 2π phase difference. The PFD fails to detect the rising transition of the leading input clock signal due to high reset pulse. Thus, the PFD produces wrong output, misleading the PLL. This leads to increase in the lock acquisition of the PLL. Hence, need to eliminate the blind zone is necessary to reduce the lock acquisition which is a major concern for high speed applications. The PFD introduces wrong output for phase differences greater than $2\pi - \phi$ where,

$$\phi = \frac{2\pi T_{Rst}}{T_R} \tag{2}$$

Here, T_R = the reference clock time period.

As seen from the above equation, blind zone depends on the reset pulse. Blind zone is lower, when the reset path delay is lower. If reset path is zero, from the equation we obtain zero blind zone.

There are various PFD designs in the literature to overcome the problems of the PFD. In [5], PFD using transmission gate is designed. It is blind zone free but has an operating range of $[-\pi, \pi]$ severely affecting the PLL locking time. In [7], PFD using selective reset technique is designed to reduce the blind zone. It has a blind zone of 3 ps. In [1], differential PFD is designed. It is blind zone free but has an operating range of $[-\pi, \pi]$. In [3], composite PFD is implemented to eliminate blind zone. This leads to PLL design complexity as it requires two charge pumps and a switchable loop filter. In [9], delays were used to push the leading input clock signal edge out of the reset pulse to get the correct output to reduce the blind zone. The problem with such a design is that it may fail across process, temperature, voltage variations. In [2], edge detector is used to design the PFD. It has a reset pulse of 80 ps, thus introducing significant blind zone. In [6], latch based PFD is designed. The reset path is reduced to obtain high operating frequency and fast locking of the PLL. It has a highest operating frequency of 1.5 GHz. The presence of reset path indicates the presence of blind zone in the latch based PFD.

This paper introduces a novel blind zone free PFD using edge detector for fast locking of PLL. Section 2 introduces the proposed design. Section 3 and Sect. 4 presents the simulation results and the conclusion of the work respectively.

2 Proposed PFD

PFD requires reset pulse only in the dead zone region [4]. Thus, in the proposed circuit the reset pulse is eliminated after the dead zone region in the PFD. The circuit diagram of the novel PFD is presented in Fig. 4. In the PFD, REFCLKD and FBCLKD are the delayed version of the reference clock (REFCLK) and feedback clock (FBCLK) respectively, to completely eliminate the blind zone. RH and FH signals are generated using edge detectors. Edge detectors are used in the discharging path so as to get the correct output beyond the dead zone region. Transistors Mu4 and Md4 are used to ensure proper operation of the PFD.

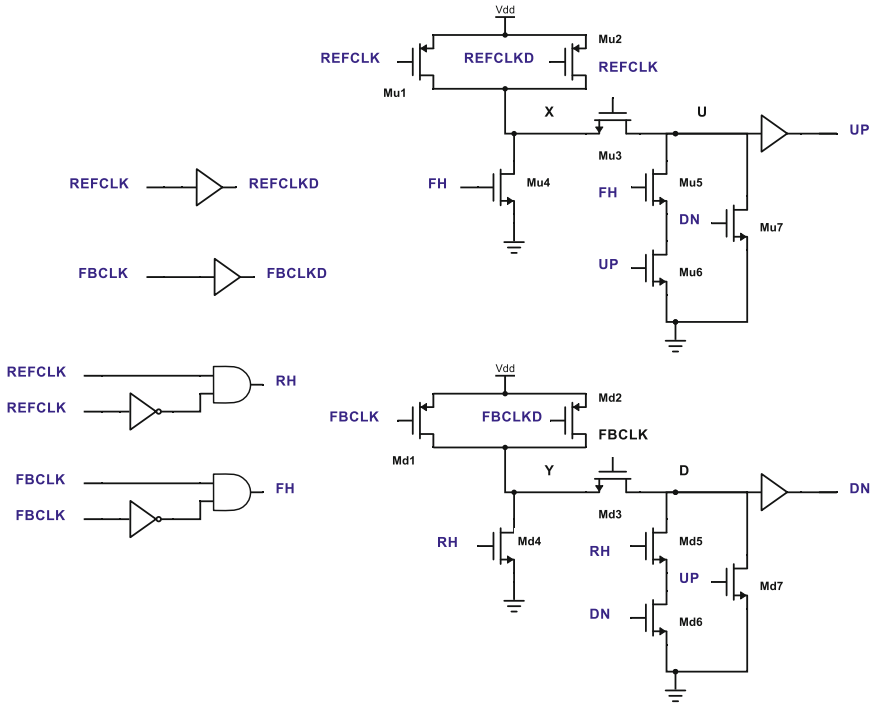

Fig. 4. Proposed PFD

2.1 PFD Operation

Let us assume REFCLK leads FBCLK. Initially node x and y are precharged to Vdd. Here, we consider two cases: (1) PFD operation beyond the dead zone region (2) PFD operation in the dead zone region.

Case 1. In Fig. 4, when REFCLK goes high, node U goes high. Thus, UP signal goes high. Transistor Md7 gets activated since, UP is high. Now, when FBCLK goes high, node D doesn't go high as it gets discharged through transistor Md7. Hence, DN is zero throughout the operation. FH gets activated since FBCLK is high. As both the transistors Mu5 and Mu6 are activated simultaneously, U is discharged to zero. Thus, UP goes low.

Hence, in the operation of PFD beyond the dead zone region, no reset pulse is generated making the PFD blind zone free.

Case 2. In Fig. 4, when REFCLK goes high, UP goes high. Since, in the dead zone region, the phase difference between REFCLK and FBCLK is small, transistor Md7 doesn't find enough time to discharge node D to zero. Thus, when FBCLK goes high, DN goes high. As the transistors Mu7 and Md7 are activated, UP and DN goes low.

Hence, in the operation of PFD in the dead zone region reset pulse is generated making PFD dead zone free.

3 Simulation Results

The proposed PFD is implemented in UMC 180 nm CMOS process. The proposed PFD consumes power of 65 μW at an operating frequency of 100 MHz and 648 μW when operated at frequency of 1 GHz. It is observed that the PFD is not sensitive to duty cycle variations of the REFCLK and FBCLK signals.

The timing diagram of the PFD is presented in Fig. 5 for a phase difference of 9.5 ns between the clocks.

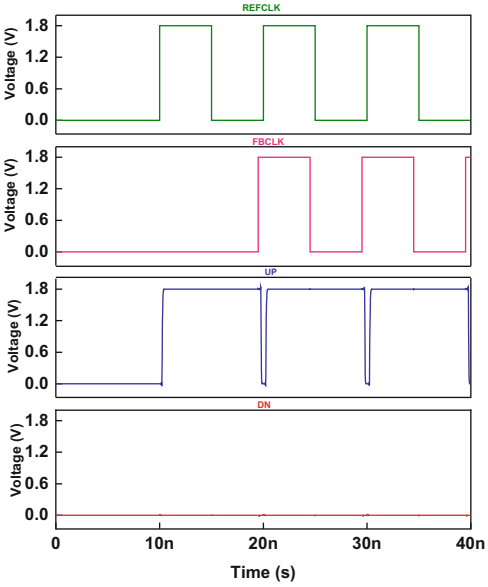

Fig. 5. PFD output when REFCLK leads FBCLK by 9.5 ns

It is observed that no signal is generated at the DN node as stated in the discussion.

The timing diagram of the PFD when REFCLK leads FBCLK by 2 ps is shown in Fig. 6. It is observed that the reset pulse is generated by the PFD when there is small phase difference.

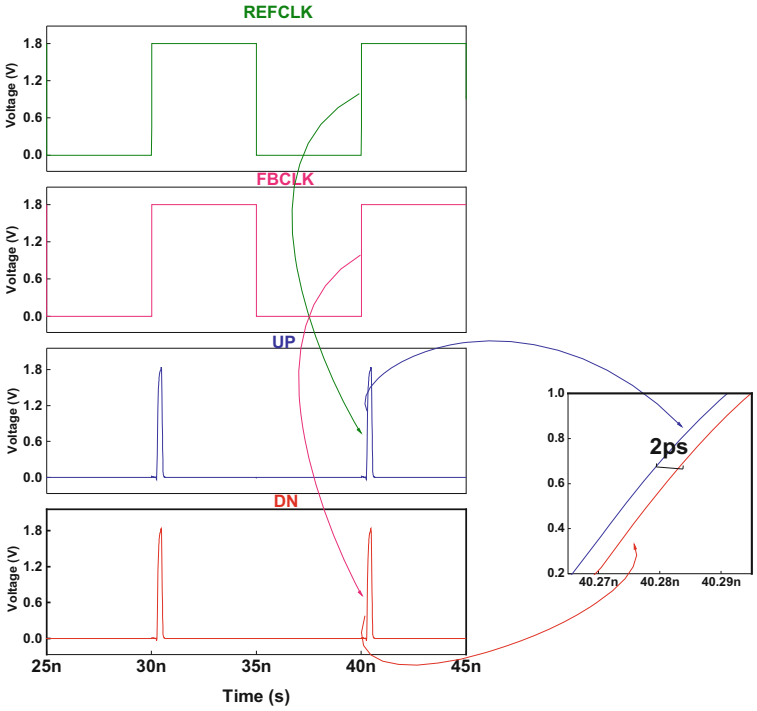

Fig. 6. PFD output when REFCLK leads FBCLK by 2 ps

In the proposed PFD, the reset pulse is generated within the dead zone region and is eliminated beyond the dead zone region. Thus, neither the dead zone nor the blind zone is present in the PFD designed in this work.

Figure 7 shows the PFD operation when REFCLK and FBCLK are in phase.

Figure 8 presents the UP and DN signals when REFCLK and FBCLK exhibits different frequencies.

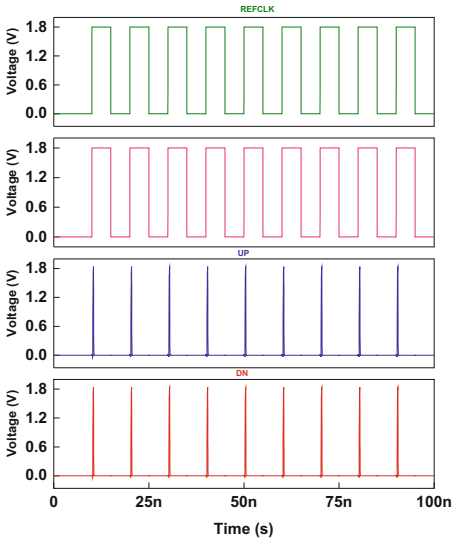

Fig. 7. PFD output when REFCLK and FBCLK are in phase

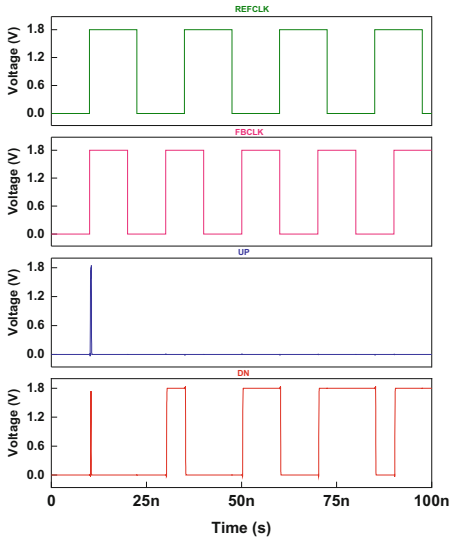

Fig. 8. PFD output when REFCLK and FBCLK signals have different frequencies

The PFD is simulated across different process corners to obtain the PFD transfer curves as shown in Fig. 9. It is found that the PFD maintains its linearity across different process corners.

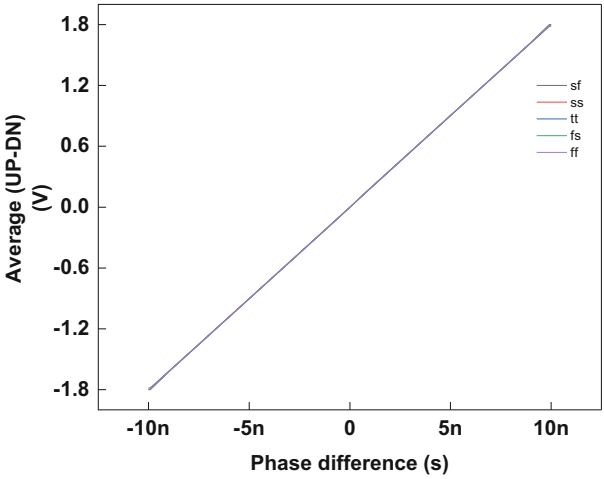

Fig. 9. PFD phase characteristic in various corners

To analyse the PFD performance in the PLL loop, it is important to design a PLL using the PFD designed in this work. The simulation setup is shown in Fig. 10.

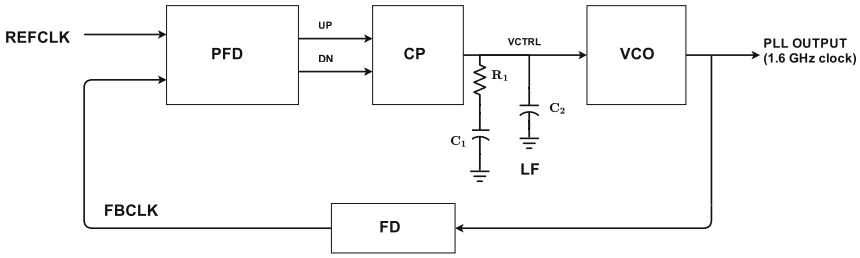

Fig. 10. Simulation setup

The PLL is designed to have an PLL OUTPUT of 1.6 GHz. The REFCLK frequency is considered as 100 MHz. The parameters of loop filter are chosen such that it has sufficient phase margin to maintain the stability of the overall PLL loop.

The conventional PFD is designed in UMC 180 nm process for the purpose of comparison. The locking of the PLL with the PFD designed in this work is shown in Fig. 11. It can be observed that the PLL locks with minimum steady state error between the UP and DN pulse which is caused due to the discrepancy between the source and sinking current of the next block, that is, CP.

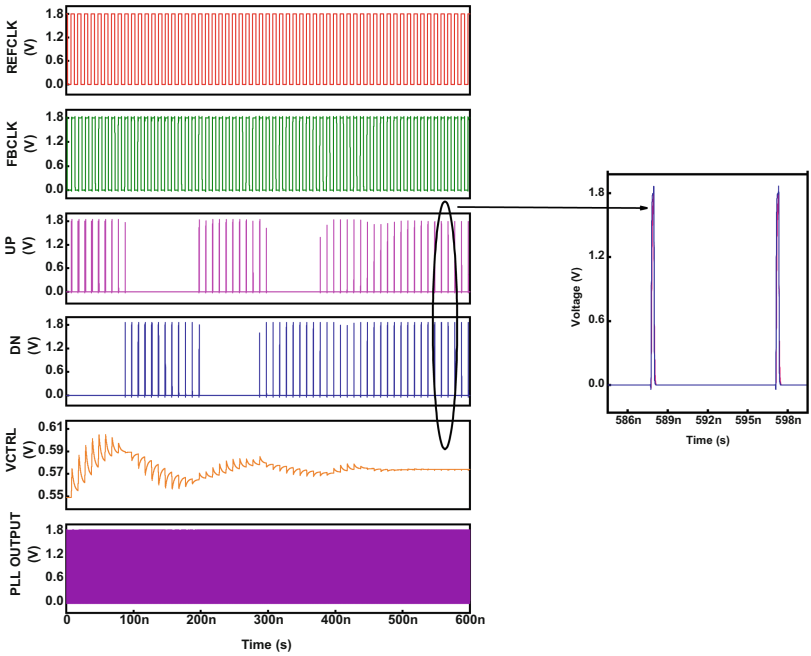

Fig. 11. PLL locking using the proposed PFD

The PLL is simulated using both the PFDs as shown in Fig. 12. It is observed that the PLL lock time using the novel PFD is 450 ns and using the conventional PFD is 790 ns.

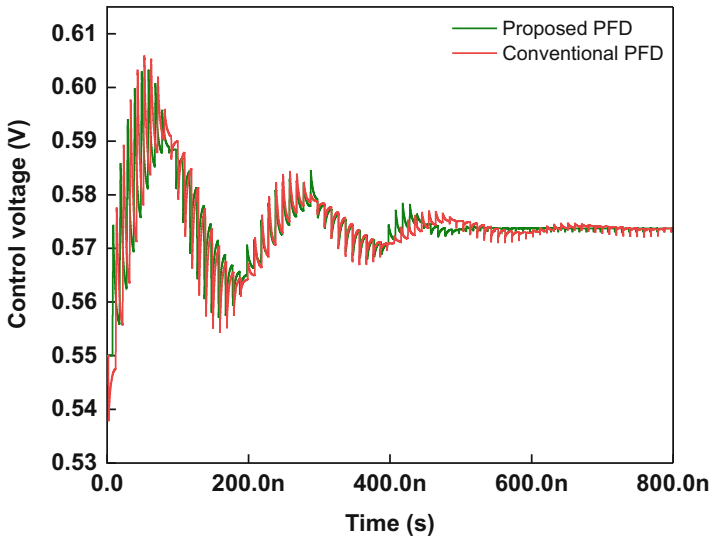

Fig. 12. Lock time of a 1.6 GHz PLL using different PFDs

The PFD designed in this paper is compared with the recent PFD designs as shown in Table 1. All the PFDs are operated at supply voltage of 1.8 V. It is observed that the PFD in [1] has an operating range of $[-\pi, \pi]$ which will severely affect the locking time of the PLL. Also, it has dead zone of 40 ps. Even though the PFD in [5] is free from dead zone and blind zone, it has an operating range of $[-\pi, \pi]$, thus leading to increase in lock time of the PLL.

Table 1. Comparison table

Designs	Technology (nm)	PFD ideal range	Blind zone (ps)	Dead zone (ps)	Power (μW)
[1]	180	$[-\pi, \pi]$	Free	40	107 @1 GHz
[7]	180	$[-2\pi, 2\pi]$	3	Free	2600 @100 MHz
[4]	180	$[-2\pi, 2\pi]$	Free	Free	1360 @1 GHz
[5]	90	$[-\pi, \pi]$	Free	Free	12.1 @100 MHz
This work	180	$[-2\pi, 2\pi]$	Free	Free	65 @100 MHz, 648 @1 GHz

In [7], the PFD architecture has an ideal operating range of $[-2\pi, 2\pi]$, but has a blind zone of 3 ps. The power consumed is 2600 μW when operated at frequency of 100 MHz which is 97.5% higher than that of the proposed PFD. In [4], the PFD is designed such that it is free from dead zone and blind zone. It has an operating range of $[-2\pi, 2\pi]$. The power consumed is 1.36 mW which is 52.3% higher than that of the proposed PFD. Thus, the PFD designed in this work has good performance when compared to the existing literatures.

4 Conclusion

In this paper, edge detector based PFD is designed and proposed. The reset pulse is not present in the PFD after the dead zone region, leading to a blind zone free PFD. The PLL using the proposed PFD acquires 43% faster locking than with the conventional PFD. The power consumption is significantly reduced when compared to the existing literatures. Thus, the designed PFD is suitable for low power high speed applications.

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