Hybrid Architectures and Controllers for Low-Dropout Regulators

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1 Introduction

For higher system power efficiency of a system-on-a-chip (SoC) or multicore microprocessors, fine-grained supply voltage management with multiple divided and adaptive voltage domains appeared in state-of-the-art computing systems, which allows the optimization of each supply voltage domain dynamically and independently. In general, advanced nanoscale CMOS devices cannot directly withstand the high voltage levels provided by a lithium-ion battery or by a board-level power supply bus, mandating off-chip and/or on-chip integrated voltage regulator(s). While off-chip switching regulators can offer one-step conversion from the sources with ~90% efficiencies, they require bulky power inductors and a large number of filtering capacitors. In addition, when delivering power with a stepped-down low voltage from the board onto the chip, the high current stress demands many package bumps. Furthermore, since the package bump pitches scale at a much slower rate than that of the CMOS devices, therefore, there are restrictions for the total number of the voltage domains provided by off-chip regulators [1]. To fulfill the fine-grained power supply management, a hierarchical power delivery network with two-step conversion/regulation is favorable (Fig. 1), with the battery

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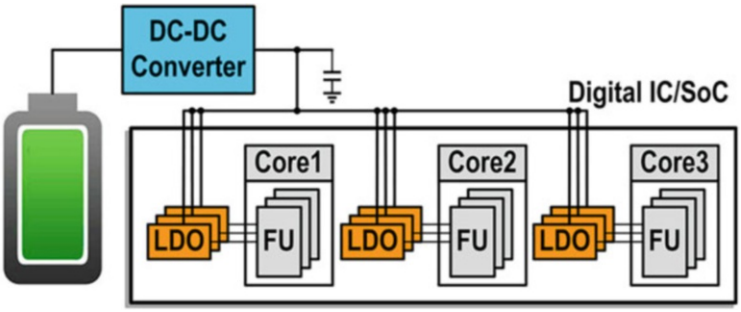

Fig. 1 Hierarchical power delivery network solution of a digital system

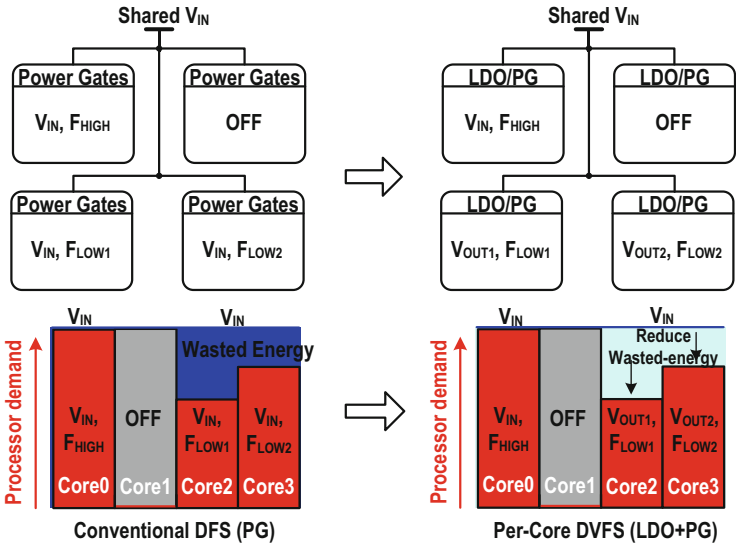

Fig. 2 Per-core DVFS with integrated LDOs and a shared power supply V_{IN}

voltage converted into an intermediate voltage using a high-efficiency DC-DC converter and then multiple fully integrated low-dropout regulators (LDOs) employed to power the function units (FUs).

Taking the multicore processor application as an example, an LDO can provide a compact and cost-effective way to realize per-core fast dynamic voltage and frequency scaling (DVFS), as presented in Fig. 2.

To analyze how much power the DVFS can save, we can calculate the power consumption P_A of the digital system with a fixed V_{IN} as its supply:

$$P_A = C_{\mathrm{dynA}} \times V_{\mathrm{IN}}^2 \times F + I_{\mathrm{LEAK\_VIN}} \times V_{\mathrm{IN}} \tag{1}$$

Then, we calculate the system power consumption P_B with LDOs that make each core operate at their corresponding optimum supply voltage V_{OUT}:

$$P_B = \frac{C_{dynA} \times V_{OUT}^2 \times F + I_{LEAK\_VOUT} \times V_{OUT}}{\eta_{LDO}} \tag{2}$$

where $\eta_{LDO} \approx V_{OUT}/V_{IN}$. The saved power consumption is

$$P_{SAVE} = P_A - P_B = C_{dynA} \times V_{IN} \times (V_{IN} - V_{OUT}) \times F + V_{IN} \times \left(I_{LEAK\_VIN} - I_{LEAK\_VOUT}\right) \tag{3}$$

According to Eq. (3), we can deduce that although the LDO power efficiency can be very low in a large dropout voltage condition (e.g., $V_{IN} = 1$ V, $V_{OUT} = 0.5$ V), it can still save a lot of power from a system perspective.

On the other hand, an analog LDO (A-LDO) is suitable for noise-sensitive analog and RF circuits, as it has fast transient response with low quiescent current and good power supply rejection [2–5]. However, it faces several challenges when powering the digital circuit in advanced nanoscale CMOS. One of the major design challenges of an A-LDO is the relatively small load capability. To deliver a large load current with low-dropout voltage (<100 mV), the size of the power transistor becomes quite large; thus, the associated gate pole, the load-dependent transconductance g_m, and the output pole p_{OUT} may cause instability. Most of the prior fully integrated A-LDOs are only capable of delivering a load current of <250 mA, which is insufficient to supply a high-performance processor. In [6] a dual function LDO/power-gating design with 4A output capability requires a 4μF capacitor in package and a 50 nF on-die compensation capacitor that increases the size and cost.

Another challenge is the performance degradation at a low input voltage. The downscaling of the fabrication process favors low V_{IN} to reduce the dynamic and leakage currents of the load circuits. The Internet of Things (IoT) and the wearable devices advanced significantly benefiting from low-power circuit technologies such as near-threshold voltage computing [7, 8]. In an advanced process, microprocessors can work in the near-threshold voltage (NTV) and even the sub-threshold voltage regions to save power [9]. When the input supply voltage goes down to the NTV or sub-threshold level, LDOs are still necessary for fine-grained voltage domain and individual performance power optimization. Nevertheless, we may not have sufficient voltage headroom for the analog error amplifier (EA) to drive the power transistor in an A-LDO. Thus, a large power transistor is necessary; besides, it would be hard to obtain a high loop gain with a low supply voltage.

Recently, the digital LDO (D-LDO), the switching LDO (S-LDO), and the hybrid architecture received significant attention, as they are more suitable for such applications. The organization of this chapter is the following: Section 2 introduces the classic LDO control methods and power stage selection. Section 3 details examples of analog-assisted and hybrid control digital LDOs. Section 4 presents the ampere-level switching LDO for high-performance multicore processors. Finally, Sect. 5 draws the conclusions.

2 Control Method and Power Stage Selection

2.1 Power Stage Comparison

According to the different regulation methods of the power stage, we can categorize the LDO into three types, as presented in Fig. 3.

An A-LDO regulates the output voltage V_{OUT} by controlling the gate voltage V_G of the power transistor, while a D-LDO regulates V_{OUT} by controlling the number n of on/off power switches. Besides, the S-LDO regulates its V_{OUT} by modulating the duty cycle D of the power transistor. We can easily get the expressions for the output current I_{OUT} and the regulating factors: V_{G}, n, and D.

For the A-LDO,

$$I_{\mathrm{OUT}} = V_G \times g_m \tag{4}$$

For the D-LDO,

$$I_{\mathrm{OUT}} \approx n \times I_{\mathrm{UNIT}} \tag{5}$$

For the S-LDO,

$$I_{\mathrm{OUT}} = D \times I_{\mathrm{SW}} \tag{6}$$

where g_m is the transconductance of the analog power transistors related to its load current, I_{UNIT} is the unit current conducted through a single digital power switch cell in a D-LDO, and I_{SW} is the current conducted through the whole switching power transistor in an S-LDO.

In terms of output regulation continuity, analog control and switching control are continuous, while the digital control is of course discrete. In order to ensure the charge balance in the output, the control code of the D-LDO usually varies between

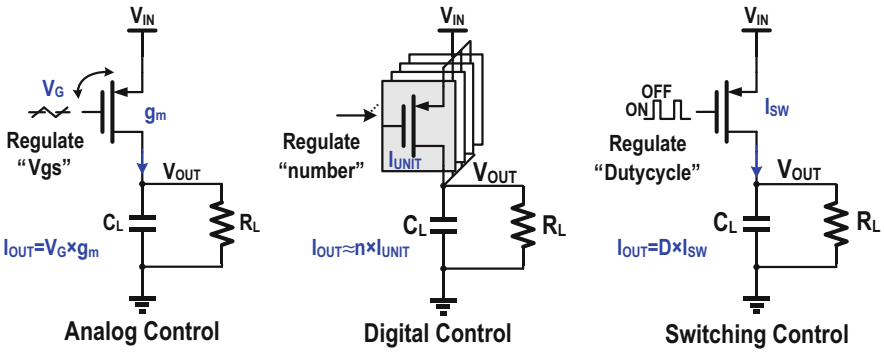

Fig. 3 LDO power stages with analog, digital, and switching control schemes

one and more adjacent codes. This is the limit cycle oscillation (LCO) in the D-LDO [10]. For a smaller LCO ripple, the simplest method uses a lower-resolution quantizer or dead-zone control but sacrificing the output accuracy. Unlike the digital control, the analog control and switching control can continuously regulate the output current, making it much easier to achieve high output accuracy. Besides, it is also easier to obtain a wide load range for the analog and switching control.

As discussed before, in the low V_{IN} condition, for the analog power stage, the gate voltage V_G needs to maintain a certain voltage (>100 mV) in order that the output of the error amplifier can be in a normal operation range for a sufficient loop gain. Nevertheless, the gate voltage of the digital power transistor or the switching power transistor can be 0 V. The switch-like power transistor can conduct more current than the analog power transistor, thus saving silicon area. Additionally, the digital power and the switching power stages are friendly to process scaling.

The frequency compensation is the key part of an LDO design. It is necessary to ensure that the LDO can remain stable over a wide load range. We can derive the transfer function of the three power stages; in the case of the analog power stage, it is

$$A_{\mathrm{VA}} = \frac{g_m R_O}{1 + sR_O C_L} \tag{7}$$

where C_L is the output capacitor. Considering the output impedance R_P of the power transistors, we can obtain the output impedance R_O. Generally, R_O and R_L have a roughly linear relationship, simply as

$$R_O = R_P // R_L \approx K \times R_L. \tag{8}$$

Assuming that the power transistors are in the saturation region, then

$$g_m = \sqrt{2\mu_p C_{\mathrm{OX}} \frac{W}{L} I_D} = \sqrt{2\mu_p C_{\mathrm{OX}} \frac{W}{L} \times \frac{|V_{\mathrm{OUT}}|}{R_L}} \tag{9}$$

where μ_p is the mobility of the charge carriers and C_{OX} is the gate-oxide capacitance per unit area. $|V_{\mathrm{OUT}}|$ represents the DC value of the output voltage. W and L are the width and length of the power transistor, respectively. Combining Eqs. (7)–(9), we have

$$A_{\mathrm{VA}} = K \times \sqrt{2\mu_p C_{\mathrm{OX}} \frac{W}{L} \times |V_{\mathrm{OUT}}| \times R_L} / (1 + sR_O C_L). \tag{10}$$

assuming that the output pole is always within the bandwidth. With two orders of reduction of R_{O}, the output pole also moves to two orders of higher frequency, but the gain of the output stage reduces only ten times, resulting in a significant increase in the bandwidth of the analog LDO under a heavy load condition. Then, the parasitic gate pole p_{G} of the power transistors may be within the bandwidth, resulting

in a sharp deterioration of the phase margin. The variations of bandwidth and p_{OUT} greatly affect the loop stability.

Therefore, the gate pole p_G, the load-dependent g_m, and the output pole p_{OUT} are the main factors leading to LDO compensation difficulties. Besides, it is necessary to consider the process, voltage, and temperature (PVT) variations, which complicate the compensation. Prior analog LDOs usually require a complicated compensation using pole-zero tracking to achieve good stability over the full load range [11, 12].

In the steady state, the input and output voltages are constant; thus, the digital power stage and the switching power stage can be equivalent to a constant current source. For the digital power stage, the transfer function is

$$A_{\mathrm{VD}} = \frac{I_{\mathrm{UNIT}} R_O}{1 + sR_O C_L} \tag{11}$$

For the switching power stage, the transfer function is

$$A_{\mathrm{VS}} = \frac{I_{\mathrm{SW}} R_O}{1 + sR_O C_L} \tag{12}$$

where I_{UNIT} is the unit current conducted through a single power switch cell and I_{SW} is the current conducted through the whole switching power transistor. Since they are all fixed values when V_{IN} and V_{OUT} are constant, the digital output stage has a constant gain bandwidth product. With the output pole placed within the loop bandwidth, we can easily get a constant bandwidth that does not change with the load current, which is very useful for improving the stability and simplifying the compensation. Therefore, the digital power stage and the switching power stage are more suitable for high-current applications.

In addition, for the high-current large area applications, we should pay attention to the integration scheme of the LDO. This has great influence on the choice of the LDO's control methods. With the LDO placed on the side of the load with a centralized power stage, due to the small area of the LDO, the contact surface between the power transistor and the digital load is quite small. Then, the limited metal width would have difficulties in allowing a large load current to pass, which may result in electromigration (EM) issues and a large IR drop (Fig. 4).

The distributed power stage can increase the top metal resource and reduce the IR drop. For the long-distance signal transmission, digital signals have certain advantages over the analog signals, and we can add digital buffers on the signal path. Therefore, this is another important reason why we chose the digital/switching power stages for high current applications.

In addition to the advantages described above, the digital/switching power stages also have some disadvantages. The first is the output ripple, especially for the switching power stage. In order to reduce the output ripple, the switching LDO usually needs a large output capacitor and high switching frequency. The large output capacitor restricts its on-die applications and the high switching frequency leads a large quiescent current.

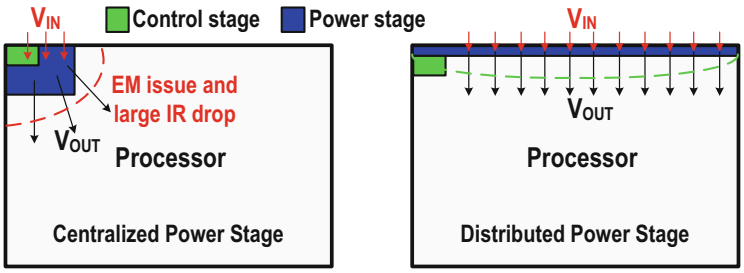

Fig. 4 Centralized power stage and distributed power stage

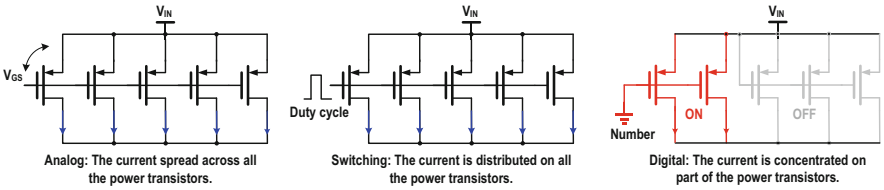

Fig. 5 Reliability issue comparison for the analog, digital, and switching LDOs

For the digital power stage, we should pay attention to reliability issues. As we know, for the analog/switching power stages, the load current and heat spread across all the power transistors. However, for the digital power stage, the load current and heat concentrate at the "on" power transistors (Fig. 5). In a large dropout voltage condition, the unit current through each power transistor significantly increases, making the load current and heat even more concentrated, which may cause serious EM and self-heating problems. We cannot solve easily these reliability issues with the layout. Reference [13] used a code roaming algorithm, and Refs. [14, 15] mitigated the EM and self-heating issues by limiting the current through the power transistor. According to the above analyses, Table 1 summarizes the specifications of the three power stage types.

We can choose the appropriate power stage according to the application requirements. It is also possible to combine two different power stages or control methods for better performance. For example, Ref. [16] adopts a digital/analog power stage for power supply rejection (PSR) improvement and LCO reduction; Ref. [17] obtains 5.6 mV/mA load regulation and a 20,000× dynamic load range by adding a sub-LSB switching power transistor to the original digital power stage; the power stage in Ref. [18] combines digital control and switching control, achieving 1 mA–6.4 A wide load range, when comparing it with a pure switching control, and then leading to a driving current significant reduction.

Table 1 Power stage comparison

	LDO		
Topology	Analog	Digital	Switching
Regulation fineness	Continuous (voltage)	Discrete (number)	Continuous (duty cycle)
Output accuracy	√	×	–
Large load capability	×	√	√
Wide load range	√	×	√
Low input power stage	×	√	√
Distributed power transistors	×	√	√
Self-heating and EM	√	×	√
Output ripple	√	×	××

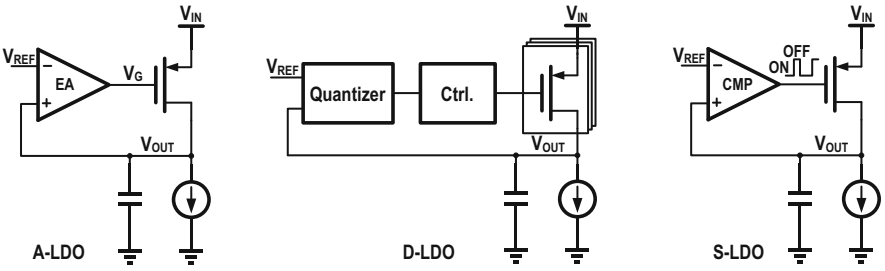

Fig. 6 Three controller types for LDOs

2.2 LDO Controller

Figure 6 shows the simple schematics of the three LDOs: A-LDO, D-LDO, and S-LDO. The A-LDO contains an error amplifier and RC compensation network, the D-LDO controller consists of a quantizer and control logic, while the switching LDO requires a high-speed comparator. Table 2 summarizes the characteristics of the three controller types. We will discuss the three controllers in terms of output voltage accuracy, transient response, and design complexity.

The output voltage accuracy is a very important indicator for the LDO, usually affected by two aspects: one is the load/line regulation; the other is the manufacturing offset error. Due to the high-gain error amplifier (EA), the A-LDO can usually obtain a good load/line regulation, and the amplifier can easily achieve small offset through common centroid-matched transistors. However, in a low V_{IN} condition, the limited voltage headroom increases the difficulty of designing a high-gain EA. To solve this problem, we can use a heterogeneous power supply: the power supplies of the LDO controller and the power stage are different. For example, in many SoCs, there is a 1.8 V supply commonly used for I/O blocks and analog circuits, such as the bandgap reference, temperature sensors, and oscillators. We can use the 1.8 V supply

Table 2 Controller comparison

	LDO		
Topology	Analog	Digital	Switching
High output accuracy	√	×	√
Ultra-low quiescent current	√	√	×
Transient response time	$\approx\frac{1}{\mathrm{BW}}+T_{\mathrm{SR}}$	$\approx\frac{1}{\mathrm{BW}}+T_S$	$\approx\frac{1}{\mathrm{BW}}$
Design challenges	Compensation and energy-efficient driver	Control logic, reliability consideration	Driver loss and output ripple

as the controller supply and the 1 V supply as the power stage supply. Of course, we could use a charge pump to generate a higher voltage for the controller.

The D-LDO quantifies the error between the output voltage V_{OUT} and the reference voltage V_{REF} and then transmits the digital error information to the control logic [19]. The output accuracy depends on the quantization error. A shift register-based D-LDO [20] consists of a clocked comparator acting as a one-bit analog-to-digital converter (ADC), and a bidirectional shift register (SR) serving as an integrator, which can obtain high output accuracy but slow transient response. A multi-bit ADC-based D-LDO can obtain a much faster transient response. However, the quantizer resolution limits the output accuracy. Both [14, 21] adopt a six-bit ADC, of which the quantization resolution is approximately 5–7 mV. Further increasing the ADC resolution will exponentially complicate the digital proportional-integral-derivative (PID) controller design, which may require higher power consumption and area. So far, there is no D-LDO achieving a load regulation of <5 mV/A.

Figure 7 shows commonly used quantizers that we can divide into voltage domain [22, 23] and time domain [24]. The voltage domain quantizer utilizes multiple comparators and voltage references to detect V_{OUT} changes ([13, 22] have 6 comparators, [23] has 13 comparators). Still, the input offset voltage of the comparators may reduce the detection window or even cause sub-window overlapping. In order to obtain high output accuracy and maintain robust operation, the comparator offsets require calibration to guarantee a monotonic detection. An event-driven D-LDO [18] obtained fine regulation by using an analog amplifier and a two-bit only current mirror-based flash analog-to-digital converter (ADC), but it requires a 1μF output capacitor to filter the output ripple to less than the minimum detection window of the ADC, limiting its fully integrated application.

The time-domain quantizers using time-to-digital converters (TDCs) and voltage-controlled oscillators (VCOs) are friendly to process scaling and can work well at low V_{IN} voltages, but they are sensitive to PVT variations. References [14, 24] utilized a pair of VCOs to resist PVT variations, which generate additional one cycle latency to the loop and still have local mismatches between the two VCOs. For high output accuracy, a piecewise multipoint calibration is usually necessary. Reference [21] only uses one six-bit TDC, but it requires a complex active calibration for the target code. Calibration is necessary for digital LDOs to obtain high output accuracy

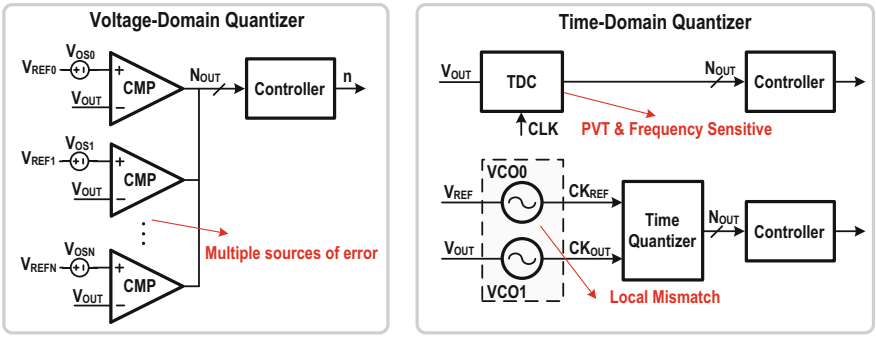

Fig. 7 Voltage domain quantizer and time-domain quantizer in DLDOs

and robust operation but increases the cost and design complexity. In contrast, by using an error amplifier, the analog LDOs can easily achieve high output accuracy for its continuous regulation and high gain, without any calibration.

For the switching LDO, with the duty cycle continuously regulated, it can obtain high output accuracy by using a high-speed and high-accuracy comparator or combining it with the analog error amplifier. The S-LDO in Ref. [25] achieved 1.5 mV/A load regulation, and Ref. [26] also obtained an excellent load regulation of 1 mV/A.

The transient response is also another important indicator of the LDO. We evaluate the transient speed of an LDO by the response time T_{R}, defined as in [27]:

$$T_R = C_{\mathrm{OUT}} \times \frac{\Delta V_{\mathrm{OUT}}}{I_L} \times \frac{I_Q}{I_L}, \tag{13}$$

where ΔV_{OUT} is the resultant output voltage spike, I_{L} is the maximum load current, and I_Q is the quiescent current. We can approximate T_{R} as

$$T_R \approx \frac{1}{\mathrm{BW}} + T_{\mathrm{SR}} + T_S, \tag{14}$$

where BW is the loop bandwidth of the LDO, T_{SR} is the delay from a limited slew rate, and T_{S} is the delay from the voltage error sampling.

Frequency compensation is also a key part of an analog LDO design, especially for high current wide bandwidth applications. The A-LDO can detect the V_{OUT} variation in real time and almost $T_{\mathrm{S}} \approx 0$. The loop bandwidth and the gate-drive slew rate limit the transient response of an A-LDO. Then, flipped voltage follower (FVF)-based LDO is the most common in fast transient applications. For example, Ref. [4] obtained a sub-ns transient response due to >400 MHz loop bandwidth and an enhanced super source follower. In general, for a fast transient response, a high slew rate requires a large current. Designing an energy-efficient driver is another

challenge. The common methods include adaptive biasing [28], class-AB driver [29], and supper source follower [4].

To implement feedback control, D-LDOs adopted a range of control schemes, including integral feedback [20], dead-zone control [30], linear PID control [21], feedforward control [31], and nonlinear control [13, 32]. I-control can achieve relatively high output accuracy but with slow transient response. Dead-zone control sets a dead-zone around V_{REF} and can remove the output voltage ripple, but the size of the dead-zone requires a cautious setting to avoid window overlapping. The PID control is a comprehensive feedback control scheme. The P-control can improve the transient response by providing an output current proportional to the V_{OUT} variation. The D-control helps to reduce the sharp V_{OUT} spikes. Similar to D-control, the feedforward scheme measures the V_{OUT} slope at the beginning of a droop event and then estimates the necessary amount of charge, which can further improve the load transient performance. For nonlinear control, when V_{OUT} drops to a certain threshold, it will suddenly turn on parts of the power transistors. Nevertheless, it can constitute an alternative way to minimize voltage droop during large load transients. Yet, this nonlinear trend may easily produce overshoot spikes on V_{OUT}. In addition, according to the analysis from Sect. 2.1, for wide input/output voltage range applications, D-LDOs need to add some control methods to solve the reliability issues of the power transistors in large dropout conditions.

The D-LDO has no slew rate limitation, but it requires several clock cycles to sample the output error and process the error information. For the shift register-based D-LDO in [20], the response time of the linear search control is N. The successive approximation D-LDO [17] achieves a faster response time of $N/2^{\mathrm{N}}$. By using a flash ADC [13] or an inverter-chain TDC [21], we can reduce the response time to 1–-2 cycles. The higher operation frequency can improve the transient performance, but increasing power consumption, and also we have to consider the impact on stability.

A simple switching LDO operates in a hysteretic mode. It uses a high-speed comparator to amplify the error between V_{REF} and V_{OUT} into binary levels, with the comparator output signal applied to the switching power transistor. The propagation delay of the comparator and gate driver determines the transient response time, which is usually in sub-nanosecond or even in tens of picoseconds. In principle, since an error of a few mV is sufficient to drive the comparator output into a binary level, the DC load regulation error can be very small but related to the loop delay. The main drawback of an S-LDO is its coherent output ripple. It usually needs a large load capacitor and high switching frequency to reduce the output ripple. Since all the power transistors are in a switching state, there will be a large driving current. Therefore, we can only find the S-LDO in high-current application scenarios.

3 Analog-Digital Hybrid LDO

Recently, hybrid LDOs (H-LDOs) gained much research and development interest for combining the advantages of both analog and digital architectures [33]. According to the hybrid methods, we can divide the analog/digital hybrid LDOs into three categories.

The first is the D-LDO with an analog-assisted loop in the digital feedback control [34, 35]. From Fig. 8, the R_C and C_C form a high-pass filter to improve the load transient response. A favorable feature of this structure is that the baseline digital loop can work normally with a slow clock frequency, even if there is no analog loop. Also, since the analog and digital loops have largely different bandwidth, basically, they will not affect each other, maintaining low design complexity.

The second is the H-LDO with individual digital and analog loops in Fig. 9. The power stage consists of a digital power stage in parallel with an analog power stage [16], or it can have a power transistor with two different operation states [36]. This structure can support the two loops working simultaneously or utilizes a finite-state

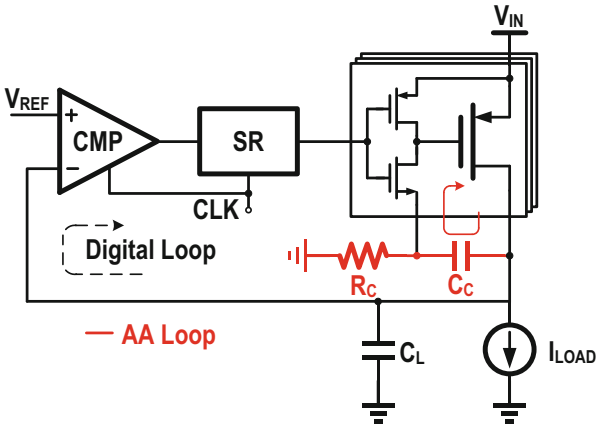

Fig. 8 A D-LDO with the analog-assisted loop in the digital feedback control

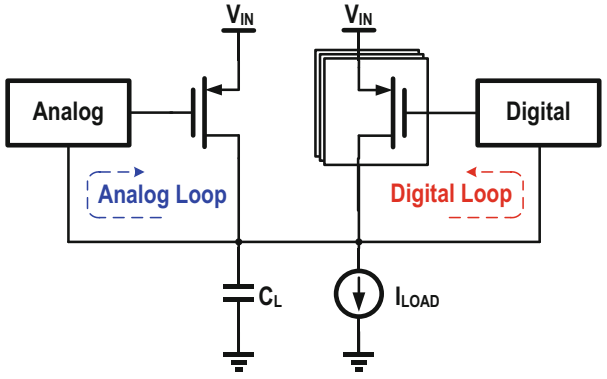

Fig. 9 A hybrid LDO with the individual digital and analog loops

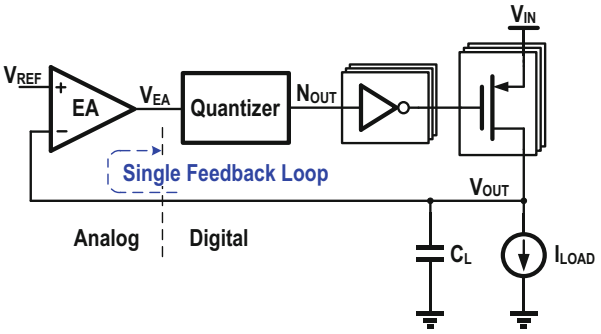

Fig. 10 An H-LDO with hybrid signal processing in a single feedback loop

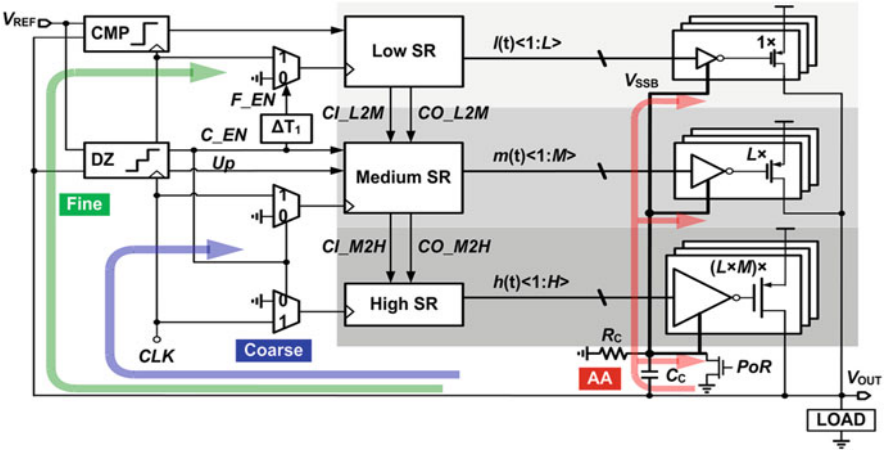

Fig. 11 Overall architecture of the analog-assisted tri-loop DLDO proposed in [34]

machine (FSM) to control the operation of the two loops to obtain the best steady-state or dynamic performance. An obvious feature of this structure is that either loop can work independently [37, 38].

The third refers to the hybrid signal processing in a single loop, where the analog control and the digital control belong to the same feedback loop. Figure 10 presents a hybrid control architecture [39]. This structure combines an analog error amplifier, a digital voltage sensor (TDC), and a digital power stage, mainly to meet the high-current application requirements with high output accuracy. Next, we will introduce hybrid LDO design examples for each of the three categories.

3.1 Analog-Assisted Digital LDOs

Figure 11 presents an analog-assisted (AA) tri-loop D-LDO [34]. Different from a conventional D-LDO, the V_{SSB} node of the gate driver of the power transistors does

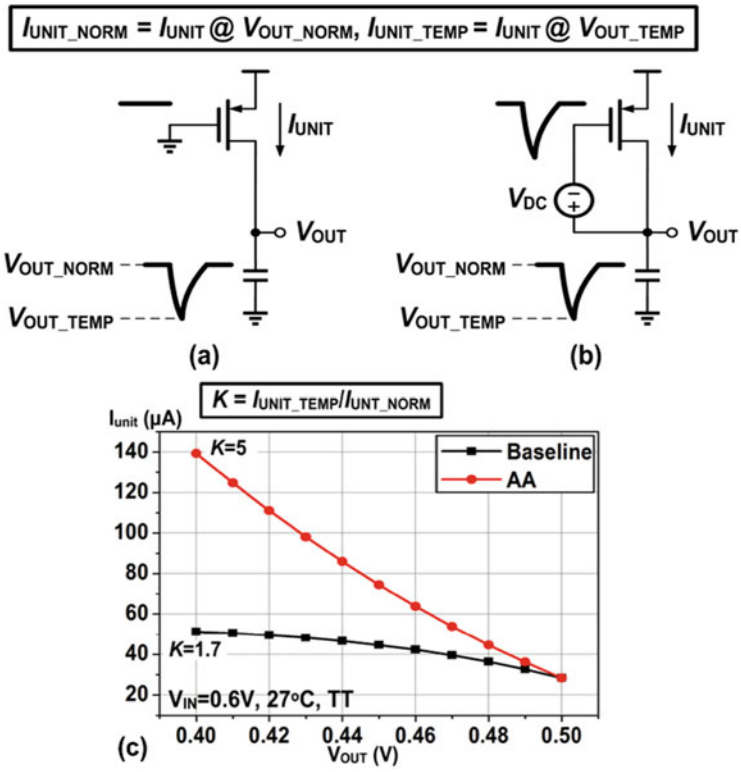

Fig. 12 Equivalent circuits of the (**a**) baseline D-LDO, (**b**) AA-loop D-LDO, and (**c**) simulated unit current comparison [34]

not connect to GND but is DC-biased to GND with a relatively large resistor R_C and AC coupled with V_{OUT} through a coupling capacitor C_C.

When a load transient occurs, the V_{OUT} droop coupled with the gate of the "on" power transistors can generate a larger instantaneous V_{GS} change and result in larger unit current I_{UNIT}. A factor K investigated in [34] evaluates the maximum unit current variations at the transient instant in the AA and the baseline schemes. Figure 12 shows the equivalent power stage circuit of the baseline and the AA schemes. When V_{OUT} changes from V_{OUT_NORM} to V_{OUT_TEMP}, only the V_{DS} of the power transistors changes in the baseline, while both the V_{GS} and V_{DS} change in the AA-Loop. Figure 12c displays the simulated results, demonstrating the effectiveness of the AA scheme. With V_{OUT} swept from 0.5 V to 0.4 V, we can observe $5 \times I_{UNIT}$ in the AA scheme and only obtained $1.4 \times I_{UNIT}$ in the conventional structure. Obviously, a larger instantaneous unit current can significantly reduce the V_{OUT} droop. A similar phenomenon can happen during the load current down transient.

Figure 13 exhibits the working principle of the tri-loop controlled D-LDO. Once the load transient occurs and the V_{OUT} exceeds the dead zone, coarse tuning activates, with a "C_EN" signal generated. When C_EN = 1, the power transistors

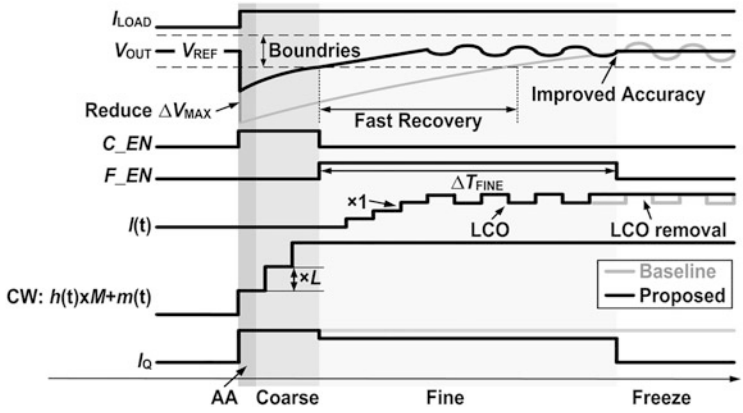

Fig. 13 Working principle of the trip-loop LDO

shift by L counts in each cycle, rapidly increasing the output current and decreasing the recovery time. When V_{OUT} is within the dead zone, the coarse control terminates, and the fine-tuning shifts by one count per cycle. At this moment, C_EN = 0 and F_EN = 1. After several cycles of fine-tuning, the LDO will enter a freeze mode and stop all the SRs for saving steady-state quiescent current, and then we can eliminate the LCO.

For the above PMOS power stage, there are only a small number of power transistors turned-on in light load; thus, the AA-loop only works on these very few power transistors which is insufficient to compensate a large load transient. Reference [35] utilizes a NMOS power stage with an AA scheme to improve the load transient performance. Figure 14 shows the NMOS power stage with a NAND-based AA loop (NAP). When V_{OUT} drops, the NMOS source follower naturally provides more current than the PMOS power stage. V_{CP} is one of the input signals of the NAND, DC biased to $2 \times V_{DD}$ by a resistor R_1 and AC coupled with the output voltage. When V_{OUT} has an undershoot voltage, the PMOS M_1 with relatively large size can amplify the coupled AC signal to the gate of the NMOS power transistor. With a 20 mA load step with 3 ns edge time, the undershoot of the PMOS AA D-LDO is close to 426 mV, while the NMOS AA D-LDO has a smaller undershoot of 244 mV due to the NMOS intrinsic response. The NMOS D-LDO with a NAP loop obtains a superior transient response of only 96 mV undershoot.

3.2 An Analog-Proportional Digital Integral Multiloop Digital LDO

The AA-loop is a passive scheme to improve the transient response by increasing instantaneous current. Another scheme has directly in parallel a fast analog

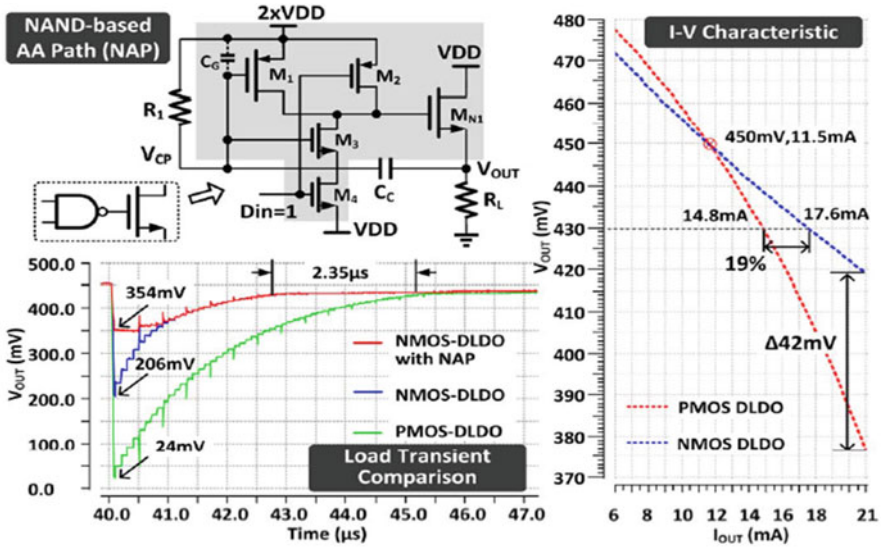

Fig. 14 NMOS power stage with NAND-based AA loop [35]

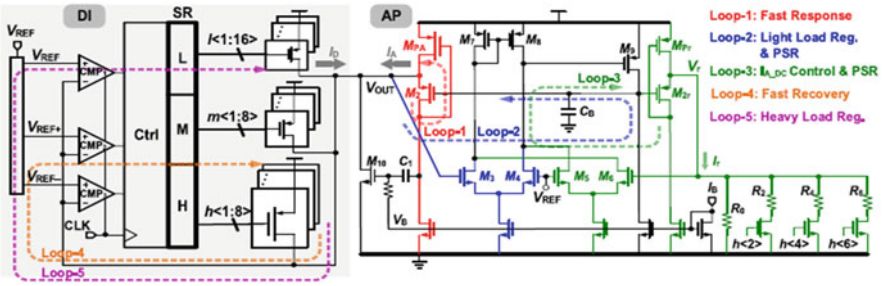

Fig. 15 The D-LDO with analog-proportional and digital integral control [16]

proportional loop with the digital integral loop. Figure 15 reveals a digital LDO with analog-proportional (AP) and digital integral (DI) control [16].

The traditional SR-based D-LDO is essentially an integral control, which can offer a high DC accuracy with low power consumption but also with slow response. The proportional control can respond fast but has a large DC error in the steady state. By combining these two controls, we can simultaneously obtain a fast transient response and high DC accuracy. We can implement the proportional control in an analog way.

The FVF-based LDO is a good choice for energy-efficient proportional control [2]. The analog power transistor M_{PA} and the common-gate PMOS M_2 compose the fast Loop-1, to handle the fast transient. The FVF circuit can still operate normally in a low V_{IN} voltage. However, the AP part may take over all the current at a very light load condition; thus, we add Loop-2 for the load current-sharing regulation. Loop-2

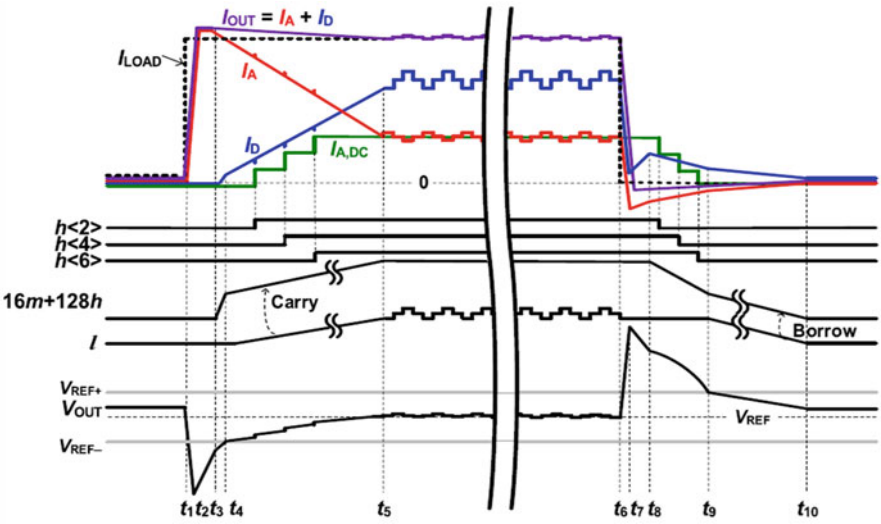

Fig. 16 The timing diagram of the AP-DI LDO proposed in [16]

consists of M_{PA}, M_2, and a two-stage error amplifier. We set the gate voltage of M_2 based on the difference between V_{OUT} and V_{REF}. Although the gain of Loop-2 may not be high, it can help to improve the PSR and output accuracy under light load conditions.

The digital integral part consists of three shift register-controlled power transistor arrays. Loop-4 is a coarse tuning, composed of M and H subsections. When V_{OUT} exceeds the preset boundaries (V_{REF-} to V_{REF+}), the outputs of CMP_2 and CMP_3 trigger a fast regulation, in which the active number of power switches changes by 16 units every cycle. When V_{OUT} is within the (V_{REF-} to V_{REF+}) boundary, Loop-5 starts work, which is a fine-tuning with a high DC gain. The active number changes according to the output of CMP_1. Figure 16 presents the timing diagram of the AP-DI LDO proposed in [16].

Figure 17 shows the simulated load transient waveforms for load steps of 0–10 mA within a 5 ns edge time, where $V_{IN} = 0.6$ V, $V_{REF} = 0.55$ V, and CLK = 5 MHz. With an AP-only LDO, the undershoot is 70 mV but with a large DC error. The DI-only LDO obtains good DC accuracy but a large undershoot of 550 mV, as well as a large LCO. The proposed AP-DI LDO not only delivers a fast transient response and good output accuracy but also eliminates the LCO in light load.

Figure 18 presents the PSR improvement of the AP-DI LDO work in [16], where $V_{IN} = 0.75$ V, $V_{OUT} = 0.7$ V, and $I_{LOAD} = 10$ mA. It is clear that the AP loop can significantly improve the PSR and Loop-2 is very effective.

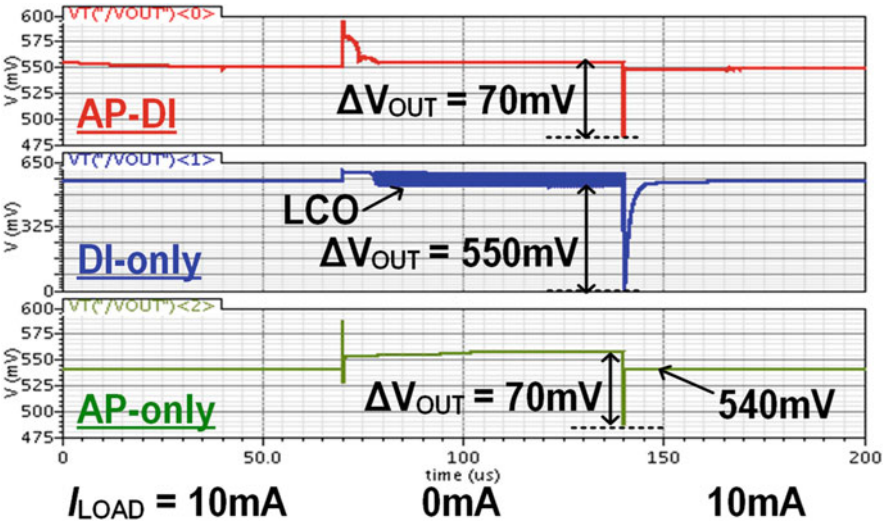

Fig. 17 Simulated load transient waveforms with AP-DI, DI-only, and AP-only conditions

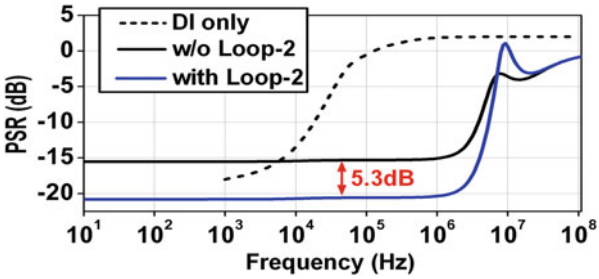

Fig. 18 Simulated PSR comparison for DI only and DI-AP with or without Loop-2

3.3 A 1.2A Calibration-Free Hybrid LDO with in-Loop Quantization

The hybrid LDOs in Sects. 3.1 and 3.2 are all for low-current applications. According to the discussions in Sect. 2.1, the digital power stage is appropriate for high-current and wide bandwidth applications. However, for high output accuracy and robust operation, calibration is necessary but increases the cost and design complexity. In contrast, analog LDOs utilize an analog amplifier that can easily achieve high output accuracy for its continuous regulation and high gain, without any calibration. Thus, we can try to combine an analog error amplifier and digital power stages to achieve large load capability and high output accuracy.

Figure 19 presents the overall architecture of the hybrid LDO with in-loop quantization proposed in [26]. Its composition includes an analog EA with RC compensation, a five-bit TDC, digital power stage, and an auxiliary constant current (ACC) circuit. Unlike the conventional DLDO which directly quantizes the output

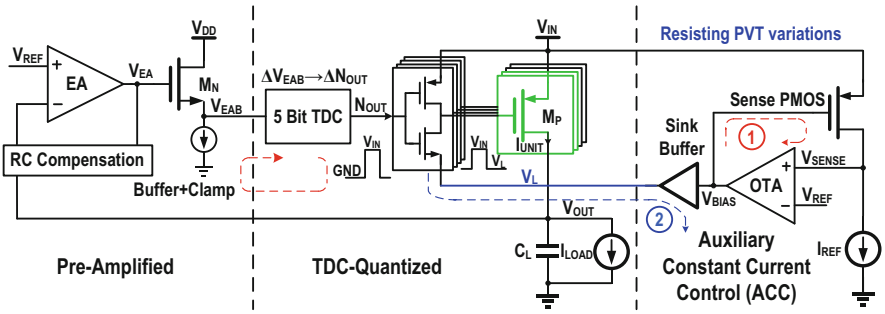

Fig. 19 Overall architecture of the in-loop quantization hybrid LDO proposed in [26]

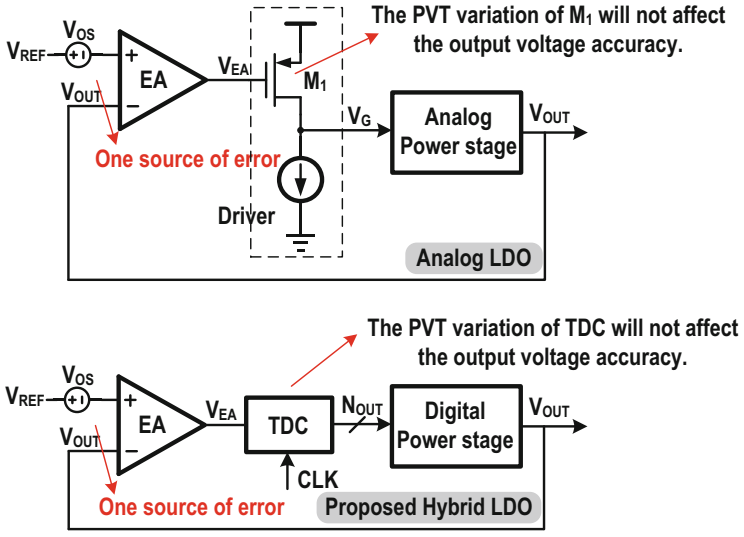

Fig. 20 In-loop quantization

voltage, the proposed LDO utilizes an analog EA to pre-amplify the error between V_{OUT} and V_{REF}. Then, a five-bit TDC quantizes the buffered EA signal V_{EAB} and outputs a thermometer code directly to control the digital power transistors.

Figure 20 illustrates the LDO structure comparison. When compared with the traditional analog LDO, this hybrid LDO replaces the analog driver with a digital TDC and replaces the power stage with a digital power stage. The inverter chain-based TDC is in the middle of the control loop; although it is sensitive to PVT variations, it will not affect the output accuracy benefitting from the closed-loop control because the error amplifier output can automatically track the PVT variations.

Since the current I_{UNIT} through a unit power transistor varies a lot in a large dropout condition, it may cause reliability and stability issues [13, 14]. We

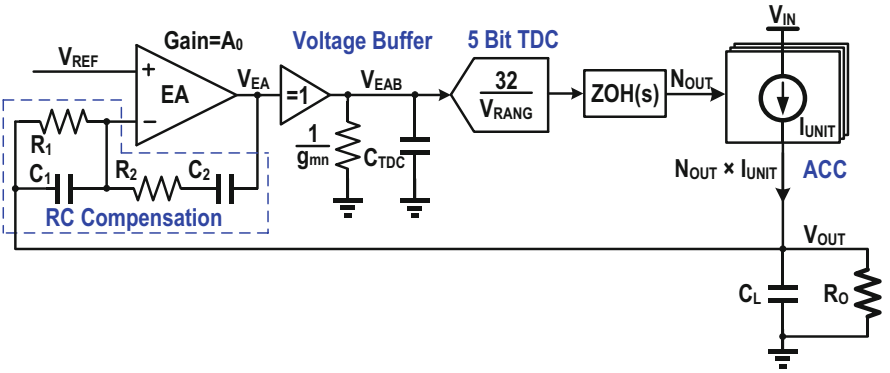

Fig. 21 Small-signal analysis of the LDO proposed in [26]

implement an auxiliary constant current (ACC) circuit to keep I_{UNIT} constant. The ACC circuit consists of two loops, and its output voltage V_L has sink capability using the adaptive "GND" from the pre-driver. The control signals of the power transistors are actually in the $[V_{\mathrm{IN}} - V_L]$ domain. The V_L voltage tracks PVT variations to ensure that the unit current through the power transistor is equal to the defined value.

The traditional D-LDOs generally utilize the PID controller for loop stability. In the proposed hybrid LDO, we used an RC compensation to replace the digital PID controller and simplify the design by eliminating the analog-to-digital converter. Figure 21 displays the small-signal model of the hybrid LDO proposed in [26]. The RC compensation consists of the resistors R_1 and R_2 and capacitors C_1 and C_2. Since the TDC's frequency far exceeds the loop bandwidth, we can simplify the five-bit TDC to a continuous voltage-to-digital model. Then, the transfer function of the loop is

$$H(s) = \frac{\frac{N \times I_{\mathrm{UNIT}}}{V_{\mathrm{RANG}}} A_0 R_O (1 + sR_2C_2)(1 + sR_1C_1) \times \frac{1 - e^{-TS}}{sT}}{[1 + s(A_0 + 1)R_1C_2]\left(1 + s\frac{R_2C_1}{1+A_0}\right)\left(1 + s\frac{C_{\mathrm{TDC}}}{g_{mn}}\right)(1 + sR_OC_L)} \tag{15}$$

There are three effective poles and two zeros in the whole loop.

4 Multiphase Switching LDO

4.1 Ripple Analysis

The switching LDO can drive power transistors fast and accurately. However, it usually needs high switching frequency and a large capacitor to mitigate its output ripple, which restricts their application in low-power and low-cost scenarios. A traditional switching LDO with hysteretic control utilizes a high-speed comparator

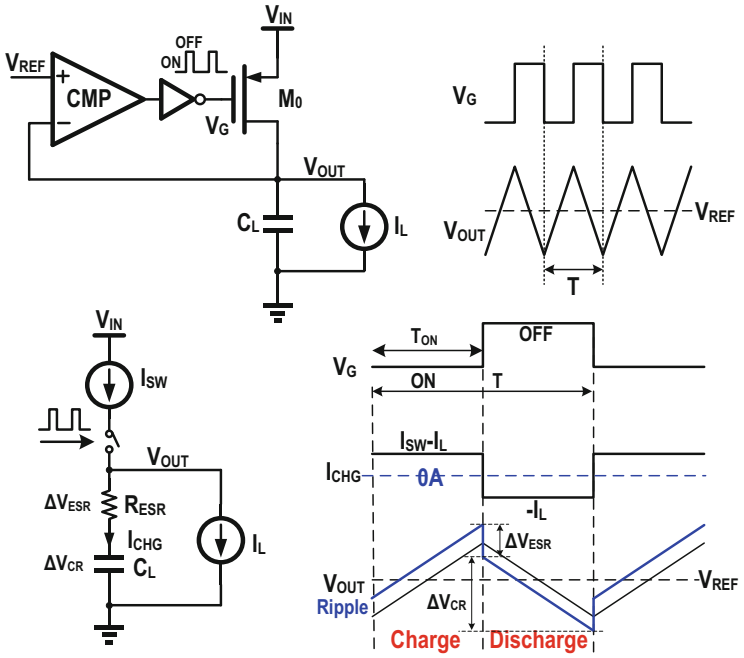

Fig. 22 The charge-discharge model of a traditional hysteretic switching LDO

to amplify the errors between V_{REF} and V_{OUT} into binary levels. The comparator output controls the power transistor for turning it on and off, regulating the output current. Figure 22 shows the charge-discharge model of a hysteretic switching LDO.

I_{SW} is the current through the power transistor when turned on, and I_L is the load current. In steady state, according to the charge-balance principle,

$$I_{\mathrm{SW}} \times T_{\mathrm{ON}} = I_L \times T \tag{16}$$

The duty cycle D is

$$D = \frac{T_{\mathrm{ON}}}{T} = \frac{I_L}{I_{\mathrm{SW}}}. \tag{17}$$

The output ripple consists of two parts: the capacitor charging-discharging component ΔV_{CR} and the contribution of its ESR that is ΔV_{ESR}:

$$\Delta V = \Delta V_{\mathrm{CR}} + \Delta V_{\mathrm{ESR}} = (1-D)D \times I_{\mathrm{SW}}/(C_L \times F) + I_{\mathrm{SW}} \times R_{\mathrm{ESR}} \tag{18}$$

where $F = 1/T$ is the switching frequency. In Eq. (18), the amplitude of the output ripple is related to the transistor current strength I_{SW}, switching frequency F, load capacitor C_{L}, and load current I_L. Assuming that $D = 50\%$, $I_{\mathrm{SW}} = 1\mathrm{A}$, $F = 1\mathrm{GHz}$,

Table 3 The K ratio comparison

	[40]	[25]	[41]
Output capacitor C_L (nF)	750	481	2.7
Load capability I_L (A)	11.9	12	0.17
$K = C_L/I_{MAX}$ (nF/A)	63.02	40.08	15.88

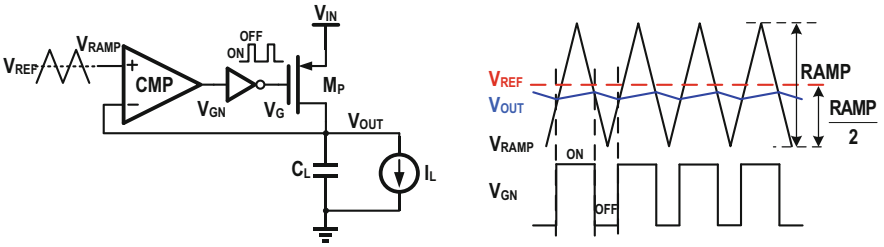

Fig. 23 The PWM control switching LDO with a triangle input signal

and $R_{ESR} = 5\text{m}\Omega$, the output capacitor C_L needs to be larger than 25 nF for a 15 mV output ripple. Considering the PVT variations of I_{SW}, the output capacitor should be even larger. Higher switching frequency can reduce the output ripple, but it increases the driver loss.

Table 3 presents the load capability and the output capacitor comparison of the prior hysteretic switching LDOs. References [25, 40] have large load capability and correspondingly need large output capacitors (481 nF in [25] and 750 nF in [40]), which require a special SOI process or a deep-trench process. Reference [41] fabricated in 16 nm CMOS with a 2.7 nF load capacitor can only drive a load current of 170 mA. We consider the ratio of output capacitance over the maximum load current $K = C_L/I_{MAX}$ as the key performance index of switching LDOs. The K values in Table 3 are 63.02 nF/A, 40.08 nF/A, and 15.88 nF/A, respectively. Such large K values restrict the application of hysteretic switching LDOs.

4.2 RAMP-Based PWM Control

A hysteretic switching LDO does not fix the switching frequency, only determined by the loop propagation delay. In order to fix the switching frequency, we use a triangle wave to replace the DC reference voltage, as presented in Fig. 23.

When $V_{RAMP} > V_{OUT}$, the comparator output will turn on the power switch and V_{OUT} rises. When $V_{RAMP} < V_{OUT}$, the comparator output will turn off the power switch and V_{OUT} drops. The switching frequency is equal to the triangle wave frequency. The V_{RAMP} amplitude is usually much larger than the output ripple. Ignoring the impact of the output ripple, we can express the duty cycle D as

$$D = \left(\frac{\text{RAMP}}{2} + V_{\text{REF}} - V_{\text{OUT}}\right)/\text{RAMP} = \frac{1}{2} + \frac{V_{\text{REF}} - V_{\text{OUT}}}{\text{RAMP}} = \frac{I_L}{I_{\text{SW}}} \tag{19}$$

Equation (19) reveals the linear relationships between I_L, V_{OUT}, D, and RAMP.

4.3 Four-Phase PWM Control

With the frequency of the PMW (pulse width modulation) control fixed, we can utilize a four-phase triangle wave and split the total current I_{SW} into four small currents (Fig. 24), with charging interleaved. When compared with the single-phase PWM control, the four-phase PWM control can reduce the maximum output ripple by 16 times.

4.4 Current Balancing

The current-sharing can be a serious issue in multiphase control, which determines the ripple cancellation effect. For the four-phase switching LDO,

$$I_L = \left(\frac{I_{\text{SW}}}{4} \times D_0\right) + \left(\frac{I_{\text{SW}}}{4} \times D_1\right) + \left(\frac{I_{\text{SW}}}{4} \times D_2\right) + \left(\frac{I_{\text{SW}}}{4} \times D_3\right) \tag{20}$$

The unbalanced current is

$$\Delta I = \frac{I_{\text{SW}}}{4} \times \Delta D \tag{21}$$

The input offset voltage of the comparator will cause a duty cycle error. Since a small error in D only causes small unbalanced current, we recommend calibrating the comparators for a good load sharing.

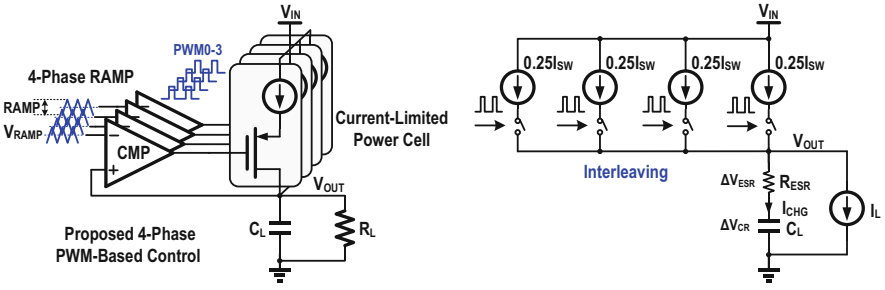

Fig. 24 The four-phase PWM control charging/discharging mode

4.5 *Dual-Loop Four-Phase PWM Control Switching LDO*

Since the reference input of the comparator becomes a triangle wave, the V_{OUT} voltage cannot obtain high DC accuracy. We add a high-gain error amplifier before the PWM controller to improve the output accuracy. Figure 25 shows the overall architecture of the dual-loop four-phase PWM switching LDO [26]. The resistor R_1 and capacitor C_1 constitute the loop compensation circuit, and we used R_F to realize the active voltage positioning (AVP) function. We can adjust R_F to obtain different AVP effects. In addition to the four-phase PMW control, we introduced two other ripple reduction techniques: (1) current-limited power cells acting as constant current source for resisting PVT variations and (2) hybrid fast-slow power transistors, with a ratio of 4:1.

Distinctive from conventional LDO designs that consider the controller and the power transistor as a whole, we can design such switching LDO like a Lego set. Each power cell has a load capability of 220 mA; after we design the controller, the switching LDO can scale to different load applications by increasing or decreasing the number of power cells, even without redesigning the main circuits and layouts, which is very flexible and convenient.

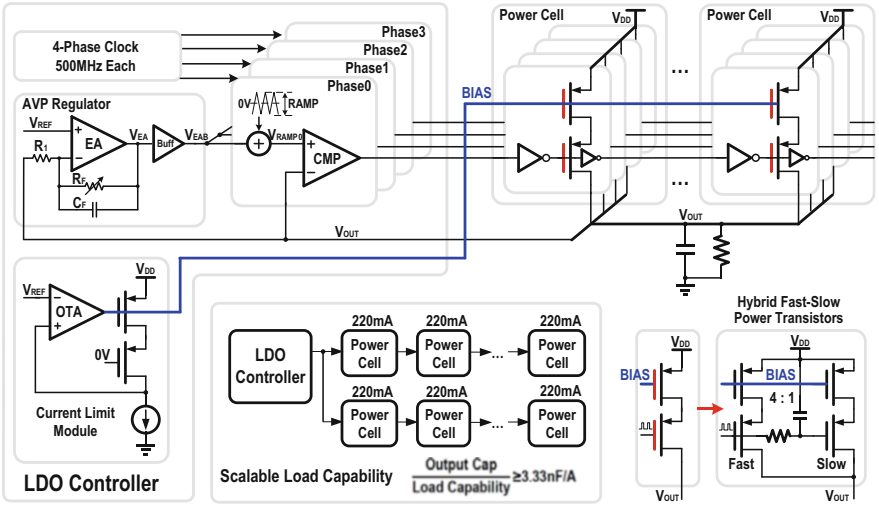

Fig. 25 Overall architecture of the dual-loop four-phase switching LDO in [26]

5 Conclusions

This chapter discussed the characteristics and design considerations of each of the three LDO types (analog, digital, switching) in terms of the power stage and the control methods, for integration in nanoscale processes. The conventional analog, digital, and switching LDOs all have some inherent shortcomings or limitations. Many recent research works obtained better performances by using a hybrid architecture that combined the advantages of different control schemes. Design example-1 adopts a high-pass analog-assisted loop to improve the transient response of a digital LDO. Design example-2 utilizes the analog-proportional and digital integral control for enhancing the PSR and improves the load transient response. In addition, by combining the analog error amplifier and the distributed digital power stage (example-3), or switching power stage (example-4), the two LDOs obtained ampere-level load current capability, as well as high output accuracy and fast transient response. In brief, there is no perfect architecture for all applications but only the most suitable architecture for a specific application. We need to choose the LDO structure based on the application requirements, not limited to specific control loop and power stage types.

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