Fully Integrated Switched-Capacitor Power Converters

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1 Introduction

In recent years, monolithic and highly integrated DC-DC power converters are in great demand for various low-power devices, like implantable, wearable, and portable devices [1]. Integrating a DC-DC power converter fully on-chip is always favorable, as it potentially results in a simpler system design and smaller PCB footprint, and it also lowers the cost by eliminating or integrating the most costly power converter component: the power inductor.

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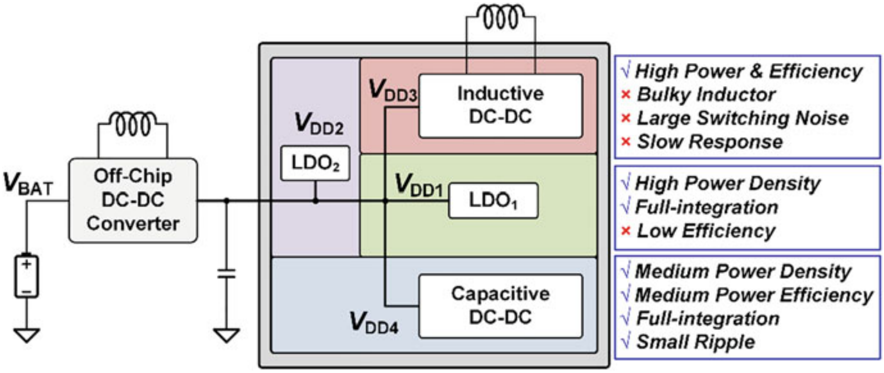

Fig. 1 A typical SoC power delivery network

In typical system-on-chip (SoC) designs (Fig. 1), there are many different logic and functional blocks that need multiple individual voltage domains, enabled by multiple power converters and voltage regulators [2]. Meanwhile, if power converters can have zero external components that can significantly reduce the number of I/O pins of the SoC chip, the converters can deliver much better transient performances by allocating the power converters closer to the point of load.

Among linear voltage regulators, switching-mode power converters, and switched-capacitor (SC) power converters, SC converters are good for full integration with only capacitors used easily built on-chip with a nanometer process [3]. Although the efficiency of an SC converter drops linearly when the output voltage deviates from its ideal output voltage, we can still obtain good efficiencies with multiple voltage conversion ratios (VCRs). Therefore, SC converters attracted great interest from both the industry and the academia and are a promising alternative for the next-generation SoC power delivery. Several practical products emerged from the application of techniques presented in prior research works.

However, designing a high-performance on-chip SC power converter can be very challenging [3, 4]: First, the power efficiency of an SC converter with only a few VCRs is not high over wide input and output voltage ranges. Second, an SC converter has limited output impedance, and its maximum power density is a function of the on-chip capacitance density and the switching frequency; thus, an increase in power density will always sacrifice power efficiency. Hence, in a standard CMOS process of which the capacitance density is relatively low, there is a fundamental trade-off between power density and efficiency, and optimizing this trade-off can be challenging. Third, the output voltage ripples due to hard-charging currents affect the performances of noise-sensitive devices, and lowering the output voltage ripple requires higher switching frequency and larger capacitance. Therefore, minimizing the voltage ripple using minimum system resources and cost is also a stringent problem to solve.

To tackle the abovementioned design challenges, many circuit- and system-level techniques came out. Researchers and circuit designers try to optimize the SC design with better trade-offs among power density, conversion efficiency, system cost, and design complexity. In this chapter, we will provide a systematic summary and design guidelines of recent SC converter design techniques. We will also review the advantages and drawbacks of these design techniques, in the aspects of topology generation, loss analysis and optimization, voltage ripple reduction, and closed-loop regulation.

The remaining of this chapter will have the following organization: Section 2 discusses the topology generation and selection, as well as the topology-level efficiency considerations. Section 3 analyzes the power conversion losses of SC converters and introduces techniques that reduce gate-drive switching loss and parasitic loss. Section 4 compares the centralized and distributive clock generation methods for multiphase SC converters. Then, we will describe two design examples: an SC converter-ring and a multi-output SC converter in Sects. 4 and 5, respectively. Finally, Sect. 6 draws the conclusions.

2 Topology Generation

2.1 Efficiency and Power Density Trade-Off

Topology generation or selection is the first step of consideration in most of the designs. With the input and output voltage ranges specified, we can determine the required VCRs first. For an SC converter, the theoretical efficiency is

$$\eta = \frac{V_{\mathrm{OUT}}}{M \times V_{\mathrm{IN}}}, \tag{1}$$

where M is the ideal VCR of the selected topology. With only one VCR, the power conversion efficiency decreases monotonically when the output voltage drops from the ideally converted voltage ($M \times V_{\mathrm{IN}}$). For applications that require a wide input or output voltage range, it is important to reconfigure the power conversion cells for several VCRs to cater for a changing input voltage. The SC converter can then operate at a proper VCR that delivers the maximum efficiency.

Figure 2 shows the theoretical efficiency of an SC converter and a low-dropout regulator (LDO) with respect to the output voltage V_O [5]. For example, if V_O needs to be 1/2 V_{IN}, the efficiency is $\eta = 50\%$ when using an LDO. With the SC converter configured as $M = 2/3$, then we get $\eta = 0.5/0.667 = 75\%$; on the other hand, with the SC converter reconfigured as $M = 1/2$, then the ideal efficiency can be 100%. Obviously, with more VCRs, the converter will have a higher averaged efficiency across the whole V_O and V_{IN} ranges. However, more VCRs need more flying capacitors and power switches; thus, combining multiple topologies in one power stage increases circuit complexity and the equivalent output resistance, reducing the output power capability and power density. Clearly, there is a trade-off between power efficiency and power density, and then, the target is to obtain an optimum high efficiency range with a reasonable design complexity.

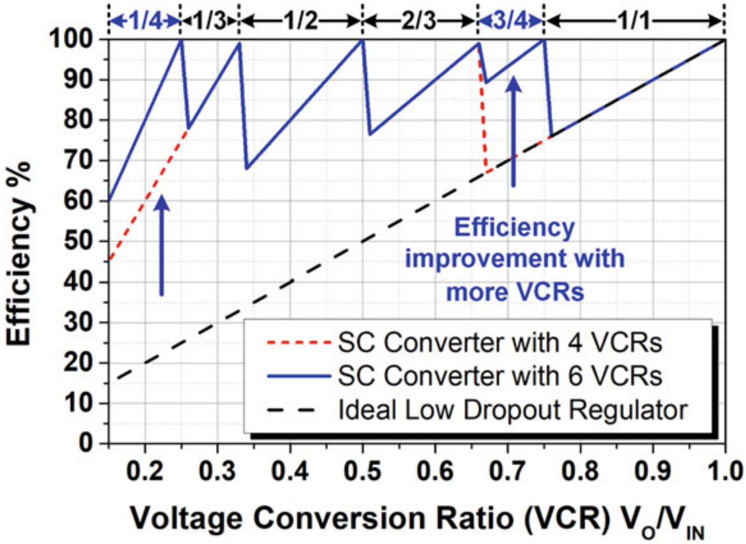

Fig. 2 Theoretical efficiency comparison of an SC converter with four VCRs and six VCRs versus an ideal low-dropout regulator [5]

2.2 *Two-Phase Limitation and Three-Phase Operation*

Most switched-capacitor converters use only two operational clock phases, with the number of VCRs limited by the number of flying capacitors [6]. For example, with two flying capacitors, the realizable step-down VCRs are 1×, 2/3×, 1/2×, and 1/3× only. If more VCRs such as 3/4× and 1/4× are necessary, the converter requires one more flying capacitors.

An alternative method to realize more VCRs while keeping the number of flying capacitors unchanged is to use a multiple clock phase operation [7–10]. A three-phase operation [7] and two- or three-phase operation [8] used in step-up SC converters boost the output voltage to 6×/7× of the input voltage for LED/LCD driver applications. Similarly, when applied to step-down SC converter in [9], it generates a very low output voltage (1/4×) for wireless biomedical implants. Experimental results show an efficiency of 70% obtained for $V_O = 0.5$ V. Figure 3 shows the three-phase topologies (3/4× and 1/4×) using only two flying capacitors and achieving up to 20% efficiency improvements together with a higher average efficiency over wide V_O and V_{IN} ranges [10].

In a short summary, multiple-phase operation uses fewer capacitors and switches; furthermore, it realizes a better trade-off between power efficiency and density, covering wider input and output voltage ranges.

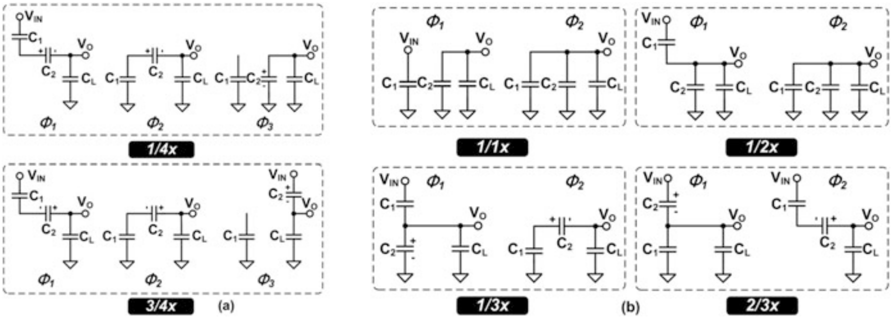

Fig. 3 Operation states of two topologies that use three-phase configuration realizing (**a**) 1/4× mode and (**b**) 3/4× mode [10]

2.3 Review of Other Topologies

To cover a wider voltage range with high efficiencies, some reconfigurable SC converters have a large number of VCRs, for example, the successive approximation (SAR)-based SC converter that has 117 VCRs [11]. By reconfiguring cascaded power cells that have $M = 1/2$, each power cell can be the top or the bottom voltage domain for the next stage, such that the output voltage has seven-bit resolution [12]. The topology is further improved by using recursive SC converters [13, 14]. In [15], a gear train topology emerged using five off-chip capacitors constructed four stacked power stages that realized 24 VCRs. We can find similar works in [16], and algebraic series-parallel topologies appeared to generate more VCRs to cover wide-voltage ranges [16, 17]. However, these converters have a common drawback; the output impedance is high due to the stacking of too many power switches in series that limit the load current capability and power density. But, we may use them in low-power applications with stringent requirements on system integration.

As mentioned above, a SoC requires multiple voltage domains for individual functional blocks, and then, single-input multiple-output SC converters, with capacitors and transistors potentially shared to save silicon area overhead and improved overall power efficiency, can serve the purpose well. Reference [18] proposed a dynamic power cell allocation scheme for multicore application processors. The dynamic allocation of power cells according to load demands can improve the efficiency by 4.8% when compared with the case without it. The peak efficiency was 83.3% and the maximum load was 100 mA, meanwhile, minimizing the cross regulation. Reference [19] presented a specific application that requires two outputs with different loads and used an on-demand strategy to compensate the current shortage, thus saving on-chip capacitor area. In [20], VCR of 2× and 3× shared one transistor and reduced silicon area and improved the efficiency.

3 Efficiency Optimization

3.1 Unified Models for Losses in the SC Converter

When designing fully integrated switched-capacitor (SC) converters, optimizing efficiency is one of the most important procedures to ensure the maximum power density under peak efficiency. However, the loss contribution of SC converters may arise from multiple factors and may vary with different topologies, leading to complexity in analysis and optimization. In this subsection, we present a methodology to predict the overall efficiency and find the optimized peak efficiency.

Switched-capacitor converters can have an ideal 100% efficiency under close-to-no-load condition, besides, the power efficiency starts to drop when the charge transfer on the flying capacitors happens, due to the well-known charge redistribution loss. In general, the output voltage drops proportionally with the loading current, forming an equivalent output resistor (R_{OUT}) at the output node. Such that, Eq. (1) above is the expression of the theoretical efficiency for a certain VCR. We can observe that there is a relationship between the efficiency and the proximity of the real output voltage (V_{OUT}) to the ideal output voltage ($\mathrm{MV}_{\mathrm{IN}}$). The charge redistribution loss, also known as hard-charging loss, is the integrated conduction energy loss from the resistive loss on the switches. M. Seeman proposed a unified model to calculate R_{OUT} (Fig. 4) [21, 22].

We can model an SC converter as an ideal DC voltage source with an ideal transformer representing the voltage conversion and also with a finite output resistance R_{OUT} [21, 22], composed by R_{SSL} (slow switching limit resistance related to the charge redistribution loss) and R_{FSL} (fast switching limit resistance due to the finite conductance of switches), expressed by

$$R_{\mathrm{SSL}} = K_C \frac{1}{C_F f_{\mathrm{SW}}} \tag{2}$$

$$R_{\mathrm{FSL}} = K_S R_{\mathrm{ON}} \tag{3}$$

where K_C and K_S are topological factors determined by the charging scenario, C_F is the capacitance of the flying capacitor, f_{SW} is the switching frequency, and R_{ON} is the on-resistance of the switches.

The overall output resistance becomes

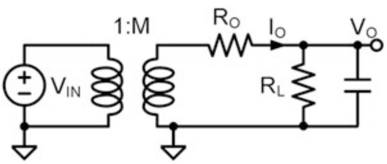

Fig. 4 Transformer-based SC converter model

Table 1 Summary of the equivalent output impedances of three VCRs

VCRs	K_{C}	R_{SSL}	K_{S}	R_{FSL}
2×	1	$\frac{1}{C_F f_{\mathrm{SW}}}$	4	$4R_{\mathrm{ON}}$
3/2×	$\frac{1}{2}$	$\frac{1}{2C_F f_{\mathrm{SW}}}$	$\frac{7}{2}$	$\frac{7}{2}R_{\mathrm{ON}}$
4/3×	$\frac{1}{3}$	$\frac{1}{3C_F f_{\mathrm{SW}}}$	$\frac{20}{9}$	$\frac{20}{9}R_{\mathrm{ON}}$

$$R_O \approx \sqrt{{R_{\mathrm{SSL}}}^2 + {R_{\mathrm{FSL}}}^2}. \tag{4}$$

This model assumes that the output voltage is an ideal DC voltage with neglected voltage ripple. Reference [23] pointed out that Eq. (4) may be inaccurate when the output ripple voltage is very large and presented an improved solution. Deviation from Eq. (4) may also occur if R_{SSL} is close to R_{FSL}. Otherwise, this model is accurate enough in the estimation of the R_{O} and in predicting the output voltage V_{O}; thus, it became a widely used practical model [24, 25].

Here, we present examples to calculate R_O for three topologies: the 2×, 3/2×, and 4/3× topologies that use two-phase clock. We design all R_{ON} as equal, as they conduct the same amount of charge. Table 1 summarizes K_C and K_S for the three VCRs. The major loss is due to the equivalent IR drop of R_{OUT}, and from Eqs. (2) and (3), it is necessary to reduce R_{OUT} loss, high f_{SW}, and large transistor width W_{SW}.

3.2 Switching and Parasitic Losses

In addition to conduction losses, the gate-drive switching loss P_{SW} and parasitic loss P_{PARA} are also significant, especially for fully integrated SC converters. They are actually determining the peak efficiency of the regulated SC converters, due to the adjustment of the output resistor $\mathrm{R_O}$ to obtain a regulated V_O under different loads. At certain V_O, the theoretical efficiency would be identical. Le et al. analyzed in [26] these two losses in addition to Seeman's model. We can calculate the gate-drive switching loss P_{SW} by knowing the switching frequency f_{SW}, the gate capacitance C_{GATE}, and the driving voltage V_{SW}. Regarding the parasitic loss, it is still complex and may vary a lot over different topologies [27, 28].

In 2020, Jiang et al. [29] presented a unified method to simplify the parasitic loss calculation by observing the voltage swing of individual parasitic capacitors. We use 1/3× mode SC converters as examples to analyze the parasitic loss reduction. We assume that the additional charge introduced by the parasitic capacitors will not affect the flying capacitor voltages, as the parasitic capacitors are much smaller (usually below 5%) than the main capacitors. We also suppose a no-load condition such that the capacitor voltages would not change among the operational phases.

Let us consider the 1/3× SC converter from Fig. 5, with the positive- and negative-plate parasitic capacitors C_{1p+}, C_{1p-}, C_{2p+}, and C_{2p-}, where we labeled their voltage swings in both phases. For the summation-mode converter, when Φ_1

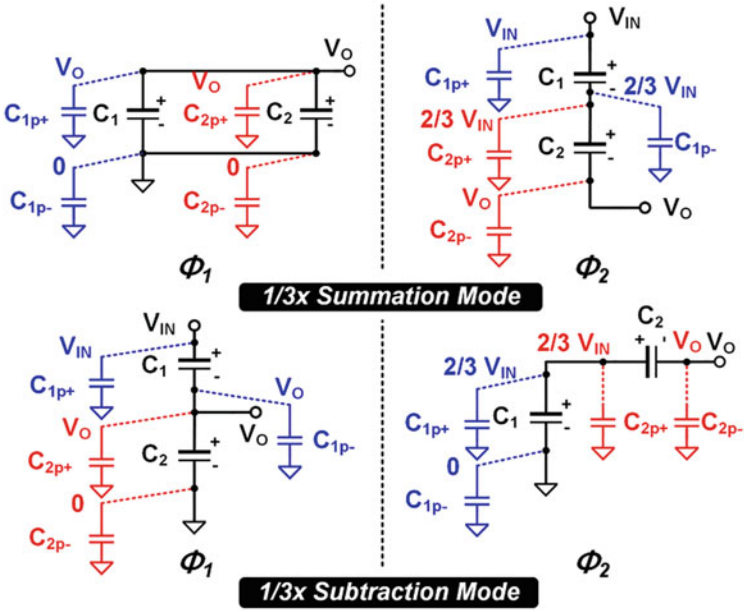

Fig. 5 Parasitic capacitors on the top and bottom plates of the 1/3× mode

changes to Φ_2, C_{1p+} charges from V_O to V_{IN} with a charge Q_{1P+}. The energy sourced from V_{IN} is

$$E_{1P+,\text{CH}} = V_{\text{IN}} Q_{1P+} = V_{\text{IN}}(V_{\text{IN}} - V_O)C_{1P+} = \frac{2}{3}V_{\text{IN}}^2 C_{1P+} \tag{5}$$

When Φ_2 changes to Φ_1, C_{1p+} discharges from V_{IN} to V_O, and the energy returned to V_O becomes

$$E_{1P+,\text{DIS}} = V_{\text{O}} Q_{1P+} = V_{\text{O}}(V_{\text{IN}} - V_O)C_{1P+} = \frac{2}{9}V_{\text{IN}}^2 C_{1P+} \tag{6}$$

The energy loss due to C_{1P+} is the difference of Eqs. (5) and (6), and we can write it as

$$E_{1P+,\text{LOSS}} = E_{1P+,\text{CH}} - E_{1P+,\text{DIS}} = \frac{4}{9}V_{\text{IN}}^2 C_{1P+} \tag{7}$$

For C_{1p-}, it charges from 0 to 2/3 V_{IN} in Φ_2:

$$E_{1P-,\text{CH}} = (V_{\text{IN}} - V_O)\frac{2}{3}V_{\text{IN}} C_{1P-} = \frac{4}{9}V_{\text{IN}}^2 C_{1P-} \tag{8}$$

In Φ_1, with all the charges dumped back to ground by C_{1p-}, the loss is

$$E_{1P-,\mathrm{LOSS}} = E_{1P-,\mathrm{CH}} = \frac{4}{9} V_{\mathrm{IN}}^2 C_{1P-} \tag{9}$$

In general, considering the parasitic capacitor C_P, charged and discharged between two voltages V_L and V_H, in the charging phase, the energy sourced from the system is

$$E_{P,\mathrm{CH}} = V_{\mathrm{H}}(V_H - V_L)C_P \tag{10}$$

In the discharging phase, the energy returned to the system is

$$E_{P,\mathrm{DIS}} = V_L(V_H - V_L)C_P. \tag{11}$$

Hence, the energy of the parasitic loss is the following:

$$E_{P,\mathrm{LOSS}} = E_{\mathrm{P,CH}} - E_{P,\mathrm{DIS}} = (V_H - V_L)^2 C_P = \Delta V^2 C_P \tag{12}$$

The dominant factor of the parasitic loss is the voltage swing ΔV that is $(V_H - V_L)$, where the parasitic capacitor C_P charges and discharges between these two voltages V_L and V_H. Then, we derive the parasitic loss of one parasitic capacitor C_P as

$$P_{\mathrm{PARA},CP} = C_P(V_H - V_L)^2 f_{\mathrm{SW}} = \Delta V^2 C_P f_{\mathrm{SW}} \tag{13}$$

By using Eq. (13), we can calculate the parasitic loss P_{PARA} of all parasitic capacitors C_{ip+} and C_{ip-} $(i = 1 \ldots N)$ by finding out the voltage swings of the positive and negative plates.

3.3 Gate Switching Loss and Parasitic Loss Reduction

The concept of reducing the gate-drive switching loss implies the use of low-voltage (thin-oxide) transistors [25]. The method places in cascode several thin-oxide transistors to withstand a higher breakdown voltage. Because the feature size of the thin-oxide transistor is less than that of the thick-oxide transistors, the gate parasitic capacitance is much lower.

Figure 6 shows the operating principle of the NMOS stacking transistors. The turn-on resistance R_{ON} of a MOS transistor is

$$R_{\mathrm{ON}} = \frac{L_{\mathrm{MIN}}}{K V_{\mathrm{OD}} W_{\mathrm{SW}}} \tag{14}$$

where K is a process-related parameter, V_{OD} is the overdrive voltage of the transistor, and L_{MIN} is the minimum channel length. We can implement a power switch using

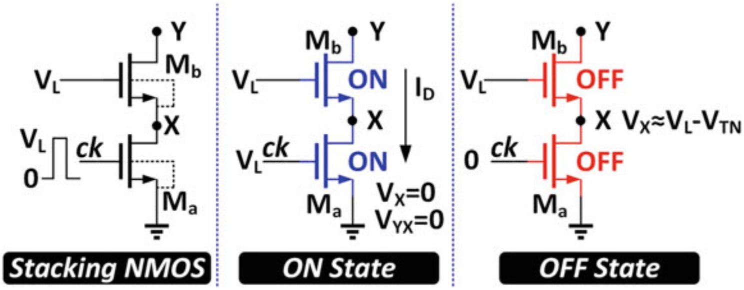

Fig. 6 Operating principle of the NMOS (N-type metal-oxide semiconductor) stacking transistors

one thick-oxide high-voltage transistor or two stacking thin-oxide low-voltage transistors. If the two implementations have the same R_{ON}, then for each type of transistors,

$$R_{\mathrm{ON}\_L} = \frac{1}{2} R_{\mathrm{ON}\_H} \tag{15}$$

Considering Eqs. (14) and (15) together, the size ratio of the thick-oxide transistor to thin-oxide transistor is

$$\frac{W_{\mathrm{SW}\_H}}{W_{\mathrm{SW}\_L}} = \frac{L_H}{2L_L} \frac{K_L V_{\mathrm{OD}\_L}}{K_H V_{\mathrm{OD}\_H}}. \tag{16}$$

Now, the switching loss becomes

$$P_{\mathrm{SW}} = V_{\mathrm{SW}}^2 f_{\mathrm{SW}} C_{\mathrm{GATE}} W_{\mathrm{SW}}. \tag{17}$$

Then, the ratio of their switching losses is

$$\frac{P_{\mathrm{SW}_H}}{P_{\mathrm{SW}_L}} = \frac{V_{\mathrm{SW}_H}^2 C_{\mathrm{GATE}_H} W_{\mathrm{SW}_H}}{2V_{\mathrm{SW}_L}^2 C_{\mathrm{GATE}_L} W_{\mathrm{SW}_L}}. \tag{18}$$

In a typical 0.18 μm CMOS process, we have 1.8 V thin-oxide transistors and 5 V thick-oxide transistors. Then, the lengths are $L_H = 0.5$ μm for NMOS, $L_H = 0.7$ μm for PMOS (p-channel metal-oxide semiconductor), and $L_L = 0.18$ μm. The overdrive voltages are $V_{\mathrm{OD\_H}} = 3$ V and $V_{\mathrm{OD\_L}} = 1.2$ V. We extract other parameters from the process design kit and list them in Table 2. The results show that using low-voltage transistors, we can obtain a 2.615× and 1.778× switching loss reduction for the NMOS and PMOS switches, respectively. This helps the converter to achieve 82% peak efficiency in 0.18 μm CMOS. In [30], six thin-oxide transistors used in a cascode arrangement allow the SC converter in 65 nm CMOS to switch faster.

Table 2 Switching loss calculations

Type	NMOS		PMOS	
	Low-V	High-V	Low-V	High-V
L_{MIN} *(μm)*	0.18	0.7	0.18	0.5
K (1 m/ΩV)	0.147	0.138	0.048	0.03
$C_{\mathrm{GAT}E}$ *(fF/*LMIN*)*	0.52	0.82	0.62	0.62
W_H/W_L	*0.829×*		*0.889×*	
$P_{\mathrm{SW}\_H}/P_{\mathrm{SW}\_L}$	*2.615×*		*1.778×*	

It is even more necessary to use cascoded devices in high-voltage applications, since the Q_gR_{ON} product of the thin-oxide transistor is much smaller than that of the high-voltage DMOS (deep diffusion metal oxide semiconductor) transistors [31, 32]. In [32], two 3.3 V transistors cascoded in an 11/1× topology convert a high voltage (35–40 V) to 3.3 V with 94.7% peak efficiency. In [8], 3.3 V and 5 V transistors cascoded in a 6× step-up SC converter with a 15 V output voltage exhibit reduced gate switching loss.

Parasitic loss is also proportional to the switching frequency. It becomes significant on a fully integrated SC converter, especially when MOS capacitors utilize flying capacitors. Multiple works [33–39] reported reduced parasitic losses, by using low parasitic ferroelectric capacitor [33], deep trench capacitor [34, 35], parasitic loss recycle techniques [36, 37], and dynamic voltage biasing techniques [38, 39]. All these methods reduce the loss caused by parasitic capacitance and can increase the efficiency.

3.4 Efficiency Optimization

We can obtain the overall efficiency as

$$\eta(f_{\mathrm{SW}}, W_{\mathrm{SW}}) = \frac{P_O}{P_O + P_{\mathrm{LOSS}}} \tag{19}$$

$$P_{\mathrm{LOSS}} = P_C + P_R + P_{SW} + P_{\mathrm{PARA}} \tag{20}$$

Obviously, the gate switching loss P_{SW} and the parasitic loss P_{PARA} are proportional to the switching frequency f_{SW} and the transistor size W_{SW}, while the charge redistribution loss $\mathrm{P_C}$ and the conduction loss P_R are inversely proportional to f_{SW} and W_{SW}. Then, we can find the optimum efficiency point by sweeping f_{SW} and W_{SW}.

Figure 7 illustrates an example of efficiency curves with the optimum point at the maximum load condition (I_{LOAD} = 600 uA) [25]. We conducted the efficiency calculation and simulation using MATLAB, and to obtain the peak efficiency of each VCR, we swept f_{SW} and W_{SW} from 10 MHz to 30 MHz and from 10 μm to 40 μm, respectively. Figure 7 shows the results in three-dimensional curves. For the 4/3× mode, the peak efficiency is 82.5% when f_{SW} is 11.3 MHz and W_{SW} is 27.5 μm. For the 3/2× mode, the peak efficiency is 80.5% when f_{SW} is 15.7 MHz and W_{SW} is

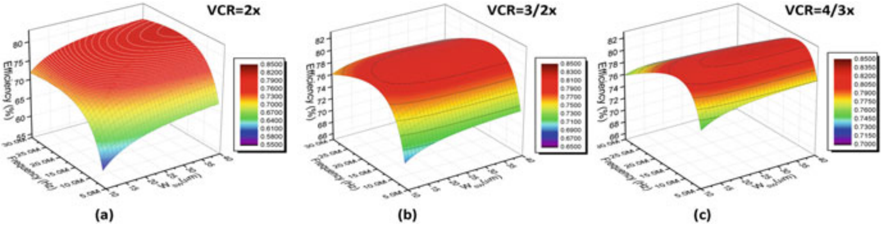

Fig. 7 Simulated efficiency with respect to the switching frequency f_{SW} and the width of the power transistor width W_{SW}

33.94 μm. The optimal f_{SW} for the 3/2× mode is higher than the optimal f_{SW} of the 4/3× mode because we used fewer transistors; as the switching loss is lower, we can employ larger transistors. For the 2× mode, the peak efficiency is 80% when $f_{SW} = 19$ MHz and $W_{SW} = 40$ μm. This mode uses the smallest number of transistors; thus, switching and parasitic losses are significantly lower than the other two modes; however, both f_{SW} and W_{SW} can be larger. In conclusion, by using this model, we can obtain optimized efficiency for certain topologies.

4 Clock Generation and Distribution: 123-Phase Converter Ring

4.1 General Concept of Multiphase Interleaving

We can consider output voltage ripple as power loss, because a larger ripple means that we should reserve a larger supply voltage for the load. To reduce the ripple, we can easily apply a multiphase interleaving scheme in fully integrated SC power converters [26, 40–47]. Figure 8 presents the concept and system diagram, where we implement multiphase interleaving by partitioning the SC power stage into multiple small cells, with these power cells driven by different clocks (ck_1 to ck_n). Adjacent clocks have a 360°/*n* phase shift and *T*/*n* delay where *T* is the switching clock period, such that the output voltage has a higher equivalent frequency; thus, we can reduce the output voltage ripple. An n-phase voltage-controlled oscillator (VCO) can easily generate multiphase interleaving clock signals. To effectively regulate V_{OUT}, a frequency modulation scheme is favorable, as it saves unnecessary switching losses as well. After the error amplifier senses V_{OUT} and generates the control signal V_C, it will adjust the switching frequency according to the load condition. Besides reducing the output voltage ripple, we can also significantly reduce the input current (I_{IN}) ripple as the discontinuous inrush input current of a single-phase converter would be evenly distributed among interleaving phases for a multiphase converter. Consequently, we can use smaller input and output capacitances. As such, more interleaving phases are beneficial and preferable in recent fully on-chip SC converter works

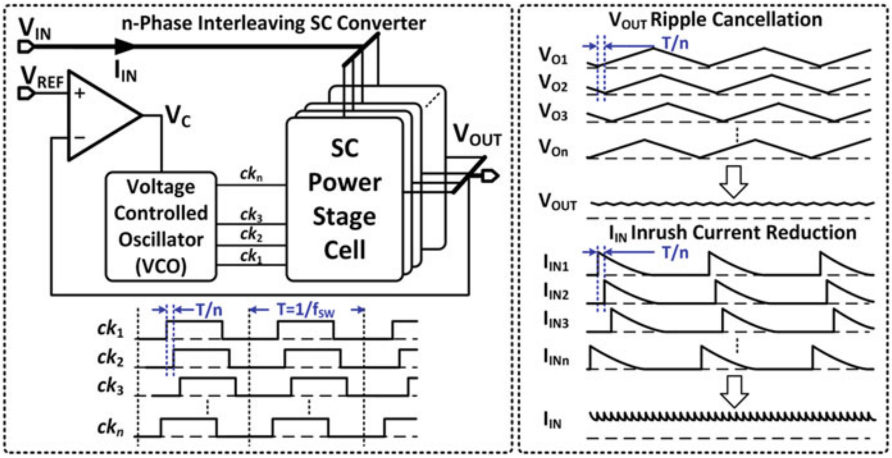

Fig. 8 System diagram and waveforms of multiphase interleaving SC converter [27]

[40–47]. However, distributing a large number of interleaving clock phases across a large converter chip area can be challenging.

4.2 *Clock Generation: Centralized Versus Distributive*

Figure 9 presents two schemes of interleaving clock generation and distribution. Figure 9a shows the H-tree structure with centralized clock generation and then distribution, commonly used in large digital circuits and systems. For a multiphase SC converter, each power cell needs one clock signal from the central VCO, and N phases will need an N-bit clock bus running over the whole converter, complicating the design. Moreover, in order to obtain good phase matching, the power stage layout has to be symmetrical, thus restricting the layout shape of the power management unit to rectangular. To distribute the interleaving clock phases by each of the power cells, we need to route them from the central VCO to the power cells. Then, we will get a parasitic capacitor $C_{P\_1\_\mathrm{CELL}} = \log_2 N \times L \times C_{\mathrm{PAR0}}$, where N is the phase number and C_{PAR0} is the unit parasitic capacitance in fF/μm. The total parasitic capacitance of all the clock wires driven by the VCO is $C_{P\_\mathrm{TOTC}} = N \times \log_2 N \times L \times C_{\mathrm{PAR0}}$. Therefore, the power consumption for the clock distribution is large. Consequently, the number of clock phases in most of the works is under 50 [26, 41–43].

On the other hand, Fig. 9b presents the distributed scheme [44–47], where we design the power cells to be identical, and the adjacent power cells generate clock phases with a fixed delay from the preceding. When connecting N such cells (N is an odd number) in a ring, we can form a ring oscillator along with the power converter. Each power cell supplies power to the power rails that run through the whole

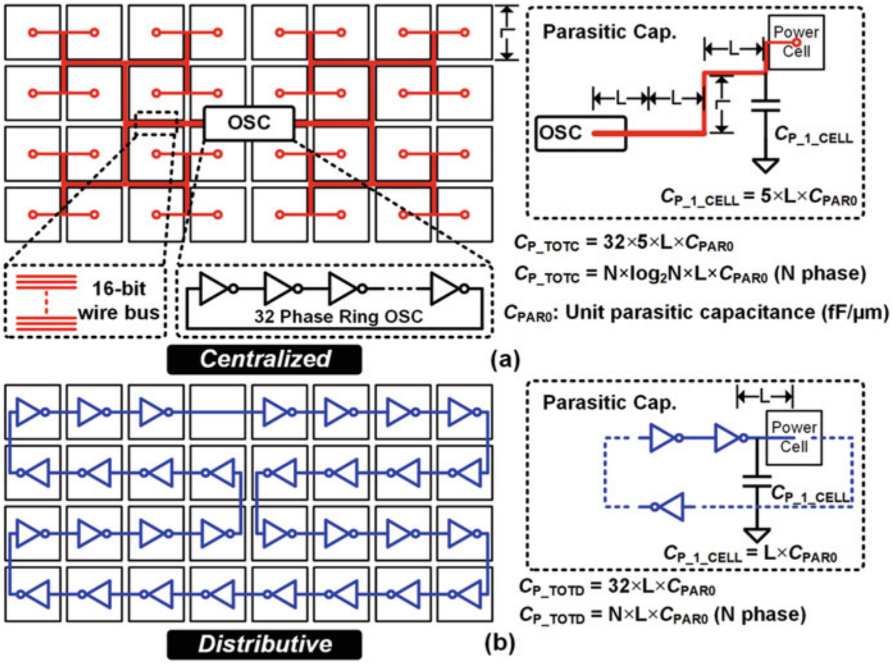

Fig. 9 Comparison between clock generation and distribution, as well as parasitic capacitance on the routing wires of (**a**) centralized scheme and (**b**) distributive scheme

converter. When compared to the H-tree scheme, the distributed clock paths are shorter, and then the parasitic capacitance along the clock wire is only $C_{P\_\mathrm{TOTD}} = N \times L \times C_{\mathrm{PAR0}}$ which is much smaller. Subsequently, the power consumption of the VCO is also much lower. Meanwhile, it is not necessary to locate the power cells on the periphery of the chip; actually they can run through the loading blocks that require power, as long as the connected power cells form a closed-loop ring. One possible drawback for this scheme is that the total parasitic capacitance along the clock routing paths will affect the switching frequency of the power ring. To tackle this issue, we should size the inverters in the ring oscillator accordingly.

For fully on-chip SC converters dealing with fast load transients, even the input and output decoupling capacitors, or at least part of them, need full integration on-chip. They would occupy a large die area, and we can reduce their values only by decreasing both the input rush current and the output-voltage ripple. We can effectively diminish these ripples by using multiphase interleaving. Two recent works with a large numbers of phases emerged, 101 phases in [47] for driving LEDs and 123 phases in [45, 46] for microprocessors, thus achieving very low output voltage ripple without using external capacitors.

To summarize, the distributed scheme has the advantages of layout flexibility and lower power consumption when compared with the centralized scheme. We should draw a special attention to the buffer capability of the distributed ring oscillator.

4.3 123-Phase SC Converter Ring

Figure 10 illustrates a ring-shaped SC converter surrounding the load, to take full advantage of the multiphase interleaving technique [45]. In addition, the converter ring achieved a unity-gain frequency (UGF) higher than its switching frequency by setting its dominant pole on the output node. The designed converter ring consists of many time-interleaved power cells and only one controller. For a Lego-like layout, the size of the controller layout is exactly the same as that of one power cell. We planned the input and GND pins of the converter ring on every corner of the chip, without affecting the pads of the load. Similar to a standard pad ring, the converter ring surrounds the load in the square, with minimum changes (if not zero change) necessary for the existing layout of the load. One of the advantages of the power cell approach is its simplicity: we only need to design one power cell and the complete power ring. The converter ring layout and bumping diagram are also compatible with flip chip packaging. One advantage of integrating a step-down DC-DC converter on chip is that the input current is much smaller than the load current, thus reducing the input bump/pad current stress.

The regulation of the SC converter can use LDO-assisted loop [48], hysteresis control [49], pulse skipping modulation [50], and frequency modulation [51]. For a multiphase SC converter, frequency modulation is the most appropriate method since using LDO and using hysteresis control are both not feasible.

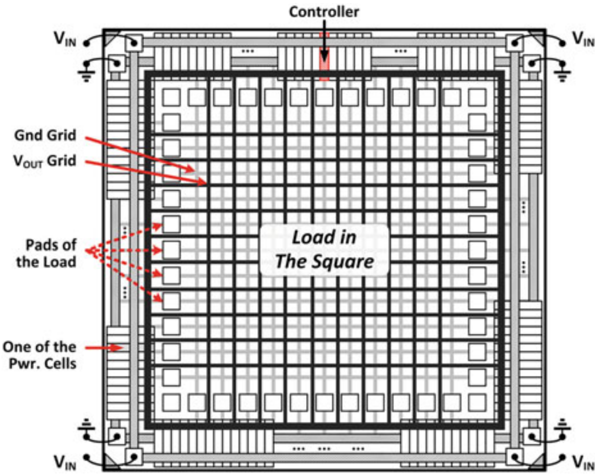

Fig. 10 A ring-shaped multiphase SC power converter [45]

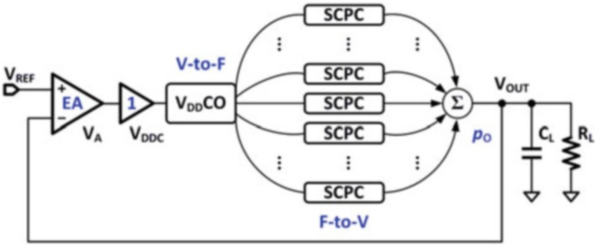

Fig. 11 Small-signal analysis of the multiphase SC converter

Figure 11 exhibits the small-signal analysis of the multiphase SC converter. One key feature of this circuit is the fact that the UGF of the designed multiphase converter is a few times higher than its switching frequency. The following features allow that to happen: (1) to consider the time-interleaved multiphase SC converter as a pseudo-continuous-time power converter, (2) to set the dominant pole at the output node, (3) to employ a high-speed error amplifier (EA), and (4) to tune the oscillator frequency through its supply to change the switching frequency of all phases instantly and simultaneously.

A switched-capacitor circuit is basically equivalent to a discrete-time resistor. Therefore, it only provides a first-order filtering in the power stage. Meanwhile, multiphase operation empowers the SC converters with more attractive features, for example, smaller input and output ripples, and faster transient responses, that allow the converter to respond within a small fraction of the switching period, acting more like a continuous-time power converter. On the other hand, the LC filter of a buck converter operating in continuous conduction mode (CCM) is a second-order filter, which can provide better filtering but limits the loop bandwidth and slows down the transient response. Also, it is necessary to change the inductor current before the regulation of the output voltage during load/line transients.

For the control loop design, there are several benefits of designing the dominant pole at the output node, as discussed in [46]. If the output pole p_O is a nondominant pole, the loop needs to have an internal dominant pole with a frequency that is a couple of decades lower than p_O, which will limit the UGF. To set p_O as the dominant pole, the converter can drive a large capacitive load without affecting the loop stability. Higher capacitive load is always better for the loop stability.

Following a conventional design methodology, the AC signals that are higher than $f_{SW}/2$ cannot pass through a discrete-time power stage, as imposed by the Nyquist theorem. On the other hand, multiple time-interleaving phase switched-capacitor power cells (SCPCs) act as a pseudo-continuous-time stage [46], which means that the AC signal higher than f_{SW} can also pass through the multiphase discrete-time power stage. In the VCO-based pulse frequency modulation (PFM) of SC converters, after the conversion of the voltage information V_{DDC} to the frequency domain by the VCO, there is another conversion back to the voltage domain through the multiphase SC power stage. Therefore, with a high-speed error amplifier (EA) design, we can obtain an UGF that is a few times higher than the f_{SW}.

Although the buck converter can also enjoy the bandwidth extension benefit of multiphase interleaving, the abovementioned pseudo-continuous-time condition does not apply to buck converters because they can use PFM control as well, including hysteretic control and constant on-/off-time control. However, in fact, the constant on-time control belongs to both categories of PWM and PFM, because the inductor-based converter always requires the duty ratio information for output voltage regulation. Besides, during the load transient period, the duty ratio should be optimally 100% for light-to-heavy load transient and 0% for heavy-to-light load transient. The PWM sampling effect still exists in the constant-on-time controller, limiting the bandwidth extension. Therefore, we can only apply to SC converters [44, 45] a fixed duty ratio PFM, considered as a pseudo-continuous-time operation.

Figure 12 presents the chip micrograph of the first version of the converter ring design [44] implemented in 65 nm CMOS, for microprocessor applications. It has 30 power cells and 1 controller on the top edge plus 31 power cells on the other 3 edges, forming a ring around the whole chip. The number of power cells can be an arbitrary large number, depending on the layout and power cell shape and sizes. But the number of power cells will also decide the number of inverters in the ring oscillator, which determines the maximum switching frequency and consequently the maximum output power.

Figure 13 displays the measured load transient response, reference tracking, and output voltage ripple waveforms of the first converter ring design. We place one load of 25 mA on each corner of the chip to emulate the load transient events. For the load transients between 10 mA and 110 mA, the output voltage variations are within 58 mV with $V_{IN} = 2$ V, $V_{OUT} = 1.1$ VCM = 2/3, benefiting from the designed high UGF. To accommodate the dynamic voltage scaling (DVS) function, we demonstrated a reference tracking speed of 2.5 V/μs. The measured output ripples range from 2.2 mV to 30 mV, in a variety of loads and V_{OUT}/V_{IN} conditions. The phase

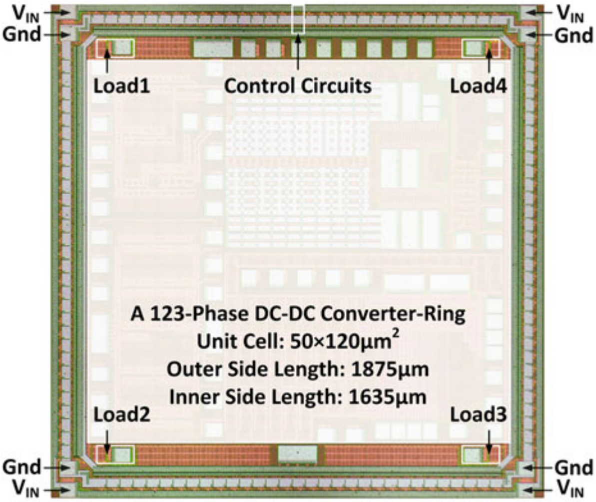

Fig. 12 Chip micrograph of the DC-DC converter ring [43]

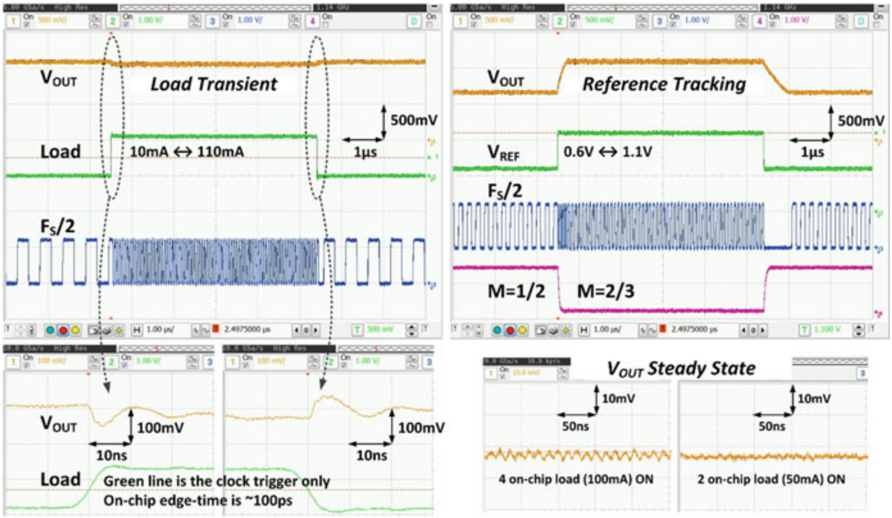

Fig. 13 Measured load transient response, reference tracking, and output voltage ripple waveforms of the converter ring [43]

mismatch on the chip corners and PVT variations dominate the nonideal output ripples. In summary, this SC converter ring exhibits low voltage ripple and fast transient response.

5 Multi-Output Switched-Capacitor Converter

For multicore application processors in the smartphone and the smart watch, power-saving techniques such as dynamic voltage and frequency scaling (DVFS) that extend the battery charging cycle are highly favorable. Yet, each core may need a different supply voltage [52, 53]. High-efficiency fully integrated SC power converters with no external component are promising candidates. Figure 14 shows the strategy of dynamic power cell allocation proposed in [18]. Typically, SC converters with different specifications have independent designs, leading to a large area overhead as each converter has to handle its peak output power. Recently, multi-output SC converters emerged to tackle this issue. Reference [19] uses the on-demand strategy to control the two outputs, each with a different loading range, with the outputs not interchangeable. Reference [20] fixes the two output voltages with voltage conversion ratios (VCRs) of 2× and 3× only. Reference [54] integrates the controller, but the three output voltages are still from three individual SC converters. Without reallocating the capacitors in the power stages, capacitor utilization is low as it is necessary to reserve margins to cater for each peak output power. Finally, [55] proposed a dual-output SC converter with one flying capacitor crossing technique to improve the power efficiency.

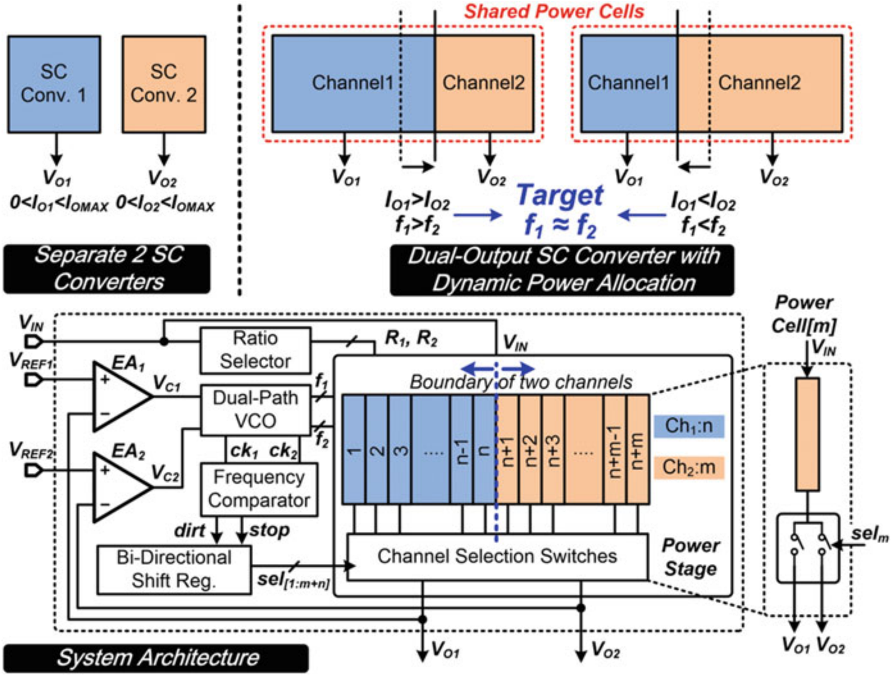

Fig. 14 Strategy of dynamic power cell allocation and system architecture of the dual-output SC converter [18]

In this subsection, we introduce a fully integrated dual-output SC converter with dynamic power cell allocation for application into processors. We can dynamically allocate the shared power cells according to load demands. A dual-path VCO that works independently of power cell allocation achieves a fast and stable regulation loop. The converter can deliver a maximum current of 100 mA: we can adjust one output to deliver 100 mA, while the other handles a very light load, or adjust both outputs to deliver 50 mA each with over 80% efficiency.

The converter consists of two channels (CH_1 and CH_2) with output voltages V_{O1} and V_{O2}, respectively, with each output regulated through frequency modulation by dual VCOs. The switching frequencies of the two channels are f_1 and f_2. The strategy of dynamic load allocations adjusts the switching frequencies to be equal in order that both channels have the same power density, and the whole converter obtains the best overall efficiency.

The SC converters that consist of multiple power cells can operate in a multiphase interleaving mode, with each power cell as the unit cell allocated between two channels. From Fig. 14, we assume that the two channels start with the same number of power cells, but the load of CH_1 is larger than that of CH_2. To regulate the outputs properly, we should initially have $f_1 > f_2$, with more power cells eventually assigned to CH_1. This means that the physical boundary should move to the right, until f_1 and

f_2 are approximately equal. By balancing the power densities of the two channels with an optimal switching frequency, we balanced both switching and parasitic losses leading to their final reduction. By dynamically adjusting both the numbers of power cells and the optimal switching frequencies, we ensure that the channels provide sufficient power to the loads and maximize the utilization of capacitors.

The channel selection switches connect the power cells to either CH_1 or CH_2. The boundary of the two channels are controlled by the outputs of the bidirectional shift register (SR) $sel_{[1:m+n]}$ control the boundary of the two channels. We determine the direction of boundary shifting with the frequency comparator. After each comparison, the boundary will only shift along adjacent power cells as $sel_{[1:m+n]}$ will only shift by one bit. As such, we minimize the potential glitches due to reconnecting the power cell. There are a total of 82 power cells, and they work with interleaved phases to reduce the output ripple voltage. The ratio selector that senses V_{REF}/V_{IN} determines the VCRs of the two outputs (R_1 and R_2).

Figure 15 presents a dual-path voltage-controlled oscillator (VCO) to enable the allocation while minimizing cross regulation. The VCO consists of 82 delay cells, generating the clock phases for each power cell. One delay cell in CH_1 ($DC_{1[n]}$) has a complementary delay cell in CH_2 ($DC_{2[n]}$). We choose the phases $\varphi_{1[n]}$ and $\varphi_{2[n]}$ through the MUX (multiplexer), subsequently distributed to the power cell. If $sel_{[n]} = 1$, it enables $DC_{1[n]}$ of VCO (CH1). Simultaneously, the MUX will short $DC_{2[n]}$ with the clock phase redirected to the next cell. In this way, the number of delay cells in each VCO is equal to the number of its power cells, and multiphase interleaving takes effect to reduce the output ripple voltage. The error amplifier controls the frequency of the VCO, with the two outputs regulated separately, regardless of the power cell arrangement. As the speed of the regulation loop is much faster than that of the power cell allocation, we ensure stability. Each power cell consists of two flying capacitors and eight power transistors with the VCR as 2/3× or 1/2×. We optimize the configuration of each power cell to minimize the parasitic loss. The channel selection switches, controlled by $sel_{[n]}$, connect the local output V_{OL} to V_{O1} or V_{O2}.

Figure 16 illustrates the control logic composed by the frequency comparator and the power cell shift register. First, the one-shot signals (ck_{1os} and ck_{2os}) control P_1 and P_2 to charge C_{C1} and C_{C2} for one clock period only. The activation of the ready signals (ready1 and ready2) happens after charging finishes, triggering the comparison between V_{F1} and V_{F2}. After a short delay, there is the reset of C_{C1} and C_{C2}. For the comparison, if $V_{F1} < V_{F2}$, it means that $f_1 > f_2$, setting the direction signal of the shift register as direct $= 0$, and the selection signals will shift left by one bit. This frequency adjustment repeats until f_1 and f_2 are very close to each other. The frequency comparator will then issue stop $= 1$, and the shift register stops shifting. To ensure accurate charging, we need to well match the current sources and capacitors (C_{C1} and C_{C2}). For robust control, we added offsets to the comparators to form the hysteresis window. The clocks ck1 and ck2 drive the whole process, without an additional system clock.

Figure 17 presents the chip micrograph of the symmetrical dual-output SC converter, fabricated in 28 nm CMOS, with and active area of 1.2×0.5 mm^2.

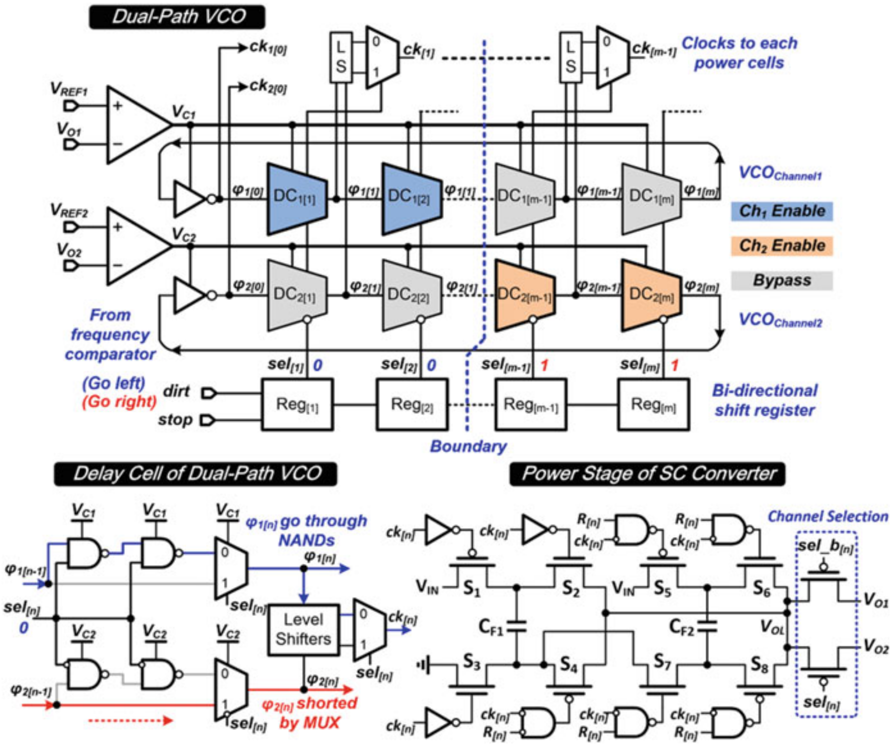

Fig. 15 Circuit implementation of the dual-path VCO, including its delay cell and power stage [18]

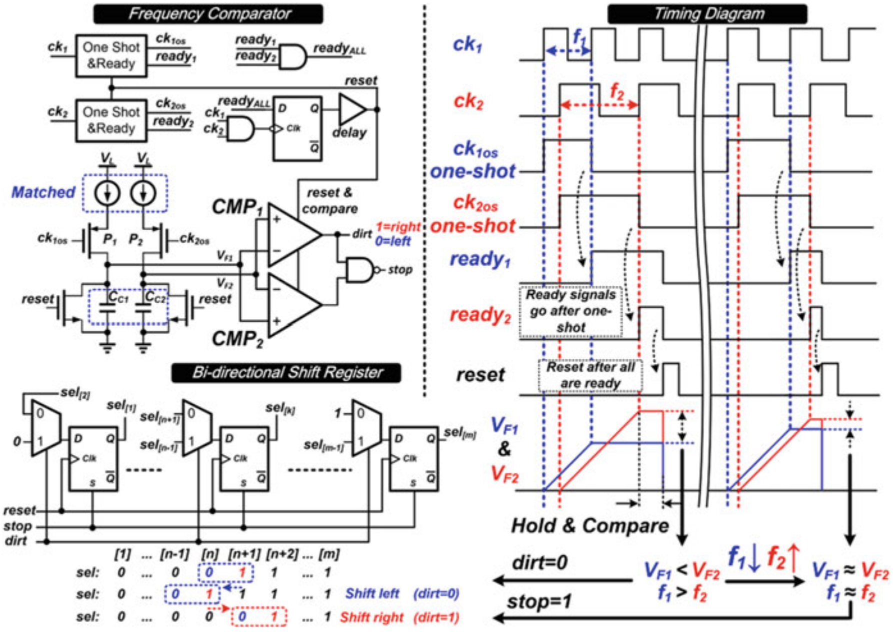

Fig. 16 Circuit implementation of the frequency comparator, the bidirectional shift register, and the timing diagram of the frequency comparison [18]

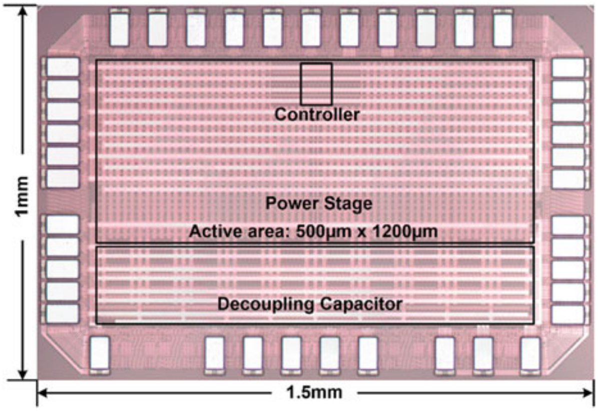

Fig. 17 Chip micrograph of the symmetrical dual-output SC converter

Figure 18 plots the measured waveforms of the steady-state outputs, reference tracking, and load transient. The measured results verified the independent regulation of the two output voltages with the adjustment of the two switching frequencies to be very close. The measured reference up- and down-tracking speeds were 500 mV/μs and 334 mV/μs, respectively. We did not observe any obvious cross regulation at V_{O2} while V_{O1} was undergoing reference tracking. With the load at V_{O1} switched from 4 mA to 40 mA, the settling time was within 500 ns. The cross regulation at V_{O2} was less than 10 mV at the rising edge and negligible at the falling edge, confirming that the dual-path VCO control can realize minimized cross regulation.

Figure 19 displays the measured efficiencies versus the load currents I_{O1} and I_{O2}. The peak efficiency was 83.3% and the split load currents were 50 mA for both channels. Due to dynamic power cell allocation, the converter reached over 80% efficiency, and it was quite constant when I_{O1} and I_{O2} were larger than 15 mA. The efficiency with allocation improves by 4.8% when compared with the circuit without. Table 3 addresses the performance comparison. We can conclude that by using dynamic power cell allocation, the proposed dual-output SC converter exhibited high efficiency over a broad load range for the two outputs with minimized cross regulation.

As a conclusion of this subsection, we presented a fully integrated dual-output SC converter with dynamic power cell allocation for application processors. We dynamically allocate the power cells according to load demands, improving the efficiency by 4.8% when compared with the structure without allocation. The circuit contains a dual-path voltage-controlled oscillator (VCO) that works independently of the power cell allocation to implement a fast and stable regulation loop. The converter achieved 83.3% peak efficiency and a maximum 100 mA while maintaining minimized cross regulation.

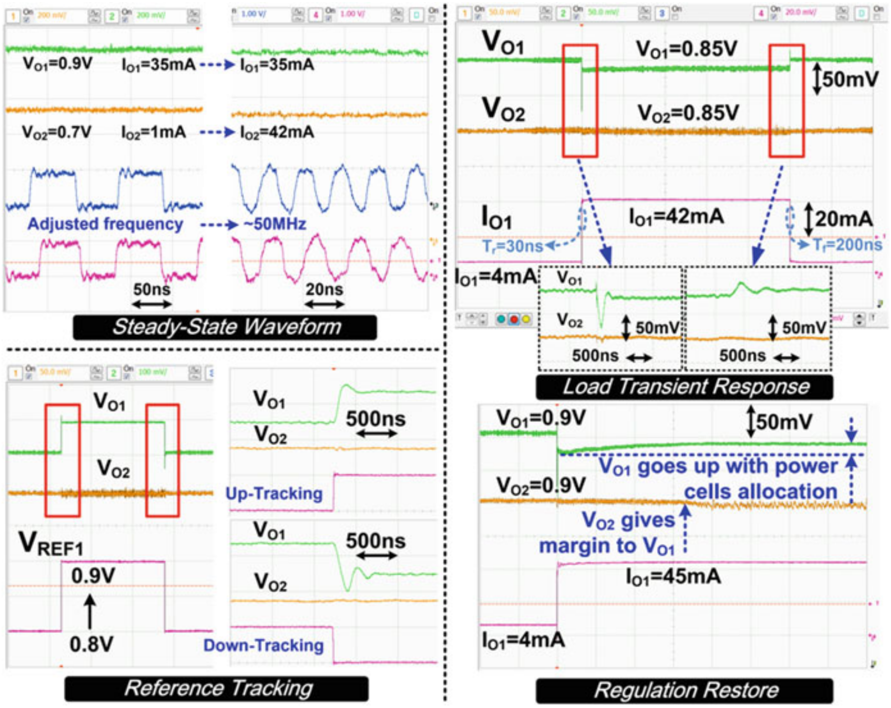

Fig. 18 Measured waveforms of the steady-state output voltages, reference tracking, and loading transient response

Fig. 19 Measured efficiency versus loading currents with and without dynamic power allocation

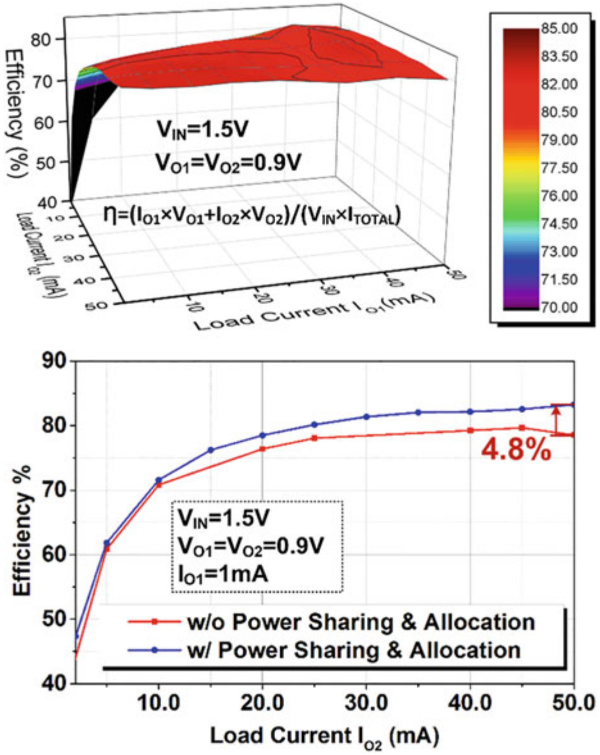

Table 3 Performance comparison with the state of the art

Work	[19] ISSCC`16	[20] JSSC`15	[54] ISSCC`16	This work ISSCC`17
Technology	65 nm	0.35 µm	180 nm	*28 nm*
Topology	Step-up/down	Step-up	Step-down	*Step-down*
Number of outputs	2	2	3	*2*
Passive type	On-chip Off-chip	Off-chip	On-chip (MIM + MOS)	*On-chip* *(MOM + MOS)*
V_{IN}	0.85–3.6 V	1.1–1.8 V	0.9–4 V	*1.3–1.6 V*
V_{OUT}	0.1–1.9 V	2 V and 3 V	0.6 V, 1.2 V, and 3.3 V	*0.4–0.9 V*
$I_{O,\ MAX}$	10 mA	24 mA	100 uA[a]	*100 mA*
Total C_{FLY}	1 µF	9.4 µF	3 nF	*8.1 nF*
η_{peak}	95.8%	89.5%	81%	*83.3%*
Power density	N/A	N/A	250 µW/mm^2	*150 mW/mm^2*
Maximum load per output	V_{O1}: 1 mA V_{O2}: 10 mA	V_{O1}: 12 mA V_{O2}: 12 mA	V_{O1}: 33 µA V_{O2}: 33 µA V_{O3}: 33 µA[a]	V_{O1}: *0–100 mA* V_{O2}: *100–0 mA*
Symmetrical outputs	No	No	No	*Yes*

[a] Extracted from the measurement results

6 Conclusions

In this chapter, we discussed state-of-the-art circuit design techniques addressing the challenges of fully integrated switched-capacitor power converters, which is one of the important ingredients of power management circuits in recent SoC designs. We discussed the design considerations including topology generation, loss analysis, ripple reduction, and closed-loop feedback control. We also presented two design examples in nanometer CMOS to demonstrate the SC converter performances. Last but not least, we exposed practical design guidelines and suggestions for future works.

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