Integrated Energy Harvesting Interfaces

Man-Kay Law, Yang Jiang, Pui-In Mak, and Rui P. Martins

1 Introduction

The approaching of the Internet of Things (IoT) era witnessed the deployment of billions of active portable devices in various applications, where each of them perform different application-specific sensing, monitoring, and processing tasks, like Fig. 1 illustrates. To fulfil the ultimate goal of smart everything, we are expecting a continuous increase in the IoT device functionality, and frequent battery replacement is a major concern due to the limited battery capacity [1]. With the continuous advancement of nanofabrication technologies, IoT devices continue to undergo drastic power and system volume miniaturization [2, 3]. In advanced applications including insect-size microrobots [4] and implantable [5–7] systems, they can have an expected power consumption down to the sub-microwatt level, with special emphasis on small system volume, light weight, and long operation lifetime. As the energy availability is becoming increasingly limited in such miniaturized systems, different energy harvesting technologies for scavenging energy from the environment are becoming viable alternatives for resolving the energy bottleneck.

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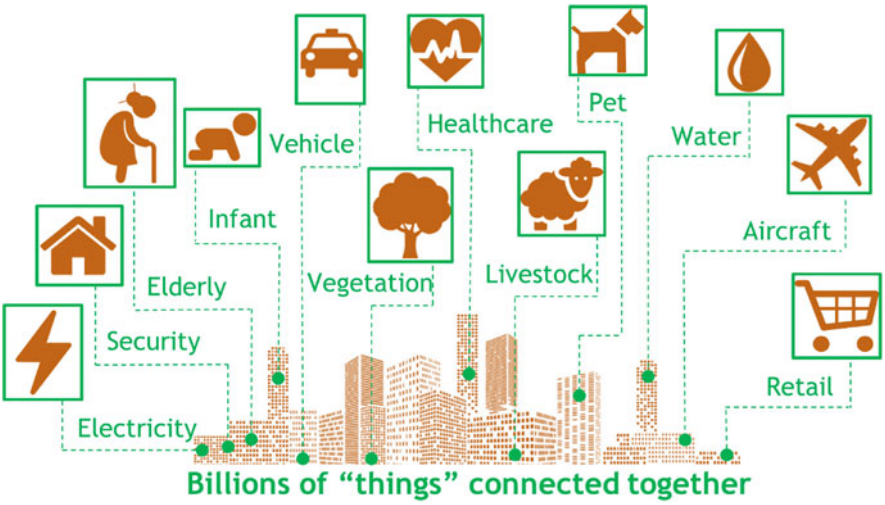

Fig. 1 Illustrative diagram of the IoT era, with connected devices customized for different application specific tasks

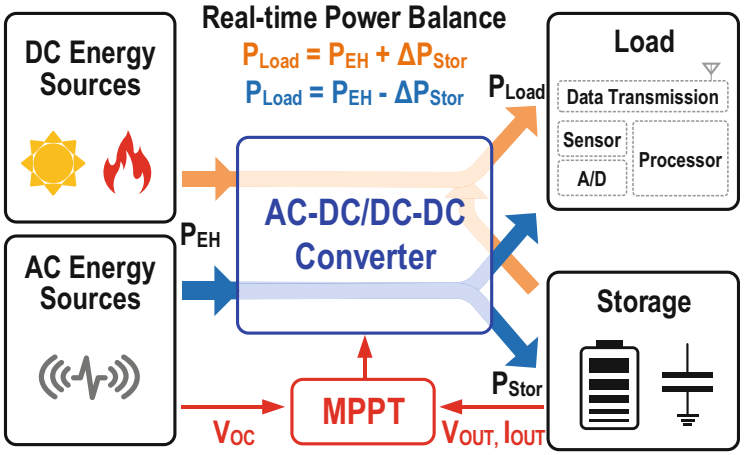

Fig. 2 A generic energy harvesting system with different energy sources powering the system load together with the storage. The maximum power point tracking (MPPT) module serves to maximize the extracted energy. The energy harvesting interface comprises DC-DC or AC-DC converters to maintain the energy flow between harvesters, storage, and load to achieve real-time system power balance

From Fig. 2, the typical composition of a generic energy harvesting system includes the energy harvesters from different sources, the system load for performing specific application tasks, and the energy storage module. The design of the energy harvesting interface specifically addresses the management of the energy flow among the source, storage, and load. Different from batteries, energy harvesters

are typically nonideal energy sources and can have a high source impedance. Therefore, maximum power point tracking (MPPT) is necessary to ensure efficient energy extraction. One popular MPPT approach is the perturb-and-observe (P&O) method [8, 9], also often referred to as the hill-climbing technique. The key idea is to enforce a small perturbation in the system, in order that it can finally converge and operate near the MPP. Obviously, P&O is flexible and we can apply it to a wide range of energy harvesting systems. However, the frequent voltage and current measurement with fast feedback control can be detrimental to energy-constrained IoT systems, not to mention the possible stability and response time issue due to the periodic system perturbations. In low power systems, a more lightweight solution is the fractional open-circuit voltage (V_{OC}) approach [10, 11]. The basic idea is to exploit the correlation between the MPP and the fractional V_{OC} of the harvester. This MPPT approach can be especially energy efficient and easy to implement, as it requires only one sampling and comparison operation. However, it is necessary to disconnect the harvester for V_{OC} sampling, then, it constitutes only a suboptimal solution which demands a priori knowledge of the energy harvester characteristics.

We can classify energy harvesters into either AC-type like vibration [12–14] or DC-type like solar [15, 16] or thermal [17, 18]. As the system load typically needs a DC supply, the energy harvesting interface should perform DC-DC or AC-DC conversion, with the harvested energy delivered to either the storage or the load. For peak power delivery, we should extract the extra energy from the storage. The MPPT circuit can either sample the source information in fractional V_{OC} or the load information in P&O. It also controls the energy harvesting interface to bias the energy source to operate at MPP. Energy harvesting systems typically have two important parameters. The energy extraction efficiency, which denotes the amount of power extracted from the harvester with respect to the maximum power available, which we can express as,

$$\eta_{\text{ext}} = \frac{P_{\text{in,conv}}}{P_{\text{harvest, max}}} \tag{1}$$

where $P_{\text{in,conv}}$ is the input power of the energy harvesting interface and $P_{\text{harvest,max}}$ is the maximum power extractable from the energy harvester. Similarly, we can define the power conversion efficiency (PCE), which is intrinsic to all power converters as,

$$\eta_{\text{conv}} = \frac{P_{\text{out,conv}}}{P_{\text{in,conv}}} \tag{2}$$

where $P_{\text{out,conv}}$ is the output power of the power converter. In theory, the energy harvesting interface should maximize both η_{ext} and η_{conv} to ensure a high end-to-end efficiency.

This chapter introduces different energy harvesting interface designs using switched-capacitor (SC) power conversion techniques to achieve full integration, ultimately targeting both high system efficiency and small size for highly miniaturized IoT systems. Based on the type of energy harvesters, we will introduce different

SC power converters for AC-type and DC-type energy harvesters together with the measurement results in Sects. 2 and 3, respectively, with the conclusions drawn in Sect. 4.

2 Flipping Capacitor Rectifier for Vibration Energy Harvesting

In case of vibration energy harvesting, a piezoelectric energy harvester (PEH) is a popular choice due to its high-power density, high scalability and high output voltage generation [19]. With the PEH subjected to mechanical vibrations, they induce stress within the material, thus giving rise to an electromotive force that generates harvestable electrical charge. From Fig. 3a, we can model a piezoelectric energy harvester using a cantilever-beam structure with one dimension of freedom, which represents a spring-mass-damper system [14]. We can divide the operation of harvesting electrical charge, referred above, into two domains, the mechanical and the electrical, interfaced with a coupling stage. As depicted in Fig. 3b, L_M, C_M and R_M in the mechanical domain represent the mechanical mass, stiffness, and mechanical loss, while C_P in the electrical domain denotes the intrinsic capacitance.

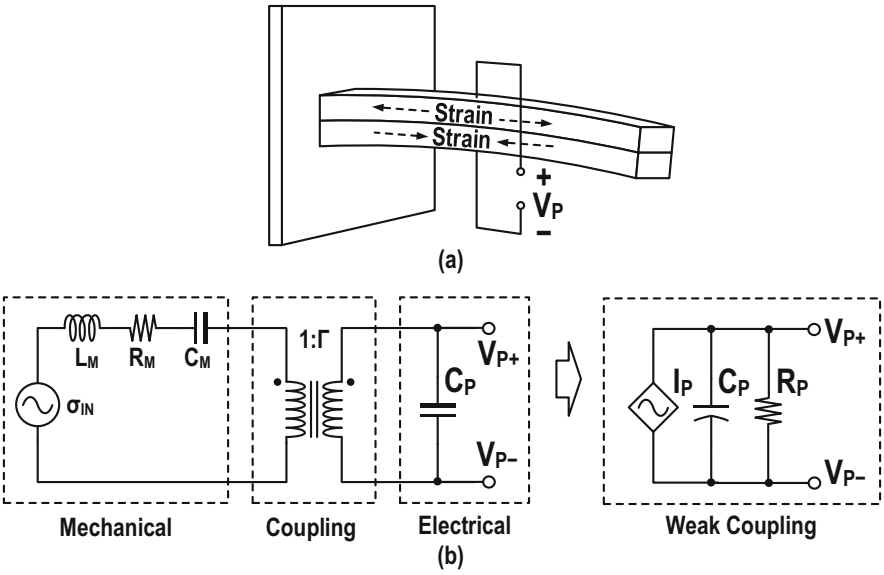

Fig. 3 (**a**) The equivalent model of a piezoelectric energy harvester using a cantilever-beam structure with one dimension of freedom. (**b**) The equivalent circuit model consisting of the mechanical domain, the electrical domain, and the coupling stage, where we can model the PEH (piezoelectric vibration energy harvester) with an equivalent circuit having in parallel I_P, C_P and R_P under weak coupling

Typically, the piezoelectric harvester operates at mechanical resonance to increase the output power. With a small size harvester in miniaturized energy harvesting systems, we can assume it weakly coupled. Then, we can model the harvester simply with a dependent current source I_P, in parallel with C_P and the intrinsic loss R_P.

With a miniaturized PEH device, we can assume the mechanical and electrical domains as weakly coupled (i.e., a small coupling coefficient, Γ). In this case, we can simply model the PEH using the equivalent circuit with I_P, C_P, and R_P connected in parallel. Assuming a sufficiently large R_P, the PEH is equivalent to a charging/discharging of C_P with the current source I_P. Consequently, we can theoretically optimize the output power by operating the PEH at the maximum power point (MPP), through biasing the PEH at approximately half of the open-circuit voltage (V_{OC}).

2.1 Conventional PEH Interfaces

Figure 4 presents the conventional piezoelectric energy harvesting typically implemented with a full-bridge rectifier (FBR) for AC-DC conversion. It is simple to implement and robust, allowing full interface integration. However, there is a limitation in the extractable electrical power due to the PEH inherent capacitance C_P. Yet, to implement such (extracting energy from the PEH) is theoretically inefficient, since part of the harvested energy dissipates with the changing of C_P polarity whenever I_P changes direction before delivering the PEH energy to the load, as exemplified with Q_{loss} in Fig. 4b.

To alleviate the effect of C_P, we can employ an impedance matching network (Fig. 5a). As the harvester impedance is capacitive, we can use an inductive component (e.g., L_{EX}) to eliminate the phase difference between V_P and I_P (Fig. 5b, c). Then, we can change the input impedance of the AD-DC rectifier by tuning R_L to extract the maximum power. However, as we should size L_{EX} to resonate with C_P at the excitation frequency, there is a direct correlation to the

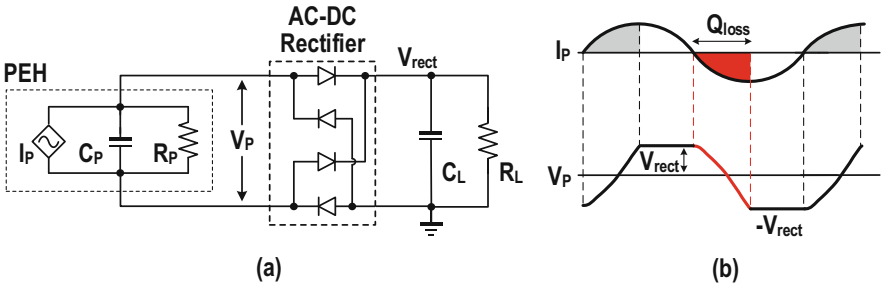

Fig. 4 The conventional PEH interface (**a**) using a full bridge rectifier (FBR) for rectifying the PEH AC voltage to a rectified DC output V_{rect} and (**b**) the corresponding timing diagram, with Q_{loss} representing the charge loss for I_P to discharge C_P

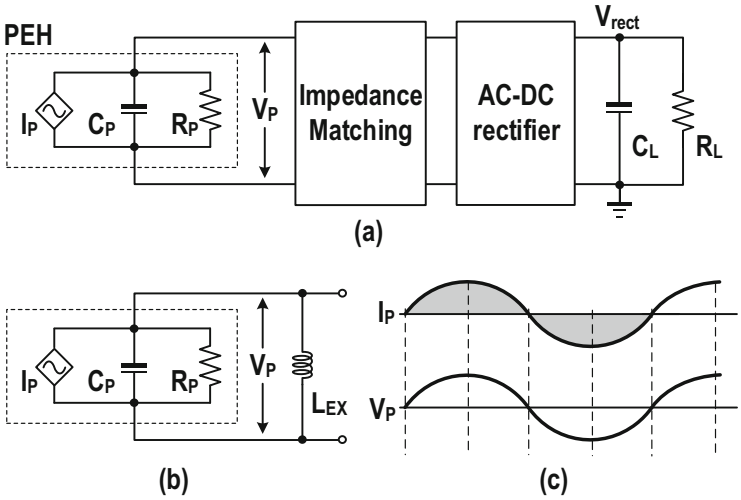

Fig. 5 (**a**) PEH interface with impedance matching network, (**b**) matching with an external inductor L_{EX}, and (**c**) the corresponding timing diagram with I_P in phase with V_P

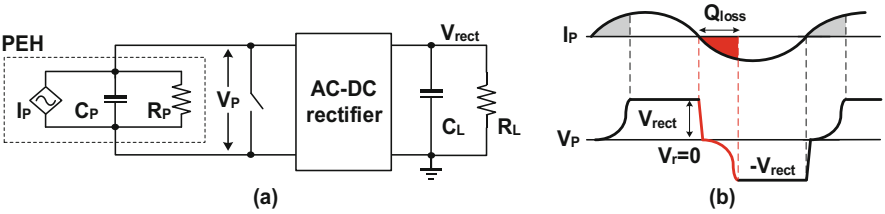

Fig. 6 (**a**) PEH interface with switch only rectifier (SOR) and (**b**) the corresponding timing diagram

PEH resonance frequency, rendering this approach unattractive if the PEH resonance frequency is low.

A simple way to reduce the Q_{loss} in Fig. 4b is the switch-only rectifier (SOR), which shorts the PEH during the zero crossing of I_P using a simple switch (Fig. 6a). As a result, instead of discharging C_P from V_{rect} to $-V_{rect}$, the harvester only discharges C_P from 0 to $-V_{rect}$ (Fig. 6b), and we can theoretically double the extracted power while preserving a simple solution. The rebuilt voltage V_r is equal to zero due to the shorting operation. This leads to a longer conduction time, and equivalently reducing Q_{loss} will increase the extracted power. Nevertheless, the shorting operation also indicates that we waste energy on C_P, ultimately limiting the extractable power.

Theoretically, we should quickly reverse the PEH voltage when I_P changes direction, in order that the V_P and I_P are in phase to reduce the charge loss (Fig. 7). This operation should be as efficient as possible through recycling the energy on C_P. The harvesting efficiency has a direct correlation with the efficiency of

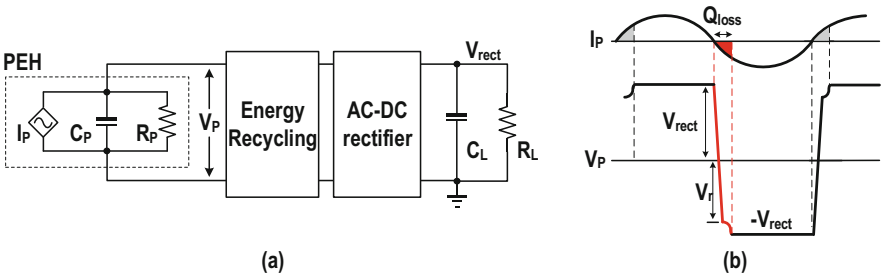

Fig. 7 (**a**) PEH interface with C_P energy recycling and (**b**) the corresponding timing diagram

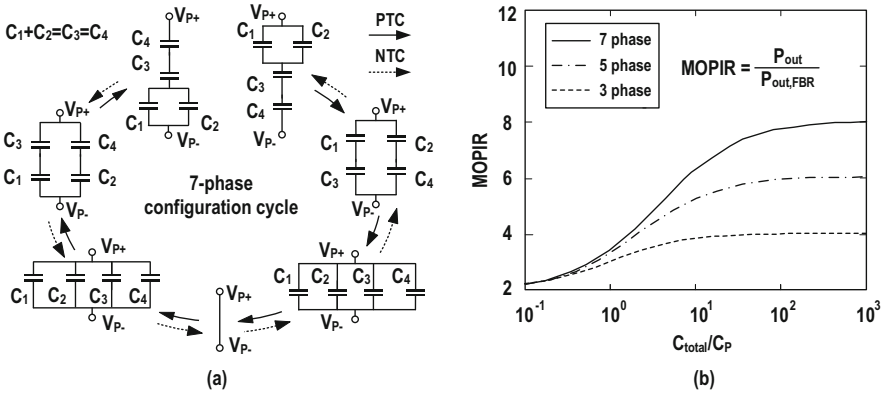

Fig. 8 (**a**) The capacitive PEH interface supporting seven-phase reconfiguration in [22] and (**b**) the relationship between the achievable MOPIR and the corresponding timing diagram

the PEH voltage flipping operation $\eta_F = (V_r + V_{rect})/2V_{rect}$. The higher the η_F, the lower the energy loss during the flipping operation, resulting in a higher extractable power.

Conventionally, we can obtain such a voltage flipping operation using the parallel-synchronous switch harvesting on inductor (P-SSHI) approach [20] but at the expense of a bulky off-chip high-Q inductor. Still, as demonstrated in [21, 22], we can also achieve efficient voltage flipping of C_P capacitively, so it is possible to have the interface circuit completely designed on-chip. The basic idea is to first extract the energy on C_P using a capacitor, with the energy then employed to recharge C_P while flipping its polarity. In that case, we can invert swiftly the voltage on C_P, while minimizing the energy loss. To realize this, a multiphase operation can provide stepwise charging or discharging of C_P for reducing the conduction loss and improving η_F.

Figure 8a shows the capacitive PEH interface (known as flipping capacitor rectifier, FCR) exploiting a seven-phase operation with four flying capacitors for both the positive transition cycle (PTC) and negative transition cycle (NTC) in [22], with the on-chip capacitors $C_{1–4}$ reconfigured over the seven C_P voltage flipping

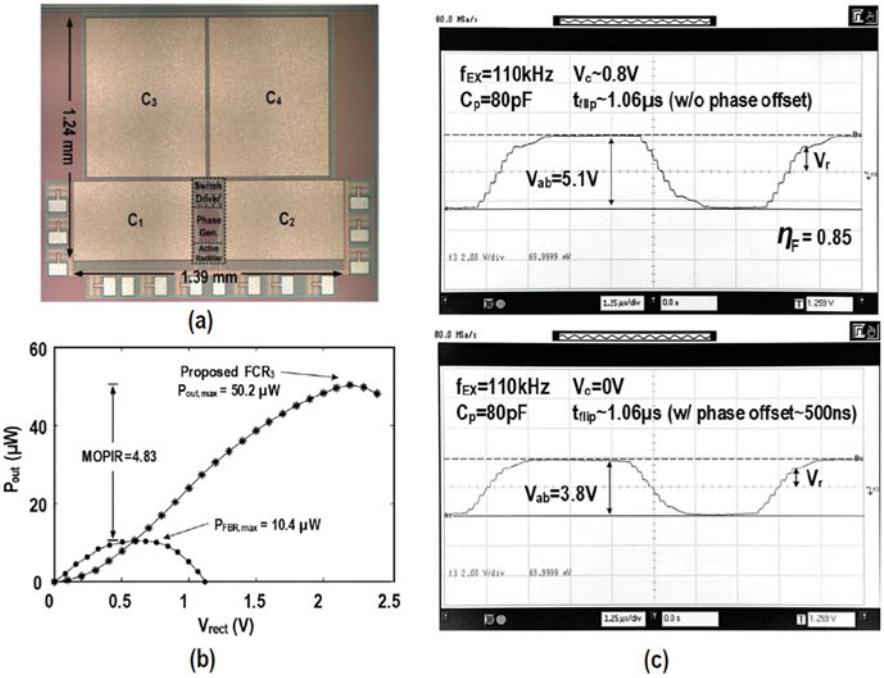

Fig. 9 (**a**) Chip micrograph in [22], (**b**) the achieved P_{OUT} over V_{rect}, and (**c**) measured waveforms of V_P at different testing conditions

phases. We can generally employ as a performance benchmark, the maximum output power improving rate (MOPIR), defined as the ratio between the extracted power and that using a FBR. From Fig. 8b, we observe that we can improve the conduction loss by either increasing the total capacitance C_{total} for a given C_P or by increasing the number of phases. As a result, the extracted output power increases.

The work in [22], fabricated in 0.18 µm CMOS 1.8/3.3/6 V process, occupied an active area of 1.7 mm^2. With the PEH C_P characterized as 80 pF, we set the total on-chip capacitance C_{total} to 1.44 nF to achieve a C_{total} over C_P ratio of 18. With all the components implemented on a single chip, the capacitor area covers ~85% of total chip area (Fig. 9a).

Figure 9b plots the measured output power P_{out} with different output V_{rect} for both the FCR in [22] and FBR at 110 kHz. The output power can be up to 50.2 µW, and the achieved MOPIR is 4.83×. At low V_{in}, the low switch turn on voltage leads to a reduced output power. Figure 9c presents the measured PEH voltage under different measurement settings to demonstrate the effect of phase offset, incomplete charge transfer, and reduced conduction time on the extracted output power. We can perceive that the maximum PEH voltage of 5.1 V occurs when the flip time is ~1 µs without the energy loss due to phase offset and reduced to 3.8 V with a phase offset of ~500 ns enforced.

Table 1 Performance comparison of FCR with state-of-the-art PEH interfaces

	FCR Design	JSSC'16 [8]	ISSCC'14 [23]	JSSC'14 [24]	JSSC'10 [25]	TCAS-I'17 [26]	JSSC'16 [27]
Technology	**0.18 μm**	0.35 μm	0.35 μm	0.35 μm	0.35 μm	0.25 μm Bi	0.35 μm HV
Energy extraction technique	**Flipping-capacitor rectifier**	P-SSHI	Energy pile-up	Energy investment	P-SSHI	P-SSHI	P-SSHI
Piezoelectric harvester	**Piezo Systems Inc. (P5A4E @ 5 mm^3)**	MIDE V21B & V22B	Emulated (transformer + RC)	MIDE V22B	MIDE V22B	MIDE V22B	MIDE V20W
Key component	**On-chip MIM capacitor (C_{total} = 1.44 nF)[a]**	External inductor (L = 3.3 mH)	External inductor (L = 10 mH)[b]	External inductor (L = 330 μH)	External inductor (L = 47 μH)	External inductor (L = 220 μH)	External inductor (L = 20 μH)
Max. output power increasing rate (MOPIR)	**4.83x 4.78x[c]**	6.81x	4.22x	3.6x	2.8x	2.07x	5x[e]
Max. voltage flipping eff. (η_F)	**0.85**	0.94	0.77[b]	NA	0.75[b]	0.75	0.67[b]
Chip size	**1.7 mm^2**	0.72 mm^2	5.5 mm^2	2.34 mm^2	4.25 mm^2	0.74 mm^2	0.6 mm^2
Output power	**50.2 μW**	160.7 μW[d]	87 μW	52 μW	32.5 μW	136 μW	75 μW
Operating freq.	**110 kHz**	225 Hz	100 Hz	143 Hz	225 Hz	144Hz	82Hz

[a]Total capacitance for $C_{1\text{-}4}$
[b]Estimated from the corresponding literature
[c]Averaged over 4 measured samples
[d]Off-resonance with 3.35 g acceleration
[e]FBR output power limited by execessive diod voltage drop

Table 1 summarizes the performance comparison of the proposed FCR technique with the state-of-the-art PEH interfaces [8, 23–27]. As observed, the proposed FCR technique can effectively achieve full integration using 1.44 nF on-chip capacitors under a chip size of 1.7 mm^2. The achieved MOPIR is up to 4.83×, which is comparable to the other inductive PEH interfaces using bulky high-Q inductors with an inductance of up to the mH range.

Based on the FCR technique in [22], we can further improve the PEH interface performance using the split-phase technique in [28, 29], obtaining an even higher MOPIR. Figure 10a presents the system diagram of the corresponding split-phase FCR (SPFCR) design, which includes both maximum power point tracking (MPPT) and output voltage control. The idea is to reuse the capacitor array with 4 C_{fly} to generate a total of 21 PEH voltage flipping phases, while utilizing the same capacitors during the non-voltage flipping time to provide multiple voltage conversion ratio (VCR) control. It also provides a MPPT scheme for relaxing the device voltage tolerance.

Figure 11 exhibits the 21-split-phase operation using 4 C_{fly}, with the harvester voltage biased in a step-wise manner. We design the voltage across each capacitor,

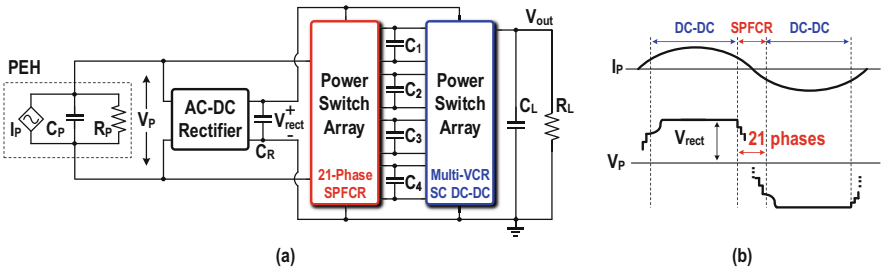

Fig. 10 (**a**) The SPFCR PEH interface using four flying capacitors with capacitor reuse as proposed in [29], (**b**) the concept of capacitor reuse between the DC-DC voltage conversion phase, and the SPFCR PEH voltage flipping phase

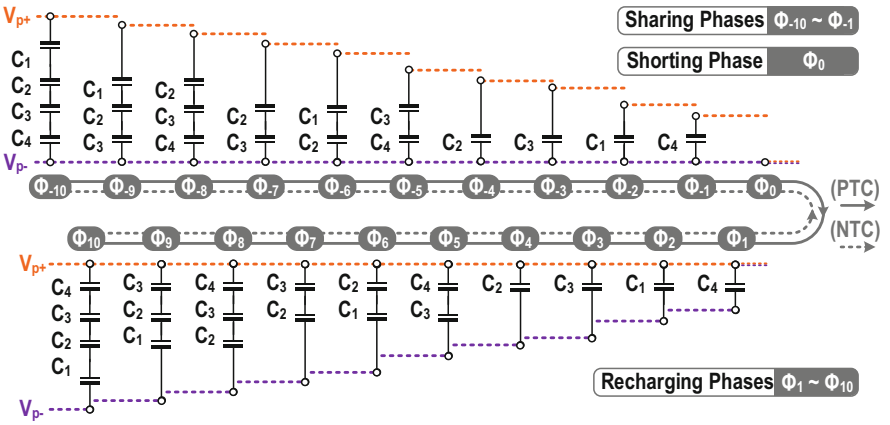

Fig. 11 The 21-phase SPFCR operation using four flying capacitors in [29]

defined by the multiphase operation, to be distinct in order to facilitate voltage level generation and DC-DC converter implementation.

Figure 12 demonstrates how we can reuse the 4 C_{fly} for DC-DC conversion. With the reconfiguration arrangement from Fig. 11, the capacitor voltages after the 21-phase SPFCR operation will be $V_{\text{C1}} = 0.27V_{\text{rect}}$, $V_{\text{C2}} = 0.32V_{\text{rect}}$, $V_{\text{C3}} = 0.19V_{\text{rect}}$, and $V_{\text{C4}} = 0.1V_{\text{rect}}$, respectively. By selecting appropriate interconnections among the capacitors in the charging (Φ_{C}) and discharging (Φ_{D}) phases, we can implement different buck/boost VCRs, with VCR update enforced after the MPPT operation for wide input adaptation.

This work employs the fractional open-circuit voltage (V_{OC}) approach to achieve MPPT. However, as V_{OC} is typically twice the MPP voltage, the voltage tolerance requirement is ultimately limited during the VOC sampling (Fig. 13a). By exploring the PEH-dependent empirical correlation between V_{MPP} and the V_{OC} of FBR in Fig. 13b, this work can achieve MPPT with a much lower voltage tolerance. Specifically, as observed in the control waveforms in Fig. 13c, the MPPT arbiter first resets C_{P} and then samples $V_{\text{OC,FBR}}$ through the peak detector. The sampled

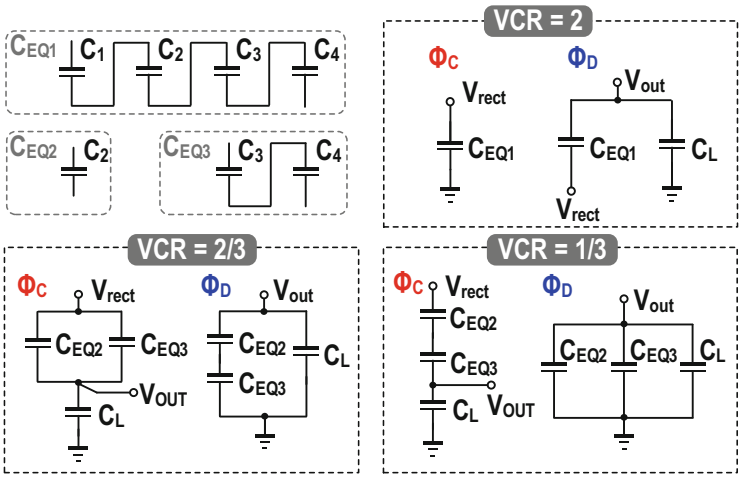

Fig. 12 Reusing of the 4 C_{fly} to realize DC-DC conversion during the non-voltage flipping period in [29]

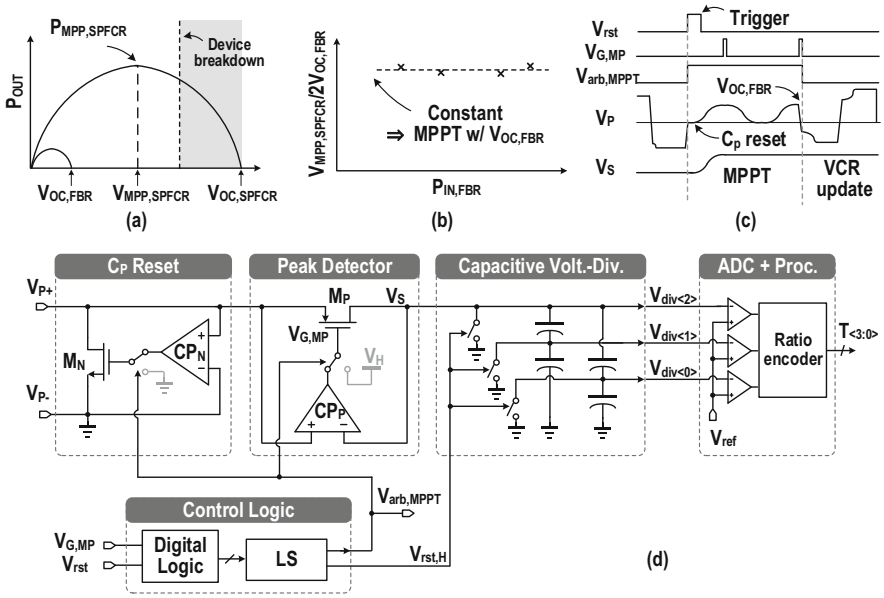

Fig. 13 (**a**) Illustration of the advantage of using $V_{OC,FBR}$ instead of $V_{OC,SPFCR}$; (**b**) the empirical relationship between VMPP, SPFCR, VOC, and FBR; (**c**) the control waveforms of the MPPT arbiter; and (**d**) the simplified circuit implementation of the MPPT arbiter in [29]

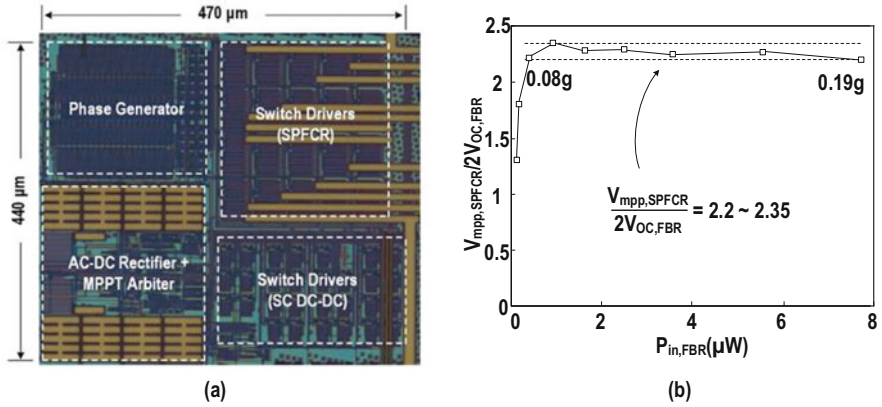

Fig. 14 (**a**) Chip micrograph of the PEH interface using SPFCR in [29] and (**b**) the empirical relationship between $V_{MPP,SPFCR}$ and 2 $V_{OC,FBR}$ over different $P_{in,FBR}$

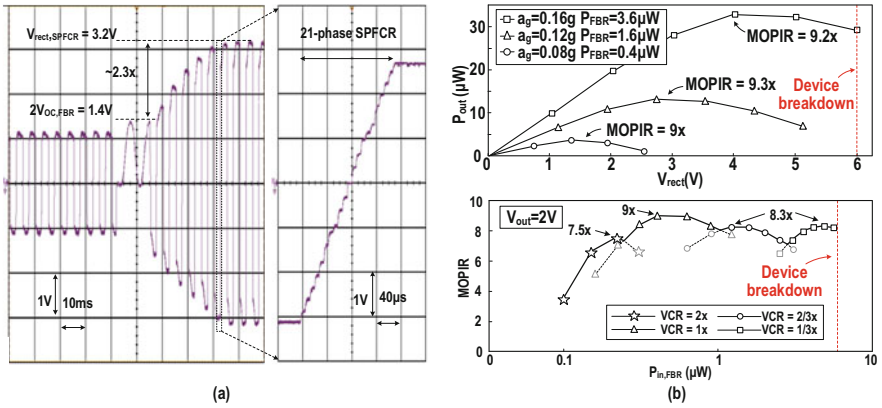

Fig. 15 (**a**) The measured waveform under MPPT and SPFCR operations and (**b**) the measured Pout versus V_{rect} under different external accelerations and the achieved MOPIR under different $P_{in,FBR}$ in [29]

value divided and compared can generate the controls for the VCR update. Figure 13d shows the simplified circuit-level implementation of the MPPT arbiter.

Figure 14a presents the PEH interface exploiting the 21-phase SPFCR approach, implemented in 0.18 µm CMOS; it occupies an area of ~0.21 mm^2, with 4 off-chip C_{fly} of 68 nF each. Figure 14b demonstrates the empirical ratio between $V_{MPP,SPFCR}$ and 2 $V_{OC,FBR}$, with a measured value of approximately 2.3, validating the possibility of using $V_{OC,FBR}$ for MPPT.

Figure 15a displays the MPPT as well as the 21-phase SPFCR operations. As observed, the MPPT arbiter can generate the required $V_{MPP,SPFCR}$ and 2 $V_{OC,FBR}$ ratio for successful MPPT operation. Figure 15b shows the measured P_{out} versus V_{rect} and the achieved MOPIR under different $P_{in,FBR}$. We can demonstrate that this

Table 2 Performance comparison of SPFCR with state-of-the-art PEH interfaces

	SPFCR	JSSC'17 [30]	JSSC'17 [22]	JSSC'19 [31]
Technology	**0.18 μm**	0.35 μm	0.18 μm	0.18 μm HV
Energy extraction technique	**Split-phase flipping capacitor rectifier**	SSHC	FCR	SE-SSHC
Piezoelectric harvester	**MIDE PPA1021**	MIDE V21BL	P5A4E @ 5 mm^3	Custom MEMS
Harvester size	**71 × 10.3 × 0.86 mm^3**	90 × 16.7 × 0.79 mm^3	5 × 1 × 1 mm^3	7 × 2 mm^2 (4 pieces)
C_p	**22 nF**	45 nF	78.4 pF	1.94 pF
Key Component	**4 Capacitors[a] 21 phase**	8 capacitors[a] 17 phase	4 Capacitors[b] 7 phase	8 Capacitors[b] 17 phase
C_{total}	**272 nF**	360 nF	1.44 nF	4 nF
MOPIR	**5.9 ~ 9.3× @V_D = 0.12 V 3.7 ~ 6.2× @V_D = 0 V**	9.7×	4.83×	8.21×
P_{in} adaptation	**Capacitor-reuse multi-VCR SC DC-DC**	no	no	no
MPPT	**Yes ($V_{OC,FBR}$-based)**	no	no	no
Voltage flipping efficiency	**0.84**	0.8	0.85	0.69
Chip size	**0.2 mm^2**	2.9 mm^2	1.7 mm^2	5.3 mm^2
Output power	**0.5 ~ 64 μW**	161.8 μW	50.2 μW	186 μW
Operating freq.	**200 Hz**	92 Hz	110 kHz	219 Hz

[a]Off-chip component
[b]On-chip component

work can obtain a high MOPIR of up to 9.3× (with a diode drop of 0.12 V), while accomplishing a wide input power adaption with V_{out} set to 2 V. The drop at the low input power end is due to the increased intrinsic loss.

Table 2 summarizes the performance comparison of the SPFCR with state-of-the-art PEH interfaces [22, 30, 31]. Using only four capacitors, the proposed SPFCR PEH interface can achieve a 21-phase PEH voltage flipping efficiency of up to 0.84. Using $V_{OC,FBR}$-based MPPT, we can realize wide P_{in} adaptation through reconfiguring the four capacitors for multi-VCR SC DC-DC conversions. It also features a high MOPIR of up to 9.3× at a diode voltage drop $V_D = 0.12$ V.

3 Reconfigurable SC DC-DC Boost Converter for Solar/Thermal Energy Harvesting

Switched-capacitor DC-DC converters attain conversion efficiency advantages for on-chip implementation when compared with inductive converters [32, 33]. The implementation of SC converters requires relatively much smaller energy storage elements, and we can realize them using a bulk CMOS process, allowing an attractive technical approach in energy-constrained miniaturized IoT devices to deliver efficient power conversion with a small system form factor [8, 9, 16, 34–42]. As depicted in Fig. 16a, the ambient variations of the energy harvester operating conditions can lead to a wide-range distribution of the output voltage from the harvester node. Consequently, the DC-DC converter after the harvester module should feature multiple ratio conversion over a wide input voltage range to improve the overall efficiency, as illustrated in Fig. 16b. For instance, the ambient harvested voltage level can be far lower than the system required supplied voltage, for example, the voltage provided by a solar cell is normally in the level of 0.2–0.4 V. A wide and variable range power converter is a prerequisite for powering a loading system or charging a storage. However, traditional single-VCR SC converters suffer from limited voltage conversion range and overall efficiency degradation under the above application scenarios. Accordingly, highly integrated SC DC-DC converters with multiple VCRs are superior solutions for wide-range voltage conversion adaptation, overall harvesting functionality and performance improvement, and also system integration level [43–54]. In this section, we discuss the generic SC converter power stage intrinsic loss model together with advanced topology techniques for generating fine-grained VCRs and improving the interfacing capability with DC-type energy harvesters (i.e., solar and thermoelectric sources).

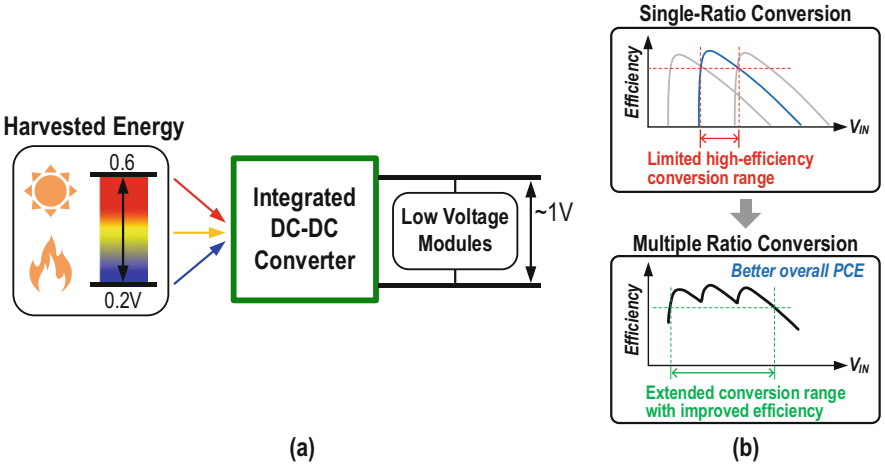

Fig. 16 (**a**) DC-DC converter with a wide input voltage range for DC-type energy harvesting powered systems. (**b**) Efficiency improvement over a wide input range through multiple ratio conversion

3.1 SC Converter Power Stage Losses

In general, the power stage intrinsic performance of two-phase SC converters is highly dependent on the charge conduction loss and flying capacitor (C_{fly}) parasitic loss power, which are critical factors that induce the efficiency degradation during the switching operations. Establishing an effective and easy-to-use model to evaluate the SC power stage losses is essential for alleviating the loss influence and optimizing the conversion efficiency in an EH interface. Figure 17a shows an SC converter equivalent model with a generic VCR of m: n [55]. The equivalent output impedance R_{OUT} demonstrates that the conduction losses are dependent on both the slow switching limit loss (R_{SSL}) and fast switching limit loss (R_{FSL}). The converter switching frequency f_{S} dominates the overall R_{OUT} under a given on-chip total capacitance and switch conductance (active area) (Fig. 17b). For a single SC cell, the charge conduction from the input to the output through a C_{fly} generates charge-sharing loss between the voltage source and capacitors, inevitably causing conversion efficiency drop. As depicted in Fig. 17c, under a slow switching condition (i.e., at a low f_{S}), we can evaluate the corresponding periodic loss power with the SC power stage in two-phase operation as

$$P_{\text{ls,SSL}} = \frac{Q_{\text{cond}}^2}{C_{\text{fly}}}. \tag{3}$$

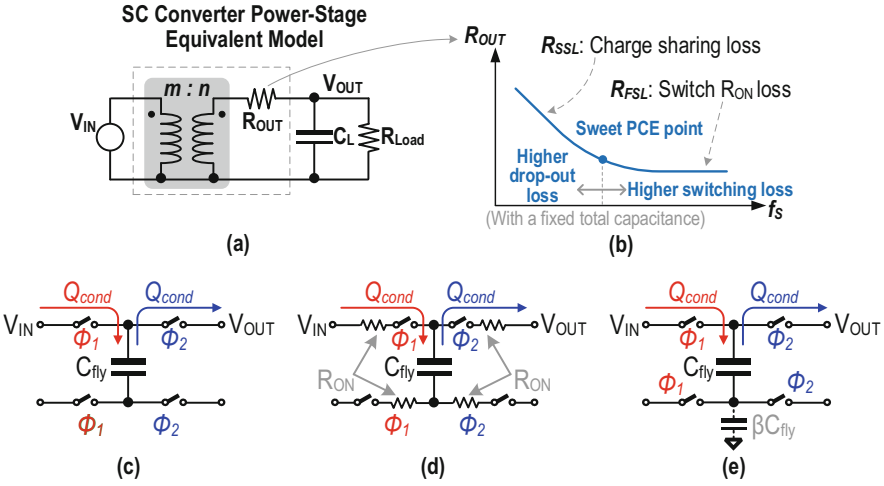

Fig. 17 (**a**) Generalized SC converter power stage equivalent model and (**b**) the equivalent output impedance versus switching frequency under a given total capacitance and switch conductance; the mechanism illustration for (**c**) charge-sharing loss, (**d**) switch conduction loss, and (**e**) bottom plate parasitic loss

where Q_{cond} is the conducted charge amount. On the contrary, at a high f_S, the switch turn-on resistance R_{ON} will dominate the loss power, as highlighted in Fig. 17d. Then, we can calculate the loss power through

$$P_{\text{ls,FSL}} = \frac{Q_{\text{cond}}^2}{2C_{\text{fly}}} \coth\left(\frac{T_S}{2R_{ON}C_{\text{fly}}}\right) f_S \tag{4}$$

With Eqs. (3) and (4), the equivalent R_{SSL} and R_{FSL} for a single SC cell becomes

$$R_{SSL} = \frac{1}{f_S C_{\text{fly}}} \left(\frac{Q_{\text{cond}}}{Q_{OUT}}\right)^2 \tag{5}$$

$$R_{FSL} = \frac{R_{SSL}}{2} \cdot \coth\left(\frac{1}{4f_S R_{ON} C_{\text{fly}}}\right) \tag{6}$$

where Q_{OUT} denotes the periodic delivered output charges. Regarding Eq. (6), as f_S approaches to infinitely high, the R_{FSL} asymptotic limit is

$$R_{FSL}|_{f_S \to \infty} = 2R_{ON} \left(\frac{Q_{\text{cond}}}{Q_{OUT}}\right)^2 \tag{7}$$

As observed, Eqs. (3)–(7) describe the loss of a single SC cell. Consequently, we need to add up the corresponding losses from all SC power cells in a converter power stage to obtain the overall R_{SSL} and R_{FSL}. From [55], we can estimate the overall R_{OUT} for an SC converter power stage by

$$R_{OUT} \approx \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{8}$$

In addition to the conduction loss, C_{fly} parasitic loss can also affect the conversion efficiency. The parasitic loss is especially critical for fully integrated SC converters because the on-chip capacitor devices generally suffer from the considerable top/bottom plate parasitic effect. The parasitic capacitance is typically proportional to the main capacitor size with a factor of β (Fig. 17e). Depending on the capacitor type, the value of β can be up to 0.1. We can use the following equation to evaluate the parasitic loss to the first order for a single SC cell:

$$P_{\text{ls,par}} = \beta C_{\text{fly}} \cdot \Delta V_{CP}{}^2 f_S \tag{9}$$

where ΔV_{CP} is the top/bottom plate voltage swing of the C_{fly}. The above-discussed conduction and parasitic losses can directly restrict the achievable conversion efficiency. The related discussion on the optimization of the SC converter power stage losses appeared in [34, 43, 55, 56].

3.2 Two-Dimensional Series-Parallel (SP)-Based Topology for Fractional VCR Generation

Several state-of-the-art topology techniques obtained reduced conduction and parasitic losses when generating fine-grained step-down VCRs [44, 48, 49]. An integer-cascading-fractional power stage architecture is a widely adopted topology solution to provide wide-range and fine-grained conversion ratio generation. Such an approach involves a converter stage that realizes a high integer VCR and a cascaded SC stage that features fractional ratio conversion to fine-tune the output levels [38, 39]. Still, this method may suffer from suboptimal conduction losses when realizing rational boost VCRs in wide range, especially in on-chip conversion scenarios due to the limited total capacitor area. We can express a general rational boost VCR as below:

$$\mathrm{VCR} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = K + \frac{m}{n}, \tag{10}$$

where K, m, and n are all positive integers with $m \leq n$ and m and n are relatively prime. In Eq. (10), we can implement the integer part of the ratio (i.e., K) using a well-developed classic integer topology, for instance, Dickson SC topology, to realize optimal on-chip loss reduction [34, 57], while we can implement the fractional ratio m/n by series-parallel (SP) topology, one of the most well-known solutions for the fractional VCR generation, using relatively modular power cells. As a designer, we can adopt an m-row-by-n-column power cell array to construct the SP power stage for implementing a flexible ratio of m/n [43, 58]. Figure 18a illustrates such a topology, defined as a two-dimensional SP (2DSP) structure. Cooperating with an integer conversion stage (e.g., Dickson structure), the 2DSP-based SC converter features high step-up rational VCR generation. To obtain a complete on-chip capacitor utilization, we can reallocate part of the C_{fly} to generate either the integer or fractional ratios [50, 59], enhancing the charge-sharing loss reduction (equivalently, lowering the R_{SSL}).

Regarding the discussed R_{SSL} loss metric, as described in Eq. (5), its optimal level when generating a boost VCR expressed in Eq. (10) under a given total flying capacitance C_{TOT} is

$$R_{\mathrm{SSL,opt}} = \frac{1}{C_{\mathrm{TOT}} f_{\mathrm{S}}} \left(\frac{Kn + m - 1}{n} \right)^2. \tag{11}$$

The above equation is valid for the existing SC boost topologies, and it involves the loss from both the integer and fractional stages. In the following discussion, we assume the generation of the integer ratio (K), based on the Dickson topology, for optimal losses in fully integrated implementation scenarios.

We discuss the issues of using 2DSP topology when generating a fractional ratio of m/n [52]. Figure 18 demonstrates the two-phase operation for implementing the

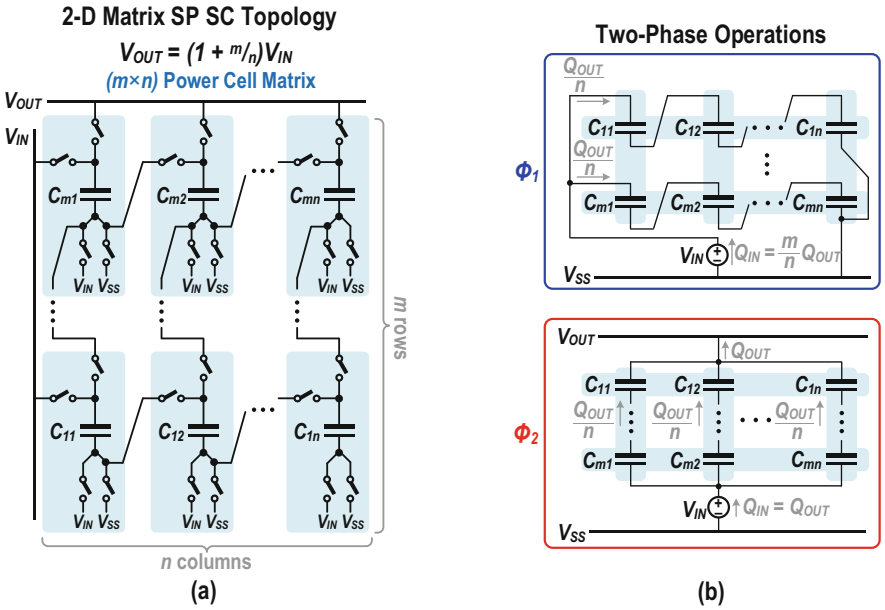

Fig. 18 (**a**) Generalized 2DSP SC power stage and (**b**) its two-phase operation states

VCR in Eq. (10) using the 2DSP topology, where the voltage $(K-1)V_{\mathrm{IN}}$ is from the integer ratio stage (Dickson SC). The $m \times n$ SC cell array produces the ratio m/n. A flexible assignment of m and n can ensure high fractional VCR possibilities. Giving that the integer part exhibits the optimal R_{SSL} property, the corresponding R_{SSL} for a general 2DSP topology under optimized C_{fly} charge flow assignment is

$$R_{\mathrm{SSL,2DSP}} = \frac{\left(\sum_{i=1}^{N_{\mathrm{C\_2DSP}}} |a_{\mathrm{c},i}| + \sum_{k=1}^{N_{\mathrm{C\_int}}} |a_{\mathrm{c},k}|\right)^2}{C_{\mathrm{TOT}} f_{\mathrm{S}}} = \frac{(m+K-1)^2}{C_{\mathrm{TOT}} f_{\mathrm{S}}}, \tag{12}$$

where $N_{\mathrm{C\_2DSP}}$ and $N_{\mathrm{C\_int}}$ are the total number of power cell units in the fractional and integer power stage, respectively. We can compare the $R_{\mathrm{SSL,2DSP}}$ in Eq. (12) with the $R_{\mathrm{SSL,opt}}$ in Eq. (11) through the following analysis:

$$\sum_{i=1}^{N} |a_{\mathrm{c},i}|_{(\mathrm{2DSP})} - \sum_{i=1}^{N} |a_{\mathrm{c},i}|_{(\mathrm{opt})} = m + K - 1 - \frac{Kn + m - 1}{n} = \frac{1}{n}(mn - n - m + 1). \tag{13}$$

From the above equation, since it defines m/n as a proper fraction with $n \neq 1$, a possible solution for $R_{\mathrm{SSL,2DSP}} = R_{\mathrm{SSL,opt}}$ is $m = 1$. Obviously, the 2DSP-based topology pulls off a suboptimal R_{SSL} with most of the conversion ratios except for

using a $1 \times n$ array (a special case) to implement a VCR of $(K + 1/n)$. Such a special case can only realize a limited set of fractional part of VCR between 0 and 1/2, which can degrade its application flexibility.

3.3 *Algebraic Series-Parallel (ASP)-Based SC Topology Development*

From the above discussion, even though the 2DSP-based topology can reach a good VCR flexibility by an $m \times n$ capacitor array, it in fact suffers from suboptimal R_{SSL} in most of the VCR cases due to using extra C_{fly}. Besides, the 2DSP topology also exhibits relatively larger C_{fly} bottom plate voltage swing ($|\Delta V_{CB}|$), resulting in increased C_{fly} parasitic loss. Those limitations affect the achievable conversion efficiency of the 2DSP-based wide-range fine-grained converter, especially for on-chip implementations. To resolve the suboptimal R_{SSL} and increased parasitic loss limitations in the conventional 2DSP, we introduced an algebraic SP (ASP) topology technique, which can theoretically deliver optimal R_{SSL} and improved parasitic loss, simultaneously, retaining the fractional VCR generation flexibility. The topology development exploits the basic power cell operations of the 2DSP followed by elaborating the V_{OUT} expression using ASP-based topology operations algebraically. By systematically assigning the terminal voltages of the SC power cells in different switching phases according to a simple algorithm, a designer can realize arbitrary rational boost VCRs using the ASP-based method (Dickson + ASP) without using extra C_{fly}. We also limited well the $|\Delta V_{CB}|$ in each cell to reduce the parasitic loss.

According to Fig. 18, we can represent the integer part generation by the voltage $(K-1)V_{IN}$ for simplicity. Then, we can express the realization of the VCR in Eq. (10) by the 2DSP-based topology as

$$V_{OUT,2DSP} = V_{IN} + \left(m \times \frac{V_{IN}}{n}\right) + (K-1)V_{IN}, \tag{14}$$

with the second and third terms implemented using the 2DSP and the integer conversion stage, respectively. By stacking both parts over the converter input, we can obtain the final output. One limitation with the 2DSP is that the fractional part during the topology reconfiguration highly relies on m and n, resulting in an excessive number of C_{fly} and leading to a suboptimal R_{SSL}. Furthermore, the limited capacitor voltage of $(1/n)V_{IN}$ also results in a higher bottom plate switching voltage $|\Delta V_{CB}|$, which contributes to significant parasitic loss.

Tackling the issues in the 2DSP structure, Fig. 19 represents the two-phase ASP-based implementation for realizing the VCR in Eq. (10), featuring a uniform charge flow amount through each capacitor. The corresponding algebraic V_{OUT} expression becomes

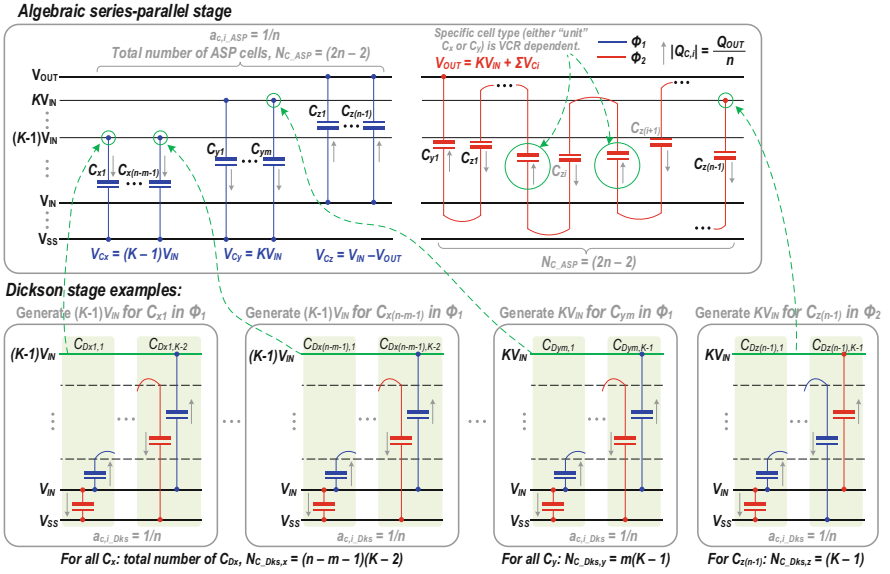

Fig. 19 Operation states for the ASP-based rational VCR boost topology with the integer-level generation by Dickson SC structure

$$V_{\mathrm{OUT,ASP}} = KV_{\mathrm{IN}} + (n-m-1)(K-1)V_{\mathrm{IN}} + mKV_{\mathrm{IN}} + (n-1) \times (V_{\mathrm{IN}} - V_{\mathrm{OUT}}) \tag{15}$$

As observed above, we construct the V_{OUT} expression with the summation of different items. The included $(V_{\mathrm{IN}} - V_{\mathrm{OUT}})$ term enables flexible m/n generation without dividing V_{IN} as the operation in 2DSP. Figure 19 shows the corresponding two-phase operations. During Φ_2, all the $(2n-2)$ SC cells connect between KV_{IN} and V_{OUT}, featuring the SP-like operations. The increased C_{fly} voltages help to lower the bottom plate switching voltage and hence reducing the parasitic loss. Similarly with the previously discussed 2DSP case, we can generate the KV_{IN} and $(K-1)V_{\mathrm{IN}}$ using Dickson SC stages for optimal conduction and parasitic losses. As illustrated in Fig. 19, the Dickson SC stages operate in parallel. It corresponds to a total of $N_{\mathrm{C\_Dks}} = (Kn - 2n + m + 1)$ capacitors in the Dickson stages with a uniform conducted charge amount of $|(1/n)Q_{\mathrm{OUT}}|$. In the ASP-based topology, there are a total of $(Kn + m - 1)$ power cells (including the Dickson cells) with each cell conducting a uniform charge flow of $|(1/n)Q_{\mathrm{OUT}}|$. Hence, it can theoretically reach the optimal R_{SSL} according to Eq. (11).

3.4 ASP Topology Generation and Analysis

Based on the above-discussed ASP operation concept, Fig. 20 shows a generalized two-phase model for an ASP-based topology framework. It requires a total number of $N_F = 2n - 2$ cells for generating a fractional of m/n for an overall VCR of n: $(Kn + m)$. From Eq. (15), there are $(n - 1)$ C_{fly} connected to the $(V_{IN} - V_{OUT})$ level, and the other $(n - m - 1)$ and m cells are charged by $(K - 1)V_{IN}$ and KV_{IN}, respectively. Also in Fig. 20, the odd cells are with $(K - p)V_{IN}$ and the even cells are with $(V_{IN} - V_{OUT})$. This cell arrangement ensures a pair-wise operation that can reduce $|\Delta V_{CB}|$. We can define a configuration factor (p) to determine whether we should connect a particular odd cell to $(K - 1)V_{IN}$ or KV_{IN}. The value of p can be either 0 or 1 to generate $(K - p_i)V_{IN}$, where i denotes the cell sequence index. Furthermore, the defined p is not applicable to even cells. Referring to Eq. (15), the sum of all p_i is equal to $(n - m - 1)$ to obtain power stage voltage balance. For the framework in Fig. 20, the steady-state voltage balancing equation is

$$\begin{aligned}&(K - p_1)V_{IN} + (V_{IN} - V_{OUT}) + (K - p_3)V_{IN} + (V_{IN} - V_{OUT}) + \ldots \\ &\quad + \left(K - p_{N_F - 1}\right)V_{IN} + (V_{IN} - V_{OUT}) = V_{OUT} - KV_{IN}.\end{aligned} \tag{16}$$

Reorganizing Eq. (16), we have the VCR expression as

$$\mathrm{VCR}_{ASP} = K + \frac{N_F - 2\sum_{k=1}^{N_F/2} p_{2k-1}}{N_F + 2}. \tag{17}$$

By substituting $\Sigma p_k = n - m - 1$ and $N_F = 2n - 2$ into Eq. (17), we can have the same VCR expression as in Eq. (10).

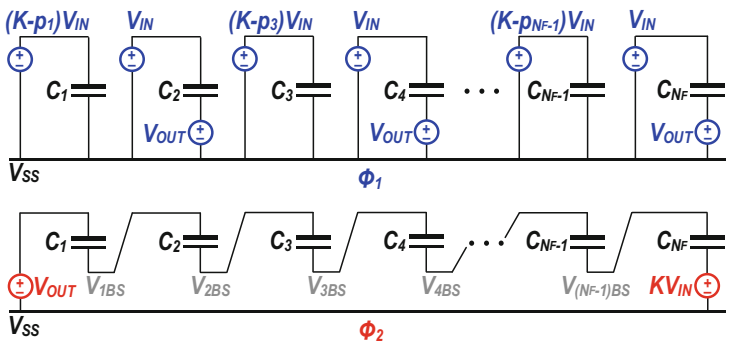

Fig. 20 Operation states for a general ASP-based boost topology (the integer-level generation by Dickson SC structure)

Observed in Eq. (17), the result of p_k is not unique, indicating that there are multiple sets of p to deliver the same VCR with optimal R_{SSL}. Yet, it may introduce suboptimal parasitic loss depending on the specific p_k determination. The algorithm presented below ensures a systematic p selection together with parasitic loss reduction:

$$p_i(i \text{ is odd}) = \begin{cases} 1, & \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right) > 1 + \sum_{k=0}^{(i-1)/2} p_{2k-1} \\ 0, & \left(\frac{i+1}{2}\right)\left(1-\frac{m}{n}\right) < 1 + \sum_{k=0}^{(i-1)/2} p_{2k-1} \end{cases} \tag{18}$$

From Eq. (18), we can find that p_i is dependent on m/n and the specific configurations of its previous cells. Figure 21 describes illustratively well the procedure for p_i determination. By applying the above cell determination rules, the ASP power cell ordering (Fig. 20) ensures that we can well bind the $|\Delta V_{\mathrm{CB}}|$ below V_{IN} for reduced parasitic loss with a specific m/n.

According to the aforementioned loss analysis for a generic SC power stage, Fig. 22a exhibits the R_{SSL} comparison between the ASP-based and the 2DSP-based topologies when generating rational VCRs between 1:1 and 1:6 under a constraint condition of the same total capacitance. In the comparison, we set the fractional part of the VCR as $m/n = \{1/5, 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5\}$. We used the Dickson SC stages in both ASP and 2DSP cases to realize integer ratios, including also the corresponding loss contributions for fair comparisons. Regarding the integer gain generation, the corresponding required number of "unit" power cell in the 2DSP-based topology is typically more than that of the ASP-based topology. Hence, it leads to a higher R_{SSL} under the same C_{fly} area. From Fig. 22a, the ASP-based topology achieves evidently lower R_{SSL} for the whole range in contrast to the 2DSP-based topology, except for the cases of $m = 1$, which exhibits the same R_{SSL} for both implementations.

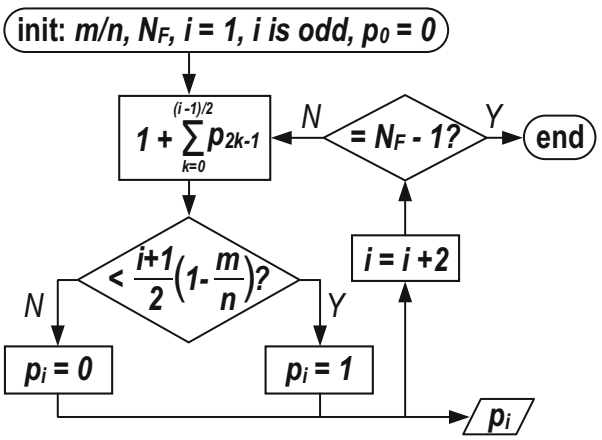

Fig. 21 Flowchart of p_i determination process for the ASP topology

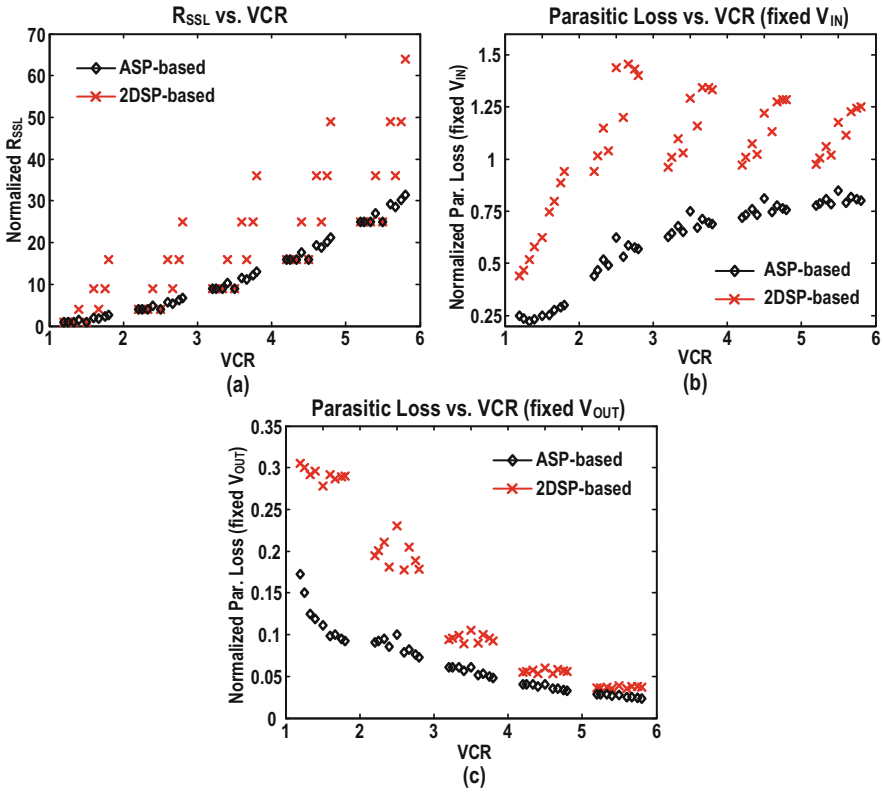

Fig. 22 Theoretical comparison between the ASP-based and the 2DSP-based topologies with the fractional VCRs from 1:1 to 1:6 on (**a**) the R_{SSL} (normalized to $C_{TOT}f_S$), (**b**) the parasitic loss (normalized to $\beta C_{TOT}f_S V_{IN}$) under fixed-V_{IN}, and (**c**) the parasitic loss (normalized to the same $\beta C_{TOT}f_S V_{OUT}$) under fixed-V_{OUT}

Figure 22b, c show the parasitic loss comparison between the ASP-based and the 2DSP-based topologies. The power loss takes the integer and fractional parts into account in both cases. Furthermore, we can observe that the ASP-based technique effectively reduces the parasitic loss in all the modeled VCRs when compared with the 2DSP-based technique. In Fig. 22c, because of the parasitic loss at higher frequency, we did not scale any of the VCRs by decreasing V_{IN}; the loss difference between the two topologies becomes smaller when VCR increases.

3.5 ASP-Based SC Boost Converter Implementation

This part introduces an ASP-based fully integrated SC boost converter with seven rational VCRs to support a wide input voltage range. Each SC power cell can be

reconfigured to generate either the integer or fractional ratios. Thus, the whole design achieves full capacitance utilization for optimizing the R_{SSL}. Figure 23a displays the SC converter overview. The power stage operates consists of dual interleaved branches operating with a 180-degree phase difference. Each branch consists of four SC cells ($C_{1 \sim 4}$) with the top and bottom plate terminals connected to V_{IN}, V_{OUT}, or V_{SS} for implementing different ratio configurations. A four-phase nonoverlapping (NOV) clock generator is employed with an externally injected master clock to reduce the shoot-through loss due to the short circuit conduction state. This design adopts an adaptive bootstrapping (ABS) gate driving technique for robust power switch control over a wide voltage dynamic range. The configuration control of all the seven VCRs is through receiving a three-bit binary code (D_{VIN}), which determines the specific topology demand according to practical conditions.

The designed ASP-based SC boost converter was implemented in a 65 nm bulk CMOS process. The total flying capacitance is about 3 nF. The on-chip filtering capacitance contains 1 nF for V_{OUT} and 0.3 nF for V_{IN}. All the on-chip SC cell implementations employ parallel-connected MIM and MOS capacitors, stacking longitudinally to save the on-chip area. This design features using low-voltage power switches to improve the switch on-resistance (R_{ON}) and reduce the switching loss. The implemented converter can boost a V_{IN} between 0.25 V and 1 V to a V_{OUT} of 1 V. Figure 23b exhibits the converter die micrograph with building block annotations, with the power switches, drivers, NOV clock generators, and buffers placed between the dual branch power cells. The chip occupies an active area of 0.54 mm^2.

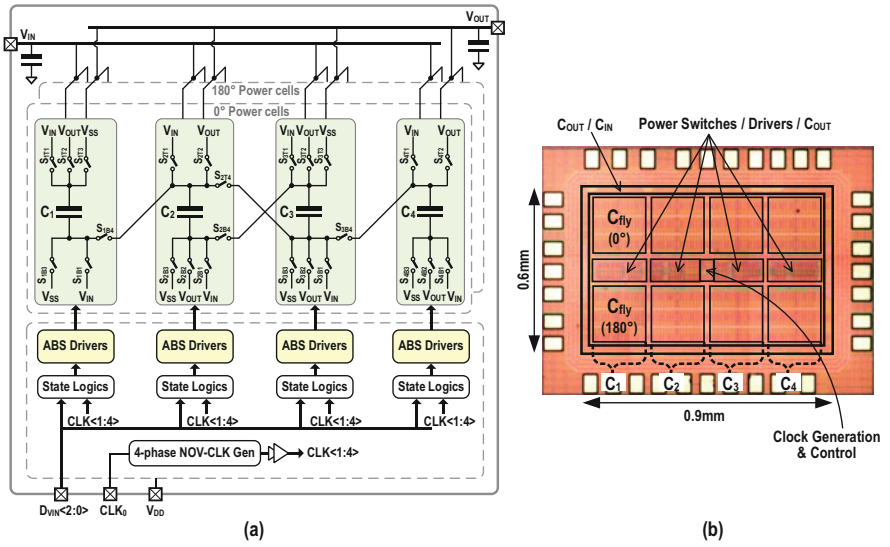

Fig. 23 (**a**) System overview of the implemented ASP-based SC boost converter and (**b**) the corresponding converter die micrograph

The SC boost converter shown in Fig. 23 covers a wide VCR range from 1:1.25 to 1:5, including 4:5, 2:3, 3:5, 1:2, 2:5, 1:3, and 1:5, specifically. By the property of uniform C_{fly} charge flow, the corresponding required SC cell number are 4, 2, 4, 1, 4, 2, and 4, respectively, implying that all seven VCR cases can be realized using $C_{1\sim4}$ with full capacitance utilization. Figure 24 gives a power cell operation and partitioning mode summary. For the implemented VCRs, $C_{1\sim4}$ can be configured to serve as either the Dickson or the ASP power cell. The designed converter generates the rational VCRs of 4:5, 2:3, 3:5, and 2:5 based on the ASP topology. A typical voltage doubler implements the 1:2 ratio, and the conventional Dickson topology generates the VCRs of 1:3 and 1:5 for optimal parasitic loss. In the converter design, $C_{1\sim4}$ can be identical as they have the same charge flow amount under all the seven VCRs, which also include all the possible VCR cases using four C_{fly}.

The converter load regulation control is through pulse-frequency modulation (PFM). We apply a three-bit digital control to achieve the VCR reconfiguration together with a resistive ladder-based input voltage detector. To resolve the startup issue at low input voltage, we can use on-chip charge-pump techniques.

Figure 25 plots the measured power conversion efficiency (PCE) using a variable resistive load R_L over the targeted input voltage range and a fixed V_{OUT} at 1 V. The resistive loading changes from 85 Ω to 800 Ω, except for VCR = 1:5 with R_L limited to 200 Ω due to the higher R_{SSL}. The measured peak PCE (η_{peak}) is ~80% with R_L between 85 Ω and 100 Ω at VCR = 2:3. From Fig. 22c, the 2:3 ratio with the ASP-based topology shows a lower parasitic loss than that with the ratio 4:5, which is in turn lower than the 1:2 ratio case. Consequently, the measured PCE for 1:2, 4:5, and 2:3 increases progressively, as displayed in Fig. 25. Regarding the ratio 3:5, even though the parasitic loss is slightly less than that of the ratio 2:3, its property of relatively higher R_{SSL} loss (Fig. 22a) eventually affects the achievable PCE, corresponding to the measured results exhibited in Fig. 25.

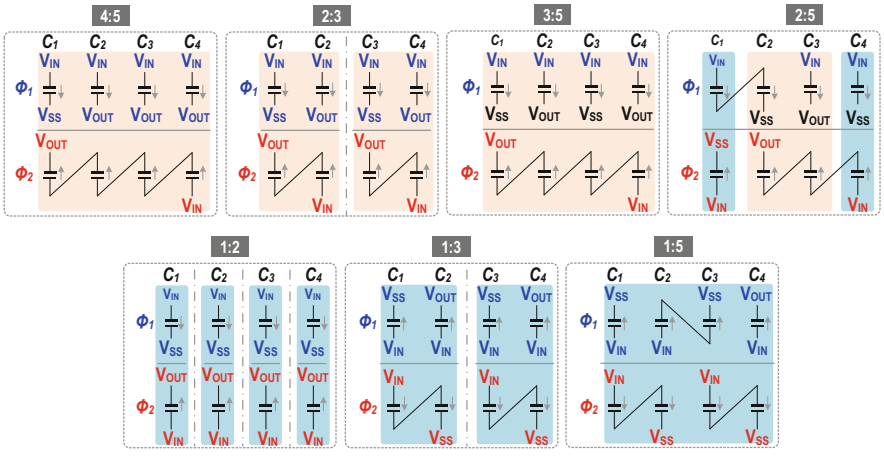

Fig. 24 Summary of the power stage operating modes under all the seven VCRs

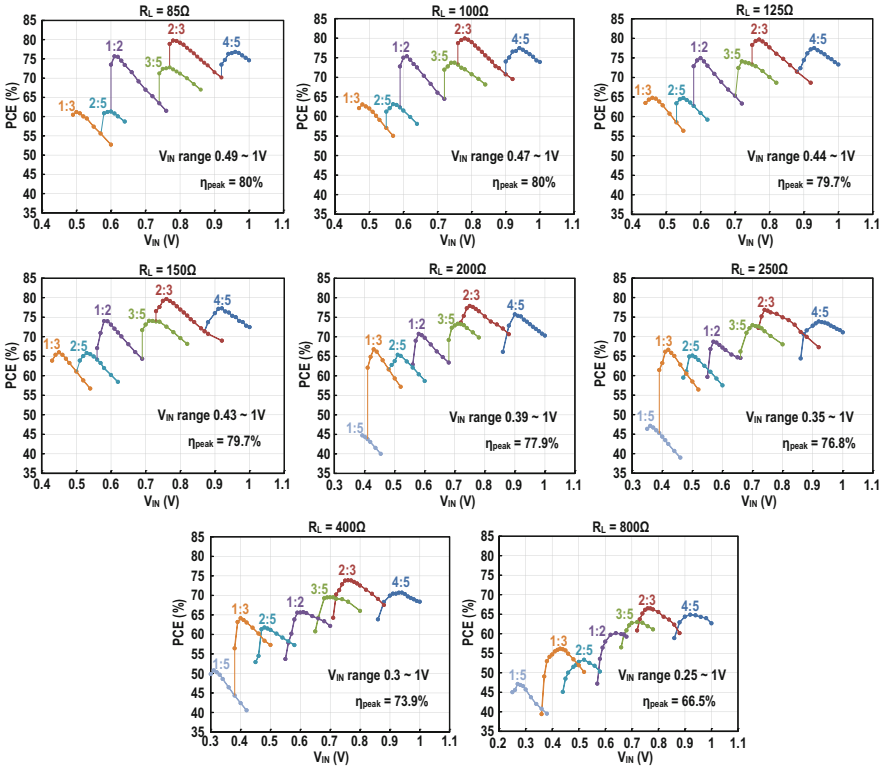

Fig. 25 Measured PCE over the targeted V_{IN} range under different resistive loads when generating a V_{OUT} of 1 V

Figure 26 exhibits the measured PCE over an output power range for each implemented VCR under a fixed $V_{OUT} = 1$ V. The output power ranges from 1.2 mW to 20.4 mW, with a maximum power delivered at VCR = 1:2. Moreover, due to the specific V_{IN} selection, the results in the plot do not include the overall peak PCE point for the converter.

Table 3 summarizes the measured performance and presents a comparison of the ASP-based converter with other state-of-the-art designs. In the table, the design presented in [38] based on SP topology adopts high-density MIM capacitors to implement the C_{fly}, hence, featuring low bottom plate parasitic capacitance. As the ASP-based converter exhibits a property of lower R_{SSL} and parasitic losses, it demonstrates a comparable peak efficiency (η_{peak}) as [38], but with an estimated 1300 times power density improvement by employing higher density capacitance (MIM+MOS) as the on-chip C_{fly}. In contrast, with the customized design using the fully depleted silicon-on-insulator (FD-SOI) process in [59], which realizes a higher η_{peak}, the ASP-based converter design attains more than 4.6× power density enhancement in bulk CMOS with finer-grained VCRs. The discussed ASP-based converter also demonstrates higher peak efficiency and higher power density than

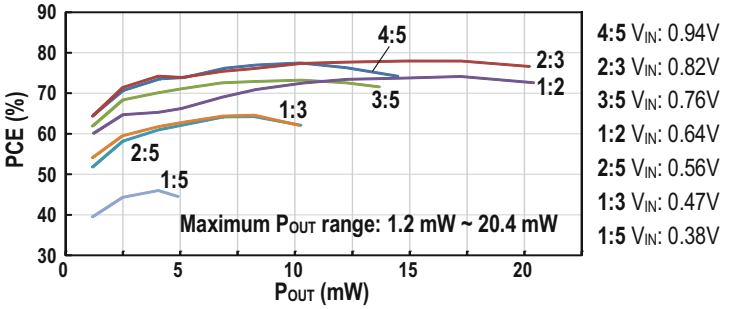

Fig. 26 Measured PCE over different output power range under fixed V_{OUT} of 1 V (DC) for all the seven VCRs

Table 3 State-of-the-art SC converter performance summary and comparison

	ASP design	JSSC'16 [39]	JSSC'15 [59]	JSSC'15 [60]	JSSC'17 [39]	JSSC'18 [50]	ISSCC'16 [47]
Technology	**65 nm CMOS**	180 nm CMOS	28 nm FD-SOI	180 nm CMOS	180 nm CMOS	65 nm CMOS	0.35 μm HVCMOS
Conversion type	**Boost**	Boost	Boost	Boost	Boost	Buck-Boost	Buck-boost
Topology type	**ASP-based**	SP-based	Customized	Customized	Moving-sum	AVFI	Binary recursive
VCR type	**Rational**	Rational	Rational	Integer	Integer	Rational	Rational
Number of VCR	**7**	14	3	2	[a]22	13 (boost)	9 (boost)
VCR range	**1.25 ~ 5**	1.33 ~ 8	1.5 ~ 2.5	4 ~ 6	10 ~ 31	1.1 ~ 7 (boost)	1.14 ~ 4 (boost)
Integrated C_{fly}	**MOS + MIM**	HD-MIM	MOS + MOM	MOS + MIM	N/R	MOS + MIM	MIM
V_{IN} Range [V]	**0.25 ~ 1**	0.45 ~ 3	1	1	0.25 ~ 0.65	0.26 ~ 1.3 (boost)	2 ~ 6 (boost)
V_{OUT} [V]	**1**	3.3	1.2 ~ 2.4	3 ~ 6	4	1.2	5
I_{OUT_MAX} [mA]	**20.1**	0.015	1	0.24	[a]0.001	21.7 (boost)	1.4 (boost)
η_{peak} [%]	**[a]80**	81	[a]88	58	60	83.2 (boost)	70.9 (boost)
***P*-density @η_{peak} [mW/mm^2]**	**[a]22.7**	[a]0.0174	[a]4.9	[a]2.4	[a]~0.0001	10.8 (boost)	[a]0.15 (boost)
Fully integrated	**Yes**	Yes	Yes	Yes	Yes	Yes	Yes

[a]Estimated from the corresponding literature
[b]Regulation control executed externally

[47, 60] in boost conversion modes. In contrast to the boost mode reported in [50], the achieved power density by the ASP-based design is 2.1× higher through reducing the power stage control redundancy. Figure 27 benchmarks the state-of-the-art fully integrated SC boost converters, including the discussed ASP-based design, in both bulk CMOS and special processes. We can observe that the ASP-based converter results in a higher power density while attaining a high number of VCR when compared with the existing designs in bulk CMOS.

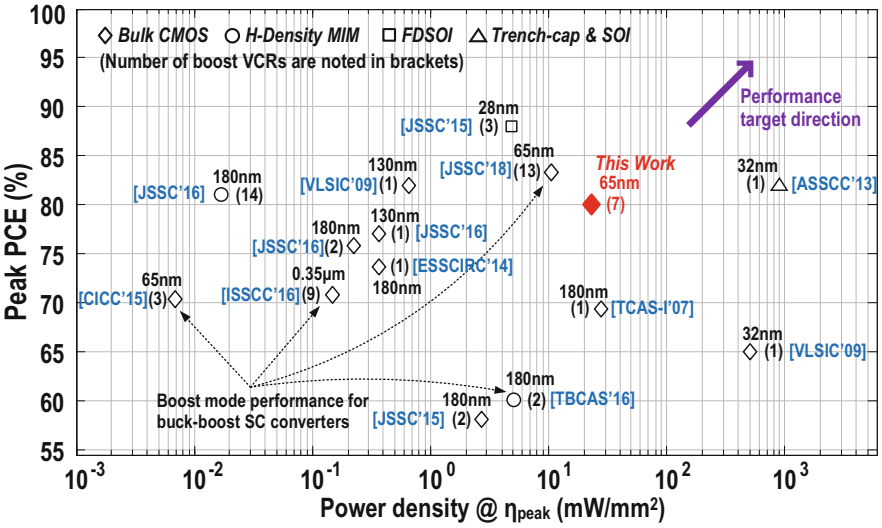

Fig. 27 Performance benchmarking with state-of-the-art fully integrated SC boost converters

4 Conclusions

In this chapter, we introduced different energy harvesting interface designs using switched-capacitor (SC) power converters suitable for miniaturized IoT systems. In terms of vibration (AC-type) sources, we discussed both the FCR and SPFCR interfaces, which can significantly increase the PEH energy extraction efficiency without using external bulky high-Q inductors to obtain a compact system implementation. We can further employ the reusing of the capacitors in the SPFCR to achieve multi-VCR DC-DC conversion for wide input-power range adaptation in a component efficient manner. In terms of solar/thermal (DC-type) sources, we studied the ASP topology, which can attain an optimal conduction loss and reduced parasitic loss in the power stage. The employment of MIM+MOS as flying capacitors can significantly improve the power density over prior arts, while featuring a peak efficiency of up to 80% without using any external components. The proposed techniques can be especially useful for the next-generation low-cost miniaturized IoT systems with an extreme level of integration.

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