High-Performance Oversampling ADCs

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1 Introduction

Driven by the rapid development of IoE, the performance of wireless communication SoCs demand high power efficiency while simultaneously allowing a wideband and high-resolution input/output signal for massive information throughput. In the receiver end, the performance bottleneck always lies in the analog-to-digital process, where the analog-to-digital converters (ADCs) need to have high dynamic range and exhibit low noise and with high-energy efficiency. Nevertheless, such a mixed-signal building block does not enjoy all the benefits inherited from the technology scaling, and it will become challenging a design to meet all the above aspects.

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Modern Wi-Fi and mobile communication standards call for an ADC with a few tens to hundred megahertz of bandwidth and with a dynamic range close to 80 dB. The continuous-time (CT) delta-sigma converter inherently embeds anti-aliasing and is the block to drive the system earlier due to its high impedance input interface. A discrete-time delta-sigma modulator (DSM) conventionally shows no obvious advantage, but when deeply hybridized with a successive approximation register (SAR) ADC, usually designated as noise-shaping (NS) SAR, the energy efficiency surpasses the CT-DSMs at a relatively low bandwidth design target. The work described in [1] introduced a multi-loop to reduce the performance gap between CT and discrete-time (DT) DSMs, increasing the noise-shaping order for higher SQNR (signal-to-quantization-noise ratio) at a low oversampling ratio (OSR). A Sturdy multistage NS delta-sigma (MASH) also designated as SMASH and an additional error feedback (EF) loop can relax the critical matching DAC. Preliminary sample and quantization techniques in [2] provide extra quantization during an idle time in the excess loop delay (ELD) compensation period, pushing the single-loop CT DSM toward low power at wide bandwidth. On the other hand, we can also extend a NS SAR ADC into a multistage configuration as in [3] and [4]. Besides, with partial interleaving techniques, a tens of megahertz bandwidth is possible. Furthermore, [3] also utilizes the residue amplifier in the pipeline architecture for EF-type NS. The N-0 multistage NS sigma-delta MASH structure in [4] further simplifies the critical gain accuracy in the NS pipeline SAR architecture.

The organization of this chapter is as follows: Section 2 introduces a SMASH CT DSM. Section 3 details the preliminary sample and quantization technique with the CT DSM. Then, Sects. 4 and 5 introduce two different NS pipeline SAR ADCs.

2 Sturdy Multistage Noise-Shaping (MASH) Continuous-Time (CT)-Delta-Sigma Modulator (DSM)

A large signal bandwidth required by wireless telecommunication applications restrains the OSR used for the DSMs. To obtain the desired resolution while keeping a better power efficiency, we need to explore the following two dimensions together in the design of the DSM.

On one hand, the DSM should aim to secure an aggressive NS. However, a higher NS order suffers from instability in a single-loop topology. Alternatively, we can use the multistage noise-shaping (MASH) [1] architecture to overcome the instability issue. Nevertheless, the noise leakage inherently exists in MASH DSMs resulting from the mismatch between analog and digital filters. A DT solution is more robust for the MASH over its CT counterpart whereas the speed remains the bottleneck. Besides, it is necessary to improve the opamp efficiency in a DT MASH. Due to the inherent switching activity, we can apply an opamp sharing technique to reduce the number of required opamps in a DT DSM [5], reducing the power and area consumptions. However, we can further improve the opamp sharing efficiency in a

DT MASH [6]. The CT solution allows a larger signal bandwidth and a better power efficiency whereas the noise leakage is detrimental in a CT MASH. The CT sturdy MASH (SMASH) [7] poses a high potential to replace the CT MASH as it exhibits a relaxed matching requirement to reduce the noise leakage.

On the other hand, we can employ a multibit quantizer to improve the resolution further and mitigate the requirements of the loop filter. Yet, the multibit feedback DAC is nonlinear owing to the element mismatch, dictating a DAC linearization technique. We can perform the DAC linearization by using either a dynamic element matching (DEM) technique or calibrations. DT architectures favorably use the DEM when the sampling frequency is relatively low. But, with a multi-GHz sampling frequency in CT solutions, the DEM is neither feasible enough nor power friendly. Instead, it is common to find DAC calibrations in wideband CT DSMs to address the DAC nonlinearity issue. Nevertheless, the on-chip DAC calibration [8] requires additional power and area consumptions. Moreover, the off-chip DAC calibration [9] is not able to track the current source mismatch error over temperature variations, which is not desirable in a high-performance CT DSM.

2.1 Related Prior Arts

To implement a large signal bandwidth required by the mainstream LTE-A cellular standard, the CT DSM is undoubtedly preferable. Besides, with low supply voltage required in an advanced process, a SAR ADC as a quantizer poses a potential attractive alternative to a traditional flash ADC. However, a SAR ADC usually demands multiple clock cycles for quantization, thus imposing a larger timing headroom when compared with a flash architecture. Therefore, most of the reported SDMs employing a SAR as the quantizer only attained a small signal bandwidth [10, 11].

The MASH DSM circumvents the stability problem associated with high-order noise shaping, but the CT MASH suffers from the mismatch between the analog and the digital filter. By feeding the second stage into the first loop, the SMASH provides a solution to this leakage issue. Still, the quantization error extraction and cancellation are still challenging due to the delay and phase shift in a CT SMASH. The work [7] presents a CT SMASH for the first time, addressing the quantization error extraction and cancellation. Figure 1 presents the block diagram of a CT SMASH. As foreseen, there is one propagation delay introduced by the first quantizer. Then, with a CT input and a delayed DT output, the correct extraction of the quantization noise E_{q1} from the first quantizer would be somewhat problematic. Straightforwardly, in Fig. 1, it is necessary to generate the same delay for the CT input of the first quantizer in order to extract correctly E_{q1}. Theoretically, we can employ a sample and hold circuit to obtain such a delay. However, with a multi-GHz sampling frequency, the sample and hold topology is not power friendly at all. Instead, the proposed CT SMASH with a passive RC low-pass filter (LPF) to generate such a delay is feasible owing to the oversampling property. Moreover, to eliminate

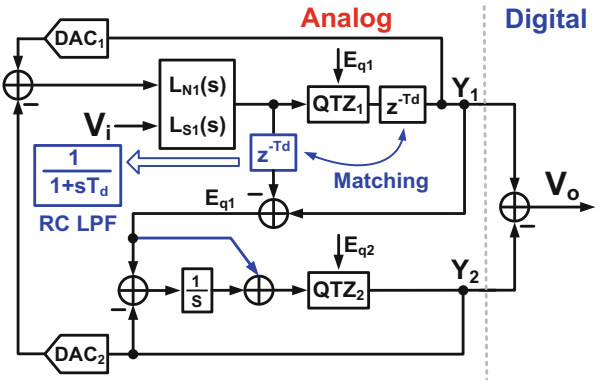

Fig. 1 A CT 3–1 SMASH DSM using feedforward in the second loop [7]

effectively the quantization noise E_{q1}, we can properly select a first-order FF topology for the second loop to implement a unity-gain STF (standard transmission format) within the band of interest.

Nonetheless, the delay generated by the passive LPF is very sensitive to temperature and process variations. Any delay mismatch results in leakage of the signal and therefore may overload the second loop. Besides, the LPF attenuates the high-frequency components, thus introducing a second peaking in the STF, not at all desirable.

2.2 *Proposed CT Sturdy MASH with DAC Nonlinearity Tolerance*

To reach 50 MHz signal bandwidth for LTE-A applications, it is almost impossible to continue using a DT MASH architecture. Instead, a CT solution allows implementing such a large signal bandwidth. A CT sturdy MASH poses higher potential over a CT MASH owing to its relaxed matching requirements [7]. Nevertheless, as mentioned before, the quantization error cancellation and its extraction are still challenging in the CT domain. Besides, DAC nonlinearity becomes problematic with multi-GHz sampling frequency since DEM is less effective at low OSR, while DAC calibrations require large power and area consumptions. Thereby, we will present a more robust CT SMASH DSM in terms of quantization error extraction and its cancellation. Moreover, it would employ multibit quantization to gain good stability, relaxed dynamic requirements of the loop filter, large maximum stable amplitude (MSA), and out-of-band gain (OBG) while achieving high linearity but avoiding any linearization technique in all multibit DACs to reduce power and area costs.

To pull off the above design goals, we introduce a dual-stage noise-coupling-assisted CT SMASH DSM using 1.5bit/4bit quantizers in both stages [12, 13]. By effectively eliminating 1.5bit quantization noise from the first stage, the SMASH

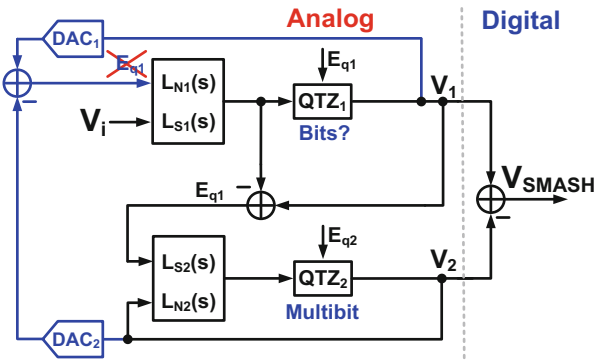

Fig. 2 Practical implementation of a CT dual-stage SMASH DSM

DSM enjoys all benefits provided by multibit operation of a DSM. The noise cancelling (NC) technique [14] applied in the SMASH not only improves the noise-shaping order by one but also works as dithering for the highly tonal 1.5bit quantization noise and further reduces its in-band tone power. Meanwhile, an FIR filter [15] incorporated in the outermost feedback path reduces the out-of-band (OOB) noise power in the nonlinear DAC input to alleviate quantization noise folding. Both features significantly mitigate the requirement for a highly linear multibit DAC, thus circumventing any DAC linearization while delivering high linearity. Moreover, we employed a SAR ADC for a 1.5bit quantizer allowing extraction of the quantization error using switched capacitor (SC), which is robust over process and temperature variations. Meanwhile, the selection of a zeroth-order architecture for the second loop eliminates more accurately the quantization error.

In practice, to speed up the whole feedback loop, we will not implement the subtraction in the digital domain by using a digital adder. Instead, as Fig. 2 shows, we obtain the subtraction in the analog domain through DAC_1 and DAC_2 in parallel in the front-end. The analog subtraction allows the ideal removal of E_{q1} inside the first loop filter. As a result, the number of bits of the quantizer used in the second loop merely determines the MSA and the OBG of the SMASH DSM. Since the OSR is low for wideband applications, we can advantageously use multibit quantization in the second quantizer to realize large MSA and OBG. Ideally, the resolution of the first-stage quantizer does not affect the performance of the SMASH. Still, a previous CT SMASH implementation [7] also applied multibit quantization in the first quantizer. In the MASH topology, using single-bit quantization in the first and multibit in the later stages is advantageous for DAC linearity due to the single-bit DAC intrinsic linearity and the suppression of multibit DAC nonlinearity in higher stages in the digital cancellation logic. Still, the noise leakage emerges from the first stage related with the single-bit, which is much worse than multibit quantization noise leakage. This leakage argument is still valid for SMASH DSMs. More unfortunately, in contrast to the MASH, with DAC_2 fed back to the most sensitive input node of the overall DSM, using a multibit DAC_2 would anyhow impose DAC linearization. This occurs because the single-bit quantization noise E_{q1} is highly tonal, rather than an approximate white noise as the multibit quantization noise. In

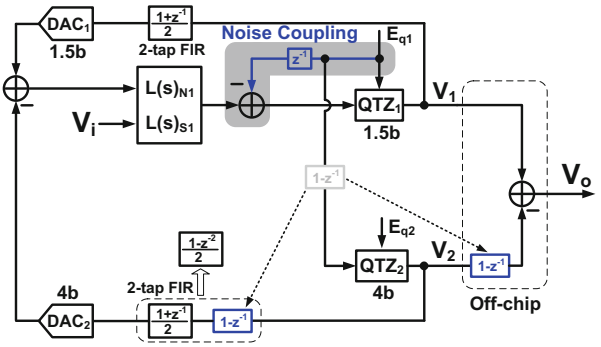

Fig. 3 The overall architecture of the proposed CT SMASH DSM

the SMASH, such highly tonal signal E_{q1} would go through the nonlinear DAC_2 located in the sensitive input front-end, thus introducing harmonic distortions. In addition, the large OOB quantization noise of the second stage mixed by the nonlinearity of DAC_2 would thereby increase the in-band noise floor. Consequently, the linearization of DAC_2 is compulsory in multibit quantization in the second stage of the SMASH. Thus, previous research work about the SMASH architecture did not find any advantage in combining an intrinsically linear single-bit quantization in the first stage with a multibit quantization in the second stage. Yet, this issue subsequently emerged in state-of-the-art SMASH DSMs, and we will address it in the proposed CT SMASH.

Figure 3 presents the overall CT SMASH DSM employing an underlying dual-loop architecture using 1.5bit/4bit quantizers in the first and second loops, respectively. As a result, the circuit processes an effective 4bit quantization noise inside the loop filter of the first stage, thus obtaining decent stability, large MSA, and OBG. Moreover, it applies a first-order noise coupling in the first loop. To account for the applied NC in the first loop and effectively eliminate the first-order noise-shaped E_{q1}, we must implement the corresponding filter $(1 - z^{-1})$ after the extraction of E_{q1}. From Fig. 3, we move this filter from the input (analog domain) of the second stage to its output (digital domain), which allows higher accuracy and further increase of the one noise-shaping order in E_{q2}. In the backend, the combination of the two digital outputs V_1 and V_2 generates the final output V_O, given by

$$V_O = \mathrm{STF}_1 X + (1 - \mathrm{STF}_2)\mathrm{NTF}_1\left(1 - z^{-1}\right)E_{q1} - \mathrm{NTF}_1\left(1 - z^{-1}\right)E_{q2} \qquad (1)$$

The utilization of a 1.5bit quantizer in the first loop, in case of an imperfect cancellation, would leak 1.5bit quantization noise E_{q1} to the final output, thus deteriorating the final performance. To alleviate the 1.5bit quantization noise (QN) leakage, we must design a unity-gain STF_2 as accurately as possible. Thereby, instead of using a first-order feedforward topology as in [3] (Fig. 3), we select a zeroth-order topology for the second loop. Without any opamps involved in the implementation of STF_2, their finite GBWs will not affect anymore the accuracy of the unity-gain STF_2. On the other hand, we can mitigate the opamp GBWs employed

in integrators to be $1 \times F_s$ (F_s is the sampling frequency of the DSM) with an SQNR loss of 3 dB in the proposed SMASH. However, in the general SMASH 3–1, we must keep such GBWs at least close to 3.5*Fs to reduce the 1.5bit noise leakage and keep the system stable.

As a result, the 3–0 topology effectively realizes a SMASH architecture where the first stage provides the noise-shaping order while the second stage determines the effective quantization bit width. Therefore, overall it allows multibit loop filter scaling in the first stage yielding larger MSA and OBG, reduced dynamic loop filter requirements, etc.

The SMASH DSM with a 1.5bit/4bit combination in both quantizers allows intrinsic linearity in the 1.5bit DAC_1 while the 4bit DAC_2 is unavoidably nonlinear. It is noteworthy that using NC not only helps to increase the noise-shaping order but also works as dithering [10] for the highly tonal 1.5bit QN E_{q1}, thus significantly reducing its idle tones and harmonic spurs. Finally, the combination of the NC technique in the 1.5bit quantizer in the first stage and an FIR LPF allows the SMASH DSM to circumvent any linearization technique for the outermost multibit DAC_2, with large in-band tones and large OOB QN highly suppressed before they are nonlinearly processed by the DAC_2.

Figure 4 illustrates the overall schematic of the NC-assisted dual-loop 3–0 SMASH DSM, employing a 1.5bit successive approximation register (SAR) and a 4bit flash ADC for both quantizers, respectively. The input resistance is 250 Ω to satisfy the thermal noise requirement. All DACs use a nonreturn-to-zero (NRZ) trilevel topology, thus resulting in less unit DAC cells as well as less preceding drivers. The first loop employs a third-order mixed feedforward (FF)/feedback (FB) topology, with an OBG of 2.3. The FF/FB combination separates the high-gain and high-speed requirements into the first and third integrators [11], respectively, which allows a better opamp power efficiency. Besides, a local resonator path generated by the first and second integrators introduces one zero in the NTF (non-fungible token) to further suppress the in-band noise. The two FF paths can effectively decrease the swings of the first and second integrators. To compensate the

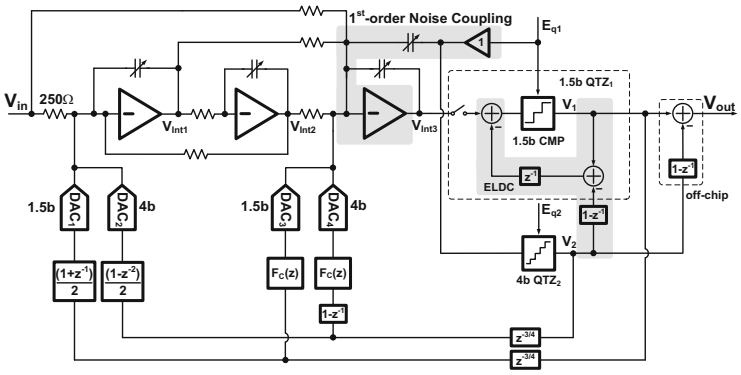

Fig. 4 The overall schematic of the proposed CT SMASH DSM

introduced outermost two-tap FIR filter, we incorporate a simple FIR compensation filter $F_C(z)$ in the inner FB branches that restores the original NTF [12]. To compensate for process variation, the integration and NC capacitors are digitally programmable with a 4bit trimming accuracy, which can cover ±40% RC variations.

By utilizing a 1.5bit SAR ADC for the first quantizer, the circuit naturally produces quantization noise E_{q1} on the summing node by the end of the charge redistribution [5]. Thereby, the capacitor ratio determines the extraction of the quantization noise E_{q1}, which is robust over process and temperature variations. After the SC extraction, the injection of the residue into the last integrator through an SC buffer generates the first-order NC branch [5]. Meanwhile, the SC buffer also directly drives the second stage. In order to close the SMASH loop, this architecture uses $0.75T_S$ as an overall ELD. To compensate the ELD, we integrate a unity-gain zeroth-order path with one cycle delay [13] inside the 1.5bit SAR ADC.

This SMASH DSM renders a fourth-order 1.5bit quantization first loop combined with zeroth-order 4bit quantization second loop into an equivalently operating overall fourth-order DSM architecture with 4bit quantization. With an OSR of 12, it obtains an ideal SQNR of 90 dB.

2.3 *Experimental Results*

Figure 5 shows the chip micrograph of the CT SMASH DSM prototype fabricated in 28 nm CMOS with an active core area of 0.085 mm^2.

Running at a sampling frequency of 1.2 GHz, Fig. 6 plots the measured 65k- FFT output spectrum with a −1.6dBFS input at 6 MHz. It exhibits an expected overall fourth-order noise-shaping slope in the output spectrum. The measured SNDR (signal-to-noise and distortion ratio)/SNR (signal-to-noise ratio)/SFDR (spurious-

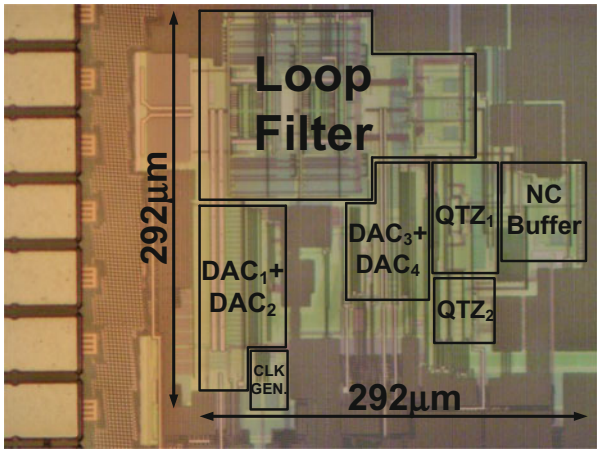

Fig. 5 Chip micrograph of the prototype SMASH

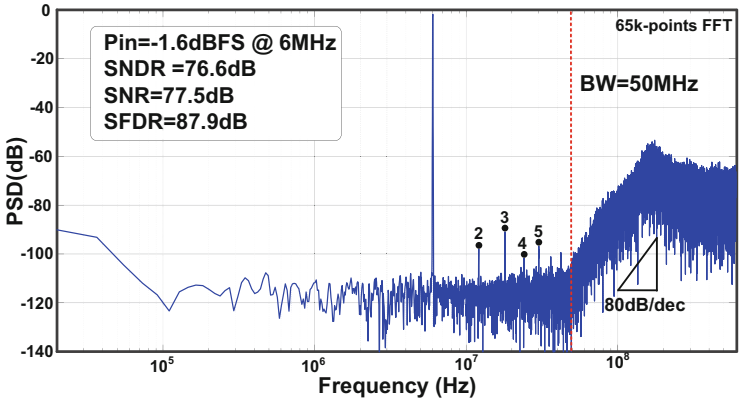

Fig. 6 Measured FFT spectrum of the prototype DSM output

Table 1 Performance summary and comparison with state-of-the-art CT DSMs

	This work	[8]	[17]	[9]	[7]	[18]
Architecture	**SMASH Fourth-order 1.5bit/4bit**	Single-loop Fourth-order 4bit	Single-loop Fourth-order 7bit	Single-loop sixth-order 4bit	SMASH fourth-order 4bit/4bit	Single-loop fourth-order 1bit
Process (nm)	**28**	28	16	65	28	40
Supply (V)	**1.2/1.5**	1.16/1.5	1/1.35/1.5	1.2/1.8	1.2/1.5	N/A
BW(MHz)	**50**	50	125	45	50	40
F_S (GHz)	**1.2**	2	2.15	0.9	1.8	2.4
SNDR (dB)	**76.6**	79.8	71.9	75.3	74.6	66.9
SFDR (dB)	**87.9**	95.2	N/A	83	89.3	N/A
THD (dBc)	**−83.9**	−94.1	−80	−78.1*	−79.9*	N/A
Power (mW)	**29.2**	64.3	54	24.7	78	5.25
Area (mm^2)	**0.085**	0.25	0.217	0.16	0.34	0.02
DAC Cal.	**Without on-chip**	With On-chip	With On-chip	With Off-chip	With On-chip	Without On-chip
FoM_S (dB)	**168.9**	168.7	165.5	167.9	162.7	165.7

free dynamic range) is 76.6 dB/77.5 dB/87.9 dB over a 50 MHz signal bandwidth, respectively.

Table 1 summarizes the performance of the prototype and compares it with other state-of-the-art CT wideband DSMs. It obtains a competitive Schreier FoM of 168.9 dB. Using the proposed techniques, it exhibits high linearity without employing any DAC linearization technique. In contrast, other works [3–5, 14] using multibit quantization either employ on-chip or off-chip DAC calibrations. As obviously observed from Table 1, when compared with such works, the power

and especially the area consumed by this prototype are much smaller. As for the single-bit DSM in [15], even though it avoids the DAC calibration as well, the resolution and the MSA are much lower. Besides, it does not only require significantly smaller input referred noise for the same SNR, but it would also impose stricter noise requirements on the preceding circuitry of the transceiver.

3 A 100 MHz Bandwidth Continuous-Time Sigma-Delta Modulator with Preliminary Sampling and Quantization

Figure 7 presents a fourth-order CT ΔΣ modulator architecture, where the modulator runs at 2 GHz with a bandwidth of 100 MHz, experiencing an OSR of 10. We choose a cascade of integrators in feedforward (CIFF), as it requires no extra DACs in the modulator for feedback and ELD compensation and the best noise suppression in the succeeding integrators [1]. It also reduces the output swing of the first integrator, which can relax the linearity requirement of the first opamp in the LF. However, when compared with the CIFB architecture, the CIFF (cascade of integrator feedforward) requires an extra low-pass filter to alleviate the high STF peaking. The modulator realizes a fourth-order LF with three opamps. One of the opamps implements a single amplifier biquad (SAB) integrator to obtain a second-order transfer function which reduces the power and the phase delay of the LF [19]. The SAB integrator also introduces a notch in the NTF to improve the SQNR, which is effective in low OSR CT DSM designs.

The CT DSM employs preliminary sampling and quantization (PSQ) to implement additional quantization from the QTZ (quantization) backend, which runs at 2 GHz with six-bit resolution and utilizes almost 90% of the clock period. The QTZ

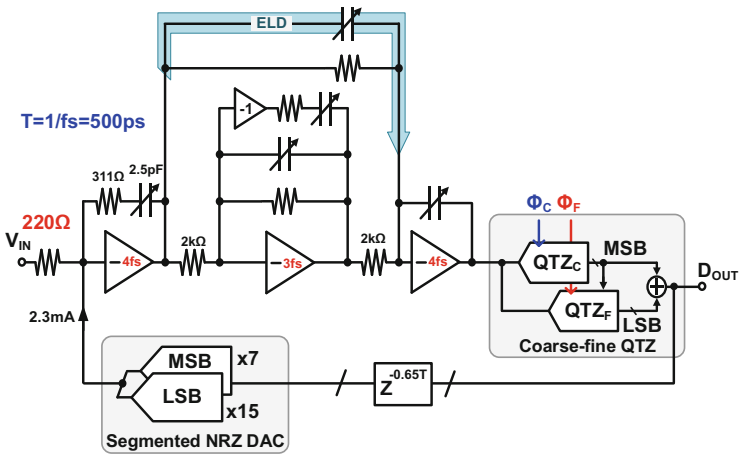

Fig. 7 The block diagram of the fourth-order CT ΔΣ modulator with the coarse-fine QTZ

of the modulator consists of a three-bit two-step coarse QTZ and a four-bit SAR fine QTZ with one-bit error correction range. In order to avoid the extra power and latency introduced by the ELD DAC, we adopt a feedforward scheme. Figure 7 highlights the ELD compensation path, which includes the first and last integrators. The LF realizes the constant term in the ELD compensation path, equivalently acting as an active adder in the ELD compensation scheme [2]. Such ELD realization requires sufficiently high impulse response speed in the modulator, while inadequate speed leads to out-of-band peaking in the frequency domain and even instability [20]. Here, we design the unity-gain bandwidth (UGBW) of the first and last opamps to be higher than the second with $4F_S$, with the ELD coefficient also over-designed, which ensures stability with high impulse response speed.

The three-bit digital tuning capacitors compensate the process variation of the RC integrator, covering ±25% time constant variation. We adopted the nonreturn-to-zero (NRZ) current-steering DAC and segmented structure [21] to reduce the clock jitter sensitivity [16] and the power as well as the area of the feedback DAC, respectively. The calibration of the DAC mismatch between the segment and the unit element occurs in the digital domain [22]. It involves three steps [19]: first, the evaluation of the DAC unit cell mismatch error in an offline procedure; second, the freezing and digital storage of the evaluated DAC error in the lookup table (LUT); and finally, a summation in the digital domain that corrects the output with the evaluated DAC error stored in the LUT. Based on the SNDR and SFDR targets, 13b final output codes are necessary to fulfill the accuracy. The estimated total power and area of the calibration, including memory, are ~1.4 mW and ~0.008 mm^2 in the adopted technology node, respectively. Under the temperature variation with a long channel device, as both the threshold and current factor mismatches only have a weak dependency on the temperature [22], the temperature-originated mismatch variation results from the g_m/I_d, where g_m and I_d are the transconductance and drain current of the MOSFET in the unit current cell, respectively. Simulation results based on the setup and sizing of this design show that such variation leads to a one sigma mismatch of ~0.05% from −20 to 80 °C after calibration at 27 °C, still within the target requirement.

The noise requirement determines the value of the input resistor (R1), which simultaneously decides the consumed current of the main DAC and the capacitance load of the first integrator, thus implying that the value of R1 induces a trade-off between the noise and power of the DAC as well as the opamp in the first integrator. Here, the target SNR is ~77 dB where the SQNR has close to a 10 dB margin. Based on such goal, the R and C values are 220 Ω and 2.5 pF, respectively, for the first integrator. Thus, the C_{DAC} dissipated ~2.3 mA.

3.1 Preliminary Sampling and Quantization (PSQ)

A moderate OSR with the number of quantization in the backend QTZ implies a limitation in the swing variation of the QTZ input signal. Therefore, it is possible to resolve several more coarse bits during such period when we can still cover the error

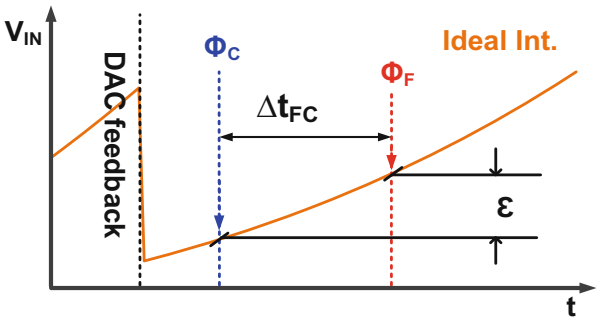

Fig. 8 The sample timing of the coarse-fine QTZ with the PSQ technique

in the fine quantization. Under this circumstance, we can extend the conversion time of the QTZ while simultaneously keeping a reasonable ELD coefficient for the energy-efficient target. Figure 8 plots the QTZ input and the PSQ coarse-fine sample timing. The coarse QTZ samples and quantizes at the time between the fine QTZ sampling and the DAC feedback instant to obtain extra quantization bits. There is a time difference Δt_{FC} between the coarse and the fine QTZ sampling instants, which leads to a sampling error (ε_{SAM}). In order to alleviate it, we should place the coarse sampling instant as close as possible to the fine, which implies an available short time for the coarse QTZ. Therefore, there is a trade-off between the amount of ε_{SAM} and the extra quantization obtained in the coarse QTZ. Apart from Δt_{FC}, the modulator OBG, the LF frequency response, the input variation, and the resolution of the QTZ all affect the ε_{SAM}. We discuss its correction and other design considerations next.

Considerations about the fine sampling instant in the PSQ technique are similar to others in conventional techniques. As the CIFF architecture realizes the ELD compensation in here, the trade-off among the fine QTZ conversation time, the stability, and the power consumption of the LF bind the fine sampling instant. Figure 9 illustrates the relation between the SQNR of the modulator and the opamp bandwidth in the LF, with different choices of the ELD coefficient, and it indicates the stability condition. Furthermore, since the fine QTZ has to cover the sampling error, we also need to consider its correction range. For instance, when the ELD coefficient is $0.4T_s$, the LF requires OPAMPs with $2F_s$ UGBW in order to keep the modulator stable. With close to ~80 ps one SAR cycle and F_s of 2 GHz in the current design, the $0.4T_s$ ELD only allows 2b conversion in the fine SAR QTZ, implying that we must resolve the remaining four bits during the coarse QTZ. Under this condition, the fine QTZ only can provide a small correction range for the sampling error that eventually limits the coarse sampling instant location and reduces the robustness of the PSQ. On the other hand, with a $0.8T_s$ ELD coefficient, a power-hungry-wide bandwidth opamp is necessary that obviously is not a good choice for an energy-efficient target. In the last case with $0.65T_s$ ELD, the modulator allows four bits fine QTZ with 1b error correction, covering a 175 mV error range.

Figure 10 displays the relation between the sampling error and the Δt_{CF}. We can observe that a shorter Δt_{FC} leads to a smaller sample error but with less available

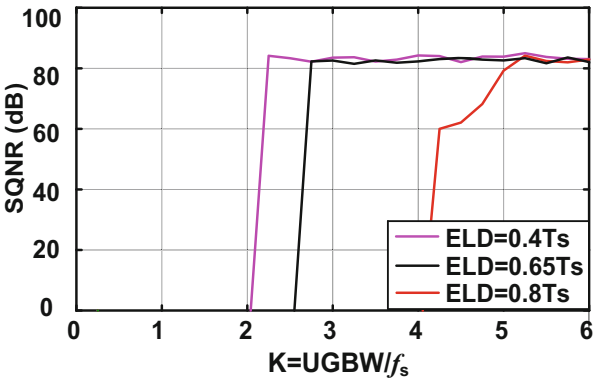

Fig. 9 Peak SQNR versus the bandwidth of the opamp with different delays for the ELD compensation in the LF

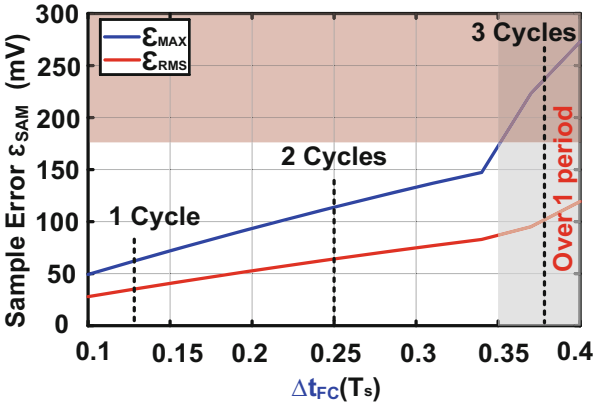

Fig. 10 The RMS (root mean square) (ε_{rms}) and max (ε_{max}) sample error versus the difference Δt_{fc} and the time between the coarse and fine sample

time for the coarse quantization. When $\Delta t_{fc} = 0.125T_S$, it has a small sampling error but only allows one SAR cycle conversion (~80 ps) in the coarse ADC. With only one cycle available but 3b quantization, the only possible architecture to achieve it is the flash that requires seven comparators with offset calibrations and a ladder with the static current. Consequently, the QTZ will occupy a large area, limiting the modulator speed. On the other hand, with a two-cycle available time, we can adopt a subranging architecture to save power and calibration overhead from the pure flash architecture. In the three-cycle case, not only is the timing over $1T_s$, but also the sampling error is over the possible correction range. According to all the abovementioned considerations, we picked here a $0.65T_s$ ELD with Δt_{FC} of 0.25. In wireless communication systems, both the conventional and the PSQ QTZ can saturate with the large out-of-band (OB) blocker under the same STF. However, the PSQ induces one more concern from the sampling error. The sampling error (rms value) exceeds the correction range of the fine stage with >300 MHz and 0 dBFs blocker signal. Yet, with a simple first-order loop pass (LP) filter, the QTZ maintains the stability within all frequencies (Fig. 11). The LP filter limits the blocker signal's amplitude at high frequency, ensuring that the sampling error is within the dedicated

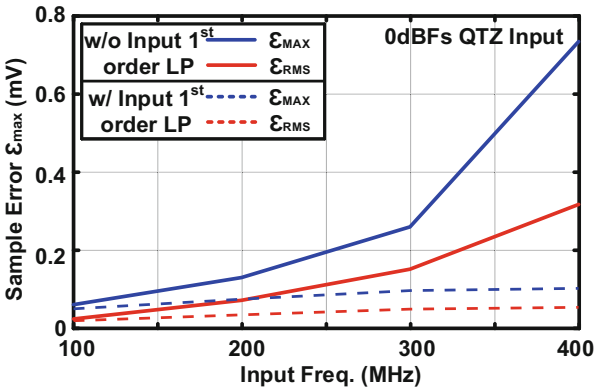

Fig. 11 Sample error versus the input signal frequency with/without first-order low-pass filter

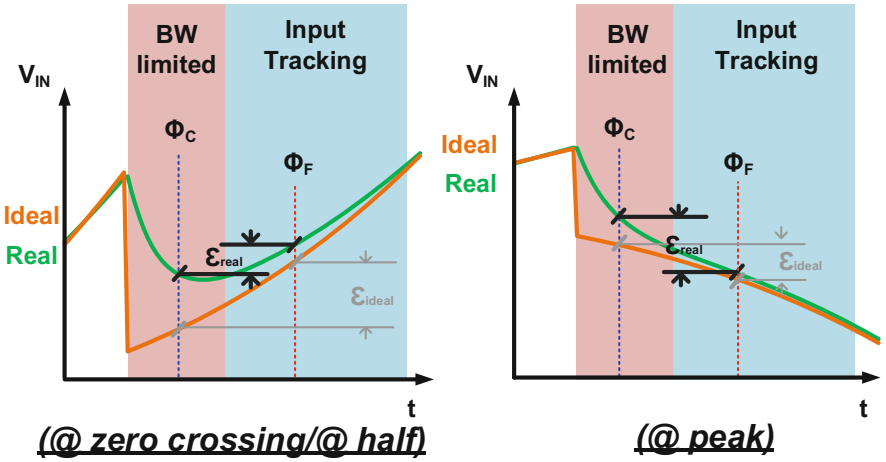

Fig. 12 The output of the LF with ideal and real integrator in the zero crossing and half and peak of the sine wave, respectively

correction range of the fine quantizer. Therefore, to tolerate the OB blocker, the overhead is an LP filter that is often available from the ADC driver.

In the CIFF DSM of Fig. 7, the feedforward path in the LF compensates the ELD. During the DAC feedback, the LF experiences a step response-like input. Restricted by the finite opamp bandwidth in the LF, the output deviates from its ideal value but eventually converges when the response becomes moderate during input tracking. From Fig. 12, when compared with the ideal case, the response of the LF in the CT DSM consists of two parts. The first is the BW limited region, where the output of the LF is mainly dependent on the step response ability of the LF, thus leading to a difference $\varepsilon_{\mathrm{SAM}}$ between the ideal and the real responses. The second is the input track, where the output is mainly dependent on the transfer function of the LF. In the BW limited region, the sampling error $\varepsilon_{\mathrm{SAM}}$ of the LF with $0.25T_{\mathrm{s}}$ Δt_{fc} becomes

$$\varepsilon \propto D_{\text{out}}\left(1-z^{-1}\right)\left(e^{-t/\tau}-e^{-(t+0.25T_s)/\tau}\right), \tag{2}$$

where $D_{\text{out}}(1-z^{-1})$ represents the difference between two sequence output codes. In the CIFF topology, the $D_{\text{out}}(1-Z^{-1})$ through the ELD compensation path directly affects the output of the LF, which is similar to the SC integrator. Therefore, the second part of Eq. (1) is the difference between two instants under the SC response, where τ is the time constant of the LF that is inversely proportional to the bandwidth of the opamp in the LF. Finally, Eq. (1) indicates the total difference between two instants of the LF output, which is the sampling error in the proposed PSQ technique.

Furthermore, the slope and the polarity of the input signal also affect the sampling error. Next, we use a sinusoidal input as an example to show their influence. The response of the LF leads to different ε_{SAM} when the input is at the peak and zero crossing. As Fig. 12 shows, the response polarity reverses at zero-crossing between the BW limited and the input-tracking regions. Then, the ε_{SAM} caused by the input variation and the LF finite response counteract with each other as indicated by the equation below:

$$\varepsilon_{\text{SAM@cross}} \propto \left|\varepsilon_{\text{input}}\right| - \left|D_{\text{out}}\left(1-z^{-1}\right)\left(e^{-t/\tau}-e^{-(t+0.25T_s)/\tau}\right)\right|, \tag{3}$$

where we subtract the error originated by the input variation ($\varepsilon_{\text{input}}$) from the LF response. When compared with the ideal integrator, the real LF experiences a smaller ε_{SAM} under this condition. We can also confirm this trend through the behavioral simulation results in Fig. 13. As the opamp bandwidth is proportional to τ, we plot the sampling error versus the bandwidth which generalizes the required opamp bandwidth consideration. From there, the $\varepsilon_{\text{SAM@cross}}$ increases with the opamp bandwidth and becomes closer to the ideal integrator condition. The $\varepsilon_{\text{SAM@cross}}$ almost saturates when the UGBW of the opamp is close to $15F_s$, but the minimum $\varepsilon_{\text{SAM@cross}}$ appears when that UGBW is ~3–4F_s. Figure 13 also shows the sampling error of the intermediate cases when the input of the QTZ is close to the one-fourth or

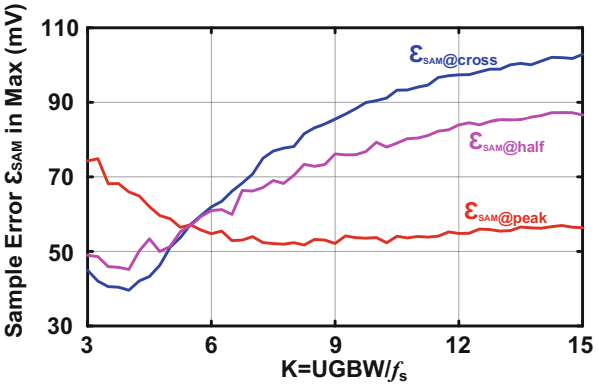

Fig. 13 The maximum sample error versus the bandwidth of the opamp in the zero crossing and half and peak of the sine wave, respectively

three-fourths location of the sine wave ($\varepsilon_{\mathrm{SAM@half}}$). The zero-crossing and peak conditions bind the originated sampling error. Indeed, the signal behavior of the half values case is similar to the zero-crossing (Fig. 12), but with a different amount of error induced from the input-dependent part ($\varepsilon_{\mathrm{input}}$).

On the other hand, still in Fig. 12, the polarity of the response is the same between the BW limited and the input-tracking region at the peak. Then, the $\varepsilon_{\mathrm{SAM}}$ caused by the input variation and the LF finite response accumulate, which we can express by

$$\varepsilon_{\mathrm{SAM@peak}} \propto |\varepsilon_{\mathrm{input}}| + |D_{\mathrm{out}}\left(1 - z^{-1}\right)\left(e^{-t/\tau} - e^{-(t+0.25T_s)/\tau}\right)|, \tag{4}$$

where the $\varepsilon_{\mathrm{input}}$ adds to the LF response error. When compared with the ideal integrator, the real LF experiences a larger $\varepsilon_{\mathrm{SAM@peak}}$ under this condition. While it is similar to the zero-crossing condition, as the bandwidth of the opamp increases, the $\varepsilon_{\mathrm{SAM@peak}}$ also approaches the ideal integrator's response, as illustrated in Fig. 11. The $\varepsilon_{\mathrm{SAM@peak}}$ is at its minimum value when the UGBW of the opamp is $>6F_{\mathrm{s}}$. Based on the above analysis, since $\varepsilon_{\mathrm{SAM@cross}}$ and $\varepsilon_{\mathrm{SAM@peak}}$ have different characteristics versus the integrator bandwidth, we need to consider both errors. In the current design, we choose a $4F_{\mathrm{s}}$ UGBW to balance the $\varepsilon_{\mathrm{SAM}}$ and opamp power with a margin for stability.

3.2 Measurement Results

Figure 14 illustrates the die photo of the CT DSM, fabricated in 28 nm CMOS and occupying an active area of 0.19 mm^2. The power supplies of the QTZ and the NRZ DAC are 1.1 V and 1.5 V, respectively, assuming low noise considerations. The other parts are working under a 1 V supply. The sampling frequency of the modulator is 2 GHz with 10 OSR (oversampling ratio). We implemented the $0.65T_{\mathrm{s}}$ ELD and $0.25T_{\mathrm{s}}$ through the inverters' delay, which varies under PVT. Here, for best speed performance, we only tune the fine sampling instant. The bandwidth is 100 MHz. Figure 15 shows the output spectrum of the modulator with a -2 dBFS, $1.4V_{\mathrm{pp}}$ single-tone signal at ~18 MHz input frequency. The SNDR, SNR, and spurious-free dynamic range (SFDR) are 72.6 dB, 73.2 dB, and 83.6 dB, respectively, after the DAC mismatch calibration [23]. The 80 dB/decade spectral slope validates the fourth-order noise shaping realized by the SAB and two conventional integrators. The total power consumption is 16.3 mW composed by 4.4 mW and 14.3 mW from the analog and digital circuits, respectively. The analog part comprises the opamps, DAC, and QTZ, and the digital part includes the clock generator, the logic buffer, and the control circuits. The first opamp consumes the largest power due to its high thermal noise requirement with a heavy load. While the second opamp should maintain enough bandwidth for the notch of the NTF that causes influence on the SQNR of the low OSR design, it together with the last opamp has relatively smaller power benefiting from their smaller load. The power

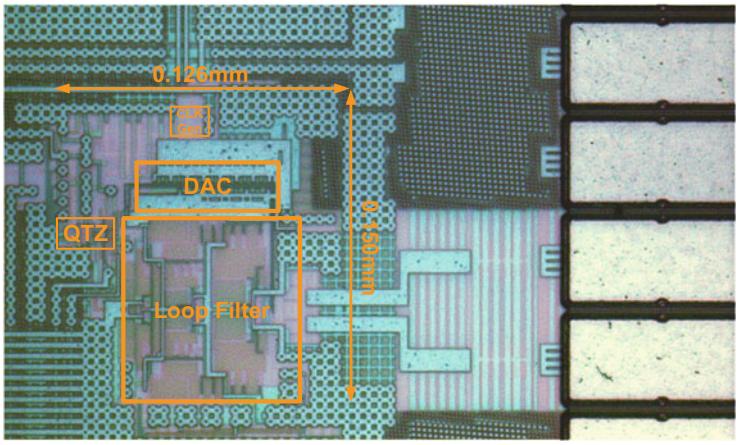

Fig. 14 Die photo

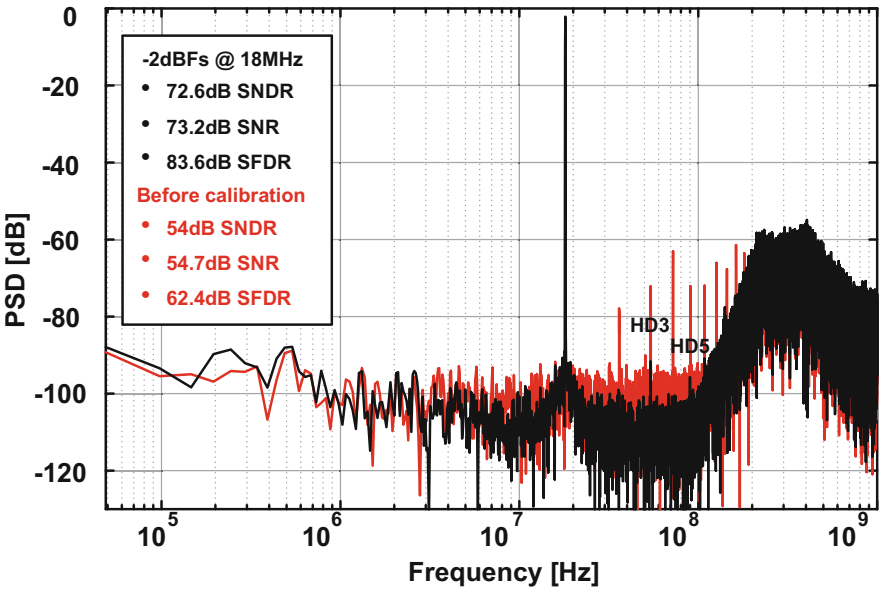

Fig. 15 Single-tone output spectrum

consumption of the 7b 2GS/s coarse-fine QTZ is 1.4 mW, only 8.6% of the total, benefiting from the PSQ technique-based two-step QTZ. The SAR directly uses the supply and ground as references; therefore, we did not adopt any reference buffer, and we include its power in the breakdown of the QTZ power. Table 2 summarizes the measured performance. The modulator achieves a peak SNDR of 72.6 dB and a DR of 76.2 dB, resulting in an excellent Schreier FoM 170.5 dB (SNDR) or 174.2 dB (DR), and a Walden FoM 23.4 fJ/conversion step.

Table 2 Key performance summary

	This work
Area (mm^2)	0.019
Technology (nm)	28
OSR	10
Fs (GHz)	2
Bandwidth (MHz)	100
Power (mW)	16.3
Peak SNDR (dB)	72.6
DR (dB)	76.3
FOMSch/SNDR (dB)	170.5
FOMSch/DR (dB)	174.2
FoMWa (fJ/conv.step)	23.4
STF peak	Yes(11.7dB)

4 A 40 MHz Bandwidth Noise-Shaping Pipeline SAR ADC with 0-N MASH Structure

Figures 16a, b present the architecture of the proposed energy-efficient SAR-assisted NS pipeline ADC and its corresponding signal flow diagram, respectively. The main ADC comprises the first-stage SAR ADC (6b), the residue amplifier, and the second-stage SAR ADC (5b). We inserted one-bit redundancy between the two stages to tolerate the conversion error from the first stage. The ADC is partially interleaved in the first stage, where a coarse SAR ADC performs the conversion and two fine DACs of Ch-1/Ch-2 DAC generate the residue voltage alternately. Subsequently, the circuit transfers that residue voltage to the residue amplifier for residue amplification. The residue amplifier adopts an open-loop dynamic amplifier architecture for low power considerations. Similar to [3], we extract the full resolution residue voltage of the second-stage SAR ADC after the end of the conversion. Then, the circuit feeds back the residue voltage to the residue amplifier, adding to the input of the second stage in the next sampling phase. Consequently, we will have the EF NS completed, where the zero of the NTF relates to the EF residue gain of α provided by the dynamic amplifier. However, the dynamic amplifier is more sensitive under PVT variation than the close-loop residue amplifier in [3], leading to the α variation and a degraded NTF. Thus, we add an extra FF path in the second stage, which enhances the NTF and compensates for the NS effect deterioration due to the gain variation in

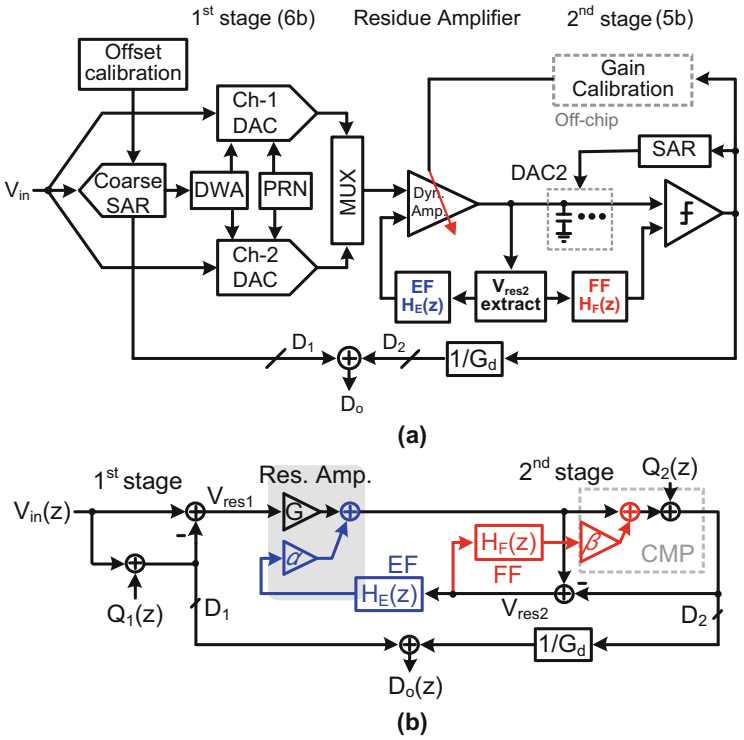

Fig. 16 (**a**) Proposed energy-efficient SAR-assisted NS pipeline ADC architecture and (**b**) corresponding signal flow diagram

the residue amplifier, with the pole of NTF related to the FF residue gain of β. Consequently, the transfer function of the ADC with the EF-FF NS structure becomes

$$D_{\mathrm{o}}(z) = V_{\mathrm{in}}(z) + \left(1 - \frac{G}{G_{\mathrm{d}}}\right) Q_1(z) + \frac{1 - \alpha H_{\mathrm{E}}(z)}{1 + \beta H_{\mathrm{F}}(z)} \cdot \frac{Q_2(z)}{G_{\mathrm{d}}}. \tag{5}$$

There are several design considerations about the NTF in Eq. (3), elaborated in the following section.

We introduce two calibrations in this case, including the gain calibration for the dynamic amplifier and the proposed interstage offset calibration. Moreover, the DWA (data-weighted averaging) technique [24] handles the DAC mismatch. The DWA and the interstage offset calibration operate in the background with their hardware completely integrated on-chip. The gain calibration includes the on-chip PRN generator and the off-chip gain calibration logic (least mean square algorithm), both detailed later.

4.1 SAR-Assisted NS Pipeline ADC

To save power, we adopted a dynamic amplifier [24] in the residue amplifier replacing the conventional static counterpart (Fig. 17). An extra input pair added to the dynamic amplifier realizes the voltage summation of the EF and the first-stage residue with dynamic power only. The transistor sizing ratio between the input and the EF residue pairs set to G: α (unit-gain implemented by $\alpha = 1$) allows a first-order NS in the ADC with the filter implemented as the unit delay of $H_E(z) = z^{-1}$. The separated bias currents of the two paths are I_{b1} and I'_{b1}, with the ratio also set as G: α for a better gain ratio accuracy. Figure 17 also illustrates the operating sequence of the dynamic amplifier.

Although the EF residue summation accomplished through the extra input pair of the dynamic amplifier exhibits good power efficiency, the gain ratio is sensitive to the nonidealities, including the input common-mode, PVT, and mismatch variations. Here, the first-stage SAR ADC determines the input common mode of the signal pair of the dynamic amplifier, while the adopted Vcm-based switching method [25] secures a stable common mode. However, the input common mode of the EF pair defined by the output common mode of the dynamic amplifier is sensitive to the PVT and mismatch variation. According to the simulation result, the output of the dynamic amplifier common-mode voltage has a maximum variation of 50 mV, which alters α by 3%.

Due to the open-loop structure, the absolute values of G and α vary greatly over PVT, but their ratio is less sensitive with the same type of transistors both in the input and the EF pairs. In Fig. 18a, we plot a 3000-run Monte Carlo simulation with the process corner variation showing that the maximum variation of the gain ratio between G and α is within ±0.5% when they are 8 and 1, respectively, while we

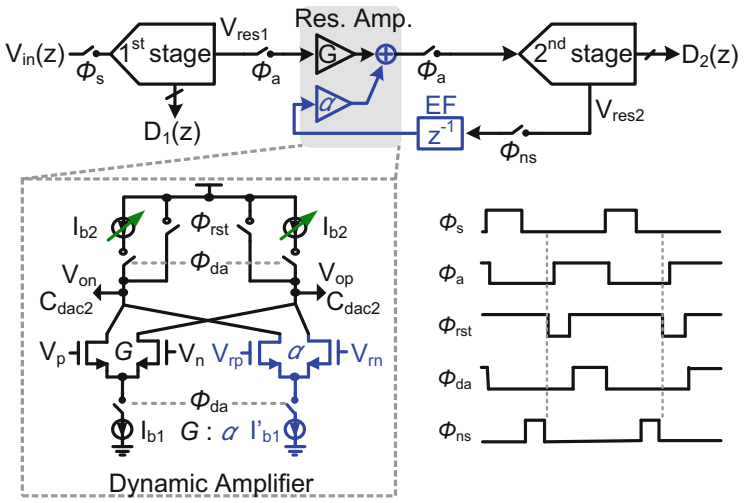

Fig. 17 Dynamic amplifier-based residue amplifier realizing EF NS and its operating sequence

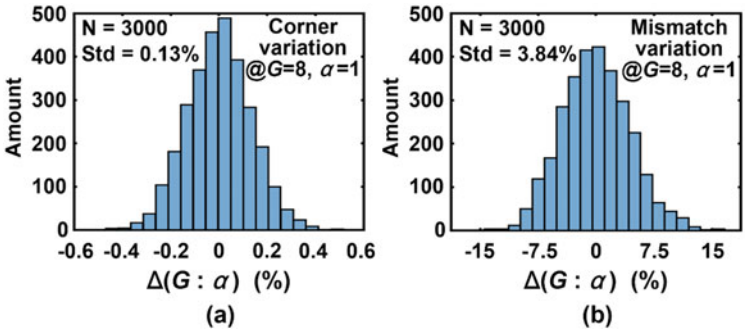

Fig. 18 Monte Carlo simulation (3000 runs) of the variation of G: α with (**a**) process corner and (**b**) mismatch variation effect

ensure the accuracy of G by background calibration [26] through tuning the current source of I_{b2}, with the proportional adjustment of α simultaneously, thus maintaining a stable ratio regarding G. Unlike the PVT variation, the mismatch affects the values of G and α independently, altering their gain ratio. Figure 18b shows the gain ratio variation under mismatch with a 3000-run Monte Carlo simulation, where the G:α has a maximum variation of $\pm 11.5\%$.

To summarize, considering all the above nonidealities and the worst condition where G and α have an opposite 3σ variation, the gain ratio between G and α experiences a maximum variation of $\pm 27\%$. Therefore, with G well calibrated, α can, in the worst case, have an error within $\pm 27\%$ departed from its ideal value. Figure 19 displays the simulated SQNR of the ADC with the variation of α, based on a ten-bit SAR-assisted pipeline structure with first-order NS and $OSR = 7.5$. The SQNR drops about 4 dB when α varies $\pm 27\%$. To avoid an extra calibration for α, we present an enhanced NS structure with a mild hardware cost, compensating for the SQNR drop due to the variation of α.

In Fig. 20, we add an extra residue FF path in the second stage. In this configuration, we further filtered the sampled V_{res2} with $H_F(z)$ and summed it with the second-stage DAC's output voltage in the comparator through an additional input pair. The comparator provides the FF residue gain of β through the ratio-sized input transistors [27]. For simplicity, we can just implement the $H_F(z)$ with one cycle delay, where $H_F(z) = z^{-1}$. Therefore, according to Eq. (3), the noise transfer function of the ADC with the EF-FF NS structure becomes

$$\mathrm{NTF}(z) = \frac{1 - \alpha z^{-1}}{1 + \beta z^{-1}}. \tag{6}$$

Ideally, with β set to 1, the additional pole leads to an extra 6 dB noise attenuation at a low frequency [28], compensating for the SQNR drop due to the α variation. However, the pole must be inside the unit circle for stability, thereby requiring $\beta < 1$.

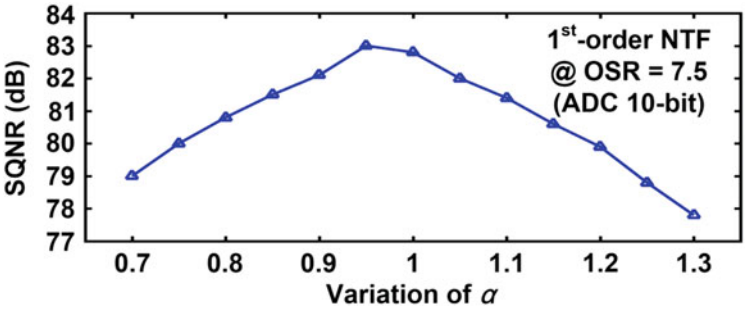

Fig. 19 Simulated SQNR versus α in a ten-bit ADC structure with first-order NS ($\alpha = 1$) and OSR = 7.5, where $G = 8$ is ideal

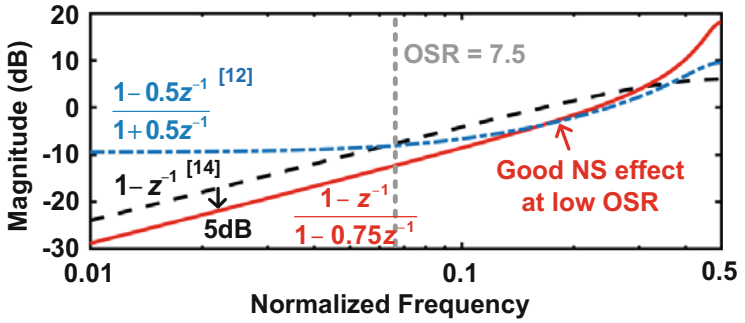

Fig. 20 Bode diagram of the NTF in the current design and its comparison

After accounting for the 3σ variation of α ($\pm 27\%$) and the maximum 4 dB SQNR, we set β as 0.75.

Figure 21 plots the bode diagram of the NTF of the EF-FF NS structure. With the pole at 0.75, it still obtains an additional 5 dB noise suppression at the low frequency when compared with the standard first-order NTF. Meanwhile, the NTF owns a low magnitude at high frequency, leading to a good NS effect with a small OSR. As a result, the enhanced NTF enables both high resolution and wide BW performance. On the other hand, according to the 3000-run Monte Carlo simulation results of the second-stage comparator, the 3σ variation of β is $\pm 20\%$, which implies that the pole moves to a maximum of 0.9 and the system potentially becomes unstable. While such large variation only happens in the extreme case, the charge sharing between the feedforward capacitor and the parasitic capacitor, which attenuates the residue voltage to move the pole away from the unit circle, also helps to stabilize the ADC. Thus, according to the five measured samples and the post-layout Monte Carlo simulation result, the ADC is stable within a 3σ case. Although such variation can alter the pole's location in the NTF, it only slightly weakens the FF NS effect. Based on a ten-bit SAR-assisted NS pipeline ADC model, Fig. 21 illustrates the SQNR distribution of a 50-run Monte Carlo simulation under different NS realizations

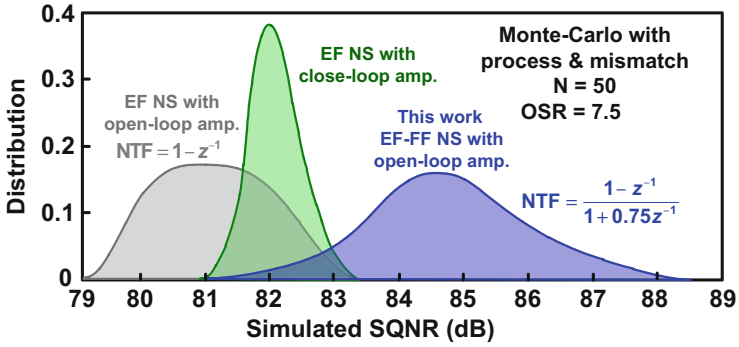

Fig. 21 Simulated SQNR distribution under different NS configurations with process corner and mismatch variations

considering both the variation of α and β, with the interstage gain of G and offset calibrated. Due to the relatively accurate gain in the close-loop residue amplifier, its EF NS structure experiences the smallest SQNR variation. At the same time, the ADC with an open-loop dynamic amplifier has a decentralized SQNR distribution under corner and mismatch variations. Fortunately, we can fully compensate the SQNR drop with the proposed EF-FF NS, saving an extra calibration for the gain of the EF path.

To overcome the speed limitation of the SAR-assisted NS pipeline ADC in [29], mainly confined by the single-channel first stage, we introduce a duplicated channel of Ch-2 in the first stage to obtaining the partial interleaving operation [29] (Fig. 22a). When Ch-1 performs the conversion at the n-th cycle, Ch-2 samples the input simultaneously. After the conversion, we employ the residue voltage in Ch-1 in the residue amplifier for amplification; meanwhile, Ch-2 can still track the input. In the $(n + 1)$-th cycle, Ch-1 and Ch-2 alter their roles, whose operation propagates down in the following samples. Like this, we save the sampling operation from the critical path of the entire ADC conversion, thereby significantly speeding up the ADC. Furthermore, since the sampling time now can be as long as the first-stage conversion plus the amplification time, the tracking time of the sampler widens, greatly relaxing the design of the sample-and-hold circuit.

We add an extra coarse SAR ADC to further improve the conversion speed, with the timing diagram illustrated in Fig. 22b. With the coarse SAR, we can simplify the two-channel SAR ADCs to two-channel DACs. The coarse-SAR quantizes six-bit MSBs (most significant bits) with its low-resolution DAC, resulting in high conversion speed and low switching power. The circuit transfers the MSB codes to one of the two DACs alternately that generate the full resolution residue voltage. Figure 22b presents the adopted DWA logic to shape the DAC mismatch error in both channel DACs. After the coarse SAR resolves three MSBs, we decoded their binary form into the thermometer code and transferred it to one of the interleaving fine DACs through the DWA logic. Simultaneously, we continuously resolve in the coarse SAR

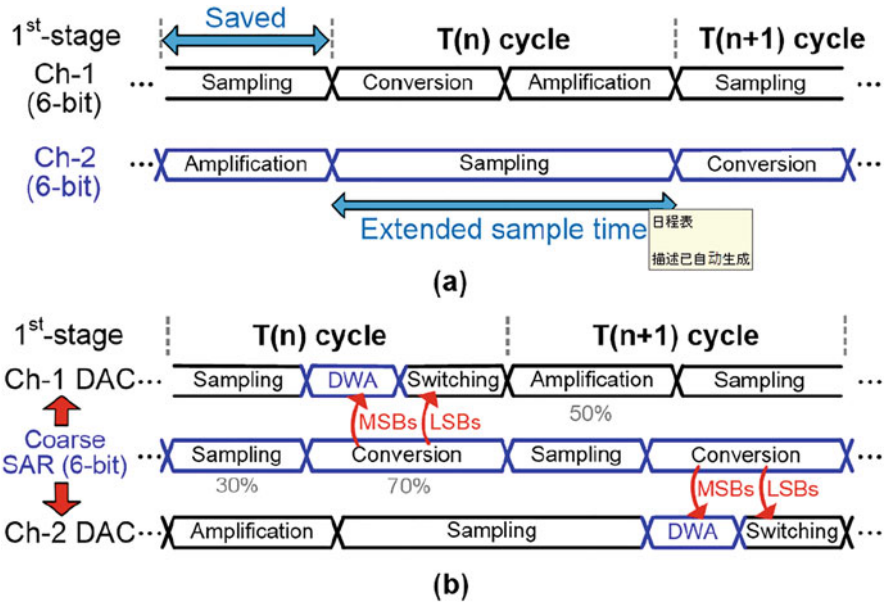

Fig. 22 Timing diagram of the first-stage ADC with (**a**) two-channel interleaving and (**b**) additional coarse SAR-assisted conversion

the remaining three LSBs (least significant bits) of the first stage. Due to the coarse SAR ADC, the DWA operation calls for no extra time slot and thereby does not slow down the ADC.

Figure 23 displays the major nonidealities in the ADC architecture. The n_{sh1}, n_{ra}, n_{cmp1}, and n_{cmp2} are the thermal noise from the first-stage sampling circuit, residue amplifier, and first- and second-stage comparators, respectively. The n_{ef} and n_{ff} are the thermal noise from the EF and FF path, respectively. The e_{mis1} and e_{mis2} are the DAC mismatch errors in the first- and second-stage SAR ADCs, respectively. We denote the input-referred offset voltages of the residue amplifier and first- and second-stage comparators as $v_{os,ra}$, v_{os1}, and v_{os2}, respectively. First, we omit the effect of the offset voltage where $v_{os,ra} = v_{os1} = v_{os2} = 0$. Therefore, when $G_d = G$, the transfer function of the ADC with the noise and mismatch error sources is

$$D_o = V_{in} + n_{sh1} + n_{ra} + e_{mis1} + \frac{1}{G} e_{mis2} + \frac{1}{G} \times \left[z^{-1} \cdot n_{ef} + \frac{3}{4} \mathrm{NTF} \cdot z^{-1} \cdot n_{ff} + \mathrm{NTF} \cdot \left(n_{cmp2} + Q_2 \right) \right]. \quad (7)$$

With the Q_1 and n_{cmp1} fully canceled, thereby they do not appear in Eq. (5). The interstage gain suppresses the n_{ef} and n_{ff}; besides, the NTF further shapes the n_{ff} along with Q_2. Consequently, the additional noises from the EF and FF paths become trivial. On the other hand, the extra input pair in the comparator for the FF

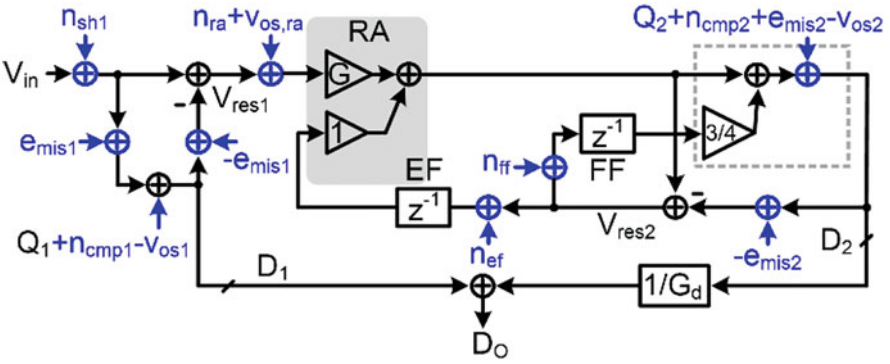

Fig. 23 Major nonidealities in the ADC architecture

path in the second stage worsens the n_{cmp2} and induces an extra 1.7 dB SNR drop of the ADC under the same power budget, while the additional FF NS imposes a 5 dB in-band noise suppression, with n_{cmp2} shaped together with Q_2. As a result, the FF NS still brings net benefit. The sampler in the first stage and the residue amplifier dominate the overall noise performance of the ADC, while the DAC mismatch error in the first stage dominates the linearity performance due to its non-shaped characteristic. Furthermore, we fulfill the noise requirement from the sampler and residue amplifier by budgeting enough sampling capacitance and integration time, respectively. The DWA technique suppresses the DAC mismatch.

Next, we consider the interstage offset in the pipeline structure. When the offset voltage exists in the comparator, the circuit shifts the searching baseline of the SAR ADC with the same offset voltage but with reverse polarity. Therefore, the v_{os1} and v_{os2} from Fig. 23 have negative polarity. The total interstage offset voltage becomes

$$v_{os,in} = v_{os1} + v_{os,ra} - \frac{1}{G} \cdot \frac{1 - z^{-1}}{1 + 3/4z^{-1}} v_{os2}. \tag{8}$$

Due to the unity EF structure, a delayed version of v_{os2} feeds back to the input of the residue amplifier, thus canceling itself out ideally. However, the residual v_{os2} indeed still contributes to v_{os} due to the non-unity gain of the EF residue (as discussed above) while the amount is small. Meanwhile, the v_{os1} and $v_{os,ra}$ are significant under the gain of G and can saturate the second-stage conversion, causing a large error. Hence, we propose a background interstage offset calibration with low timing and hardware overhead (detailed next).

4.2 Measurement Results

Figure 24 presents the chip micrograph of the ADC prototype fabricated in 28 nm CMOS occupying an active area of 0.016 mm^2. The pseudo-random noise generator, DWA, and interstage offset calibration logic account for only 1%, 1.3%, and 1% of the total ADC's area, respectively. The ADC operates at the sampling rate of 600 MHz and achieves a BW up to 40 MHz at an $OSR = 7.5$. Figure 25 depicts the measured 32,768-point FFT spectrum with a 2 MHz and -04dBFS sinusoidal input signal at different calibration configurations. With all calibrations enabled, the prototype reaches a peak SNDR and spurious-free dynamic range (SFDR) of 75.2 dB and 87.1 dB, respectively. The residual DAC mismatches and the nonlinearity from the dynamic amplifier impose the remaining harmonics. The DWA effectively improves the SFDR, and the interstage offset calibration enhances both the SNR and SFDR of the ADC. The high-frequency noise floor looks mild with the DWA enabled (Fig. 25). It is because the DWA shapes the harmonic tones to high frequency and the quantization error floor superposes the high-frequency spectrum and the shaped nonideal spurs. However, the NTF of the ADC remains unchanged. Under a supply voltage of 1 V, the ADC consumes 2.56 mW, leading to a good FoM of 177.1 dB. The digital part consumes most of the power, including the control logic and DAC drivers. The power-efficient dynamic amplifier only accounts for less than 7% of the total power consumption. All the calibrations and DAC mismatch correction, including the pseudo-random noise generator, the DWA logic, and the proposed interstage offset calibration, consume only 0.34 mW (13% of the total ADC power).

Table 3 summarizes the performance of the ADC. It exhibits both high resolution and BW with outstanding FoMs among all the converters listed, revealing the

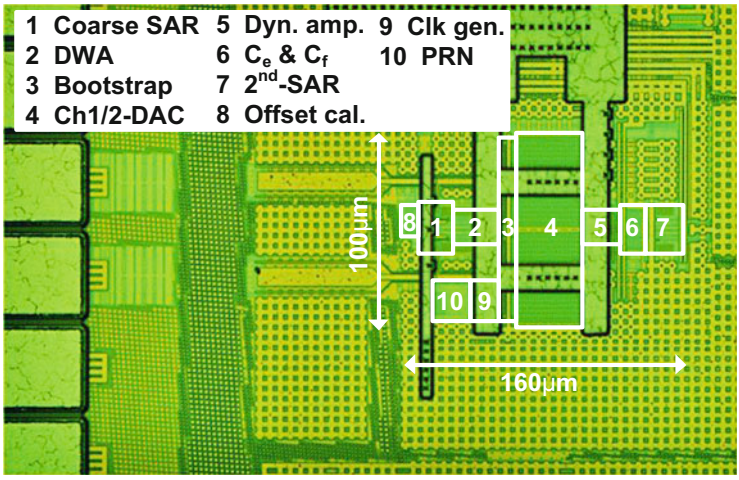

Fig. 24 Die photo

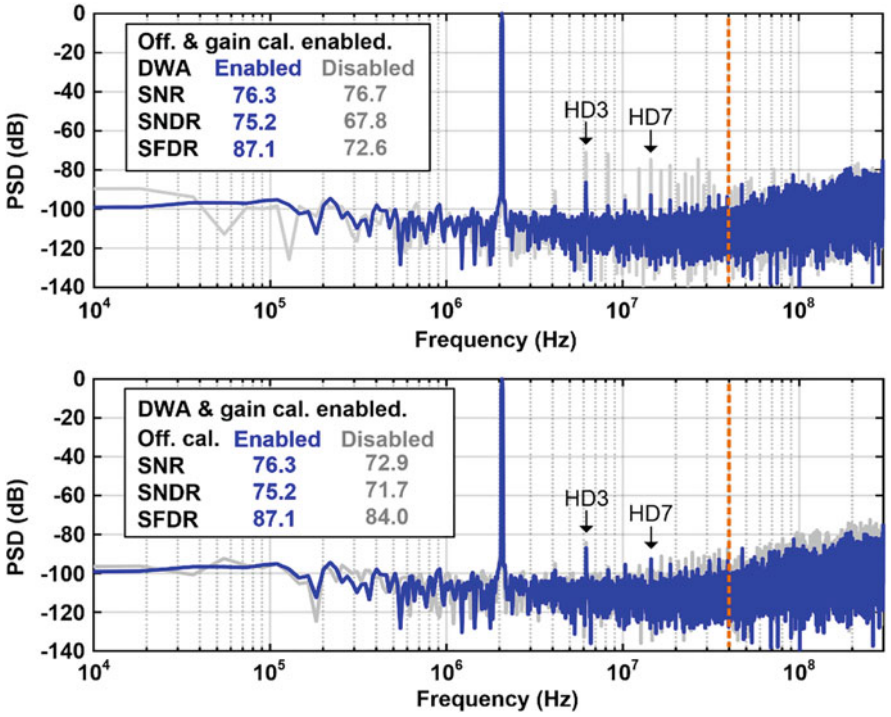

Fig. 25 Measured output spectrum with different configurations at 600 MS/s

Table 3 Key performance summary

	This work
Technology [nm]	28
Architecture	NS pipe-SAR
Fs [MHz]	600
OSR	7.5
BW [MHz]	**40**
SNDR [dB]	**75.2**
SFDR [dB]	87.1
DR [dB]	76.6
Power [mW]	2.56
FoM_W [fJ/step]	6.8
FoM_S [dB]	**177.1**
Area [mm^2]	0.016
Off. Cal.	On-chip

effectiveness of the EF-FF NS structure and the partial interleaving architecture, including the on-chip calibration. The ADC is robust under PVT variation with the background calibrations and additional FF path. Besides, with only two DACs partially interleaved, we can maintain the channel mismatches within a reasonable level through a careful layout.

5 A 25 MHz Bandwidth Gain Error-Tolerant N-0 MASH Noise-Shaping Pipeline SAR ADC

To realize the noise shaping in the first stage, we can consider both EF and CIFF. The EF structure often calls for an amplifier with accurate gain to construct the sharp NTF [26], leading to extra noise and requiring calibration. In this work, we use a fully passive CIFF NS structure in the first stage to implement a stable NTF. Figure 26 illustrates the proposed MASH 2–0 NS-SAR-assisted pipelined ADC with a simplified schematic and timing diagram. We realized the second-order NS-SAR ADC in the first stage based on a passive CIFF filter [30], while the second stage is a pure SAR ADC. The NTF in Eq. (2) of the first stage is $(1–0.5z^{-1})^2$ as two integration capacitors, C_1 and C_2, are equal to the main DAC capacitor. Its operation procedure is the following. Initially, the DAC capacitor samples the input voltage (V_{in}) during Φ_S. Then, the NS-SAR ADC of the first stage converts 6b with the three-input comparator where the ratio of the input pairs (g_c, g_{c1}, and g_{c2}) is 1:1:2. After the sampling and conversion phases, the circuit sums the first stage's residue (V_{res1}) and the voltage on two integration capacitors (V_{int1} and V_{int2}), subsequently amplified by a three-input dynamic amplifier where the ratio among the input pairs is the same as the three-input comparator. Eventually, considering the feedforward path summation, the amplifier and the comparator (equivalently at their inputs) undertake $-E_{q1}$ during the amplification phase Φ_{da}. With $-E_{q1}$ handed over to the second stage, it maintains the noise-shaping ability for the quantization error and comparator noise.

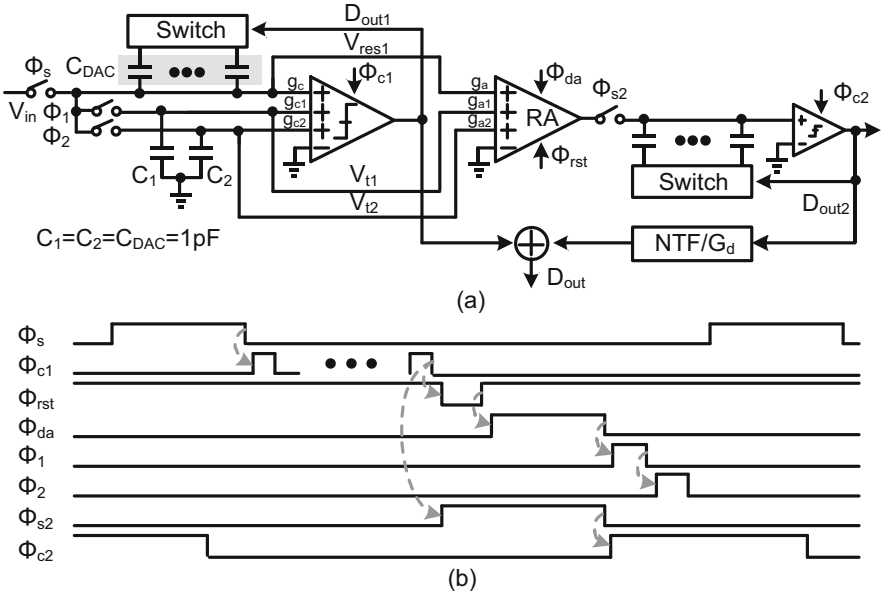

Fig. 26 The CIFF MASH 2–0 SAR-assisted pipeline: (**a**) a simplified schematic and (**b**) timing diagram

After the amplification, V_{res1} on C_{DAC1} charge-shared with two integration capacitors (C_1 and C_2) sequentially during Φ_1 and Φ_2 leads to a second-order passive integration. Simultaneously, the second-stage SAR ADC attains the remaining 6b resolution. After all, the output of the second stage (D_{out2}) passes through the digital reconstruction filter (NTF/G_d) and then sums with the first-stage output (D_{out1}), thus removing the quantization noise in the first stage at the final output (D_{out}).

Figure 27 displays the major sources of nonideality in the proposed MASH 2–0 SAR-assisted pipeline ADC. The n_{DAC} is mainly from the kT/C noise while $n_{0,\Phi1}$, $n_{1,\Phi1}$, and $n_{2,\Phi2}$ are the noises from the two passive integration phases Φ_1 and Φ_2 [30]. The n_{AMP} is the total input-referred noise of the amplifier. E_{q1}, e_{mis1}, and n_{CMP1} are the quantization noise, mismatch error in the capacitance DAC array, and comparator noise of the first stage, respectively, while E_{q2}, e_{mis2}, and n_{CMP2} are the corresponding impairments of the second stage (same as above). The overall transfer function, including these nonidealities, is

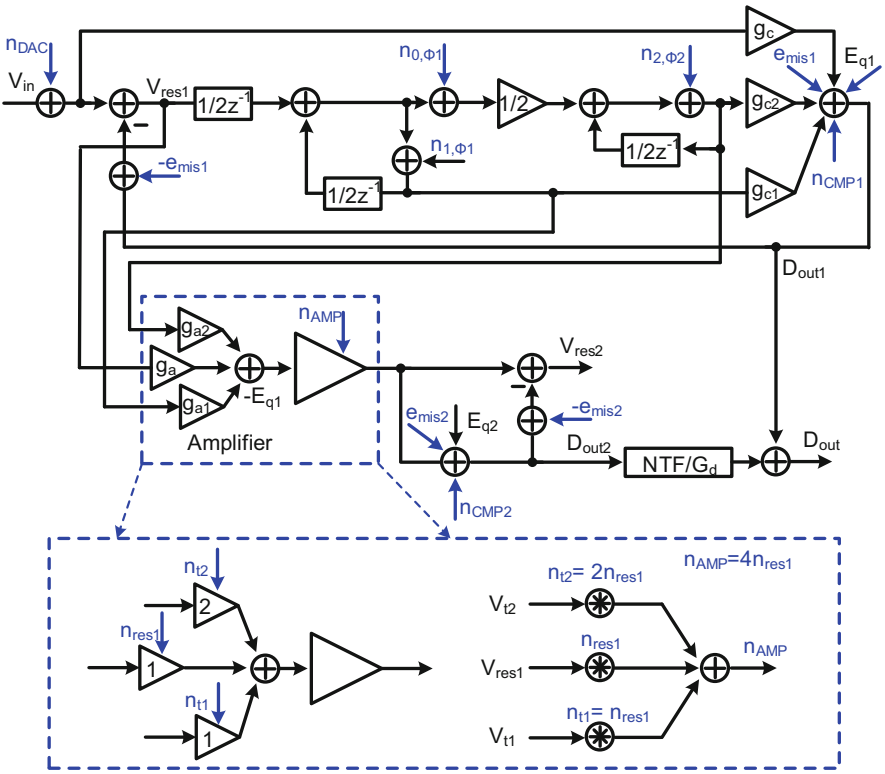

Fig. 27 Noise and mismatch analysis of the MASH 2–0 structure

$$D_{\text{out}} = V_{\text{in}} - e_{\text{mis1}} + n_{\text{DAC}} + n_{0,\Phi1}\left(1 - 1/2z^{-1}\right) + n_{1,\Phi1} + 2n_{2,\Phi2}\left(1 - 1/2z^{-1}\right) \\ \text{NTF} \cdot n_{\text{CMP1}} + \text{NTF} \cdot n_{\text{AMP}} + \frac{\text{NTF}}{G}\left(E_{\text{q2}} + e_{\text{mis2}} + n_{\text{CMP2}}\right) \tag{9}$$

Then, we cannot shape e_{mis1}, n_{DAC}, and $n_{1,\Phi1}$ while $n_{0,\Phi1}$ and $n_{2,\Phi2}$ are first-order shaped. With sufficiently large sampling and integration capacitors, we can well suppress n_{DAC}, $n_{0,\Phi1}$, $n_{1,\Phi1}$, and $n_{2,\Phi2}$, with e_{mis1} addressed by the 4-b DWA in this design (detailed later). The NTF shapes both n_{CMP1} and E_{q1}, while the redundancy between stages can further cover n_{CMP1} and the reconstruction filter (without gain error) cancels E_{q1}. Furthermore, the NTF shapes the E_{q2}, e_{mis2}, and n_{CMP2} while the interstage gain G suppresses them.

We split the amplification into three paths and list their noises individually. The n_{AMP} divides itself into three-input referred noises n_{res1}, n_{t1}, and n_{t2}, which connect to the signal path V_{res1}, V_{t1}, and V_{t2}, respectively. The n_{AMP} is the lump sum of all the above noises. On the other hand, from Eq. (4), the NTF configures all of them as second-order shaped. Nevertheless, the multiple input pairs worsen the noise when compared with a single pair at the same power budget [30]. The total noise increases by 4× because of the two additional added paths. Fortunately, the noise attenuates ~4× due to the NTF with OSR = 8. Its net in-band noise is almost the same as in the case of the one-pair device. Eventually, we ensure an overall small n_{AMP} by budgeting a sufficiently long integration time.

We carefully studied the noise leakage issue in the MASH architecture due to the nonideal first-stage NTF. The ratios of the capacitors (DAC array capacitor and two integration capacitors) and the ratio between the comparator and amplifier input pairs determine the NTF in this work. As we implement the DAC and integration capacitors with the same type of capacitors (MoM), we assume them as well matched in the following analysis with $C_1 = C_2 = C_{\text{DAC}}$. We set $G_{\text{d}} = G_{\text{a}} = 1$ to simplify the analysis and focus on the discussion of the NTF mismatch. We can detail the noise transfer function of the first stage of the MASH SDM as

$$\text{NTF}_1(z) = \frac{\left(1 - 0.5z^{-1}\right)^2}{1 + (0.5g_{\text{c1}} + 0.25g_{\text{c2}} - 1)z^{-1} + (0.25 - 0.25g_{\text{c1}})z^{-2}} \tag{10}$$

where g_{c1} and g_{c2} are the gain ratios of the input pairs of the comparator normalized to g_{c}. Besides, a three-input amplifier constructs the first-stage residue of this MASH?SDM, which implies that we can model the output voltage of the amplifier $V_{\text{amplifier}}$ as

$$V_{\text{amplifier}} = -\text{NTF}_1(z)E_{q1}(z) \times \frac{1 + (0.5g_{a1} + 0.25g_{a2} - 1)z^{-1} + (0.25 - 0.25g_{a1})z^{-2}}{(1 - 0.5z^{-1})^2} \tag{11}$$

where g_{a1} and g_{a2} are the gain ratios of the input pairs of the amplifier normalized to g_a. In the ideal case, where $g_{c1} = g_{a1} = 1$ and $g_{c2} = g_{a2} = 2$, the transfer function of the digital reconstruction filter is

$$\text{NTF}_d(z) = \left(1 - 0.5z^{-1}\right)^2 \tag{12}$$

Then, the complete output of this MASH SDM will be

$$D_{\text{out}}(z) = V_{\text{in}}(z) + \text{NTF}_d(z)E_{q2}(z) + E_{q1}(z)\text{NTF}_1(z) \times \left(1 - \frac{1 + (0.5g_{a1} + 0.25g_{a2} - 1)z^{-1} + (0.25 - 0.25g_{a1})z^{-2}}{(1 - 0.5z^{-1})^2}\text{NTF}_d(z)\right) \tag{13}$$

Here, we cancel completely $E_{q1}(z)$ in the ideal case. Under PVT and mismatch variations, the zeros of the NTF_1 are robust and set by the capacitor ratios, while the pole locations can drift due to the mismatch among g_{c1} and g_{c2}, but they are not crucial in the cancellation process. Besides, the mismatch between g_{a1} and g_{a2} affects the cancellation procedure. Fortunately, the robust NTF_1 can relax their variations. It is noteworthy that the ratio between g_{c1}, g_{c2}, g_{a1}, and g_{a2} are in the first-order set by the width of the same type of transistors, and they therefore are relatively insensitive to PVT variations.

Only the absolute variation of the amplifier gain is a direct cause of the interstage gain error. The variations of g_{a1} and g_{a2} associated with g_a mainly affect the transmission of $-E_{q1}(z)$ to the second stage and therefore potentially cause noise leakage. We implement the ratio among g_a, g_{a1}, and g_{a2} with the same type of transistor in different sizes, and they experience similar variations over PVT. On the other hand, the mismatch, altering the NTF and affecting the gain error tolerance ability, can influence the relative value between g_a, g_{a1}, and g_{a2}, altering the NTF and affecting the gain error tolerance ability. To demonstrate the sensitivity, we performed a behavioral simulation based on the ADC structure. Figure 28 shows the SQNR with g_{c1}, g_{c2}, g_{a1}, and g_{a2} variations. Furthermore, the proposed ADC is more sensitive to the input pair mismatch of the amplifier than the comparator as the perfect cancellation relies on g_{a1} and g_{a2}, which is consistent with Eq. (8). To have a good matching, the inputs of the amplifier are sufficiently large with sizes 16 μm/0.05 μm, 16 μm/0.05 μm, and 32 μm/0.05 μm, respectively. Figure 29 depicts their variations with a 100-run Monte Carlo simulation, and such large size ensures small

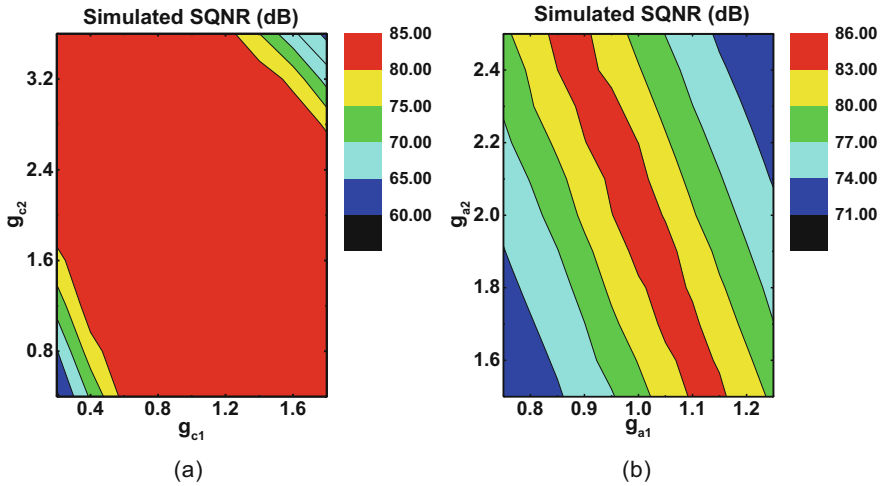

Fig. 28 Simulated SQNR varies with (**a**) extra comparator ratio and (**b**) extra amplifier ratio

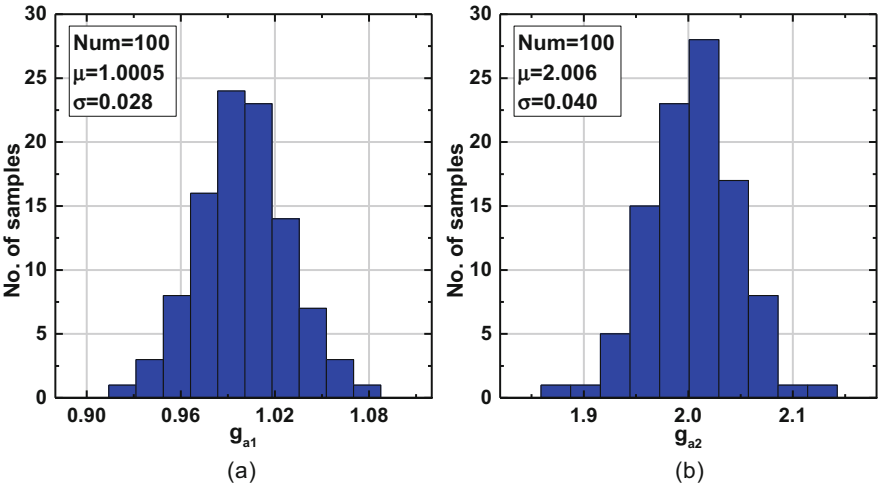

Fig. 29 Monte Carlo simulation results of (**a**) g_{a1} and (**b**) g_{a2}

enough standard variations. The 3σ coefficient variations of g_{a1} and g_{a2} are $\pm 8.4\%$ and $\pm 12\%$, respectively, leading to the worst SQNR of 77 dB. Figure 30 presents a 100-run post-layout Monte Carlo simulation, which illustrates the SQNR variations due to the mismatch of the input pairs of the comparator and the amplifier. The mean and standard deviation values of the SQNR are 80.26 dB and 1.25, respectively, leaving enough margin for an overall 75 dB SNDR target.

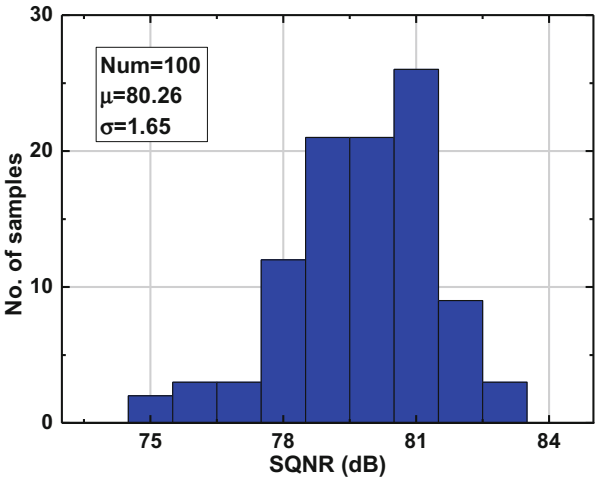

Fig. 30 Post-layout ADC simulation results with multiple-input first-stage comparator and amplifier mismatch

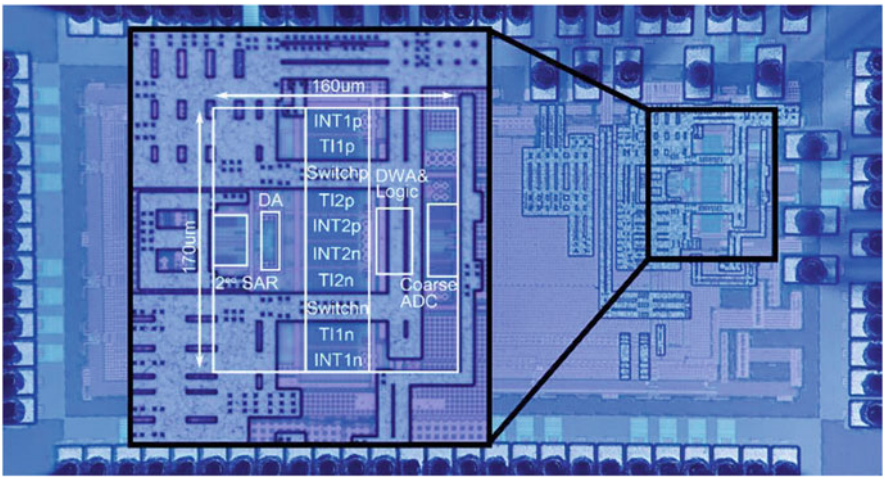

Fig. 31 Die photo

5.1 Measurement Results

Figure 31 presents the fabricated device in 28 nm CMOS, with the ADC occupying an area of 0.027 mm^2. Figure 32 plots the measured ADC's output spectrum with and without DWA. The input frequency is 2.04 MHz with more than nine harmonics included. Consequently, the interstage gain and nonlinearity error shaping ability lead to a peak SFDR and SNDR of 92.1 dB and 75 dB, respectively. To demonstrate the tolerant range, we introduce a wide range of gain errors by adjusting the

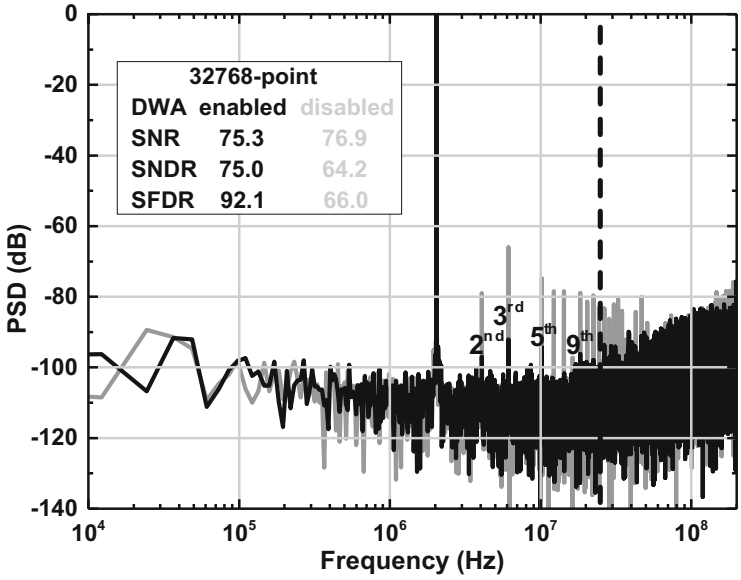

Fig. 32 Measured spectrum

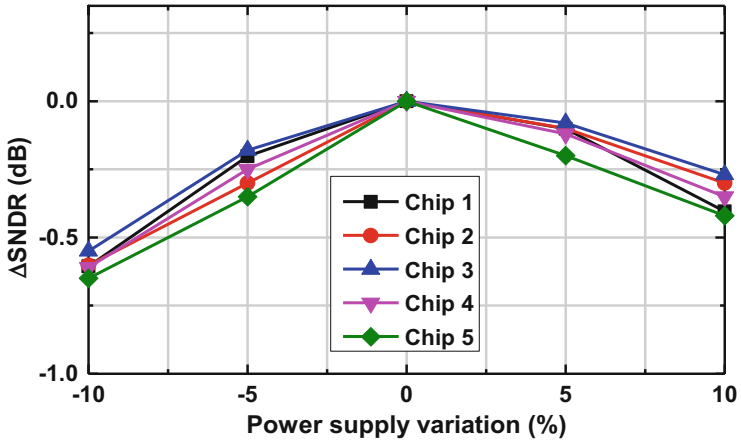

Fig. 33 Measured SNDR variations versus power supply with five chips

reference voltage of the second-stage SAR ADC. We brought off-chip the reference voltage of the second-stage ADC for measurement purposes. We measured five samples and their SNDR variations across ±10% supply voltages that appear in Fig. 33. The largest SNDR drop is 0.65 dB which agrees with the analysis. The

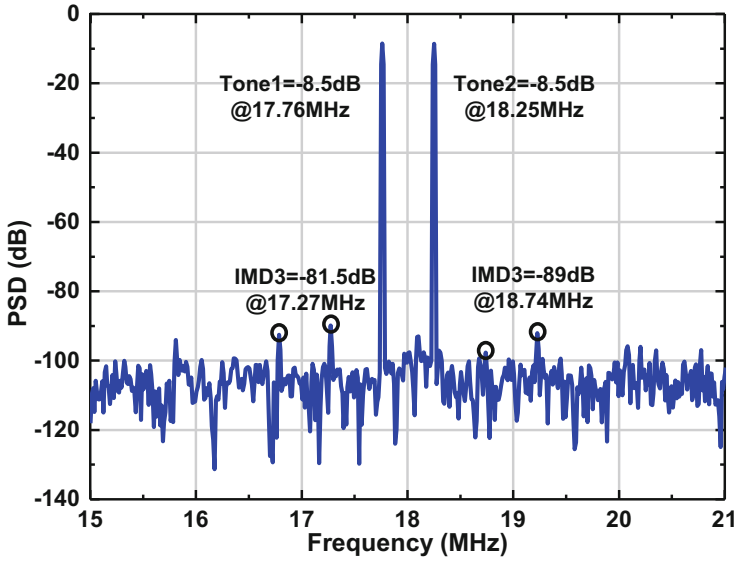

Fig. 34 Two-tone spectrum

two-tone spectrum with −8.5 dBFS appears in Fig. 34 and the IMD3 is −81.5 dB. The prototype ADC runs at 400 MHz and consumes 1.26 mW power. The digital circuits consume the major portion. Table 4 compares the proposed design with the state of the art having similar specifications. Unlike the gain error shaping (GES) [31] scheme, the proposed design can handle positive and negative gain errors with small hardware overhead while still maintaining a relatively high-speed operation. Reference [32] reaches a good energy efficiency without calibration. However, the SNDR is ~4 dB and ~8 dB better with OSR = 8 and OSR = 20, respectively. The prototype avoids off-chip DAC calibration and is within a −16% to +12% gain error tolerable range with OSR = 8. The design exhibits a larger gain error tolerance range with a larger OSR with the SNDR mainly limited by other noises and nonlinearities, which the NTF cannot shape. We obtained a FoM_W and a FoM_S of 5.5 fJ/conv.-step and 178 dB, showing that this design can maintain a good power efficiency with an additional gain error tolerance ability.

Table 4 Key performance summary and comparison

	Gregoire ISSCC2008 [33]	Yoshioka ISSCC2017 [34]	Song JSSC2020 [3]	Hsu JSSC2020 [35]	Song JSSC2021 [36]	Hsu JSSC2020 [31]	Wang JSSC2020 [2]	This work		
Process [nm]	180	28	65	40	28	40	28	28		
Architecture	Pipeline ADC	Pipeline SAR	0–1 MASH	Pipeline SAR	Pipeline NS SAR	Pipeline SAR	Pipeline SAR	2–0 MASH		
Interstage gain error suppression scheme	Closed-loop SAR	Digital amplifier	Closed-loop opamp	Second-order GES	Foreground calibration	Second-order GES + DEF	WACLS	Inherent architecture		
Interstage offset suppression scheme	N/A	Digital amplifier	Foreground calibration	N/A	Background calibration	N/A	Auto zeroing	Code-counting-based background calibration		
DAC mismatch calibration	N/A	N/A	Foreground off-chip calibration	Foreground off-chip calibration	3b DWA	Foreground off-chip calibration	RS	4b DWA		
Supply [V]	1.2	0.7	1.0	1.0	1.0	1.0	1.1	1.0		
Fs [MHz]	20.2	160	200	100	600	100	100	400		
Power [mW]	7.5	1.9	4.5	1.54	2.56	1.38	0.7	1.26		
Area [mm^2]	2.3	0.097	0.014	0.061	0.016	0.054	0.018	0.027		
OSR	1	1	8	4	7.5	8	1	8	10	20
−3 dB SNDR gain [%]	N/A	N/A	N/A	<−5 to N/A*	N/A	<−25 to N/A*	N/A	−16~+12	−17~+13	−19~+14
BW [MHz]	10.1	80	12.5	12.5	40	6.25	50	25	20	10
SNDR [dB]	65	61.1	77.1	75.8	75.2	77.1	71.7	75	76.2	79.5
FoM_S [dB]**	156.3	167.3	171.5	174.9	177.1	173.7	180.2	178	178.2	178.5
FoM_W [fJ/conv.-step]***	255.5	12.8	30.8	12.2	6.8	18.9	2.2	5.5	6	8.5

*Does not provide the positive gain error data.

**$FoM_S = SNDR + 10\log_{10}(BW/Power)$.

***$FoM_W = Power/(2 \times BW \times 2^{(SNDR-1.76)/6.02})$

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