# Chapter 2
# SiC and GaN Power Devices

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## 1 Introduction

In an increasingly electrified, technology-driven world, power electronics is central to the entire clean energy manufacturing economy. Power switching semiconductor devices are key enablers in a wide range of power applications, including novel lighting technologies, automotive and rail traction, on board chargers, consumer electronics, aerospace, photovoltaic, flexible alternative current transmission systems, high-voltage DC systems, microgrids, energy storage, motor drives, UPS, and data centers. Silicon power devices have dominated power electronics due to their low-cost volume production, excellent starting material quality, ease of processing, and proven reliability and ruggedness. Although Si power devices continue to

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make progress, they are approaching their operational limits primarily due to their poor high-temperature performance and their relatively low bandgap and critical electric field, which result in high conduction and switching losses. Wide bandgap (WBG) SiC and GaN power semiconductor devices have recently emerged as highly efficient alternatives to their venerable MOSFET and IGBT Si counterparts. With smaller form factor, reduced cooling requirements, and established reliability, WBG devices are cost-effective silicon replacements at the system level while allowing for novel circuit architectures and simplification. In particular, as environmental awareness and a worldwide push for a zero emissions economy gain prominence, the energy efficiency offered by WBG solutions is a strong driver in their wide market acceptance and mass commercialization.

The compelling material properties of WBG devices are at the core of their suitability for more efficient, lighter, smaller form-factor power electronics operating at high frequencies, and at elevated temperatures with reduced cooling. The wider energy bandgap of 4H-SiC and GaN materials compared to that of Si allows for orders of magnitude lower intrinsic carrier density, which enables high-temperature operation with simplified thermal management. With a critical electric field that is seven to ten times larger than Si's, combined with their wider energy bandgap, WBG semiconductors can be used to make practical high-voltage (10 kV) power devices with reduced conduction and switching losses. This allows for efficient high-frequency operation that minimizes the weight and volume of passive components, increases power density, and lowers the overall system cost. For instance, the drift layer of a 4H-SiC power MOSFET can have one-tenth the thickness and about hundred times higher doping concentration of the drift layer of a silicon power MOSFETs with the same blocking capability. This results in a factor of ~800 reduction in drift layer resistance and enables smaller die sizes compared to those of silicon power devices with comparable on-state resistance and blocking voltage. Therefore, it is possible to achieve low switching and conduction losses for a wide range of blocking voltages and frequencies. Lower losses simplify circuit topology and control design and reduce the complexity of gate drivers. Overall, WBG power devices enable novel power electronics systems with higher efficiency and higher gravimetric and volumetric power-conversion densities.

High-yield manufacturing at volume fabs is a prerequisite for mass WBG commercialization. Numerous well-established processes from silicon technology have been successfully transferred to SiC. In addition, several fabrication processes specific to SiC have been developed and are at a stage of maturity. Today, SiC is produced in dedicated fabs as well as alongside silicon fabrication. The latter has the potential of SiC manufacturing at the economy scale of silicon and is a particularly attractive model. Overall, a vibrant worldwide fab infrastructure produces cost-effective 650 V to 1.7 kV SiC devices having successfully duplicated the integrated device manufacturer (IDM), foundry, fabless, and design-house silicon fabrication models. Similarly, lateral GaN power devices, commercially available from several vendors in the 100–650 V range, are CMOS-compatible and are fabricated cost-competitively in volume Si fabs and foundries.

Barriers to WBG mass commercialization still exist. Primarily, they are the higher than silicon device cost, reliability and ruggedness concerns, and the need for a trained workforce to skillfully insert WBG devices into power electronics systems. In many applications, at the system level, SiC-based systems are more cost-effective than those of silicon due to passive component simplifications. And this is before energy savings over the life of the system are taken into account. Device manufacturers have accumulated extensive field data that supports reliable operation over system lifetime. Ruggedness is addressed through design trade-offs and by employing intelligent gate drives with prognostic and diagnostic functions. A plethora of educational opportunities is presently available to train students and the existing workforce in WBG power technology. Without a doubt, WBG devices are rapidly overcoming barriers to system insertion and mass commercialization, with their cost-lowering benefits. The recent insertion of SiC in automotive traction inverters, by several electric vehicle manufacturers, is a good example of a volume application where WBG brings competitive advantages like longer range and faster charging.

The present chapter reviews commercial SiC power diodes, MOSFETs, junction gate field-effect transistors (JFETs), and bipolar junction transistors (BJTs) as well as promising insulated gate bipolar transistors (IGBTs) best suited for +10 kV applications. Unipolar SiC diodes are commercially available and are significantly faster than competing Si *p-i-n* diodes as they have no minority carrier current. SiC MOSFETs, JFETs, and BJTs have been developed for power applications. SiC JFETs are simpler to fabricate and have no gate oxide reliability issues. They are native normally-on (depletion mode), which is regarded as undesirable due to safety concerns, and are made normally-off in the cascode circuit configuration. The SiC MOSFET became commercially available by Cree in 2011 and is the workhorse of the SiC power electronics industry today. SiC MOSFETs are commercially available by several vendors in the 650–1700 V range. They have been demonstrated at 3.3, 6.5, and 10 kV with those voltage nodes up for commercial release over the next few years. SiC BJTs are bipolar devices with switching speeds similar to those of MOSFETs due to the absence of sizable minority carrier storage in their drift region [1]. As with all SiC bipolar devices, their long-term performance can deteriorate due to forward-bias voltage and current gain degradations. These degradations are caused by the growth of stacking faults from basal plane dislocations within the drift epitaxial layer. BJTs are current controlled devices, which makes them less attractive for certain high current power applications. Above 10 kV, the thick drift layer of MOSFETs becomes highly resistive and bipolar conduction can lower conduction losses with acceptable switching losses. SiC IGBTs exploit this trade-off and have been demonstrated in the 15 kV node. They are briefly presented in this chapter.

Both lateral and vertical GaN power devices are reviewed in this chapter. The GaN high-electron mobility transistor (HEMT) is the most mature among these, and the only one that is commercially available with voltage ratings in the range of 15 to 650 V [2]. Adoption of these devices is rapidly increasing for a number of applications, including fast chargers, wireless charging, data centers, and electrified transportation. Various GaN HEMT configurations exist, such as the p-GaN gate

HEMT and the cascode configuration. Commercial devices with integrated drivers are also available. The lateral layout of GaN HEMTs also facilitates the development of integrated circuits based on this technology. Thus, the combination of low-loss device performance and fast switching made possible by monolithic integration makes GaN HEMTs very attractive below 1 kV. Due to recent progress made in GaN substrate technology, research in vertical GaN devices has also intensified. Vertical unipolar and bipolar diodes with breakdown ratings exceeding 1 kV have been demonstrated. Vertical transistors, including MOSFETs, JFETs, and CAVETs, have also been reported, and, in some cases, it has been experimentally confirmed that GaN offers superior performance to SiC, thus moving closer to fulfilling its potential. Among the available vertical transistor topologies, GaN JFETs are the closest to commercialization. Given recent breakthroughs in epitaxy and selective area doping, it is also expected that GaN superjunction devices could play an important role, in turn intensifying the competition with SiC technology in medium- and high-voltage applications.

## 2 Silicon Carbide Diodes

Silicon carbide (SiC) diodes can be and are already being used in various areas of solid-state electronics. They may demonstrate parameters superior to that one of diodes made of conventional semiconductors owing to unique SiC properties including wide bandgap, high avalanche breakdown field, and excellent thermal conductivity, chemical inertness, and thermal resistance. Some types of SiC diodes are briefly described in this section.

### *2.1 Silicon Carbide Power Microwave Diodes*

The interest to SiC microwave diodes was based on theoretical estimations of the saturated drift velocity of electrons ($v_S$) in 4H polytype SiC (4H-SiC), which was expected to be 2.5 times higher than that one in silicon. Also, it was supposed that SiC microwave diodes more powerful than their Si counterparts could be fabricated due to about ten times higher avalanche breakdown field ($E_B$) in SiC than that one in Si. Indeed, SiC *p-i-n* diodes capable of commutating high microwave power [3] and SiC IMPATT (IMPact ionization Avalanche Transit-Time) diodes [4–6] were demonstrated. The first SiC IMPATT oscillator generated pulsed power of 300 mW in X-band frequency range (8.0–12.0 GHz) [4]. The $v_S$ value was measured in SiC at electric fields close to $E_B$ ($8 \times 10^6$ cm/s at about 2 MV/cm) [7, 8] and it was found to be noticeably lower than that one in silicon. Although SiC IMPATT diodes can be more powerful than that ones made of Si, they have not received further development due to the emergence of high-power microwave transistors based on GaN. SiC *p-i-n* diodes designed to switch high microwave power still can find some niches

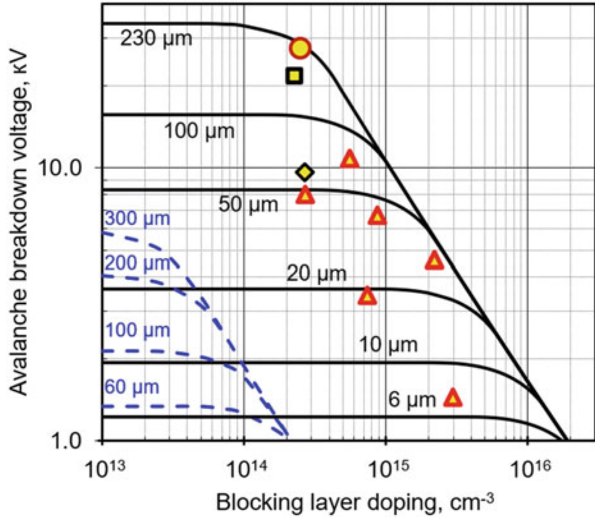


**Fig. 2.1** Calculated parallel plane avalanche breakdown voltages of Si (dashed lines) and 4H-SiC (solid lines) devices as a function of $n^-$ drift layer doping level with its thickness as a parameter. Markers denote: ▲, SiC SB and JBS diodes [15, 17, 18, 25]; ■, SiC *p-i-n* diodes [15, 46]; ◆, SiC MPS diodes [25]; ●, SiC IGBT [122]

of application and awaiting on the appearance of sufficient commercial interest to continue their development. A comprehensive overview of SiC microwave diodes can be found elsewhere [9].

## 2.2 *Silicon Carbide Power Diodes*

High-power diodes are critical building blocks of power-conversion circuits. They are commonly used, for example, in front-end rectification bridges as well as freewheeling diodes, which are placed antiparallel to power transistors to protect them from excessive reverse voltage. They are so important for this purpose that essentially every commercial power transistor package contains such a freewheeling diode.

All rectifying diodes have a lightly doped blocking layer, which is depleted at a diode's reverse bias and does not conduct current up to designed blocking voltage ($V_{BL}$). As far as the $E_B$ value in SiC is about ten times higher than in Si, SiC rectifying diodes can have about ten times thinner blocking layer at the same $V_{BL}$. Figure 2.1 shows calculated parallel plane avalanche breakdown voltages ($V_{BR}$) of Si (dashed lines) and 4H-SiC (solid lines) power devices as a function of $n^-$ blocking layer doping level ($N_D$) with its thickness ($L$) as a parameter.

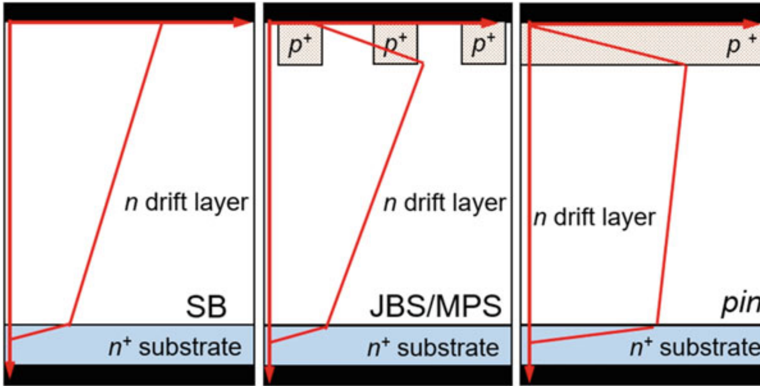


**Fig. 2.2** Schematic cross sections of SiC SB, JBS/MPS, and *p-i-n* diodes (not in scale). The red graphs show schematic electrical field distributions in reverse biased diodes

Rectifying diodes may have unipolar or bipolar conductivity in on-state. Unipolar diodes, which are Schottky barrier (SB) and junction barrier Schottky (JBS) diodes, are designed to conduct current by majority charge carriers which concentration does not exceed the $N_D$ level. *p-i-n* diodes are bipolar rectifiers, which involve a thick and lightly doped *n*-region (*i*-region), which is sandwiched between highly doped *p*- and *n*-regions. *p-i-n* diodes instead of *p-n* ones are used for power switching because the *i*-region is needed to produce a high blocking voltage. *p-i-n* and merged *p-i-n* Schottky (MPS) diodes are designed to conduct current by minority charge carriers injected in a blocking layer. In the on-state mode, the *i*-layer is conductivity modulated when the concentration of injected electrons and holes is higher than the doping concentration and thus the $R_{SP\text{-}ON}$ value is reduced as the current increases. Schematic cross sections of SiC SB, JBS/MPS, and *p-i-n* diodes are shown in Fig. 2.2. All these types of SiC high-power rectifying diodes are briefly discussed below.

## 2.3 Schottky Barrier Power Diodes (SBDs)

SBDs have a rectifying metal-semiconductor contact with low built-in voltages ($V_{bi}$) in comparison to that one in *p-n* junctions. The blocking layer conductivity in SBDs is unipolar, and hence, these diodes have a low reverse-recovery charge density ($Q_{RR\text{-}ON}$). On the other hand, the lack of the conductivity modulation in the case of SBDs results in a bend-over in the SBD characteristics at high currents due to the resistance of the lightly doped drift region. Another feature of SB diodes is the large reverse leakage current that can lead to non-negligible off-state power dissipation primarily due to thermionic field emission of carriers from the metal into the semiconductor, and exacerbated by the barrier-lowering effect. SiC SB diodes

**Table 2.1** Demonstrated 4H-SiC SB diodes

| $V_{BL}$ (kV ) | $V_{ON}$ (V ) | $R_{SP\text{-}ON}$(mΩ·cm$^2$) | References |
|---|---|---|---|
| 1.2 | 1.35 at 200 A/cm$^2$ | – | [11] |
| 1.4 | 2 at 732 A/cm$^2$ | 1.5 | [12] |
| 1.7 | 2 at 126 A/cm$^2$ | 8.7 | [13] |
| 3 | 7.1 at 100 A/cm$^2$ | 34 | [14] |
| 4.6 | 2.3 at 20 A/cm$^2$ | 10.5 | [15] |
| 5 | 2.4 at 25 A/cm$^2$ | 17 | [16] |
| 6.7 | 4 at 60 A/cm$^2$ | 43 | [17] |
| 10 | 11.75 at 20 A/cm$^2$ | 97.5 | [18] |

have a higher $V_{bi}$ value in comparison to that of Si due to higher barrier height. The higher $V_{bi}$ value results in smaller reverse leakage currents, thus making it possible to fabricate SiC SB power diodes with very high $V_{BL}$ voltages which are unattainable in Si SBDs as shown in Table 2.1 [10].

A recent review on SiC SB diodes with a deep description on their operation is given in [19].

High-voltage 4H-SiC SB diodes have been introduced to the market since 2001 [20], and for a long time, they have been the only SiC diodes commercially available despite the advantages of p-n diodes for very high voltages. Note that using SiC SB diodes for $V_{BL}$ higher than 600 V is impractical due to a non-negligible off-state power dissipation, and for this reason, JBS diodes have been introduced. Practically, most of commercial SiC Schottky diodes are of JBS type.

## *2.4 JBS and MPS Diodes*

The problem of high leakage current in reverse direction of SBDs was overcome when the JBS/MPS design [21] was first implemented in development of SiC high-power diodes [22]. The structure of the JBS/MPS diodes consists of interdigitated pin and Schottky diodes, electrically connected in parallel (Fig. 2.3a [23]). Under reverse bias, the diodes operate like *p-i-n* diodes minimizing thus off-state losses. Indeed, in this case, the multiple $p^+$ regions push the maximum of electrical field away from the Schottky contact toward the bottom of the $p^+$ region (see Fig. 2.2) reducing the electrical field under metal contact and, hence, the leakage current.

The difference between a MPS and a JBS rectifier is that the $p^+$-$n$ junctions in JBS diodes do not turn on during on-state operation, while in the MPS rectifier, the SB regions are very narrow so that the $p^+$-$n$ junctions are turned on resulting in minority carrier injection and reduction of $R_{SP\text{-}ON}$.

More precisely, the JBS and MPS represent modes of operation under forward bias (Fig. 2.3b). For low forward current values, most of the current is conducted through the Schottky areas of the diodes resulting in no minority-carrier-charge-stored, and thus the turn-off transient is fast, minimizing switching loss (JBS mode).

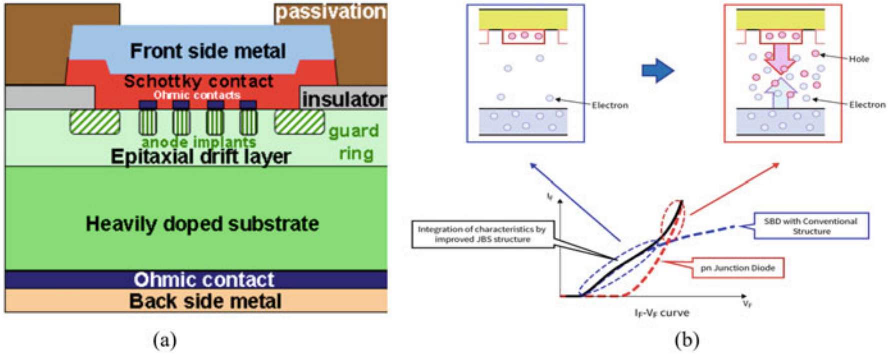


**Fig. 2.3** (**a**) The structure of a 4H-SiC JBS/MPS diode. The $p^+$ anode regions are spaced far enough apart that their depletion regions do not touch under zero or forward bias. (From [19]). (**b**) Forward *I-V* of *p-i-n*, SB, and MPS diodes showing that the characteristic of the MPS diode is a combination of that of SB (low current values-unipolar conduction) and *p-i-n* (high current values-bipolar conduction). Note the bend-over in the SBD characteristics at high currents (1000 $\text{Acm}^{-2}$ [24]) due to the resistance of the lightly doped drift region resulting in diode overheating. (From [23])

**Table 2.2** Demonstrated 4H-SiC JBS/MPS diodes

| $V_{BL}$ (kV ) | $V_{ON}$ (V ) | $R_{SP\text{-}ON}$(mΩ·cm$^2$) | References |
|---|---|---|---|
| 0.98 | 3.1 at 100 A/cm$^2$ | 19 | [26] |
| 1.6 | 1.4 at 100 A/cm$^2$ | 7.5 | [27] |
| 1.7 | 1.6 at 100 A/cm$^2$ | 2.9 | [28] |
| 2.8 | 2 at 100 A/cm$^2$ | 7.5 | [29] |
| 5 | 3.5 at 108 A/cm$^2$ | 25.2 | [30] |
| 6.5 | 4 at 83 A/cm$^2$ | | [31] |
| 10 | 3.37 at 20 A/cm$^2$ | 100 | [32] |

However, with no conductivity modulation, the series resistance of the drift region leads to a voltage drop that dominates the total voltage drop in Schottky areas at high currents [24]. At a certain point, the voltage drop reaches a value "turning-on" the PN areas of the diodes inducing injection of minority carriers (MPS mode). So, significant minority charge storage occurs reducing the on-state loss at high current densities, but the stored charge increases the switching loss. The crossover point between JBS and MPS mode in current density value decreases with the blocking voltage of the diode. This means that the MPS mode dominates above quite low current density values for blocking voltages above 10 kV [24, 25].

Table 2.2 summarizes some recent results on JBS diodes [10].

As mentioned above, nowadays all commercial high-power 4H-SiC diodes are of JBS type even if they often are mentioned as Schottky diodes. Samples of SiC MPS diodes with maximum rating 3300 V/50 A are available from GeneSiC Semiconductor Inc. [33].

## 2.5 *p-i-n* Power Diodes

*p-i-n* diodes can be more efficient at higher blocking voltages than the unipolar diodes, thanks to the conductivity modulation effect leading to the significant reduction of $R_{SP\text{-}ON}$. Since the $R_{SP\text{-}ON}$ does not depend on $N_D$ at conductivity modulation, a punch-through design can be realized in *p-i-n* diodes for further reduction of $R_{SP\text{-}ON}$ and switching time. The reverse leakage in *p-i-n* diodes is primarily due to thermal generation and is extremely small in comparison to SB diodes. Furthermore, *p-i-n* diodes are distinguished by their inherent better reliability and thermal stability. At $V_{BL}$ ratings exceeding 6 kV, reduction of $R_{SP\text{-}ON}$ resulting from the conductivity modulation in SiC *p-i-n* diodes compensates additional resistance of a $p^+$ layer and larger $V_{bi}$ voltage (~2.8 V vs. 0.9 V) in comparison with SiC SB diodes, and using SiC *p-i-n* diodes becomes more preferable.

Injected minority carriers must have a lifetime long enough to drift through the full length of a blocking layer (about 40 μm for $V_{BL} = 6$ kV in 4H-SiC *p-i-n* diodes) for an effective conductivity modulation. That was the first pitfall on the way to SiC power bipolar devices because SiC epitaxial layers grown in the 1990s suffered from very low minority carrier lifetimes not exceeding 100 ns. Thanks to the introduction of new epitaxial methods [34], minority carrier lifetime of the order of 2 μs was measured in 4H-SiC *n*-type ($10^{16}$ cm$^{-3}$) epilayers in 2001 [35]. This lifetime value corresponds to the diffusion length of about 30 μm but still remains too low for conductivity modulation of thick layers required for high-voltage SiC *p-i-n* diodes (~100 ÷ 200 μm). An effective solution of this problem was found in 2007. A two times increase of minority carrier lifetime in 4H-SiC epilayers after carbon ion implantation into the shallow surface layer and subsequent post-implantation annealing (PIA) was reported [36]. In 2009, T. Hiyoshi and T. Kimoto replaced the implantation and PIA by a single processing step of thermal oxidation [37]. Since then, the lifetime enhancement thermal oxidation has become a standard step in processing SiC power devices. Recently, S. Ryu, et al. reported carrier lifetimes ranging from 15 μs to 20 μs (corresponding to the diffusion length of 90 μm at ambipolar diffusion coefficient of 4 cm$^2$/s) in *n*-type 4H-SiC layers (140 μm thick, $2 \times 10^{14}$ cm$^{-3}$) measured after the thermal oxidation at 1450 °C for 5 hours [38].

Another obstacle on the way to the SiC bipolar power devices was identified in 2000. H. Lendenmann et al. reported that the voltage drop in 4H-SiC *p-n* junction diodes anomalously increased during their operation at a forward bias [39]. It was observed that triangular planar defects interpreted as stacking faults (SF) lying in basal planes of SiC originating from basal plane dislocations (BPDs) appeared and expanded in SiC epilayers concurrently with the degradation of *I-V* characteristics. It was found that the energy of electron-hole recombination in SiC is high enough to induce a SF nucleation and expansion. Since the carrier recombination is a fundamental process in bipolar devices and cannot be avoided, the development of SiC bipolar devices was significantly hampered. Moreover, SFs can be created during device processing and special care has to be taken to avoid this

[40]. Tremendous efforts were spent to overcome this problem [41–44]. As a result, degradation-free SiC *p-i-n* diodes with active area of 0.22 cm$^2$ and $V_{BL} = 6.5$ kV were reported [45].

Resolving the problems of low minority carrier lifetime and forward-bias degradation paved the way to successful development of 4H-SiC *p-i-n* diodes. In 2012, H. Niwa et al. [46] reported SiC *p-i-n* diodes with $V_{BL} = 21.7$ kV. Nowadays, SiC *p-i-n* diodes with maximum rating 15 kV/1 A and 8 kV/2 A are offered by GeneSiC Semiconductor Inc. [33].

## 2.6 Edge Termination

Due to a very high $E_B$ value in SiC, one of technical challenges that must be addressed in design of high-voltage SiC devices is the surface electrical field reduction at the edge of a device. This is especially important for SiC SB diodes where the maximum of electrical field is located at the metal-semiconductor interface. Numerous planar edge termination techniques have been demonstrated in SiC diodes, most of them based on similar concepts used in Si power devices [47]. Typical ones are junction termination extension (JTE) [16], floating field ring (FFR) [48], field plates [49], mesa structure [50], bevel structure [51], and hybrid solution methods [25–28]. The JTE and FFR are regarded as the most effective methods for high-voltage SiC devices. Although a single-zone JTE conceptually works, it shows a narrow window of dose optimization range to achieve the desired voltage. Therefore, multiple zone JTE is mostly used [15]. The multiple zones are formed either by performing different dose implantation steps or by creating unsymmetrical shapes and/or distances among the zones. In the case of FFR termination method, a single implant can be used, thereby reducing the processing steps. However, the optimization of the spacing between the floating zones is complex and challenging.

## 2.7 Main Points on SiC Power Diodes

The most important SiC diode rectifier device design trades off roughly parallel well-known silicon rectifier trade-offs, except for the fact that numbers for current densities, voltages, power densities, and switching speeds are typically much higher in SiC. Indeed, the high breakdown field of SiC allows for low $R_{ON}$, $V_{ON}$, values, and practical absence of reverse recovery and thus permitting operation of SiC diodes at much higher voltages, current densities, and switching speeds. Moreover, the higher SiC bandgap in comparison to Si allows for a higher barrier height of Schottky diodes by almost 1 eV and thus reducing the reverse current by 17 orders of magnitude at room temperature [24]. On the other hand, SiC *p-i-n* diodes have a larger built-in voltage ($\sim$2.8 V) due to its wider bandgap than the Si PiN diodes, but they have a lower forward voltage drop at high current density and higher

switching speed due to the much thinner i-region. Furthermore, SiC diodes are distinguished by the inherent better reliability and thermal stability of their electrical characteristics as well as their possibility to operate at temperatures higher than 125 °C. Indeed, most commercial SiC power diodes are rated up to 175 °C [1], while diodes operating well above 200 °C have been demonstrated.

Unipolar SiC diode is the main commercially available diode on the market; its typical voltage ratings are 600 V, 650 V, 1.2, and 1.7 kV. Some 3.3 and 8 kV products also are available but their current rating is limited by the thick drift layer and the associated resistance [1]. For instance, the current rating for 8 kV SiC diode is only 50 mA. At 10–20 kV voltage ratings, 4H-SiC *p-i-n* rectifiers offer the best trade-off between on-state voltage drop, switching losses, and high-temperature performance as compared to Si *p-i-n* or SiC Schottky/JBS rectifiers.

SiC diodes have a long and enthralling story of their development and commercialization which is still ongoing and far from over. Currently, the main driving force for further development of high-power SiC diodes is a rapidly growing demand of highly efficient switches and rectifiers for automotive and industrial applications with blocking voltages and commutated power ranging from ~600 V/100 kW in invertors for electrical vehicles to ~1.1 kV/13 GW in convertors for high-voltage DC power transmission.

## 3 SiC BJTs

Bardeen, Brattain, and Shockley invented the bipolar junction transistor (BJT) in 1947 at Bell Laboratories [52]. BJT is a three-terminal power device, schematically shown in Fig. 2.4, available in the market for more than 50 years [53]. Muench et al. reported the first SiC BJT in 1977 [54]; however, the first SiC BJT that got attention was the first high-voltage 4H-SiC BJT reported by Ryu in 2001 [55]. 4H-SiC BJT has been extensively developed in recent years for high-voltage and high-temperature applications due to its unique properties such as low on-resistance, normally-off behavior, fast switching, and lack of gate-oxide reliability issues.

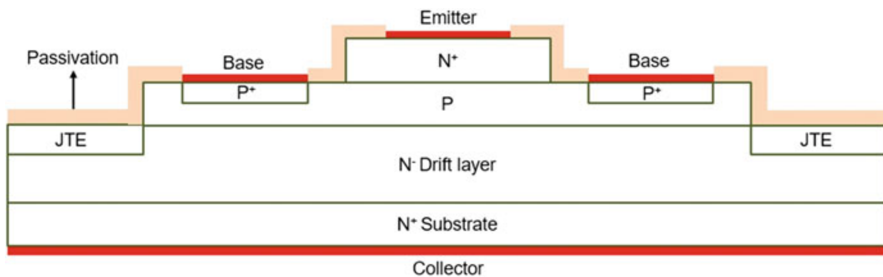


**Fig. 2.4** Simplified cross sections of SiC BJT (not in scale)

**Table 2.3** Recent reported high-voltage 4H-SiC BJTs

| BV (kV) | Ron (mΩ•cm$^2$) | Current gain ($\beta$) | References |
|---|---|---|---|
| 1.8 | 4.4 | 40 | [62] |
| 2.7 | 4 | 132 | [63] |
| 3.2 | 28 | 28 | [64] |
| 5.65 | 18.8 | 44 | [58] |
| 5.85 | 28 | 40 | [59] |
| 6 | 28 | – | [65] |
| 10.5 | 110 | 75 | [66] |
| 16.25 | 579 | 139 | [60] |
| 23.5 | 321 | 7 | [67] |

SiC BJTs have a large *safe operating area (SOA)* in which the second breakdown occurs at very high current densities (outside the range of possible operation) [56]. Moreover, SiC BJTs have some advantages compared to SiC MOSFETs:

1. Possibility to have conductivity modulation in the drift layer, thus lowering the on-resistance and power losses in on-state mode.
2. Lower fabrication cost.
3. The positive temperature coefficient of the on-resistance and negative temperature coefficient of the current gain ($\beta$) results in an easy device paralleling configuration.
4. Non-dependency on a gate oxide and no suffering from the oxide reliability for high-voltage, high-temperature, and harsh environment applications.

It should be noted that the on-resistance for a 4H-SiC unipolar device like MOSFETs above 15 kV increases to a point where it is impractical from a yield standpoint and cost [57]. Bipolar devices like SiC BJTs are good candidates to replace them. However, to be fully competitive with SiC MOSFETs and SiC IGBTs in the market, the SiC BJT characteristics need to be improved. In recent years, there has been a growing investigation to improve the on-resistance, current gain, current density, and breakdown voltage. Table 2.3 summarizes some of these works.

The first obstacle to the commercialization of SiC BJTs was the forward-bias degradation observed in all SiC bipolar devices originating from BPDs existing in epitaxial layers (see above part on SiC diodes). This problem has been hopefully resolved [45]. The second obstacle to the commercialization of SiC BJTs was the formation of new BPDs and lifetime killer defects during the processing [40]. For example, ion implantation followed by high-temperature annealing produces new lifetime killer defects that cause bipolar degradation and reduce the common-emitter current gain. To overcome this problem, the ion implantation for forming JTE and $p^+$ region base (Fig. 2.4) can be easily replaced by etched-JTE-zone [58–60] and by epitaxial regrowth of $p^+$ region [61], respectively. The third obstacle was surface recombination caused by the presence of interface trap density at the SiC/$SiO_2$-passivation-layer interface, thus lowering the current gain. Different techniques have been addressed in recent years for overcoming this issue [10].

In recent years, high-temperature SiC BJTs ICs have also been investigated in depth at device physics, circuit, and process integration [68, 69]. The short-circuit ruggedness of 10 kV SiC BJTs with a 16 μs withstand time was recently reported. It shows that the SiC BJTs can handle without failing about three times the critical short-circuit energy of the commercial SiC MOSFETs [70].

## 4 SiC Junction Field-Effect Transistors

The SiC junction field effect transistor (JFET) is capable of high-power and high-temperature switching as it only uses *p-n* junctions in the active device area, where the high electric fields occur, and can therefore fully exploit the high-temperature properties of SiC in a gate voltage-controlled switching device. Provided the gate-to-source junction of the JFET is biased below its built-in potential, negligible gate current is needed to drive the device and voltage controlled switching is realized. JFETs are free of MOS native oxide problems like low channel mobility, threshold voltage instability, and lack of reliability at elevated temperatures. They have demonstrated electrostatic discharge immunity to 16 kV (V Veliadis, Private communication) and as unipolar devices do not suffer from forward voltage degradation at the same degree as bipolar devices [39–42]. SiC power JFETs are almost exclusively implemented in a vertical configuration and are native depletion mode or normally-on (Non).

Several SiC JFET designs have been demonstrated over the years schematically shown in Fig. 2.5. The first power 4*H*-SiC JFETs were reported by H. Mitlehner et al. in 1999 [71]. Those were vertical JFETs (VJFETs) with lateral channel (Fig. 2.5a) and they have been further developed by D. Stephani et al. [72] and S-H. Ryu et al. [73]. This JFET is similar to a SiC double-implanted MOSFET (DMOSFET), with the oxide controlled inversion channel having been replaced with a bulk channel. This eliminates the SiC/SiO2 interface with its channel mobility and reliability drawbacks and creates a bulk channel where the SiC mobility is fully utilized.

Zhao et al. have implemented a JFET design with relatively critical dimensions (Fig. 2.5b) [74]. The design requires three implantation events. In order to implant the lower portion of the sidewalls, the wafer must be tilted against the direction of the ion beam and rotated. No epitaxial regrowth is needed.

A simplified cross-sectional schematic of a trenched-gate vertical channel $p^+$ ion-implanted depletion mode (normally-on) 4H-SiC JFET is shown in Fig. 2.5c [75]. This representative for all JFET designs will be used to analyze, in the following, the SiC JFETs electrical characteristics, thermal performance, and ruggedness. A series of papers reported on the detailed fabrication and the related electrical characteristics [76–78] of this SiC JFET design.

The inherent simplicity of the design shown in Fig. 2.5c, which does not require epitaxial regrowth, is the reason for the demonstration of reliable JFETs with excellent yields and parameter uniformity [75]. 1680 V SiC JFETs with an active

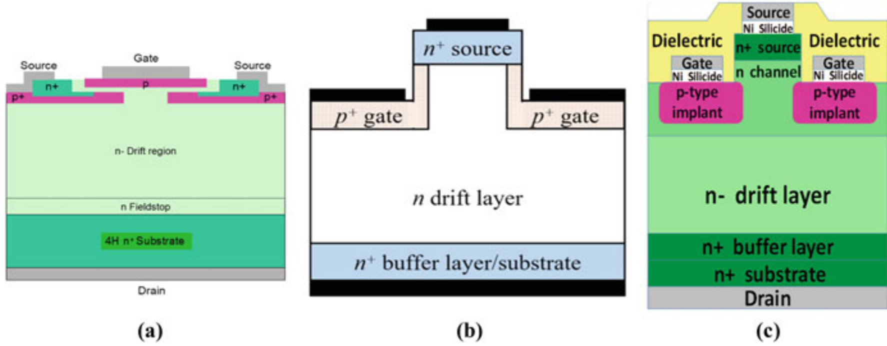


**Fig. 2.5** Simplified cross sections of (**a**) a vertical JFET with a lateral channel (the $n^+$ source is embedded in the $p$-well and reaches below the $p$ gate, in order to minimize source resistance), (**b**) a trench and implanted vertical JFET, (**c**) a depletion mode ion-implanted SiC vertical-channel JFET

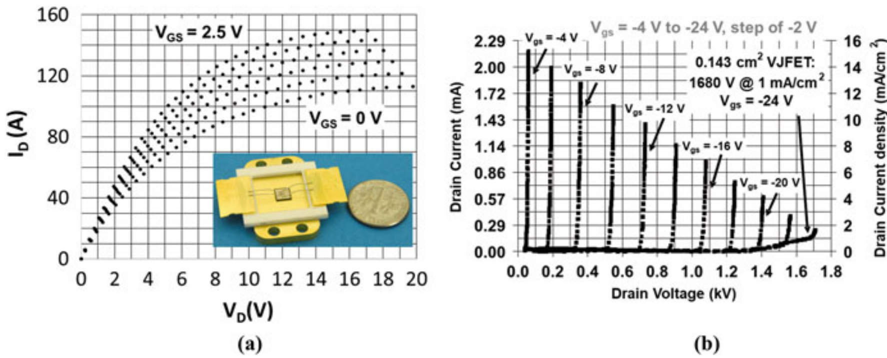


**Fig. 2.6** (**a**) On-state drain current vs. drain voltage and (**b**) blocking voltage characteristics of a single 1680 V, 0.143 cm$^2$ packaged SiC JFET

area of 0.143 cm$^2$ (0.19 cm$^2$ total area) and on-state current capability of 50 A were fabricated by Veliadis et al. in seven photolithographic levels, with a single masked ion implantation event that simultaneously implanted the p$^+$ gates and guard rings [5]. Indeed, the simplicity of the design greatly reduces process complexity and JFETs using even only four lithography steps have been demonstrated [76–78]. Room-temperature on-state drain-current vs. voltage characteristics are shown in Fig. 2.6a at a gate bias range of 0 to 2.5 V in steps of 0.5 V. To maintain voltage-control capability (high $I_D/I_G$ gain), the gate must be biased below its 2.7 V built-in potential value. If the gate bias increases in excess of 2.7 V, significant gate current injection occurs into the channel of the JFET, and its current gain $I_D/I_G$ degrades. At a gate-to-source bias of 2.5 V, the JFET outputs 53.6 A at a forward drain voltage drop of 2.08 V. The specific on-state resistance is 5.5 m$\Omega$·cm$^2$, and the transistor current gain is $I_D/I_G = 26{,}800$.

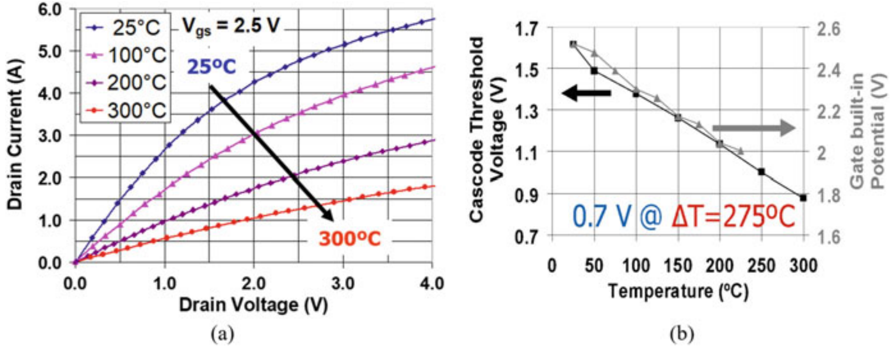


**Fig. 2.7** Temperature dependence of the SiC cascode's (**a**) on-state drain current at $V_{GS} = 2.5$ V and (**b**) threshold voltage (left axis) and gate-junction built-in potential (right axis). At a temperature swing of 275°C, the threshold voltage only shifts by 0.7 V

The blocking voltage characteristics of the 0.143 cm$^2$ active area JFET at gate biases of −4 to −24 V, in steps of −2 V, are shown in Fig. 2.6b. At a gate-to-source bias of −24 V and a low drain current density of 1 mA/cm$^2$, the JFET blocks 1680 V.

An important contribution to SiC device reliability is eliminating threshold voltage instability. In SiC MOSFETs, threshold voltage instability is primarily due to the oxide traps at the SiC/gate-oxide interface (see corresponding part below).

To investigate the threshold voltage stability of JFETs, a JFET-based all-SiC normally-off switch was implemented by combining a 1200 V normally-on JFET with a low-voltage normally-off (enhancement mode) JFET in the cascode configuration [79]. To evaluate threshold voltage shift with temperature, the $I_{DS}$-$V_{DS}$ characteristics of the all-SiC cascode switch were measured at junction temperatures of 25 °C, 100 °C, 200 °C, and 300 °C and are shown in Fig. 2.7a [80]. The cascode's on-state resistance is 6.2 mΩ·cm$^2$ and was extracted from the data of Fig. 2.7 at $V_{DS} = 0.5$ V. The increase in on-state resistance with temperature agrees well with the theoretical reduction of the electron mobility in 4H-SiC. The cascode threshold voltage was extracted and is plotted as a function of temperature on the left axis of the graph of Fig. 2.7b.

The threshold voltage decreases from 1.6 V to 0.9 V as the temperature increases from 25 °C to 300 °C; the cascode switch remains normally-off at 300 °C. The cascode's gate-junction built-in potential variation with temperature was also extracted and was plotted on the right axis of the graph of Fig. 2.7. As the temperature increases from 25 °C to 225 °C, the cascode's threshold voltage decreases by 0.54 V, while its gate-junction built-in potential decreases by 0.52 V. This excellent agreement confirms that the decrease in cascode threshold voltage with temperature stems from the reduction of its gate-junction built-in potential as expected from solid-state physics. Thus, SiC JFETs have remarkably stable threshold voltages due to the fact that it uses p-n junctions instead of gate oxides to control the current flow.

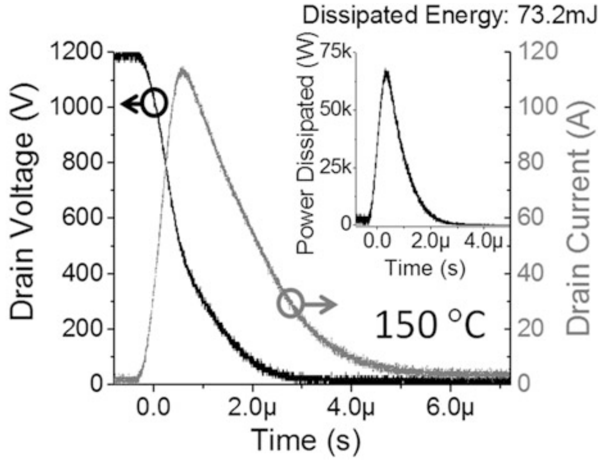


**Fig. 2.8** Representative 1200 V/115 A hard switching waveforms of the SiC JFET testing at 150 °C. The energy dissipated by the JFET during each hard switching event is 73.2 mJ (inset), and the peak dissipated power is 68.2 kW

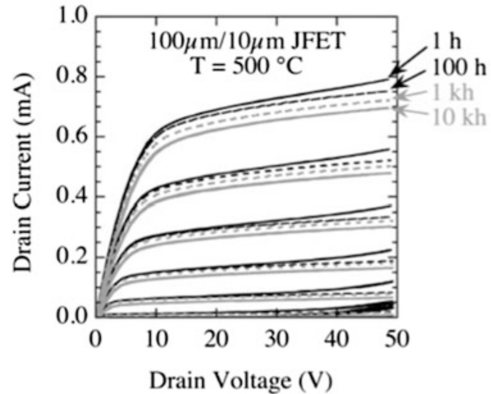


**Fig. 2.9** $I_D$-$V_D$ characteristics of a descrete 6H-SiC JFET. (From [84])

To evaluate ruggedness, a SiC JFET was subjected to over 2.4 million 1200 V/115 A hard switching events at 150 °C, at what is 13 times its 8.8 A 150 °C rated current (Fig. 2.8) [81]. The JFET drain voltage is plotted in black (left axis) in Fig. 2.8, while the current through the JFET is plotted in gray (right axis). By multiplying voltage by current, the power dissipated by the JFET is calculated and plotted in the inset of Fig. 2.8. The energy dissipated by the JFET during each 1200 V/115 A switching transient is 73.2 mJ, and the peak dissipated power is 68.2 kW. Finally, it has been shown [81] that the electrical characteristics (on- and off-state) do not degrade with stressing (Fig. 2.9).

The ruggedness of SiC JFETs especially at high temperatures has been validated by the group of Philip Neudeck at NASA John Glenn Research Center. They demonstrated a short-term operation of packaged 4*H*-SiC junction field effect

transistor (JFET) logic integrated circuits (ICs) at ambient temperatures exceeding 800 °C in air [82]. They also demonstrated SiC lateral JFETs with operating time of 6000 hours at 500 °C which was limited by the thermal degradation of a metal stack used for the formation of ohmic contacts in these devices [83, 84].

Today, power SiC JFETs are commercially available as discrete components in the 650–1700 voltage range [85]. The MOSFET dominates SiC-based power electronics. JFETs are being inserted in systems in smaller numbers. As SiC power electronics continue to gain ground, the JFET has the potential to be the device of choice for rugged high-temperature applications.

## 5 SiC MOSFETs

A power MOSFET is a high-speed, easy-to-drive device, which makes it a very attractive option for power switching applications. The main advantage of the power MOSFET structure is the high impedance gate, which does not require steady-state gate current, and the gate drives are only required to provide relatively small amount of current to charge and discharge the capacitances. The current conduction in the power MOSFET structure occurs through transport of majority carriers in the drift region and does not involve minority carrier injection. Hence, there are no delays associated with storage or recombination of minority carriers in power MOSFETs. It is also easy to parallel multiple power MOSFETs because of the positive temperature coefficient of the forward voltage drop, due to the decrease in carrier mobility at elevated temperatures, which prevents subsequent thermal runaways. In addition, the power MOSFETs do not go through second breakdown like bipolar junction transistors and offer excellent safe operating area.

On-resistance of a power MOSFET increases quite rapidly with blocking voltage of the device. For silicon power MOSFETs, which is the most commonly used semiconductor material, the on-resistance of a power MOSFET can be very small if the design voltage of the device is 200 V or less [47]. Silicon power MOSFETs designed for voltages greater than 200 V have an unacceptably high on-resistance, large chip area, and significant increases in parasitic capacitances. Researchers in silicon power devices addressed this issue by placing an injecting junction at the drain side of the device, which reduced the drift layer resistance by minority carrier injection, or conductivity modulation of the drift layer [86, 87], resulting in the development of insulated gate bipolar transistors (IGBTs). The other approach used to reduce the on-resistance of silicon power MOSFETs is the use of superjunction (SJ) structure [88], which utilizes alternating n- and p-columns with relatively heavy doping concentrations. Excellent results have been achieved for devices with blocking voltages up to 950 V [89].

A silicon (Si) IGBT provides significantly lower forward voltage drops compared to a conventional Si power MOSFET in higher blocking voltage (>600 V) rated devices and at high current levels. However, this reduction in on-state forward voltage drop comes with some serious drawbacks such as (i) at lower current levels,

the forward voltage drop of power MOSFETs can be lower than in IGBTs; (ii) unlike power MOSFETs, IGBTs cannot conduct currents in the reverse direction; and (iii) IGBTs exhibit longer switching times and substantially higher switching losses, when compared to a power MOSFET due to the minority carrier injection into the drift region.

Power MOSFETs in silicon carbide (SiC) can address these issues [90]. The wide bandgap properties of SiC provide high breakdown electric field, which allows thinner drift layer with significantly higher doping concentration. This makes possible designs of unipolar SiC power devices with extremely low on-resistance, which addresses most of the issues discussed above. Fabrication processes, including techniques to form high-quality gate oxide films and selective doping methods, are well established in silicon carbide, which culminated in successful development and commercialization of silicon carbide power MOSFETs.

### *5.1 4H-SiC DMOSFETs*

Figure 2.10 shows a simplified cross section of a power double-implanted MOSFET (DMOSFET) in SiC, which was the first commercially available power MOSFET structure in SiC. The $n^+$ sources and MOS channel regions are built in implanted p-wells. The $n^+$ source regions and the p-wells are tied together using common contacts to source, to keep the potential difference between the two regions at minimum. The device turns on when a positive bias exceeding the threshold voltage of the device is applied to the gate electrode. In the on-state, electrons flow from the $n^+$ source regions through the MOS channel formed in the p-well into the junction field effect transistor (JFET) region. The JFET regions are defined as the n-type region formed between adjacent p-wells. The length of the MOS channel is determined by the distance from the edges of the $n^+$ regions and the p-wells. The electrons then spread into the drift layer and then flow into the $n^+$ substrate and exit the structure through the drain electrode. In the off-state, a bias less than the threshold voltage of the device is applied to the gate electrode, which removes the inversion channel in the MOS region in the p-well and isolates the $n^+$ regions from the JFET regions. The device turns into a *p-i-n* diode structure, which can block the voltage when a positive bias is applied to the drain electrode and allow current to flow through when a negative bias is applied to the drain electrode. It should be noticed that the depletion regions from the p-wells merge and provide shielding to the gate oxide layers. The doping concentration and the width of the JFET region should be set carefully to provide adequate shielding to the gate oxide in the off-state, as well as low resistance during the on-state operation of the device [91].

Theoretical specific on-resistance ($R_{\text{SP-ON}}$) values based on drift resistance calculations are plotted in Fig. 2.11 for silicon and 4H-SiC. Performance points of Wolfspeed power MOSFETs with blocking voltages ranging from 900 V to 15 kV are also shown on the plot [92]. For devices with blocking voltages of 6.5 kV or higher, the performance points are close to the ideal silicon carbide 1-D limit, since

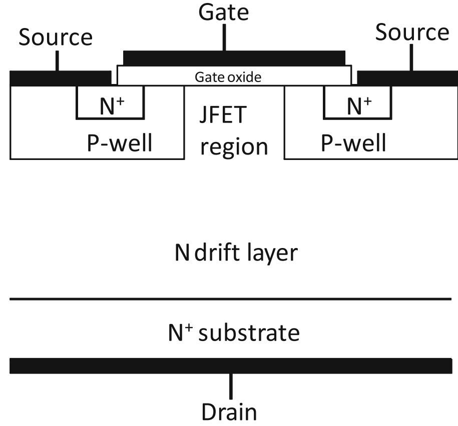


**Fig. 2.10** Simplified cross section of a SiC DMOSFET

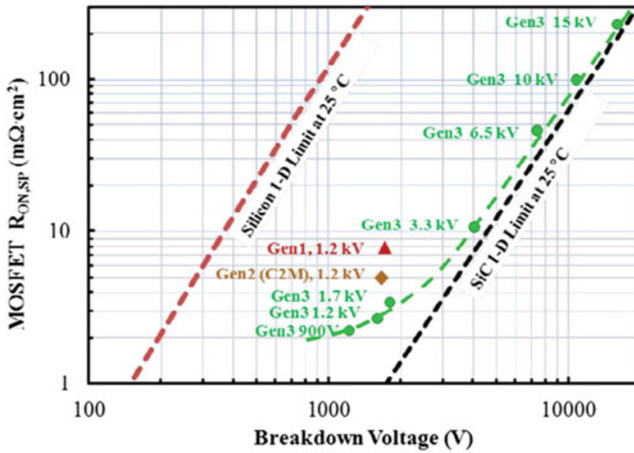


**Fig. 2.11** Experimental $R_{\text{SP-ON}}$ values of SiC DMOSFET for blocking voltages ranging from 900 V to 15 kV. (From [92])

the on-resistance of the devices is dominated by the drift resistance. For devices with blocking voltages of 3.3 kV or lower, the performance points deviate from the ideal 1-D limit due to impacts of other parasitic resistance components, most significantly from the MOS channel resistance.

## 5.2 *MOS Channel Resistance Issue*

For optimization of power DMOSFETs in 4H-SiC, it is very important to minimize the MOS channel resistance. First successful approach for reducing the MOS channel resistance was to utilize self-aligned ion implantation to reduce the MOS

channel length [93]. This approach resulted in 2 kV power MOSFETs in 4H-SiC with a specific on-resistance of 10.3 $m\Omega \cdot cm^2$ and provided a foundation for the commercialization of power MOSFETs in silicon carbide.

Attempts were made to further improve MOS interface properties, by incorporating impurities other than nitrogen into the gate oxide to achieve greater MOS channel mobility than what can be obtained using NO or $N_2O$ anneals. Doping of the oxide layers with phosphorus [94] and boron [95, 96] has been investigated. A MOS channel mobility of 98 $cm^2/(V \cdot s)$ is achieved using phosphorus doping approach [94], and boron doping approach resulted in a MOS channel mobility of 102 $cm^2/(V \cdot s)$ [95], and a 4.5 kV power DMOSFET was demonstrated [96]. Approximately a factor of 3 improvement in MOS channel mobility over nitridation using NO or $N_2O$ was observed using this approach. However, it was determined that these approaches were not suitable for commercial 4H-SiC power MOSFETs since a reasonable threshold voltage stability could not be achieved (P. Godignon, private communications).

Usage of alkaline earth elements, such as strontium (Sr) and barium (Ba), as interface passivation materials for 4H-SiC MOSFETs was also investigated [97]. The passivation was performed by placing a very thin interlayer material directly on the 4H-SiC surface, followed by deposition of gate dielectric layer, typically $SiO_2$, which was annealed in $O_2/N_2$ ambient for densification [97]. Sr passivation of the MOS interface showed a very promising result, resulting in a MOS channel mobility of 40 $cm^2/(V \cdot s)$, which was comparable to the values achievable using an NO anneal [97]. Passivation using Ba turned out to be significantly more efficient, resulting in a MOS channel mobility of 85 $cm^2/(V \cdot s)$ at room temperature, which is approximately double the value from an NO annealed sample [97]. A comparison of MOS channel mobility at temperatures ranging from 25 °C to 150 °C is shown in Fig. 2.12. A test lateral MOSFET with conventional NO anneal process and a device with barium interlayer (Ba IL) passivation process were used for this comparison [97]. The samples were fabricated on $5 \cdot 10^{15}$ $cm^{-3}$ doped p-type epilayers on 4H-SiC substrates. The MOS channel mobility of the Ba IL-passivated sample decreases with temperature, as expected due to phonon scattering effects. This is in contrast to the NO annealed sample, which showed an increase in MOS channel mobility with temperature due to the higher interface density near the conduction band.

Recently, C-C bonds formed during thermal oxidation of SiC were identified as one of the important factors limiting MOS channel mobility [98]. The impacts of C-C bonds are also present on samples that received sacrificial oxidation, where the resulting thermal oxide layer was chemically removed [99]. Various approaches to form gate oxide layers with minimum thermal oxidation have been presented. This includes a deposition of a thin Si film, which was converted to $SiO_2$ by low-temperature oxidation [100] as well as a direct deposition of $SiO_2$ layer onto SiC surface [101]. For both approaches, $H_2$ treatment of SiC surface to etch away thermally oxidized region and interface nitridation to achieve a low density of interface traps ($D_{it}$) were performed. The elimination of thermal oxidation process resulted in approximately a factor of 2 increase in MOS channel mobility, as shown in Fig. 2.13.

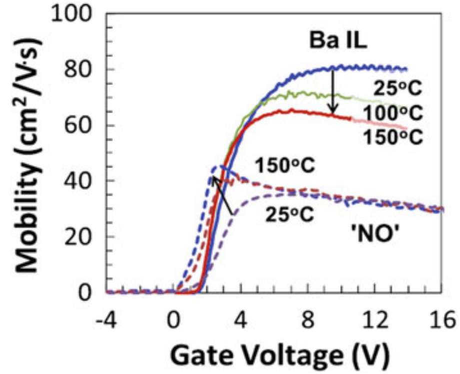


**Fig. 2.12** MOS channel mobility as a function of temperature from Ba IL processed device. Results were compared to values from an NO annealed sample

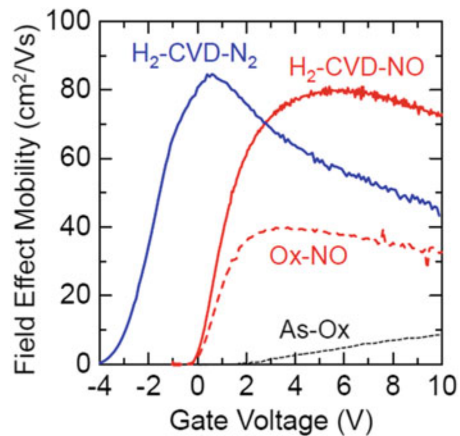


**Fig. 2.13** MOS channel mobility of n-channel MOSFETs, fabricated using various processes [99]

Reduction in surface nitridation temperature to avoid in situ oxidation and material decomposition was attempted using supercritical $N_2O$ fluid ($SCN_2O$) [102]. The approach utilized gas-like high penetration property and liquid-like solubility of supercritical fluids. 4H-SiC MOS interface with thermally grown gate oxide was processed with supercritical $N_2O$ fluid at a temperature of 120 °C. A MOS channel mobility of 72.3 $cm^2/(V\cdot s)$ was reported, showing significant improvement in MOS channel properties over devices that received thermal nitridation processes [102].

### *5.3 4H-SiC Trenched MOSFETs*

A trench MOSFET structure, shown in Fig. 2.14, can provide devices with significantly smaller cell pitch because it places the MOS channel on the etched sidewalls. Additional real estate necessary for proper MOSFET operations, such as gate-to-source overlap and gate-to-contact metal gap, can also be placed on the sidewalls. Such design can result in a huge increase in gate packing density,

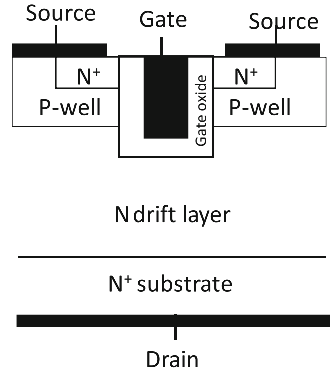


**Fig. 2.14** Simplified cross section of a SiC trench MOSFET

and associated gate-to-source capacitance which is a highly desirable feature for high-speed switching power applications since it improves immunity of the power MOSFET to self-turn-on during a high *dv/dt* turn-off event. However, the associated increase in gate-to-drain capacitance has to be avoided [103]. The first trench MOSFETs in silicon carbide, using 6H-polytype, were reported by Palmour et al. [104]. The first trench MOSFETs in 4H-SiC were also demonstrated by Palmour et al. [105].

It was also experimentally demonstrated that the MOS channel mobility can be significantly higher on the etched sidewall compared to the Si-face of 4H-SiC [106] due to the anisotropic SiC mobility. The simplified trench MOSFET structure shown in Fig. 2.14 does not have a JFET region, which also helps reducing the on-resistance. It is expected that a well-optimized 4H-SiC trench MOSFET structure can offer significantly lower on-resistance compared to a 4H-SiC DMOSFET with the same voltage rating.

The simple trench MOSFET structure, shown in Fig. 2.14, works very well in silicon, since the breakdown electric field for $SiO_2$ is two orders of magnitude greater than that of silicon; hence, oxide breakdown is not an issue in silicon devices. However, the breakdown electrical field of 4H-SiC is only about three times lower than the theoretical breakdown electrical field of $SiO_2$. The electrical field increases further at the $SiO_2$/SiC interface by more than a factor of 2 due to the difference in dielectric constant between the two materials. This represents a huge reliability issue of 4H-SiC trench MOSFETs. For reliable operation, the gate oxide at the trench bottom must be properly shielded from the high voltage during the off-state. Figure 2.15 shows a 4H-SiC trench MOSFET structure with a p-type implanted in the bottom of the gate trench [107–109]. The p-shielding region was connected to the source region and provided excellent protection to the gate oxide at the bottom of the trench. It should be noted that this p-type protection layer and the p-base of the trench MOSFET can form a very narrow JFET region, which can add significant amount of JFET resistance, increasing the total on-resistance of the structure. This issue was addressed by placing a thin, heavier doped n-type current spreading layer (CSL) beneath the p-well layer

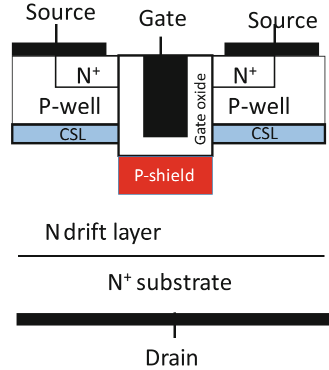


**Fig. 2.15** SiC Trench MOSFET structure with trench bottom protection implants

[107]. It should be noted that the gate-to-drain capacitance is very small. However, switching losses will be very high if the resistance between the protection p-region and source is extremely high. Device layout must be optimized for this structure to achieve optimal on-state and switching performances [109]. Figure 2.16 shows a 4H-SiC trench MOSFET structure with double-trench protection approach [110]. The bottom of the gate trench was shielded by a deeper source trench. The distance between the gate trench and protection trench was approximately 2 μm in [110]. The MOS channel mobility on the etched sidewall was 11 $cm^2/(V·s)$, which was considerably lower than that expected for a trench MOSFET in 4H-SiC. With this structure, a specific on-resistance of 0.79 $m\Omega·cm^2$ was achieved for a 630 V 4H-SiC trench MOSFET, and an on-resistance of 1.41 $m\Omega·cm^2$ was achieved for a 1260 V trench MOSFET, respectively. Figure 2.17 shows a 4H-SiC trench MOSFET structure with asymmetric protection implants. In this device, only one side of the trench sidewall is used as MOS channel, which is exactly aligned to the <1120> crystal plane [111]. The deep p-wells are used to limit the electric field in the gate oxide at the bottom and the corners of the trench. This cell structure has a small ratio of the Miller charge ($Q_{GD}$) to gate-source charge ($Q_{GS}$). It should be noted that this structure adds significant amount of JFET resistance. However, the added JFET regions resulted in reduced saturation currents, which improved the short-circuit withstand time ($t_{scwt}$).

A last point on SiC UMOSFETs related to the interface states. The etched sidewalls of 4H-SiC trench MOSFET/UMOSFETs) have lower density of interface states ($D_{it}$) closer to the conduction band edge than the Si-face of 4H-SiC. However, the a-face has significantly more midgap states, which may not impact the MOS channel mobility, but result in significant subthreshold hysteresis [112]. A preconditioning routine is required to measure threshold voltage from 4H-SiC trench MOSFET. This may not impact the device reliability or stability [112]. However, it is preferred to minimize the hysteresis for easier control of the devices. Further developments in MOS surface passivation techniques are needed to minimize interface trap density across the bandgap of 4H-SiC.

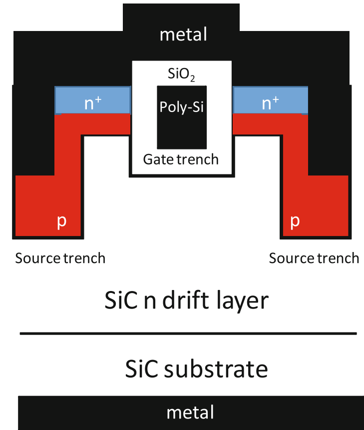


**Fig. 2.16** SiC trench MOSFET structure with double-trench protection

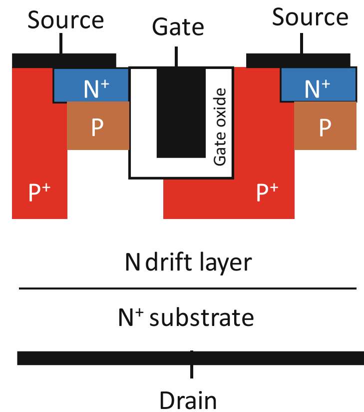


**Fig. 2.17** SiC trench MOSFET structure with asymmetric protection implants

## 5.4 *4H-SiC Superjunction MOSFETs*

Superjunction (SJ) MOSFETs in 4H-SiC were also demonstrated. The first published approach used multiple implants and epiregrowth steps to form vertical SJ structures [113–115]. Dopant diffusion cannot be utilized in the fabrication of SJ structures in 4H-SiC due to negligible diffusion coefficients in 4H-SiC [113]. Hence, for this type of approach, the SJ drift layer requires several iterations of thin epigrowth and ion implantations. Cross-sectional images of 1200 V class 4H-SiC SJ trench MOSFETs, with a pitch of 5 and 2.5 μm, are shown in Fig. 2.18 [116]. The signs of multiple epigrowths and p-type implantations are clearly visible in the image. As mentioned above, on-resistances of 4H-SiC MOSFETs, with blocking voltage less than 3.3 kV, are dominated by parasitic resistances, which include MOS channel resistance. For this reason, a 1200 V class SiC SJ MOSFET did not show any on-resistance advantage over conventional structure SiC power MOSFET at room temperature, as shown in Fig. 2.19 [114, 117]. However, the

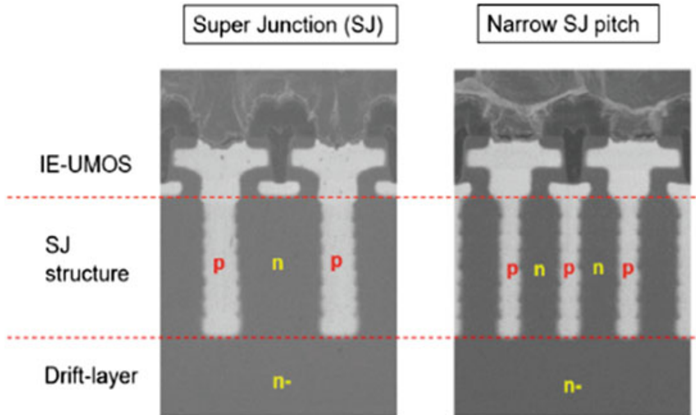


**Fig. 2.18** Cross-section of 1200 V class 4H-SiC SJ trench MOSFET [116]

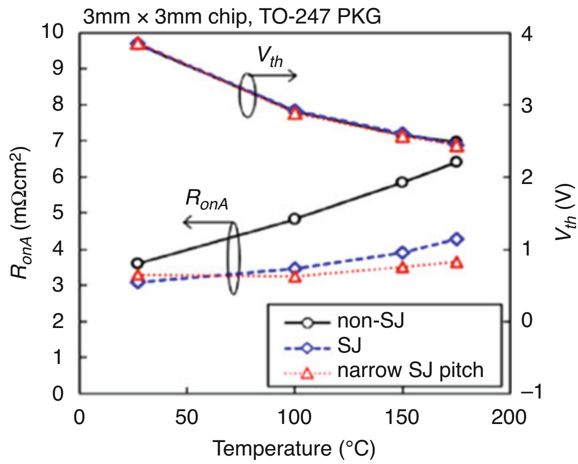


**Fig. 2.19** $R_{ds,on}$ as a function of temperature for SiC SJ MOSFET, compared to a conventional SiC MOSFET [115]

SJ MOSFETs showed significantly lower on-resistance at elevated temperatures, where the MOS channel resistance reduces due to a reduction on threshold voltage, and drift resistance increases due to a decrease in bulk mobility. SJ devices showed significantly smaller rate of increase in on-resistance over temperature compared to the conventional device. The SJ device with tighter pitch and higher drift doping concentration showed smaller rate of increase compared to the SJ device with larger pitch.

The benefits of the SJ structure are greater for higher voltage (>6 kV) devices, where drift layer resistance becomes more dominant. Multiple regrowth approach used for 1200 V class SiC SJ MOSFETs is not feasible for high-voltage devices due to manufacturing costs associated with the approach. For such thick SJ structures, "trench etch and refill" approach is more reasonable. A 6.5 kV 4H-SiC MOSFET with partial SJ structure, with 23-μm-thick SJ region and 41-μm-thick,

$2 \times 10^{15}$ cm$^{-3}$ doped drift region was experimentally demonstrated [118]. A trench pitch of 5 μm was used. For proper epi-fill of the trenches, the trenches must be precisely aligned to <11–20> direction. 4H-SiC power DMOSFET structure with a cell pitch of 10 μm was built on the SJ drift layer to complete the fabrication of the device. The completed 4H-SiC partial SJ MOSFET showed an on-resistance of 17.8 mΩ·cm$^2$ with a blocking voltage of 7.8 kV, which is significantly lower than the theoretically predicted drift resistance of a 7.8 kV 4H-SiC unipolar device with conventional structure.

## 6 SiC IGBTs

Ultrahigh-voltage (>10 kV) 4H-SiC MOSFETs have very high specific on-resistance, which leads to very large die size, resulting in increased manufacturing costs and gate drive requirements. Bipolar devices utilizing conductivity modulation to reduce drift region resistivity, such as SiC IGBTs, can be introduced to alleviate this issue. As shown in Figs. 2.20 and 2.21, SiC power MOSFETs have unipolar drift conduction, which is limited by the doping concentration of the drift layer. On-resistance and, consequently, forward voltage drop ($V_{ON}$), increases with temperature due to decreases in bulk electron mobility with temperature. On the other hand, SiC IGBTs depend on conductivity modulation achieved by injection of excess carriers, which significantly reduces drift region resistivity of the device, which reduces further at elevated temperatures due to enhanced charge injection and increased carrier lifetime.

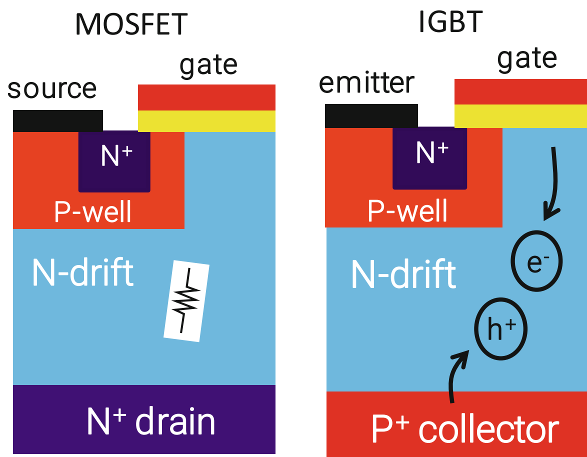


**Fig. 2.20** SiC MOSFET and SiC IGBTs

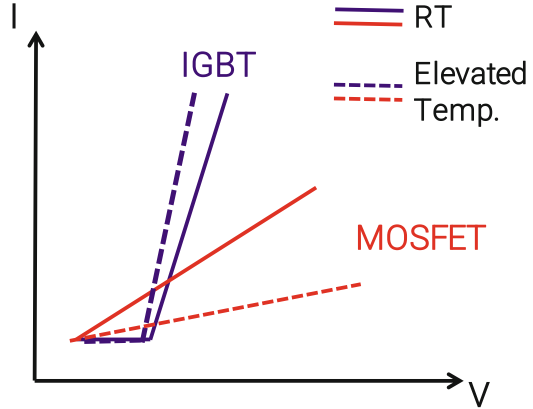


**Fig. 2.21** On-state behavior of SiC MOSFETs and IGBTs

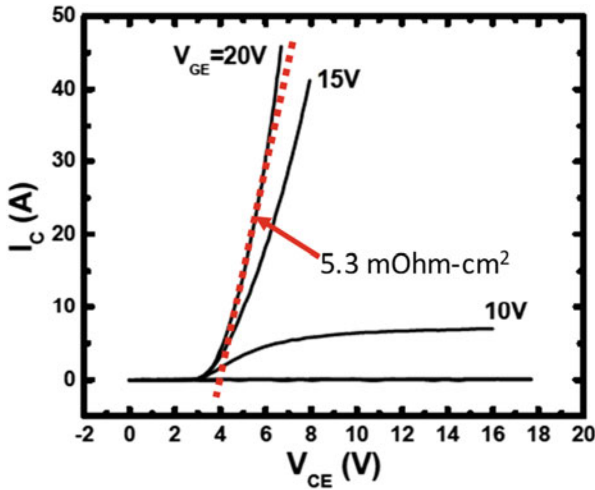


**Fig. 2.22** Representative *I-V* characteristics of a 12 kV 4H-SiC IGBT. The chip size was 6.7 × 6.7 mm, with an active area of 0.16 $cm^2$

Figure 2.22 shows representative *I-V* characteristics of a 12 kV 4H-SiC n-IGBT [119]. The device used a 140-μm-thick, $2 \times 10^{14}$ $cm^{-3}$ doped drift layer, with a 6.7 × 6.7 mm device area (0.16 $cm^2$ active). A differential specific on-resistance of 5.3 mΩ·$cm^2$ was reported with a gate bias of 20 V at room temperature. This is significantly lower than those of 10 kV SiC power MOSFETs, which showed a specific on-resistance of around 100 mΩ·$cm^2$ [120].

Due to the excess carrier injection and associated increases in diffusion capacitance, switching speed of the 4H-SiC IGBTs is significantly slower, which limits the usable switching frequency of the device. The maximum controllable current in a hard switching application, with 50% duty cycle, was compared for the 15 kV 4H-SiC power MOSFETs and the 15 kV 4H-SiC n-IGBTs (see Fig. 2.23) [120,

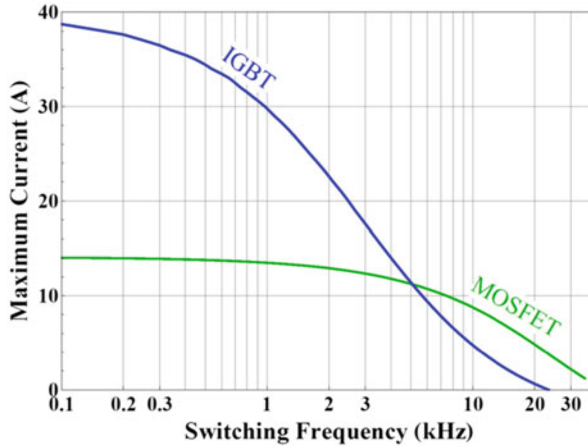


**Fig. 2.23** Comparison of maximum controllable currents for the 15 kV 4H-SiC power MOSFETs and the 15 kV 4H-SiC n-IGBTs in a hard switching application

121]. A power dissipation density of 300 W/cm$^2$, a chip size of 8 × 8 mm (32 mm$^2$ active), and a supply voltage of 10 kV were assumed. A 15 kV SiC n-IGBT with a 5-μm-thick field-stop (FS) buffer layer with fast turn-off time was used for this comparison. At switching frequencies lower than 5 KHz, 4H-SiC n-IGBTs offer more advantage, showing up to 2.8 times the controllable current compared to 4H-SiC power MOSFETs. At higher switching frequencies, the 4H-SiC MOSFET has the advantage, showing 1.8 times the controllable current over the 4H-SiC n-IGBTs at 10 kHz.

The use of thick drift layer with extremely light doping concentration enables the increase of blocking capability of 4H-SiC IGBTs to beyond 20 kV [122]. A 4H-SiC IGBT, using a 230-μm-thick drift layer with a doping concentration of $2.5 \times 10^{14}$ cm$^{-3}$, demonstrated a blocking voltage of 27.5 kV, which is the highest blocking voltage for a solid-state switching device reported to date [123]. The device had a die area of 0.81 cm$^2$ (0.28 cm$^2$ active). The drift layer received a lifetime enhancement oxidation at 1300 °C for 15 hours, and a $V_{ON}$ of 11.8 V at a collector current of 20 A (approximately 71 A/cm$^2$) at 25 °C. Recently, a 4H-SiC n-IGBT using 230-μm-thick drift layer with a doping concentration of $2.0 \times 10^{14}$ cm$^{-3}$ was reported [124]. This device showed a blocking voltage of 26.8 kV. Carbon implantation and subsequent annealing processes were employed for carrier lifetime enhancement. A $V_{ON}$ of 8.2 V at a current density of 100 A/cm$^2$ and a differential specific on-resistance of 36.9 mΩ·cm$^2$ were measured at room temperature.

Further improvements in 4H-SiC IGBTs can be achieved by enhancing the amount of carriers (both holes and electrons) in the top region of the structure [125]. Several approaches were proposed and used in silicon, including the use of cell designs with wide distance between the cells (IEGT) [126], forming micro trench and floating cells [127], and employing carrier storage layer (CSL), which

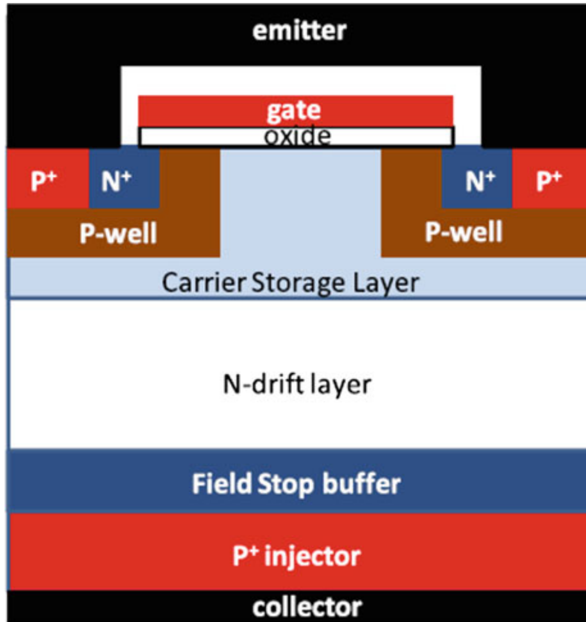


**Fig. 2.24** A simplified cross section of a 4H-SiC IGBT, with carrier storage layer (CSL)

is a moderately doped n-type layer placed near the blocking junction [128]. IEGT approach is not suited for 4H-SiC IGBTs due to gate reliability issues caused by high electric field in 4H-SiC and lack of gate shielding in IEGT structure. Moreover, the use of floating cells is not favored in 4H-SiC IGBTs because of the low MOS channel mobility in 4H-SiC. However, 4H-SiC IGBT cell design can be optimized to utilize the CSL concept without compromising gate reliability (Fig. 2.24). The 4H-SiC IGBT without CSL layer showed a positive temperature coefficient in $V_F$ due to high JFET resistance and lack of topside injection. The addition of CSL significantly reduced the JFET resistance and improved electron injection from the topside, resulting in negative temperature coefficient in $V_{ON}$, as shown in Fig. 2.25 [129]. It was also reported that heavier CSL doping concentration results in further reduction in $V_{ON}$ [129].

## 7 III-Nitrides Power Devices

Gallium nitride (GaN) is a polar III-nitride semiconductor with a wide and direct bandgap. Due to this unique combination of highly attractive material properties, GaN has obtained significant commercial and research interest for a broad spectrum of applications, ranging from optoelectronics (e.g., displays and lighting) to high-frequency electronics (e.g., telecommunications and radar) to power electronics

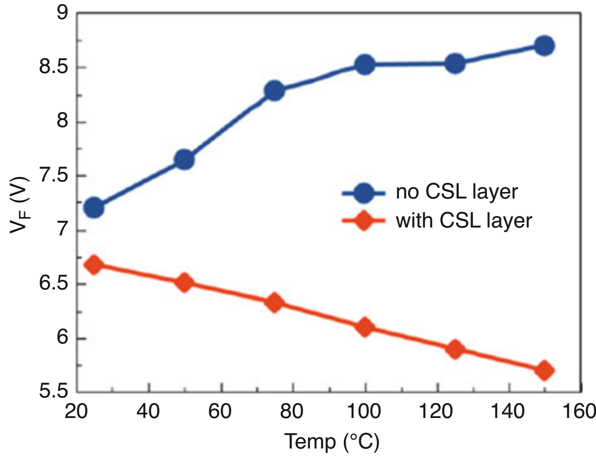


**Fig. 2.25** Forward voltage drop of 15 kV 4H-SiC n-IGBTs, with and without CSL layers. $V_{GE}$ was fixed at 20 V, and an $I_C$ of 20 A was used for the measurements

(e.g., battery chargers and electric motor drives). This diverse ecosystem has driven rapid innovation, with advances in one application space subsequently supporting another, and vice versa. In what follows, the focus will be placed on the development of GaN devices for power electronics.

According to the Baliga Figure of Merit (BFOM), which provides a measure of a semiconductor's performance in the drift region of a vertical unipolar power device (e.g., Schottky diode), GaN can outperform conventional silicon (Si) by approximately 4000 times and silicon carbide (SiC) by approximately six times. In other words, for a given breakdown voltage and current rating, GaN devices have a significantly lower specific on-resistance ($R_{ON}$) and area. The latter also permits them to be driven at larger frequencies, which further reduces losses and necessitates smaller passive components, in turn shrinking the size and weight of the overall power module. The abovementioned BFOM predictions stem from the properties of bulk GaN, in particular its large critical electric field ($E_C$), which is linked to its wide bandgap, as well as its mobility. However, early challenges associated with manufacturing native GaN substrates steered the community away from vertical devices and spurred interest in developing lateral GaN devices on foreign substrates, such as sapphire, SiC, and Si. Consequently, it was understood that the polar nature of III-nitrides in conjunction with the use of heterojunctions (e.g., AlGaN/GaN) can be harnessed to form highly conductive channels. These heterojunctions lie at the core of GaN high-electron mobility transistors (HEMTs), which now possess record-breaking speed and power, and are the most technologically and commercially mature GaN-based power device available today. Thus, the text that follows will begin by discussing these devices. Vertical GaN devices, which have more recently been the target of resurgent attention, will then be explored, followed by an examination of future opportunities for GaN and III-nitride power devices.

## 7.1 Lateral GaN HEMTs

While a number of GaN-based lateral transistor topologies are technically possible, the undisputed winner is the HEMT. Very recently, the GaN HEMT has been commercialized in the 15–650 V classes [2], and its market size is projected to exceed $1.25 billion by 2027 [130]. Owing to GaN's superior physical properties over Si and SiC for power applications, GaN HEMTs allow for higher switching frequency and therefore, have already seen wide adoptions in fast chargers, wireless charging, data centers, and electrified transportation. In addition, GaN HEMTs can accommodate various substrates, e.g., Si, sapphire, SiC, and GaN. Most commercial GaN HEMTs for power electronics rely on large-diameter GaN-on-Si, and their process is CMOS-compatible, enabling a similar material and processing cost as compared to SiC power devices [131].

At the heart of the GaN HEMT is a heterojunction that provides a quasi-two-dimensional channel with high-electron density ($N_S$) and mobility ($\mu$), i.e., the two-dimensional electron gas (2DEG) channel. Unlike GaAs HEMTs, the 2DEG in GaN HEMTs forms without the need for any extrinsic dopants. As shown in Fig. 2.26, when a thin aluminum gallium nitride (AlGaN) layer (typically 5–30 nm thick) is grown on top of a thicker GaN layer, a 2DEG with $N_S \sim 10^{12}$–$10^{13}$ cm$^{-2}$ forms below the AlGaN/GaN hetero-interface due to polarization fields and donor-like surface states [132, 133]. Electrons are vertically confined within a thin triangular potential well, allowing for a high mobility of 1500–2000 cm$^2$/(V·s). Note that the 2DEG can be formed in numerous combinations of group III-nitride heterostructures, and the AlGaN/GaN is the most popular heterostructure of choice. The 2DEG is a unique feature not available in Si and SiC technologies. It is the combination of high current densities obtainable via the 2DEG and the large $E_C$ of GaN that make it such an attractive power device, despite the lateral configuration. It is also worth noting that the 2DEG forms without the application of a gate bias, meaning that GaN HEMTs are inherently depletion mode (D-mode) or normally-on devices. While this makes them directly usable for power amplifiers in telecommunications applications [134, 135], power electronics require normally-off or enhancement mode (E-mode) operation. Methods to satisfy this requirement are explored below.

## 7.2 Commercial and R&D Devices

Currently, four main structures are adopted in commercial power GaN HEMTs, as illustrated in Fig. 2.27. While all of commercial devices employ the 2DEG channel, main difference between them lies in the gate stack, or more specifically the techniques to enable enhancement-mode (E-mode) operation, which is highly desirable for power electronics applications [136]. The Schottky-type p-gate HEMT (SP-HEMT) (Fig. 2.27a) and gate injection transistor (GIT) (Fig. 2.27b) [137] both

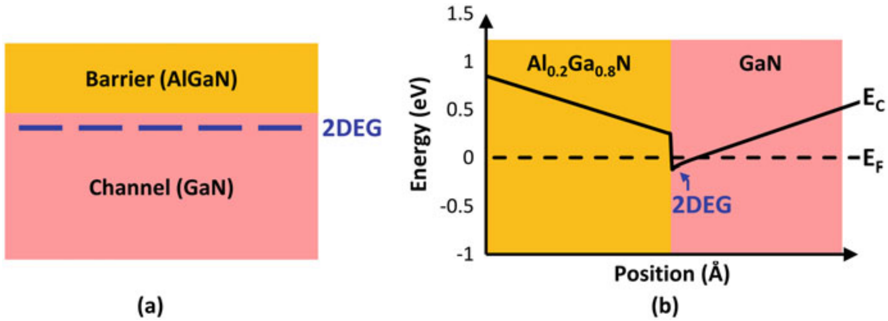


**Fig. 2.26** (**a**) Schematic cross section of a heterojunction consisting of an AlGaN barrier layer and GaN channel layer. (**b**) Energy band diagram across the AlGaN/GaN heterojunction demonstrating the formation of a two-dimensional electron gas (2DEG) within the GaN layer characterized by large mobility and sheet carrier density

use p-GaN to deplete the 2DEG under the gate, but they feature different contacts between the gate metal and p-GaN. The recessed gate and ohmic gate contact in the GIT favor the hole injection and conductivity modulation, which are not present in the SP-HEMT. Given the large voltages that these devices are expected to block, field management is critical. As shown, field plates are often used to suppress field crowding. The cascode (Fig. 2.27c) and direct-drive devices usually co-package a high-voltage D-mode GaN HEMT with a low-voltage E-mode Si power MOSFET to make the composite device function like a single high-voltage E-mode transistor [138]. Direct-drive devices also co-package the gate driver and protection Si ICs with the GaN HEMTs [139].

Despite their success, the performance of commercial GaN devices has not yet reached the predicted material limit. In the last few years, two emerging GaN devices, i.e., the FinFET and trigate device as well as the multichannel device, have arguably been among the most innovative and promising lateral GaN power devices. The GaN FinFET and trigate devices have been comprehensively reviewed in [140]. As shown in Fig. 2.28a, these nonplanar GaN devices take advantage of the multi-gate fin channels to improve the gate controllability. Very different from Si FinFETs, GaN FinFETs and trigate devices have many structural innovations, such as wrapping around 2DEG channels with the MIS stack [141] or the p-n junction [142]. The superior gate controllability has not only allowed higher current on/off ratio, steeper threshold swing, and suppression of short-channel effects, but also E-mode operation, on-resistance reduction, current collapse alleviation, and enhanced thermal management [140].

Recently, the large-diameter wafer with multiple, vertically stacked 2DEG channels becomes available. This multichannel wafer allows for a sheet resistance below 120 Ω/sq, i.e., at least three times lower than that of a single 2DEG channel [143]. Despite a much lower $R_{ON}$ of multichannel devices, it is challenging to manage the

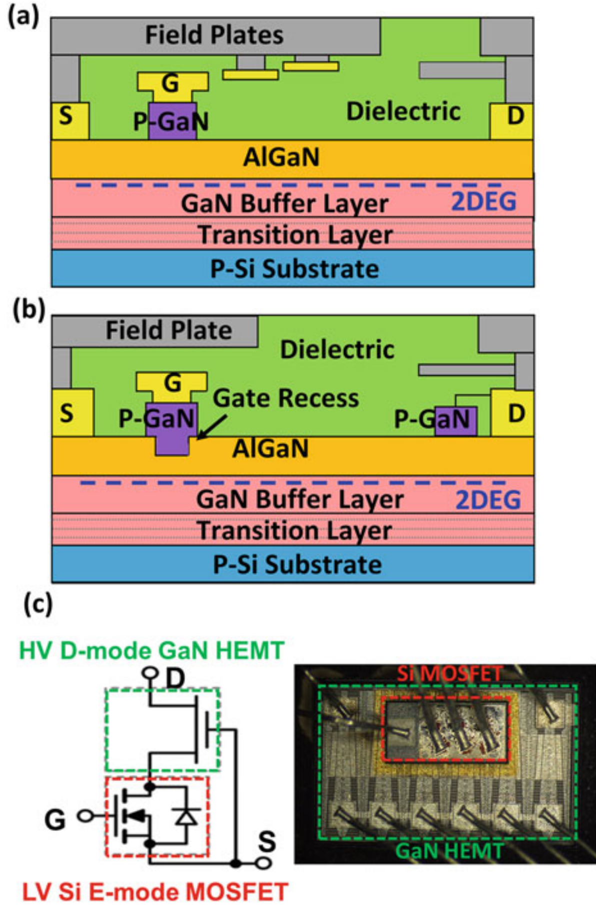


**Fig. 2.27** Schematic of (**a**) SP-HEMT, (**b**) GIT, and (**c**) cascode GaN HEMT. (A de-capped device photo is shown in (**c**), which is adapted from [139])

electric field crowding at high reverse biases due to high volume charges. Various structures, e.g., trigate [144], p-GaN termination [143], 3-D junction fin [145], and reduced surface field cap layer [146], have been developed in multichannel rectifiers, which enabled their performance to exceed the 1-D SiC limit up to a voltage class of 10 kV. For multichannel HEMTs, trigate [140] and monolithic-cascode [147] designs have been innovatively applied; the monolithic-cascode device (Fig. 2.28b) demonstrates the E-mode operation with a performance surpassing SiC up to 10 kV [148].

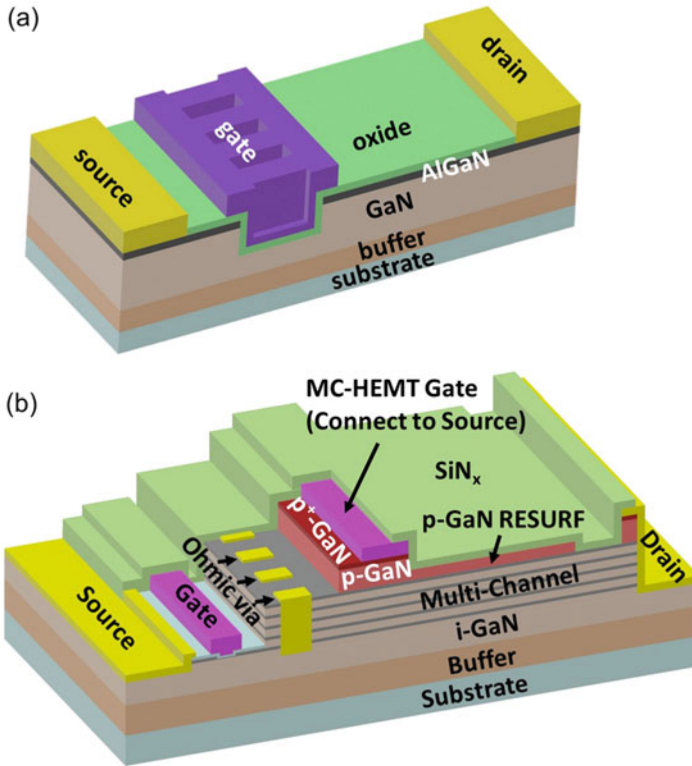


**Fig. 2.28** Schematic of (**a**) trigate GaN HEMTs and (**b**) multichannel monolithic-cascode GaN HEMTs. ((**a**) is adapted from [142], and (**b**) adapted from [147])

## *7.3 Discrete Device Packaging*

The aforementioned innovations in GaN HEMT design and chip manufacturing make it possible to push the limits of output power and switching frequency, in turn demanding careful consideration at the package level. As the junction temperature ($T_J$) increases, $R_{ON}$ increases and transconductance ($g_m$) decreases, which contribute to increased conduction and switching losses, respectively. If left unchecked, self-heating can lead to thermal runaway and a catastrophic failure of the device. To combat these problems, thermal management and hot spot evaluation of GaN HEMTs have been extensively studied using a variety of electrical and optical techniques [148, 149]. Most commercial products call for a maximum junction temperature of approximately 150 °C for reliable operation, as defined by JEDEC standards [150].

In lower-frequency applications, well-established through-hole, lead frame packages (Fig. 2.29a), such as TO-220 and TO-247, can be used. An example of a TO-247 package is shown in Fig. 2.29b [151]. Within the package, the GaN

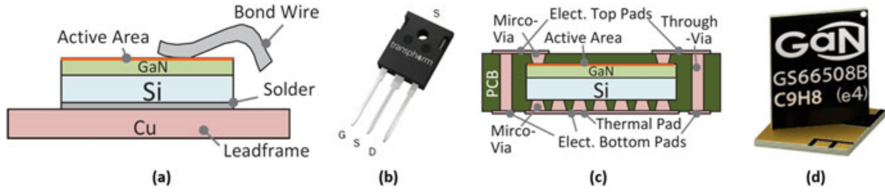


**Fig. 2.29** (**a**) Schematic cross section of a lead frame package. [153] (**b**) Picture of a commercial GaN HEMT in a lead frame package. [151] (**c**) Schematic cross section of a no-lead package with an embedded GaN HEMT. [153] (**d**) Picture of a GaN HEMT in a proprietary embedded package [154]

HEMT is attached to a thermally conductive substrate, such as a direct-bonded copper (DBC) substrate. Electrical connections to the leads are made via wire- or ribbon-bonding, as shown in Fig. 2.29c. Since one of the major advantages of GaN HEMTs is their high mobility, they are extremely well-suited for high-frequency applications. As the switching frequency of the application increases, however, the parasitic inductances associated with the bond wires and leads impede performance. As a first step toward mitigating parasitics, no-lead packages, such as the Power Quad Flat No Leads (PQFN) topology have been adopted. Within these packages, however, wire-bonds are still used. For highest-frequency performance, micro-vias or flip-chip bonding [152] can instead be employed to fully embed the chip within a multilayered package, as shown in Fig. 2.29c [153] and Fig. 2.29d [154]. Thermal management is achieved by strategically introducing thermal vias and novel materials with superior thermal conductivity. The small footprint of these packages drives down the size and weight of power modules, making them highly attractive for portable applications. Chip embedding also facilitates multi-chip and heterogeneous technology integration [155].

## *7.4 Robustness and Reliability*

The reliability and robustness challenges of GaN HEMTs come from not only the distinct device physics (e.g., the lack of p-n junctions between source and drain) but also the heterogenous GaN-on-Si epitaxy with a high dislocation density. Many issues regarding device stability, reliability, and robustness arise from the presence of traps in various regions of the epi structure. Trapping behavior is usually time-dependent. Hence, device characteristics in fast switching could significantly differ from the ones under DC conditions. A recent paper nicely overviews the relevant device physics and material issues [156]. As commercial GaN HEMTs have passed reliability qualifications, many recent studies emphasized on testing them in switching circuits to understand their robustness outside the safe operating areas.

The dynamic $R_{ON}$ phenomenon, where $R_{ON}$ immediately after device turn-on is higher than the DC value, is a well-known issue of GaN HEMTs that increases their

conduction losses in power converters. A decade of study has revealed its origins to be associated with buffer trapping, surface trapping, and gate instability [156]. After relentless efforts by the GaN community, this issue has been significantly alleviated. Steady-state switching measurements have shown the worst-case dynamic $R_{ON}$ of commercial GaN HEMTs to be less than two times higher than the static value [157].

Two major robustness metrics of a power transistor is the avalanche and short-circuit capabilities. The former evaluates the device's capability to pass a high avalanche current ($I_{AVA}$) at its avalanche breakdown voltage ($BV_{AVA}$) and thereby dissipate the circuit surge energy in device. GaN HEMTs have no avalanche capability and a destructive breakdown. The surge energy cannot be dissipated but induces a capacitive charging in GaN HEMTs, and they fail when the capacitive overvoltage reaches the transient BV [158]. More interestingly, this transient BV in fast switching was found to be dynamic and higher than the static BV measured in quasi-static *I-V* sweeps [159, 160]. This is attributed to the reduced buffer trapping in short pulses, where the buffer trapping intensifies the peak electric field and make it reach the critical electric field of GaN at lower drain biases [159]. Different from the standalone GaN HEMTs, the dynamic BV of cascode GaN HEMTs was found to be much lower than their static BV due to the internal Si avalanching [138].

Short-circuit robustness evaluates the device's capability of withstanding an abnormally high current in forward conduction and reverse blocking states for a certain time (usually required to be >10 μs) before the protection circuit intervenes [161]. The short-circuit robustness of GaN HEMTs is insufficient at a high blocking voltage. For example, the short-circuit withstand time of all 600/650 V rated commercial GaN HEMTs was found to be below 1 μs at a bus voltage of 400 V [162].

It is worth noting that the insufficient avalanche and short-circuit capabilities of GaN HEMTs are related to the HEMT device instead of the GaN material. In vertical GaN devices comprising p-n junctions, which will be introduced in Sect. 3, robust avalanche and short-circuit capabilities have been demonstrated. For example, a reverse $I_{AVA}$ over 50 A [163] and forward surge current over 50 A [164] were reported in 1.2 kV vertical GaN p-n diodes; an avalanche energy comparable to Si and SiC devices has been demonstrated in vertical GaN fin-channel JFETs [165–167]. In the 650 V vertical GaN JFETs, a short-circuit withstand time over 30 μs has been reported at the 400 V bus voltage, with a short-circuit energy superior to SiC and Si MOSFETs [160].

Note that many of the above reliability and robustness challenges facing GaN HEMTs limit the further advancement of their performance. For example, due to the lack of avalanche capability, a larger voltage over-design is implemented in commercial GaN HEMTs as compared to Si and SiC MOSFETs [137, 157], which leads to larger specific on-resistance and offsets the inherent advantages of GaN devices. Addressing these challenges will not only facilitate GaN's applications but also bring considerable performance advancements to the device itself.

## 7.5 Approaches to GaN ICs

To take full advantage of the high switching speed of GaN HEMTs, it is necessary to minimize parasitic inductances between them and their gate driving circuits, which is desirably to be realized through monolithic integration. The E-mode/D-mode logic, which is also known as the direct coupled logic (DCL), has been employed to make the GaN HEMT-based driving circuits and integrate them with the high-voltage GaN power HEMTs [168]. Such GaN power ICs are already commercially available from companies such as Navitas Semiconductor, Power Integration, and EPC, and they have been widely used in consumer electronics systems such as fast chargers and wireless chargers.

A key limitation of the DCL-based power ICs is the high-power consumption and limited circuit design flexibility [136]. To overcome these issues, there has been extensive research on the GaN complementary technology comprising high-performance n-channel and p-channel GaN E-mode transistors [136]. For this, the key challenge is on the p-channel GaN transistor design. An early GaN CMOS demonstration employs p-channel GaN MOSFETs on a regrown epitaxial structure [169]. Later, it was proposed to utilize the p-GaN layer in standard p-gate GaN HEMTs to make the p-channel GaN transistors [170], which obviates the need for epitaxy regrowth. Subsequently, a regrowth-free GaN CMOS has been demonstrated [171].

Heterogeneous integration of GaN HEMTs with Si CMOS technology is another approach that is being pursued to enhance power and functionality. A prominent example is the use of oxide bonding at the wafer scale [172]. GaN HEMTs are first fabricated on 300 mm highly resistive Si wafers and then bonded to Si wafers. The second Si wafer is controllably removed using an etch stop layer, ultimately leaving behind single crystal Si, with which Si p-channel MOSFETs are fabricated. More recently, both Si NMOS and PMOS devices have been integrated with E- and D-mode GaN HEMTs [173] using this approach. Whereas the primary focus has been on power amplifier development thus far, the introduction of field management techniques that permit high-voltage operation would unlock several exciting opportunities in the power electronics space as well.

## 7.6 Vertical GaN Devices

### 7.6.1 Transistors

The vertical structure is often believed to favor high-voltage, high-power devices as it facilitates current spreading and thermal management [174] and allows for the realization of high voltage without enlarging the chip size. Additionally, as compared to GaN-on-Si, GaN-on-GaN homoepitaxial layers possess a much lower dislocation density, which favors the minimization of trapping effects. Over the

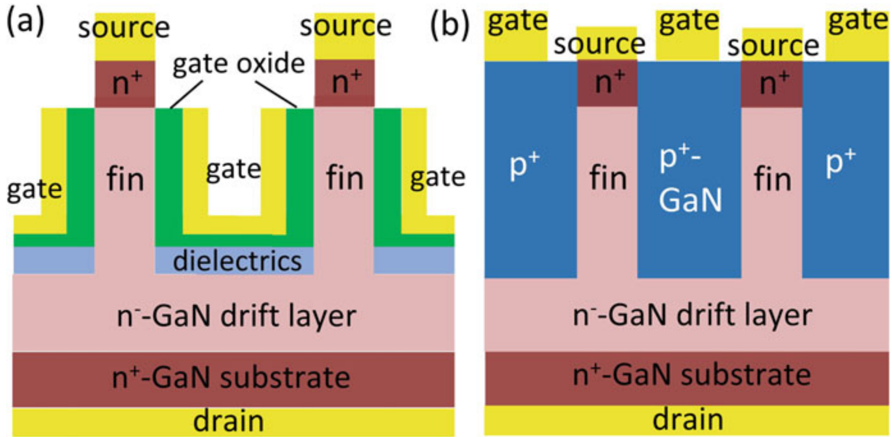


**Fig. 2.30** Schematic of (**a**) the vertical GaN Fin-MOSFET and (**b**) vertical GaN Fin-JFET [175]

last several years, the cost of GaN-on-GaN wafer is dropping fast, and 4-inch freestanding wafer is widely available now [131]. Several vertical GaN transistors with a voltage class over 1.2 kV have been demonstrated recently.

The vertical GaN FinFETs leverage the digital FinFET concept and employ the submicron-meter fin-shaped channels to provide superior gate control as well as enable the E-mode operation and bidirectional conduction. The small footprint of fin channels also allows for very high channel density and thereby low channel resistance. The development of this device concept as well as its application to other materials have been reviewed in [175] and [140]. Depending on the sidewall gate stack, there are two types of power FinFETs, the Fin-MOSFET (Fig. 2.30a) and Fin-JFET (Fig. 2.30b). In each fin, the Fin-MOSFET features a bulk fin channel in parallel with two sidewall accumulation-type MOS channels [176] and the device needs only n-type GaN. In the Fin-JFET, the inter-fin region is filled with p-GaN, and the strong depletion of the lateral p-n junction allows a high doping concentration in the fin while keeping the E-mode operation [165, 166]. 1.2 kV vertical GaN Fin-MOSFETs [177, 178] and Fin-JFETs [165, 166] have both shown three- to fivefold lower specific $R_{\mathrm{ON}}$ and superior switching performance [165, 178] as compared to 1.2 kV SiC MOSFETs. Industrial GaN Fin-JFETs for the first time demonstrates the avalanche capability in GaN transistors [165, 166] and have a record short-circuit robustness in GaN transistors [161]. The Fin-JFET also demonstrates a unique short-circuit robustness at a bus voltage close to its $\mathrm{BV}_{\mathrm{AVA}}$ [161], which was not reported in other devices.

The AlGaN/GaN current aperture vertical electron transistor (CAVET) is a unique transistor topology that seeks to leverage the highly conductive AlGaN/GaN heterostructure’s 2DEG with the voltage handling of a vertical drift region. Early demonstrations were conducted on sapphire substrates and relied on regrowth [179], but the more recent availability of native GaN substrates has improved material

quality and permitted the use of Mg implantation to form the current blocking layer (CBL) and consequently define the aperture [180]. Current challenges associated with both etch and regrowth as well as ion implantation limit the quality of the CBLs, as well as their interfaces with adjacent regions. Thus, trench CAVETs were also developed, both with MIS gate [181] and p-GaN [182] gate structures to provide E-mode operation. In the latter work [182], 1.7 kV/1.0 mΩ $cm^2$ devices were reported, which surpassed the SiC BFOM limit at this voltage rating, and represent the current state of the art for GaN CAVETs.

While the conventional DMOSFET and UMOSFET topologies have been readily adopted in both Si and SiC technologies, they remain difficult to realize in GaN. This is primarily due to a lack of a native, high-quality oxide that can be used in the gate structure. Poor GaN/oxide interfaces lead to poor channel conduction and channel inversion. The use of ALD and MOCVD dielectrics [183, 184] as well as UID GaN interlayer/oxide (known as the "OG-FET") [185] structures has been investigated at the gate, but the performance and reliability needed to displace SiC MOSFETs have yet to be achieved. An additional challenge is selective area p-type doping, which is needed to define the channel, contacts, and edge terminations. Recently, Mg implantation has been explored for this purpose [186], but progress in this space is still needed.

### 7.6.2 Diodes

Early studies of vertical GaN devices started from p-n diodes, as the p-n junction is a key building block for many advanced devices. Multiple groups have reported 3.3–5 kV GaN p-n diodes with a differential $R_{ON}$ *v.s.* $V_{BL}$ trade-off exceeding the 1-D SiC unipolar limit [187, 188]. In addition to the aforementioned avalanche and surge capabilities, a breakdown field of 2.8–3.5 MV/cm close to intrinsic GaN limits has also been reported in vertical GaN p-n diodes. As compared to SiC p-n diodes, industrial GaN p-n diodes show a comparable robustness but smaller reverse recovery and faster switching speed [165].

However, the vertical GaN p-n diode may not be competitive as a standalone rectifier due to the large turn-on voltage due to the GaN bandgap. Advanced Schottky barrier diodes (SBDs) are highly desirable, as they combine Schottky-like forward characteristics (small turn-on voltage) and p-n-like reverse characteristics (high breakdown field and low leakage current). These advanced SBDs include the trench MIS/MOS barrier Schottky (TMBS) diode, junction barrier Schottky (JBS) diode, and merged p-n/Schottky (MPS) diode. These diodes employ either the MIS stack or the p-n junction to deplete the top part of the drift region at low reverse biases, thereby shielding the top Schottky contact from high electric field. 600–700 V GaN TMBS diodes [189] and JBS diodes [190], as well as 2 kV MPS diodes [191], have exhibited at least 100-fold lower leakage current compared to standard SBDs. Toyoda Gosei reported an industrial 10 A, 750 V GaN TMBS diode operational at over 200 °C [192].

### 7.6.3 Vertical Devices on Foreign Substrates

In addition to freestanding GaN substrates, vertical GaN devices can be also fabricated on low-cost foreign substrates, such as Si, sapphire, and engineering substrates. The relevant studies date back to the first demonstration of vertical GaN-on-Si diodes using a quasi-vertical structure [193]. Fully vertical GaN-on-Si devices were later realized by various approaches to handle the insulative, defective transitional layers, including the layer transfer [194], buffer doping [195], and deep backside trenches [196]. The state of the art includes 500–800 V vertical GaN-on-Si diodes [196] and MOSFETs [197] as well as 1.4 kV vertical GaN-on-sapphire SBDs [198]. Regarding the cost and performance trade-offs, the higher dislocation density in GaN-on-Si was found to induce a relatively small degradation in forward characteristics but a higher off-state leakage current at high biases [199], at the same time bringing the material and processing cost by at least tenfold [131].

### 7.6.4 GaN Superjunction Devices

The SJ is arguably the most conceptually innovative and commercially successful device in Si, which relies on alternative n- and p-doped pillars and can break the theoretical trade-off between $R_{ON}$ and BV of 1-D drift regions [200]. The SJ has not reached experimental demonstrations in GaN. Instead of p-n junction, balanced polarization charges were used in lateral AlGaN/GaN devices to produce a "natural SJ" for superior E-field management [201]. However, their $R_{ON}$ is still much higher than the 1-D GaN limit (and even the SiC limit).

The recent experimental realization of selective p-type doping in GaN devices [165, 190] has shown the promise for fabricating GaN SJ devices. Selective p-GaN/2DEG junctions with a high blocking electric field have also been reported [202]. Simulations predict that vertical GaN SJ transistors with fin channels and 2DEG channels can enable at least 20-fold smaller switching charges as compared to today's transistors and allow multi-MHz, multi-kilovolts power switching [203].

A novel approach to realizing the GaN SJ involves the use of the lateral polar junction (LPJ), wherein neighboring n-type and p-type pillars are formed by the simultaneous growth of selectively doped N-polar and Ga-polar GaN [204]. Recently, charge balance between neighboring pillars, a critical design requirement in any SJ, was demonstrated with this approach [205]. Steps forward are also being made to reduce background doping in N-polar GaN, which is needed to achieve large blocking voltages. Given the progress being on all fronts, we believe the demonstration of a GaN SJ will arrive soon.

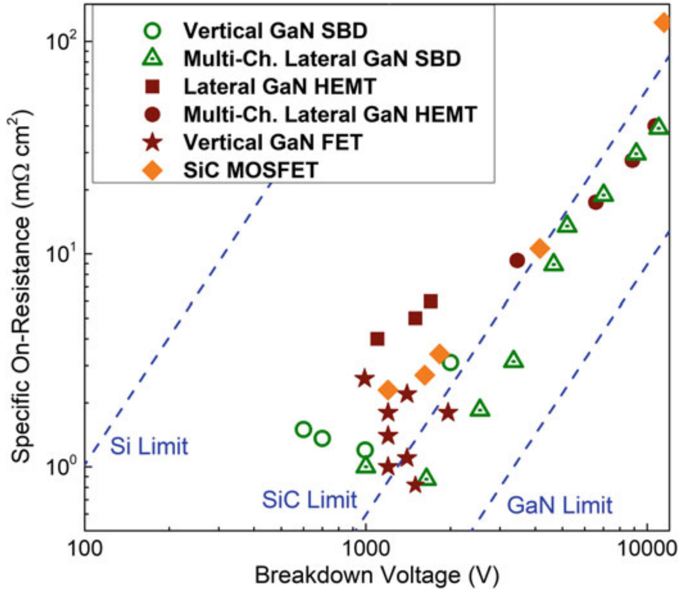


**Fig. 2.31** On-resistance versus breakdown voltage trade-offs of the state-of-the-art GaN Schottky barrier diodes and power transistors as well as SiC power MOSFETs

## *7.7 Outlook: Research Opportunities*

GaN technology has developed rapidly in the last decade, as evidenced by the significant commercial and research investments made for power electronics. Figure 2.31 shows the on-resistance versus breakdown voltage trade-offs of the state-of-the-art GaN Schottky barrier diodes and power transistors as compared to SiC power devices. The performance of commercial GaN HEMTs is between the Si and SiC theoretical limits, and many emerging GaN devices, particularly the vertical and multichannel lateral GaN devices, have shown performance exceeding the 1-D SiC theoretical limit. This suggests a good promise of expanding the GaN's application space in power electronics through device innovations. In the meanwhile, the state-of-the-art GaN device performance is still inferior to the 1-D unipolar GaN limit, suggesting room for further improvement. While many opportunities for future progress have already been presented in the preceding discussion, this section provides more detail on some of the most exciting research trends that lie ahead for GaN and III-nitrides more generally.

### 7.7.1 Selective Area P-Type Doping

Selective area doping is a critical process technology for both vertical and lateral power devices, including JBS diodes, MOSFETs, JFETs, and SJ devices. In Si and SiC technologies, efficient implantation of both donor and acceptor impurities has been established for this purpose. Beyond the formation of the device's active area, ion implantation is also relied on to create efficient edge terminations, such as guard rings and junction termination extensions [206]. While Si implantation is available for n-type doping of GaN, the ability to selectively form p-type GaN regions remains critical and elusive. Etch and regrowth process has been explored extensively, but is often limited by defects at the etched interface [179, 207–210]. Very recently, encouraging results have emerged using proprietary methods for etch and regrowth, which have enabled avalanche breakdown to be observed in vertical 1.2 kV GaN JFETs [166].

Mg implantation for selective area p-type doping has also been pursued for a long time, since it is expected to offer high-quality interfaces, reduced processing steps, and greater control over doping profiles. The principle challenge is suppressing decomposition of the surface at the high annealing temperatures (>~1100 °C) [211] needed to activate the Mg ions and repair the crystal damage introduced by implantation. Several annealing techniques have been proposed to activate Mg-implanted GaN while avoiding surface decomposition. Pulsed techniques such as multicycle rapid thermal annealing (MRTA) [212], gyrotron microwave annealing [213], and laser annealing [214] have successfully suppressed surface decomposition. However, the reported activation ratios are quite low (e.g., ~0.5–8%) [190, 212, 213], which limits their practical adoption. Ultrahigh-pressure annealing (UHPA) is another strategy, which calls for an $N_2$ ambient pressure of >300 MPa to stabilize the surface during the anneal. Most importantly, experimental results have shown that ~100% activation of the implanted Mg can be achieved with UHPA [215], though significant Mg diffusion has also been observed [216]. GaN PN junctions with kV-level blocking voltages have been recently reported with this technique [217]. How this technology develops, in particular for use in devices with even larger blocking voltages (i.e., >5 kV), could have a major impact on future generations of vertical GaN devices.

### 7.7.2 High-Voltage GaN Devices

As current GaN HEMTs are mainly commercialized in the low-voltage range (<650 V), there has been a popular belief that GaN devices are suitable only for low-voltage applications. Contrary to this popular belief, GaN rectifiers [146] and E-mode HEMTs [147] have been demonstrated up to 10 kV with the performance beyond the 1-D SiC unipolar limit. These results suggest that material and device landscapes for the $5 billion medium-voltage (1–35 kV) power electronics market could be reshaped, and multi-kilovolt GaN devices are very promising for applications like electric grid and renewable energy processing. From the device

architecture point of view, both vertical GaN devices and multichannel lateral devices are promising candidates of the medium- and high-voltage GaN switches, as they address the challenges facing the conventional single-channel HEMTs for voltage upscaling and power upscaling (e.g., crowding current and electric field distributions, limited current capability). Looking forward, numerous research opportunities exist in physics, materials, and devices for multi-kilovolts GaN power devices, as well as reliability, robustness, and converter applications.

### 7.7.3 N-Polar GaN HEMTs

The band diagram for the GaN HEMT provided in Fig. 2.26 assumes the use of Ga-polar or Ga-face GaN. While it was understood early on by the community that a 2DEG could also be formed in N-polar GaN [132], virtually all GaN HEMTs reported in the literature have been based on Ga-polar technology due to its superior chemical and thermal stability of N-polar GaN [218]. Advancements in surface roughness, doping control, and in situ passivation of N-polar GaN have renewed interest in N-polar GaN. This is because the two-dimensional electron gas (2DEG) is formed with an AlGaN back-barrier because of the opposite polarization field. The consequence of this is a reduced contact resistance for the source and drain, as well as easier gate length scaling. For RF applications, N-polar GaN HEMTs have been experimentally demonstrated to outperform Ga-polar GaN HEMTs [219]. An initial report of an N-polar GaN/AlGaN HEMT on sapphire achieved a breakdown voltage of 2 kV and state-of-the-art dynamic $R_{on}$ compared to Ga-polar GaN HEMT competitors [220]. Additional performance gains are expected after transitioning to Si or SiC substrates, as well as via improvements to the surface passivation.

### 7.7.4 UWBG III-Nitrides

Due to the cubic dependence of the BFOM on the critical electric field ($E_C$) of a material, there has been a large push to develop ultra-wide bandgap (UWBG) semiconductors for power devices [221]. This is clearly visualized in Fig. 2.32a. Among these, $Al_xGa_{1-x}N$ is a III-nitride semiconductor that shares many similarities to GaN, such as piezoelectric properties and a direct bandgap, and it can be grown on single crystal AlN substrates with a state-of-the-art dislocation density <$10^4$ $cm^{-2}$ [222]. For reference, if 100% Al composition (i.e., AlN) is used, the BFOM is predicted to yield an up to 34- or 80-fold increase in the BFOM over GaN and SiC, respectively, resulting in significant loss reductions.

To study the voltage handling capability of Al-rich AlGaN, $Al_{0.85}Ga0_{.15}N/Al_{0.6}Ga_{0.4}N$ HEMTs were recently fabricated on native AlN substrates [223]. The HEMT structure consists, bottom to top, of an unintentionally doped (UID) AlN layer, a 300 nm $Al_{0.6}Ga_{0.4}N$ channel layer, and a 20 nm UID $Al_{0.85}Ga_{0.15}N$ barrier layer. The upper 150 nm of the $Al_{0.6}Ga_{0.4}N$ channel layer is doped with Si at $5 \times 10^{17}$ $cm^{-3}$. The channel layer was doped instead of the barrier layer to avoid

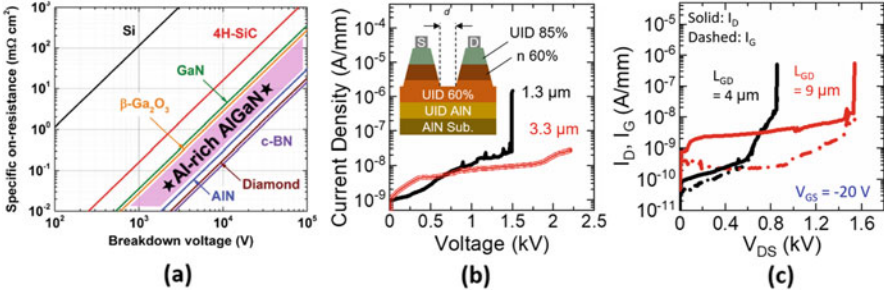


**Fig. 2.32** (**a**) Trade-off of on-resistance vs. breakdown voltage for different semiconductor technologies per the BFOM. (Modified from [221]). (**b**) Two-terminal mesa breakdown characteristics for an UID $Al_{0.6}Ga_{0.4}N$ layer grown on native AlN substrate. (**c**) Three-terminal breakdown characteristics of $Al_{0.85}Ga_{0.15}N$/ $Al_{0.6}Ga_{0.4}N$ HEMT for $L_{GD}$ of 4 and 9 μm. The $L_{SG}$ and $L_G$ are 1.5 μm each and $V_{GS}$ is −20 V [223]

high gate leakage while simultaneously facilitating ohmic contact formation. The cross-sectional schematic of the resulting mesa test structure is shown in the inset of Fig. 2.32b, which shows the two-terminal mesa breakdown characteristics for two mesa separations (*d*): 1.3 and 3.3 μm. Fluorinert was used to prevent premature breakdown. At 1.3 μm separation, UID $Al_{0.6}Ga_{0.4}N$ layer breaks down at ~1500 V, which corresponds to a breakdown electric field of 11.5 MV/cm. For context, this breakdown field is ~2× and ~4× higher than that previously observed in the UID AlN buffer mesa breakdown field in AlN/$Al_{0.5}Ga_{0.5}N$/AlN HEMTs [224] and AlN MESFETs [225], respectively. The structure with 3.3 μm separation was measured up to the upper limit of the testbench used (2.2 kV) and did not break down. The three-terminal HEMT breakdown characteristics for two different gate-to-drain ($L_{GD}$) distances, 4 and 9 μm, are shown in Fig. 2.32c. In both cases, the source-to-gate ($L_{SG}$) distance and gate length ($L_G$) are 1.5 μm, and $V_{GS}$ is −20 V. As seen, the 4 and 9 μm devices break down at $V_{DS}$ 850 and 1500 V, respectively, without using any edge termination techniques. This confirms the potential for low defect density Al-rich AlGaN on AlN to be used for power devices. Following the introduction of edge terminations in the future, improvements in performance are expected. In order for AlGaN HEMT technology to truly threaten the GaN HEMT's position in the market, however, the inferior thermal conductivity of AlGaN and ohmic contacts will need to be improved significantly.

## 8 Conclusions

WBG devices have compelling advantages over their Si counterparts and are presently inserted in numerous power applications enabling higher efficiency, smaller form factor, higher power density, and operation at elevated temperatures with simplified circuit topologies and thermal management.

Commercial SiC power devices (diodes, MOSFETs, JFETs, and BJTs) as well as bipolar devices (IGBTs) best suited for +10 kV applications were reviewed. Unipolar SiC devices are commercially available in the 650–1700 V range with the SiC MOSFET being inserted in the vast majority of SiC power applications. SiC MOSFETs have also been demonstrated at 3.3, 6.5, and 10 kV with commercial release coming in the next few years. Above 10 kV, the thick drift layer of MOSFETs becomes highly resistive, and bipolar devices like the SiC IGBT provide a good trade-off between lower conduction and increased switching losses.

Lateral GaN power devices will most probably, with time, dominate applications in the voltage range below 600–1000 V, in particular as GaN-based ICs mature. The low-loss and fast switching speed offered by this platform promises to not only improve performance but also reduce system cost, size, and weight. Despite the many technological advancements in GaN HEMTs over the years, they have not yet fulfilled their predicted performance potential. Multichannel and trigate device configurations are closing the gap, but thermal management remains a key hurdle that must be overcome via efforts in device and materials engineering. Due to the relatively recent introduction of GaN HEMTs to the power electronics market, there remain several opportunities to better understand the mechanisms that determine reliability and robustness in these devices. As time passes and the technology matures, consumer hesitance will dissipate. Vertical GaN technology is also catching up for >1 kV applications. In order for these devices to displace their SiC counterparts, the cost of native GaN substrates must be reduced, drift region doping must be lowered, and efficient selective area doping via ion implantation must be realized.

Barriers to WBG mass commercialization include the higher than silicon device cost, reliability and ruggedness concerns, and the need for a trained workforce to skillfully insert WBG devices into power electronics systems. In many applications, at the system level, WBG-based solutions are at parity or even more cost-effective than those of silicon primarily due to passive component simplifications. WBG devices are rapidly overcoming barriers to system insertion and are entering mass production in volume fabs with its cost-lowering benefits.

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